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High Sensitivity Dual-Gate Four-Terminal Magnetic Sensor Compatible With SOI FinFET Technology

Nebojsa Jankovic, *Senior Member, IEEE*, Olga Kryvchenkova, Steve Batcup, and Petar Igic, *Senior Member, IEEE*

Abstract—This letter presents a novel device concept of split-current magnetic sensor that is fully compatible with silicon-on-insulator (SOI) FinFET technology. The fabricated dual-gate four-terminal device brings a step change in SOI integrated sensor capabilities, and its measured current-related relative sensitivity is as high as $3400\% \text{ T}^{-1}$ at $2 \mu\text{A}$ of total supply current. The device's very high sensitivity is attributed to its novel current conduction phenomena and the internal magnetic deflection enhancement loop demonstrated using 3-D TCAD numerical simulations. This new magnetic sensor is a very promising candidate for the next generation of magnetic sensitive smart-power integrated circuits.

Index Terms—SOI, FinFET, magnetic sensor, split-current, dual gate, IC.

I. INTRODUCTION

THE magnetic sensitive (MS) smart-power integrated circuits (ICs) are used for detecting the position or rotation of magnetized objects [1], [2], portable battery-operated magnetodosimeters [3] and galvanic current sensing for over current protection [4], amongst other various applications. The desire to increase device density (lower cost) and functionality (better signal-to-noise ratio, higher reliability) of the MS ICs requires on-chip integration of the magnetic sensors into the mainstream CMOS technology [5]. Among the innovative CMOS processes [6], a fully depleted (FD) thin silicon film SOI technology with multi-gate transistors (FinFETs) is a leading candidate for the next generation of MS ICs. To date, efforts have been focused on the integration of MagFETs into CMOS processes.

The relative magnetic sensitivity achieved with planar FD SOI MagFETs is typically shown in the range of $S_r \sim 10\text{-}15\% \text{ T}^{-1}$ [7], [8]. Performance of these devices is fundamentally limited by poor mobility of electrons in the

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N. Jankovic is with the Faculty of Electrical and Electronics Engineering, University of Nis, 18000 Nis, Serbia.

O. Kryvchenkova, S. Batcup, and P. Igic are with the College of Engineering, Swansea University, Swansea SA1 8EN, U.K. (e-mail: p.igic@swansea.ac.uk).

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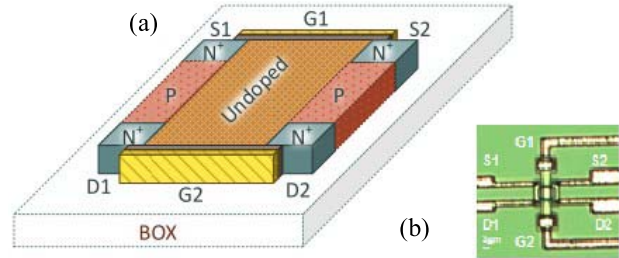


Fig. 1. (a) The 3D schematic of a novel dual-gate four-terminal magnetic sensor realized in FD SOI technology and (b) Microphotograph of a fabricated sensor.

inversion layer [9]. Perin and Giacomini [10] have proposed the L-shaped gate FinFET whose magnetic sensitivity arises from a carrier mobility spatial difference at the front, back and sidewalls interfaces. Using numerical simulations, the relative magnetic sensitivity of FinFET based MagFET was predicted to be $S_r \sim 30\% \text{ T}^{-1}$ [10].

In order to achieve a step change, rather than an increment, in sensitivity performance of an integrated magnetic sensor, a novel device concept is needed. This letter presents fabrication, operation and sensitivity measurements of a newly proposed dual-gate four-terminal magnetic sensor fully compatible with SOI FinFET technology. The fabricated prototypes exhibit very high relative magnetic sensitivity, $S_r > 3000$, at $2 \mu\text{A}$ of total supply current. A substantially increased sensitivity is attributed to current filament conduction with internal magnetic deflection loop, relying on the high mobility of bulk electrons which leads to enhanced current differences at the drain terminals.

II. DEVICE FABRICATION AND OPERATION PRINCIPLE

Microphotograph and 3D schematic of a fabricated magnetic sensor are shown in Fig. 1. A custom defined nine mask two-metal polysilicon gate SOI process was used; key process steps are illustrated and described in Fig. 2. The starting SOI wafer has 500nm thick buried oxide (BOX). A 320nm (100) silicon layer on top of BOX is intrinsic P^- type with a doping concentration of 10^{14} cm^{-3} (Fig. 2(a)). In comparison with standard SOI FinFET technology [11], the fabrication of this novel magnetic sensor requires only one extra masking step for removing the polysilicon gate section above the intrinsic P^- region of the fin area as shown in Fig. 2(d). No additional materials or any micromachining is needed.

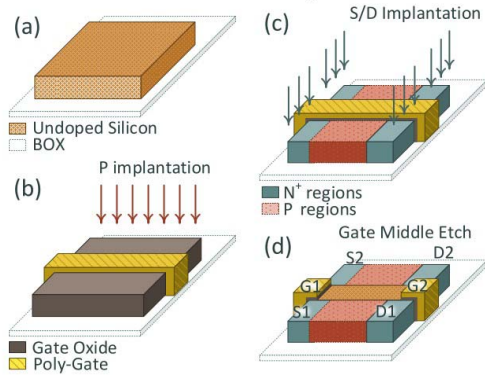


Fig. 2. Basic technology steps of processing the experimental thin-film SOI dual-gate four-terminal magnetic sensor (from top to bottom): (a) defined active area (after etching) in undoped top silicon; (b) P- blank implantation of low boron concentration after gate oxidation and poly-silicon gate definition; (c) through-mask N+ arsenic implantation for source/drain regions; (d) after etching the gate middle region for forming the two sidewall NMOS FETs.

The fabricated dual-gate sensor structure has a large fin area with a size of $5\mu\text{m} \times 9\mu\text{m}$. The polysilicon gates are denoted in Fig. 1(a) as G1 and G2. Gate oxide thickness is 20 nm, and gate regions are $3\mu\text{m}$ long. For the purpose of commonality with FinFET technology, device terminals are named sources (S1 and S2) and drains (D1 and D2), but effectively they act more as emitters and collectors. Their diffused areas are $0.5\mu\text{m}$ long and manufactured using identical N^+ doping with peak concentration of 10^{20}cm^{-3} . Two floating P type areas with doping concentration of $9 \cdot 10^{17}\text{cm}^{-3}$ were created between sources and drains to provide a narrower current filament formation in the middle of the intrinsic region.

To operate the magnetic sensor device, a positive voltage is applied at the gate contacts to create electron channels. Source contacts are kept at 0V. When a positive voltage is applied at the D1 and D2 contacts, the drain electric field spreads throughout the undoped region eventually reaching the G1 channel. It induces the effect of MOS inversion layer carrier injection [12], [13] from the G1 channel creating a current filament of electrons traveling from sources to drains in the undoped bulk region as seen in the 3D device simulation results shown in Fig. 4(b). The formation of the current filament, having a peak electron density along the device's z-axis of symmetry, is caused by a specific saddle-like distribution of potential lines in the undoped region occurring due to the presence of two floating P doped regions shown in Fig. 1. Once it reaches the G2 region, the electron filament splits, forming two equal internal current components, I_{DS1} between S1 and D1 terminals and I_{DS2} between S2 and D2 terminals. When no magnetic field is present, these two currents are identical ($I_{DS1} - I_{DS2} = 0$). The presence of a magnetic field will cause a deflection of electrons in the current filament leading to a current difference, $I_{DS1} - I_{DS2} = \Delta I$. By measuring ΔI one can determine the magnetic field value.

III. MAGNETIC SENSITIVITY TEST, RESULTS AND DISCUSSION

The probe station LA-150 bench-top system by INSETO was used to test the magnetic sensor sensitivity. It has a

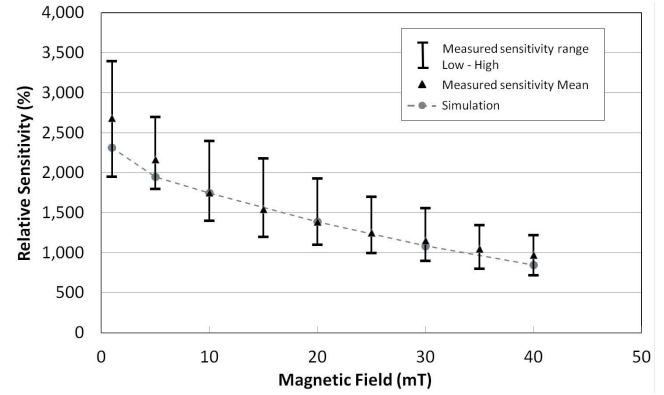


Fig. 3. Measured and simulated dependences of S_r versus $|\vec{B}_y|$ at total drain current $I_D = I_{DS1} + I_{DS2} = 2\mu\text{A}$.

150mm chuck with full x-y-z movement and dual-mode optics for both microscope and digital video viewing. The probe station connects the device under-test to a Keithley 4200-SCS semiconductor characterisation system with 200V/1A DC, pulse and CV measurement capability.

The magnetic field \vec{B}_y perpendicular to a chuck surface was produced by an electromagnet embedded in the chuck plate and level with the chuck surface. By precise control of the coil supply current, the different field intensities $|\vec{B}_y|$ from 0 to 65mT in 5mT steps were generated in-situ and verified using a precise digital magnetometer. Because the coil diameter (2cm) is much larger than the sensor dimension ($5 \times 9\mu\text{m}$), it is justified to assume that the homogenous magnetic field \vec{B}_y was applied over the whole device area.

A common figure of merit of split-current magnetic sensors' performance is current relative sensitivity S_r defined as $S_r = \Delta I_D \cdot (I_D |\vec{B}_y|)^{-1} \cdot 100\%$, where $I_D = I_{DS1} + I_{DS2}$ is the total drain current [1]. Fig. 3 shows the measured S_r versus $|\vec{B}_y|$ extracted from testing a number of devices on the same SOI wafer, as well as simulated S_r . The simulated values were obtained with the industrial standard numerical device simulator Atlas Silvaco [15]. The sensor operation under the influence of perpendicular magnetic field $|\vec{B}_y|$ was analyzed using the MAGNETIC module of ATLAS package taking into account the 3-D influence of Lorentz force on carrier transport. All numerical values of S_r shown in Fig.3 were extracted from the magnetic simulations after tuning the Hall coefficients of charge carriers in Atlas against measured mean sensitivity at $|\vec{B}_y| = 20\text{mT}$.

The biasing conditions of $V_{GS} = 3\text{V}$, $V_{DS1} = V_{DS2} = 1\text{V}$ and I_D in the micro-amperes range were used to find maximum device sensitivity. A very high S_r with a maximum value of over $3000\%T^{-1}$, at very low magnetic fields, is extracted from magnetic sensor measurements as shown in Fig. 3. Table I summarizes the peak values of S_r for split-current magnetic sensors reported so far by other authors [7], [10], [14] for magnetic sensors in thin film FD SOI technologies. The associated total drain currents and layout dimensions of sensors are also shown in Table I, since these parameters are important for the on-chip sensor integration. It is clear from

TABLE I
THE CURRENT RELATED PEAK SENSITIVITY, TOTAL SUPPLY CURRENT AND AREA DIMENSIONS OF SPLIT-CURRENT MAGNETIC SENSORS IN THIN-FILM FD SOI TECHNOLOGY REPORTED BY DIFFERENT AUTHORS

Reference	Peak sensitivity (%T ⁻¹)	Total current (μA)	Area (μm×μm)	Extraction method
Puicun et al [7]	15	10	300×33	experiment
Perin et al [10]	30	100-150	0.55×0.05	simulation
Losantos et al [14]	50	0.1-0.5	60×50	experiment
This work	>3000	2	5×9	experiment

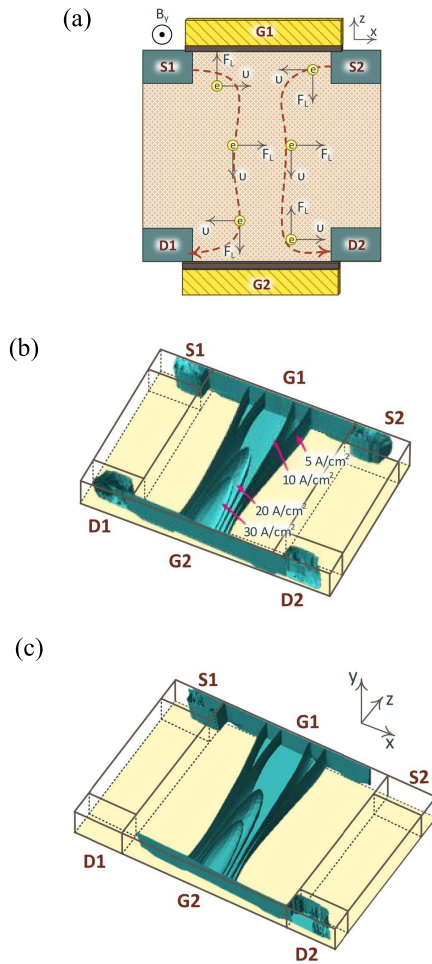


Fig. 4. (a) Directions of Lorentz forces \vec{F}_L and electron velocity \vec{v} depicted in various regions of the novel magnetic sensor structure with respect to equi-lines of electron flux density. A current density distribution in the device at $V_{GS} = 5V$ and $V_{DS} = 3$: the 3D iso-lines extracted for (a) $|\vec{B}_y| = 0$ and (b) $|\vec{B}_y| = 30 mT$ extracted from 3D simulations [15]. Absence of iso-lines in D1 and S2 regions in (b) indicates an occurrence of drain current imbalance $\Delta I_D = I_{D1} - I_{D2} > 0$ for $|\vec{B}_y| = 30 mT$.

presented data that this novel device concept brings a step change in design and performance of the integrated magnetic sensors while maintaining full compatibility with SOI FinFET technology.

The outstanding performance of the fabricated sensor can be attributed to the high mobility of bulk conducted electrons in the current filament and enhanced deflection of electrons caused by the spatial magnetic field influence on 2D current

flow in the 3D device structure, as explained in the text that follows. As a result of the applied magnetic field, $|\vec{B}_y|$, electrons moving along the z direction are deflected by \vec{F}_L toward D2, and hence the drain current difference $\Delta I_D = I_{DS1} - I_{DS2} > 0$ will be induced as illustrated in Fig. 4(a).

Besides this common effect, \vec{F}_L also contributes to the increase of ΔI_D through its influences in the G1 region. Fig.4(a) shows that the S1 injected electrons traveling along the x-axis are pushed toward the G1 inverted channel where they are further transported to the current filament. The S2 injected electrons are directed away by \vec{F}_L from the G1 inverted channel and do not contribute to the peak region of the middle current filament as illustrated in Fig. 4(a). The opposite deflection of electrons injected from S1 and S2 along the x-axis creates a positive magnetic loop, which enhances ΔI_D and improves the sensitivity of the sensor. From the principle of charge neutrality, the increase of I_{D2} and I_{S1} results in a corresponding decrease of I_{D1} and I_{S2} . The latter effect is demonstrated in Figs. 4(b) and 4(c) showing the iso-lines of current densities extracted from 3D simulations of novel dual-gate four-terminal magnetic sensor for $|\vec{B}_y| = 0T$ and $|\vec{B}_y| = 30mT$, respectively. At $|\vec{B}_y| = 0T$ the current density is symmetric (Fig. 4(b)), while at $|\vec{B}_y| = 30mT$ the current density at S2 and D1 is reduced below $5 A/cm^2$ (Fig 4(c)).

IV. CONCLUSIONS

The operation, fabrication and sensitivity measurement of a novel split-current dual-gate four-terminal magnetic sensor that is fully compatible (no extra materials or micromachining needed) with SOI FinFET technology is described. Due to the high mobility of bulk conducted electrons and an internal current deflection enhancement loop, the fabricated prototype of $5\mu m \times 9\mu m$ magnetic sensing device exhibited S_r with a value of over $3000 \% T^{-1}$ at $2\mu A$ of supply current. It is the highest S_r reported among semiconductor integrated sensors fabricated in FD SOI technology, and clearly represents a step change in the integrated magnetic sensors' performance.

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REFERENCES

- [1] H. Konno and H. Kataniwa, "Integrated ferromagnetic MR sensors," *J. Appl. Phys.*, vol. 69, no. 8, pp. 5933–5935, Apr. 1991, doi: <http://dx.doi.org/10.1063/1.347820>.

- [2] D. Draxelmayr and R. Borgschulze, "A self-calibrating Hall sensor IC with direction detection," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1207–1212, Jul. 2003, doi: 10.1109/JSSC.2003.813240.
- [3] P. Malcovati and F. Maloberti, "An integrated microsystem for 3-D magnetic field measurements," *IEEE Trans. Instrum. Meas.*, vol. 49, no. 2, pp. 341–345, Apr. 2000, doi: 10.1109/19.843075.
- [4] T. J. Brauhn, M. Sheng, B. A. Dow, H. Nogawa, and R. D. Lorenz, "Module-integrated GMR-based current sensing for closed-loop control of a motor drive," *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 222–231, Jan. 2017, doi: 10.1109/TIA.2016.2614771.
- [5] H. P. Baltes and R. S. Popovic, "Integrated semiconductor magnetic field sensors," *Proc. IEEE*, vol. 74, no. 8, pp. 1107–1132, Aug. 1986.
- [6] A. B. Sachid, Y.-M. Huang, Y.-J. Chen, C.-C. Chen, D. D. Lu, M.-C. Chen, and C. Hu, "FinFET With encased air-gap spacers for high-performance and low-energy circuits," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 16–19, Jan. 2017, doi: 10.1109/LED.2016.2628768.
- [7] G. Picun and D. Flandre, "Characterization of thin-film SOI split-drain MOS transistors as magnetic sensors," in *Proc. Tenth Int. Symp. Silicon-Insulator Technol. Devices*, Mar. 2001, pp. 289–294.
- [8] D. Flandre, A. Adriaensen, A. Afzalilian, J. Laconte, D. Levacq, C. Renaux, L. Vancaillie, J.-P. Raskin, L. Demeus, P. Delatte, V. Dessard, and G. Picun, "Intelligent SOI CMOS integrated circuits and sensors for heterogeneous environments and applications," in *Proc. SENSORS*, Jun. 2002, pp. 1407–1412, doi: 10.1109/ICSENS.2002.1037327.
- [9] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. Hoboken, NJ, USA: Wiley, 2006.
- [10] A. L. Perin and R. Giacomini, "Sensing magnetic fields in any direction using FinFETs and L-gate FinFETs," in *Proc. IEEE Int. SOI Conf. (SOI)*, Oct. 2012, pp. 1–2, doi: 10.1109/SOI.2012.6404368.
- [11] E. J. Nowak, I. Aller, T. Ludwig, K. Kim, R. V. Joshi, C.-T. Chuang, K. Bernstein, and R. Puri, "Turning silicon on its edge [double gate CMOS/FinFET technology]," *IEEE Circuits Devices Mag.*, vol. 20, no. 1, pp. 20–31, Jan. 2004, doi: 10.1109/MCD.2004.1263404.
- [12] F. Udrea, G. A. J. Amaratunga, J. Humphrey, J. Clark, and A. G. R. Evans, "The MOS inversion layer as a minority carrier injector," *IEEE Electron Device Lett.*, vol. 17, no. 9, pp. 425–427, Sep. 1996.
- [13] N. D. Jankovic, "High-gain emitter inversion layer PNP vertical bipolar transistor in compensated CMOS technology," *Electron. Lett.*, vol. 34, no. 10, pp. 984–985, May 1998.
- [14] P. Losantos, C. Cané, D. Flandre, and J.-P. Eggermont, "Magnetic-field sensor based on a thin-film SOI transistor," *Sens. Actuators A, Phys.*, vol. 67, nos. 1–3, pp. 96–101, May 1998. [Online]. Available: [http://dx.doi.org/10.1016/S0924-4247\(97\)01771-8](http://dx.doi.org/10.1016/S0924-4247(97)01771-8)
- [15] *Atlas User's Manual*, SILVACO International, Santa Clara, CA, USA, 2007.