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Finite Control Set Model Predictive Control for a Matrix Converter with Zero Common-mode Voltage

Abstract: In this paper a finite control set model predictive control method is presented that eliminates the common-mode voltage at the output of a matrix converter. In the predictive control process only the rotating vectors are selected to generate the output voltage and the input current in order to remove the common mode voltage. In addition, a modified four-step commutation strategy is proposed to eliminate common-mode voltage spikes caused by the conventional four-step commutation strategy based on the current direction. The proposed method reduces the computational complexity greatly compared with the enhanced space vector modulation with rotating vectors. The feasibility and operation of the proposed method are verified using experimental results. The resulting common-mode voltage is near to zero with good quality input and output converter waveforms.

Keywords: common-mode voltage, finite control set model predictive control, matrix converters.

1. Introduction

Matrix Converters (MCs) are AC/AC power converters that, unlike conventional AC/DC/AC converters, employ no DC-link energy storage elements [1-2]. This feature provides for more compact, robust, and reliable power converters, and facilitates potential applications in future aircraft and large electric vehicle applications which will use a greater number of electrically driven actuation systems [3-4] and which have requirements for high-temperature operation as well as space and weight restrictions. However, MCs still require further development to address problems such as power quality, operation under abnormal conditions, and common-mode voltage (CMV) [5]. Among these problems, CMV leads to shaft voltage, leakage current, and bearing current damage, which can cause damage to electric motors and reduces the reliability of motor drive systems [6]. CMV and its high electrostatic-coupled discharge or displacement are reported as the main cause of motor failures [7], and also introduce electromagnetic interference (EMI) to the system and its surroundings [8]. Therefore, eliminating CMV in MCs has attracted considerable attention in recent years [9]-[11].

For conventional AC/DC/AC converters, the methods employed to minimize CMV include using isolation transformers, active switching methods, and zero sequence impedance [12]. When using isolation transformers, since the secondary of the isolation transformer in the zero sequence network is floating, the neutral of the motor or WYE point of the output filter capacitors can be grounded through a grounding network or directly if a large enough zero sequence impedance is added in the dc link, and the motor neutral voltage will not lead to any excessive CMV. With active switching methods the CMV is reduced by active pulse-width modulation (PWM) switching methods, but the total harmonic distortion (THD) of the output voltage and switching losses are increased [12]. Using a zero sequence impedance provides a high impedance to common-mode current and eliminates the CMV at the expense of system cost and size. Although the issues with CMV is well known, the problem of CMV for AC drives remains largely unresolved, and potential solutions must consider the specific application and operation conditions of converters [13].

The problem of CMV exists for MCs as well as conventional AC/DC/AC converters, and some methods for the mitigating of CMV have also been developed. Methods for reducing CMV in MCs can generally classified into two types:

- hardware elimination methods

- software reduction methods.

Hardware elimination methods modify the topology of the MC. For example Yue et al. [14] proposed a common-mode canceller, consisting of an H-bridge, a common-mode transformer, an external power source, and an output filter to eliminate CMV. Nath and Mohan [15] utilized a sinusoidal input/output three-winding high-frequency transformer to eliminate CMV. Although hardware methods have been shown to effectively solve the problem of CMV, they invariably result in higher cost and lower power density, which obviously detracts from their applicability.

Software CMV reduction methods typically involve the selection and arrangement of the zero vectors in the modulation process. The proper selection of zero vectors has been shown to lead to a decreased level of CMV [16]-[20]. However, rather than zero vectors, two active vectors producing reverse effects have also been employed to reduce CMV [21]-[23]. Nguyen and Lee [24] synthesized the reference output voltage vector using three couples of nearest active space vectors to reduce CMV. Guan et al. [9] achieved a reduction in CMV using the switching configurations (SCs) that connect each input phase to a different output phase, or the SC that connects all the output phases to the same input phase with minimum absolute voltage.

While these software methods can reduce CMV to a great extent, they cannot eliminate CMV completely. Hence, an enhanced space vector modulation (SVM) method has been presented to fully eliminate CMV using rotating vectors [10]. However, this approach introduces some noise in practical applications when using the conventional four-step commutation strategy. To solve this problem, a modified four-step commutation strategy [25] was proposed to eliminate CMV spikes for MCs. However, the complex computation of the optimal duty cycle required by this strategy is difficult to implement. As an alternative method for CMV elimination, model predictive control (MPC) using a cost function has been explored due to advantages such as the easy inclusion of system nonlinearities and constraints as well as the flexibility for including other system requirements in the controller [26]-[28]. A cost function has been used which included information regarding load current, input reactive power, and CMV [29]. Vargas et al. [30] proposed a predictive scheme for an induction motor control with a cost function that included information regarding torque, flux magnitude, input reactive power, and CMV. Rivera et al. [31] proposed a MPC method for an indirect matrix converter including load current, source current, and CMV information in the cost function. Those works have shown that employing a sufficiently large CMV weight factor in the cost function can

ensure an effective reduction of CMV. However, they cannot eliminate CMV completely also. And, all the possible SCs are included in the finite control set and the computational burden of these approaches is large [29]-[31]. In addition, those studies have not considered the effect of dead time, where the switching between two states requires a finite dead time to avoid commutation failure, which inevitably produces CMV spikes in practical applications.

This paper presents a novel simplified MPC method for eliminating the CMV in the output voltages of direct MCs (DMCs). Like H. N. Nguyen did in [10], only the six rotating vectors generating zero CMV are selected in our proposed method. A simplified MPC method is proposed to select the best SC to be applied for the following time interval in this paper while a very complex enhanced space vector modulation (SVM) method is applied for using the rotating vectors in a repetitive pattern in [10]. To decrease the computational burden further and avoid the difficulty to adjust multi weight factors, a simple evaluation criterion, which needs no CMV information, is proposed to determine the most suitable SC. The proposed method eliminates CMV by selecting only those six SCs that produce zero CMV, rather than using all the possible 27 SCs and including CMV information in the cost function as did in [29-30]. The computational effort is largely reduced. The evaluation criterion focuses solely on the source current and the load current for good input and output performance and avoids coupling effects. The final CMV value over a period can be theoretically eliminated due to the selection of these specific SCs. In addition, a modified four-step current commutation is applied to eliminate the dead-time effect, which results in greatly reduced spikes. The performance of the proposed method is experimentally verified.

2. Cause and elimination of CMV for DMCs

2.1 Cause of CMV

As shown in Fig. 1, a DMC consists of 3*3 matrix bidirectional switches, which typically connects a three-phase voltage source to a three-phase inductive load. A filter is used at the input of the matrix converters to reduce the switching frequency harmonics present in the input current. Theoretically, an AC voltage of arbitrary frequency can be synthesized by switching among the nine bidirectional switches. There are 27 possible SCs to satisfy the two main rules in a DMC: 1) no open circuit for the inductive load current, and 2) no short circuit for the voltage source. The 27 allowable SCs are listed in Table I, where u_{eil} ($i, l \in \{a, b, c\}, i \neq l$) represents the line-to-line input voltage. The CMV (i.e., V_{com}) is defined as one-third of the total value

of the three output phase voltages.

$$V_{CMV} = \frac{u_{oA}+u_{oB}+u_{oC}}{3} \quad (1)$$

The input voltages are assumed to be symmetrical. The CMV value of each allowable SC is also listed in Table I. Based on the listed CMV values, all 27 SCs are classified into the following three sets.

(1) Set I (State Nos. 1–18): Any two of the three output phases are connected to the same input phase, and the generated CMV is a variable with a maximum value $V_P/\sqrt{3}$, where V_P is the peak value of the input phase voltage.

(2) Set II (State Nos. 19–21): All three output phases are connected to the same input phase, and the generated CMV is variable with a maximum value V_P.

(3) Set III (State Nos. 22–27): The three output phases are respectively connected to different input phases, and the generated CMV is zero.

From the above classification of SCs, we see that the use of SCs from set I or II will generate a corresponding CMV. In most modulation strategies for DMCs, such as the often used SVM method, the modulation objective is more easily realized when adopting SCs from set I or II than those from set III; meanwhile, the development is simpler. Therefore, sets I and II are usually considered, and set III is usually excluded, in most modulation strategies for DMCs. That's the main reason of CMV in DMCs.

Though in most modulation strategies for DMCs, it is more difficult to control the DMC with the SCs from set III than those from set I and II, all the valid SCs can be employed in the same simple way for the MPC. And MPC has demonstrated to offer a very simple and effective alternative to classical control algorithms with Pulse Width Modulation (PWM) for the control of power converters [26][33]. Based on the above considerations, we propose a simplified finite control set model predictive control (FCS-MPC) method using SCs selected only from set III to exploit the zero-CMV, and to avoid a complicated modulation strategy design.

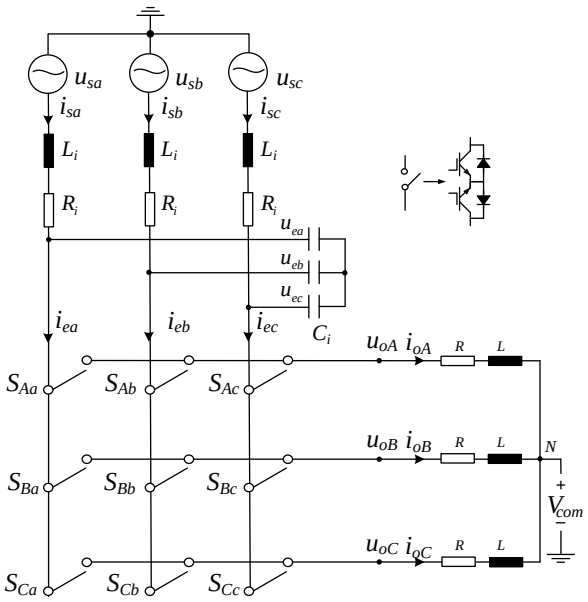


Fig. 1. The topology of a direct matrix converter.

Table I

The INSTANTANEOUS CMV WITH DIFFERENT SWITCHING CONFIGURATIONS

NO.	Switching configurations	CMV	NO.	Switching configurations	CMV
1	a b b	$u_{ebc}/3$	15	c c b	$u_{eca}/3$
2	b a a	$u_{eac}/3$	16	b b c	$u_{eba}/3$
3	b c c	$u_{eca}/3$	17	a a c	$u_{eab}/3$
4	c b b	$u_{eba}/3$	18	c c a	$u_{ecb}/3$
5	c a a	$u_{eab}/3$	19	a a a	u_{ea}
6	a c c	$u_{ecb}/3$	20	b b b	u_{eb}
7	b a b	$u_{ebc}/3$	21	c c c	u_{ec}
8	a b a	$u_{eac}/3$	22	a b c	0
9	c b c	$u_{eca}/3$	23	a c b	0
10	b c b	$u_{eba}/3$	24	c a b	0
11	a c a	$u_{eab}/3$	25	b a c	0
12	c a c	$u_{ecb}/3$	26	b c a	0
13	b b a	$u_{ebc}/3$	27	c b a	0
14	a a b	$u_{eac}/3$			

2.2 Method for eliminating CMV

In order to introduce the proposed simplified FCS-MPC method to reduce CMV in a DMC, it is necessary to present the operating principle of a DMC. The power circuit of the system considered can be observed in Fig. 1. The balanced operation is assumed. The relationship between the input and the output can be expressed as:

$$\begin{bmatrix} u_{oA} \\ u_{oB} \\ u_{oC} \end{bmatrix} = S \begin{bmatrix} u_{ea} \\ u_{eb} \\ u_{ec} \end{bmatrix} \tag{2}$$

$$\begin{bmatrix} i_{ea} \\ i_{eb} \\ i_{ec} \end{bmatrix} = S^T \begin{bmatrix} i_{oA} \\ i_{oB} \\ i_{oC} \end{bmatrix} \tag{3}$$

$$S = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \tag{4}$$

where, u_{oj} ($j \in \{A, B, C\}$), u_{el} ($l \in \{a, b, c\}$), i_{el} ($l \in \{a, b, c\}$), and i_{oj} ($j \in \{A, B, C\}$) represent the output voltage, the input voltage, the input current, and the load current, respectively, and S is the switching function matrix and S_{Xy} ($X \in \{A, B, C\}$, $y \in \{a, b, c\}$) is the switching function of a single switch. S_{Xy} =1 implies that the switch S_{Xy} is on, closed or conduction, and S_{Xy} =0 implies that S_{Xy} is off, open or blocking. As mentioned before, 27 SCs are valid as listed in Table I. However, in order to obtain zero CMV, only the SCs from set III are selected in the proposed method. The selection of the SC to be set at the following time interval is performed via a cost function minimization. For the computation of this cost function, certain variables are predicted based on models. In this case, the load current i_o and the source current i_s at the next sampling interval are predicted for each SC with the aid of a mathematical model of the load and the input filter, respectively.

1) Model of the load

The *RL* load mathematical model can be expressed as

$$L\frac{di_o}{dt} = u_o - Ri_o \tag{5}$$

where L and R are the load inductance and resistance, respectively, u_o is the DMC output phase voltage and i_o is the load current.

Applying a sampling period T_s, the derivative form di_o/dt can be approximated by

$$\frac{di_o}{dt} \approx \frac{i_o^k - i_o^{k-1}}{T_S} \tag{6}$$

where i_o^k and i_o^{k-1} are the load currents at time T_S^k and T_S^{k-1}, respectively.

Replacing (6) in (5) and shifting the discrete time one step forward, the relation between the discrete-time variables can be described as

$$i_o^{k+1} = \frac{T_S}{L} u_o^k + \left(1 - \frac{T_S R}{L}\right) i_o^k \tag{7}$$

where u_o^k are the output voltage vector at time T_S^k under the case of the newest switching configuration.

Equation (7) is used to obtain predictions for the future value of the load current i_o^{k+1} for each voltage vector u_o^k generated by SCs from set III. The corresponding voltage vector u_o^k for each SC can be calculated by means of (2).

2) Model of the input filter

As indicated in Fig. 1, the input filter is related to the source voltage u_s, input voltage u_e, source current i_s, and input current i_e. The mathematical model of the input filter can be expressed as:

$$L_i \frac{di_s}{dt} = u_s - u_e - R_i i_s \tag{8}$$

$$C_i \frac{du_e}{dt} = i_s - i_e \tag{9}$$

where R_i and L_i represent the total resistance and inductance of the line and the input filter, respectively, and C_i represents the input filter capacitance. Equations (8) and (9) can be given in the form of the following state-space equation.

$$\begin{bmatrix} du_e/dt \\ di_s/dt \end{bmatrix} = A \begin{bmatrix} u_e \\ i_s \end{bmatrix} + B \begin{bmatrix} u_s \\ i_e \end{bmatrix} \tag{10}$$

$$A = \begin{bmatrix} 0 & 1/C_i \\ -1/L_i & -R_i/L_i \end{bmatrix}, B = \begin{bmatrix} 0 & -1/C_i \\ 1/L_i & 0 \end{bmatrix} \tag{11}$$

Using a forward Euler approximation, a discrete state-space model can be derived when a zero-order hold input is applied to a continuous-time system. Applying a sampling period T_S, the discrete-time system derived from (10) is

$$\begin{bmatrix} u_e^{k+1} \\ i_s^{k+1} \end{bmatrix} = e^{AT_s} \begin{bmatrix} u_e^k \\ i_s^k \end{bmatrix} + A^{-1}(e^{AT_s} - I)B \begin{bmatrix} u_s^k \\ i_e^k \end{bmatrix} \tag{12}$$

where u_e^{k+1} and i_s^{k+1} are the predicted values of u_e and i_s at time T_S^{k+1}, respectively, u_e^k, u_s^k and i_s^k are the measured values of u_e, u_s and i_s at time T_S^k. Equation (12) is used to obtain predictions for the future values of i_s^{k+1} for each i_e^k generated by valid SCs. i_e^k for each SC from set III can be calculated by means of (2).

Equations (7) and (12) together compose the prediction model. They can be rewritten:

$$\begin{cases} u_e^{k+1} = X_1 u_s^k + X_2 u_e^k + X_3 i_s^k + X_4 i_e^k \\ i_s^{k+1} = Y_1 u_s^k + Y_2 u_e^k + Y_3 i_s^k + Y_4 i_e^k \\ i_o^{k+1} = Z_1 u_o^k + Z_2 i_o^k \end{cases} \tag{13}$$

where X_1, X_2, X_3, X_4, Y_1, Y_2, Y_3, and Y_4 depend on R_i, L_i, C_i, and T_S, and Z_1 and Z_2 depend on R, L, and T_S.

3）Cost function

The selection of the optimal SC to be set at the following time interval is performed via a cost function evaluation. The cost function definition is one of the most important stages in the design of the MPC, since it allows to select the variables to be optimized. For the DMC in this paper, the objectives can be summarized as follow:

- The load currents accurately follow the reference values.
- The converter runs with unity power factor. In other words, the source currents accurately follow the reference value.
- The CMV is eliminated to zero.

Since zero CMV is naturally satisfied in theory by using only the SCs from set III, the variables to be optimized here are the load and source currents. So only a combination of a load current error and a source current error is considered in constructing the cost function, which reflects the first and the second control objectives of the DMC.

The error between the predicted load currents and its references can be expressed as:

$$\Delta i_o = i_o^p - i_o^* \tag{14}$$

where Δi_o, i_o^p and i_o^* are the current error, the predicted current and the current reference of the load. i_o^p is calculated by means of (13). And i_o^* is determined according to the control objective.

The error between the predicted source currents and its references can be expressed as:

$$\Delta i_s = i_s^p - i_s^* \tag{15}$$

where Δi_s, i_s^p and i_s^* are the current error, the predicted current and the current reference of the source. i_s^p is calculated by means of (13). The reference value of the source current i_s^* can be given by:

$$i_s^* = [I_{sm}^* cos\varphi \quad I_{sm}^* cos(\varphi - 2\pi/3) \quad I_{sm}^* cos(\varphi + 2\pi/3)] \tag{16}$$

where I_{sm}^* is the amplitude of the expected source current, which is determined by the active power flow, and φ is the angle of u_s, which can be obtained through the measured line voltages u_{sab}, and u_{sbc}. The input active power P_{in} and the output active power P_o can be calculated as:

$$P_o = \frac{3}{2} {I_{om}^*}^2 R \tag{17}$$

$$P_{in} = \frac{3}{2}\left(U_{sm} I_{sm}^* cos\theta - {I_{sm}^*}^2 R_i\right) \tag{18}$$

$$\eta = \frac{P_o}{P_{in}} \tag{19}$$

Here, I_{om}^* and U_{sm} are the amplitude of the reference load current and the source phase voltage, respectively, θ is the phase difference between the source phase voltage and the source phase current, and η is the efficiency of the converter. To achieve unity power factor, θ is set to zero. Hence, the amplitude of I_{sm}^* is determined:

$$I_{sm}^* = \frac{\eta U_{sm} \pm \sqrt{\left(\eta U_{sm}\right)^2 - 4\eta R_i R {I_{om}^*}^2}}{2\eta R_i} \tag{20}$$

Putting (20) in (16), i_s^* can be obtained. Combining (15) and (16), the source current error between its prediction i_s^p and its reference i_s^* can be calculated.

Then a cost function is constructed as:

$$g = \left(\Delta i_{o\alpha}^2 + \Delta i_{o\beta}^2\right) + \lambda\left(\Delta i_{s\alpha}^2 + \Delta i_{s\beta}^2\right) \tag{21}$$

where $\Delta i_{o\alpha}$, $\Delta i_{o\beta}$, $\Delta i_{s\alpha}$, and $\Delta i_{s\beta}$ are the real and imaginary parts of the load and the source current errors, which are transformed from static three-phase coordinates to static two-phase coordinates. And λ is the weighting factor that handles the relation between the source and load conditions and determines the priority of the source current compared with the load current, which is flexibly adjusted in response to different control requirements.

The predictions i_o^p and i_s^p under the case of each SC from set III are then evaluated so that the optimal SC, which minimizes the cost function g, is applied to the converter in the next period interval. The specific implementation steps are as

follows:

(a) In the k^{th} sampling period T_S^k, the newest SC is put into effect, and u_s^k, i_s^k, u_e^k, and i_o^k are measured, and the switching function matrix S^k in T_S^k are recorded. For initiation, S^0 can be set as:

$$S^0 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{22}$$

(b) Based on the measured values u_e^k and i_o^k together with S^k, u_o^k and i_e^k are calculated by (2) and (3), respectively.

(c) Based on the measured values u_s^k, i_s^k, u_e^k, and i_o^k got in step (a) and the calculated values u_o^k and i_e^k got in step (b), the predicted values u_e^{k+1}, i_s^{k+1} and i_o^{k+1} in the next sampling period T_S^{k+1} are obtained by means of (13).

(d) Then, based on the $(k+1)^{th}$ predicted values u_e^{k+1} and i_o^{k+1}, the predicted u_o^{k+1} and i_e^{k+1} for each SC from set III are calculated by (2) and (3), respectively.

(e) u_s^{k+1} is obtained as following:

$$u_s^{k+1} = [U_{sm}cos\varphi^{k+1} \qquad U_{sm}cos(\varphi^{k+1} - 2\pi/3) \qquad U_{sm}cos(\varphi^{k+1} + 2\pi/3)] \tag{23}$$

where φ^{k+1} is the phase angle of the source voltage at time T_S^{k+1}, which can be calculated as

$$\varphi^{k+1} = \varphi^k + 100\pi T_S \tag{24}$$

And φ^k is the phase angle of the source voltage at time T_S^k, which can be calculated through the measured source voltages u_{sab}^k and u_{sbc}^k at time T_S^k.

(f) Based on u_e^{k+1}, i_s^{k+1}, i_o^{k+1} and u_s^{k+1}, which are respectively obtained from step (c) and (e) , and six pairs u_o^{k+1} and i_e^{k+1} from six SCs, which are obtain in step (d), the corresponding predicted values i_o^{k+2} and i_s^{k+2} in the next sampling period T_S^{k+2} are further obtained by means of (13).

(g) Substituting the predicted values i_o^{k+2} and i_s^{k+2} from each SC into (21), g^{k+2} can be obtained for each SC. The SC, which obtains the minimum g^{k+2} is the best choice in T_S^{k+1}.

Since only six elements are contained in the finite control set, and the cost function only includes a combination of a load current error and a source current error, the above steps are denoted herein as the simplified FCS-MPC method.

3. Modified four-step current-based commutation

In practice, the FCS-MPS method alone cannot fully eliminate the CMV of a DMC. Due to the multi-switching characteristic of DMCs, the switching between two states requires a finite dead time to avoid commutation failure. Due to the dead time, the proposed predictive strategy cannot effectively control the CMV value when the switches commutate from one state to another, and CMV spikes are inevitably obtained in the conventional four-step commutation process [32]. Therefore, a modified four-step commutation process is proposed in this paper to solve this problem.

Fig. 2(a) presents a simplified circuit when the current commutates from S_{Aa} (i.e., S_{Aap} and S_{Aan}) to S_{Ab} (i.e., S_{Abp} and S_{Abn}), where S_{ijp} and S_{ijn} ($i = A, B, C$; $j = a, b, c$) are the two quadrant switches contained in S_{ij}. The corresponding switching process for conventional four-step current-based commutation is shown in Fig. 2(b). The commutation relies on the current direction information of i_{oA}. The following four-step switching principle is adopted for $i_{oA} > 0$:

Step 1 (S1): turn off S_{Aan};

Step 2 (S2): turn on S_{Abp};

Step 3 (S3): turn off S_{Aap};

Step 4 (S4): turn on S_{Abn}.

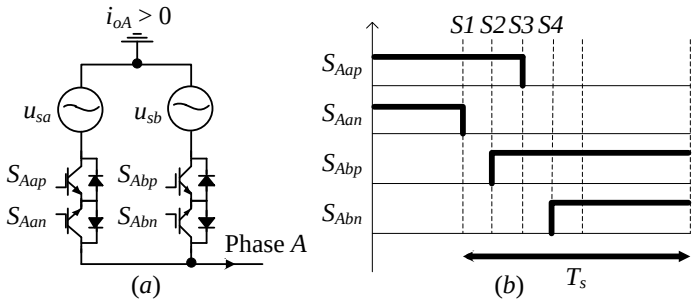


Fig. 2. (a) A simplified DMC for explaining the switching principle of conventional four-step current-based commutation. (b) The switching process for conventional four-step current-based commutation, where S1–S4 represent the four switching steps given in Section 3.

The commutation time for a single step is denoted as t_d. On the basis of conventional four-step current-based commutation, a simplified DMC for the switching configuration commutating from “abc” to “bac” is shown in Fig. 3(a). The corresponding

switching process for conventional four-step current-based commutation is given in Fig. 3(b). The commutation of load current i_{oA} is forced, and occurs in the second step of conventional four-step current-based commutation. The commutation of load current i_{oB} is natural, and occurs in the first step of conventional four-step current-based commutation. Thus, the commutations for load currents i_{oA} and i_{oB} are not simultaneous. Rotating vectors are selected in the processes of steps 1, 3, and 4, but the non-rotating vector "aac" appears in the process of step 2, which results in a nonzero CMV. Thus, the CMV is not always equal to zero in a switching period.

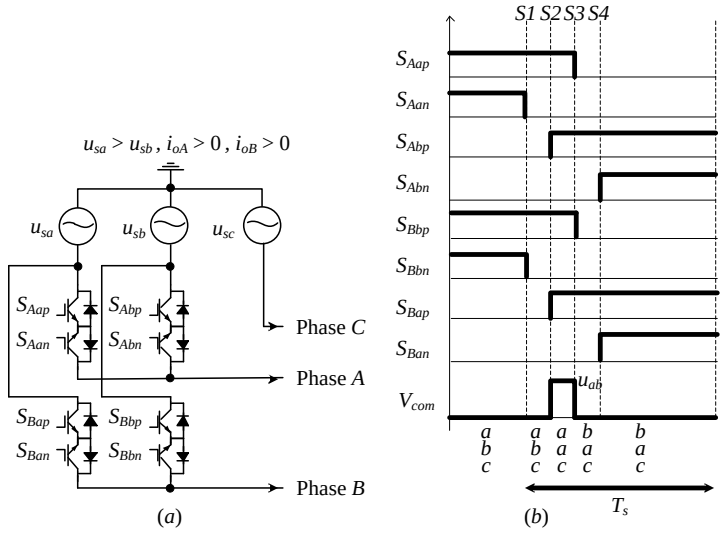


Fig. 3. (a) A simplified DMC describing the switching configuration commutating from "abc" to "bac".
(b) The switching process of conventional four-step current-based commutation and the value of CMV (V_{com}) obtained during commutation.

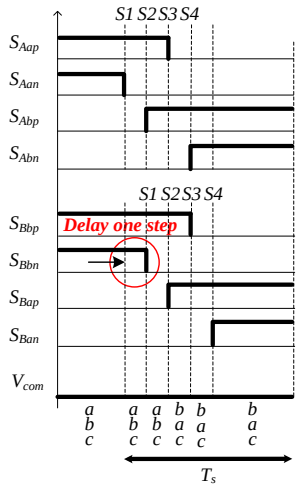


Fig. 4. The switching process from "abc" to "bac" corresponding to the simplified DMC in Fig. 3(a) for the modified four-step current-based commutation, and the value of CMV obtained during commutation.

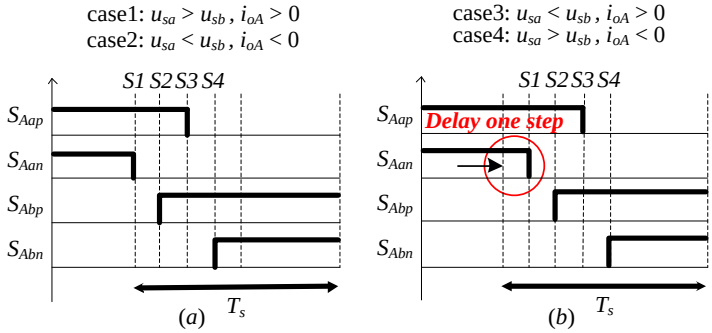


Fig. 5. The generalized switching process of the modified four-step current-based commutation in the four possible cases involving u_{sa}, u_{sb}, and i_{oA}: (a) forced commutation; (b) natural commutation.

To achieve zero CMV, a modified four-step current-based commutation is proposed. The method intentionally delays the natural commutation of i_{oB} in the first step of conventional four-step current-based commutation so that it occurs simultaneously with the forced commutation of i_{oA} in the second step of conventional four-step current-based commutation. The switching process of the proposed modified four-step current-based commutation is illustrated in Fig. 4 based on the simplified DMC shown in Fig. 3(a), where, again, the switching configuration commutates from "abc" to "bac". As observed, the CMV is zero over T_Ss. Thus, the generalized switching process for the modified four-step current-based commutation in the four possible cases involving u_{sa}, u_{sb}, and i_{oA} is given in Fig. 5. For cases 1 and 2 involving forced commutations, the

switching processes are equivalent with conventional four-step current-based commutation. However, for cases 3 and 4 involving natural commutations, the switching processes are delayed t_d compared with those of conventional four-step current-based commutation.

4. Experimental results

In this section, based on the specifications listed in Table III, the operation and performance of the proposed simplified FCS-MPC method were validated experimentally. As comparison, the experimental performance of an ordinary FCS-MPC method is also given. The ordinary FCS-MPC method here refers to the one, in which all 27 possible SCs are considered. The same cost function is used for the ordinary FCS-MPC method and the proposed simplified FCS-MPC method. The experimental setup was developed using a floating-point digital signal controller (DSP; TMS320F28335, Texas Instruments) and a field programmable gate array (FPGA; EP2C8T144C8N, Altera Corp.).

Table II

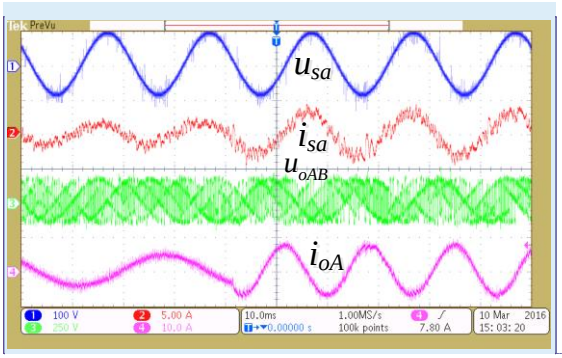
SPECIFICATIONS OF THE EXPERIMENTAL SETUP

Parameters	Value
Supply phase RMS voltage $\boldsymbol{U_s}$ (V)	60
Supply frequency $\boldsymbol{f_{in}}$ (Hz)	50
Inductance of the line and the input filter $\boldsymbol{L_i}$ (mH)	0.6
Resistance of the line and the input filter $\boldsymbol{R_i}$ (Ω)	0.1
Input filter capacitance $\boldsymbol{C_i}$ (μF)	6.6
Input filter damping resistance $\boldsymbol{R_P}$ (Ω)	9
Load resistance $\boldsymbol{R}$ (Ω)	4.4
Load inductance $\boldsymbol{L}$ (mH)	6
Sampling period $\boldsymbol{T_S}$ (μs)	70

The parameter λ in the cost function (21) are empirically adjusted. It can be adjusted from a large value, for example 2, in order to prioritise the control of the source current. Later, it is slowly reduced, aiming to obtain low current THD both at the input and output sides. For the presented experimental results, 0.5 is set for λ.

Fig. 6 shows the experimental waveforms of the source voltage u_{sa}, source current i_{sa}, output line-to-line voltage u_{oAB}, and load current i_{oA} when the DMC is operating under the proposed simplified FCS-MPC method with a reference load current set from 5A@30Hz to 8A@60Hz. The load current tracks the reference current over several sampling periods, and is seen to

be sinusoidal with low distortions.

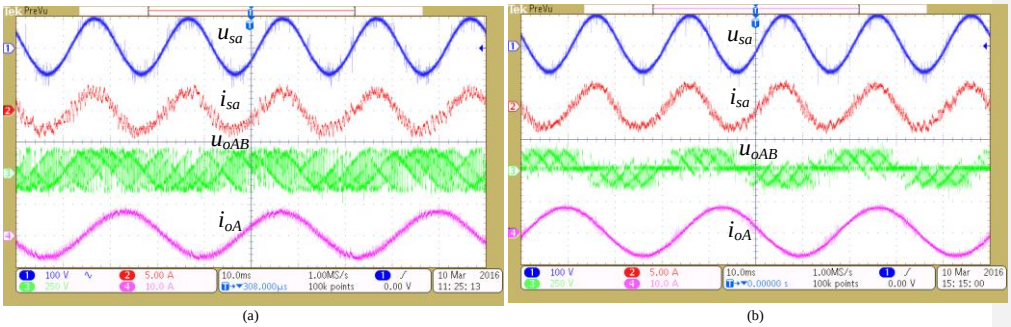


Commented [WP1]: I would prefer to see these presented with roper axis with labels rather than as a scope screen short – this can be done with a simple edit of the picture,

Commented [l2]: We didn't save waveform data. It's not convenient to do these experiments at present since Dan Hanbing who did the experiments are at PEMC in Nottingham now.

Fig. 6. Experimental results under normal conditions with the reference load current set from 5A@30Hz to 8A@60Hz

Figs. 7(a) and (b) show the input and output experimental waveforms with a reference load current of 8A@30Hz under the ordinary and the proposed simplified FCS-MPC methods, respectively. As shown, the waveforms of i_{sa} are in phase with those of u_{sa}, and a unity power factor is obtained. Simultaneously, i_{oA} accurately follows the reference. The THD values of i_{sa} and i_{oA} obtained in the experiment are listed in Table III for reference load currents of 5A@30Hz and 8A@60Hz. From the u_{oAB} waveforms, we observe that the valid SCs of the proposed FCS-MPC method are reduced relative to those of the ordinary FCS-MPC method. The THD values for i_{sa} and i_{oA} obtained under the proposed FCS-MPC method are a bit greater than those of the ordinary FCS-MPC method. The computation times required by the ordinary and the proposed FCS-MPC methods are compared in Fig. 8. The computational time of the proposed method is only 24.97 μs, which is less than the 62.1 μs required for the ordinary method, therefore it is appropriate for the proposed method to be used in higher switching frequency applications. Higher switching frequency benefits to the performance of an MPC.



(a) (b)

Fig. 7. Input and output experimental waveforms with a reference load current of 8 A and 30 Hz: (a) the ordinary FCS-MPC

method; (b) the proposed FCS-MPC method.

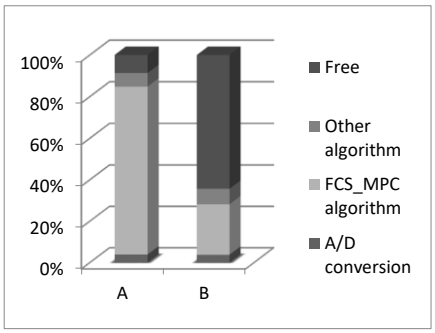


Fig. 8. Comparison between required running times for Algorithm A: the ordinary FCS-MPC method, and Algorithm B: the proposed simplified FCS-MPC method.

Table III

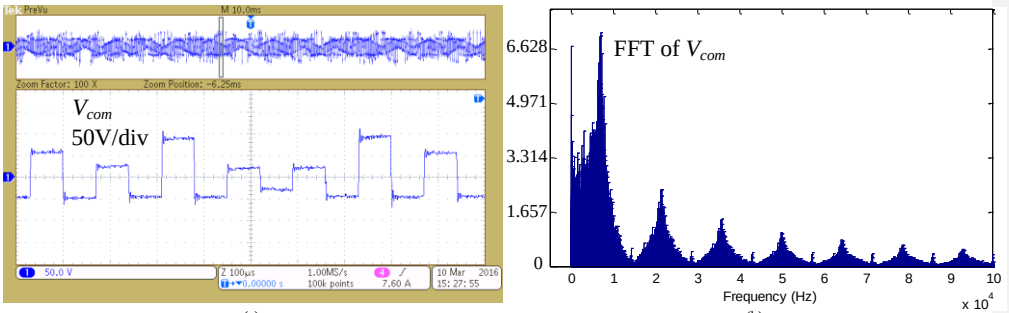
THD VALUES OF THE SOURCE CURRENT AND THE LOAD CURRENT

THD (%)	Cases (8A, 30Hz,)		Cases (8A, 60Hz,)	
	Ordinary	Proposed	Ordinary	Proposed
i_{sa}	15	19.85	14.7	18.41
i_{oA}	4.04	6.75	2.83	5.04

Fig. 9(a) and Fig. 10(a) show the CMV waveforms with a reference load current of 8A@60Hz under the ordinary and proposed FCS-MPC methods, respectively. The root mean square (RMS) value of the CMV is calculated as

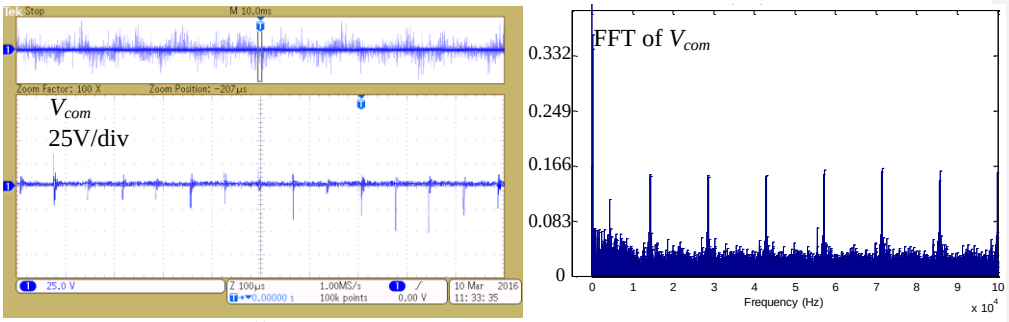
$$V_{comRMS} = \sqrt{\frac{\sum_{1}^{n} V_{com}^2(n)}{n}} \tag{25}$$

For the computation of V_{comRMS}, 100,000 points were sampled using an oscilloscope (DPO3014, Tektronix) with a sampling frequency of 1 MHz, i.e., n = 100,000. The values of V_{comRMS} obtained for the ordinary and proposed FCS-MPC methods are 46.13 V and 3.29 V, respectively. Thus, the proposed FCS-MPC method reduced V_{comRMS} to nearly zero, and is far less than the V_{comRMS} value obtained with the ordinary method. However, some CMV spikes are observed with the proposed method during the turning-on and turning-off switching times, as shown by the Fast Fourier transform (FFT) data presented in Fig. 10(b), due to the non-ideal switching characteristics of the semiconductor switches. However these are significantly smaller than the results without the proposed methods.



(a) (b)

Fig. 9. CMV under ordinary FCS-MPC with the reference load current 8A/30Hz



(a) (b)

Fig. 10. CMV under proposed FCS-MPC with the reference load current 8A/30Hz

5. Conclusion

This paper proposes a simplified zero CMV FCS-MPC method that considers the dead-time effect as well as the modulation process. The proposed method is simple to implement, and employs no complex calculations. In the example given in this paper the proposed method has a computational time of only 24.97µs, while that required for the ordinary FCS-MPC method is 62.5µs. Moreover, the CMV was reduced nearly to zero, and good source and load currents were obtained. Experimental results have been presented to validate the proposed method and demonstrate the advantages.

6. References

1. P. Wheeler, J. Rodriguez, J. Clare, L. Empringham, and A. Weinstein, "Matrix converters: A technology review", *IEEE Trans. Ind. Electron*., vol. 49, no. 2, pp. 276-288, 2002.

2. T. Friedli, J.W. Kolar, J. Rodriguez, P.W. Wheeler, "Comparative evaluation of three-phase AC-AC matrix converter and voltage dc-link back-to-back converter systems", *IEEE Trans. Ind. Electron*., vol. 59, no. 12, pp. 4487-4510, 2012.

3. E. Yamamoto, H. Hara, T. Uchino, M. Kawaji, T.J. Kume, J.K. Kang, H.-P. Krug, "Development of MCs and its applications in industry", *IEEE Trans. Ind. Electron*., vol. 5, no. 1, pp. 4-12, 2011.

4. M. Aten, G. Tower, C. Whitley, P. Wheeler, J. Clare, and K. Bradley, "Reliability comparison of matrix and other converter topologies" *IEEE Trans. Aerosp. Electron. Syst*., vol. 42, no. 3, pp. 867–875, Jul. 2006.

5. J.W. Kolar, T. Friedli, J. Rodriguez, P.W. Wheeler, "Review of three phase PWM AC–AC converter topologies", *IEEE Trans. Ind. Electron*., vol. 58, no. 11, pp. 4988–5006, 2011.

6. S. Chen, T.A. Lipo, D. Fitzgerald, "Source of induction motor bearing currents caused by PWM inverters", *IEEE Trans. Energy Convers*., vol. 11, no. 1, pp. 25–32, 1996.

7. J.M. Erdman, R.J. Kerkman, D.W. Schlegel, G.L. Skibinski, "Effect of PWM inverters on AC motor bearing currents and shaft voltages", *IEEE Trans. Ind. Appl*., vol. 32, no. 2, pp. 250–259, 1996.

8. J. K. Kang, T. Kume, H. Hara, E. Yamamoto, "Common-mode voltage characteristics of matrix converter-driven AC machines", *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005. IEEE*, 2005, vol. 4, pp. 2382-2387.

9. Q. X. Guan, P. Wheeler, Q. S. Guan, and P. Yang, "Common-mode voltage reduction for matrix converters using all valid switch states", *IEEE Transactions on Power Electronics*, vol. pp, no. 99, pp: 1, 2016.

10. H. Nguyen, H. Lee, "An Enhanced SVM Method to Drive Matrix Converters for Zero Common-Mode Voltage", *IEEE Trans. Power Electrons.*, vol. 30, no. 4, pp. 1788-1792, 2015.

11. T. Peng, H. Dan, J. Yang *et al*.: "Open-switch fault diagnosis and fault tolerant for matrix converter with finite control set-model predictive control", IEEE Trans. Ind. Electron., 2016, 63, (9), pp. 5953-5863.

12. S. Wei, N. Zargari, B. Wu, S. Rizzo, "Comparison and mitigation of common mode voltage in power converter topologies", *Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE*, 2004, vol. 3, pp. 1852-1857.

13. M. Jussila, J. Alahuhtala, H. Tuusa, "Common-Mode Voltages of Space-Vector Modulated Matrix Converters Compared to Three-Level Voltage Source Inverter", *Power Electronics Specialists Conference*, 2006. PESC '06. 37th IEEE, 2006, pp. 1-7.

14. F. Yue, P.W. Wheeler, J. Clare, "Cancellation of 3rd common mode voltage generated by matrix converter", *Industrial Electronics Society*, 2005. IECON 2005. 31st Annual Conference of IEEE. IEEE, 2005, vol. 6, pp. 1217-1222.

15. S. Nath, N. Mohan, "A matrix converter fed sinusoidal input output three winding high frequency transformer with zero common mode voltage", *Power Engineering, Energy and Electrical Drives (POWERENG)*, 2011 International Conference on. IEEE, 2011, pp. 1-6.

16. H.H. Lee, H.M. Nguyen, "An effective direct-SVM method for matrix converters operating with low-voltage transfer ratio", *IEEE Trans. Power Electron*., vol. 28, no. 2, pp. 920-929, 2013.

17. C. Ortega, A. Arias, C. Caruana, M. Apap, "Reduction of the common mode voltage of a matrix converter fed direct torque control", *IEICE Electron*., vol. 7, no. 14, pp. 1044–1050, 2010.

18. C. Ortega, A. Arias, C. Caruana, "Common mode voltage in DTC drives using matrix converters", *Electronics, Circuits and Systems, 2008. ICECS 2008. 15th IEEE International Conference on. IEEE*, 2008, pp. 738-741.

19. L. Hua, H. Bi, Z. Xiaofeng, "A modulation strategy to reduce common-mode voltage for current-controlled matrix converters", *IEEE Industrial Electronics, IECON 2006-32nd Annual Conference on. IEEE*, 2006, pp. 2775-2780.

20. H.J. Cha P.N. Enjeti, "An approach to reduce common-mode voltage in matrix converter", *IEEE Trans. Ind. Appl.*, vol. 39, no. 4, pp. 1151–1159, 2003.

21. C. Rui, M. Su, Y. Sun, W. Gui, "A novel commutation strategy to suppress the common mode voltage for the matrix converter", *Power and Energy Engineering Conference, 2009. APPEEC 2009. Asia-Pacific. IEEE*, 2009, pp. 1-4.

22. L. Hong-Hee, H.M. Nguyen, T.W. Chun, "A study on rotor FOC method using matrix converter fed induction motor with common-mode voltage reduction", *Power Electronics, 2007. ICPE'07. 7th International Conference on. IEEE*, 2007, pp. 159-163.

23. L. Hong-Hee, H.M. Nguyen, J. Eui-Heon, "A study on reduction of common-mode voltage in matrix converter with unity input power factor and sinusoidal input/output waveforms", *Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE. IEEE*, 2005, vol. 7, pp. 1210–1216.

24. H.M. Nguyen, H.H. Lee, "A new SVM method to reduce common-mode voltage in direct matrix converter", *Power Electronics, IPEC 2014. IEEE*, 2014, pp. 1013 - 1020.

25. H. N. Nguyen, H. H. Lee,"A modulation scheme for matrix converters with perfect zero common-mode voltage", *IEEE Transactions on Power Electronics*, vol.31, no. 8, pp: 5411-5422, 2016.

26. J. Rodriguez, M. P. Kazmierkowski, J. R. Espinoza, P. Zanchetta, H. Abu-Rub, H. A. Young, and C. A. Rojas, "State of the Art of Finite Control Set Model Predictive Control in Power Electronics," *IEEE Transactions on Industrial Informatics*, vol. 9, pp. 1003-1016, 2013.

27. S. Kouro, P. Cortes, R. Vargas, U. Ammann, and J. Rodriguez, "Model Predictive Control — A Simple and Powerful Method to Control Power Converters," *IEEE Transactions on Industrial Electronics*, vol. 56, pp. 1826-1838, 2009.

28. S. Kouro, M. A. Perez, J. Rodriguez, A. M. Llor, and H. A. Young, "Model Predictive Control: MPC's Role in the Evolution of Power Electronics" IEEE Industrial Electronics Magazine, vol. 9, no. 4, pp. 8-21, 2014.

29. R. Vargas, U. Ammann, J. Rodriguez, J. Pontt, "Predictive strategy to control common-mode voltage in loads fed by matrix converters", *IEEE Trans. Ind. Electron*., vol. 55, no. 12, pp. 4372-4380, 2008.

30. R. Vargas, J. Rodriguez, C.A. Rojas, M. Rivera, "Predictive control of an induction machine fed by a matrix converter with increased efficiency and reduced common-mode voltage", *IEEE Trans. Energy Convers*., vol. 29, no. 2, pp. 473-485, 2014.

31. M. Rivera, J. Rodriguez, J. Espinoza, B. Wu, "Reduction of common-mode voltage in an indirect matrix converter with imposed sinusoidal input/output waveforms", *IECON 2012-38th Annual Conference on IEEE Industrial Electronics Society. IEEE*, 2012, pp. 6105-6110.

32. N. Burany, "Safe control of four-quadrant switches", *Industry Applications Society Annual Meeting*, 1989. Conference Record of the 1989 IEEE. IEEE, 1989, pp: 1190-1194.

33. P. Cortes, M. P. Kazmierkowski, R. M. Kennel, D. E. Quevedo, and J. Rodriguez, "Predictive control in power electronics and drives", IEEE Trans. Ind. Electron., vol. 55, no. 12, pp. 4312 – 4324, Dec. 2008.