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Modular assembly of a single-phase inverter based on integrated functional blocks

Alberto Castellazzi, Adane Kassa Solomon, Nicola Delmonte, *Member, IEEE*, and Paolo Cova

Abstract— This paper presents an original modular plug-in type assembly approach for a single phase-inverter. The main focus here is, indicatively, on the power range 1-20 kW, but the methodology can be transferred to higher power levels, too. At the core of the inverter lies a power-dense double-sided-cooled half-bridge power switch architecture with integrated cooler, which is interconnected to filter elements, gate-driver and control circuitry by means of compact flat connectors. The integration exercise targets, on the one hand, the optimization of the power switch performance and reliability, as well as the reduction of circuit parasitic elements; on the other, the production of a system compatible with maintenance and repairing, featuring minimized impact of single component failure on the system maintenance and repair cost and thus on its availability. Preliminary experimental tests demonstrate the nominal functionality of the inverter.

Index Terms—Integrated circuit packaging; inverters; reliability; electro-thermal effects; electro-magnetic interference.

I. INTRODUCTION

Efficiency, power density and reliability are the main figures of merit which have traditionally driven power electronics technology evolution. Recently, emphasis has also been put more and more on manufacturability and modularity as key enablers of competitive product development. In view of the conflicting requirements typically underlying the optimization of these characteristics of a power system, their conjunct optimization proves a challenging undertaking, which requires consideration of all main components of a converter: solid-state devices, thermal management, passive filter elements and auxiliary circuitry used for control, driving and protection. Fig. 1 schematically illustrates the breakdown of a single-phase inverter into its main functional parts. This work proposes an exercise of overall re-consideration and comprehensive optimization of the way the inverter is put together. The main focus being on the optimization of performance, reliability and power density, manufacturing, assembly and maintenance aspects are also duly taken into account to deliver a novel approach at system level integration.

Past examples of advanced inverter integration and assembly have delivered significant progress beyond state-of-the-art as far as packaging, layout, cooling and interconnection solutions are concerned [1-4]. In particular, [1, 2] focused on fully bond-wireless power modules with double sided cooling and demonstrated a 30% higher power density capability in the development of a railway traction inverter with the same reliability figures as with conventional assembly using commercial power modules. [3] progressed the ideas presented

in [1-2] by simplifying the assembly process and reducing the number of manufacturing steps and interfaces and addressing the integration of a functional switch (i.e., a half-bridge structure), as opposed to the integration of a single switch with free-wheeling diode: this was demonstrated to be beneficial to the device switching performance and to the electro-magnetic interference (EMI) signature of the system. Also, [2] has the merit of fully decoupling the drive and power current paths and of using embedded flat terminals for external interconnections. Both [1-2] and [3] targeted, however, the comprehensive integration of the inverter system within a unique block and did not devise credible solutions to bring along reduced system impact by single component failure, nor to enhance the repairable nature of the system to yield improved availability. Also, much of the benefits of the proposed integration exercise at power switch level are lost in the system level assembly, due to relative lack of advancement in the design of suitable connectors. Other noteworthy examples of comprehensive system level integration have been produced, which however, address different power ranges and application domains, relying on technologies which would not be applicable and transferable in a straightforward manner to higher power (and, in particular, higher voltage) levels due to both very challenging technological needs associated with the high integration level and with quite high manufacturing costs [4]. Also, since such solutions do not cater for the ability to intervene on the system and repair it, they are not-viable for a number of applications, ranging from transport to renewable energies. Finally, a number of packaging and integration exercises have targeted the production of high-temperature capable solutions, specifically in relation to the use of wide-band-gap (WBG) power devices [5].

In this work, the novelty is threefold:

- the integration of the power switches is further enhanced by adopting flip-chip type device mounting and by introducing the use of vertical vias and embedded parallel current conduction layers, which benefit both the electro-magnetic and the electro-thermal performance of the semiconductor devices;
- protruding embedded flat contact terminals and bespoke connectors are used to ensure the low parasitic inductance nature of the design is preserved when moving from the switch to the system level;

- packaging bases on the identification of functional blocks within the inverter structure and the integration exercise correspondingly addresses, first, the optimization of each block individually, then, the optimization of their interconnection.

The result is a solution which preserves all of the positive features of [1-3] and which enhances the state-of-the-art with better performing power switches, reduced assembly and repair costs, improved availability of the system.

The design follows a built-in reliability approach, consisting in the minimization of the electro-thermal and electro-thermal stresses on the device, which, at the same time, benefits the inverter efficiency. These considerations include both the manufacturing process (reduction of residual stresses) and the actual mission and load profile of the inverter. At the center is a very compact high-performance half-bridge power switch concept (HBS in Fig. 1), which makes use of a number of advanced features in both device and substrate manufacturing to deliver a fully bond-wire-less, double-sided-cooled, low profile high-frequency capable switching element. The design of the power switch is tightly coupled with that of its cooler to deliver a solution, which progresses beyond state-of-the-art in performance and reliability, by enabling very effective cooling while reducing significantly the number of interfaces and eliminating altogether the use of wire-bonds. The switch is interconnected to the rest of the system by means of custom designed connectors, which also serve the function of packaging for a number of components, while ensuring that the enhanced features implemented at switch level are not lost in the interconnection to the additional components of the inverter.

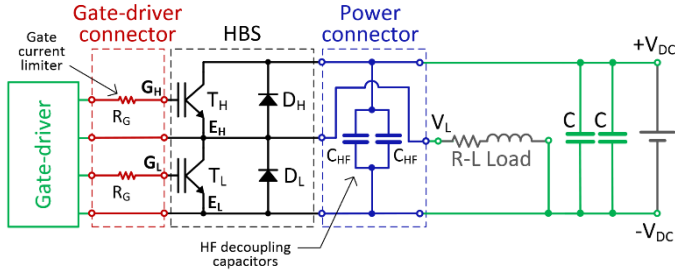


Fig.1 Schematic diagram of the open-loop inverter, with identification of its main functional parts.

The exercise presented here has future developments centered on wide-band-gap semiconductor device technologies in its field of sight, particularly as far as the need for higher switching frequencies and higher operating temperatures are concerned.

II. POWER SWITCH

A. Module

Fig. 2 shows a basic schematic of a half-bridge type switch, implemented with diodes and IGBTs in this case.

In switching applications supplying inductive loads, the load current is commutated at high-frequency between the devices in either the leg referred to as positive (p) cell or the leg referred

to as negative (n) cell: the terminology to denote the switching cells is derived from inverter current polarity, but similar considerations apply to the case of dc-dc converters, depending on the direction of power transfer [6]. So, from an application point of view, to minimize parasitic inductance and optimize switching performance, the ideal layout and packaging scheme of a half-bridge type switch should target the integration of the transistor in the high-side switch (T_H) with the diode in the low-side switch (D_L), and, vice-versa, the integration of the transistor in the low-side switch with the diode in the high-side switch (T_L - D_H).

Here, the switch is implemented in an innovative sandwich type assembly, where each IGBT-diode pair is soldered back-side down on separate substrates [7]: as compared with previously proposed approaches (see [8], for example), this arrangement offers the possibility to keep the interconnection loops and the corresponding stray inductance between T_H - D_L and between T_L - D_H at a minimum, while ensuring that all devices can be efficiently cooled via their preferential heat-transfer path, that is the backside. This way, while double sided cooling is still achieved, the thermal performance of the assembly is fully symmetrical. The devices used in this work are shown in Fig. 3: they are $70\mu\text{m}$ thin IGBTs and diodes rated at 600 V/ 200A, with lateral dimensions of 10mm x 9.5mm and 9.5mm x 5.5mm for IGBT and diode, respectively.

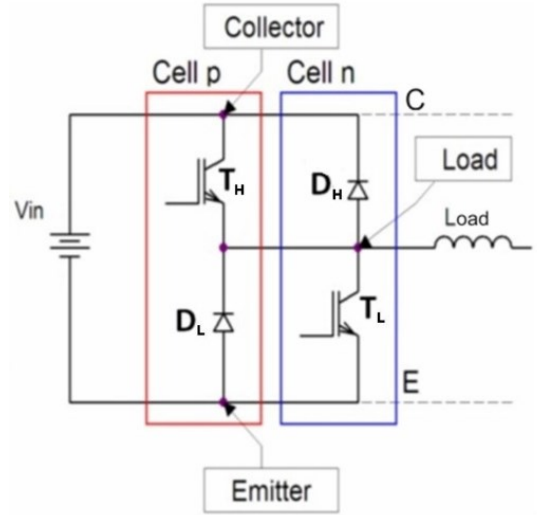


Fig.2 Schematic diagram of a half-bridge switch connected to an inductive load, with indication of p- and n-Cells to be integrated for optimum switching performance.

The device top and bottom finishing is non-conventional, consisting of a thin alloy of aluminum (Al) and copper (Cu) with nickel-phosphor (Ni-P) flash on the top and silver (Ag) finishing on the bottom such as to enable the devices to be compatible with soldered and sintered assembly processes on both sides.

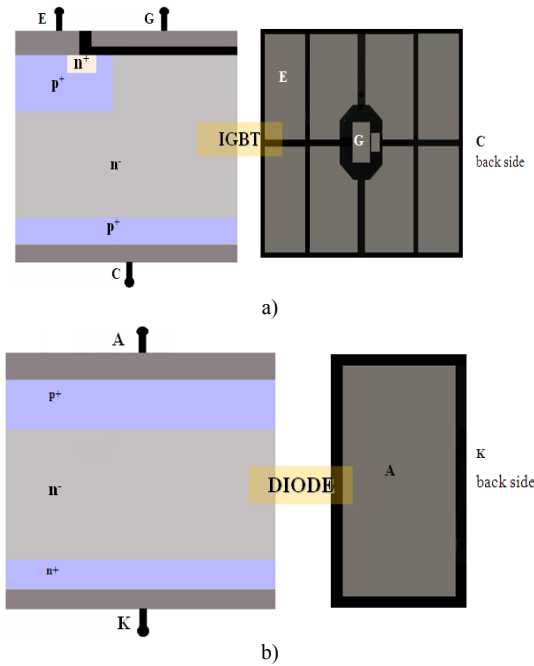


Fig. 3. Schematic cross-section and actual structure of IGBT, a), diode, b), chips. E, G and C indicate the IGBT Emitter, Gate and Collector terminals; A and K indicate the diode Anode and Cathode terminals.

The integration relies on advanced ceramic substrate technology, featuring double-etched patterned copper tracks for bond-wire-less interconnection and packaging; filled vias are also used in the ceramic substrates for vertical current conduction, which enables the introduction of a ground-plane structure within the switch, with greatly reduced overall values of parasitic inductance; finally, protruding broad and flat contacts derived from the substrate tracks themselves are used for interconnection to the rest of the system (filters, load and gate-drivers). With relevance to the circuit schematic of Fig. 2, the switch integration concept is illustrated in Fig. 4. It comprises of two ceramic substrates, with devices soldered back-side down pairwise onto them. To connect the chips top metallization, double-etching of the tracks on the ceramic substrates is used, which creates interconnection posts of suitable dimensions even for the smaller gate terminal. This solution allows for the use of a single solder layer between device metallization and copper post, enabling very compact and thin assembly when the two substrates are interconnected to form a sandwich type structure. As also indicated in Fig. 4, vias in the ceramic substrates are used for interconnection to a ground plane (denoted by the terminal E), which enables minimization of stray inductance. The intermediate ground plane is achieved by actually pressing together two ceramics substrates into a multi-layer single one. In this design, the power and drive terminals are on opposite sides of the switch and are both implemented with high-frequency compatible terminals, also integrated within the substrate design.

A cross-sectional view of the resulting final assembly, with the top substrate connected onto the bottom one, is shown in Fig. 5, with a detail of each component dimensions. The copper tracks are colored orange, the ceramic in dark grey, while the

lighter grey layers indicate tin-silver (Sn-3.5Ag) solder layers with 100 μm thickness. The IGBT chip is colored green.

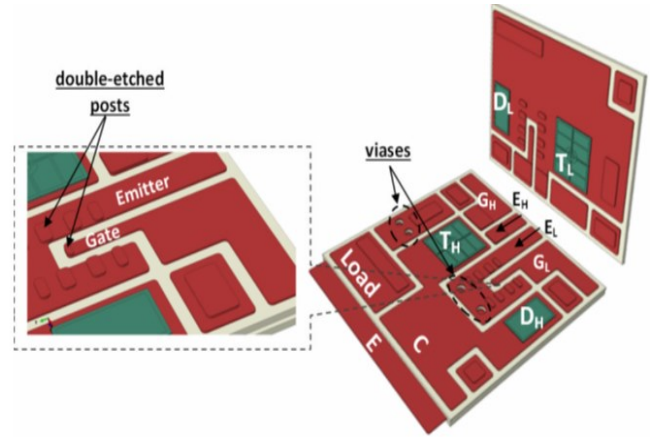


Fig. 4. Schematic 3D finite element structural model with detail of topical features.

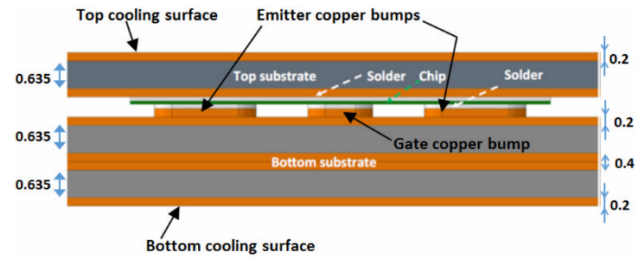


Fig. 5. Vertical cross section (at the T_L IGBT) of the proposed integrated power switch. All dimensions are in mm.

This concept represents a significant incremental development on recently proposed solutions, from both a manufacturing and an application perspective [9].

B. Manufacturing

The devised solution is compatible with both sintering and soldering technologies, which can be applied according to the needs and aims of the hardware development. Whereas soldering proved sufficient for the prototype presented here, to cope with the reduced feature sizes of upcoming WBG power device technologies, it is expected that sintering will yield better control of resulting interface layers and their quality. Also, sintering becomes a necessity when higher temperature operation electronics is in focus. The devices require bespoke finishing independent of what joining solution is applied. The finished chosen in this case, as described above, ensures compatibility with both processes. The quality of the finish clearly plays a major role in the final reliability of the assembly: most device manufacturers do now cater for solder-able device finish of high quality and the possibility for procurement of suitably finished semiconductor chips is certainly open, depending mainly on purchase quantities.

A known difficulty in the manufacturing of the proposed kind of structures is substrate warpage intervening during the assembly process, which prevents the obtainment of satisfactory electrical and thermal contacts or implies longer terms reliability issues as a result of thermal cycling during

operation of the switches [9]. In this case, that is particularly important in view of the double substrate used in the bottom part of the switch and the asymmetry in the volume and weight distribution of the substrates. So, it is extremely important to carefully select the thickness and shape of all materials involved in the assembly to ensure satisfactory results. To that aim, power switch design also needs to encompass a phase of parametric thermo-mechanical simulations aimed at delivering optimum structural design choices (e.g., ceramic and copper tracks thicknesses; relative thickness of tracks on different substrates and sides of the ceramic) for a given set of assembly process parameters (e.g., reflow profile). Fig. 6 shows the normalized solder reflow temperature profile used in our laboratory to manufacture the switch. Fig. 7 shows the substrate displacement at the time of maximum warpage during the reflow temperature cycle for both the top (a) and bottom (b) substrates when optimized values of ceramic and copper track thicknesses have been chosen, indicating contained values that enable proper assembly process.

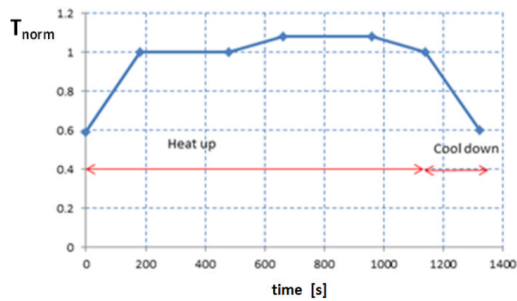


Fig. 6. Reflow temperature profile for switch assembly.

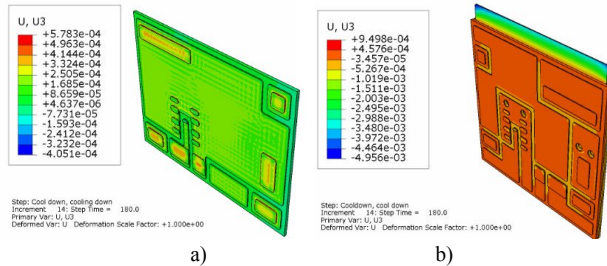


Fig. 7. Results of thermo-mechanical simulations indicating contained maximum warpage values during the assembly solder reflow process with optimized structural design choices for ceramic and copper tracks thicknesses. The scale unit is cm.

Extensive thermo-mechanical studies of the switch assembly have been carried out also for representative mission profiles, confirming the design and validating the technology options in terms of longer-term degradation and reliability.

In view of the results obtained in the design phase on the thermo-mechanical performance, the prototype was constructed using silicon-nitride (Si_3N_4) ceramic substrates. A photograph of the devices and of the double-etched substrates is shown in Fig. 8; Fig. 9 shows the fully assembled switch with the protruding electrical contacts for interconnection to gate drivers, load inductor and input filter. The assembly was

successful, with no evidence of any residual stresses in the switch.

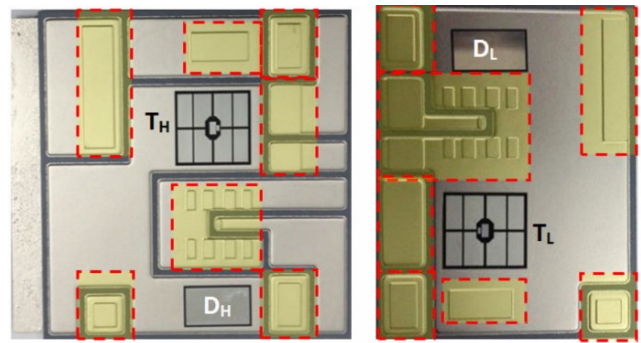


Fig. 8. Open view with detail of the double-etched posts (shaded areas). Here, the vias are not visible since they are filled with copper and plated.

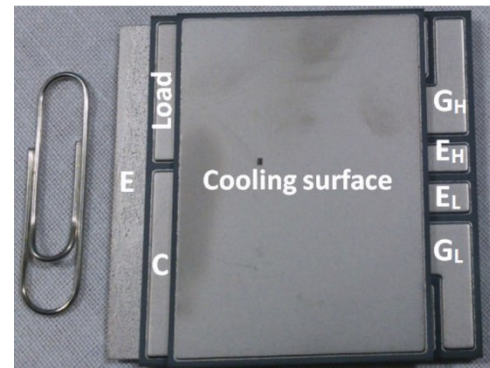


Fig. 9. Fully integrated half-bridge switch (HBS) featuring complete separation of power and driving loops.

Insulation, another key aspect in the manufacturing of power switches and modules, is achieved using two part one-to-one ratio mix silicone gel cured with a room temperature vulcanization process (RTV). The sample is dipped into a small container with mixed silicone gel in it: the container is then subjected to a vacuum drying oven passage at low pressure and room temperature condition to eliminate any air bubbles. Fig. 10 shows a detail of the resulting final rubbery material. Checks on quality for transfer to higher voltages (typically, in excess of 1 kV) are on-going. Preliminary results on static tests indicate straightforward transfer of the approach to 2 kV; partial discharge tests are still on-going.

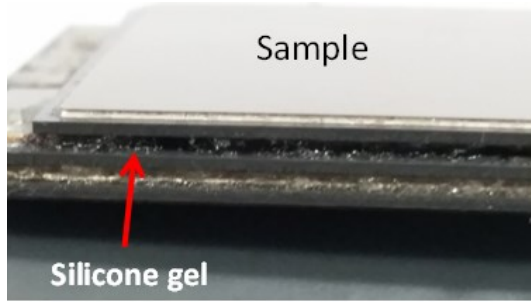


Fig. 10. Detail of switch filling for dielectric isolation and environmental insulation.

C. Electromagnetic analysis

From an electro-magnetic point of view, the design enables to: minimize the stray inductance associated with the *drive* loop (terminals GH-EH and GL-EL, indicating the high side and low-side gate and emitter contacts, respectively); to keep the drive and *power* loops fully separated, so that fast switch current variations do not interfere with the driving action as a result of the stray inductance [10]; finally, by means of the conducting vias created in the ceramic substrate, to implement a tight three-planes current conduction assembly (terminals C, Load and E) with largely overlapping conductors and an effective *ground-plane* covering the whole surface of the bottom metallization. The overall switch loop inductance can be thus greatly contained. The stray inductance of the power loop is important because it is mainly responsible of the over-voltages on the IGBTs at turn-off. Electromagnetic simulations have been done to evaluate the power loop stray inductance of our layout, followed by experimental validation. INCA3D, a software based on the PEEC (Partial Element Equivalent Circuit) method was used for the simulation [11]. With the PEEC method it is possible to extract the electric parameters as resistance, self and mutual inductance, from the geometry of the electric conductors of a circuit. The analysis, made with the software package INCA3D [12], was carried out varying the frequency of the test current applied to the power loop. We chose to mesh the 3D domain adapting it with the frequency of the sinusoidal current applied (automatically done by the software). We considered a switching frequency of 10 kHz, then frequency analysis has been done starting from this frequency up the harmonic at 10 MHz. The result of this parametric simulation is shown in Fig. 11. L_s varies from around 3.5 nH at 10 kHz, to 2.4 nH at 10 MHz. To validate the results of computer aided design, a measurement of a power switch module was carried out. This was done using an LCR meter HP 4284A and its test fixture. Biasing the loop with a maximum amplitude current of around 2 mA, we obtained 3.6 nH and 2.5 nH, at 1 kHz and 1 MHz respectively. The match between simulation and measurement is good.

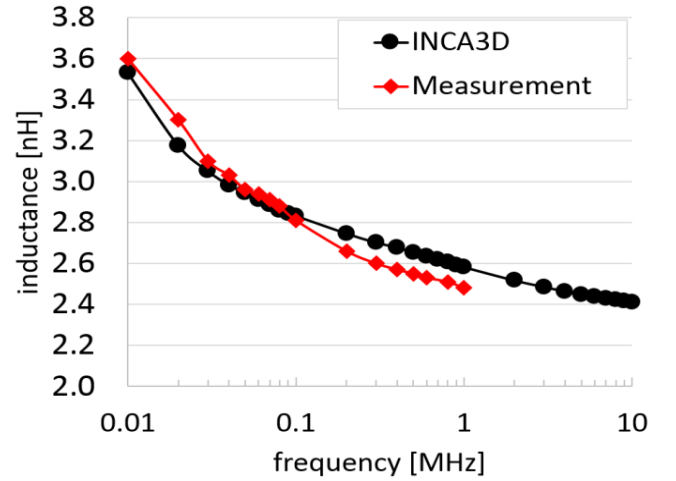


Fig. 11. Simulated and measured power loop stray inductance.

The stray inductance in the gate-source drive loop, L_{SG} , was also measured. The results are reported in Fig. 12, the length of the gate-emitter copper tracks is shorter than the ones of the power loop, then L_{SG} is lower than L_s .

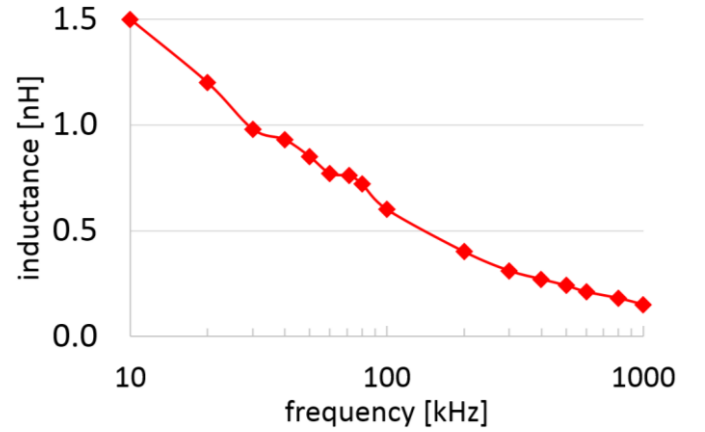


Fig. 12. Measured L_{SG} of the lower IGBT.

The presence of the intermediate ground plane on top of the bottom cooling surface is also key in reducing common-mode issues, which is often an important limiting factor in the transfer of conventional packaging solutions to the high-frequency operation desired with upcoming wide-band-gap device technology (e.g., silicon-carbide, SiC, and gallium-nitride, GaN).

D. Thermal management

The design of the switch typically needs to satisfy specific requirements in terms of thermal performance for given boundary conditions: ensuring that the temperature at some critical locations within the assembly stays below a given value is of paramount importance for the reliable definition of the component; in turn, this requirement determines to a significant extent its geometric and structural properties. Here, in particular, the attempt was made to finalize the design of the copper tracks, used primarily for electrical interconnection, also

from a thermal design perspective, as they are an integral part of the thermal management arrangement. The ceramic layers act as mechanical supports, electrical insulators and as good thermal bridges toward the cooling surfaces, because they have small thickness together with large area and good thermal conductivity. In other words, as illustrated in Fig. 13, from a thermal design point of view, the layers where IGBTs and diodes are soldered work as heat spreaders integrated in the module.

Multi-domain physical simulation was used to carry out a detailed analysis and design refinement of a number of design features and parameters. This kind of analysis is essential for determining the maximum heat that can be generated in the IGBTs and the diodes for given assembly dimensions and given boundary conditions. So, it was also applied to the study of required heat-sinking solutions under representative operational conditions. To choose the heat sink it is necessary to evaluate the heat flux at the cooling surfaces. Both IGBTs and diodes are rated for a maximum operating junction temperature of 448 K.

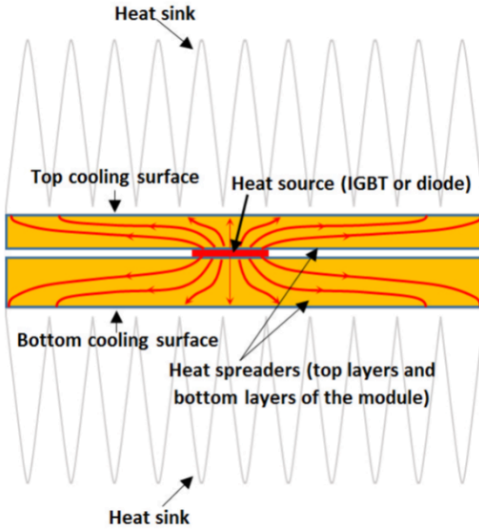


Fig. 13. Schematic of the thermal management arrangement of the power switch module.

The main target of the thermal analysis is to assess the design requirements in order to keep a satisfactory margin from the maximum value at worst-case or maximum load/ambient temperature conditions. Here, we present the results of a steady-state analysis. The solution of the heat equation is based on the finite element method. As thermal load, a worst case was considered with a total dissipated power by the semiconductor devices of 300 W: 100 W generated inside each IGBT and 50 W generated inside each diode. These values correspond to a 10 kW inverter leg with a representative 97% efficiency. The low resistance of the copper traces allows neglecting of the Joule heating inside them. The thermal conductivities of the materials were set as follows [13-14]:

- $k_{Cu} = 400 \text{ W/mK}$;
- $k_{Si} = 130 \text{ W/mK}$;
- $k_{Si3N4} = 27 \text{ W/mK}$;

- $k_{Sn3.5Ag} = 40 \text{ W/mK}$.

The heat-transfer coefficient for both the top and bottom cooling surfaces was initially set at a quite conservative value of $h = 2400 \text{ W/m}^2\text{K}$, to account for the whole thermal resistance between the cooling surface and ambient, including the contributions of a heat sink and a thermal conductive filler between the heat-sink and the cooling surface. The heat transfer coefficient of all the other surfaces was set to zero (adiabatic walls). In this case, ambient temperature was set at 293 K and a study was conducted using different heat generation profiles and different heat sink characteristics. Fig. 14 shows the resulting 3D thermal maps. The maximum temperature, reached inside the IGBTs, is around 387 K, well below the maximum limit of 448 K.

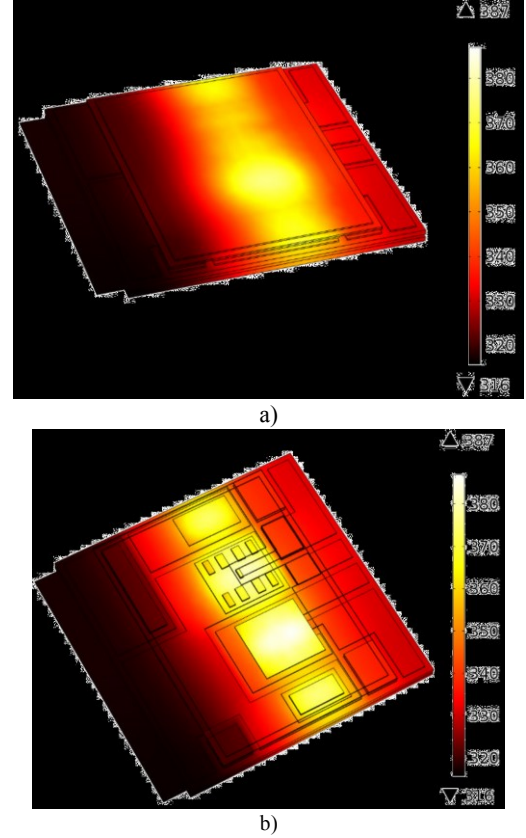


Fig. 14. Thermal maps (in K) obtained by a simulation of the power switch module with a total heat generation of 300 W, $h=2400 \text{ W/m}^2\text{K}$ on cooling surfaces and $T_{amb} = 293 \text{ K}$: (a) external surfaces (top); (b) inner temperatures at the silicon component layer.

III. COOLER

A. Cooler design

Taking the above thermal simulation into account, a forced liquid cooling system was also designed using computational fluid-dynamic (CFD) analysis in order to obtain an efficient heat extraction from the HBS. Fig.13 shows the result of CFD simulation fully coupled with the heat-transfer (HT) problem. From Fig. 13 a), it can be noticed that the relevant vorticity is in the portion where the liquid is in contact with the HBS cooling surface, hence improving the heat transfer. The total

dissipated power is 300 W, with a flow rate of 2 l/min and an inlet coolant temperature of 293 K.

High power inverters used, for instance, in transportation, need miniaturization and weight reduction (see [15], for example). This, in turn, requires cooling systems with high efficiency and reliability. Such inverters, either in research prototypes or commercially available power modules often introduce water or air cooled heat sink system [16, 17]. One of the goals of the cooling system design is to maintain the junction temperature of the power device below its maximum allowable temperature for nominal operation.

The first version of the water cooling system developed here is shown in Fig. 15: it was designed so as to maximize cooling at the locations of the hot-spots (i.e., the in correspondence of the power devices), corresponding to the rectangular red-colored area in the top-side photograph of Fig.15. It is also considered that the restrictions which are imposed by the position of the inlet and outlet of the coolant including the bolting locations for the gasket and 3D print polyamide plastic cover are dependent on the packaging conditions. The liquid flows from the inlet toward the top cooling surface, and once it passes this surface, it turns down and flows via the bottom cooling area of the switch to get to the outlet. Rectangular gaskets were designed to seal the plastic and the switch cooling surface. Finally, the cooling system is assembled and fixed with screws. Its nominal performance was investigated and optimized with the help of fluid-dynamic computer aided simulation and yielded the nominal full load steady-state results shown in Fig. 16, which corresponded to the intended target for the devices used here (rated for up to 175 °C steady junction temperature operation): as can be noted in Fig. 16 b) and c), the maximum temperatures of IGBTs and diodes were 323 K, 322 K, 333 K, 332 K for Q_H , Q_L , D_H , D_L , respectively.

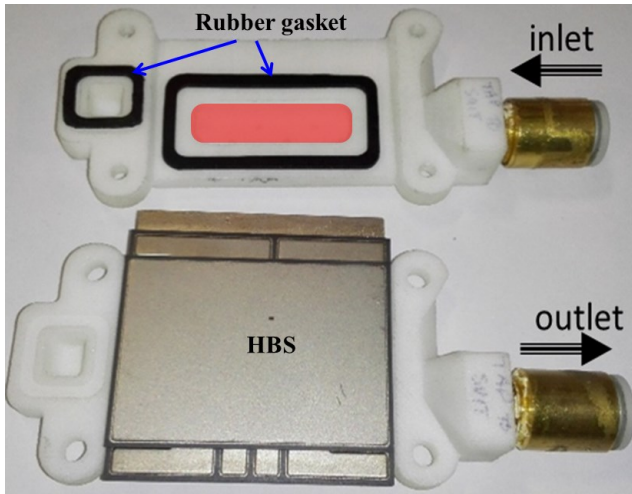


Fig. 15 Liquid cooler prototype.

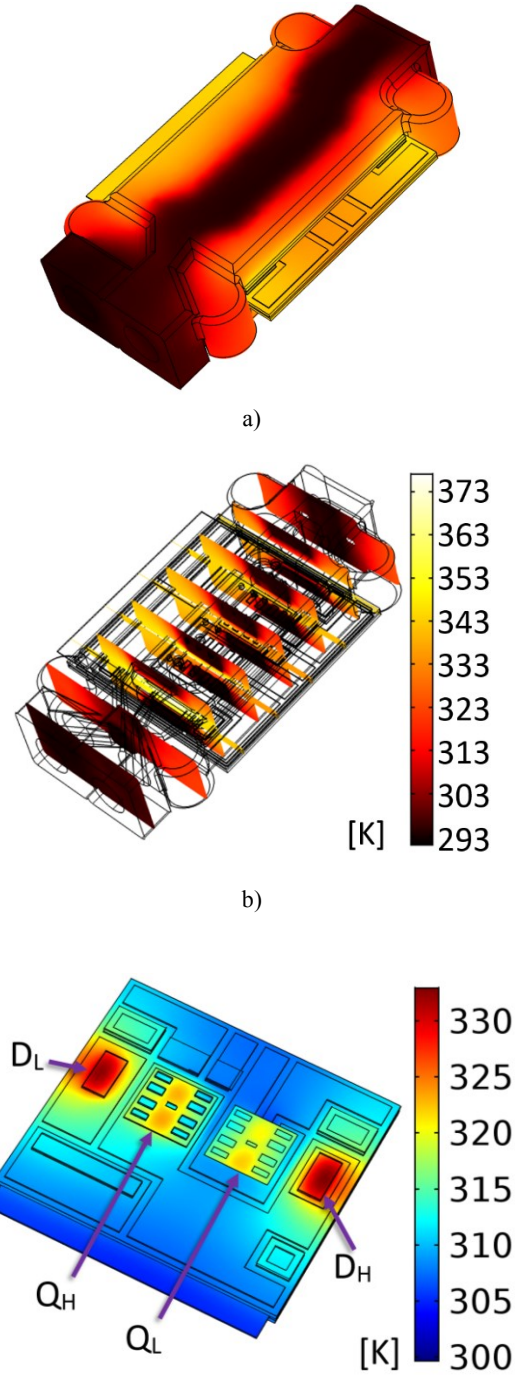


Fig. 16. Cooler external (a) and internal temperature distribution (b); detail of estimated temperature on the semiconductor chips (c)

B. Experimental characterization

The thermal performances of the assembly were verified by means of measurements performed with an infrared (IR) camera and thermocouples on a HBS prototype operating at the conditions reported in Tab. I. Due to non-optimized system level experimental setup (i.e., gate-drivers; filter design), the overall power dissipation was still relatively high, amounting to 180 W. The losses in the switches were calculated subtracting

from this value the estimated power losses in the filter elements and their value indirectly verified by comparison of thermal measurements with structural thermal simulations, as discussed ahead.

TABLE I THERMAL MEASUREMENTS OPERATING CONDITIONS	
Parameter	Value
Input voltage	298 V
Input power	1037 W
Switching frequency	10 kHz
Output voltage	160 V
Output power	857 W
Power losses	180 W
Temperature at the inlet	298 K
Flow rate	2 l/min
Ambient temperature	297 K

The cooling liquid inlet temperature was regulated by a liquid cooling system (Thermo Fisher Artic A25-SC100 refrigerated/heated bath circulator) and a 40% propylene glycol was used for corrosion and frost protection. The top surface of the cooler was painted with high emissivity coating. Fig. 17 shows the external thermal map measured by the IR camera, which is in very good agreement with the values estimated using structural simulations (finite element method).

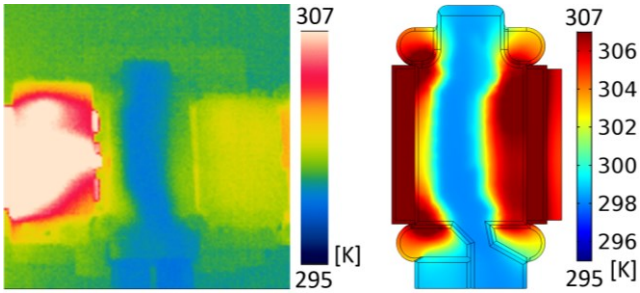


Fig. 17. Measured (left) and simulated (right) thermal map on the upper surface of the cooler + HBS assembly at the steady-state operating conditions of Tab. I.

IV. SYSTEM LEVEL INTERCONNECTION

In building a whole inverter, it is important that the electro-thermal and electro-magnetic advantages brought along by the integrated switch are not penalized at the moment of interconnecting more switches among them and with filters, gate drivers and the load. As part of this philosophy, in this work we also looked at integrating high-frequency decoupling capacitors as close as possible to the semiconductor devices.

For power ratings of few kW's typical values for high frequency decoupling capacitors are in the range of few microfarads. To contain parasitic inductance and resistance value it is moreover customary to implement these filters with either ceramic or film capacitor technology. The latter technology is however too bulky to be considered for an integration exercise, unless one can directly collaborate with capacitor

manufacturers or has in-house production capability. Ceramic technology offers much better capacity-density figures, but typically suffers from serious limitations in terms of capacitance value stability over bias voltage and temperature, with the result that, for application at few 100 V's, as in this work, over design is typically required, consisting in the parallel connection of a relatively large number of components.

Moreover, the maximum operational temperature values are typically lower than what is realistically required for mounting in the close vicinity of power switches. More recently, a new family of capacitors has been introduced, so called CeraLink™ capacitors, which is specifically designed for fast switching 650V semiconductors and offers new benchmark performance in terms of ratings, size and stability [18]. Fig. 18 shows a snapshot and indication of dimensions for a 1 μ F-500 V nominal rating component; data-sheet information about capacitance stability over bias voltage and temperature indicate excellent stability [18]. In view of these characteristics, this is presently regarded by the authors as the best commercially available product for integration purposes.

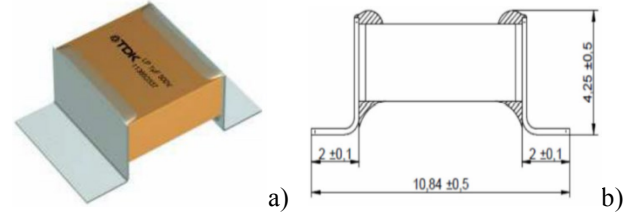


Fig. 18. High frequency CeraLink capacitor: snapshot, a), and dimensions, b), of a 1 μ F-500 V component [18].

In moving to system level integration, it is very important to be able to place the high-frequency decoupling capacitors as close as possible to the switching devices. Ideally, these should be embedded within the HBS itself. However, in view of their relative thickness, it was preferred in this case to still keep them outside of the sandwich structure, since they would have impaired the ability to achieve an equally compact and high performing design. So, external power line connections were designed following the same philosophy applied to the switch to still contain overall parasitic inductance. A plug-in type flat connector was designed, inspired by the edge connectors used in high frequency signal and thus re-branded as *power edge connector*. The concept is illustrated in Fig. 19: the ceramic capacitors are embedded within the connector; inside the connector, folded metal clips ensure good mechanical and electrical contacts with the emitter, collector and load tabs of the switch. Fig. 20 shows a picture of the actually manufactured prototype, connected to the power switch (the cooler was painted black for experimental infrared thermal characterization). On the side not receiving the HBS power terminals, the connector is designed to receive a standard PCB, on which the DC-link capacitors are mounted.

A similar approach was adopted for the design of the connector on the drive side of the switch. Concept and hardware prototype for the gate-side connector are shown in Fig. 21. The

connector is designed to receive on one side the HBS and on the other the logic circuitry in the gate-driver. Analog switches, capacitors and resistors belonging to the gate-driver circuit are housed within the connector itself, in the close vicinity of the HBS terminals.

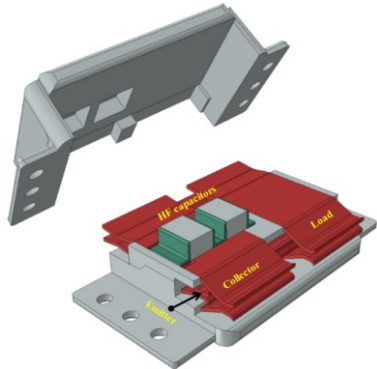


Fig.19. Power edge connector model with embedded high-frequency decoupling capacitors.

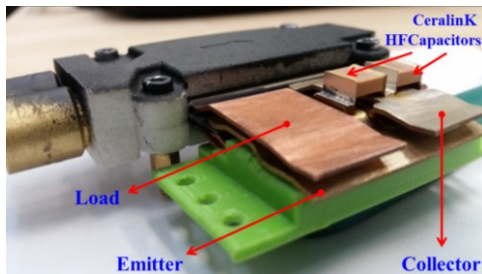
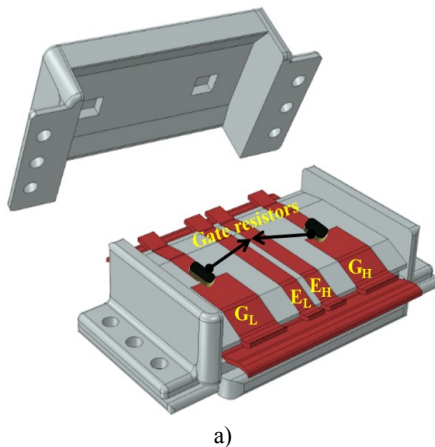
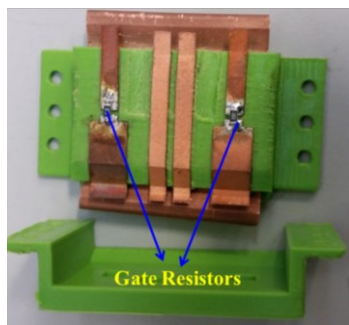


Fig.20. Power edge connector prototype with detail of interconnection to the HBS.



a)



b)

Fig. 21. Gate-side power edge connector: 3D CAD model a); and prototype b).

The resulting overall system level assembly, corresponding to the schematic functional inverter breakdown diagram of Fig.1, is shown in Fig. 22.

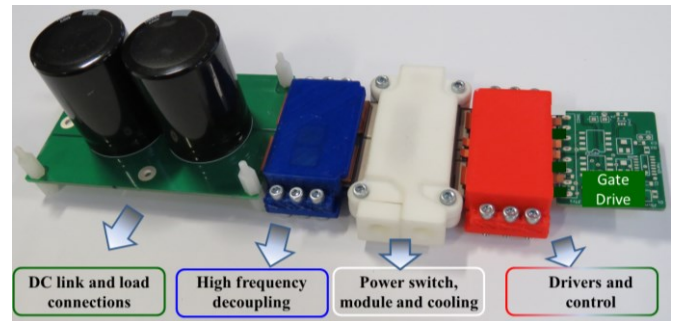


Fig.22. Photograph of the fully assembled inverter, corresponding to the schematic breakdown of Fig. 1.

The assembled single-phase inverter contains all components required for operation. All functional modules within the inverter system are interconnected by plug-in type connectors: so, failure of any one individual module requires dedicated maintenance, to replace the failed module only. With the proposed approach, that can be achieved quite speedily, as it does not require de-soldering or un-screwing of the modules, nor the replacement of interface materials, for instance, towards a heat-sink or mounting substrate. Connection to the loads and to the input power supply is implemented by means of the DC-link and load connections PCB-type board, which only mounts the DC-link electrolytic filter capacitors and foresees the use of cables and screwed terminals. It is important to note, that these terminals may not strictly need to be removed for repairing and maintenance purposes.

V. PRELIMINARY FUNCTIONAL TESTS

A preliminary full system functional test was carried out in open loop configuration, Fig. 23, with 300 V_{DC} input voltage and 10 kHz switching frequency, with a fixed dead time of 500ns. The cooling liquid temperature was regulated to 25 °C, using propylene glycol as the coolant. A dedicated test set-up was built, which accommodates additional filter elements (magnetics) and the driving platform, based on an Altera FPGA. Some representative waveforms are reported in Fig. 24. These results confirm the correct operation of the inverter and, albeit with relatively slow switching transitions, support the indication of contained value of parasitic inductance involved in the commutation process.

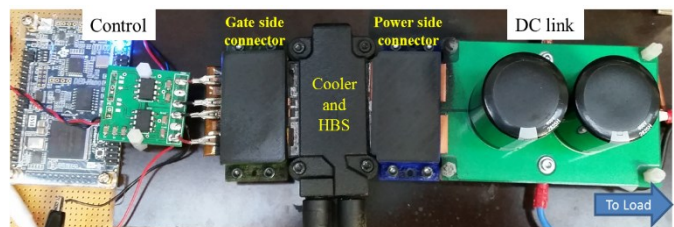


Fig.23 Overall integrated single-phase inverter test setup.

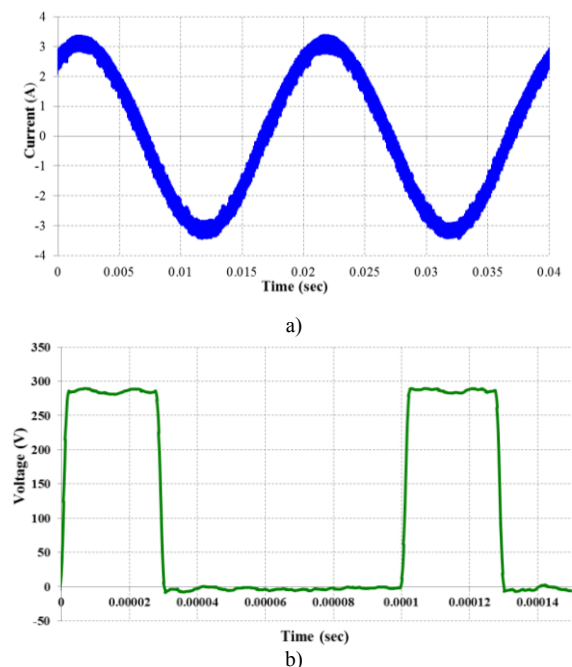


Fig.24 Representative experimental result a); and zoomed version of voltage across the switch b).

VI. CONCLUSIONS

This paper has proposed an innovative modular integration scheme for power converters which brings along advanced electro-thermal and electro-magnetic performance, as well as modularity and reduced impact of single component failure for system maintenance and availability. The devised solution bases on a competitive assembly process, which can be made to reduce manufacturing time to compensate for somewhat higher material costs, as compared with traditional assembly processes. The benefits achieved at power switch level are kept when integrating a whole system by bespoke development of *power edge connectors* with embedding capability for passive components and auxiliary circuitry. The proposed solution enables the development of modular power converters, thus potentially enabling significant gains in system level maintenance cost, which, again, are likely to offset any extra cost incurred due to initial higher price. Preliminary experimental results show correct operation of the system. More quantitative details of electro-thermal performance are presented in [19, 20]. Overall, the proposed approach is transferable to upcoming wide-band-gap device technology, as it is compatible with higher heat-generation rates and higher switching frequencies than the more traditional assembly solutions. Some specific features need of course re-design for the needs of the devices at hand. In the future, integration of magnetic components, neglected in this study, also needs to be looked at.

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