Characterisation of temperature dependent parameters of multi-quantum well (MQW) Ti/Au/n-AlGaAs/n-GaAs/n-AlGaAs Schottky diodes

Walid Filali[1], Nouredine Sengouga[1,*], Slimane Oussalah[2], Riaz H. Mari[3], Dler Jameel[4], Noor Alhuda Al Saqri[5], Mohsin Aziz[6], David Taylor[6], Mohamed Henini[6]

[1] Laboratory of Metallic and Semiconducting Materials, Université de Biskra, B.P. 145, 07000 Biskra RP, Algeria

[2]Centre de Développement des Technologies Avancées, Algiers, Algeria

[3]Institute of Physics, University of Sindh, Jamshoro, Pakistan

[4]Department of Physics, Faculty of Science, University of Zakho, Kurdistan Region, Iraq.

[5]Department of Physics, College of Science, Box 36, Sultan Qaboos University, Al Khoud 123, Oman

[6]School of Physics and Astronomy, Nottingham Nanotechnology and Nanoscience Center, University of Nottingham, Nottingham, NG7 2RD, UK

[*]Corresponding author: n.sengouga@univ-biskra.dz (N. Sengouga)

Abstract

Forward and reverse current-voltage (I-V) of Ti/Au/n-$Al_{0.33}Ga_{0.67}As$/n-GaAs/n-$Al_{0.33}Ga_{0.67}As$ multi-quantum well (MQW) Schottky diodes were measured over a range of temperatures from 20 to 400 K by a step of 20 K. The Schottky diodes parameters were then extracted from these characteristics. The Cheung method is used for this purpose, assuming a thermionic conduction mechanism. The extracted ideality factor decrease with increasing temperatures. But their values at low temperatures were found to be unrealistic. In order to explain this uncertainty, three assumptions were explored. Firstly an assumed inhomogeneous barrier height gave better parameters especially the Richardson constant but the ideality factor is still unrealistic at low temperatures. Secondly, by using numerical simulation, it was demonstrated that defects including interface states are not responsible for the apparent unrealistic Schottky diode parameters. The third assumption is the tunneling mechanism through the barrier in the low temperature range. At these lower temperatures, the tunneling mechanism was more suitable to explain the extracted parameters values.

Key words:

MQW; GaAs/AlGaAs Schottky diodes; inhomogeneous barrier height; defects, tunneling

1. Introduction

Schottky diodes are the basic building component in many semiconductor devices (field effect transistors, solar cells, photodetectors, Gunn diodes, microwave diodes, etc...) and integrated circuits, hence the intense interest they receive from the research community. The characterization of the Schottky barrier is important not only because the Schottky diodes are the basic block of many semiconductor devices but because they may exhibit a potential barrier at the metallization of a semiconductor surface for external device connection. Although silicon continues to dominate the semiconductor industry, III-V semiconductors (GaAs and related alloys) dominate the high frequency and low power applications [1–4]. Schottky diodes based on III-V semiconductors make the gate of high-electron mobility transistors (HEMTs) and metal–semiconductor field effect transistors (MESFETs) [5, 6]. Furthermore, III-V semiconductors are also used in many optoelectronic devices such as light emitting diodes, lasers, photodetectors, etc. [7]. The performance of such devices can be improved by alloying different types of III-V semiconductors. Hence the use of more and more sophisticated structures such as superlattices (SL's), quantum wells (QW's), quantum dots (DQ's), quantum wires (QW's), etc. Perhaps the most important III–V system is the GaAs/$Al_xGa_{1-x}As$ heterostructure. In detectors, it can cover a wide wavelength range from UV to far-infrared (THz) [8]. Multilayer GaAs/AlGaAs structures are used in highly sensitive bolometers based on high temperature coefficient of resistance (TCR) [9] and bacteria photonic biosensing [10].

Measurements of Schottky diodes by current-voltage (I-V) and capacitance-voltage (C-V) characteristics are used to extract their parameters such as the Schottky barrier height (SBH) and ideality factor (n) at room temperature [11, 12]. The conduction mechanism in these structures can be revealed from the temperature dependence of the I-V and C-V characteristics [13, 14]. In real simple metal-semiconductor Schottky diodes, however, it is difficult to obtain Schottky diodes with an ideality factor n = 1 primarily due to non-ideal thermionic emissions, which include a thermionic-field emission, a quantum mechanical tunnelling, and generation-recombination in the space charge region, hence the I–V characteristics always deviate from the ideal case where abrupt junction and a fixed homogeneous SBH are assumed [2]. The deviation from ideality may be attributed to interface states induced by the presence of defects which leads to lateral Schottky barrier inhomogeneities [15] or tunnelling current [16, 17]. In more complicated structures such as superlattices and multi-quantum wells, the departure from ideality is even bigger [8-10]. In this paper Au/n-AlGaAs/n-GaAs multi quantum wells Schottky diodes were characterised by I-V from 20 to 400 K. The diode parameters

were then extracted from these characteristics and analysed to reveal the conduction mechanism involved. Assuming pure thermionic conduction mechanism, it was observed that the apparent ideality factor increases with decreasing temperature and it reaches a very high value of ~20 at 20 K. The purpose of this work is to explain this unusual behaviour. To achieve this goal, a combination of numerical simulation using TCAD simulator [18] and analytical modelling based on well established diodes models were carried out. The numerical simulation was to study whether defects have a role in this abnormal behaviour. The analytical modelling was used to reveal which conduction mechanism is dominant.

2. Theory

In ideal Schottky diode the current transport mechanism is due to thermionic emission (TE). The current is given by:

$$I = AA^{*}T^{2}exp\left(\frac{-q\emptyset_b}{kT}\right)\left(exp\left(\frac{qV}{kT}\right)-1\right) \qquad (1)$$

A is the surface of the diode of a circular shape with diameter of 600 µm, $A^{*}$is the effective Richardson coefficient, T is the absolute temperature, q is the electronic charge, k is the Boltzmann constant, Φ_b is the Schottky barrier height and V is the applied voltage. In reality, however, other current-transport mechanisms are present. These include thermionic field emission (TFE), field emission (FE), recombination and tunnelling. The total current, taking into account all these mechanisms, can be written as [19]:

$$I = \underbrace{I_{TE0}\left(exp\left(\frac{q(V-IR_S)}{kT}\right)-1\right)}_{1} + \underbrace{I_{GR0}\left(exp\left(\frac{q(V-IR_S)}{2kT}\right)-1\right)}_{2} + \underbrace{I_{Tun0}\left(exp\left(\frac{q(V-IR_S)}{E_0}\right)-1\right)}_{3} + \underbrace{\frac{V-IR_S}{R_{Sh}}}_{4} \qquad (2)$$

In equation 2, the first, second, third and fourth term represent the thermionic field emission (TFE), the recombination mechanism, the tunnelling mechanism and the series and shunt resistances effects, respectively. Obviously one of these components may dominate the others at a certain temperature and voltage regions. Furthermore, I_{TE0} is the thermionic emission saturation current, -I_{GR0} is the generation-recombination saturation current and I_{Tun0} is the tunnelling saturation current.

If the tunnel component and shunt resistances effect are neglected, equation 2 can be written in a more convenient way so that [2]:

$$I = I_S\left(exp\left(\frac{q(V-IR_S)}{nkT}\right)-1\right) \quad (3)$$

I_S is the saturation current and n is the ideality factor.$n = 1$if the conduction mechanism is pure thermionic while $n = 2$ if the conduction mechanism is pure recombination. Usually both mechanisms are simultaneously present so that $1 < n < 2$. In this case I_S is given by:

$$I_S = AA^*T^2 exp\left(\frac{-q\emptyset_b}{kT}\right) \qquad (4)$$

Most extraction methods of the Schottky diode are based on this well-established equation. Equation (3) is sometimes modified to take into account the non-saturation of the saturation current while neglecting the series resistance [20], thus:

$$I = I_S exp\left(\frac{qV}{nkT}\right)\left(1 - exp\left(\frac{-qV}{nkT}\right)\right) \quad (5)$$

On the other hand, if the conduction mechanism is dominated by tunnelling then (1) is reduced to:

$$I = I_{Tun0}\left[exp\left(\frac{q(V-IR_S)}{E_0}\right) - 1\right] \qquad (6)$$

In this work, firstly by assuming that the dominant conduction is thermionic conduction, (3), (4) and (5) are used to extract the Schottky diode parameters.The numerical simulation is carried out using the SILVACO software to check whether defects and interface states have any role in the anomalous behavior of the ideality factor at low temperatures. ATLAS is one of the modules of SILVACO. ATLAS is a physically based two- and three-dimensional semiconductor device simulator. It evaluates the electrical characteristics of the specified physical structure including DC, AC, transient, frequency dependence. ATLAS, like any software simulating semiconductor devices, divides the specified structure into a two or three-dimensional mesh grid and solves the descritised and linearised Poisson's equation, the carrier continuity equations and the transport equations. Further details can be found in the ATLAS manual [18] or in one of our papers [21].

3. Results and discussion

3.1. Sample structure

The sample, referred to as NU1054, is grown in Nottingham Nanoelectronics MBE Laboratory. The N-type Silicon doped GaAs/AlGaAs multi-quantum wells (MQWs) are grown by molecular beam epitaxy (MBE) on a semi-insulating (100) GaAs substrate. GaAs and $Al_{0.33}$ $Ga_{0.67}$ As epilayers were doped to a concentration level of 2×10^{16} cm^{-3} and 1.33×10^{16} cm^{-3}, respectively, and the growth temperature of the buffer and the epitaxial layers was 580 °C and 630°C, respectively. Layer structure

of the samples starting from the substrate is: 1 µm GaAs (n = 2 × 10^{16} cm^{-3}) buffer layer, 0.14 µm $Al_{0.33}Ga_{0.67}As$ (n = 1.33 × 10^{16} cm^{-3}) barrier, a 60 periods GaAs (50 Å) (n = 2 × 10^{16} cm^{-3}) /$Al_{0.33}Ga_{0.67}As$ (90 Å) (n = 1.33 × 10^{16} cm^{-3}) MQW's, 0.14 µm $Al_{0.33}Ga_{0.67}As$ (n = 1.33 × 10^{16} cm-3) barrier. Ohmic contacts were made to the bottom of n-type-doped GaAs buffer layer using wet chemical etching, metal evaporation of Ge/Au/Ni/Au (54-nm/60-nm/20-nm/136-nm thick layers) and annealing at 360 °C for 30 sec. The Schottky contacts were fabricated by evaporating Ti/Au (40 nm/175 nm) on the top of the n-type-doped $Al_{0.33}Ga_{0.67}As$ layer. The different thicknesses are typical of structures used MQW solar cells for example, that is for better absorption of light. A two-dimensional schematic view of the sample is shown in figure 1.

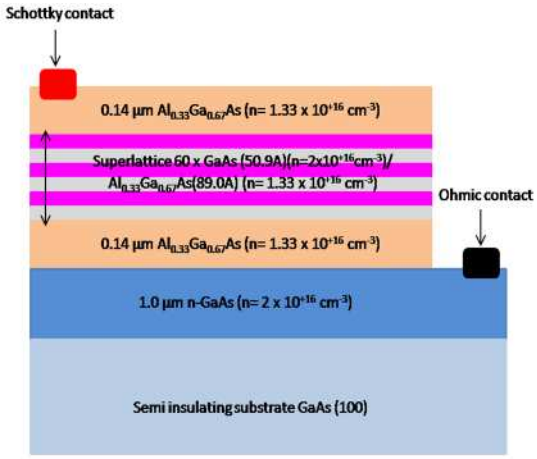

Figure 1. A two-dimensional schematic cross section of the silicon doped N-type Ti/Au/n-AlGaAs/n-GaAs/n-AlGaAs MQW Schottky diode.

Electrical characterisation of the devices is is the current voltage (I-V) versus temperature ranging from 20Kto 400K. The instruments used in these characterization are : a cryostat (Janis CCS-450), a temperature controller (Lake Shore 331), a Keithley 428 I-V meter, an Agilent 41501B pulse generator and a personal computer. The measured I-V characteristics of the Schottky barrier diode are presented in figure 2 in the temperature range of 20–400 K. In the forward bias, the current increases rapidly with increasing bias in the low bias region but slows down considerably for higher voltages especially at lower temperatures. The I–V characteristics have the usual form in the low voltage region while at high voltages the series resistance effect is well observed. The reverse current increases with increasing reverse bias and no saturation is observed. This is a well-known defects related phenomenon (surface states and/or bulk defects) [2]. Another observation is that the forward and reverse current increases with increasing temperature indicating a usual thermal activation. Now these characteristics will be analysed in detail by extracting the Schottky diode parameters.

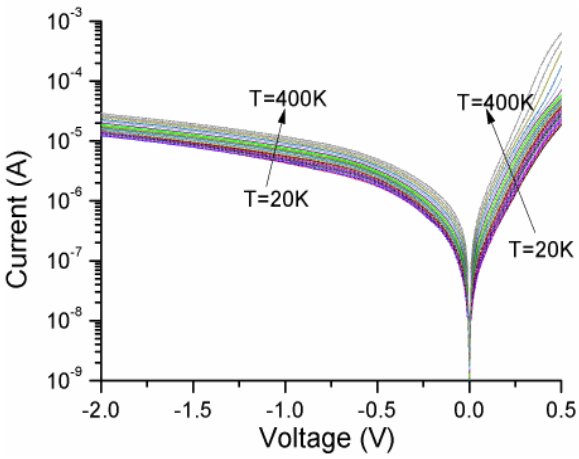

Figure 2. Measured forward and reverse bias semi-logarithmic current –voltage (I-V) characteristics of the silicon doped N-type Ti/Au/n-AlGaAs/n-GaAs/n-AlGaAs MQW Schottky diode for temperatures ranging from 20 to 400 K.

3.2. Diode parameters extraction

As mentioned in section 2, the simplest form of the thermionic conduction mechanism may be represented by equation 2. Some parameters can be extracted from the reverse while others can be extracted from the forward I-V characteristics. The saturation current, on the other hand can be determined from both characteristics. First, from the reverse characteristics, the saturation current is calculated from the intercept of a plot of $I/\left[1-\exp\left[\frac{qV}{KT}\right]\right]$ versus V. Such a plot is shown in Figure 3.

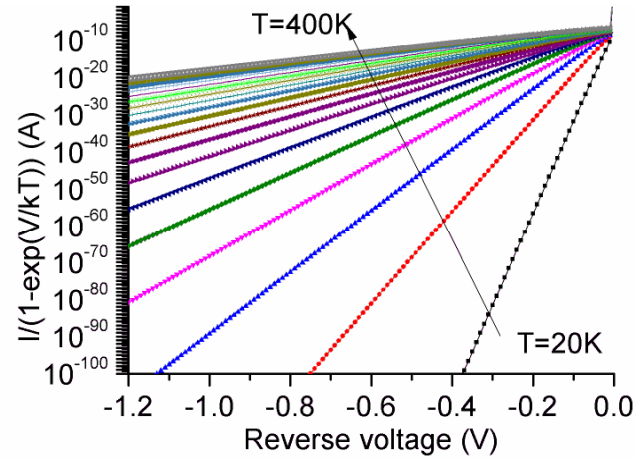

Figure 3. A plot of $I/(1-\exp[-qV/kT])$ versus reverse bias voltage to extract the saturation current.

Second the saturation current can also be extracted from the forward characteristics using the classic Cheung fitting method by carefully choosing the region of the forward characteristics where the series resistance is negligible and the semi-logarithmic plot is linear [22]. The Cheung method is based on a series of transformations of equation 3, thus:

$$\ln(I) = \ln(I_S) + \frac{q(V - R_S I)}{nkT} \qquad (7)$$

Replacing I_S by its relation with $\emptyset_b$ from (4), equation 7 can be written as:

$$\ln(I) = \ln(AA^*T^2) - \frac{q\emptyset_b}{kT} + \frac{q(V - R_S I)}{nkT} \qquad (8)$$

Equation (8) can be written in a more convenient way as:

$$H(J) = R_S A J + n\emptyset_b \quad (9)$$

Where A is the diode area and $H(J)$ is a function given by:

$$H(J) = V - \frac{nkT}{q}\ln(AA^*T^2) \qquad (10)$$

A plot of ln(I) of equation 8 is shown in Figure 4.

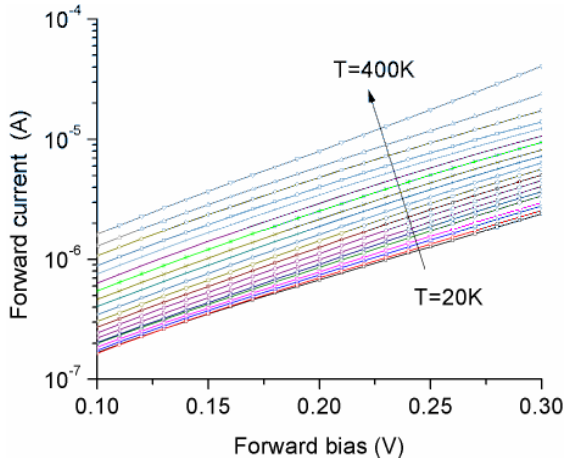

Figure 4. A semi-logarithmic plot of the forward current versus forward bias voltage to extract the saturation current.

The intercept of the linear curve with the forward current axis gives the saturation current. The extracted saturation current from the reverse and forward characteristics is shown in figure 5. There is a factor of ≈ 3.5 between the values extracted from the reverse characteristics compared to those extracted from the forward characteristics. It has to be mentioned that the term $\left(1 - exp\left(\frac{-qV}{nkT}\right)\right)$ in

equation 5 has no physical meaning; it is only used for fitting purposes. Therefore it is perhaps fair to state that the values extracted from the forward characteristics are more reliable. In both cases the saturation current increases with increasing temperature. This behaviour is expected since the saturation current is proportional to the free carrier intrinsic density which increases with increasing temperature.

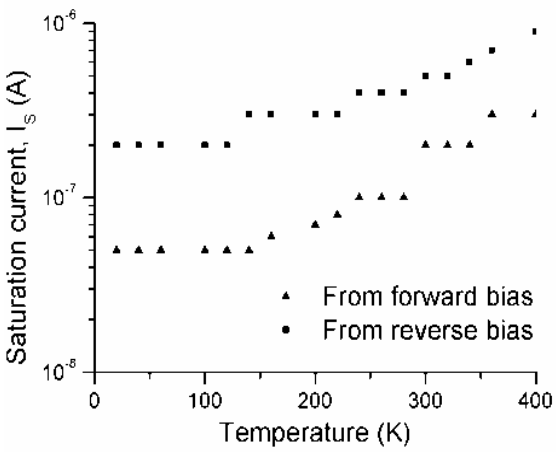

Figure 5. The extracted saturation current from the reverse and forward I-V characteristics versus temperature.

From the extracted values of the saturation current, the barrier height $\emptyset_b$ can be evaluated using equation 4, assuming the theoretical value of the Richardson constant A^* for AlGaAs which is 8.05 Acm^{-2} K^{-2}[18]. From (4) $\emptyset_{b0} = \frac{kT}{q} Ln(AA^*T^2/I_s)$.

The extracted barrier height is shown in figure 6.

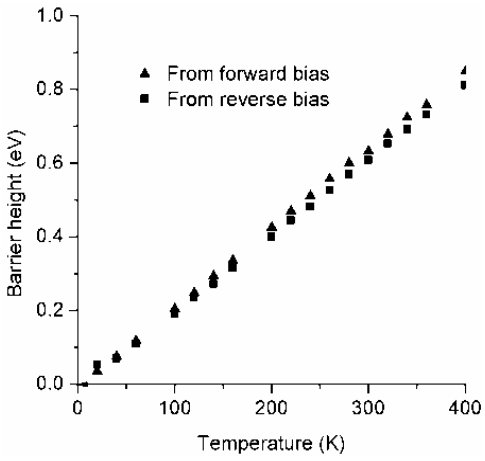

Figure 6. Barrier height versus temperature plot for the Ti/Au/n-AlGaAs Schottky diode in the temperature range of 20 – 400K

The ideality factor $n$can be extracted from the slope of the semi-logarithmic plot of the forward current of figure 4 since it is given by

$$n = \frac{q}{KT}\frac{dV}{dln(I)} \qquad (11)$$

The extracted ideality factor is shown in figure 7 in the temperature range 20-400 K.

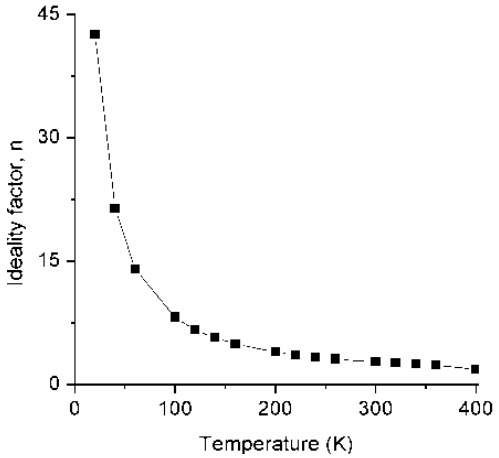

Figure 7. The extracted ideality factor n from the forward I-V characteristics of the silicon doped N-type Ti/Au/n-AlGaAs/n-GaAs/n-AlGaAs Schottky diode for temperatures ranging from 20 to 400 K.

The first observation is the apparent high values of the ideality factor especially at lower temperatures where it reaches $n \approx 42$ at 20 K. Although several authors [23-26] observed this behaviour at low temperatures but not as down as to 20 K. Some have attributed the high ideality factor and the low barrier height values to inhomogeneities of the barrier itself due to interface traps [27, 28]. The main aim of this paper is to try to understand this unusual behaviour which will be discussed in detail in the next section.

3.3. Inhomogeneous barrier height

As mentioned before, several authors have attributed the high values to inhomogeneities of the barrier height. First the Richardson constant is evaluated by transforming equation (4) to the so-called Richardson plot, thus:

$$\ln(\frac{I_S}{T^2}) = \ln(AA^*) - \frac{q\emptyset b}{kT} \qquad (12)$$

A plot of $\ln(I_S/T^2)$ versus $1000/T$ yields the Richradson constant A^* from the intercept and the average barrier hight from the slope. Such a plot is shown in figure 8.

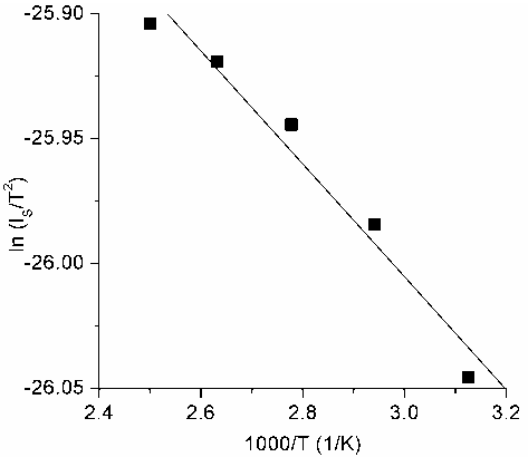

Figure 8. The Richardson plot of $\ln(I_S/T^2)$ versus $1000/T$.

The value of A^* obtained from the intercept of the linear portion of the ordinate is $8.86\text{x}10^{-10}$ $A\cdot cm^2\cdot K^2$, which is much lower than the theoretically calculated valueof8.05 $A\cdot cm^2\cdot K^2$ for n-type Ti/Au/AlGaAs. The slope of the straight line gives a value of 0.259 eV for the barrier height. The unrealistic value of the Richardson constant is usually attributed to inhomogeneities of the barrier height [28-30]. To remedy this, an inhomogeneous distribution of the barrier height was suggested [28]. The Gaussian distribution is given by

$$G(\emptyset_B) = \frac{1}{\sigma_0\sqrt{2\pi}} e^{-\frac{(\emptyset_B - \overline{\emptyset_{B0}})^2}{2\sigma_0^2}} \qquad (13)$$

In this case the ideality factor η and the barrier height $\emptyset_b$are replaced by apparent values $\eta_{ap}$and $\emptyset_{ap}$ respectively in the current-voltage relation (equations 4 and 5), thus:

$$I = AA^*T^2 exp\left(\frac{-q\emptyset_{ap}}{kT}\right) exp\left(\frac{qV}{nkT}\right)\left(1 - exp\left(\frac{-qV}{\eta_{ap}kT}\right)\right) \qquad (14)$$

The apparent ideality factor and the barrier height are given, respectively, by [29-30]:

$$\emptyset_{ap} = \overline{\emptyset_{b0}} - \frac{q\sigma_0^2}{2kT} \qquad (15)$$

$$\left(\frac{1}{\eta_{ap}} - 1\right) = -\rho_2 - \frac{q\rho_3}{2kT} \qquad (16)$$

$\overline{\emptyset_{b0}}$is the mean barrier height, σ_0 is the standard deviation of the Gaussian distribution of the barrier height, $\rho_2$and $\rho_3$are voltage coefficients.

A plot of equations (15) and (16) versus $\frac{q}{2kT}$ yields $\overline{\emptyset_{b0}}$, σ_0, $\rho_2$and ρ_3. Such plots are shown in figures 9 and 10.

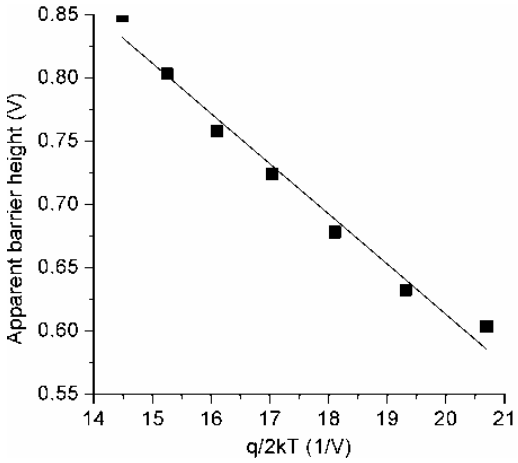

Figure 9. The apparent barrier height versus q/2kT curves of Ti/Au/n-AlGaAs Schottky barrier diode according to a Gaussian distribution of BHs.

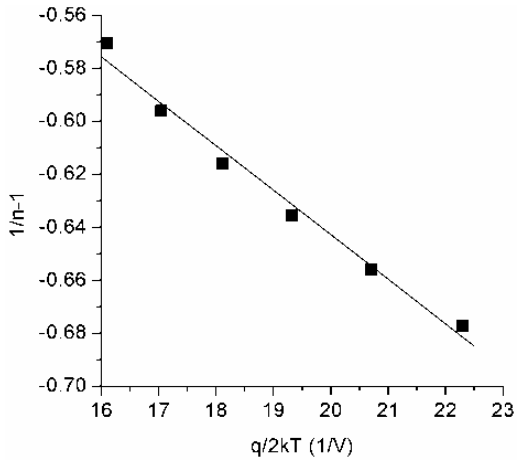

Figure 10. The 1/n-1 versus q/2kT curve of Ti/Au/n-AlGaAs Schottky barrier diode according to a Gaussian distribution of BHs. This plot represents a part of temperature values.

Values of 1.40 V, 0.20 V, -0.30, and -0.016 V were obtained for $\overline{\emptyset_{b0}}$, σ_0, $\rho_2$and ρ_3 respectively. This indicates the presence of interface inhomogeneities as σ_0 is not smaller than the $\overline{\emptyset_{b0}}$ mean value. The Richardson constant can now be evaluated by taking into account the Gaussian distribution of the barrier height by combining equations 12 and 15,

$$F=\ln(\frac{I_S}{T^2}) - \left(\frac{q^2\sigma_0^2}{2k^2T^2}\right) = \ln(A.A^*) - \frac{q\emptyset_{b0}}{kT} \qquad (17)$$

Plotting this modified function of the Richardson plot versus $q\emptyset_{b0}/kT$ gives the modified Richardson constant and the mean value of the barrier height. This plot is shown in figure 11.

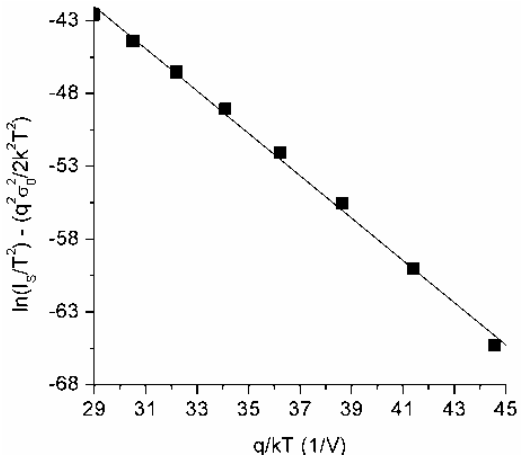

Figure 11. The modified Richardson function versus q/kT plot for the Ti/Au/n-AlGaAs Schottky barrier diode according to a Gaussian distribution of BHs.

The plot of modified Richardson according to equation (17) should give a straight line with the slope and intercept at the ordinate directly yield the mean barrier height and the Richardson constant. Using the least square curve fitting of the data, the value of A* is 103.21 A·cm^{-2}·K^{-2}wich is ten times greater than the theoretical value of 8.05 A·cm^{-2}·K^{-2} [18, 31]. This means that the inhomogeneous distribution of the barrier height is not the only factor responsible for the anomalous behavior. It has to be mentioned that the Richardson plot (I_0/T^2) versus 10^3/T is examined at 320 to 400K in order to make a comparison with literature [31, 32].

3.4. **Effect of trap**s

After showing that the inhomogeneous distribution of the barrier height is only partially responsible for the anomalous behavior, we will now investigate whether the presence of defects have a contribution to this effect using the SILVACO TCAD package numerical simulation [18]. It was assumed the presence of an acceptor trap located in the quantum well region with the following parameters: an activation energy$E_T = 0.44$ eV from the valence band, a density of $N_T = 4.4 \times 10^{14} cm^{-3}$, a capture cross section$\sigma_P = 1.86 \times 10^{-14} cm^2$. It was found that the traps have negligible effect on the forward I-V characteristics, from which the ideality factor is extracted as shown in figure 12. On the other hands traps have a bigger effect on the reverse characteristics. It may be explained by the fact that traps in the semiconductor behind the interface should not influence the current– that is

why it is Schottky diode; even more in the thermionic emission collisions in depletion layer are not assumed – electrons go over the barrier without collisions in the depletion layer. Obviously in this work, the main aim is not to compare simulation to measurement, but just to show whether traps can have an effect on the ideality factor or not. Detailed simulation was presented in one of our previous work [32]

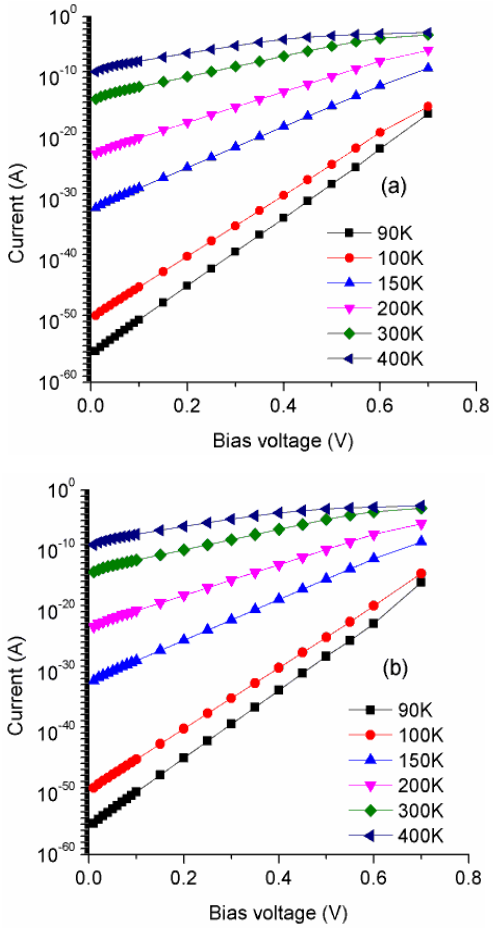

Figure 12. The simulated I-V characteristics in the absence (a) and presence (b) of traps in the Ti/Au/n-AlGaAs Schottky barrier diode.

3.5. Tunnelling current

Another effect which may have an influence on the unusual behaviour of the extracted diode parameters is the possibility of the presence of an important contribution of the tunnelling through the thin low barrier height. It has to be reminded that the barrier height actually decreases with decreasing temperature (figure 6). This decrease indicates the possibility of an increased contribution of the tunnelling current at lower temperatures. The tunnelling current is given by equation (6) above. The tunnelling energy E_0 can thus be extracted from the slope of the forward $\ln(I)$ versus $1/kT$ plot

neglecting the series resistance. Furthermore E_0 is also known as the tunnelling current parameter and is given by [33-36]:

$$E_0 = \eta \frac{kT}{q} = E_{00} coth\left(\frac{qE_{00}}{kT}\right) \qquad (18)$$

with $E_{00} = \frac{h}{4\pi}\sqrt{\frac{N_A}{m^* \varepsilon_0 \varepsilon_r}}$

The extracted tunnelling energy E_0 using equation (6) is compared to E_0 evaluated by (18) and are shown in figure 13 At low temperatures E_0 is much greater than kT. As the temperature increases the difference $E_0 - kT$ decreases. This means that the tunnelling current contribution to the total current is higher at low temperatures. Furthermore, the fact that the extracted tunnelling energy E_0 using equation (6) and E_0 evaluated by (18) are comparable also indicates the tunnelling is the dominant conduction mechanism at low temperatures. Comparable behaviour of the ideality factor is also attributed to tunnelling by [37].

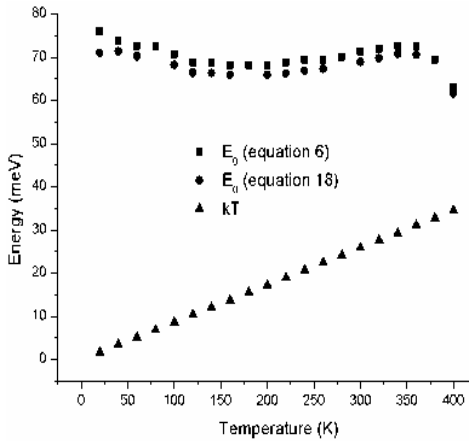

Figure 13. The extracted tunnelling energy (a) and current (b) versus temperature.

4. Conclusion

In this work Au/n-AlGaAs/n-GaAs multi quantum wells Schottky diodes were investigated by I-V techniques at temperatures ranging from 20 to 400 K. The diode parameters were then extracted from these characteristics and analysed to reveal the conduction mechanism involved. The apparent ideality factor, assuming thermionic conduction mechanism, was found to increase with decreasing temperature and it reaches a very high value of ~20 at 20 K. A combination of analytical modelling and numerical simulation were carried out to elucidate these unusual values of the ideality factor. The numerical simulation revealed that the high values of the ideality factor are not a result of the presence of traps. The analytical modelling has confirmed that at low temperatures the tunnelling mechanism is

dominant and hence the ideality factor is an artefact of assuming a thermionic conduction mechanism which proved to be wrong assumption. It has also to be mentioned that measurement at such low temperature as 20 K is connected with freezing of the carriers, this effect should be mentioned and taken into account by explanation of the barrier height limiting to zero at very low temperatures, the semiconductor has practically no free carriers and the theory of the transport through the interface is in problems for such low temperatures.

References

[1] C.H. Liu, T.K. Lin, S.J. Chang, GaAs MOS capacitorswith photo-CVD SiO_2 insulator layers, Solid-State Electron. 49 (2005) 1077-80.

[2] S.M. Sze, Physics of Semiconductor Devices, second ed., Wiley, New York, 1981.

[3] A.K. Ghosh, T. Feng, J.I. Haberman, H.P. Maruska, Effects of interfacial charge on the electron affinity, work function, and electrical characteristics of thinly oxidized semiconductor-insulator-semiconductor and metal-insulator-semiconductor devices, J. Appl. Phys. 55 (1984) 2990-4.

[4] K.K. Ng, H.C. Card, Asymetry in the SiO_2 tunneling barriers to electrons and holes, J. Appl. Phys. 51 (1980) 2153-7.

[5] Sassen S, Witzigmann B, Wolk C, Brugger H. Barrier height engineering on GaAs THz Schottky diodes by means of high-low doping, InGaAs- and InGaP-layers. IEEE Trans Electro Dev 2000; 47:24–32.

[6] Yu Z, Schablitsky SJ, Chou SY. NanoscaleGaAs metal–semiconductor–metal photodetectors fabricated using nanoimprint lithography, Appl Phys Lett 1999; 74:2381–3.

[7] Y. Hasegawa, T. Egawa, T. Jimbo, M. Umeno, GaAs-basedLED on Si substrate with GaAs islands active region by droplet-epitaxy, Appl. Surf. Sci. 100–101 (1996) 482-6.

[8] A.G.U. Perera, Heterojunction and superlattice detectors for infrared to ultraviolet, Progress in Quantum Electronics 48(2016) 1–56.

[9] P.K.D.D.P. Pitigala, P.V.V. Jayaweera, S.G. Matsik, A.G.U. Perer, H.C. Liu, Highly sensitive GaAs/AlGaAs heterojunction bolometer, Sensors and Actuators A 167 (2011) 245–248.

[10] Elnaz Nazemi, SrivatsaAithal, Walid M. Hassen, Eric H. Frosta, Jan J. Dubowskia, GaAs/AlGaAs heterostructure based photonic biosensor for rapid detection of Escherichia coli in phosphate buffered saline solution, Sensors and Actuators B 207 (2015) 556–562

[11] J.L. Everaert, R.L. Van Meirhaeghe, W.H. Laflere, F. Cardon, Characterisation of CoSi2/- and TiSi2/n-GaAs Schottky barriers, Semicond. Sci. Technol. 5 (1990) 60-4.

[12] A.B. Mclean, R.H. Williams, Schottky contacts to cleaved GaAs (110) surfaces. I. Electrical properties and microscopic theories, J. Phys. C: Solid State Phys. 21 (1988) 783-806.

[13] S. Karatas, S. Altındal, Temperature dependence of barrier heights of Au/n-type GaAs Schottky diodes, Solid-State Electron. 49 (2005) 1052-4.

[14] M. Soylu, F. Yakuphanoglu, Analysis of barrier height inhomogeneity in Au/n-GaAs Schottky barrier diodes by Tung model, J. Alloys Compd. 506 (2010) 418-22.

[15] S. Karatas, S. Altındal, Analysis of I–V characteristics on Au/n-type GaAs Schottky structures in wide temperature range, Mater. Sci. Eng., B 122 (2005) 133-9.

[16] J. Osvald, Temperature dependence of barrier height parameters of inhomogeneous Schottky diodes, Microelectron. Eng. 86 (2009) 117-20.

[17] F. Nutku, A. Erol, M. Gunes, L.B. Buklu, Y. Ergun, M.C. Arikan, I–V characterization of a quantum well infrared photodetector with stepped and graded barriers, Superlattices and Microstructures 52 (2012) 585–593.

[18] SILVACO-TCAD, ATLAS User's Manual: Device simulation software, SILVACO International, California, 2004.

[19] K. Takahashi, A. Yoshikawa, A. Sandhu, Wide Bandgap Semiconductors: Fundamental Properties and Modern Photonic and Electronic Devices, Springer, Berlin, 2007.

[20] S.S. Naik,V.R. Reddy, Analysis of current-voltage-temperature (I-V-T) andcapacitance-voltage-temperature (C-V-T) characteristics of Ni/Au Schottky contacts on n-type InP, Superlattices and Microstructures 48 (2010) 330-342.

[21] R. Boumaraf, N. Sengouga , R.H. Mari , Af. Meftah, M. Aziz, Dler Jameel, Noor Al Saqri, D. Taylor, M. Henini, Deep traps and temperature effects on the capacitance of p-type Si-doped GaAs Schottky diodes on (211) and (311) oriented GaAs substrates, Superlattices and Microstructures 65 (2014) 319–331.

[22] S. K. Cheung and N. W. Cheung, Extraction of Schottky diode parameters from forward current-voltage characteristics, Appl. Phys. Lett., vol. 49, no. 2, pp. 85–87, 1986.

[23] D. A. Aldemir, A. Kökce, and A. F. Özdemir,Temperature dependent ideality factor and barrier height of Ni/n-GaAs/In Schottky diodes, Microelectronic Engineering, 98 (2012), 6-11.

[24] S. Saadaoui, M. M. Ben Salem, M. Gassoumi, H. Maaref, and C. Gaquiere, Electrical characterization of (Ni/Au)/Al0.25Ga0.75N/GaN/SiC Schottky barrier diode, Journal of Applied Physics, 110 (2011), 013701.

[25] R. Sharma, Temperature Dependence of I-V Characteristics of Au/n-Si Schottky Barrier Diode, Journal of Electron Devices, 8 (2010), 286-292.

[26] A. Bobby, N. Shiwakoti, and B. K. Antony, Theoretical and experimental analysis of barrier distribution in nearly ideal Schottky diodes, In the Proceedings of the 59th DAE Solid State Physics Symposium, 16–20 December 2014, Tamilnadu, India, pp. 110001-1 - 110001-3.

[27] Nezir Yildirim, Kadir Ejderha, and Abdulmecit Turut, On temperature-dependent experimental I-V and C-V data of Ni/n-GaN Schottky contacts, Journal of Applied Physics, 108, (2010), 114506-1 - 114506-8.

[28] F.E. Cimilli, M. Saglam, H. Efeoglu, and A. Turut, Temperature-dependent current–voltage characteristics of the Au/n-InP diodes with inhomogeneous Schottky barrier height, Physica B, 404, (2009) 1558–1562.

[29] J. H. Werner and H. H.Guttler, Barrier inhomogeneities at Schottky contacts. J Appl Phys, 1991, 69: 1522

[30] M. K. Hudait and S. B. Krupanidhi, Doping dependence of the barrier height and ideality factor of Au/n-GaAs Schottky diodes at low temperatures, Physica B: Physics of Condensed Matter 307 (2001) 125-137.

[31] Ç. Ş. Güçlü · A. F. Özdemir, · Ş. Altindal, Double exponential I–V characteristics and double Gaussian distribution of barrier heights in (Au/Ti)/Al2O3/n-GaAs (MIS)-type Schottky barrier diodes in wide temperature range, Appl. Phys. A (2016) 122:1032.

[32] K. Zeghdar, L. Dehimi, A. Saadoune, N. Sengouga, Inhomogeneous barrier height effect on the current–voltage characteristics of an Au/n-InP Schottky diode, Journal of Semiconductors, Vol. 36, No. 12, Dec. 2015.

[33] E.H. Rhoderick, R.H. Williams, Metal–Semiconductor Contacts, second ed., Clarendon Press, Oxford, 1988.

[34] H.C. Card, E.H. Rhoderick, Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes, J. Phys. D: Appl. Phys. 4 (1971) 1589.

[35] H.C. Card, E.H. Rhoderick,Studies of tunnel MOS diodes II. Thermal equilibrium considerations, J. Phys. D: Appl. Phys. 4 (1971) 1602

[36] Ş Altındal, I. Dökme, M. M. Bülbü, N. Yalçın, T. Serin, The role of the interface insulator layer and interface states on the current-transport mechanism of Schottky diodes in wide temperature range, Microelectronic Engineering 83 (2006) 499–505.

[37] H. Tecimer, A. Türüt, H. Uslu, S¸ . Altındal, ˙I. Uslu, Temperature dependent current-transport mechanism in Au/(Zn-doped)PVA/n-GaAs Schottky Barrier Diodes (SBDs), Sensors and Actuators: A Physical (2013).