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The Alternate Arm Converter (AAC) – “Short-Overlap” Mode Operation – Analysis and Design Parameter Selection

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Abstract—This paper presents converter operation principles and theoretical analyses for “short-overlap” mode operation of the Alternate Arm Converter (AAC), which is a type of modular multilevel Voltage Source Converter (VSC) that has been proposed for HVDC transmission applications. Fourier series expressions for the ideal arm current and reference voltage are derived, for the first time, in order to develop an expression for the sub-module capacitance required to give a selected peak-peak voltage ripple of the summed sub-module capacitor voltages in an arm. The DC converter current contains non-negligible low order even harmonics; this is verified by deriving, for the first time, a Fourier series expression for this current. As the DC converter current needs to be filtered to form a smooth DC grid current, a novel DC filter arrangement is proposed, which uses the characteristics of a simplified DC cable model, as well as the capacitance of the DC link and additional DC link damping resistance, in order to form a passive low pass filter. Results obtained from a simulation model, which is based on an industrial HVDC demonstrator, are used in order to verify the presented converter operation principles and theoretical analyses.

Index Terms—AC-DC power conversion, DC-AC power conversion, HVDC converters, HVDC transmission, Multilevel systems.

I. INTRODUCTION

THERE is currently a great deal of interest in transmitting bulk power by using HVDC systems, for a number of reasons, such as allowing asynchronous AC networks to be connected. Additionally, when transmitting bulk power over a distance greater than 400-700 km and 25-50 km for overhead lines and for submarine cables, respectively, using HVDC is more favourable than HVAC because the total cost is lower [1]–[4]. Furthermore, as the HVAC submarine cable transmission distance increases, there becomes a point at which the shunt capacitive charging current equals the

cable current rating, and therefore HVAC submarine cable transmission distances are limited [1], [5].

As a HVDC system connects AC networks together, converter station equipment is required to convert from AC to DC, or vice versa. Initially, HVDC systems only comprised Line Commutated Converters (LCCs) [6], and later also comprised two-level Voltage Source Converters (VSCs) or three-level Neutral Point Clamped (NPC) VSCs [6], [7]. Cascaded type converters, which use series connected bridges to provide “wave-shaping” functionality, have been used for some time with only capacitors on the DC side for Static Synchronous Compensator (STATCOM) applications [8]. In 2003, a type of modular multilevel VSC, termed the Modular Multilevel Converter (MMC), was proposed for HVDC transmission applications [9]. Each arm comprises an inductor and a series connection of sub-modules. The first commercial application of HVDC-MMC was the Trans Bay Cable project, where there are 216 sub-modules per arm [10], [11]. Each sub-module comprises a local floating capacitor and semiconductor devices, which are typically IGBTs with anti-parallel diodes. As hundreds of converter voltage levels are available, a switching frequency of only a few multiples of the fundamental frequency is necessary in order to synthesise a converter voltage with a low enough Total Harmonic Distortion (THD) so that dedicated AC side filtering equipment is not required [9], [12], [13]. The overall efficiency of a HVDC-MMC station is approximately 99% [14].

This paper focuses on the Alternate Arm Converter (AAC), which is a type of modular multilevel VSC that has been proposed for HVDC transmission applications. The AAC was developed in order to provide a number of advantages over its predecessor – the MMC – such as improved attributes for handling DC side faults and requiring fewer sub-modules with a smaller capacitance [15]–[19]. The AAC was first published in 2010 [20] and was then initially discussed further in [21], relating to the original “short-overlap” mode of operation (“overlap” state angular duration of typically 15-18°). To date, the AAC is yet to seek a commercial application because the research and development phase is still ongoing. A 20 MW AAC simulation model was reported to have an efficiency of 98.85% in [22].

In [17], [18], the sizing of the sub-module capacitors in the AAC and MMC were compared by analyses and then validated by simulations. In order to have a continuous analytical AAC model, without requiring Fourier analysis,

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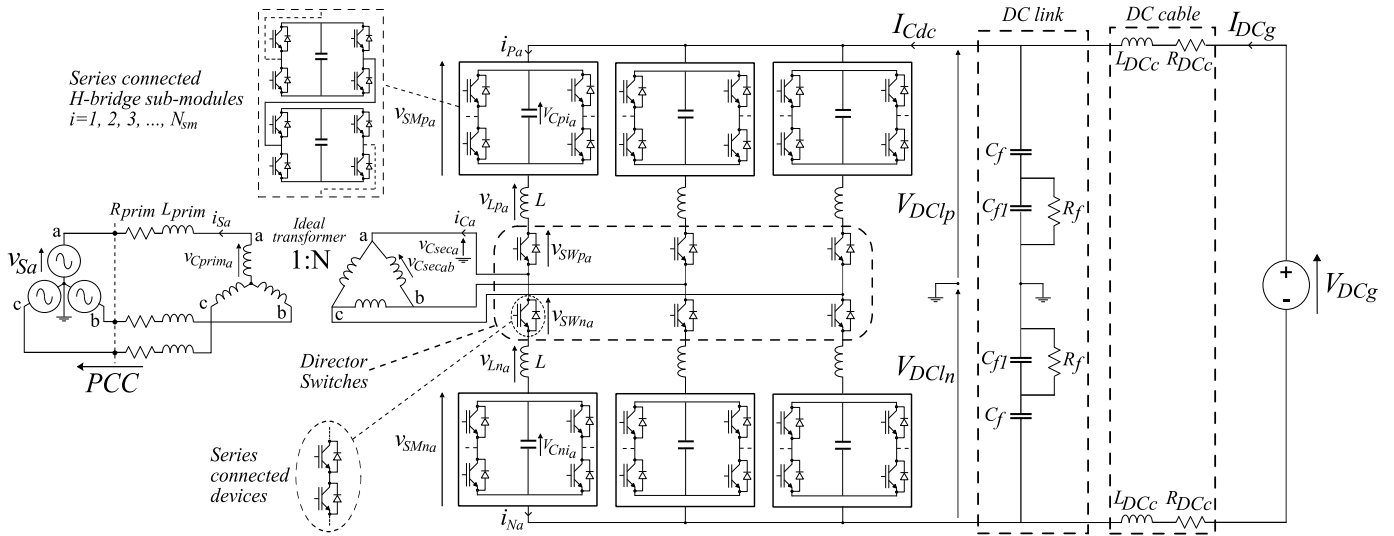


Fig. 1. Alternate Arm Converter (AAC) schematic

each arm was assumed to conduct the entire AC converter current for half a fundamental period. In fact, during the two “overlap” states per fundamental period, each arm in a phase-leg conducts half the AC converter current, as well as a DC side circulating current. The results revealed that the AAC sub-module capacitance can be approximately half that of the MMC in order to give the same maximum peak-peak sub-module capacitor voltage deviation, around the real and reactive power operation envelope. This is beneficial because the physical size and weight of a sub-module is dominated by the sub-module capacitor [20]. Additionally, when compared to an equivalently rated MMC, the number of sub-modules required by the AAC is typically between 30-40% fewer [19].

In previous work for “short-overlap” mode operation [15], [16], [22]–[24], the DC link capacitor, and a parallel connected inductor and resistor located between the DC link and the external DC connection, were used in order to form a smooth DC grid current, from a DC converter current which contains non-negligible low order even harmonics. This DC filter arrangement has the advantage of being ideally lossless, due to the resistor being connected in parallel with the inductor. However, when a HVDC link is connected to the DC filter, as opposed to being connected to a stiff DC voltage source, the characteristics of the HVDC link will dominate the DC filter characteristics.

An alternative “extended-overlap” mode of operation for the AAC was proposed in [25], [26] and was utilised in [27]. By using an “overlap” state angular duration of 60° , a continuous DC current conduction path is available, with respect to the DC side. This benefits the AAC by ideally eliminating the DC converter current ripple, thereby easing DC side filtering requirements. When operating with only a fundamental secondary-side converter voltage component, extending the “overlap” state duration increases the required voltage rating of the series connection of sub-modules in each arm. As the nominal sub-module capacitor voltage is usually

already limited by the capacitor and semiconductor device voltage ratings, increasing the number of sub-modules per arm negatively impacts the cost and efficiency of the converter. However, adding a zero sequence component to the secondary-side converter voltages, which is not present on the primary-side due to using a wye-delta transformer, reduces the required voltage rating of the series connection of sub-modules in each arm by “flattening” the secondary-side converter voltage zero-crossings, at the expense of increased secondary-side AC to ground voltage stress and increased director switch voltage rating, when compared to an AAC operating in the “short-overlap” mode [19]. The number of sub-modules required for “extended-overlap” operation with zero sequence injection is ideally equal to that for “short-overlap” operation without zero sequence injection, whereas the director switch voltage rating is 59% higher for “extended-overlap” operation [19]. Note that, the zero sequence voltages which are typically applied in “extended-overlap” mode or in conventional VSCs have the effect of “flattening” the secondary-side converter voltage zero-crossings or the peaks and troughs, respectively [19], [28]. However, their purpose is the same – the maximum fundamental converter voltage which can be synthesised is increased, for given ratings.

This paper presents a detailed analysis of the AAC in “short-overlap” mode operation so that the selection of key design parameters can be made. The considered parameters are the sub-module capacitance and the parameters of a novel DC side filter arrangement (noting that the DC side filter is an important consideration for “short-overlap” mode operation). The analytical approach taken to derive a continuous expression for the summed sub-module capacitor energy in an arm, in order to then find the sub-module capacitance required for a selected peak-peak voltage ripple, also lends itself well to deriving a continuous expression for the DC converter current, which is then used to design and analyse the proposed DC side filter arrangement.

The remainder of this paper is organised as follows. In Section II, the AAC topology is described and converter operation, for the case when operating without zero sequence voltage injection in the “short-overlap” mode, is explained. The Conseil International des Grands Réseaux Électriques (CIGRÉ) DC grid test system is summarised in Section III in order to justify the selection of the relevant parameters and test cases. By deriving, for the first time, Fourier series expressions for the ideal arm current and reference voltage, an expression for the sub-module capacitance required to give a selected peak-peak voltage ripple of the summed sub-module capacitor voltages in an arm is developed in Section IV. In Section V, a Fourier series expression for the DC converter current is derived, for the first time, in order to verify that this current contains non-negligible low order even harmonics. Furthermore, as the DC converter current needs to be filtered in order to form a smooth DC grid current, a novel DC filter arrangement is proposed, where a passive low pass filter is formed by the characteristics of a simplified DC cable model, as well as the capacitance of the DC link and additional DC link damping resistance. As implementing a full switching simulation model of the CIGRÉ DC grid test system would not have been feasible, a relatively small scale HVDC demonstrator is described in Section VI, which is used as the simulation exemplar. The per unit values of the CIGRÉ DC grid test system and of the HVDC demonstrator are equal, where possible. In Section VII, the results obtained from the AAC simulation model are used in order to validate the presented converter operation principles and theoretical analyses. Finally, conclusions are drawn in Section VIII.

II. CONVERTER TOPOLOGY AND OPERATION

The AAC is illustrated in Fig. 1. Each arm comprises an inductor, a series connection of H-bridge sub-modules and a director switch. The maximum director switch blocking voltage, V_{SWmax} , equals $V_{DCI}/2 + \hat{V}_{Csecx}^{ref} - N_{sm}V_{CAPnom}$ (see Figs. 2 and 3). In a HVDC system, each director switch can be formed by a series connection of IGBTs with anti-parallel diodes so that the required director switch blocking voltage can be reached.

Typical waveforms are shown in Fig. 2, for the case when the AC converter current, i_{Cx} , is in-phase with the reference secondary-side converter voltage, v_{Csecx}^{ref} , and when the “overlap” state angular duration equals 18° . During half a fundamental period, the AAC uses two director switch combinations per phase-leg. In the first interval, which occupies the majority of the half fundamental period, only one director switch is closed, and in the second interval, which is centred about the zero crossings of the converter voltage in Fig. 2, both director switches are closed.

When only one director switch is closed, the sub-modules in this arm are solely responsible for synthesising the reference converter voltage by using the modulating waveform of this arm, as shown in Fig. 2a). Furthermore, this arm conducts all of the AC converter current, as seen in Fig. 2b). The intervals when only the positive or only the negative arm director switches are closed are termed the “positive arm active” and

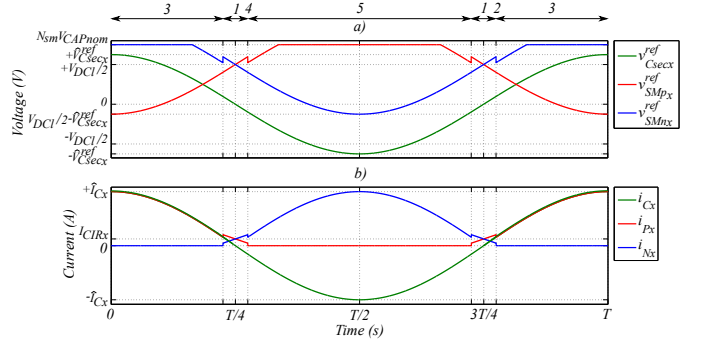


Fig. 2. Typical AAC a) reference secondary-side converter voltage, and positive and negative arm modulating waveforms, and b) AC converter current, and positive and negative arm currents

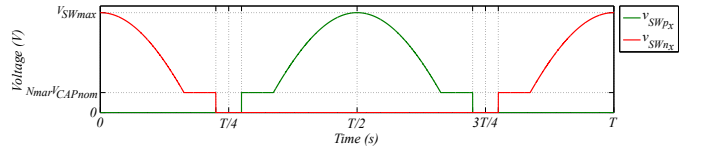


Fig. 3. Typical AAC positive and negative arm director switch voltages

“negative arm active” converter operation states, respectively, and denoted by ‘3’ and ‘5’ in Fig. 2, respectively.

The interval in which both director switches are closed, termed the “overlap” state and denoted by ‘1’ in Fig. 2, aids with sub-module capacitor voltage regulation by introducing a controllable DC side circulating current, I_{CIRx} , as discussed in [23]. The circulating current flows in both arms, in addition to half the AC converter current flowing in each arm, as seen in Fig. 2b). The arm inductors allow the circulating current to be controlled with a hysteresis controller by appropriately modulating both the positive and negative arm sub-modules [not shown in Fig. 2a) for the sake of clarity], as well as the reference converter voltage being synthesised by using both the positive and negative arm modulating waveforms shown in Fig. 2a). At the end of the “overlap” state, a similar current control procedure is used to force the opening director switch arm current to zero before this switch is actually opened, thereby implementing zero current director switch turn-off functionality. The intervals when the positive arm or the negative arm current are forced to zero are termed the “positive arm director switch opening” and “negative arm director switch opening” states, respectively, and are denoted by ‘4’ and ‘2’ in Fig. 2, respectively.

When an arm is not synthesising the reference converter voltage, the series connection of sub-modules in this arm are modulated so that the director switch voltage in this arm is kept positive; this ensures that the director switch anti-parallel diodes remain reversed biased. However, each series connection of sub-modules can only generate a nominal maximum voltage of $N_{sm}V_{CAPnom}$, as shown in Fig. 2a). Fig. 3 shows that the director switch voltages are always $\geq N_{mar}V_{CAPnom}$, where N_{mar} is chosen so that the director switch voltages remain positive during all steady-state and transient conditions.

The maximum voltage required by the series connection of sub-modules, due to reference converter voltage synthesis, occurs at the start and end of the “overlap” state. At these two points, one of the arm modulating waveforms is greater than half the DC link voltage, but less than the total DC link voltage. The maximum voltage depends on the chosen duration of the “overlap” state and on the peak reference converter voltage. Additionally, the number of sub-modules in each arm which are used to control the circulating current during the “overlap” state, and therefore cannot be used for reference converter voltage synthesis, needs to be considered because this requirement further increases the maximum voltage required.

Typical AC converter currents and positive arm currents are shown in Figs. 4a) and b), respectively. With the phase-leg operation principle described above, the DC converter current, I_{Cdc} , has harmonics at multiples of six times the fundamental frequency because the director switch combinations, which are tabulated in Fig. 4, cause this current to be chopped between the AC converter currents, with a repetition interval of 60° , as seen in Fig. 4c). Additionally, the DC converter current includes the circulating current during the six “overlap” states per fundamental period. As the AC converter current and secondary-side converter voltage approach quadrature, the DC converter current ripple increases. Furthermore, during asymmetrical faulted AC grid conditions, the DC converter current contains harmonics at even multiples of the fundamental frequency [24]. The DC converter current needs to be filtered in order to form a smooth DC grid current, I_{DCg} , which, in steady-state, ideally equals the mean DC converter current, as seen in Fig. 4c). The novel DC filter arrangement utilised in this work is described in Subsection V-B.

The transformer turns ratio, N , is set so that, ideally, the converter has an inherent AC and DC side power balance, and therefore no DC side circulating currents are required, at the operating point where the AC side real and reactive powers are zero; this is termed the “sweet-spot” [22]. At the “sweet-spot”, the secondary-side converter voltage is 27% greater than half the DC link voltage; this is why the AAC comprises H-bridge sub-modules. As the ‘-1’ sub-module state is available, the maximum positive converter voltage which could be generated equals $+V_{DC1}/2 - N_{sm}(-V_{CAPnom})$. The controlled circulating currents, which aid with sub-module capacitor voltage regulation, maintain the AC and DC side power balance across the entire real and reactive power operating envelope. However, these circulating currents are minimised due to the selected transformer turns ratio enabling converter operation around the “sweet-spot”.

III. CIGRÉ DC GRID TEST SYSTEM

In order to enable selection of relevant parameters and test cases for this work, the exemplar HVDC system used has been based on the CIGRÉ DC grid test system, which is comprehensively described in [29]. A number of ratings used in this work have been based on converter “Cm-A1”, which interfaces onshore AC network ‘A’ with DC subsystem “DCS1”; this part of the test system is depicted in Fig. 5.

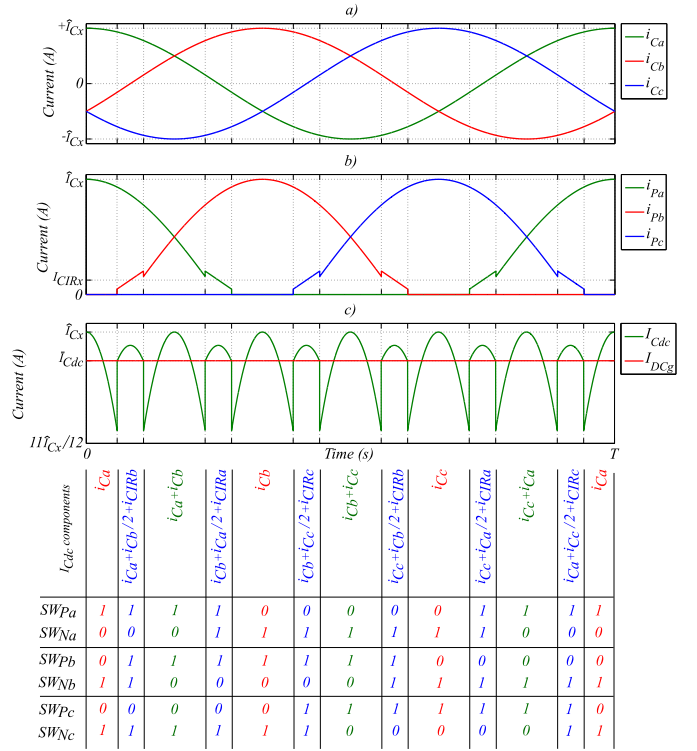


Fig. 4. Typical AAC a) AC converter currents, b) positive arm currents, c) DC converter and DC grid currents, and table of director switch combinations

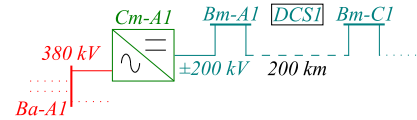


Fig. 5. Selected section of the CIGRÉ DC grid test system

Converter “Cm-A1” has an apparent power, S_{base} , of 800 MVA, onshore AC network ‘A’ is rated at 380 kV, and DC subsystem “DCS1” is a two terminal, symmetric monopole HVDC link, rated at ± 200 kV. The per unit value of the transformer leakage inductance, L_{TFpu} , equals 18%. The rated reactive power, Q_{base} , has been selected to be 40% of the rated real power, P_{base} . The nominal sub-module capacitor voltage, V_{CAPnom} , has been set to 1.5 kV so that sub-modules could safely comprise IGBT and anti-parallel diode modules with a voltage rating of 3.3 kV.

On the primary-side of the transformer, the base current and impedance ($I_{BASEprim}$ and $Z_{BASEprim}$) are defined by (1) and (2), respectively. The absolute value of the transformer leakage inductance, L_{TF} , is found by using (3), where ω_0 is the nominal fundamental angular frequency. On the DC side of the converter, the base current and impedance (I_{BASEdc} and Z_{BASEdc}) are defined by (4) and (5), respectively. The per unit value of the nominal sub-module capacitor voltage, $V_{CAPnom,pu}$, is found by using (6). The ratings and values described above, for the selected part of the DC grid test system, are tabulated in the middle column of Table I.

$$I_{BASEprim} = \frac{S_{base}}{\sqrt{3}V_{Su}} \quad (1)$$

TABLE I
SYSTEM PARAMETERS

Parameter	CIGRÉ DC grid test system	HVDC demonstrator
S_{base} (MVA)	800	21.54
P_{base} (MW)	742.78	20
Q_{base} (MVar)	297.11	8
V_{Sll} (kV)	380	11
$I_{BASEprim}$ (kA)	1.22	1.13
$Z_{BASEprim}$ (Ω)	180.5	5.62
L_{TF} (mH)	103.4	3.22
L_{TFpu} (%)	18	18
V_{DCg} (kV)	400 (± 200)	20 (± 10)
I_{BASEdc} (kA)	1.86	1
Z_{BASEdc} (Ω)	215.41	20
V_{CAPnom} (kV)	1.5	1.5
$V_{CAPnompu}$ (%)	0.375	7.5

TABLE II
SUBMARINE CABLE PARAMETERS

Parameter	CIGRÉ DC grid test system	HVDC demonstrator
R'_{DCc} (m Ω /km)	9.5	0.882
R_{DCc} (Ω)	1.9	0.1764
R_{DCcpu} (%)	0.88	0.88
L'_{DCc} (mH/km)	2.111	0.196
L_{DCc} (mH)	422.2	39.2
L_{DCcpu} (%)	61.58	61.58
C'_{DCc} (μ F/km)	0.2104	2.266
C_{DCc} (μ F)	42.08	453.2
C_{DCcpu} (%)	35.12	35.12

$$Z_{BASEprim} = \frac{V_{Sll}^2}{S_{base}} \quad (2)$$

$$L_{TF} = \frac{L_{TFpu} Z_{BASEprim}}{\omega_0} \quad (3)$$

$$I_{BASEdc} = \frac{P_{base}}{V_{DCg}} \quad (4)$$

$$Z_{BASEdc} = \frac{V_{DCg}^2}{P_{base}} \quad (5)$$

$$V_{CAPnompu} = \frac{V_{CAPnom}}{V_{DCg}} \quad (6)$$

The ± 200 kV HVDC link is a 200 km submarine cable and its parameters are tabulated in the middle column of Table II. The distributed DC cable model parameters per kilometre are denoted by R'_{DCc} , L'_{DCc} and C'_{DCc} , and the lumped 200 km DC cable model parameters are denoted by R_{DCc} , L_{DCc} and C_{DCc} . The lumped DC cable per unit resistance, inductance and capacitance are calculated by using (7), (8) and (9), respectively.

$$R_{DCcpu} = \frac{R_{DCc}}{Z_{BASEdc}} \quad (7)$$

$$L_{DCcpu} = \frac{\omega_0 L_{DCc}}{Z_{BASEdc}} \quad (8)$$

$$C_{DCcpu} = \frac{1}{\omega_0 C_{DCc} Z_{BASEdc}} \quad (9)$$

IV. SUB-MODULE CAPACITANCE

The sub-module capacitance time constant is introduced in Subsection IV-A and the sub-module capacitance selection procedure is described in Subsection IV-B.

A. Sub-Module Capacitance Time Constant

The sub-module capacitance time constant, defined by (10), can be used in order to fairly compare converters with different power ratings and/or an unequal number of sub-modules. This time constant defines the ratio between the electrostatic energy stored in all of the sub-module capacitors and the rated real power [30].

$$\tau = \frac{6E_{nom}}{P_{base}} = \frac{6N_{sm} \frac{1}{2} C_{sm} V_{CAPnom}^2}{P_{base}} \quad (10)$$

When the series connection of sub-modules in each arm is selected to be rated in order to provide a maximum voltage of $3/2 \times V_{DCg}/2$, the number of sub-modules per arm is defined by (11). Additionally, with reference to Subsection IV-B, selecting the per unit peak-peak voltage ripple, for the summed sub-module capacitor voltages in an arm, to equal 13.7%, results in a sub-module capacitance time constant of 14.5 ms.

$$N_{sm} = \left\lceil \frac{\frac{3}{2} \frac{V_{DCg}}{2}}{V_{CAPnom}} \right\rceil \quad (11)$$

B. Sub-Module Capacitance Selection

In order to analytically size the sub-module capacitance to give a selected peak-peak voltage ripple for the summed sub-module capacitor voltages in an arm, a number of simplifications and assumptions are made:

- Due to the AAC positive and negative arm symmetry, only the positive arm is analysed.
- The duration of the “positive arm director switch opening” and “negative arm director switch opening” states are assumed to be negligible.
- The effect of the arm inductors on the converter voltage is assumed to be negligible.
- Only ideal steady-state arm current and reference voltage waveforms are examined.
- In steady-state, the average duty cycle of each sub-module is assumed to be equal, due to the implementation of an effective sub-module rotation algorithm [23], [31].

By finding the maximum summed capacitor energy in an arm, an analytical procedure for determining the minimum sub-module capacitance required by a MMC in order to not exceed the sub-module voltage rating is presented in [28]. The procedure presented here for determining the maximum and minimum summed sub-module capacitor energies in an AAC arm (and hence the capacitance for a given peak-peak voltage ripple specification) is conceptually similar to that presented in [28], but is analytically more tedious, due to the arm currents and voltages having a discontinuous nature. The analytical details of the presented procedure are given

in Appendix A and the method outline is described here. Firstly, it is recognised that the maxima and minima of the arm energy occur at the instants when the instantaneous arm power is zero. These instants coincide with times when either the arm current or the arm voltage are zero, and are readily found from (12) and (13), respectively. Using the Fourier series approach detailed in Appendix A, it is possible to arrive at a continuous expression for the arm energy, as given in (39). Evaluating this expression at the zero power instants yields the maximum and minimum arm energies. Re-expressing these energies in terms of the capacitance, and the maximum and minimum summed capacitor voltages in an arm enables the expression in (14) to be derived, which can be solved to yield the capacitance required to meet the given peak-peak voltage ripple specification. Again, the analytical details are tedious, and are therefore given in Appendix A in (41) – (47).

Over a fundamental period, the positive arm current and reference voltage are defined by discontinuous expressions, due to the arm sequentially adopting the “overlap”, “positive arm active”, “overlap” and “negative arm active” states, as a consequence of the director switch combinations given in Fig. 4. The discontinuous expressions for the positive arm current and reference voltage are defined by (12) and (13), respectively, where α_x is the phase of the AC converter current with respect to the AC supply voltage, δ_x is the phase of the reference secondary-side converter voltage with respect to the AC supply voltage, and Φ_{OVx} is the angular duration of the “overlap” state.

$$i_{Px}(t) = \begin{cases} \frac{\hat{I}_{Cx}}{2} \sin(\omega_0 t + \alpha_x) + I_{DCcir_x} & \text{if } k_1 \leq t < k_2 \\ \hat{I}_{Cx} \sin(\omega_0 t + \alpha_x) & \text{if } k_2 \leq t < k_3 \\ \frac{\hat{I}_{Cx}}{2} \sin(\omega_0 t + \alpha_x) + I_{DCcir_x} & \text{if } k_3 \leq t < k_4 \\ 0 & \text{if } k_4 \leq t < k_5 \end{cases} \quad (12a)$$

$$k_1 \equiv k_5 \equiv \frac{-\delta_x - \Phi_{OVx}/2}{\omega_0} \equiv \frac{2\pi - \delta_x - \Phi_{OVx}/2}{\omega_0} \quad (12b)$$

$$k_2 = \frac{-\delta_x + \Phi_{OVx}/2}{\omega_0} \quad (12c)$$

$$k_3 = \frac{\pi - \delta_x - \Phi_{OVx}/2}{\omega_0} \quad (12d)$$

$$k_4 = \frac{\pi - \delta_x + \Phi_{OVx}/2}{\omega_0} \quad (12e)$$

$$v_{SMpx}^{ref}(t) = \begin{cases} \frac{V_{DCI}}{2} - \hat{V}_{Csec_x} \sin(\omega_0 t + \delta_x) & \text{if } k_1 \leq t < k_2 \\ 0 & \text{if } k_2 \leq t < k_3 \end{cases} \quad (13a)$$

$$k_1 \equiv k_3 \equiv \frac{-\delta_x - \Phi_{OVx}/2}{\omega_0} \equiv \frac{2\pi - \delta_x - \Phi_{OVx}/2}{\omega_0} \quad (13b)$$

$$k_2 = \frac{\pi - \delta_x + \Phi_{OVx}/2}{\omega_0} \quad (13c)$$

The ideal waveform of the phase ‘a’ positive arm current, when operating with an “overlap” state angular duration of 18° at the positive rated real and reactive powers, is plotted in green in Fig. 6(a), when normalised to $\sqrt{2}I_{BASEsec}$. Positive

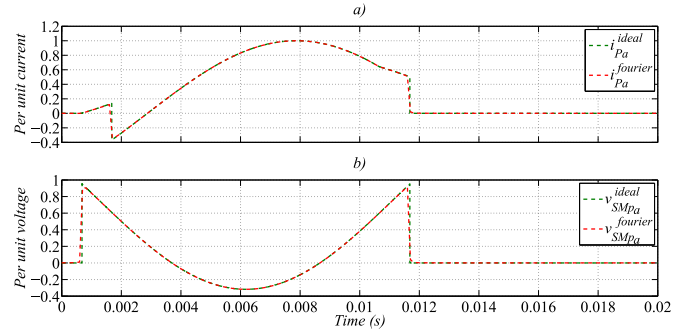


Fig. 6. Normalised ideal and Fourier series waveforms of the phase ‘a’ positive arm a) current and b) reference voltage

real power occurs when inverting and positive reactive power occurs when the AC supply current lags the AC supply voltage (inductive load). During the “overlap” state, the AC converter current is divided equally between the two arms and the circulating current flows through both arms. Throughout the “positive arm active” state, the AC converter current only flows through the positive arm and the circulating current does not flow. During the “negative arm active” state, no current flows through the positive arm.

The ideal waveform of the phase ‘a’ positive arm reference voltage used in this analysis is plotted in green in Fig. 6(b), when normalised to $\sqrt{2}V_{BASEsec}/\sqrt{3}$ ($V_{BASEsec} = NV_{BASEprim}$). During the “overlap” and “positive arm active” states, the positive arm reference voltage influences the stored energy in the positive arm because a non-zero current is flowing through this arm. Conversely, throughout the “negative arm active” state, the positive arm reference voltage does not influence the stored energy in the positive arm sub-module capacitors because the positive arm current is zero.

As the Fourier series of the positive arm current and reference voltage, developed in Appendix A, include an infinite sum, they are approximated when run in a MATLAB ‘.m’ script by using the first 1000 harmonics; this many harmonics are used due to the sharp edges visible in the ideal waveforms of Fig. 6, which are caused by the ideal instantaneous transitions between converter operation states. The normalised current and voltage Fourier series expressions are plotted in red in Figs. 6(a) and b), respectively. The ideal and Fourier series expressions for the instantaneous power and energy are plotted in Figs. 7(a) and b), respectively, when normalised to $E_{nom}f_0$ and to E_{nom} , respectively.

The result derived in Appendix A for the required sub-module capacitance to give a selected peak-peak voltage ripple for the summed sub-module capacitor voltages in an arm is shown in (14). The value of the sub-module capacitance to give a desired per unit peak-peak voltage ripple, κ , is found by solving (15) for the positive root.

$$0 = k_1 C_{sm}^2 + k_2 C_{sm} + k_3 \quad (14a)$$

$$k_1 = \frac{1}{4} N_{sm}^2 (\kappa V_{CAPnom})^4 - N_{sm}^2 \kappa^2 V_{CAPnom}^4 \quad (14b)$$

$$k_2 = (E_x^{max} - E_x^{min}) N_{sm} (\kappa V_{CAPnom})^2 -$$

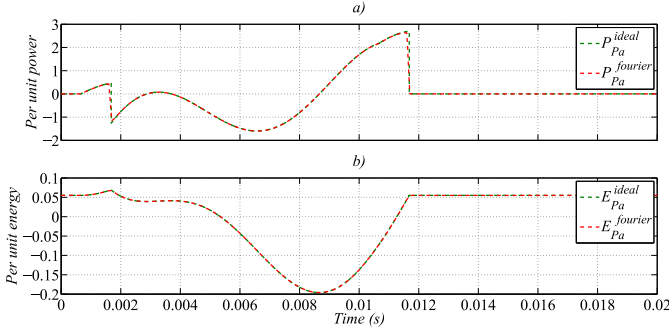


Fig. 7. Normalised ideal and Fourier series waveforms of the phase ‘a’ positive arm inserted sub-module capacitor instantaneous a) power and b) energy

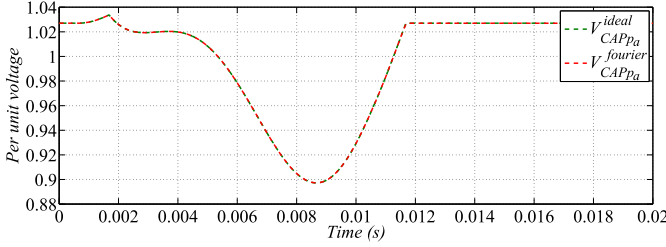


Fig. 8. Normalised phase ‘a’ positive arm summed sub-module capacitor voltage from the ideal and Fourier series expressions

$$2E_x^{max} N_{sm} (\kappa V_{CAPnom})^2 \quad (14c)$$

$$k_3 = (E_x^{max} - E_x^{min})^2 \quad (14d)$$

$$C_{sm} = \frac{-k_2 \pm \sqrt{k_2^2 - 4k_1 k_3}}{2k_1} \quad (15)$$

By using (14) and (15), selecting the AAC based the CIGRÉ DC grid test system ratings to have a per unit peak-peak voltage ripple of 13.7%, at the positive rated real and reactive powers, results in a sub-module capacitance of 8 mF, which is equivalent to 0.18% when using (16). The summed sub-module capacitor voltage is plotted in Fig. 8, when normalised to $N_{sm} V_{CAPnom}$. During normal AC grid conditions, this is the largest peak-peak voltage ripple across the real and reactive power operation envelope (see Fig. 17).

$$C_{sm_{pu}} = \frac{1}{\omega_0 C_{sm} Z_{BASEdc}} \quad (16)$$

V. DC LINK AND DC CABLE MODEL

This section considers the DC converter current, with the objective of deriving a continuous expression for this current, as described in Subsection V-A; this enables the development of the DC filter arrangement presented in Subsection V-B. However, the continuous expression for the DC converter current provides general analysis and could therefore be used for other DC filter designs.

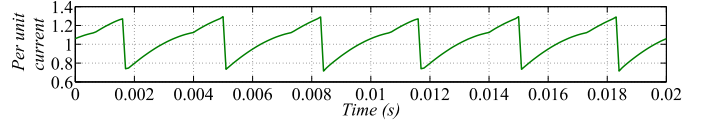


Fig. 9. Normalised DC converter current from the Fourier series expression

A. DC Converter Current Analysis

In this section, a continuous expression for the DC converter current is derived. Over a fundamental period, the DC converter current has twelve defined intervals, as a result of the twelve distinct director switch combinations given in Fig. 4. With reference to Fig. 4, when none of the phase-legs are in the ‘‘overlap’’ state, either two positive and one negative arm director switches are closed (green columns), or one positive and two negative arm director switches are closed (red columns). Therefore, the DC converter current equals the AC converter current of one phase or the inverse of the AC converter current of one phase (e.g. $-i_{Cc} = i_{Ca} + i_{Cb}$). When one phase-leg is in the ‘‘overlap’’ state, this phase-leg has both its director switches closed, another has only its positive arm director switch closed, and the third has only its negative arm director switch closed (blue columns). Therefore, the DC converter current equals half the AC converter current plus the circulating current of the phase-leg in the ‘‘overlap’’ state, in addition to one of the other two AC converter currents.

The six intervals, when one phase-leg is in the ‘‘overlap’’ state, are centred about multiples of $k60^\circ$, where $k \in \{0, 1, 2, 3, 4, 5\}$, minus δ_x of the phase-leg which is in the ‘‘overlap’’ state. The remaining six intervals occur when none of the phase-legs are in the ‘‘overlap’’ state. Two of the twelve aforementioned intervals are defined by (17) and a continuous expression for the DC converter current over a fundamental period is derived in Appendix B. The Fourier series of the DC converter current is plotted in Fig. 9, when normalised to I_{BASEdc} and when operating at the positive rated real and reactive powers. As the DC converter current contains non-negligible low order even harmonics, filtering is required. The filtering approach used in this work is described in Subsection V-B.

$$I_{Dc}(t) = \begin{cases} -\hat{I}_{Cb} \sin(\omega_0 t + \alpha_b) & \text{if } k_1 \leq t < k_2 \\ \hat{I}_{Ca} \sin(\omega_0 t + \alpha_a) + \frac{\hat{I}_{Cc}}{2} \sin(\omega_0 t + \alpha_c) + I_{cirDCc} & \text{if } k_2 \leq t < k_3 \end{cases} \quad (17a)$$

$$k_1 = \frac{-\delta_a + \Phi_{Ova}/2}{\omega_0} \quad (17b)$$

$$k_2 = \frac{\pi/3 - \delta_c - \Phi_{Ovc}/2}{\omega_0} \quad (17c)$$

$$k_3 = \frac{\pi/3 - \delta_c + \Phi_{Ovc}/2}{\omega_0} \quad (17d)$$

B. DC Link and DC Cable Model Design

As illustrated in Section V-A, the DC converter current has harmonics at multiples of six times the fundamental

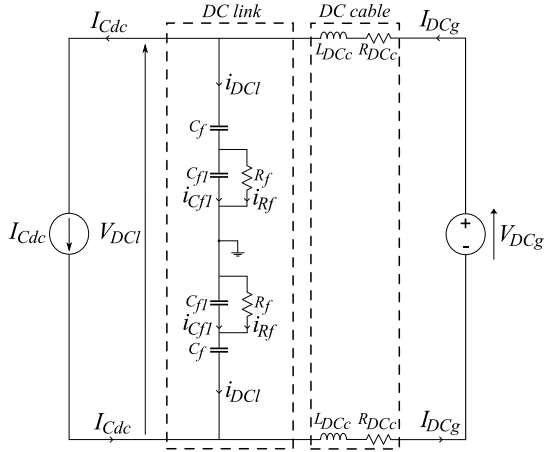


Fig. 10. DC link and DC cable model arrangement schematic

frequency during balanced AC grid conditions. Furthermore, as mentioned in Section II, this current has harmonics at even multiples of the fundamental frequency during asymmetrical faulted AC grid conditions [24]. Consequently, the DC converter current can be passively low-pass filtered, with a cut-off frequency of less than twice the fundamental frequency, in order to form a smooth DC current for the DC grid, during all AC grid conditions. In this paper, the filter arrangement depicted in Fig. 10 has been proposed. The characteristics of a DC cable model are used as part of the filter, along with the capacitances of the DC link (C_f and C_{f1}) and additional DC link damping resistance, R_f . The transient response between the DC converter current and the DC grid current is considered and typical waveforms are presented.

The distributed DC cable model for the CIGRÉ DC grid test system, described in Section III, has $200 R'_{DCc} L'_{DCc} C'_{DCc}$ sections. These sections combine to form a model of a 200 km ± 200 kV HVDC submarine cable. The design problem is simplified by neglecting the capacitive elements. However, the validity of doing so is shown in Fig. 19. The $200 R'_{DCc}$ and L'_{DCc} sections combine in series to form a lumped DC cable model with a resistance and inductance of R_{DCc} ($200 \times R'_{DCc}$) and L_{DCc} ($200 \times L'_{DCc}$), respectively. By using the equivalent model of Fig. 10, the transfer function between the DC converter and DC grid currents is found to be defined by (18).

$$\frac{I_{DCg}(s)}{I_{Cdc}(s)} = \frac{C_f R_f + C_{f1} R_f s + \frac{1}{C_f C_{f1} L_{DCc} R_f}}{s^3 + k_1 s^2 + k_2 s + \frac{1}{C_f C_{f1} L_{DCc} R_f}} \quad (18a)$$

$$k_1 = \frac{C_f L_{DCc} + C_f C_{f1} R_f R_{DCc}}{C_f C_{f1} L_{DCc} R_f} \quad (18b)$$

$$k_2 = \frac{C_f R_f + C_{f1} R_f + C_f R_{DCc}}{C_f C_{f1} L_{DCc} R_f} \quad (18c)$$

The poles of a third order system can be defined by (19), where ω_n and ζ_n are the natural angular frequency and damping ratio of the complex conjugate pole pair, respectively, and α_n is ratio between the natural frequencies of the pole pair and of the first-order pole.

$$K(s) = (s + \alpha_n \omega_n) (s^2 + 2\zeta_n \omega_n s + \omega_n^2) \quad (19)$$

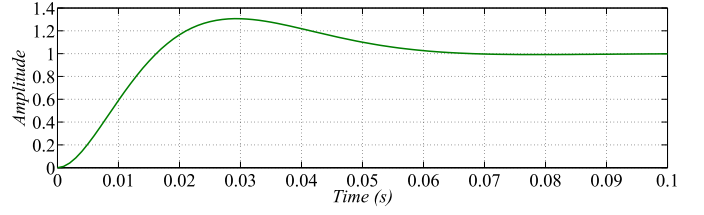


Fig. 11. DC link and DC cable model current response to a unitary input

TABLE III
DC LINK PARAMETERS

Symbol	CIGRÉ DC grid test system	HVDC demonstrator
C_f (mF)	0.555	5.98
C_{fpu} (%)	2.66	2.66
C_{f1} (mF)	0.124	1.34
C_{f1pu} (%)	11.9	11.9
R_f (Ω)	33.8	3.137
R_{fpu} (%)	15.7	15.7

By equating the denominator coefficients of (18) with (19), the DC link parameters (C_f , C_{f1} and R_f) can be found in terms of the desired transient response characteristics (α_n , ω_n , and ζ_n) and the imposed DC cable parameters (L_{DCc} and R_{DCc}), as given in (20).

$$C_f = \frac{k_1}{L_{DCc}^2 \alpha_n \omega_n^3} \quad (20a)$$

$$C_{f1} = \frac{\frac{1}{k_2 \omega_n}}{k_3} \quad (20b)$$

$$R_f = \frac{-k_3}{\frac{k_1 k_2}{L_{DCc} \omega_n}} \quad (20c)$$

$$k_1 = L_{DCc} \alpha_n \omega_n - R_{DCc} + 2L_{DCc} \zeta_n \omega_n \quad (20d)$$

$$k_2 = \alpha_n - \frac{R_{DCc}}{L_{DCc} \omega_n} + 2\zeta_n \quad (20e)$$

$$k_3 = R_{DCc} + 2R_{DCc} \alpha_n \zeta_n - 2L_{DCc} \zeta_n \omega_n - 4L_{DCc} \alpha_n \zeta_n^2 \omega_n - 2L_{DCc} \alpha_n^2 \zeta_n \omega_n + \frac{k_1}{L_{DCc} \omega_n} \left(-\frac{R_{DCc}^2}{L_{DCc} \omega_n} + R_{DCc} \alpha_n + 2R_{DCc} \zeta_n \right) \quad (20f)$$

The filter is designed so that the complex conjugate pole pair has a natural angular frequency of $2\pi 16$ rad/s and is ideally damped ($\zeta_n = 1/\sqrt{2}$), and the natural frequency of the first-order pole is the same as pole pair ($\alpha_n = 1$). The transient response to a unitary input is plotted in Fig. 11. By using (20), the values of C_f , C_{f1} and R_f for the CIGRÉ DC grid test system are tabulated in the middle column of Table III, where the per unit values are with respect to the DC base impedance.

By using the DC converter current expression developed in Appendix B, continuous expressions for the currents flowing through C_f , C_{f1} and R_f can be found, as shown in Appendix B, and are plotted in Figs. 12a), b) and c), respectively, where $i_{Cf1} = i_{DCl} - i_{Rf}$.

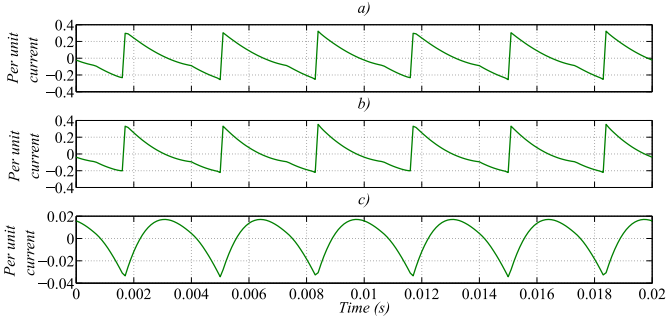


Fig. 12. Normalised a) DC link (C_f) current, b) C_{f1} current, and c) R_f current from the respective Fourier series expressions

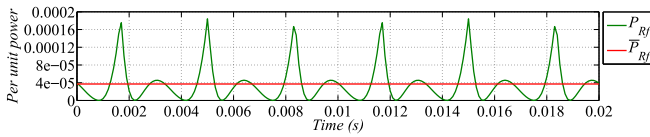


Fig. 13. Normalised instantaneous and mean R_f power

The steady-state instantaneous power dissipation in R_f can be found from the continuous expression for the R_f current and is plotted in Fig. 13. The mean of the instantaneous power dissipation is shown to equal approximately 0.004%, which is equivalent to 29.7 kW for the CIGRÉ DC grid test system. Note that, only the losses of the additional damping resistance have been considered here. Practically, the overall filter losses will be greater.

VI. HVDC DEMONSTRATOR

In line with the approach taken in [32], a relatively small scale industrial HVDC demonstrator has been used as the basis of the exemplar for the simulation studies. Implementing a full switching simulation model of the selected part of the CIGRÉ DC grid test system would not have been feasible, mainly due to the number of semiconductor devices required. However, the HVDC demonstrator provides an exemplar which allows a switching model of a manageable number of semiconductor devices to be simulated.

The ratings of the power, AC grid voltage and DC grid voltage have been chosen so that they are similar to the HVDC demonstrator presented in [32]. As with the CIGRÉ DC grid test system, the per unit transformer inductance is 18%, the ratio between the rated real and reactive powers is 40%, and the nominal sub-module capacitor voltage is 1.5 kV. Combining these ratings and values, along with using (1) – (6), allows the HVDC demonstrator ratings to be found, which are tabulated in the right-hand column of Table I.

In order to represent the CIGRÉ DC grid test system submarine cable model at the HVDC demonstrator ratings, the per unit characteristics of the submarine cable are kept constant. By using (7) – (9), and defining the test system as system one and the demonstrator as system two, equations for the absolute values of cable resistance, inductance and

TABLE IV
HVDC DEMONSTRATOR PARAMETERS

Parameter	Value
XFMR turns ratio (N)	$\sqrt{3} \times 1.4$
XFMR equivalent winding resistance (R_{TF})	100 m Ω
Number of sub-modules per arm (N_{sm})	10
Arm inductance (L)	0.25 mH
Sub-module capacitance time constant (τ)	14.5 ms
Sub-module capacitance (C_{sm})	4.31 mF
Per unit sub-module capacitance ($C_{sm_{pu}}$)	3.69%

capacitance at HVDC demonstrator ratings can be found, as shown in (21), (22) and (23), respectively.

$$R_{DCc2} = R_{DCc1} \frac{Z_{BASEdc2}}{Z_{BASEdc1}} \quad (21)$$

$$L_{DCc2} = L_{DCc1} \frac{Z_{BASEdc2}}{Z_{BASEdc1}} \quad (22)$$

$$C_{DCc2} = C_{DCc1} \frac{Z_{BASEdc1}}{Z_{BASEdc2}} \quad (23)$$

By using the information in Tables I and II, along with (21) – (23), the characteristics of an equivalent 200 km submarine cable for the demonstrator ± 10 kV HVDC link can be found, as tabulated in the right-hand column of Table II. The ratings of the DC link components can then be found by using the procedure described in Subsection V-B and are tabulated in the right-hand column of Table III. In reality, cables with a smaller power rating do not have the same per unit parameters as larger rated cables. However, since the objective of the scaled down system simulation is to represent the exact performance of a much larger rated system, just scaled down, then it is appropriate to use a per unit representation.

Further HVDC demonstrator parameters are listed in Table IV, where the sub-module capacitance selection procedure is described in Subsection IV-B. Even though the number of sub-modules per arm, the per unit sub-module capacitor voltage, and the per unit sub-module capacitance are different between the CIGRÉ DC test system and the HVDC demonstrator, consistency is maintained by having an equal sub-module capacitance time constant.

VII. HVDC DEMONSTRATOR SIMULATION RESULTS

A simulation model of the AAC has been implemented, by using the PLECS blockset within MATLAB Simulink, in order to validate the presented converter operating principles and theoretical analyses. The model is rated based on the HVDC demonstrator exemplar, due to the reasons stated in Section VI.

The reference power profile of Table V is used in order to demonstrate converter operation at the four corners of the real and reactive power operation envelope, and when transitioning between these power operation points. Fig. 14 illustrates that the measured powers are suitably regulated to their respective references at each of the four power operation points, and during transients, by designing a Decoupled Double Synchronous Reference Frame – Current Controller (DDSRF-CC)

TABLE V
SIMULATION MODEL REFERENCE POWER PROFILE

Time (s)	P^{ref} (MW)	Q^{ref} (MVar)
0 – 0.5	+20	-8
0.5 – 0.6	+20	-8 \Rightarrow +8
0.6 – 1.1	+20	+8
1.1 – 1.3	+20 \Rightarrow -20	+8
1.3 – 1.8	-20	+8
1.8 – 1.9	-20	+8 \Rightarrow -8
1.9 – 2.4	-20	-8

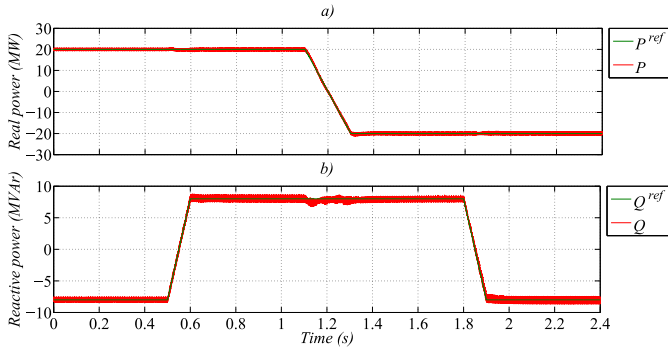


Fig. 14. Simulation results of the reference and measured a) real and b) reactive powers

[33], based on an AC side equivalent circuit model [34], [35].

Fig. 15 shows the steady-state AC supply voltages, synthesised secondary-side converter voltages, and AC supply currents, over one fundamental period, when the reference real and reactive powers are set to +20 MW and +8 MVar, respectively.

The steady-state phase-leg ‘a’ positive and negative arm currents and series connections of sub-module voltages are shown in Fig. 16. By inspecting Fig. 16a), the arm currents can be seen to follow the description given in Section II. When an arm director switch is closed, the secondary-side converter voltage is synthesised by the series connection of sub-modules in this arm, as shown in Fig. 16b).

The circulating current is controlled by using the hysteresis

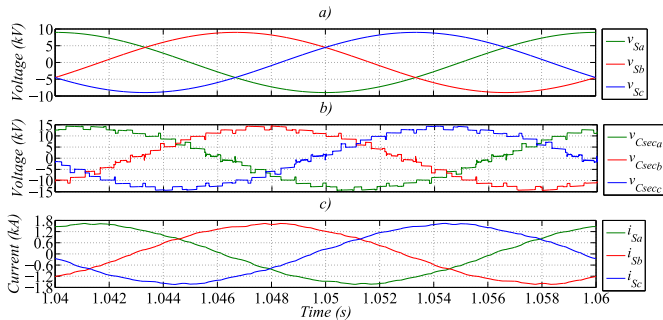


Fig. 15. Simulation results of the steady-state a) supply voltages, b) synthesised secondary-side converter voltages, and c) supply currents when $P^{ref} = +20$ MW and $Q^{ref} = +8$ MVar

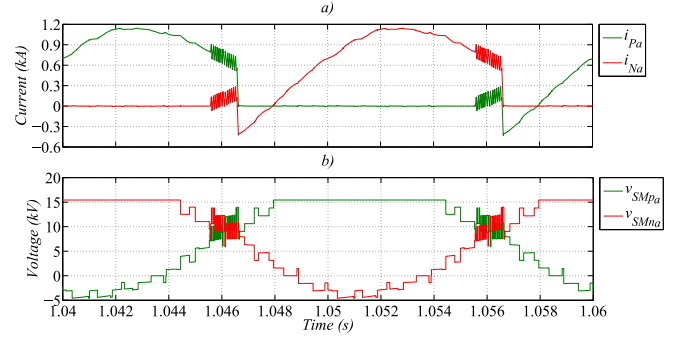


Fig. 16. Simulation results of the steady-state phase-leg ‘a’ positive and negative arm a) currents and b) series connections of sub-module voltages when $P^{ref} = +20$ MW and $Q^{ref} = +8$ MVar

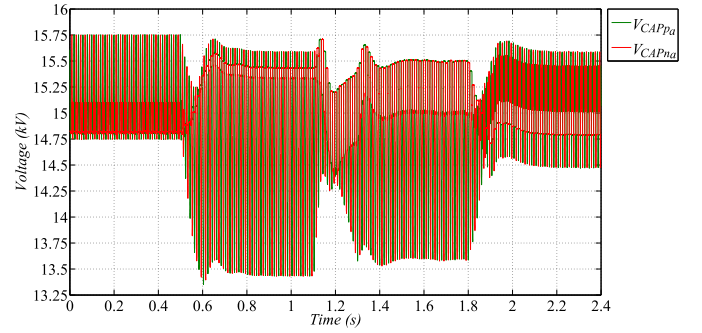


Fig. 17. Simulation results of the phase-leg ‘a’ positive and negative arm summed sub-module capacitor voltages

controller discussed in [23]. During “overlap”, at least one sub-module in each arm is not synthesising the secondary-side converter voltage. These sub-modules can therefore be used by the hysteresis controller. Practically, the indices of these sub-modules are written to FPGA registers, by a DSP, at the sub-module rotation frequency. During “overlap”, the upper and lower thresholds for the circulating current controller are written to FPGA registers, at the DSP sampling frequency. The FPGA calculates the circulating current, directly from the A2D converter registers corresponding to the positive and negative arm currents, which are triggered at a frequency limited by the A2D conversion duration. The FPGA executes a state machine which has the circulating current as an input, along with the sub-module indices and the controller thresholds. The outputs are the sub-module states required to keep the circulating current within its thresholds.

Fig. 17 shows the sum of the positive arm and the sum of negative arm sub-module capacitor voltages for phase-leg ‘a’, over the reference power profile. The maximum steady-state peak-peak voltage ripple of the summed sub-module capacitor voltages in each arm is seen to occur when operating at the rated positive real and reactive power. During this case, maximum and minimum voltages are approximately 15.54 kV and 13.43 kV, respectively, giving a peak-peak voltage ripple of approximately 14%; this ripple is similar to 13.7% specified in Subsection IV-B.

Fig. 18 shows the DC converter current, DC grid current,

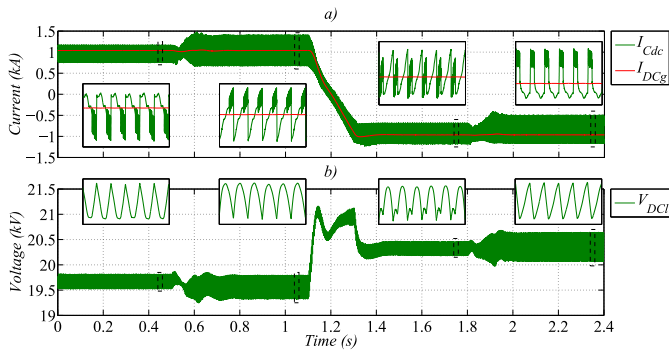


Fig. 18. Simulation results of the a) DC converter and DC grid currents, and b) DC link voltage

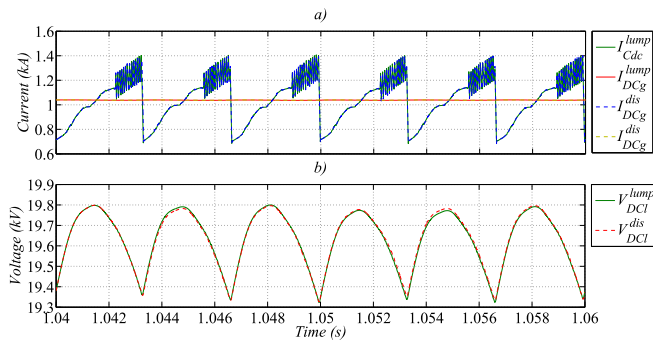


Fig. 19. Simulation results of the a) DC converter and DC grid currents, and b) DC link voltage for the lumped and distributed DC cable models

and DC link voltage, over the reference power profile. The inset graphs of Fig. 18 show the steady-state waveforms over a fundamental period for each of the four power operation points, as indicated in the main graphs by the dashed boxes. Over a fundamental period, the DC converter current has a repetition interval of 60° , and therefore this current has harmonics at multiples of six times the fundamental frequency. The DC link and DC cable model filters the DC converter current in order to form a smooth DC grid current. The DC link voltage contains a ripple of between 1.5-2.9%, depending on the power operation point, caused by the DC link current ($i_{DCi} = I_{DCg} - I_{Cdc}$).

In order to validate the simplified DC cable model described in Subsection V-B, the steady-state waveforms of the DC converter current, DC grid current, and DC link voltage, when using the lumped DC cable model with one $R_{DCc}L_{DCc}$ section and when using the distributed DC cable model with 200 $R'_{DCc}L'_{DCc}C'_{DCc}$ sections, are shown in Fig. 19.

In order to show the validity of the selected sub-module capacitance, found by using the procedure described in Subsection IV-B, during faulted AC grid conditions, a phase 'a' to ground fault is applied on the primary-side of the transformer for 500 ms. After the fault is detected, the pre-fault real power reference is halved from +20 MW to +10 MW over 2 ms, whilst the reactive power reference is maintained at +8 MVar throughout. After fault clearance is detected, the real power reference is doubled over 100 ms. The AAC AC fault ride-

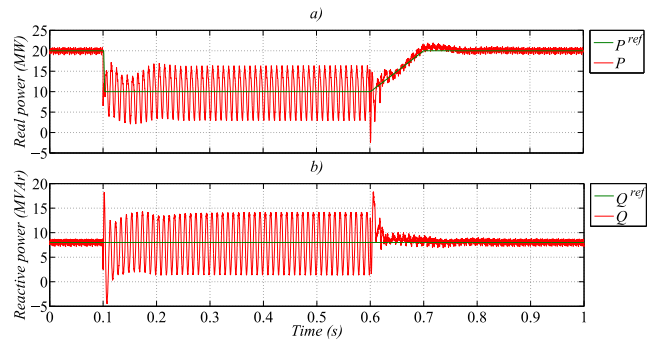


Fig. 20. Simulation results of the reference and measured a) real and b) reactive powers during a primary-side phase 'a' to ground fault

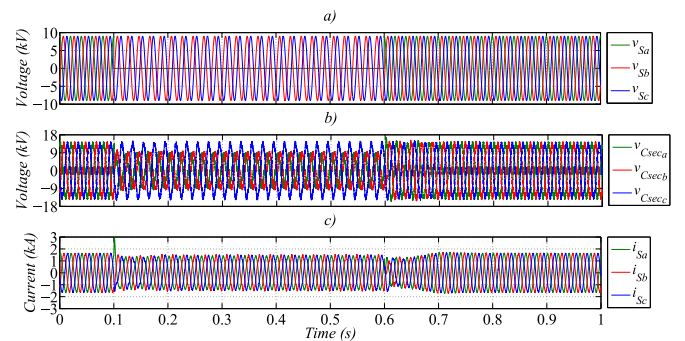


Fig. 21. Simulation results of the a) supply voltages, b) synthesised secondary-side converter voltages, and c) supply currents during a primary-side phase 'a' to ground fault

through strategy is described further in [24].

Fig. 20 shows the reference powers and their respective measured values. During the fault, the measured values have twice fundamental frequency ripples because symmetrical supply currents are demanded, in the presence of asymmetrical supply voltages, as shown in Fig. 21.

The phase-leg 'a' positive and negative arm sub-module capacitor voltages are shown in Fig. 22. Upon inspecting this figure, the maximum sub-module capacitor voltage is seen to be less than 2 kV. Say, for example, a dry resin filled, metallised polypropylene film capacitor based on [36] is used, this overvoltage is within the short-term ratings defined by IEC 61071 (capacitors for power electronics), given as a standard in [36]. The overvoltage is also below the proposed IGBT and anti-parallel diode modules rating of 3.3 kV, stated in Section III.

VIII. CONCLUSION

The AAC is a type of modular multilevel VSC which has been proposed for HVDC transmission applications. The AAC has a number of benefits over the MMC, such as improved attributes for handling DC side faults and requiring fewer sub-modules (typically $\approx 30\text{-}40\%$ fewer) with a smaller capacitance (typically $\approx 50\%$ smaller). This paper has described the converter topology and has provided an explanation of the converter operation, for the case when operating without zero sequence voltage injection in the "short-overlap" mode.

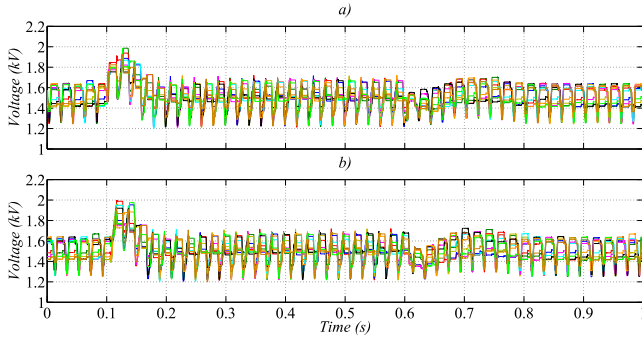


Fig. 22. Simulation results of the phase-leg ‘a’ a) positive and b) negative arm sub-module capacitor voltages during a primary-side phase ‘a’ to ground fault

In order to enable the selection of relevant parameters and test cases for this work, the exemplar HVDC system used has been based on a section of the CIGRÉ DC grid test system. A relatively small scale HVDC demonstrator has been used as the simulation exemplar because implementing a full switching simulation model of the selected part of the CIGRÉ DC grid test system would not have been feasible. However, the per unit values of the two exemplars are equal, where possible.

By deriving, for the first time, Fourier series expressions for the ideal arm current and reference voltage, an expression for the sub-module capacitance required to give a selected peak-peak voltage ripple of the summed sub-module capacitor voltages in an arm has been developed. The CIGRÉ DC grid test system and HVDC demonstrator both have maximum peak-peak voltage ripples of 13.7% and both have a sub-module capacitance time constant of 14.5 ms, when the sub-module capacitors equal 8 mF (0.18%) and 4.31 mF (3.69%), respectively. By deriving, for the first time, a Fourier series expression for the DC converter current, this current has been shown to contain non-negligible low order even harmonics. As the DC converter current needs to be filtered in order to form a smooth DC grid current, a novel DC filter arrangement has been proposed, where a passive low pass filter is formed by the characteristics of a simplified DC cable model, as well as the capacitance of the DC link and additional DC link damping resistance. The filter has been designed to have a natural frequency which is less than twice the fundamental frequency ($\omega_n = 2\pi 16$ rad/s) and to be ideally damped ($\zeta_n = 1/\sqrt{2}$). The transient response between the DC converter current and the DC grid current has been considered and typical waveforms have been presented. The additional damping resistance included in the DC link is shown to have steady-state losses of approximately 0.004%; although, practically, the overall filter losses will be greater.

APPENDIX A SUB-MODULE CAPACITOR SIZING

This appendix develops an analytical expression for the sub-module capacitance required to give a selected peak-peak voltage ripple of the summed sub-module capacitor voltages in an arm.

A. Positive Arm Current

The discontinuous expression of the positive arm current, defined by (12), can be represented by a continuous expression, termed the Fourier series, which can be defined by (24) for a periodic function [37].

$$w(t) = a_0 + \sum_{n=1}^{\infty} c(n) \cos(n\omega_0 t - \gamma(n)) \quad (24a)$$

$$a_0 = \frac{1}{T_0} \int_{t=0}^{T_0} w(t) dt \quad (24b)$$

$$a(n) = \frac{2}{T_0} \int_{t=0}^{T_0} w(t) \cos(n\omega_0 t) dt \quad (24c)$$

$$b(n) = \frac{2}{T_0} \int_{t=0}^{T_0} w(t) \sin(n\omega_0 t) dt \quad (24d)$$

$$c(n) = \sqrt{a(n)^2 + b(n)^2} \quad (24e)$$

$$\gamma(n) = \tan^{-1} \left(\frac{b(n)}{a(n)} \right) \quad (24f)$$

By using (24b), with $w(t) = i_{P_x}(t)$, the positive arm DC term can be expressed by (25). By using (24c), the positive arm current cosine term can be expressed by (26) and (27), when $n = 1$ and $n \neq 1$, respectively. By using (24d), the positive arm current sine term can be expressed by (28) and (29), when $n = 1$ and $n \neq 1$, respectively.

$$a_0 = \frac{1}{\omega_0 T_0} \left[\hat{I}_{C_x} \left(\cos(-\delta_x + \frac{\Phi_{OV_x}}{2} + \alpha_x) + \cos(-\delta_x - \frac{\Phi_{OV_x}}{2} + \alpha_x) \right) + 2\Phi_{OV_x} I_{DC} c_{ir_x} \right] \quad (25)$$

B. Positive Arm Reference Voltage

The discontinuous expression of the positive arm reference voltage is defined by (13). Assuming that the converter at the other end of the HVDC link is controlling its mean DC voltage to V_{DCg} (1 pu), the DC voltage of the converter being studied (V_{DCi}) depends on the link resistance and the real power being transmitted [see Fig. 18b)]. If the studied converter and its transformer are assumed to be lossless, the Point of Common Coupling (PCC) power, P , and the converter DC terminal power can be equated, as shown in (30). By solving (30) for I_{DCg} , (31) determines the current for a given amount of real power transmission, and then (32) evaluates the voltage.

$$P = I_{DCg} (V_{DCg} - I_{DCg} R_{DCc}) \quad (30)$$

$$I_{DCg} = \frac{V_{DCg} \pm \sqrt{(-V_{DCg})^2 - 4R_{DCc}P}}{2R_{DCc}} \quad (31)$$

$$V_{DCi} = V_{DCg} - 2I_{DCg} R_{DCc} \quad (32)$$

When defining the Fourier series for the positive arm reference voltage, $a = e$, $b = f$, $n = m$, $c = g$ and $\gamma = \varphi$ in (24). By using (24b), with $w(t) = v_{SMp_x}^{ref}(t)$, the positive arm reference voltage DC term can be expressed by (33). By using (24c), the positive arm reference voltage cosine term can be expressed by (34) and (35), when $m = 1$ and $m \neq 1$, respectively. By using (24d), the positive arm reference voltage

sine term can be expressed by (36) and (37), when $m = 1$ and $m \neq 1$, respectively.

$$e_0 = \frac{1}{\omega_0 T_0} \left[\frac{V_{DCI}}{2} (\pi + \Phi_{OVx}) - 2\hat{V}_{Csecx} \cos(\Phi_{OVx}/2) \right] \quad (33)$$

C. Positive Arm Inserted Sub-Module Capacitor Instantaneous Energy

When using (24), the positive arm inserted sub-module capacitor instantaneous energy is defined by (38). Expanding and then integrating (38), yields (39).

$$E_{P_x}(t) = \int \left[\underbrace{\left(a_0 + \sum_{n=1}^{\infty} c(n) \cos(n\omega_0 t - \gamma(n)) \right)}_{i_{P_x}(t)} \times \underbrace{\left(e_0 + \sum_{m=1}^{\infty} g(m) \cos(m\omega_0 t - \varphi(m)) \right)}_{v_{SM_{P_x}}^{ref}(t)} \right] dt \quad (38)$$

The turning points of the instantaneous energy can be found by solving (40), where $P_{P_x}(t)$ is the instantaneous power of

the inserted sub-module capacitors. However, when (38) has a sensible number of harmonics, solving (40) is impossible. Therefore, the instantaneous power zero crossings are instead found from the zero crossings of the discontinuous expressions which describe the positive arm current and reference voltage, given by equations (12) and (13), respectively. It should be noted that zero crossings of the arm current can also occur when transitioning to or from the “positive arm active” state.

$$\frac{d}{dt} E_{P_x}(t) = P_{P_x}(t) = 0 \quad (40)$$

D. Relationship between the Sub-Module Capacitance and the Summed Sub-Module Capacitor Instantaneous Energy in an Arm

Once all of the energy turning points (power zero crossings) are known, they can be substituted into (39) in turn, in order to find the maximum and minimum changes in the summed sub-module capacitor energy (E_x^{max} and E_x^{min}). The peak-peak energy ripple is given by (41), which needs to be solved for the sub-module capacitance, C_{sm} , based on a given peak-peak voltage ripple for the summed sub-module capacitor voltages

$$a(n=1) = \frac{1}{\omega_0 T_0} \left[\frac{\hat{I}_{C_x}}{4} \left(\begin{array}{c} -\cos(\alpha_x) \left(\begin{array}{c} \cos(-2\delta_x + \Phi_{OVx}) - \\ \cos(-2\delta_x - \Phi_{OVx}) \end{array} \right) + \\ \sin(\alpha_x) \left(\begin{array}{c} 2\Phi_{OVx} + \sin(-2\delta_x + \Phi_{OVx}) - \\ \sin(-2\delta_x - \Phi_{OVx}) \end{array} \right) \end{array} \right) + \right. \\ \left. 2I_{DCcir_x} \left(\sin(-\delta_x + \frac{\Phi_{OVx}}{2}) - \sin(-\delta_x - \frac{\Phi_{OVx}}{2}) \right) \right] + \quad (26)$$

$$\frac{\hat{I}_{C_x}}{2\omega_0 T_0} \left[\begin{array}{c} -\cos(\alpha_x) \left(\begin{array}{c} \cos(-2\delta_x - \Phi_{OVx}) - \\ \cos(-2\delta_x + \Phi_{OVx}) \end{array} \right) + \\ \sin(\alpha_x) \left(\begin{array}{c} 2(\pi - \Phi_{OVx}) + \sin(-2\delta_x - \Phi_{OVx}) - \\ \sin(-2\delta_x + \Phi_{OVx}) \end{array} \right) \end{array} \right] +$$

$$\frac{1}{\omega_0 T_0} \left[\frac{\hat{I}_{C_x}}{4} \left(\begin{array}{c} -\cos(\alpha_x) \left(\begin{array}{c} \cos(-2\delta_x + \Phi_{OVx}) - \\ \cos(-2\delta_x - \Phi_{OVx}) \end{array} \right) + \\ \sin(\alpha_x) \left(\begin{array}{c} 2\Phi_{OVx} + \sin(-2\delta_x + \Phi_{OVx}) - \\ \sin(-2\delta_x - \Phi_{OVx}) \end{array} \right) \end{array} \right) + \right. \\ \left. 2I_{DCcir_x} \left(\sin(\pi - \delta_x + \frac{\Phi_{OVx}}{2}) - \sin(\pi - \delta_x - \frac{\Phi_{OVx}}{2}) \right) \right] +$$

$$a(n \neq 1) = \frac{2}{\omega_0 T_0} \left[\frac{\hat{I}_{C_x}}{4} \left(\begin{array}{c} \frac{1}{(n+1)} \left(\begin{array}{c} -\cos(\alpha_x + (1+n)(-\delta_x + \frac{\Phi_{OVx}}{2})) + \\ \cos(\alpha_x + (1+n)(-\delta_x - \frac{\Phi_{OVx}}{2})) \end{array} \right) + \\ \frac{1}{(n-1)} \left(\begin{array}{c} \cos(\alpha_x + (1-n)(-\delta_x + \frac{\Phi_{OVx}}{2})) - \\ \cos(\alpha_x + (1-n)(-\delta_x - \frac{\Phi_{OVx}}{2})) \end{array} \right) \end{array} \right) + \right. \\ \left. \frac{I_{DCcir_x}}{n} \left(\sin(n(-\delta_x + \frac{\Phi_{OVx}}{2})) - \sin(n(-\delta_x - \frac{\Phi_{OVx}}{2})) \right) \right] + \quad (27)$$

$$\frac{\hat{I}_{C_x}}{\omega_0 T_0} \left[\begin{array}{c} \frac{1}{(n+1)} \left(\begin{array}{c} -\cos(\alpha_x + (1+n)(\pi - \delta_x - \frac{\Phi_{OVx}}{2})) + \\ \cos(\alpha_x + (1+n)(-\delta_x + \frac{\Phi_{OVx}}{2})) \end{array} \right) + \\ \frac{1}{(n-1)} \left(\begin{array}{c} \cos(\alpha_x + (1-n)(\pi - \delta_x - \frac{\Phi_{OVx}}{2})) - \\ \cos(\alpha_x + (1-n)(-\delta_x + \frac{\Phi_{OVx}}{2})) \end{array} \right) \end{array} \right] +$$

$$\frac{2}{\omega_0 T_0} \left[\frac{\hat{I}_{C_x}}{4} \left(\begin{array}{c} \frac{1}{(n+1)} \left(\begin{array}{c} -\cos(\alpha_x + (1+n)(\pi - \delta_x + \frac{\Phi_{OVx}}{2})) + \\ \cos(\alpha_x + (1+n)(\pi - \delta_x - \frac{\Phi_{OVx}}{2})) \end{array} \right) + \\ \frac{1}{(n-1)} \left(\begin{array}{c} \cos(\alpha_x + (1-n)(\pi - \delta_x + \frac{\Phi_{OVx}}{2})) - \\ \cos(\alpha_x + (1-n)(\pi - \delta_x - \frac{\Phi_{OVx}}{2})) \end{array} \right) \end{array} \right) + \right. \\ \left. \frac{I_{DCcir_x}}{n} \left(\sin(n(\pi - \delta_x + \frac{\Phi_{OVx}}{2})) - \sin(n(\pi - \delta_x - \frac{\Phi_{OVx}}{2})) \right) \right] +$$

in an arm.

$$\begin{aligned}
E_x^{pk-pk} &= E_x^{max} - E_x^{min} \\
&= \frac{1}{2} N_{sm} C_{sm} \left[\frac{(V_{CAPnom} + V_{CAPx}^{max})^2 - (V_{CAPnom} + V_{CAPx}^{min})^2}{2} \right] \\
&= \frac{1}{2} N_{sm} C_{sm} \left[\frac{2V_{CAPnom} (V_{CAPx}^{max} - V_{CAPx}^{min}) + (V_{CAPx}^{max})^2 - (V_{CAPx}^{min})^2}{2} \right] \quad (41)
\end{aligned}$$

In (41), the maximum and minimum changes in the summed sub-module capacitor voltage in an arm (V_{CAPx}^{max} and V_{CAPx}^{min}) are unknowns, and therefore need to be eliminated. By defining the peak-peak voltage ripple as in (42), where κ is the desired per unit nominal sub-module capacitor voltage ripple, $V_{CAPx}^{max} - V_{CAPx}^{min}$ and V_{CAPx}^{min} can be expressed as shown in (42) and (43), respectively.

$$V_{CAPx}^{max} - V_{CAPx}^{min} = \kappa V_{CAPnom} \quad (42)$$

$$V_{CAPx}^{min} = V_{CAPx}^{max} - \kappa V_{CAPnom} \quad (43)$$

The maximum and nominal energies can be defined by (44) and (45), respectively. By substituting (45) into (44), in order to eliminate E_{nom} , an expression for V_{CAPx}^{max} in terms of known quantities can be found; the result is shown in (46). An expression for V_{CAPx}^{min} can be found by substituting

(46) into (43), in order to eliminate V_{CAPx}^{max} , yielding (47). Finally, substituting (46) and (47) into (41) yields (14), when a quadratic equation in terms of C_{sm} is formed.

$$E_{nom} + E_x^{max} = \frac{1}{2} N_{sm} C_{sm} (V_{CAPnom} + V_{CAPx}^{max})^2 \quad (44)$$

$$E_{nom} = \frac{1}{2} N_{sm} C_{sm} V_{CAPnom}^2 \quad (45)$$

$$V_{CAPx}^{max} = \left(V_{CAPnom}^2 + \frac{2E_x^{max}}{N_{sm} C_{sm}} \right)^{\frac{1}{2}} - V_{CAPnom} \quad (46)$$

$$V_{CAPx}^{min} = \left(V_{CAPnom}^2 + \frac{2E_x^{max}}{N_{sm} C_{sm}} \right)^{\frac{1}{2}} - V_{CAPnom} - \kappa V_{CAPnom} \quad (47)$$

APPENDIX B

DC SIDE CURRENT FOURIER SERIES EXPRESSIONS

This appendix defines the Fourier series expressions for the DC converter current, DC link (C_f) current, and R_f current. Additionally, as $i_{Cf1} = i_{DCI} - i_{Rf}$, the Fourier series expression for the C_{f1} current is found indirectly.

$$\begin{aligned}
b(n=1) &= \frac{1}{\omega_0 T_0} \left[\frac{\hat{I}_{Cx}}{4} \left(\cos(\alpha_x) \left(\frac{2\Phi_{ov} - \sin(-2\delta_x + \Phi_{ov}) + \sin(-2\delta_x - \Phi_{ov})}{\cos(-2\delta_x + \Phi_{ov})} \right) + \right) - \right. \\
&\quad \left. 2I_{DCcir_x} \left(\cos(-\delta_x + \frac{\Phi_{ov}}{2}) - \cos(-\delta_x - \frac{\Phi_{ov}}{2}) \right) \right] + \\
&\quad \frac{\hat{I}_{Cx}}{2\omega_0 T_0} \left[\cos(\alpha_x) \left(\frac{2(\pi - \Phi_{ov}) - \sin(-2\delta_x - \Phi_{ov}) + \sin(-2\delta_x + \Phi_{ov})}{\cos(-2\delta_x + \Phi_{ov})} \right) + \right. \\
&\quad \left. \sin(\alpha_x) \left(\frac{-\cos(-2\delta_x - \Phi_{ov}) + \cos(-2\delta_x + \Phi_{ov})}{\cos(-2\delta_x + \Phi_{ov})} \right) \right] + \quad (28)
\end{aligned}$$

$$\begin{aligned}
b(n \neq 1) &= -\frac{2}{\omega_0 T_0} \left[\frac{\hat{I}_{Cx}}{4} \left(\frac{1}{(n+1)} \left(\frac{\sin(\alpha_x + (1+n)(-\delta_x + \frac{\Phi_{OVx}}{2}) - \sin(\alpha_x + (1+n)(-\delta_x - \frac{\Phi_{OVx}}{2}))}{\sin(\alpha_x + (1-n)(-\delta_x + \frac{\Phi_{OVx}}{2})} \right) - \right) + \right. \\
&\quad \left. \frac{1}{(n-1)} \left(\frac{\sin(\alpha_x + (1-n)(-\delta_x + \frac{\Phi_{OVx}}{2}) - \sin(\alpha_x + (1-n)(-\delta_x - \frac{\Phi_{OVx}}{2}))}{\sin(\alpha_x + (1-n)(-\delta_x - \frac{\Phi_{OVx}}{2})} \right) - \right) \right] + \\
&\quad \frac{I_{DCcir_x}}{n} \left(\cos(n(-\delta_x + \frac{\Phi_{OVx}}{2})) - \cos(n(-\delta_x - \frac{\Phi_{OVx}}{2})) \right) \right] + \\
&\quad \frac{\hat{I}_{Cx}}{\omega_0 T_0} \left[\frac{1}{(n+1)} \left(\frac{-\sin(\alpha_x + (1+n)(\pi - \delta_x - \frac{\Phi_{OVx}}{2}) + \sin(\alpha_x + (1+n)(-\delta_x + \frac{\Phi_{OVx}}{2}))}{\sin(\alpha_x + (1+n)(-\delta_x + \frac{\Phi_{OVx}}{2})} \right) + \right. \\
&\quad \left. \frac{1}{(n-1)} \left(\frac{-\sin(\alpha_x + (1-n)(\pi - \delta_x - \frac{\Phi_{OVx}}{2}) + \sin(\alpha_x + (1-n)(-\delta_x + \frac{\Phi_{OVx}}{2}))}{\sin(\alpha_x + (1-n)(-\delta_x + \frac{\Phi_{OVx}}{2})} \right) + \right) \right] - \quad (29) \\
&\quad \frac{2}{\omega_0 T_0} \left[\frac{\hat{I}_{Cx}}{4} \left(\frac{1}{(n+1)} \left(\frac{\sin(\alpha_x + (1+n)(\pi - \delta_x + \frac{\Phi_{OVx}}{2}) - \sin(\alpha_x + (1+n)(\pi - \delta_x - \frac{\Phi_{OVx}}{2}))}{\sin(\alpha_x + (1+n)(\pi - \delta_x - \frac{\Phi_{OVx}}{2})} \right) + \right) + \right. \\
&\quad \left. \frac{1}{(n-1)} \left(\frac{\sin(\alpha_x + (1-n)(\pi - \delta_x + \frac{\Phi_{OVx}}{2}) - \sin(\alpha_x + (1-n)(\pi - \delta_x - \frac{\Phi_{OVx}}{2}))}{\sin(\alpha_x + (1-n)(\pi - \delta_x - \frac{\Phi_{OVx}}{2})} \right) - \right) \right] + \\
&\quad \frac{I_{DCcir_x}}{n} \left(\cos(n(\pi - \delta_x + \frac{\Phi_{OVx}}{2})) - \cos(n(\pi - \delta_x - \frac{\Phi_{OVx}}{2})) \right) \right]
\end{aligned}$$

A. DC Converter Current

Two of the twelve DC converter current intervals, per fundamental period, are defined by (17). By using (24b), with $w(t) = i_{Cdc}(t)$, the DC converter current DC term, for the first and second defined intervals, can be expressed by (48) and (49), respectively. The remaining intervals follow similar mathematical patterns to those in (48) and (49). Over a fundamental period, the DC converter current DC term can be defined by (50).

$$a_{10} = -\frac{\hat{I}_{Cb}}{T_0\omega_0} \begin{bmatrix} \cos(-\delta_c - \Phi_{OVc}/2 + \alpha_b) + \\ \cos(-\delta_a + \Phi_{OVa}/2 + \alpha_b) \end{bmatrix} \quad (48)$$

$$a_{20} = \frac{1}{\omega_0 T_0} \begin{bmatrix} -2\hat{I}_{Ca} \sin(-\delta_c + \alpha_a) \sin(\Phi_{OVc}/2) - \\ \hat{I}_{Cc} \sin(-\delta_c + \alpha_c) \sin(\Phi_{OVc}/2) + \\ I_{cirDCc} \Phi_{OVc} \end{bmatrix} \quad (49)$$

$$a_0 = \sum_{int=1}^{12} a_{int_0} \quad (50)$$

By using (24c), the DC converter current cosine term, for the

first and second defined intervals, can be expressed by (51) and (52), respectively. By using (24d), the DC converter current sine term, for the first and second defined intervals, can be expressed by (53) and (54), respectively. Over a fundamental period, the DC converter current cosine and sine terms can be defined by (55) and (56), respectively.

$$a(n) = \sum_{int=1}^{12} a_{int}(n) \quad (55)$$

$$b(n) = \sum_{int=1}^{12} b_{int}(n) \quad (56)$$

B. DC Link (C_f) Current

Ratio $\mathbf{G}_1(n)$ is defined by (57). Substituting (58) and (59) into (57), yields (60).

$$\mathbf{G}_1(n) = \frac{\mathbf{Z}_{DCc}(n)}{\mathbf{Z}_{DCc}(n) + \mathbf{Z}_{DCl}(n)} \quad (57)$$

$$\mathbf{Z}_{DCc}(n) = R_{DCc} + jn\omega_0 L_{DCc} \quad (58)$$

$$e(m=1) = \frac{1}{\omega_0 T_0} \left[\begin{array}{l} V_{DCl} \left(\sin\left(\pi - \delta_x + \frac{\Phi_{OVx}}{2}\right) - \sin\left(-\delta_x - \frac{\Phi_{OVx}}{2}\right) \right) - \\ \hat{V}_{Csecx} \left(\frac{\cos(\delta_x)}{2} \left(\begin{array}{l} -\cos(-2\delta_x + \Phi_{OVx}) + \\ \cos(-2\delta_x - \Phi_{OVx}) \end{array} \right) + \right. \\ \left. \frac{\sin(\delta_x)}{2} \left(\begin{array}{l} 2(\pi + \Phi_{OVx}) + \sin(-2\delta_x + \Phi_{OVx}) - \\ \sin(-2\delta_x - \Phi_{OVx}) \end{array} \right) \right) \end{array} \right] \quad (34)$$

$$e(m \neq 1) = \frac{1}{\omega_0 T_0} \left[\begin{array}{l} \frac{V_{DCl}}{m} \left(\begin{array}{l} \sin\left(m\left(\pi - \delta_x + \frac{\Phi_{OVx}}{2}\right)\right) - \\ \sin\left(m\left(-\delta_x - \frac{\Phi_{OVx}}{2}\right)\right) \end{array} \right) + \\ \hat{V}_{Csecx} \left(\frac{1}{(m+1)} \left(\begin{array}{l} \cos\left(\delta_x + (1+m)\left(\pi - \delta_x + \frac{\Phi_{OVx}}{2}\right)\right) - \\ \cos\left(\delta_x + (1+m)\left(-\delta_x - \frac{\Phi_{OVx}}{2}\right)\right) \end{array} \right) + \right. \\ \left. \frac{1}{(m-1)} \left(\begin{array}{l} \cos\left(\delta_x + (1-m)\left(-\delta_x - \frac{\Phi_{OVx}}{2}\right)\right) - \\ \cos\left(\delta_x + (1-m)\left(\pi - \delta_x + \frac{\Phi_{OVx}}{2}\right)\right) \end{array} \right) \right) \end{array} \right] \quad (35)$$

$$f(m=1) = \frac{1}{\omega_0 T_0} \left[\begin{array}{l} -V_{DCl} \left(\cos\left(\pi - \delta_x + \frac{\Phi_{OVx}}{2}\right) - \cos\left(-\delta_x - \frac{\Phi_{OVx}}{2}\right) \right) - \\ \hat{V}_{Csecx} \left(\frac{\cos(\delta_x)}{2} \left(\begin{array}{l} 2(\pi + \Phi_{OVx}) - \sin(-2\delta_x + \Phi_{OVx}) + \\ \sin(-2\delta_x - \Phi_{OVx}) \end{array} \right) + \right. \\ \left. \frac{\sin(\delta_x)}{2} \left(\begin{array}{l} -\cos(-2\delta_x + \Phi_{OVx}) + \\ \cos(-2\delta_x - \Phi_{OVx}) \end{array} \right) \right) \end{array} \right] \quad (36)$$

$$f(m \neq 1) = \frac{1}{\omega_0 T_0} \left[\begin{array}{l} \frac{V_{DCl}}{m} \left(\begin{array}{l} \cos\left(m\left(-\delta_x - \frac{\Phi_{OVx}}{2}\right)\right) - \\ \cos\left(m\left(\pi - \delta_x + \frac{\Phi_{OVx}}{2}\right)\right) \end{array} \right) + \\ \hat{V}_{Csecx} \left(\frac{1}{(m+1)} \left(\begin{array}{l} \sin\left(\delta_x + (1+m)\left(\pi - \delta_x + \frac{\Phi_{OVx}}{2}\right)\right) - \\ \sin\left(\delta_x + (1+m)\left(-\delta_x - \frac{\Phi_{OVx}}{2}\right)\right) \end{array} \right) + \right. \\ \left. \frac{1}{(m-1)} \left(\begin{array}{l} \sin\left(\delta_x + (1-m)\left(\pi - \delta_x + \frac{\Phi_{OVx}}{2}\right)\right) - \\ \sin\left(\delta_x + (1-m)\left(-\delta_x - \frac{\Phi_{OVx}}{2}\right)\right) \end{array} \right) \right) \end{array} \right] \quad (37)$$

$$E_{Px}(t) = a_0 e_0 t + a_0 \sum_{m=1}^{\infty} \frac{g(m)}{m\omega_0} \sin(m\omega_0 t - \varphi(m)) + e_0 \sum_{n=1}^{\infty} \frac{c(n)}{n\omega_0} \sin(n\omega_0 t - \gamma(n)) + \sum_{n=1}^{\infty} \sum_{m=1}^{\infty} \left\{ \begin{array}{l} \frac{c(n)g(m)}{2} \left(\begin{array}{l} \cos(-\gamma(n) + \varphi(m)) t + \\ \frac{1}{(n+m)\omega_0} \sin((n+m)\omega_0 t - \gamma(n) - \varphi(m)) \end{array} \right) \text{ if } n = m \\ \frac{c(n)g(m)}{2} \left(\begin{array}{l} \frac{1}{(n-m)\omega_0} \sin((n-m)\omega_0 t - \gamma(n) + \varphi(m)) + \\ \frac{1}{(n+m)\omega_0} \sin((n+m)\omega_0 t - \gamma(n) - \varphi(m)) \end{array} \right) \text{ if } n \neq m \end{array} \right. \quad (39)$$

$$\mathbf{Z}_{DCI}(n) = \frac{(C_f R_f + C_{f1} R_f) j n \omega_0 + 1}{C_f C_{f1} R_f (j n \omega_0)^2 + C_f j n \omega_0} \quad (59)$$

$$\angle i_{DCI}(n \neq 0) = \theta(n) + \pi + \angle \mathbf{G}_1(n \neq 0) \quad (63)$$

$$\mathbf{G}_1(n) = \frac{k_4 (j n \omega_0)^3 + k_5 (j n \omega_0)^2 + k_6 j n \omega_0}{k_1 (j n \omega_0)^3 + k_2 (j n \omega_0)^2 + k_3 j n \omega_0 + 1} \quad (60a)$$

$$k_1 = C_f C_{f1} L_{DCc} R_f \quad (60b)$$

$$k_2 = C_f L_{DCc} + C_f C_{f1} R_f R_{DCc} \quad (60c)$$

$$k_3 = C_f R_f + C_{f1} R_f + C_f R_{DCc} \quad (60d)$$

$$k_4 = C_f C_{f1} L_{DCc} R_f \quad (60e)$$

$$k_5 = C_f L_{DCc} + C_f C_{f1} R_f R_{DCc} \quad (60f)$$

$$k_6 = C_f R_{DCc} \quad (60g)$$

The DC link current DC term is found by using (61). Similarly, the DC link current n^{th} harmonic amplitude can be found by using (62). The DC link current n^{th} harmonic phase angle can be found by using (63). As the DC converter and DC link currents are defined positive in opposite directions, π is also added in (63).

$$|i_{DCI}(n = 0)| = a_0 |\mathbf{G}_1(n = 0)| \quad (61)$$

$$|i_{DCI}(n \neq 0)| = c(n) |\mathbf{G}_1(n \neq 0)| \quad (62)$$

C. R_f Current

Ratio $\mathbf{G}_2(n)$ is defined by (64). Equation (66) can be found by substituting (65) into (64).

$$\mathbf{G}_2(n) = \frac{\mathbf{Z}_{Cf1}(n)}{\mathbf{Z}_{Cf1}(n) + R_f} \quad (64)$$

$$\mathbf{Z}_{Cf1}(n) = \frac{1}{j n \omega_0 C_{f1}} \quad (65)$$

$$\mathbf{G}_2(n) = \frac{1}{C_{f1} R_f j n \omega_0 + 1} \quad (66)$$

The R_f current, i_{Rf} , has its DC term, and its n^{th} harmonic amplitudes and phase angles defined by (67), (68) and (69), respectively.

$$|i_{Rf}(n = 0)| = |i_{DCI}(n = 0)| |\mathbf{G}_2(n = 0)| \quad (67)$$

$$|i_{Rf}(n \neq 0)| = |i_{DCI}(n \neq 0)| |\mathbf{G}_2(n \neq 0)| \quad (68)$$

$$\angle i_{Rf}(n \neq 0) = \angle i_{DCI}(n \neq 0) + \angle \mathbf{G}_2(n \neq 0) \quad (69)$$

$$a_1(n) = -\frac{\hat{I}_{Cb}}{\omega_0 T_0} \left[\begin{array}{c} -\frac{1}{(n+1)} \left(\begin{array}{c} \cos(\alpha_b + (1+n)(\pi - \delta_c - \frac{\Phi_{OVc}}{2})) \\ \cos(\alpha_b + (1+n)(-\delta_a + \frac{\Phi_{OVa}}{2})) \end{array} \right) - \\ \frac{1}{(n-1)} \left(\begin{array}{c} \cos(\alpha_b + (1-n)(\pi - \delta_c - \frac{\Phi_{OVc}}{2})) \\ \cos(\alpha_b + (1-n)(-\delta_a + \frac{\Phi_{OVa}}{2})) \end{array} \right) - \end{array} \right] + \quad (51)$$

$$a_2(n) = \frac{\hat{I}_{Ca}}{\omega_0 T_0} \left[\begin{array}{c} -\frac{1}{(n+1)} \left(\begin{array}{c} \cos(\alpha_a + (1+n)(\pi - \delta_c + \frac{\Phi_{OVc}}{2})) \\ \cos(\alpha_a + (1+n)(\pi - \delta_c - \frac{\Phi_{OVc}}{2})) \end{array} \right) - \\ \frac{1}{(n-1)} \left(\begin{array}{c} \cos(\alpha_a + (1-n)(\pi - \delta_c + \frac{\Phi_{OVc}}{2})) \\ \cos(\alpha_a + (1-n)(\pi - \delta_c - \frac{\Phi_{OVc}}{2})) \end{array} \right) - \end{array} \right] + \quad (52)$$

$$\frac{\hat{I}_{Cc}}{2\omega_0 T_0} \left[\begin{array}{c} -\frac{1}{(n+1)} \left(\begin{array}{c} \cos(\alpha_c + (1+n)(\pi - \delta_c + \frac{\Phi_{OVc}}{2})) \\ \cos(\alpha_c + (1+n)(\pi - \delta_c - \frac{\Phi_{OVc}}{2})) \end{array} \right) - \\ \frac{1}{(n-1)} \left(\begin{array}{c} \cos(\alpha_c + (1-n)(\pi - \delta_c + \frac{\Phi_{OVc}}{2})) \\ \cos(\alpha_c + (1-n)(\pi - \delta_c - \frac{\Phi_{OVc}}{2})) \end{array} \right) - \end{array} \right] +$$

$$\frac{4I_{DCc}^{circ}}{n\omega_0 T_0} \cos(n(\pi - \delta_c)) \sin\left(n \frac{\Phi_{OVc}}{2}\right)$$

$$b_1(n) = \frac{\hat{I}_{Cb}}{\omega_0 T_0} \left[\begin{array}{c} \frac{1}{(n+1)} \left(\begin{array}{c} \sin(\alpha_b + (1+n)(\pi - \delta_c - \frac{\Phi_{OVc}}{2})) \\ \sin(\alpha_b + (1+n)(-\delta_a + \frac{\Phi_{OVa}}{2})) \end{array} \right) - \\ \frac{1}{(n-1)} \left(\begin{array}{c} \sin(\alpha_b + (1-n)(\pi - \delta_c - \frac{\Phi_{OVc}}{2})) \\ \sin(\alpha_b + (1-n)(-\delta_a + \frac{\Phi_{OVa}}{2})) \end{array} \right) - \end{array} \right] + \quad (53)$$

$$b_2(n) = -\frac{\hat{I}_{Ca}}{\omega_0 T_0} \left[\begin{array}{c} \frac{1}{(n+1)} \left(\begin{array}{c} \sin(\alpha_a + (1+n)(\pi - \delta_c + \frac{\Phi_{OVc}}{2})) \\ \sin(\alpha_a + (1+n)(\pi - \delta_c - \frac{\Phi_{OVc}}{2})) \end{array} \right) - \\ \frac{1}{(n-1)} \left(\begin{array}{c} \sin(\alpha_a + (1-n)(\pi - \delta_c + \frac{\Phi_{OVc}}{2})) \\ \sin(\alpha_a + (1-n)(\pi - \delta_c - \frac{\Phi_{OVc}}{2})) \end{array} \right) - \end{array} \right] + \quad (54)$$

$$-\frac{\hat{I}_{Cc}}{2\omega_0 T_0} \left[\begin{array}{c} \frac{1}{(n+1)} \left(\begin{array}{c} \sin(\alpha_c + (1+n)(\pi - \delta_c + \frac{\Phi_{OVc}}{2})) \\ \sin(\alpha_c + (1+n)(\pi - \delta_c - \frac{\Phi_{OVc}}{2})) \end{array} \right) - \\ \frac{1}{(n-1)} \left(\begin{array}{c} \sin(\alpha_c + (1-n)(\pi - \delta_c + \frac{\Phi_{OVc}}{2})) \\ \sin(\alpha_c + (1-n)(\pi - \delta_c - \frac{\Phi_{OVc}}{2})) \end{array} \right) - \end{array} \right] +$$

$$\frac{4I_{DCc}^{circ}}{n\omega_0 T_0} \sin(n(\pi - \delta_c)) \sin\left(n \frac{\Phi_{OVc}}{2}\right)$$

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