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DC-link Capacitor Second Carrier Band Switching Harmonic Current Reduction in Two-Level Back-to-Back Converters

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Abstract— This paper proposes an active switching harmonic current reduction method within the DC-link capacitor of two-level, three-phase, back-to-back converters. The method is based on the derived analytical solution for switching harmonic currents in the DC-link. It is shown that by controlling the PWM carrier waveform's phase angles, the harmonics in the 2nd carrier band of the rectifier and the inverter can be synchronized such that cancellation occurs in the DC-link capacitor. This synchronization is provided by harmonic phase feedback control. The feasibility of the proposed approach has been verified experimentally and results are presented in the paper.

Index Terms— converters, AC-DC power conversion, capacitors, harmonic analysis, switching functions, power quality, pulse-width modulation, testing.

I. INTRODUCTION

Due to advantages such as bidirectional power flow capability, unity power factor and high efficiency, two-level AC-DC-AC power converters, also known as “back-to-back” converters, are widely utilized in industry [1], wind power generation [2], more-electric transportation [3], microgrids [4] etc. The topology of this converter is shown in Fig. 1.

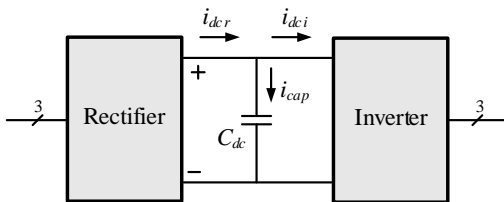


Fig. 1. Back-to-back converter topology

The inherent switching nature of power converters results in significant current pulses being injected into the DC-link from both rectifier and inverter sides. Consequently, losses in the capacitor are increased and a higher capacitor ripple current rating is required. This therefore increases the capacitor weight,

volume and cost, as well as lowering the power density and reliability for the overall converter. In many areas, like aerospace, electric vehicles and the military, these issues are of great importance. Therefore, the problem of DC-link capacitor current ripple minimization is the focus of many research studies.

The DC-link capacitor current ripple is caused by the instantaneous difference between the rectifier-side i_{dcr} and inverter-side i_{dci} currents, as shown in Fig. 1. Numerous methods, such as direct capacitor current control [5], active damping [6], feedback linearization control [7] and average voltage constraint control [8] have been reported to address this problem. However, as the achievable current control bandwidth is limited by the Pulse Width Modulation carrier frequency [16], these control based methods are only able to reduce low-frequency ripple effects caused by power flow imbalance and cannot address high frequency harmonics generated by the PWM switching. The amplitude of this higher frequency ripple is typically much higher than the low-frequency ripple and these higher frequency components generate the majority of the capacitor losses. In addition, the DC-link voltage harmonics induced by the switching currents cannot be ignored if the electric power quality is required to meet strict standards such as those found in aerospace; for example DO-160E [17] or MIL-STD-704F [18].

Only a few publications have addressed the problem of switching harmonic current reduction. In [9] Kolar et al developed a simple analytical expression to evaluate the DC-link capacitor RMS current in PWM-based converter systems. McGrath [10] has employed a double Fourier series to derive the exact solution to the DC-link current harmonic spectrum. These two works were instrumental in developing a theoretical understanding of switching harmonic generation, however just a few studies have reported practical approaches to the problem. Nguyen [11] proposed to reduce the switching harmonics using two non-adjacent active vectors in a space-vector PWM converter. Kieferndorf [12] proposed to maintain a high value of modulation index by the addition of a DC-DC boost circuit, however this limits the method's applicability.

Another trend in DC-link harmonic reduction employs PWM interleaving. In this method harmonics are cancelled by manipulating the PWM carrier waveforms. In [13], Gui-Jia Su employs segmented inverters to drive an induction motor with parallel windings. The DC-Link capacitor harmonic current is minimized by interleaving the carrier of each inverter. The PWM interleaving concept has also been applied in

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DC-AC-DC converters [19] to reduce the DC-link ripple current by adjusting the carrier phases according to the inverter input current. A dynamic PWM interleaving method was proposed by Shen [15]. In [15], the PWM carriers of each converter are closed-loop controlled according to the phase difference between the rectifier and the inverter harmonic currents. As such the inverter and rectifier DC-link harmonic currents are ensured to be in phase and hence cancel. The method demonstrated significant reduction of switching harmonic currents in the 1st and 2nd carrier bands, however as a side effect of this method, the AC harmonic current deteriorates, which limits its application.

In this paper, a method to reduce the DC-link capacitor switching harmonic currents while not compromising the AC-side current quality in two-level back-to-back converters is proposed. The approach is based on a derived analytical solution and targets the 2nd-carrier band harmonics only. The reduction in Total Harmonic Distortion (THD) is less than that provided by [15] however the AC side current does not deteriorate. The proposed method has been experimentally validated, results are given in Section IV.

II. THEORY OF THE PROPOSED METHOD

Typically, a three-phase AC-DC-AC back-to-back converter consists of two two-level converters, as shown in Fig. 2. One of them acts as rectifier and the other as an inverter.

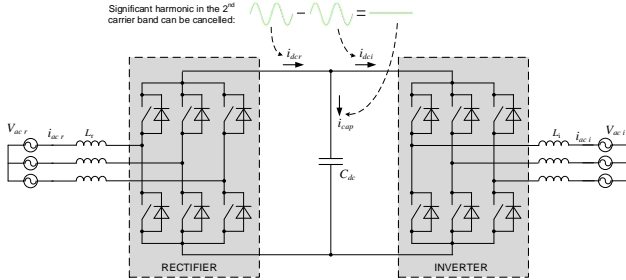


Fig. 2. Back-to-back converter schematic

From circuit theory, the harmonic current in the capacitor, including harmonic content, is the difference between the DC current of the inverter, i_{dc_i} , and the rectifier, i_{dc_r} :

$$i_{cap}(t) = i_{dc_i}(t) - i_{dc_r}(t) \quad (1)$$

For a two-level converter, the AC-side current is as follows:

$$i_{ac}(t) = I_{ac} \cos(2\pi f_0 t + \beta) \quad (2)$$

where I_{ac} is the amplitude of the fundamental component of the AC current, f_0 is the AC fundamental frequency and β is the angle between the AC source voltage and the AC current. The AC current flows into the DC-link through the power electronic switches; these conduct according to the interaction between the PWM carrier and the reference sinusoidal wave. For asymmetrical regular sampling PWM, the switching function can be expressed by:

$$sf(t) = K_{0,1} \cos(2\pi f_0 t + \theta_0) + \sum_{m=1}^{+\infty} \sum_{n=-\infty}^{-\infty} K_{m,n} \cos(m[2\pi f_c t + \theta_c] + n[2\pi f_0 t + \theta_0]) \quad (3)$$

where f_c is the carrier frequency, θ_c is the PWM carrier angle, $\theta_0 = 2k\pi/3$, m is the carrier band number, n is the side band number and k is the phase number. $k = 0, 1$ and 2 for phases A, B and C respectively. $K_{m,n}$ is the harmonic amplitude that is calculated using a Bessel function, J , of the 1st kind:

$$K_{m,n} = \frac{1}{q} J_n(qM) \sin\left([m+n] \frac{\pi}{2}\right) \quad (4)$$

In (4) $q = (m + n f_0 / f_c) \pi / 2$ and M is the modulation depth:

$$M = \frac{\sqrt{(V_{ac} - 2\pi f_0 L I_{ac} \sin \beta)^2 + (2\pi f_0 L I_{ac} \cos \beta)^2}}{V_{dc} / 2} \quad (5)$$

Using (2)-(5), the DC-link harmonic currents generated by one phase leg can be obtained as follows:

$$i_{dc}(t) = \frac{I_{ac}}{2} \left\{ \begin{aligned} & K_{0,1} \{ \cos(4\pi f_0 t + \theta_0 + \beta) + \cos(\theta_0 - \beta) \} \\ & + \sum_{m=1}^{+\infty} \sum_{n=-\infty}^{-\infty} K_{m,n} \{ \cos(2\pi[mf_c + (n+1)f_0]t + m\theta_c + n\theta_0 + \beta) \\ & \quad + \cos(2\pi[mf_c + (n-1)f_0]t + m\theta_c + n\theta_0 - \beta) \} \end{aligned} \right\} \quad (6)$$

The DC-link harmonic currents from the rectifier or the inverter are a superposition of the harmonic currents generated by each leg of corresponding converter. The difference between the rectifier and the inverter DC currents will determine the harmonic content of the ripple current through the DC-link capacitor. Hence, the analytical solution for the DC-link capacitor harmonic current can be derived as:

$$i_{cap}(t) = i_{dc_i}(t) - i_{dc_r}(t) = \frac{I_{ac}}{2} \left\{ \begin{aligned} & K_{r,0,1} \{ \cos(4\pi f_{0r} t + \sigma_{r,k,1}) + \cos(\varphi_{r,k,1}) \} \\ & + \sum_{m=1}^{+\infty} \sum_{n=-\infty}^{-\infty} K_{r,m,n} \left\{ \begin{aligned} & \cos(2\pi[mf_{cr} + (n+1)f_0]t + m\theta_{cc} + \sigma_{r,k,n}) \\ & + \cos(2\pi[mf_{cr} + (n-1)f_0]t + m\theta_{cc} - \varphi_{r,k,n}) \end{aligned} \right\} \end{aligned} \right\} \quad (7)$$

$$- \frac{I_{ac}}{2} \left\{ \begin{aligned} & K_{i,0,1} \{ \cos(4\pi f_{0i} t + \sigma_{i,k,1}) + \cos(\varphi_{i,k,1}) \} \\ & + \sum_{m=1}^{+\infty} \sum_{n=-\infty}^{-\infty} K_{i,m,n} \left\{ \begin{aligned} & \cos(2\pi[mf_{ci} + (n+1)f_0]t + \sigma_{i,k,n}) \\ & + \cos(2\pi[mf_{ci} + (n-1)f_0]t - \varphi_{i,k,n}) \end{aligned} \right\} \end{aligned} \right\}$$

where

$$\sigma_{k,n} = n \frac{2k\pi}{3} + \frac{2k\pi}{3} + \beta + n\alpha \quad (8)$$

$$\varphi_{k,n} = -n \frac{2k\pi}{3} + \frac{2k\pi}{3} + \beta + n\alpha \quad (9)$$

Here, α is the angle between the AC fundamental current and the AC-side converter voltage. θ_{cc} is the PWM carrier phase difference between the rectifier and the inverter, as illustrated by Fig. 3. Please note that in this study the inverter's PWM carrier phase is used as the reference. For each converter all legs use the same carrier without an inter-phase shift. This is the same control approach as was used in [15].

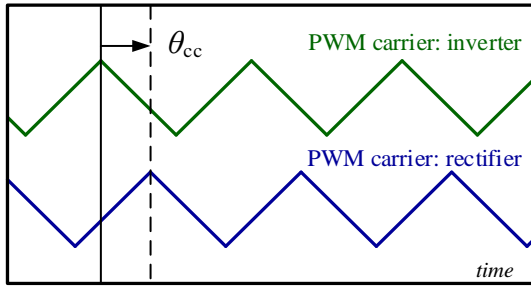


Fig. 3. Definition of PWM carrier angle

Using (7), the significant harmonic component in the 2nd carrier band (i.e. $m=2$) of the DC-link capacitor current can be derived:

$$i_{dc,2cap}(t) = i_{dc,i}(t) - i_{dc,r}(t)$$

$$= \frac{3I_{ac}}{2q} J_1(q_i M_i) (\cos(4\pi f_c t + 2\theta_{cc} - \beta_r - \alpha_r) - \cos(4\pi f_c t + 2\theta_{cc} + \beta_r - \alpha_r)) \quad (10)$$

$$- \frac{3I_{ac}}{2q} J_1(q_r M_r) (\cos(4\pi f_c t - \beta_i - \alpha_i) - \cos(4\pi f_c t + \beta_i - \alpha_i))$$

Analyzing (10), it can be concluded that the phase of the significant harmonic in the 2nd carrier band can be manipulated by the phase difference between PWM carriers, i.e. θ_{cc} . Hence this leads to the key idea proposed by this study; to reduce the DC-link capacitor harmonic currents in the 2nd carrier band by controlling the phase of the PWM carrier within one of the converters.

The advantage of the proposed method is that the AC-side current, in contrast to the method presented in [15], is not compromised. Based on the equation derived in [15] for AC-side phase voltage harmonics, the analytical solution to the AC harmonic current for a two-level converter can be obtained as follows:

$$I_{ac,k} = \frac{\frac{2V_{dc}}{q} \sum_{m=1}^{+\infty} \sum_{n=-\infty}^{-m} J_n(qM) \sin\left((m+n)\frac{\pi}{2}\right) \cos\left(m[2\pi f_c t + \theta_{cc}] + n[2\pi f_0 t + \frac{2k\pi}{3}]\right)}{2\pi m f_c L} \quad (11)$$

From (11) it can be concluded that the carrier angle can impact the phase of the AC harmonic currents but not their magnitudes. In the method detailed in [15] the DC-link harmonic current reduction is achieved by manipulating the carrier phases between different converter legs, changing the harmonic distribution and increasing the harmonic content of AC current spectrum. In contrast, the method proposed by this paper employs a common (or synchronized) PWM carrier for all legs and only the phase angle between the inverter and rectifier carrier waveforms is varied. Therefore, there is no impact on the AC harmonic content, as evidenced by (11). Based on theoretical discussion above, the next section describes the implementation of the proposed method.

III. THE PROPOSED METHOD

For conventional back-to-back converters, the DC-link current spectrum is shown in Fig. 4. The DC-link capacitor current harmonics of the 2nd carrier band dominate and therefore need to be suppressed.

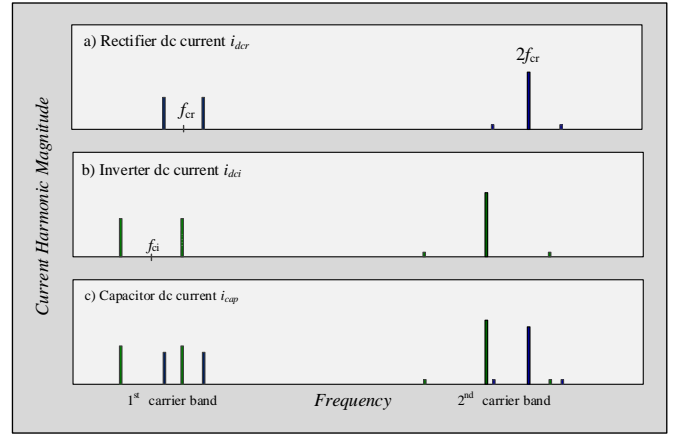


Fig. 4. DC-link current spectrum

Based on the theoretical considerations in the previous Section, the proposed active control of DC-link capacitor harmonic current content, targeting the significant harmonic of the 2nd carrier band, can be implemented using the following simple procedure:

- Adjust the frequencies of the rectifier and the inverter 2nd-carrier harmonics.
- Synchronize the carriers.

These steps are considered in more detail below.

Step 1. Adjusting the 2nd carrier band harmonic frequencies

In order to minimize the significant harmonic current in the 2nd carrier band, the frequency of the rectifier and the inverter 2nd carrier band harmonics should first be made identical. From (10) it can be seen that the 2nd carrier band harmonic frequency is double the carrier frequency. Hence the rectifier and the inverter carriers should be set to the same frequency (i.e. $f_{cr}=f_{ci}=f_c$) such that the harmonic frequencies of their 2nd carrier bands are identical. The DC-link capacitor current spectrum after this step is illustrated by Fig. 5.

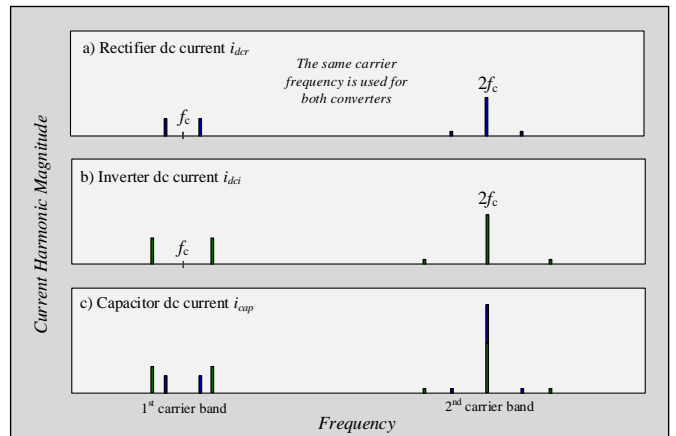


Fig. 5. DC-link current spectrum with the same carrier frequency for rectifier and inverter

Step 2. Synchronizing the 2nd carrier band harmonics

The 2nd carrier band harmonic current from the rectifier and the inverter can now be considered as two harmonic currents of the same frequency, however their phases are different. Hence, in

order to minimize the DC-link capacitor harmonic current, the phases of these two harmonic currents should be made the same. This can be achieved by adjusting the carrier phase difference θ_{cc} . In this study we propose to achieve this using closed-loop control, as will be detailed in Section IV. The DC-link capacitor current spectrum after this step is shown in Fig. 6. It can easily be seen from Fig. 6 that the harmonic content of the 2nd carrier band is significantly reduced.

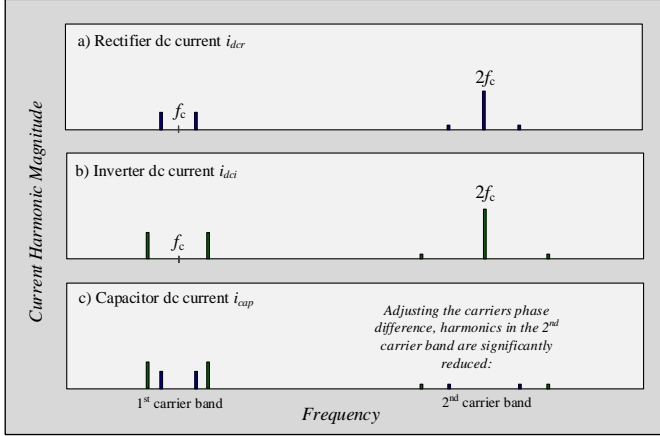


Fig. 6. DC-link current spectrum with PWM interleaving between the rectifier and the inverter

IV. EXPERIMENT VERIFICATION

In practical back-to-back converters, the rectifier and the inverter are normally controlled by separate controllers and the initial phases of their carriers are unknown. In order to synchronize the phases of both converters, the carrier waveform of the rectifier can be adjusted by either the discretion of the digital control system or by the settings of the oscillator within digital controller.

For the purpose of practical implementation, re-write (10) into the following form, assuming the harmonic phase of the inverter as the reference:

$$i_{dc2cap}(t) = \frac{3I_{acr}}{2q} J_1(q_r M_r) \begin{pmatrix} \cos(4\pi f_c t + 2\theta_{cc} - \beta_r - \alpha_r + \gamma) \\ -\cos(4\pi f_c t + 2\theta_{cc} + \beta_r - \alpha_r + \gamma) \end{pmatrix} - \frac{3I_{aci}}{2q} J_1(q_i M_i) \begin{pmatrix} \cos(4\pi f_c t - \beta_i - \alpha_i) \\ -\cos(4\pi f_c t + \beta_i - \alpha_i) \end{pmatrix} \quad (12)$$

where $\gamma = 4\pi\Delta f_c t + 2\theta_{cr0}$, Δf_c is the rectifier carrier frequency variance and θ_{cr0} is the initial carrier angle. Equation (12) can be simplified by introducing a new variable τ to denote the harmonic phase difference in the 2nd carrier band:

$$i_{dc2cap}(t) = \frac{3I_{acr}}{2q} J_1(q_r M_r) \cos(4\pi f_c t + 2\theta_{cc} + \tau) - \frac{3I_{aci}}{2q} J_1(q_i M_i) \cos(4\pi f_c t) \quad (13)$$

In general, the two harmonic current vectors from the rectifier and the inverter will not be in the same direction due to the resultant harmonic phase error. To solve the issue, this study

proposes a harmonic phase feedback to guarantee the same direction of both harmonics, as shown in Fig. 7. The DC-link current is measured and the harmonic current component of the 2nd carrier band is extracted using a Digital Band-pass Filter (BPF). The harmonic phase difference between the rectifier and the inverter is extracted using a phase meter which is implemented using an FPGA. Then, the required rectifier carrier angle can be derived from (13) assuming $i_{dc2cap}(t)=0$:

$$\theta_{cc} = -\tau/2 \quad (14)$$

To verify the proposed strategy, a test rig based on the diagram in Fig. 7 was implemented. A three-phase programmable power supply was used to feed the rectifier and an isolation transformer was used to eliminate the potential zero-sequence current loop. Both the rectifier and inverter employed asymmetric regular sampling PWM and were controlled in reference frames aligned with the corresponding AC voltages. Two Infinite Impulse Response (IIR) band-pass filters were implemented using FPGAs to extract the phases of the DC-link harmonic currents in the 2nd carrier band. As discussed above, the PWM carrier angle of the inverter is considered as the reference, hence considered as zero. Table I details the test rig configuration. During the experiments, θ_{cc} was updated every 1/3rds, and the rectifier was operated at unity power factor.

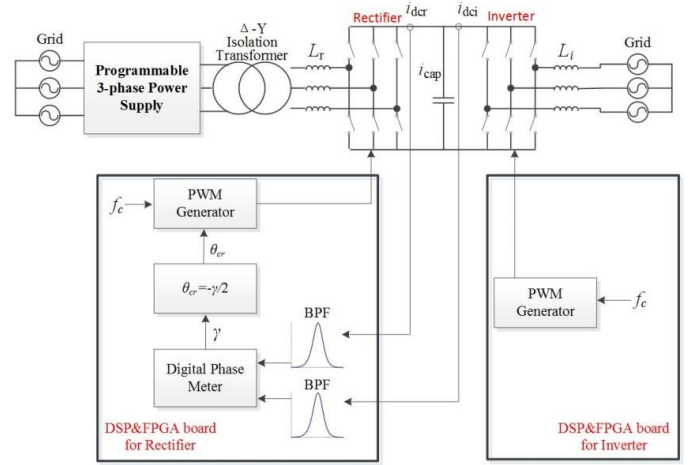


Fig. 7. Proposed method: control system diagram

TABLE I. TEST RIG CONFIGURATION

Parameters	Value
DC-link capacitance	4.4mF
Rectifier line inductance L_r	2.33mH
Inverter line inductance L_i	2.33mH
DC bus voltage	750V
Rectifier power factor	Unity
Output voltage of programmable power supply	240Vrms
Output frequency of programmable power supply	60Hz
Grid voltage	240Vrms
Grid frequency	50Hz
Carrier Frequency	7000Hz
Bandwidth of IIR band-pass filter	13900Hz-14100Hz

The experimentally measured DC-link currents, when using conventional PWM and when utilizing the proposed method, are shown in Fig. 8 and Fig. 9 respectively. During the tests shown in Fig. 8 and Fig. 9 the AC-side current magnitude was 7.8A and the inverter was operated at unity power factor. The PWM carrier frequency was set to 7kHz and so as such the frequency of the significant harmonic in the 2nd carrier band was 14kHz. For the reported case the magnitudes of the rectifier and the inverter DC-link harmonic currents in the 2nd carrier band are similar, hence the DC-link capacitor harmonic current is greatly reduced. Comparing the results highlighted by a dashed red square in Fig. 9 against those for the conventional system in Fig. 8, the effectiveness of the proposed method can easily be seen. Fig. 8 and Fig. 9 also highlight that as the 1st carrier band harmonics of the rectifier and the inverter are of different frequencies, the distribution and magnitude of the harmonics in the 1st carrier band remain the same as for conventional PWM.

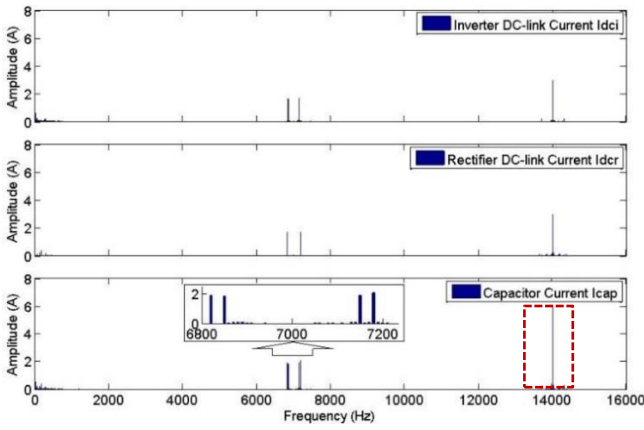


Fig. 8. DC-link current spectrum of the conventional PWM

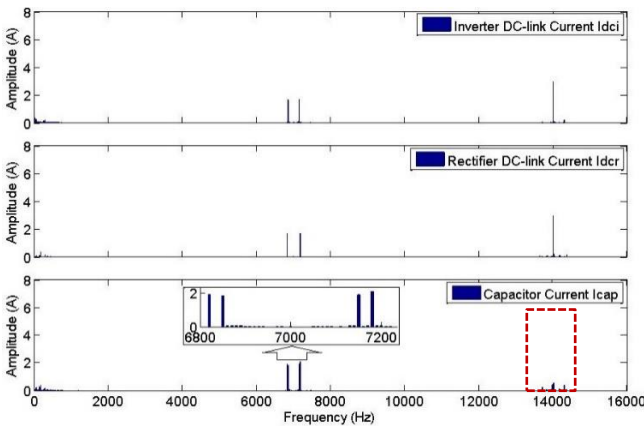


Fig. 9. DC-link current spectrum of the proposed method

The effectiveness of the proposed harmonic reduction method has also been verified by examining the capacitor current waveforms, as shown in Fig. 10. It can be seen that the current ripple when using the proposed method is significantly lower than that obtained when using the conventional PWM approach.

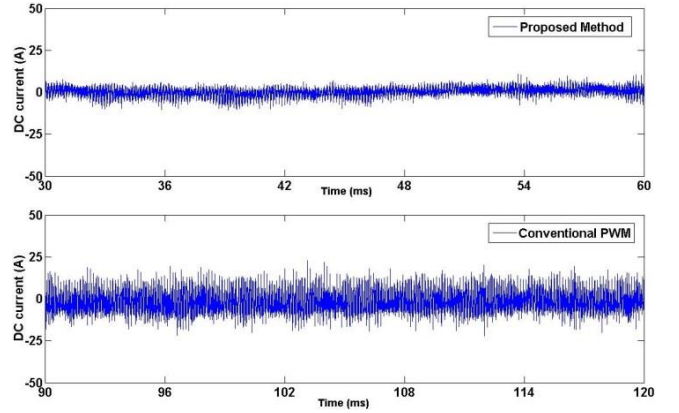


Fig. 10. DC-link capacitor harmonic current waveform comparison

Experimental verification was also performed on the effect of the proposed carrier shift method on AC side currents. As established theoretically in Sections II and III this method should have no influence on the AC current waveforms. The results shown in Fig.11 confirm this theoretical finding as the AC current spectrums, and their waveforms, do not change when the carrier shift is introduced.

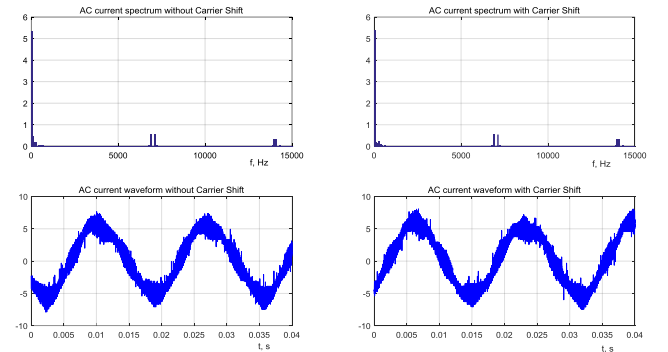


Fig. 11. Effect of the proposed Carrier Shift method on AC-side current

V. DISCUSSION

This section gives further discussion on the performance of the proposed method under differing converter operating conditions. It also examines the impact of the converter carrier shift on AC harmonic current.

A. Effect of harmonic magnitude difference in the 2nd carrier band

The magnitude of the harmonic current injected into the DC-link varies with the operating conditions of the converter. Using the analytical result for i_{dci} in (7), Fig. 12 shows the relationship between the significant harmonic amplitude in the 2nd carrier band, the AC current and β of the inverter. The harmonic magnitude increases with increasing AC current and the highest value is achieved at unity power factor. Harmonics with different magnitudes can be injected into the DC-link from the rectifier and the inverter as they operate under different operating conditions. As a result, some residual capacitor harmonic current in the 2nd carrier band can be observed. Fig. 13 shows this residual harmonic amplitude as a function of AC current and β . It can be seen that compared to the amplitude of the harmonic injected into DC-link, the residual capacitor harmonic current is relatively small. The results in Fig. 13 also

confirm that reduction of the harmonic current can be achieved over the entire current- β plane.

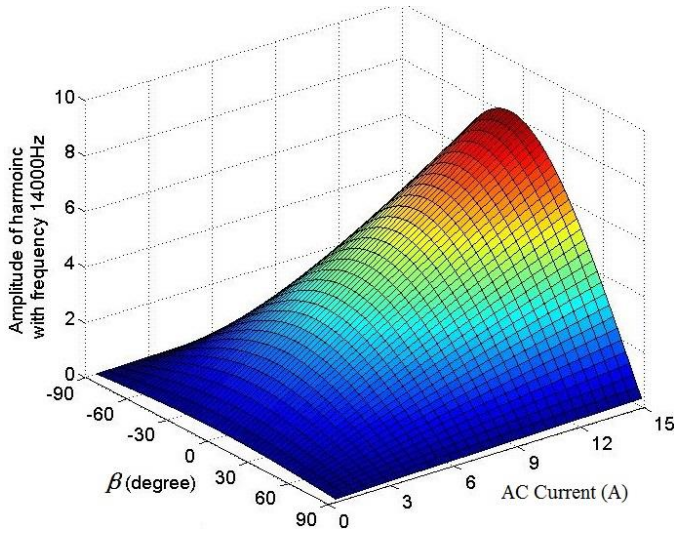


Fig. 12. Significant harmonic current amplitude in the 2nd carrier band of the inverter under different operating conditions

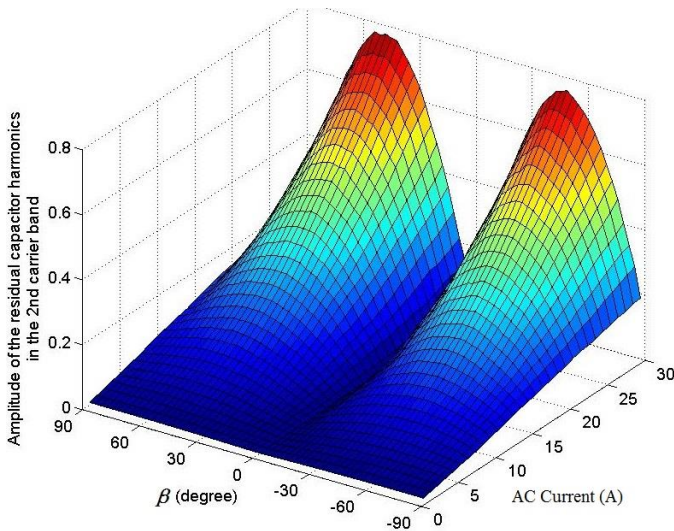


Fig. 13. The amplitude of the residual harmonic current in DC-link capacitor

B. Improvement of THD over the conventional method

The overall improvement of capacitor harmonic current, in comparison to conventional PWM, can be assessed by calculating the THD before and after implementation of the proposed method. This can be expressed as η and defined as given below:

$$\eta = \frac{\text{THD}_c - \text{THD}_p}{\text{THD}_c} \quad (15)$$

where THD_c and THD_p are the capacitor current THD for conventional PWM and for the proposed method, respectively. Fig. 14 shows the dependence of η on the AC current magnitude and β . As can be observed, the best THD improvement is obtained when the inverter operates around the unity power factor.

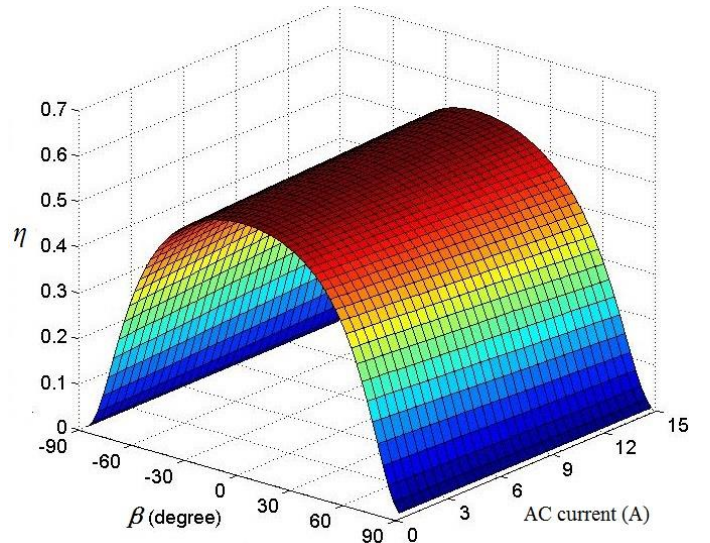


Fig. 14. THD improvement vs AC current and β

From Fig. 14 it can be seen that an improvement in THD of up to 55% can be achieved by using the proposed method.

The research findings presented in this paper, the advantages of the proposed method and the practical implications can be summarized as follows:

- The proposed method greatly reduces the 2nd carrier band harmonics in the DC-link capacitor of two level, three phase, back-to-back AC-DC-AC converters;
- It has been shown that the DC-link capacitor current THD can be reduced by up to 55% in comparison to the conventional PWM methodology;
- Unlike previously reported methods, the proposed method does not degrade the AC-side waveforms;
- It has been shown that using the proposed method harmonic mitigation can be achieved over the entire inverter current- β plane;
- The proposed method also has significant practical advantages. Firstly, it has no impact on the voltage and current control loops and so can be very easily integrated into new and existing control systems of back-to-back converters. Furthermore, the implementation of this method requires no additional cost as modifications only take place in software, no extra hardware is needed;
- Finally, as highlight in the introduction, the proposed method enables the reduction in DC-link capacitor rating by minimizing DC link current ripple. This therefore decreases the capacitor weight, volume and cost, as well as increasing the power density and reliability for the overall converter.

Overall, the proposed method is able to increase converter power density and reliability by decreasing DC-link harmonic content while, unlike previous methods, also having no deteriorating impact on AC side current waveforms. This method could therefore be of great importance for applications such as aerospace, electric vehicles and the military where minimization of size, weight and AC side harmonics are crucial.

VI. CONCLUSIONS

This paper has proposed a novel method of actively-controlled PWM interleaving for back-to-back converters in order to suppress the DC-link capacitor harmonic current in the 2nd carrier band and reduce the overall harmonic content. The theory of the proposed approach has been reported. Based on a derived analytical solution for DC-link capacitor harmonic current, it was shown that by adjusting the phase difference between the PWM carriers of the rectifier and inverter it becomes possible to synchronize their 2nd carrier band harmonics. As a result, self-cancellation of the 2nd carrier band harmonics can be achieved. Unlike previous methods, it has been shown that the proposed method has no effect on the AC side waveforms.

The proposed method has been verified experimentally using a three-phase, two-level, back-to-back converter. As the proposed method enables increased converter power density and reliability by decreasing DC-link harmonic content, while also having no deteriorating impact on AC side current waveforms and requiring no additional hardware, this method is highly applicable for applications such as aerospace, electric vehicles and the military.

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