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Low Source/Drain Contact Resistance for AlGaN/GaN HEMTs with High Al Concentration and Si-HP [111] Substrate

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An optimized fabrication process of ohmic contacts is proposed to reduce the source/drain access resistance (R_C) and enhance DC/RF performance of AlGaN/GaN HEMTs with a high Al concentration. We show that source/drain R_C can be considerably lowered by (i) optimally etching into the barrier layer using Ar^+ ion beam, and by (ii) forming recessed contact metallization using an optimized Ti/Al/Ni/Au (12 nm/200 nm/40 nm/100 nm) multilayers. We found that a low R_C of ~0.3 Ω.mm can be achieved by etching closer to the 2-Dimensional Electron Gas (2DEG) at an optimum etching depth, 75% of the barrier thickness, followed by a rapid thermal annealing at 850°C. This is due to the very small distance between the alloy and the 2DEG (higher electric field) as shown by 2D drift-diffusion simulations combined with Transmission Line Model (TLM) extractions.

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AlGaN/GaN High Electron Mobility Transistors (HEMTs) are significantly beneficial to the semiconductor device industry. They have the potential to replace Si in a range of high-power and high-frequency applications due to the wide bandgap, high electron saturation velocity, good thermal conductivity and high piezoelectricity of III-Nitrides materials.[1–4] To fully benefit from the aforementioned material properties, reduction of extrinsic source and drain access resistances (R_C) of AlGaN/GaN HEMTs is essential to enhance their DC/RF performance. To achieve this, several methodologies have been previously proposed.[5–9] Firstly, implanting Si into the AlGaN barrier is known to reduce ohmic contact, R_C. However, annealing contacts at high temperatures, to activate dopants, results in diffusion of the Si dopants away from the contacts. The result is increased high-frequency (HF) charge trapping and gate leakage current.[10] Secondly, increasing the Al concentration in the barrier and/or using AlN exclusion layer is known to increase 2-Dimensional Electron Gas (2DEG) confinement and to enhance 2DEG density and mobility, which enhances performance.[8,9] However, it results in increased R_C due to low metal diffusion beneath the metal contact.[11,12]

In this work, we propose a fabrication process of ohmic contacts to reduce R_C of AlGaN/GaN HEMTs with a high Al concentration, while avoiding implantations that cause HF-traps and gate leakage. This is essential for enhancing device DC and RF performance. For this new proposal, the outer edges of an AlGaN/GaN HEMT, where the source and drain ohmic contacts are to be placed, are etched from the surface of the device down into the AlGaN barrier layer. Contact metal is then evaporated onto the etched locations and rapidly annealed under high temperatures. During the annealing process, contact metal diffuses into the AlGaN barrier layer to form an alloy beneath the metal contact. The change in R_C at different etching depths at various annealing conditions is investigated to identify the optimal etching depth given by the lowest R_C.

The epi-structure of the investigated devices is presented in Device structure section of this paper. The source and drain contact metallization multilayer scheme and ohmic contact formation are described in Ohmic contact formation section. The experimental procedure describing the barrier etching technique and various configurations in terms of etched depths and annealing conditions is presented in Experimental section. In Performance of the contact scheme section, the optimal fabrication process of ohmic contact is identified and verified by comparing R_C values for each configuration with the corresponding transfer length (L_T), characterized by the current distribution beneath the contact. Finally, conclusions are drawn in Conclusions section.

Device Structure

A schematic cross-section of the investigated AlGaN/GaN epi-structure is illustrated in Fig. 1. This structure is grown by Molecular Beam Epitaxy (MBE) on a High-Purity (HP) and highly-resistive ($\rho >$ 5 kΩ.cm) Silicon substrate with [111] orientation. It consists, from the substrate to the top, of low-temperature AlN/GaN/AlN nucleation layers for stress accommodation, and a 1 μm $Al_{0.07}Ga_{0.93}N$ back-barrier to reduce alloy scattering and to improve the carrier confinement of the 2DEG. A channel is made of a 100 nm thick unintentionally doped

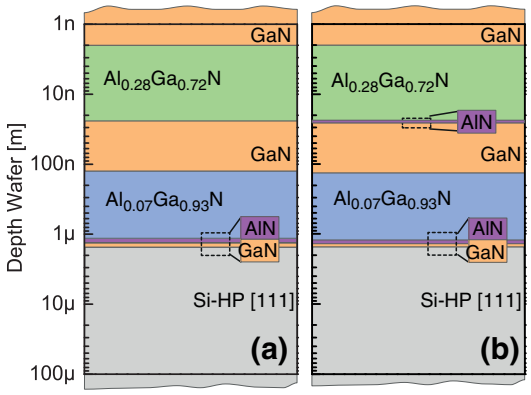

Figure 1. Schematic cross-section of AlGaN/GaN epi-structures grown on the Si-HP [111] substrate with Ti/Al/Ni/Au (12 nm/200 nm/40 nm/100 nm) contact metallization (a) without AlN exclusion layer, (b) with AlN exclusion layer.

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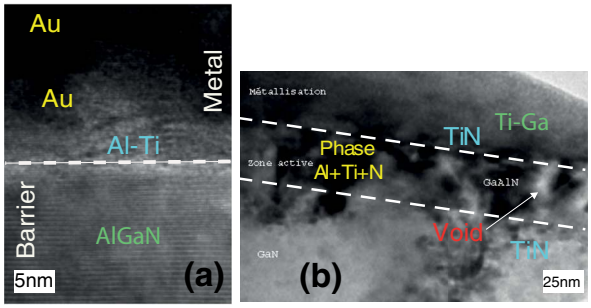

Figure 2. HRTEM images of ohmic contacts at the Ti/$Al_{0.28}Ga_{0.72}N$ interface after rapid thermal annealing forming an alloy compositions at (a) 750°C and (b) 900°C.

GaN buffer followed by a 1 nm AlN exclusion and a 20 nm undoped $Al_{0.28}Ga_{0.72}N$ layers to increase the electron density in the 2DEG and to reduce alloy disorder scattering.[13] Finally, a 2 nm GaN cap layer is grown in order to reduce surface traps. The material growth process and conditions to form this epi-structure are similar to those given in previous works by Cordier.[14]

Ohmic Contact Formation

To optimize the metallization scheme, particularly the Ti/Al ratio, Ti metal is first evaporated on the epi-structure shown in Fig. 1a, without AlN exclusion layer. The contact is then annealed at two different temperatures, one sample (S1) at 750°C and another one (S2) at 900°C. The Ti/AlGaN/GaN interfaces are then examined using High Resolution Transmission Electron Microscopy (HRTEM) images. The HRTEM image of S1, annealed at 750°C, shows few Ti-Al alloy clusters and an abrupt interface (Fig. 2a). Here, the reactivity of Ti with AlGaN is low and, therefore, the formed alloy is small. However, S2, annealed at 900°C, has a larger alloy formation (Fig. 2b). Multiple compositions of alloy are formed, consisting of (i) Ti-Ga on the top, (ii) TiN at the interface, and (iii) Al + Ti + N + Ga. The formation of the alloy stems from N atoms reacting with Ti, to create a TiN alloy. This is observed below the contact metallization. The greater reactivity between Ti and N can be seen at high annealing temperatures, which produces a greater TiN alloy formation. However, as a result of higher annealing temperature, a greater void formation is observed. This void formation can be reduced with incorporation of Al through the metallization scheme. Al concentration in the barrier layer also increases reactivity of Ti from the metal contact and N from the barrier layer to form an $AlTi_2N$ alloy.[15,16]

The addition of Al into the metallization scheme is observed in Fig. 3 with HRTEM imaging at 900°C annealing temperature to clearly show alloy formation. At such high temperatures, (i) Al diffuses into the Ti layer of the metallization to form Ti-Al bonds, and (ii) there is a high reactivity with oxygen at the Ti/Al interface which causes an AlO_X-TiO_X alloy to form. The increase in the Ti/Al ratio allows the formation of TiN layer, which is favorable to obtain a good ohmic contact. Decreasing the Ti/Al ratio, however, reduces the reactivity of Ti at the interface and, consequently, leads to the formation of voids. Therefore, a compromise between these two has to be find. A Ti/Al ratio of 6% has been found experimentally to be the best Ti/Al/Ni/Au (12 nm/200 nm/40 nm/100 nm) multilayers for the ohmic contact metallization.[17]

The challenge is how to form a good ohmic contact with a low R_C for the epi-structure shown in Fig. 2b, including the AlN exclusion layer. We have observed that the presence of high Al concentration in the barrier and/or AlN exclusion layer, reduces the diffusion of metal in the barrier and significantly degrades R_C. To overcome this difficulty, we use the same metallization scheme as described above and recessed the source/drain metallization at different depths to find an optimum contact as summarized in the following section.

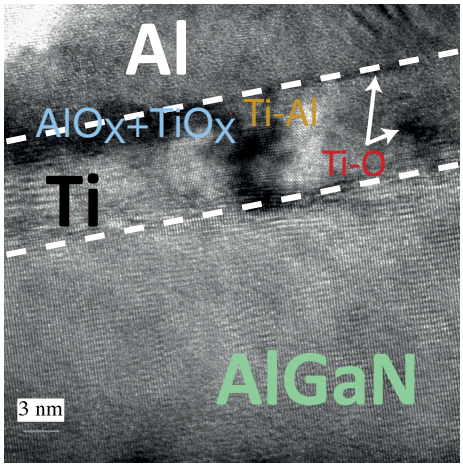

Figure 3. HRTEM image of ohmic contact at the Al/Ti/$Al_{0.28}Ga_{0.72}N$ interface after rapid thermal annealing forming alloy compositions at 900°C.

Experimental

In order to identify an optimal contact formation that provides lowest R_C, various ohmic contact configurations are tested. The GaN/$Al_{0.28}Ga_{0.72}N$/AlN barrier layers of the epi-structure (Fig. 2b) are dry etched using an Ar^+ ion ebeam evaporation at different depths ranging from 0% to 100%, as illustrated in Fig. 4. The condition used for the etching is Ar flow of 12sscm and ion energy of 300 eV. The etching rate of the barrier is around 4 nm/min. The source and drain contact metallization, which consists of Ti/Al/Ni/Au (12 nm/200 nm/40 nm/100 nm) multilayers, are then evaporated onto this epi-structure. The metallization for each etched depth is rapidly annealed at various temperatures ranging from 750°C to 900°C for 30 s in a nitrogen atmosphere.

Upon annealing the contacts, an alloy forms due to metal diffusion. The alloy thickness is dependent on the Al volume beneath the metal. When the epi-structure is etched further into the GaN/$Al_{0.28}Ga_{0.72}N$/AlN layers, there is less Al volume beneath the metal contact. Here, a greater quantity of alloy, and therefore greater alloy thickness, is formed during the annealing process; i.e. 75% etching depth has greater alloy thickness than 0%.

In order to identify and analyze the influence of the etched depth on alloy thickness and R_C, the Transmission Line Model (TLM) model, illustrated in Fig. 4, is used.[18] The sheet resistance beneath the metal contact (R_{SK}) and the sheet resistance outside of the contact area (R_{SH}) are also calculated using the TLM approach. R_C is extracted for each

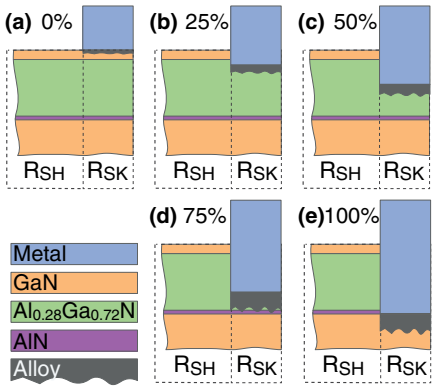

Figure 4. Illustration of alloy thickness under different etching depths. Greater quantity of Al beneath the metal results in less alloy thickness (a) 0%, (b) 25%, (c) 50%, (d) 75% and (e) 100% [not to scale]. R_{SK} is the sheet resistance beneath the metal contact and R_{SH} is the sheet resistance outside of the contact area.

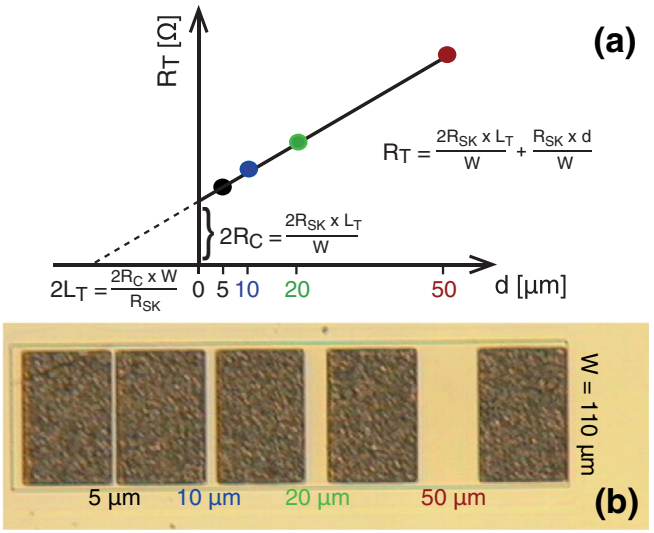

Figure 5. (a) Illustration of the TLM model, showing equations for extraction of its parameters (R_C, R_{SH}, R_{SK}, L_T). (b) top-down view of used TLM and dimensions for parameters extraction.

etched depth and at different annealing temperatures ranging from 750°C to 900°C. To apply the TLM, the spacing between the ohmic contacts, d, is varied from 5 μm to 50 μm as shown in Fig. 5a. DC I-V characteristics of each neighboring contacts are measured. Then, the slope of the linear region of I-V characteristics are taken to extract the total resistance (R_T) for each TLM, in Fig. 5b. In order to extract R_C, the relationship between R_T and d is extrapolated to d = 0 μm where $R_T = 2 \times R_C$. Extrapolating further to $R_T = 0$ Ω extracts L_T, which is later used to analyze the current distributions. R_{SK} is then extracted through substitution of L_T at d = 0 μm. Finally, R_{SH} is extracted through substitution of R_{SK} and L_T into the extracted R_T-d.

Performance of the Contact Scheme

Fig. 6 represents the R_{SK}/R_{SH} ratio as a function of R_C to denote the impact of sheet resistance beneath the contact. The different data points at each recess depth correspond to different annealing temperatures. At recess depth of 0%, 25% and 50%, there is relatively a small metal diffusion and, consequently, the contact metal is away from the

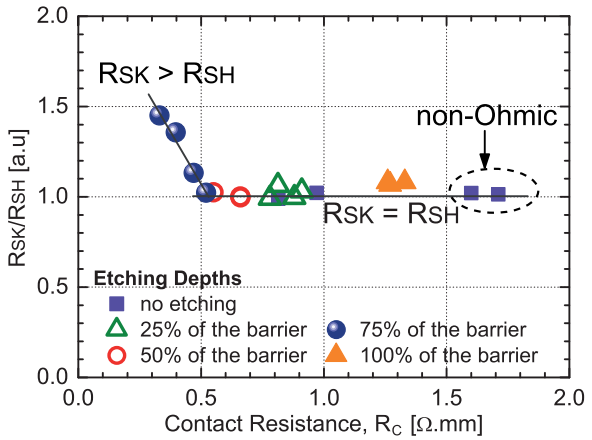

Figure 6. Ratio of R_{SK}/R_{SH} versus R_C. The different data points at each etching depth correspond to different annealing temperatures. 75% etching depth provides $R_{SK} > R_{SH}$ whereas other etching provides $R_{SK} \approx R_{SH}$. This is due to (i) minimal diffusion of alloy and a large volume of AlGaN barrier beneath the contact in 0%, 25% and 50% etching, and (ii) damage to the 2DEG in 100% etching.

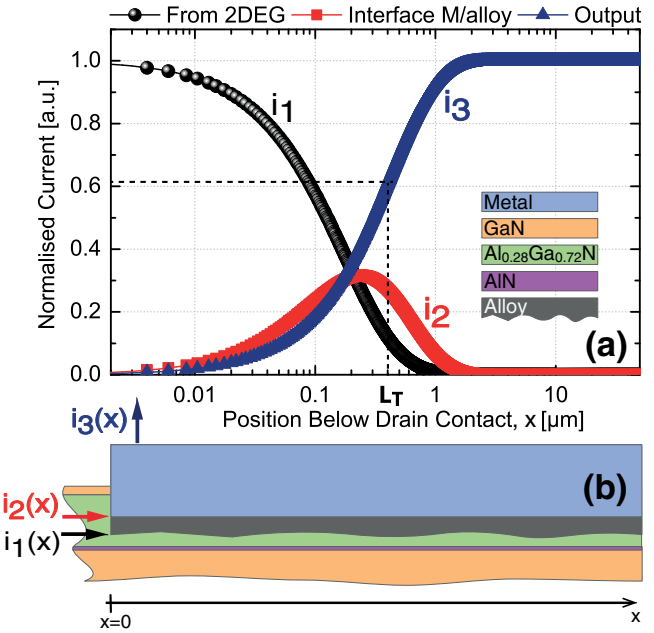

Figure 7. (a) Lateral current distribution at the alloy/AlGaN interface (i_1), at the metal/alloy interface (i_2), and the current entering/exiting in/out of the contact (i_3). (b) Illustration of the corresponding current distributions for i_1, i_2, and i_3.

2DEG. This is due to the large Al volume beneath the metal contact, which induces less reactivity in Ti as described in Ohmic contact formation section. Therefore, the AlGaN barrier layer is the limiting factor for current to flow and hence $R_{SK} \approx R_{SH}$. $R_{SK} > R_{SH}$ only at 75% etching depth, where only 25% of the barrier is left. This occurs due to bombardment of Ar^+ ions that partially destroys the crystal alignment near the 2DEG during the etching process.[17] However, in this case, there is a small distance between the diffused metal and the 2DEG due to the large alloy thickness that has formed. Hence, there is an overall reduction of R_C. Like all etching depth configurations, the ohmic contacts for '75% etching depth' are annealed at different temperatures (circle symbols in Fig. 6). As annealing temperature increases, the alloy thickness increases as well as the void formation. This results in poorer alloy quality which increases R_{SK} but the alloy becomes increasingly closer to the 2DEG, reducing R_C further. For '75% etching depth' configuration, the optimal annealing temperature, to provide lowest $R_C \approx 0.3$ Ω.mm, that forms an alloy close enough to 2DEG with less crystal alignment damage, is found to be 850°C. It is noted that the annealing temperature has a greater impact on '75% etching depth' devices, when excluding the non-ohmic contacts.

One could expect that at 100% etching depth there would be the lowest R_C and $R_{SK} > R_{SH}$, which is not the case. As the GaN/$Al_{0.28}Ga_{0.72}N$/AlN layers are completely etched at the contact locations (see Fig. 4e), the 2DEG at the contact is destroyed. On top of this, current flow can only access the contact at its inner edge as opposed to the whole contact width of the alloy/AlGaN interface. These contribute toward the significant increase of R_C. To note, R_{SK} is slightly larger than R_{SH} for 100% etching as the AlGaN barrier has been completely etched. Therefore, in this instance, R_{SK} only considers the sheet resistance of the alloy and GaN buffer layer; both of which have higher resistance than AlGaN.

The current distributions in the contact of '75% etching depth' with the lowest R_C is calculated using TLM model. Fig. 7 presents the lateral current distributions at the alloy/AlGaN interface (i_1), the metal/alloy interface (i_2), and the current collected by the metal layer of a contact (i_3). These results show an exponential decrease in current dispersion which occurs in i_1 as the majority of current enters the inner edge of the contact. Here, the current density at the inner edge is at its peak across the lateral span of the contact. The high resistance

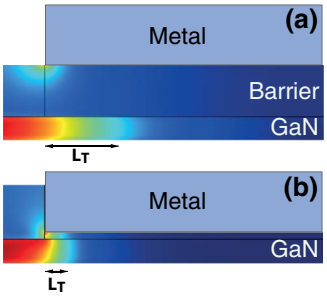

Figure 8. 2D current density distributions of two ohmic contact configurations, 0% and 75% etched barrier depths. The L_T decrease as etching depth increases is caused by larger electric field between the contact metal and 2DEG.

alloy limits the current flowing through to the metal contact at the inner edge. Current flows laterally away from the inner edge in the alloy/AlGaN interface to where less high resistance alloy clusters have formed. Then current is able to flow vertically through the metal layer. Therefore, an exponential increase in i_3 occurs. The transfer length (L_T), that characterizes the current distribution beneath the contact,[19] is found to be ~0.6 μm for the lowest R_C configuration.

To illustrate the relationship between L_T and etched barrier depth, 2D drift-diffusion simulations have been carried out. 2D distributions of the current density for 0% and 75% etched barrier depths are shown in Fig. 8. This shows that with increased etching depth (e.g. 75%) then L_T reduces. With deeper etching depth, a greater electric field is induced between the metal/alloy and the 2DEG and more energy is induced for charge carriers to enter/exit into or out of the contact at its inner edge, not shown. Hence, the current density at the inner edge of the contact will be higher, reducing R_C.

Using the TLM model, L_T is extracted and compared with R_C for each ohmic contact configuration, etching depth and annealing temperature, in Fig. 9. As expected, L_T is generally proportional to R_C, independently of the contact configuration. However, a significant issue may occur with low L_T. A high current density at the inner edges of the contact could result in a large increase in self-heating at this location. The heat dissipates throughout the device and contributes to degradation and potential failure of the device.[20] This issue will be investigated in future works.

Conclusions

We have experimentally shown that the contact resistance, R_C, of AlGaN/GaN HEMTs with AlN exclusion layer ($GaN/Al_{0.28}Ga_{0.72}N/AlN$) can be significantly reduce to 0.3 Ω.mm. This has been achieved by (i) etching $\frac{3}{4}$ of the barrier using Ar^+ ion beam dry etching, (ii) using an optimized Ti/Al/Ni/Au (12 nm/200 nm/40 nm/100 nm) multilayer metallization scheme and (iii) rapid annealing temperature of 850°C. Despite the possible partial damage of 2DEG due to Ar^+ bombardment during etching process, the very small distance between the alloy and the 2DEG has led to an overall reduction of R_C. The TLM model extraction combined with 2D drift-diffusion simulations have shown that small R_C leads to a small transfer length, L_T. This could be an issue in terms of thermal management. With the small L_T, a high current density at the inner edges of the contact could results in a large increase in self-heating at this location.

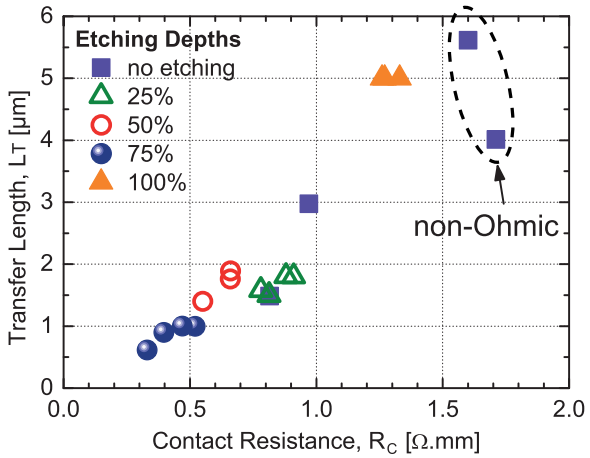

Figure 9. Transfer length (L_T) versus R_C. Device with 75% etching depth has the lowest R_C at 850°C annealing temperature.

Acknowledgments

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