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ELECTRICAL CHARACTERISTICS
OF SRO-MISS DEVICES
AND THEIR APPLICATIONS

by

Burhanuddin bin Haji Yeop Majlis

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This thesis is submitted to the University of Durham
in candidature for the degree of Doctor of Philosophy

School of Engineering and Applied Science
University of Durham
October 1988

- 2 NOV 1989

Dedicated to my mother, wife and sons.

Know that the life of this world is only play, and idle talk, and pageantry, and boasting among you, and rivalry in respect of wealth and children; as the likeness of vegetation after rain, whereof the growth is pleasing to the husbandman, but afterward it drieth up and thou seest it turning yellow then it becometh straw. And in the Hereafter there is grievous punishment, and (also) forgiveness from Allah and His good pleasure, whereas the life of the world is but matter of illusion.

(Holy Qu'ran 57:20)

DECLARATION OF ORIGINALITY

I declare that the work presented here has not been submitted for any other degree. This thesis is my original work, except where indicated by refrence to other work.

ABSTRACT

The electrical characteristics of the Metal-Insulator-Semiconductor - Switch (MISS) device with Silicon-Rich-Oxide (SRO) as the semi-insulating material have been comprehensively studied at room temperature in an exploratory way. The SRO films were deposited by atmospheric pressure chemical vapour deposition (APCVD) at 650^oC with SiH_4 and N_2O reactant gases and N_2 carrier. The reactant gas phase ratio R_o varying from 0.09 to 0.25 and the deposition time varying from 0.6 to 2 min. Some preliminary investigations on SRO-MIS devices were also carried out in order to understand the electronic process in the structure. Various parameters which governed the switching behaviour of an MISS were investigated. In general the switching characteristics are similar to those of the tunnel oxide MISS. The geometrical dependence of the switching behaviour in the tunnel oxide MISS has been extended to the present device by looking at the effects of electrode area, junction area, electrode perimeters and of a metal guard ring. Other effects, such as SRO deposition time, work function difference, gold doping, heat treatment, light illumination and film ageing were also observed. The dynamic characteristic of the device was studied using a double pulse technique.

The characteristics of the three-terminal SRO-MISS were studied in both forward and reverse bias. The former exhibited a thyristor-like characteristic and the latter a transistor-like characteristic. A preliminary study on the MIS-emitter transistor was carried out with different emitter areas. In general the characteristics are the same as for the equivalent tunnel oxide devices. However it was also found that if the n-type epilayer is very thin the transistor characteristics exhibits an N-type negative resistance.

The negative resistance region of the two-terminal MISS has been shown to be stable and the stability has been analysed in terms of equivalent circuit elements. The reason for the stability is that the device also has an negative capacitance. This has been proved experimentally and it is a new property of the MISS structure which never been reported before. The negative capacitance has been measured as a function of electrode area, SRO type and light illumination. An important circuit application for the negative capacitance has also been suggested and demonstrated

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LIST OF SYMBOLS

A_j - p-n junction area.

A_o - Tunnel insulator area.

$A_e(A_p)$ - Effective Richardson constant for electrons (holes).

C_i - Insulator capacitance per unit area.

$D_n(D_p)$ - Diffusion coefficient for electron (holes).

d - Semi-insulator thickness.

E_c - Lowest conduction band energy level.

E_i - Intrinsic Fermi level.

E_v - Highest valence band energy level.

E_g - Semiconductor energy gap.

E_t - Interface trap energy level.

E_{Fm} - Fermi level of metal.

E_{Fp} - Fermi level of the p-type semiconductor.

E_{Fn} - Fermi level of the n-type semiconductor.

G - Small-signal total gain.

G_s - Small-signal MIS gain.

G_j - Small-signal p-n junction gain.

I_h - Holding current.

I_s - Switching current.

I_{OFF} - Total current through the MISS in the OFF state.

I_{ON} - Total current through the MISS in the ON state.

I_g - Generation current density in the surface depletion region.

J_{dn} - Electron p-n junction diffusion current density.

J_{dp} - Hole p-n junction diffusion current density.

J_{nj} - Electron diffusion current density in the p-n junction.

J_{tn} - Electron tunnel current density.

J_{tp} - Hole tunnel current density.

J_{pj} - Hole diffusion current density in the p-n junction.

J_{rj} - Recombination current density in the p-n junction.

k - Boltzman constant in eV/°K.

L - Length of the neutral n region.

L_n - Diffusion length for electrons in the p region.

M - Current multiplication factor for MIS in reverse bias.

M_a - Avalanche multiplication coefficient.

$N_a(N_d)$ - Impurity doping density in the p[n] region.

n_i - Intrinsic carrier density in the semiconductor.

q - Magnitude of electronic charge.

Q_i - Total charge per unit area at the interface.

Q_f - Fixed charge density per unit area.

Q_s - Charge per unit area in the semiconductor.

T - Temperature in degrees Kelvin.

V - Voltage applied to the MISS device.

V_a - Avalanche breakdown voltage of the n-type epilayer.

V_{FB} - Flat-band voltage.

V_h - Holding voltage.

V_s - Switching voltage.

V_j - Voltage drop across the p-n junction.

V_i - Voltage drop across the insulator.

X_d - Width of the surface depletion region.

W_j - Width of the p-n junction depletion region.

W_n - Epitaxial layer thickness.

Greek Letters

β_p - p-n junction gain for holes.

$\epsilon_i(\epsilon_s)$ - Permittivity of the insulator (semiconductor) in farad/cm.

τ_{epi} - Lifetime of holes in the n-type epitaxial layer.

τ_n - Lifetime of electrons in the p-type subtrate.

ϕ_{ms} - Metal-semiconductor work function difference.

ϕ_m - Metal work function.

ϕ_s - Semiconductor work function.

ϕ_b - Potential difference between the Fermi level and intrinsic Fermi level.

$\sigma_n(\sigma_p)$ - Capture cross section of electrons (holes).

ψ_s - Surface potential in the semiconductor.

ψ_{sp} - Surface potential in the semiconductor at punch-trough.

$\chi_n(\chi_p)$ - Tunnelling barrier height for electrons (holes).

$\gamma_n(\gamma_p)$ - Injection efficiency of electrons (holes).

$\eta_n(\eta_p)$ - Barrier tunnelling transmision coefficient for electrons (holes).

Abbreviations

APCVD- Atmospheric Pressure Chemical Vapour Deposition

CID - Control-Inversion-Device

CVD - Chemical Vapour Deposition

MIS - Metal-Insulator-Semiconductor

MISS - Metal-Insulator-Semiconductor-Switch

MIST - Metal-Insulator-Semiconductor-Thyristor

MISM - Metal-Insulator-Semiconductor-Metal

MISIM - Metal-Insulator-Semiconductor-Insulator-Metal

SIPOS - Semi-Insulating-Polycrystalline-Silicon

SRO - Silicon-Rich-Oxide

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CHAPTER ONE

INTRODUCTION

1.1 SEMICONDUCTOR DEVICE STRUCTURES

In general semiconductor devices can be classified into two classes, bulk effect and junction (or interface) effect devices. The former are related to the properties of the homogeneous semiconductor, and the latter can be divided in two groups depending on the number of junctions in the device. A single junction device consists of a two layer structure such as the p-n diode, Schottky diode, tunnel diode etc. and a multiple junction device comprises at least a three layer structure such as metal insulator semiconductor diode, junction transistor, p-n-p-n diode etc. This thesis is concerned with a multiple junction device with a four layer structure part of which is a metal insulator semiconductor diode.

1.2 THE MISS STRUCTURE

1.2.1 Review of MISS Characteristics

The Metal-Insulator(tunnel)-n-p^+ structure has long been known as a switching device, called a **M**etal-**I**nsulator-**S**emiconductor-**S**witch (MISS). Some investigators have called it a **C**ontrolled **I**nversion **D**evice (CID), because its operation is governed by the formation of an inversion layer at the insulator-semiconductor interface. These devices have three regions in their current-voltage characteristics, a high impedance

(OFF state)†, a negative resistance region and low impedance (ON state)‡ as shown in figure 1.1. The current and voltage at which the device begins to switch from the high resistance state to the low resistance state are called the switching current (I_s) and switching voltage (V_s). The minimum current to sustain the device in the low impedance state is called the holding current (I_h), and the voltage at this point is called the holding voltage (V_h).

The negative resistance region is generally regarded as an unstable region in which there is no operating point that is stable with time. This characteristic is similar to that of the p-n-p-n Shockley diode or thyristor, but the physics of the operation is quite different. The MISS device also has a higher switching speed compared to the p-n-p-n diode, and switching times of less than 10ns have been reported [1,4]. The fabrication technology of these two devices is also very different, and MISS devices have better compatibility with standard IC fabrication.

These features have given rise to potential applications of the MISS as an integrated circuit component, such as a memory cell [2,8], a shift register cell [4], a comparator, monostable or astable multivibrator [10]. The device has also been found to be sensitive to light, and hence it can be used as an optical switch [4] in digital optical communication systems. The switching of the MISS device with palladium as the metal electrode has been found to be sensitive to hydrogen, so that can be used in an alarm system for hydrogen leakage [13].

1.2.2 Device Structure and Material

The basic structure of the MISS device is shown in figure 1.2(a) , and the symbol which is normaly used for the device is in figure 1.2(b). The device consists of an MIS

† A resistance of the order of $500k\Omega - 10M\Omega$

‡ A resistance of the order of $10\Omega - 500\Omega$

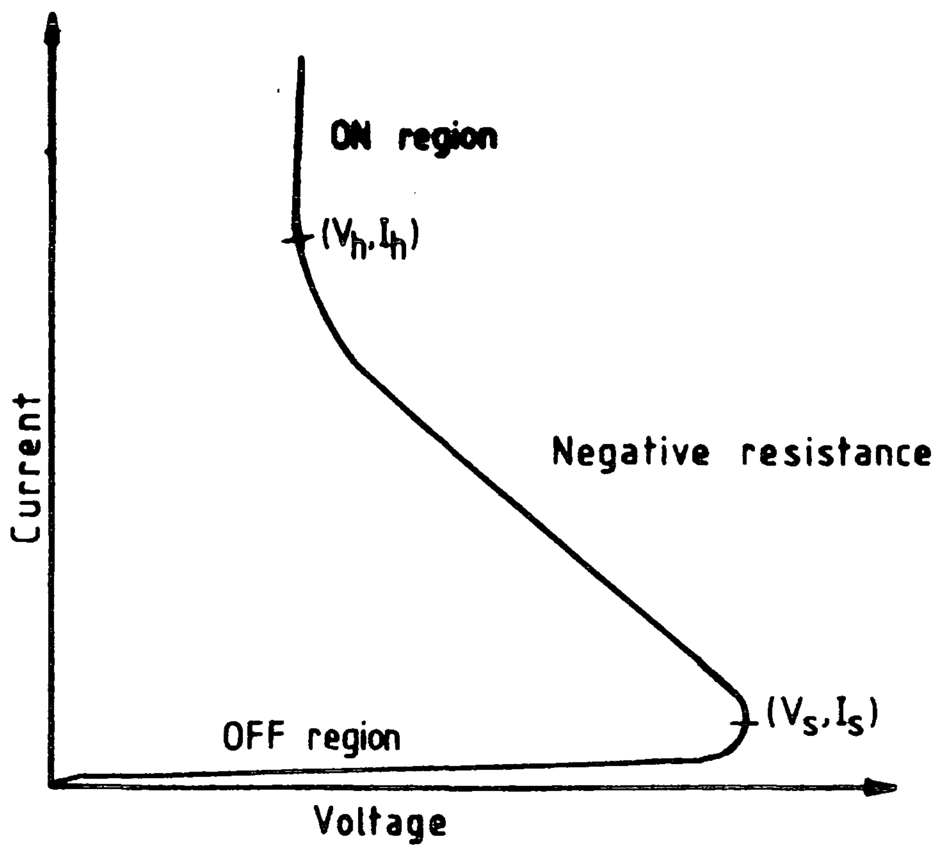

Figure 1.1 Current-voltage characteristics of MISS device.

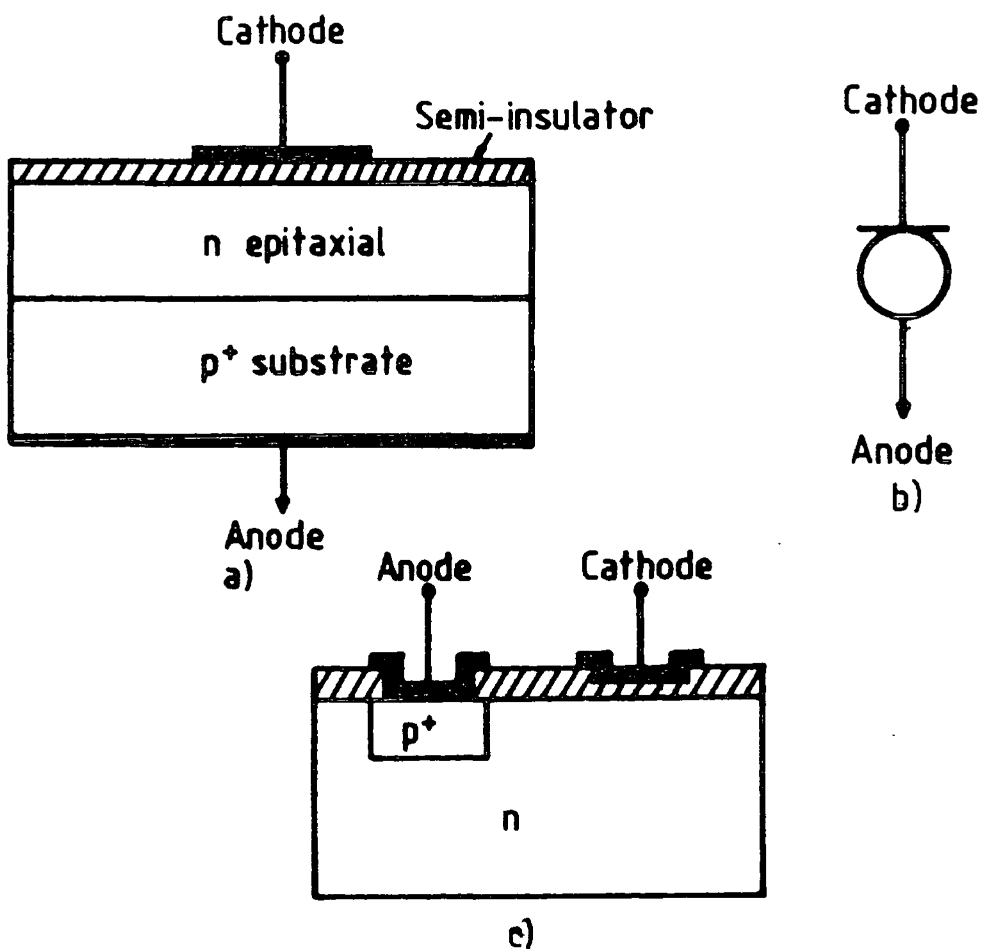

Figure 1.2 a) Basic structure of MISS device.

b) Symbol for MISS device. c) Lateral MISS device

tunnel diode backed by a p-n junction. The p-n junction can be either n-p^+ or p-n^+, where the n or p layer is often an epitaxial film. A MISS device can also be made in a lateral form as shown in figure 1.2(c) [16,17]. Most of the research on MISS devices has been based on silicon as the semiconductor. However switching has also been reported for a GaAs MISS [4,12]. Metals such as aluminium, gold and molybdenum [1,4] may be used as the top electrode.

In most of the previous research that has been done, a thin silicon dioxide film (thickness $< 50\AA$) has been used as a tunnel insulator in the MISS device [1-5,8,11,13]. The conduction of the semi-insulating film has been found to have a considerable effect on the electrical characteristics of the MISS. The conduction of the layer can be controlled by changing the thickness, as is the case for silicon dioxide, or the material. However it is very difficult to control the thickness of silicon oxide, typically a few tens of Ångström sufficiently accurately. Hence, thicker and less insulating materials become of interest. Semi-insulating materials like silicon nitride [5,6], silicon-rich-silicon- nitride, and polycrystalline silicon ($1000 - 2000\AA$) [7,10,11] and organic films deposited by the Langmuir-Blodgett technique [12], have been found to give similar switching characteristics in MISS devices. For the present study silicon-rich silicon oxide (SRO) was used as the semi-insulator.

Instead of a p-n junction, a Schottky barrier can be used as a minority carrier injector in the four-layer structure, and this gives rise to a new form of device called MISM for Metal - Insulator - Semiconductor - Metal [9,10,11]. As an extention to this idea, a second MIS diode has also been used as an injector to form a bidirectional switching device, MISIM [14,15]. The switching voltage V_s of any of these devices can be controlled by a third terminal. For the MISS, injecting or extracting current through the third terminal controls V_s, and the device structure is then called a Metal - Insulator - Semiconductor - Thyristor (MIST). However the difference compared

with a thyristor is that the switching voltage of the MIST can be increased above, or reduced below the intrinsic switching voltage, depending upon the polarity of the gate voltage.

1.3 OBJECTIVE AND THESIS OUTLINE

The objective of this thesis is to study experimentally the electrical characteristics of MISS devices made with SRO as the semi-insulating layer. At the begining of the research SRO had not been used previously in MISS devices but very recently a paper on this has been published [19]. Ever since tunnel oxide MISS device was discovered in 1972 by Yamamoto and Morimoto, almost all the experimental and theoretical investigations by other workers have concentrated on the switching characteristics of the device [2-15], and only very little has been reported [11] about its electrical behaviour in the negative resistance region. In this work we are concerned particularly with the negative resistance region.

The overall work presented in this thesis is deliberately wide and exploratory rather than analytical. This is because it is necessary in investigating a new device to find out first which characteristics are likely to be of use in electronic circuits and to concentrate later on the detailed modelling of the most important ones. Therefore all the electrical characteristics of the MISS with two and three terminals were studied. In Chapter 2 the fundamental device theories which are related to the operation of MISS devices are reviewed. The physical operation of the MISS itself is discussed in detail in Chapter 3. The device fabrication and measurement techniques used in the present work are presented in Chapter 4. The magnitude of the negative resistance of the device is strongly related to V_s, V_h, I_s, andI_h, and experimental results on these switching parameters are presented in Chapter 5. This chapter also contains the experimental results for geometrical effects in the device, and for the effect of

SRO type, gold doping, etc. The dynamic behaviour of the MISS is also studied. In Chapter 6 the switching and transistor characteristics of three terminal MISS devices are presented. A new phenomenon is also reported in this chapter.

A negative capacitance in the MISS device has been reported by Millan et al. [18]. The total capacitance was found to decrease sharply and reach a negative value as the dc bias increases in the high impedance state, the capacitance becoming negative before the switching process takes place. They explained this behaviour as due to the interaction of the carriers with the interface states at the insulator-semiconductor interface and the influence of the electric field on the tunnelling emission rate of these states. In the present work an entirely different type of negative capacitance has been discovered. To the best of our knowledge, the capacitance in the negative resistance region has never been measured previously probably because of circuit instability when one tries to bias the device in this region. In Chapter 7 the stability condition of a circuit containing a negative differential resistance is discussed, and we also present experimental evidence to show that the device does indeed have a negative capacitance as a consequence of its stable S-type negative differential resistance. Later in this chapter we demonstrate how such a negative capacitance device can be used in electronics. It appears to have many potential applications in a digital integrated circuits.

Finally in Chapter 8 we conclude the thesis with a summary of the experimental results and make suggestions for future work in this field with emphasis on the negative capacitance and its application.

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CHAPTER TWO

THEORETICAL CONCEPTS FOR MISS DEVICES

2.1 INTRODUCTION

Although this thesis is largely concerned with the experimental electrical characteristics of MISS devices, it is essential to understand the background physics which is of relevance to the device operation in order to explain the results. The MIS and p-n junction diodes are the two components which are inherent in the operation of the MISS device. This chapter is therefore devoted to a review of the device physics of the MIS structure and of the p-n junction.

2.2 THE MIS DIODE

2.2.1 The Ideal MIS Diode

The Metal-Insulator-Semiconductor (MIS) structure was first proposed by Moll in 1959 as a variable capacitor [1], but it is now a fundamental element in microelectronic devices such as the MOS transistor, and the charge-coupled device (CCD). This structure is also used as a tool to study the properties of insulating films. MIS systems with an oxide insulator can be classified into three different types depending upon the thickness of the insulator layer. 1) If the insulator thickness large ($d > 50Å$) the system behaves purely as an MIS capacitor. 2) If the insulator thickness is very low ($d < 10Å$), the system behaves as a Schottky diode. 3) For intermediate insulator thickness ($10Å < d < 50Å$) this structure is called an MIS tunnel diode and it

behaves like a leaky capacitor. For other semi-insulating materials the conductivity of the film must also be taken into consideration.

The electronic mechanism of an MIS system can best be explained by using energy band-diagrams. Depending on the applied voltage between the metal and the semiconductor, the energy bands take on one of three different conditions: accumulation, depletion, and inversion. For simplicity we will first consider the ideal MIS system with an n-type semiconductor.

At zero applied voltage, the energy band structure is shown in figure 2.1(a). The work function difference between the metal and the semiconductor is given as,

$$\phi_{ms} = \phi_m - \phi_s = 0 \qquad 2.1$$

$$\phi_{ms} = \phi_m - (\chi + \frac{E_g}{2} - q\psi_b) = 0 \qquad 2.2$$

where

ϕ_{ms} = work function difference in eV

ϕ_s = semiconductor work function in eV

χ = semiconductor electron affinity in eV

E_g = semiconductor bandgap energy in eV

ψ_b = potential difference between the Fermi level and the intrinsic Fermi level $\frac{E_F - E_i}{q}$

Since we assume that the system is ideal, the metal work function, ϕ_m, and the semiconductor work function, ϕ_s, are equal, and the metal- semiconductor work function difference, $\phi_{ms} = 0$. At zero applied voltage the energy bands are therefore flat, and as a result, the dc current through the structure is zero. Under this condition, the flat band voltage, V_{FB}, is said to be zero.

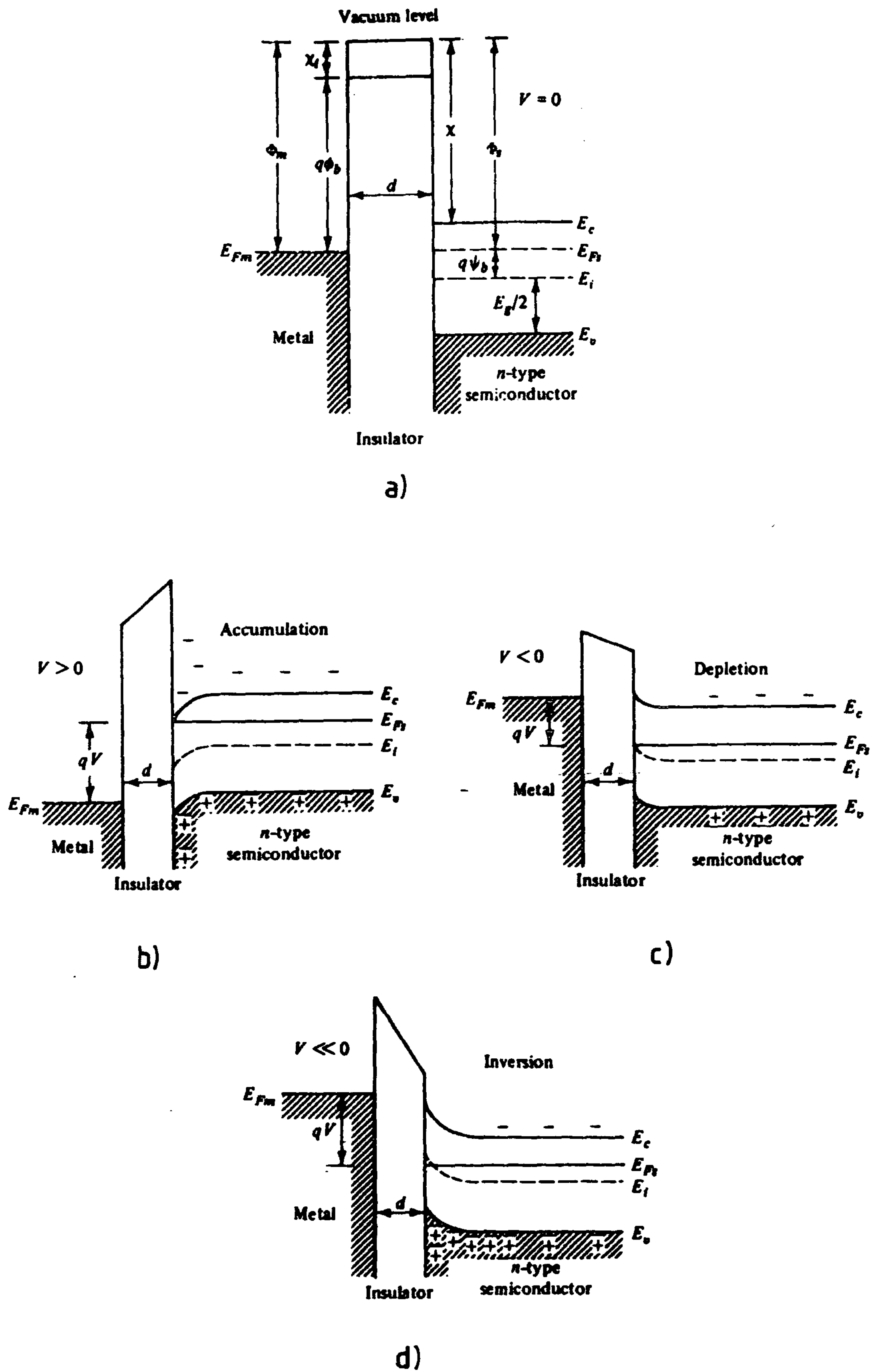


Figure 2.1 Energy band diagram of the MIS, **a)** at zero bias, **b)** forward bias, **c)** reverse bias (depletion), **d)** reverse bias inversion.

Under steady-state bias, the MIS system is considered to be in equlibrium and the applied potential is dropped partly across the insulator and partly in the semiconductor. The concentration of both electrons and holes in the semiconductor can be expressed as a function of electrical potential, $\psi(x)$, which is taken to be zero in the bulk. For an n-type semiconductor the electron and hole concentrations are therefore given by,

$$n_n = n_{n0}\exp\left[\frac{q\psi(x)}{kT}\right] \quad \text{and} \quad p_n = p_{n0}\exp\left[\frac{-q\psi(x)}{kT}\right] \qquad 2.3$$

where n_{n0} and p_{n0} are the equlibrium bulk concentrations of the majority and minority carriers respectively.

When a positive voltage (forward bias) is applied to the metal of the ideal MIS diode, (figure 2.1(b)), the metal Fermi level is lowered with respect to the semiconductor, and the energy bands at the surface of the semiconductor bend downwards. The band bending causes an accumulation of majority carriers (electrons) near the semiconductor surface, and this condition is known as *accumulation.*

When a small negative (reverse bias) is applied, as shown in figure 2.1(c), the negative charge on the metal repels the negative charges (electrons) in the semiconductor. As a result the semiconductor bands bend upwards and a region depleted of majority carriers is formed between the semiconductor surface and the bulk. The potential at the semiconductor-insulator interface relative to the bulk is known as the surface potential, ψ_s, and, it can be expressed in terms of the depletion width, X_d, by [4],

$$\psi_s = \frac{qN_dX_d^2}{2\epsilon_s} \qquad 2.4$$

where ϵ_s and N_d are the semiconductor permittivity and donor concentration per cm^3 respectively.

If the negative voltage applied to the metal of the MIS diode is increased, the band bends even further upwards as shown in figure 2.1(d) where the intrinsic Fermi level E_i crosses the Fermi level E_F at the surface. As a result, the concentration of minority carriers(holes) at the surface becomes greater than that of the majority carriers(electrons), and this situation is known as *inversion*. The MIS is said to be in *strong inversion*, if the intrinsic Fermi level E_i at the surface is above E_F by an amount ψ_b, where ψ_b is the potential between the Fermi level and the intrinsic Fermi level in the bulk. The condition for strong inversion can be expressed as,

$$\psi_s(\text{inv}) = 2\psi_b \qquad 2.5$$

which can be written as,

$$\psi_s(\text{inv}) = 2\frac{kT}{q}\ln\frac{N_d}{n_i} \qquad 2.6$$

When strong inversion occurs, the depletion layer width reaches its maximum value. A further increase in voltage in the semiconductor is prevented by the increase in the number of holes in the inversion layer. The maximum width of the depletion layer, $X_{d_{max}}$ can be derived from equation 2.4 and 2.6, and is given by,

$$X_{d_{max}} = \sqrt{\frac{4\epsilon_s kT\ln(N_d/n_i)}{q^2 N_d}} \qquad 2.7$$

Therefore, at a constant temperature the maximum depletion width decreases with an increase in the impurity concentration, N_d.

2.2.2 The Non-Ideal MIS Diode

A real MIS diode differs from the ideal in several ways. Firstly for the non- ideal MIS diode the work function difference, ϕ_{ms} is not zero and, as a results a voltage equal to $V_{FB}(= \phi_{ms})$ would have be applied to get to the flat band condition. In addition to that, the presence of fixed surface charge in the insulator also modifies the value of V_{FB}. If the fixed charge density is Q_f per unit area, then,

$$V_{FB} = -\frac{Q_f}{C_i} + \phi_{ms} \tag{2.8}$$

The magnitude of V_{FB} determines whether the surface is accumulated, depleted or inverted at zero bias. Figure 2.2 shows the energy bands of a non- ideal MIS diode in equilibrium.

A more complicated effect in a non-ideal MIS diode is due to interface states. The surface of real semiconductor always has some imperfections due to incomplete bonding (dangling bonds) and surface contamination or chemical impurities. It has been shown [6,7,8] that, the density and energy distribution of the interface states due to these imperfections are determined by the electrode metal, the crystallographic orientation of the semiconductor, thermal annealing, and the degree of oxidation. These imperfections disturb the periodicity of the crystal potential, and give rise to new states with energy levels lying within the forbidden gap of the semiconductor. Such energy states are often termed either *surface* or *interface states.* They can have a very strong influence on the electrical behaviour of a semiconductor device. The interface states also act as recombination centres, electron or hole traps, donor or acceptor centres, etc, depending on the electrical behaviour being considered.

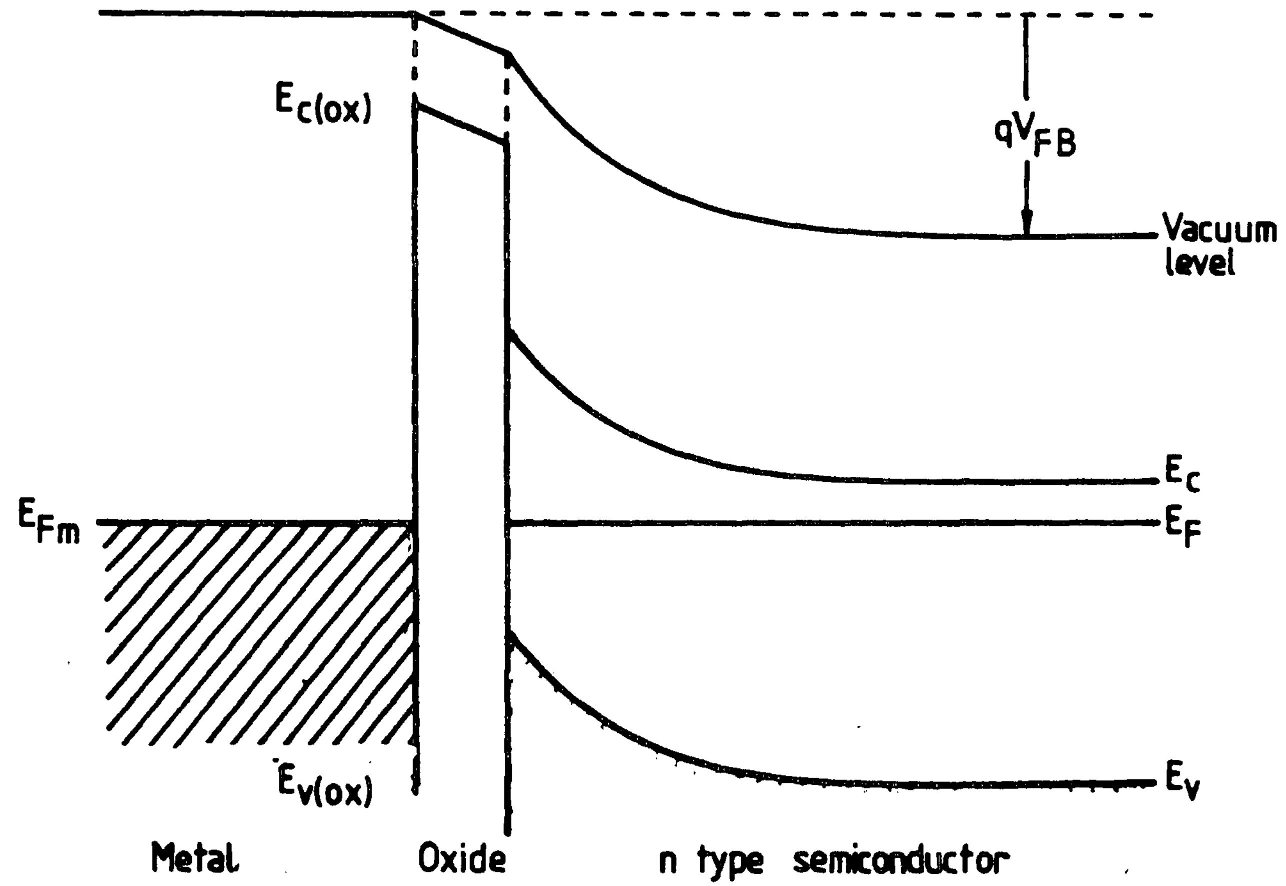


Figure 2.2 Energy band diagram of the non-ideal MIS diode at zero bias.

Interface states are considered to be donor-type when those above the Fermi level are empty (ie. positively charged) and those below the Fermi level are full with electrons (ie. neutral) as shown in figure 2.3. On the other hand, acceptor-type states are neutral when empty and negative when filled. Both of them have the ability to exchange charge with the conduction and valence bands by trapping holes or electrons. Their occupancy depends upon their position in the gap relative to the Fermi level at the surface of the semiconductor. The probability, f, of occupancy in thermal equilibrium is governed by Fermi- Dirac statistics and given by,

$$f_d(E_t) = \frac{1}{1 + g \quad \exp(\frac{E_t - E_F}{kT})} \qquad 2.9a$$

for donors, and

$$f_a(E_t) = \frac{1}{1 + g \quad \exp(\frac{E_F - E_t}{kT})} \qquad 2.9b$$

for acceptors, where g is the spin degeneration factor which is equal to 2 for acceptors and 1/2 for donors, and E_t is the interface state energy level.

Under biasing conditions, the interface states together with the conduction and valence band edges will move up or down depending on the applied voltage while the Fermi level remains constant. This results in a changing difference between E_F and E_t, and hence a change in the occupancy of the interface states. The resulting change in the interface charge affects the electrical characteristics of the MIS.

The interface states associated with the MIS system can be summarised to have the following properties;

1) They are charge storage centres, the amount of charge stored depending on the

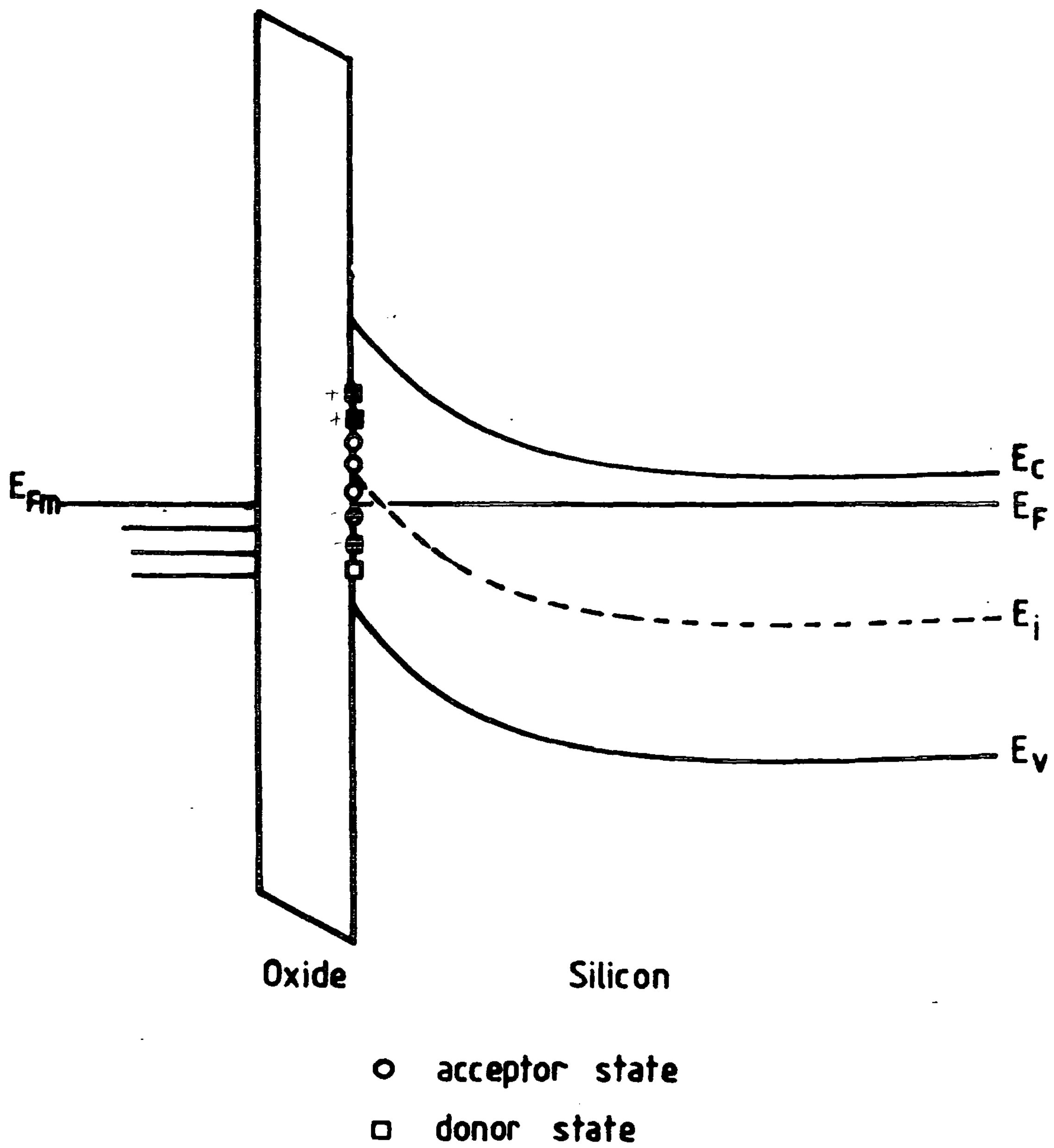


Figure 2.3 The band bending gives donor states a tendency to neutral and acceptor states a tendency to be charged negatively.

bias condition.

2) They provide a spatially concentrated region of recombination-regeneration centers.

3) They can cause additional current flow between the metal and interface states if the insulator allows charge to flow.

Including the charge in the interface states the flat-band voltage of the MIS structure becomes

$$V_{FB} = -\frac{Q_i}{C_i} + \phi_{ms}$$

where Q_i is the sum of the fixed charge Q_f and the interface charge Q_{is}. The MIS concepts described above will be applied to the MISS structure in Chapter 3.

2.3 GENERATION-RECOMBINATION IN DEPLETION LAYERS

In the MIS structure, one of the effects that can make it non-ideal is leakage current through the insulator. In this case the surface potential may be affected by the generation or recombination of carriers in the depletion layer of the semiconductor. In the bulk semiconductor there are two types of generation-recombination process, band-to-band and the Shockley-Read-Hall (SRH) mechanism. The former process is very rare in silicon and generation- recombination generally occurs through SRH centres which provide intermediate states or stepping stones in the transition of electrons and holes between conduction and valence bands. These generation-recombination centres are created by impurity atoms in the semiconductor which form deep energy levels near the midgap. In fact, silicon always has some residual impurities such as nickel, iron, manganese, zinc, and copper [9] giving recombination levels in the energy gap.

The theory of the generation-recombination mechanism has been established

by Shockley, Read and Hall, in term of four basic process involving electrons and holes being captured and emitted by a single impurity level. This process is clearly demonstrated in figure 2.4, where r_a and r_b are the rate of electron capture and emission, and r_c, r_d are the rate of hole capture and emission respectively. For simplicity we consider only the case of a single energy level E_t having a concentration $N_t f$ filled centres per unit volume and $N_t(1-f)$ unoccupied (neutral) centres, where f is the probability of the centre being occupied by an electron . In equlibrium, where there is no external generation mechanism, the rates of generation and recombination are equal, thus $r_a = r_b$ and $r_c = r_d$, and the electron and hole emission rates are given by [10],

$$e_n = v_{th}\sigma_n n_i \exp(\frac{E_t - E_i}{kT}) \qquad 2.10a$$

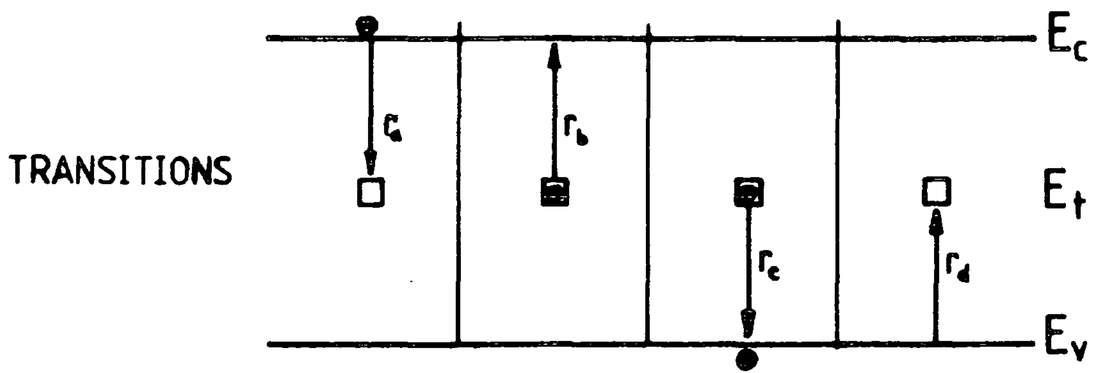
for electrons, and,

$$e_p = v_{th}\sigma_p n_i \exp(\frac{E_i - E_t}{kT}) \qquad 2.10b$$

for holes, where v_{th} is the thermal velocity, σ_n and σ_p are the capture cross sections of electrons and holes respectively. Note that the emission probability of electrons increases as the SRH level E_t approaches the conduction band edge, E_c, and the emission probability of holes increases as it approaches the valence band edge, E_v.

In the non-equlibrium case, where an external energy source such as light is applied uniformly to the semiconductor, the net generation-recombination rate of a single SRH centre is given by [4],

$$U = \left[\frac{\sigma_n\sigma_p v_{th}(pn - n_i^2)N_t}{\sigma_n[n + n_i\exp(\frac{E_t - E_i}{kT})] + \sigma_p[p + n_i\exp(\frac{-E_t - E_i}{kT})]}\right] \qquad 2.11$$



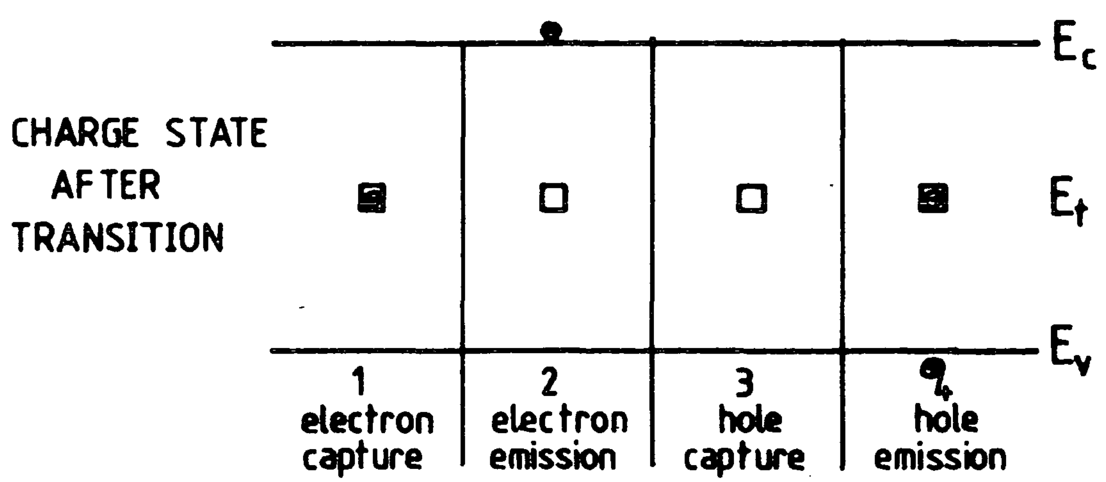


Figure 2.4 SRH generation-recombination processes.

From this equation it is clear that in either generation or recombination, the most effective centre will have E_t close to E_i. Gold has been found to give a very effective trapping centre in silicon with an acceptor level near midgap and a donor level about 0.2eV below midgap. The theory for such a two- level centre is more complicated than for a SRH centre but expressions such as equation 2.11 are still used.

In a depletion region like in reverse biased MIS diode or p-n junction, the concentration of carriers is reduced below the equlibrium concentration and $pn < n_i^2$. The depletion region therefore has net generation of carriers. The rate of generation can be obtained from equation 2.11 and is given by,

$$U = -\left[\frac{\sigma_n \sigma_p v_{th} N_t}{\sigma_n \exp(\frac{E_t - E_i}{kT}) + \sigma_p \exp(\frac{E_i - E_t}{kT})}\right] n_i$$

$$U = -\frac{n_i}{\tau_o} \qquad 2.12$$

where τ_o is the effective lifetime which is the reciprocal of the term in brackets and the negative sign implies net generation. If the SHR centre is at the middle of the bandgap ($E_t = E_i$), the effective lifetime can be simplified to

$$\tau_o = \frac{\sigma_n + \sigma_p}{\sigma_n \sigma_p v_{th} N_t}$$

2.4 THE MIS TUNNEL DIODE

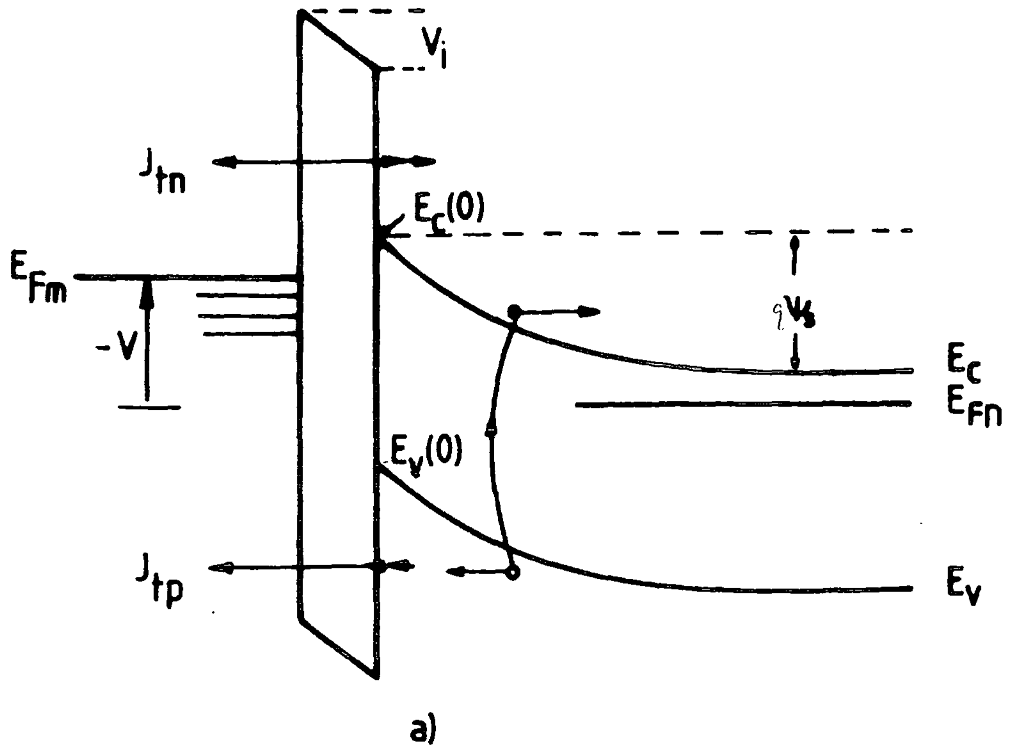
The MIS diode with a very thin insulator can pass current by quantum mechanical tunnelling through the insulator. This structure is known as an MIS tunnel diode.

2.4.1 MIS Tunnel Diode at Reverse Bias

When the MIS tunnel diode is reverse biased, the energy levels in the semiconductor are bent up as shown in figure 2.5(a), and holes (the minority carriers) tend to accumulate near the surface due to the electric field. Unlike an MIS with a thick insulator (MOS capacitor) the semiconductor will not generally go into strong inversion because the generated holes at the insulator-semiconductor interface leak away through the insulator to the metal electrode and they are unable to maintain the inversion layer at the interface. As a consequence, most of the applied voltage drops in the semiconductor and this causes the silicon surface to be driven into a steady-state deep depletion condition (i.e. $\psi_s > 2\psi_b$). This deep depletion condition is in equilibrium whereas deep depletion in an MOS capacitor never occurs in the steady state condition.

For an MIS structure containing a very thin silicon oxide insulator the electronic conduction between the metal and semiconductor is by a tunnelling mechanism. There are two main tunnel current components, the electron tunnel current, J_{tn}, from the metal to the semiconductor conduction band, and the hole tunnel current, J_{tp}, of holes tunnelling from the semiconductor valence band to the metal. The hole tunnel current is controlled by both the probability of holes penetrating the tunnel barrier presented by the insulator and the supply of holes, $p(x)$, at the insulator-semiconductor interface which is taken to be at $x = 0$. This current can be expressed as (see appendix A)[5],

$$J_{tp} = A_p T^2 e^{-\eta_p} \left\{ F_1 \left(\frac{E_v(0) - E_{Fp}(0)}{kT} \right) - F_1 \left(\frac{E_v(0) - E_{Fm}}{kT} \right) \right\} \qquad 2.12$$



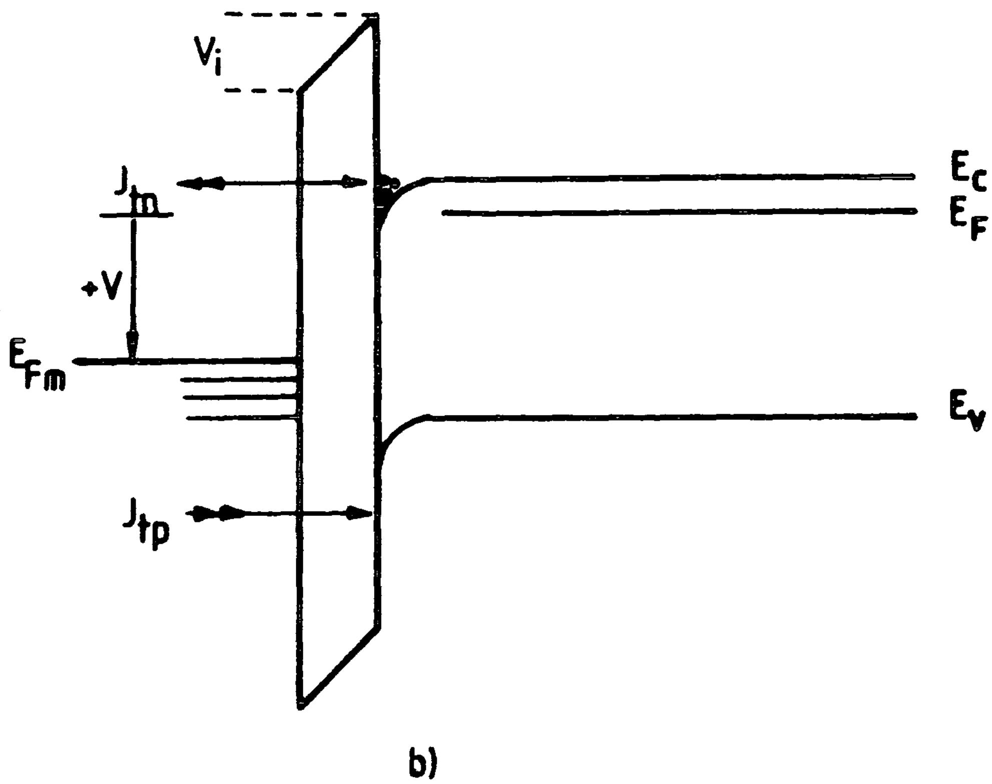


Figure 2.5 Energy band diagram of the MIS tunnel diode a) reverse biased, b) forward biased.

where

$$A_p = \text{ the effective Richardson constant for holes}$$

$$T = \text{ temperature in } {}^oK$$

$$\eta_p = \text{ the barrier tunnelling transmision coefficient}$$

$$= \chi_p^{\frac{1}{2}} d, \text{ where } \chi_p \text{ is the tunnelling barrier height for holes}$$

$$F_1 = \text{ Fermi- dirac integral of order 1}$$

$$E_{Fp}(0) = \text{ the quasi Fermi-level of holes at the interface } x = 0$$

$$E_v(0) = \text{ the energy of the valence band edge at } x = 0$$

$$E_{Fm} = \text{ the metal Fermi-level}$$

Since the MIS is reverse biased, the hole tunnel current is limited by the rate at which holes are generated in the depletion region. The generation current can be expressed as

$$J_g = \int_0^{X_d} q|U|dx = q|U|X_d \quad 2.13$$

and from 2.11 this can be written as,

$$J_g = \frac{qn_iX_d}{\tau_o} \quad 2.14$$

Under steady state conditions, the hole tunnel current is equal to the generation current ($J_{tp} = J_g$).

In a similar way, the electron tunnel current, J_{tn}, associated with electron tunnelling from the metal to the semiconductor conduction is a function of the rate of supply of electrons which are capable of tunnelling to the conduction band from within the metal (figure 2.5(a)). The current is also a function of the probability of the electrons penetrating the tunnel barrier. By analogy to equation 2.12, the electron tunnel current can be written as [5],

$$J_{tn} = A_e T^2 \epsilon^{-\eta_e} \left\{ F_1 \left(\frac{E_{Fm} - E_c(0)}{kT} \right) - F_1 \left(\frac{E_{Fn}(0) - E_c(0)}{kT} \right) \right\} \qquad 2.15$$

where $E_{Fn}(0)$ is the quasi Fermi-level of electrons at the interface and $E_c(0)$ is the energy of the conduction band edge at $x = 0$.

For a normal case where $E_{Fm} < E_c(0)$ the hole generation current, J_g, is much greater than the electron tunnel current, J_{tn}. So for this system the reverse bias current J_R is approximately equal to the generation current ($J_R = J_g$).

The total voltage across the reverse biased MIS is the voltage across the insulator plus the voltage drop in the depletion layer which is equal to the surface potential ψ_s

$$V = V_i + \psi_s \qquad 2.16$$

The voltage across the insulator is given by,

$$V_i = \frac{Q_s d}{\epsilon_i} \qquad 2.17$$

where ϵ_i is the insulator permittivity in farad/cm, Q_s is the total charge per unit area in the semiconductor and is given by

$$Q_s = \sqrt{2q\epsilon_s N_d \psi_s} \qquad 2.18$$

From equation 2.17 and 2.18, V_i can be expressed as

$$V_i = \frac{\sqrt{2q\epsilon_s N_d \psi_s}}{C_i} \qquad 2.19$$

where $C_i (= \epsilon_i / d)$ is the insulator capacitance per unit area. For the MIS tunnel oxide C_i is in the order of $10^{-6} F.cm^{-1}$, and the doping density of the semiconductor, N_d is in

the order of $10^{15} cm^{-3}$. By substituting these values in equation 2.19 it can be shown that $\psi_s \gg V_i$. Therefore for the reverse bias MIS the majority of the applied voltage drops across the deep depletion region of the semiconductor.

2.4.2 MIS Tunnel Diode at Forward Bias

When the MIS is forward biased the energy levels in the semiconductor are bent down as shown in figure 2.5(b), and excess electrons accumulate at the insulator-semiconductor interface. The electron concentration at the surface is given by equation 2.3, so that a small change in surface potential ψ_s causes a large change in the concentration of the accumulated electrons. These electrons act like a plate capacitor so that most of the applied voltage drops across the insulator ($V \simeq V_i$).

The electron tunnel current, J_{tn}, is due to the tunnelling of electrons from the semiconductor conduction band to the metal. The hole tunnel current is due to holes tunnelling from the metal to the semiconductor valence band and is a function of the supply of holes and the probability of them penetrating the tunnel barrier. This current is analogous to the electron tunnel current for the case of reverse bias. Thus, the electron current is much greater than hole current and it is the dominant component in the forward bias current of the MIS.

The forward current, depending on the concentration of electrons in the accumulated surface will rise rapidly with voltage. The reverse current is however limited by generation in the depletion layer so that it will become almost constant with voltage. The overall current-voltage characteristic of the MIS tunnel diode has been considered by Simmons and Taylor [12] and it is as illustrated in figure 2.6. This characteristic looks very similar that of a p-n junction.

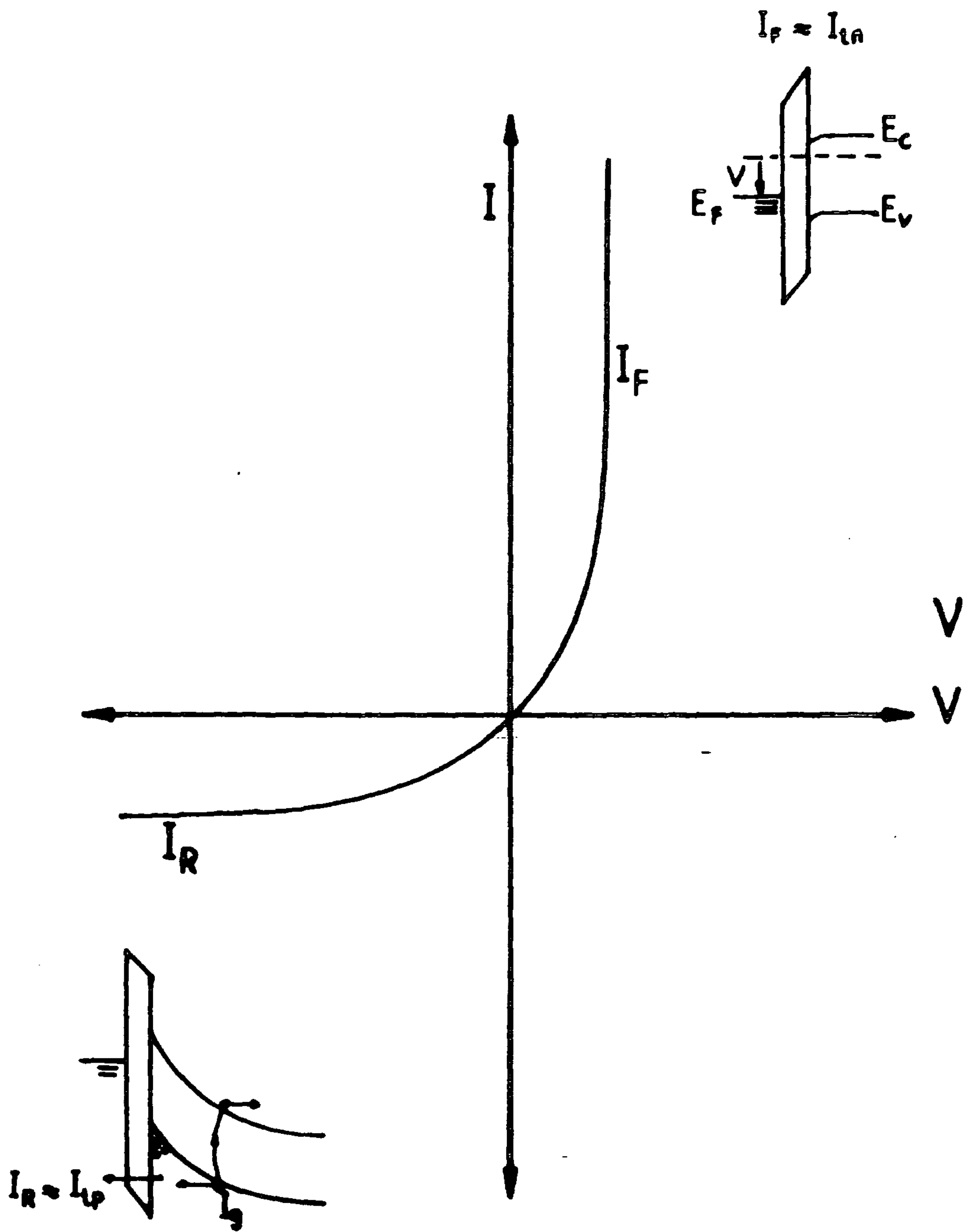


Figure 2.6 Typical current-voltage characteristic of the MIS tunnel diode.

2.4.3 Current Multiplication in Reverse Bias

For the MIS in the reverse biased condition, the tunnel current is limited by the rate at which holes are generated in the depletion region. If additional holes are supplied to the surface of the semiconductor by external processes such as illumination with light or by injection from a third terminal they cannot be lost by increased tunnelling so that their concentration increases and the semiconductor surface becomes inverted. When the surface is in strong inversion, the field at the semiconductor surface increases, and this increases the electric field in the insulator and hence the voltage drop across it. This causes the difference between the metal Fermi-level and the conduction band edge, $(E_{Fm} - E_c(0))$, to decrease, and this increases the number of electrons in the metal which are capable of tunnelling from metal to the semiconductor conduction band. This will greatly increase the electron tunnel current and this phenomenon is referred to as current multiplication [2,13]. This not be confused with current multiplication due to impact ionisation.

The multiplication factor, M, due to this effect can be defined as the ratio of the majority carrier to the minority carrier current or,

$$M = \frac{J_{tn}}{J_{tp}} \qquad 2.20$$

The magnitude of the current multiplication in the n-type MIS tunnel diode is dependent on the metal work function, insulator thickness, doping concentration, N_d, temperature and the injected current [2,13]. At the same insulator thickness, the current multiplication, M, increases with decreasing metal work function. The effect of insulator thickness, d, on M has been further investigated by C. W. Jen et al. [2], who showed that a thicker insulator led to a larger multiplication.

2.5 P-N JUNCTION DIODE

2.5.1 Current-Voltage Equation

There are two major mechanisms which contribute to the current in a forward biased p-n junction; 1) injection current, and 2) space charge recombination current. For a first-order diode model the latter is ignored, and the analysis assumes that the injection of minority carriers is low. In a forward biased p- n junction, holes are injected from the the p-side over the potential barrier into the n-side where as minority carriers they diffuse away from the junction. Eventually they recombine with majority carriers in the n-side or move to the end contact by diffusion. For a long p type substrate, the hole diffusion current density is given by the Shockley equation [11],

$$J_{dp} = \frac{qD_p p_{no}}{L_p}\left\{\exp(\frac{qV_j}{kT}) - 1\right\} \qquad 2.21$$

Similarly the injection of electrons from the n-side to the p-side gives an electron diffusion current density

$$J_{dn} = \frac{qD_n n_{po}}{L_n}\left\{\exp(\frac{qV_j}{kT}) - 1\right\} \qquad 2.22$$

where D_n and D_p are the diffusion constants of electrons and holes, n_{po} and p_{no} are the equilibrium minority carrier concentrations in the p-side and the n-side respectively, L_p and L_n are the diffusion lengths for holes and electrons, V_j is a voltage across the junction. The total current density for an ideal p-n diode is the sum of the hole and electron diffusion currents

$$J = J_{dp} + J_{dn} = J_s \left\{ \exp(\frac{qV_j}{kT}) - 1 \right\} \tag{2.23}$$

where

$$J_s = \frac{qD_p p_{no}}{L_p} + \frac{qD_n n_{no}}{L_n} \tag{2.24}$$

The second component of the current is due to recombination of carriers in the space charge region resulting in an increase in the total current through the device. This current was first explained by Sah et al. [3] by assuming that (i) the doping levels were **similar** on opposite sides of the junction, (ii) only single level recombination centres located in the middle of the bandgap are important, and (iii) the recombination rate is approximately constant within the space charge region. The expression for the recombination current density can then be simplified to [4],

$$J_{rj} = \frac{qn_i W_j}{2\tau_o} \exp(\frac{qV_j}{2kT}) \tag{2.25}$$

where τ_o is the effective carrier lifetime and W_j is the junction width which is given by

$$W_j = \sqrt{\frac{2\epsilon_s}{q}(\frac{N_d + N_a}{N_a N_d})(V_{bi} - V_j)} \tag{2.26}$$

where ϵ_s is the semiconductor permitivity, N_d is a donor concentration, and V_{bi} is the built-in voltage given by,

$$V_{bi} = \frac{kT}{q} \ln(\frac{N_d N_a}{n_i^2}) \tag{2.27}$$

For the p$^+$-n junction of interest in this thesis $N_a \gg N_d$ and

$$W_j \approx \sqrt{\frac{2\epsilon_s}{qN_d}(V_{bi} - V_j)} \qquad 2.28$$

2.5.2 P-N Junction Ratio β_p for Holes.

The capability of the junction to inject holes or electrons is called the *injection efficiency,* γ. The injection efficiency for holes γ_p is defined as,

$$\gamma_p = \frac{\text{hole current}}{\text{total current}}$$

i.e.

$$\gamma_p = \frac{J_{dp}}{J_{dp} + J_{dn} + J_{rj}} \qquad 2.29(a)$$

The injection efficiency for electrons,γ_n, is

$$\gamma_n = \frac{\text{electron current}}{\text{total current}}$$

$$\gamma_n = \frac{J_{dn}}{J_{dp} + J_{dn} + J_{rj}} \qquad 2.29(b)$$

The ratio of the hole to electron injection efficiency is called p-n junction ratio, β_p, for holes

$$\beta_p = \frac{\gamma_p}{\gamma_n} = \frac{J_{dp}}{J_{dn}} \qquad 2.30$$

For a wider p section of the p-n junction

$$\beta_p = \frac{D_p N_a L_n}{D_n N_d L_p} \qquad 2.31$$

As we can see that the junction ratio for holes increases if the p-substrate has a higher doping density. This is a very important parameter in MISS devices where high hole injection is needed.

2.5.3 Practical PN Junctions

For practical p-n junction diodes, the current expressions discussed earlier would not be seen experimentally. In a practical model of a p-n junction diode, apart from recombination-generation current, the effects of two external resistances in the form of a series resistance r_s and a shunt resistance r_{sh} must be included. The series resistance r_s represents the bulk resistance of the p, and n regions outside the transistion region, and the resistance of the ohmic contacts. The resistance r_{sh} arises from the leakage current at the edge of the junction. In the case of a good diode this resistance is very large and its effects are negligible.

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CHAPTER THREE

PRINCIPLE OF OPERATION OF MISS DEVICES

3.1 INTRODUCTION

As has been mentioned MISS devices have three regions in their I-V characteristics, a high impedance region which is between zero voltage and the switching point, a negative resistance region, and a low impedance state. A great deal of work has been done to establish the theory of operation of the MISS most of which has been based on the tunnel oxide device. Yamamoto and Morimoto [1] postulated that an inversion layer formed at the insulator-semiconductor interface causing an increase in the tunnelling current so turning the device ON. Kroger and Wegener [2] quite properly recognised that the high impedance state was due to deep depletion in the semiconductor. Five years later the first quantitative model was proposed by Simmons and El-Badry [3,4] in which they assumed that punch-through or avalanching in the semiconductor was responsible for the switching process. For a lightly doped epilayer ($< 10^{15}cm^{-3}$) the switching action was thought to be controlled by punch- through and for a heavily doped layer ($> 10^{17}cm^{-3}$) it was due to avalanche breakdown.

Habib and Simmons [5] put forward a theory, which appears to be very convincing, in which where the switching mechanism is based on a positive feedback interaction between the p-n junction and the MIS tunnel diode. Sarrabayrouse et al. [6,7] extended the regenerative feedback model and obtained agreement between their calculated variation of switching voltage with illumination and temperature and the experimental evidence. Adán and Zólomy [8] proposed a thyristor like model where positive feedback is normaly used, the MISS being regarded as being composed of two

amplification devices. The first element was a bipolar transistor with p^+ substrate as emitter, the neutral region of the epitaxial layer as base and the semiconductor–semi–insulator interface as collector. The MIS section was treated as the second amplification device.

The regenerative positive feedback model had been used by many workers in the field as the general switching mechanism for the MISS [3–8]. Board [10] seems to suggest that this mechanism is responsible for any type of device which exhibits current-controlled negative resistance, although the physics of the operations of MISM, MISIM and thyristor devices may be quite different. According to the positive feedback model, before switching takes place the total loop gain, G, of the system is less than one, at the switching and holding points it is equal to 1, and in the negative resistance region G is greater than 1. The stability condition of the feedback loop is $G \leq 1$ and the instability condition is $G > 1$. A stable steady state negative resistance which has been found in earlier work in this department and is now the main interest of the present work, disproves the validity of this model. However, it is generally accepted that a feedback model still applies to the MISS under certain external conditions which will be discussed in Chapter 7.

Although this thesis is concerned with MISS devices made with SRO as a semi-insulating material with a different conduction mechanism compared to that of tunnel-oxide, the basic switching process appears to be the same for all types of MISS. Therefore in this chapter we will first consider the principle of operation of one-dimensional MISS devices based on a tunnelling mechanism in the semi-insulator. Later in the chapter the SRO conduction mechanism will be briefly reviewed, followed by speculation about the electronic mechanism which leads to switching in the SRO-MISS device. Experimentally, the device characteristics are found to depend on area and the reasons for this will be described in Chapter 5.

The terms forward and reverse bias as used for the MISS are different from

those for MIS. In this thesis we define forward bias for the switching direction or in other words the voltage to enable a large amount of current to flow, biasing the MIS section into what would normally called reverse bias. Reverse bias for the MISS is the non-switching direction where only a small amount of current can flow through the MIS section would normally be said to be forward biased. The forward and reverse bias conditions for the MISS are the opposite of those the MIS as illustrated in figure 3.1.

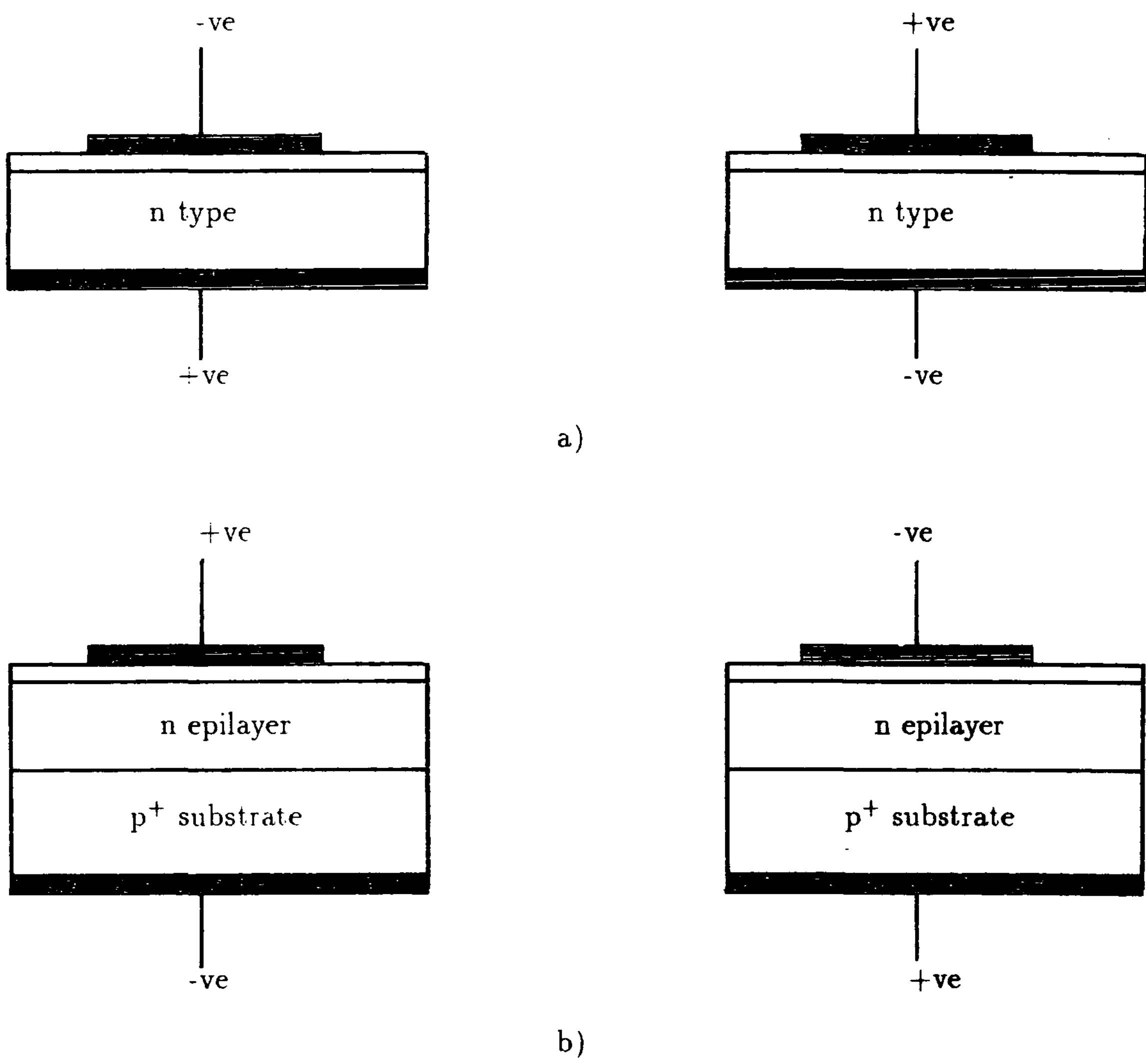


Figure 3.1 a) MIS in reverse and forward bias, **b)** MISS in reverse and forward bias.

3.2 OPERATION WITH REVERSE BIAS

The energy band structure of an idealised MISS device under zero bias condition and thermal equlibrium is shown as in figure 3.2. If a positive voltage is applied to the metal with respect to the substrate the MIS section with its leaky insulator is forward biased while the p^+-n junction is reverse biased as shown in figure 3.3. As discussed in Chapter 2, the MIS tunnel diode behaves as a rectifier, so that if forward biased it can pass a relatively large current resulting in a small voltage drop. As a consequence, most of the applied voltage is droped across the depletion region of the reverse bias p-n junction. The I-V characteristic in this condition is therefore dominated by the reverse biased p-n junction and the current is limited by generation, predominantly in the depletion region. The reverse bias current of the device can therefore be written approximately as

$$J_g = \frac{n_i}{\tau_o} W_j (V_{bi} + V_j)^{1/2}$$

$$= \frac{n_i}{\tau_o} \left(\frac{q\epsilon_s}{2N_d} \right)^{1/2} (V_{bi} + V - V_i)^{1/2} \qquad 3.1$$

where $V(= V_i + V_j)$, is the voltage across the device, V_{bi} is the p-n junction built-in voltage, and V_i is the voltage drops across the semi- insulator. If the semi-insulator is leaky, the voltage drop in it can be ignored ($V_i \simeq 0$), and, the reverse bias current may be written as,

$$J_R \approx \frac{n_i}{\tau_o} \left(\frac{q\epsilon_s}{2N_d} \right)^{1/2} (V + V_{bi})^{1/2} \qquad 3.2$$

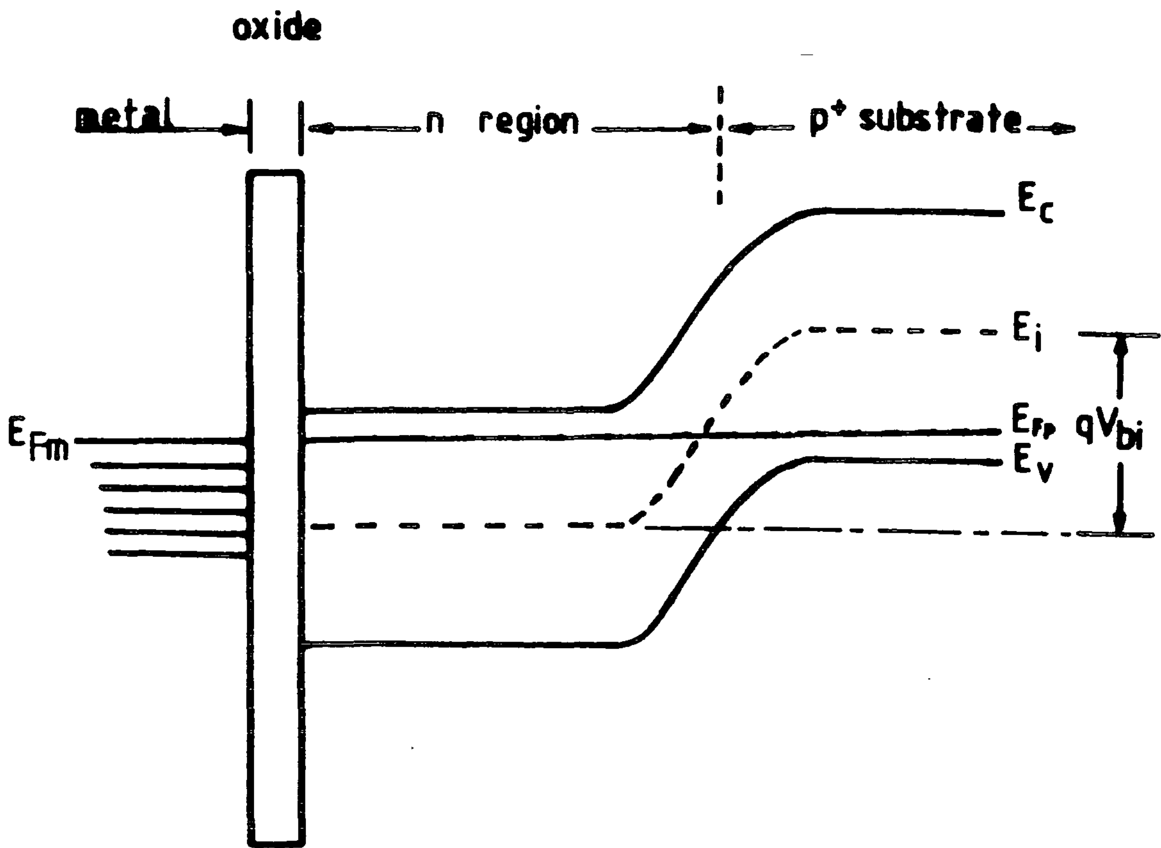


Figure 3.2 Energy diagram of the MISS at zero bias.

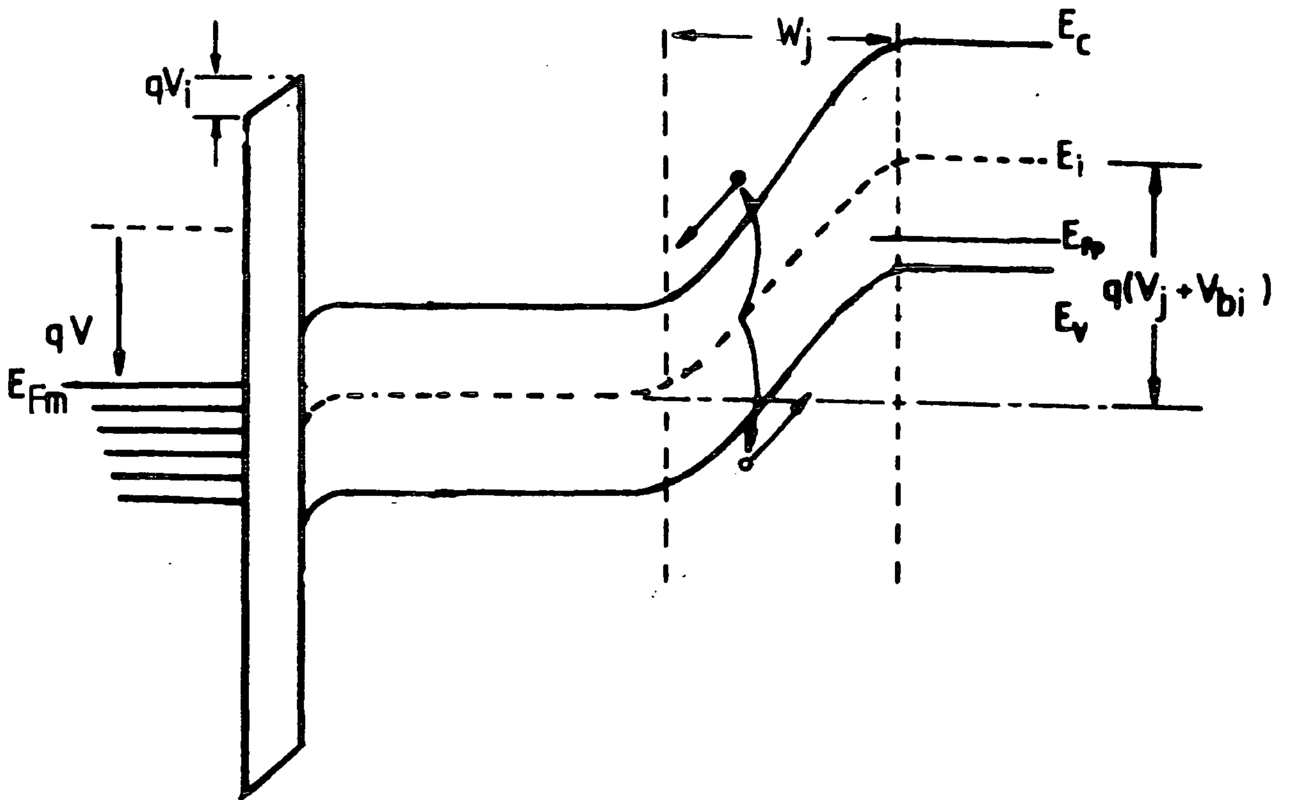


Figure 3.3 Energy diagram of the MISS at reverse bias.

The reverse current of the MISS therefore increases slowly with voltage until the onset of avalanche breakdown.

3.3 OPERATION WITH FORWARD BIAS

3.3.1 High Impedance State

If the voltage on the metal increases negatively with respect to the substrate, the MIS section is reverse biased and the p^+-n junction is forward biased. As a result, an interfacial depletion region grows in the n type epitaxial layer under the metal electrode. This will cause a net generation of electron-hole pairs within the depletion region, the electrons being swept out through the p-n junction and the holes being swept to the insulator semiconductor (I-S) interface. If the insulator is thick enough and highly insulating the generated holes will accumulate at the I-S interface causing the surface of the n type layer under the insulator to invert. However, since the insulator is leaky in the MISS some of the holes tunnel through the insulator to the metal electrode. Thus as the voltage increases the n-layer becomes more depleted rather than inverted as illustrated in figure 3.4(a). Under this condition, the generated current is given by the same type of expression (equation 3.2) as for the case of reverse bias except that the term $(V + V_{bi})$ is replaced by a surface potential, ψ_s, since the majority of the applied voltage drops across the depletion layer. This current is very weakly dependent on voltage and at a relatively high voltage across the device only a very small current can pass through it. This condition is recognised to be the high impedance state or high voltage low current state.

Under these circumstances the junction voltage is just sufficient to enable the generated electron current from the depleted region to flow. These electrons will

recombine with holes in the p^+-n junction and a few will diffuse through it because the junction voltage is very small. Similarly in the deep depletion condition, the voltage across the semi-insulator is just sufficient to allow the very small generated hole current to flow to the metal. The current passed through the junction is limited to the generation current in the surface depletion region which is almost independent of applied voltage, so that the total current passed through the junction remains almost constant. As a result, the voltage dropped across the junction is also constant and very small and it can be neglected compared to the total voltage across the device. It follows that the majority of the applied voltage drops across the depletion region, and is equal to the surface potential, ψ_s. For an ideal case, where the work function difference, $V_{FB} = 0$, the voltage across the MISS can be written as,

$$V = V_i + \psi_s + V_j \qquad 3.3$$

where V_i and V_j are the voltage across the semi-insulator and the p^+-n junction respectively. Since $\psi_s \gg V_i + V_j$

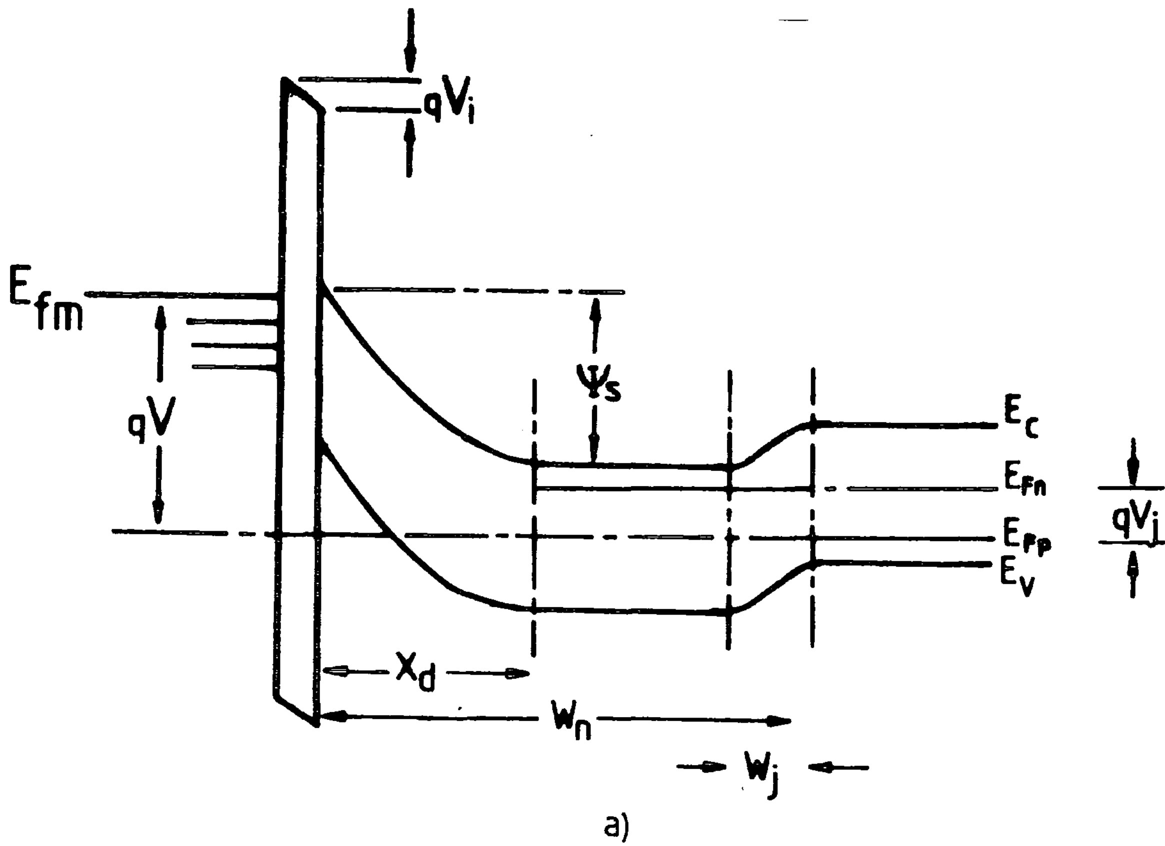
$$V \approx \psi_s \qquad 3.4$$

Therefore the initial forward bias current of the MISS, which is known as the OFF current, is the generation current and is given by,

$$J_{OFF} \simeq \frac{n_i}{\tau_o}\left(\frac{q\epsilon_s V}{2N_d}\right)^{1/2} \qquad 3.5$$

3.3.2 Switching Point in Punch-Through Mode

When the voltage across the device is increased the depleted region under the semi-insulator extends toward the p^+-n junction. When it becomes sufficiently high ($V = V_s$) the interfacial depletion region reaches the depletion region of the junction



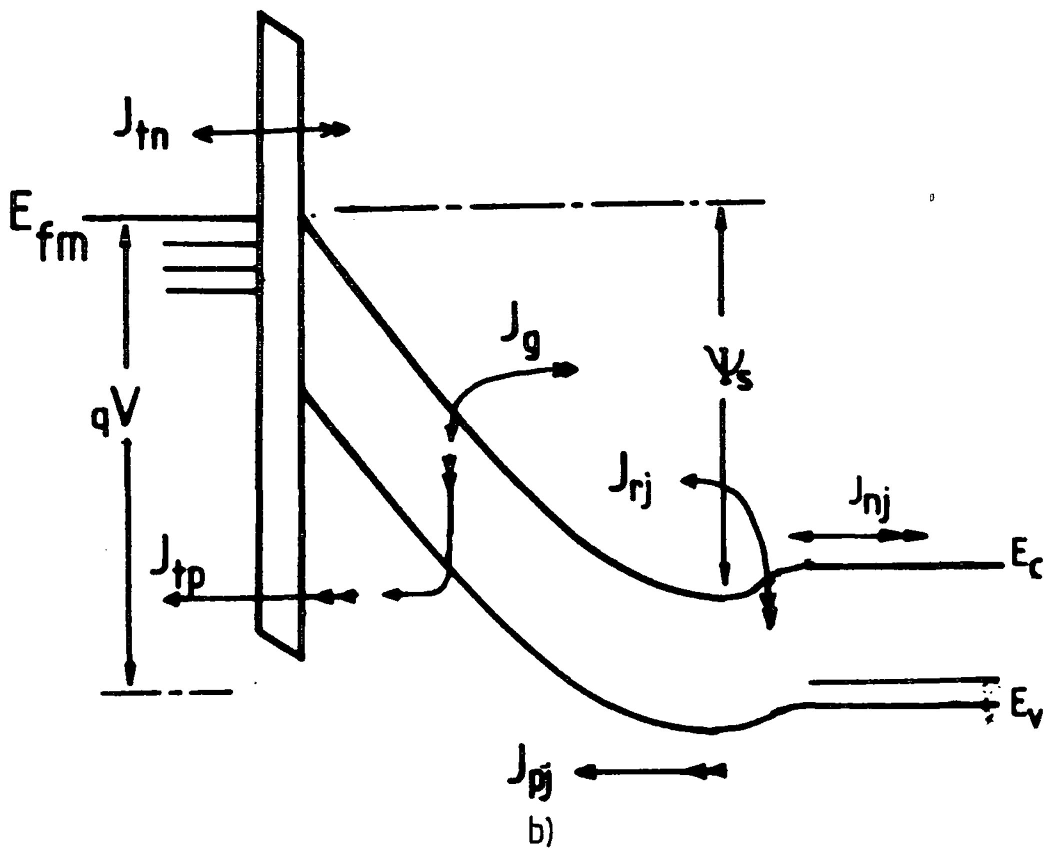
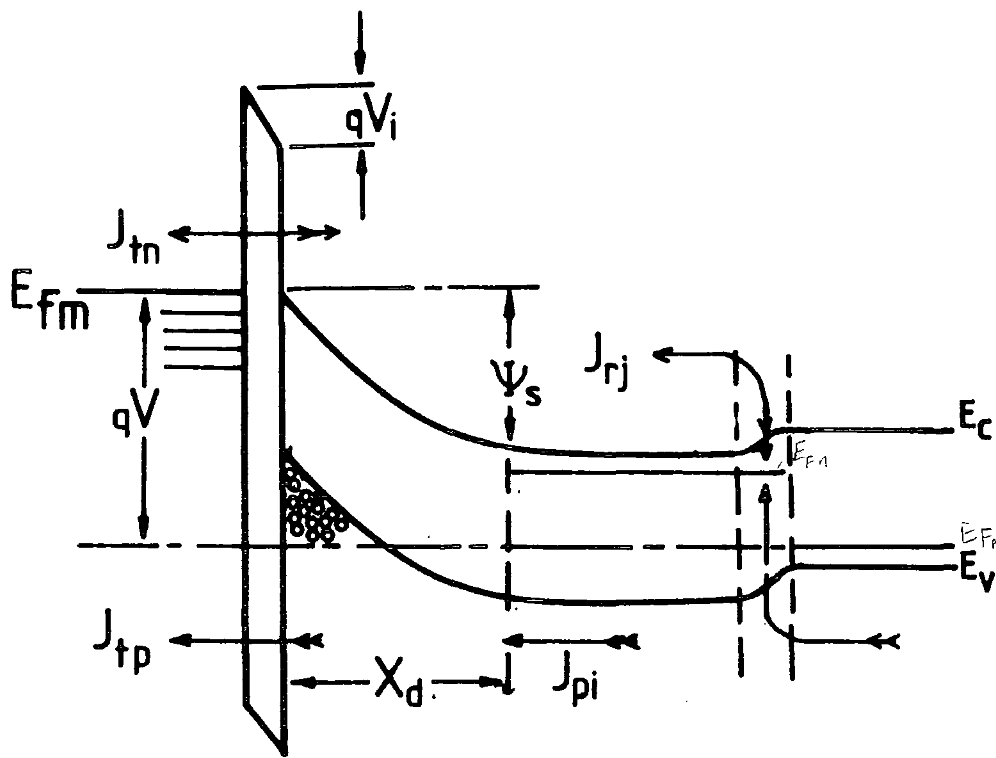


Figure 3.4 Energy band diagram of the MISS, a) in the high impedance state, b) in the punch-through regime.



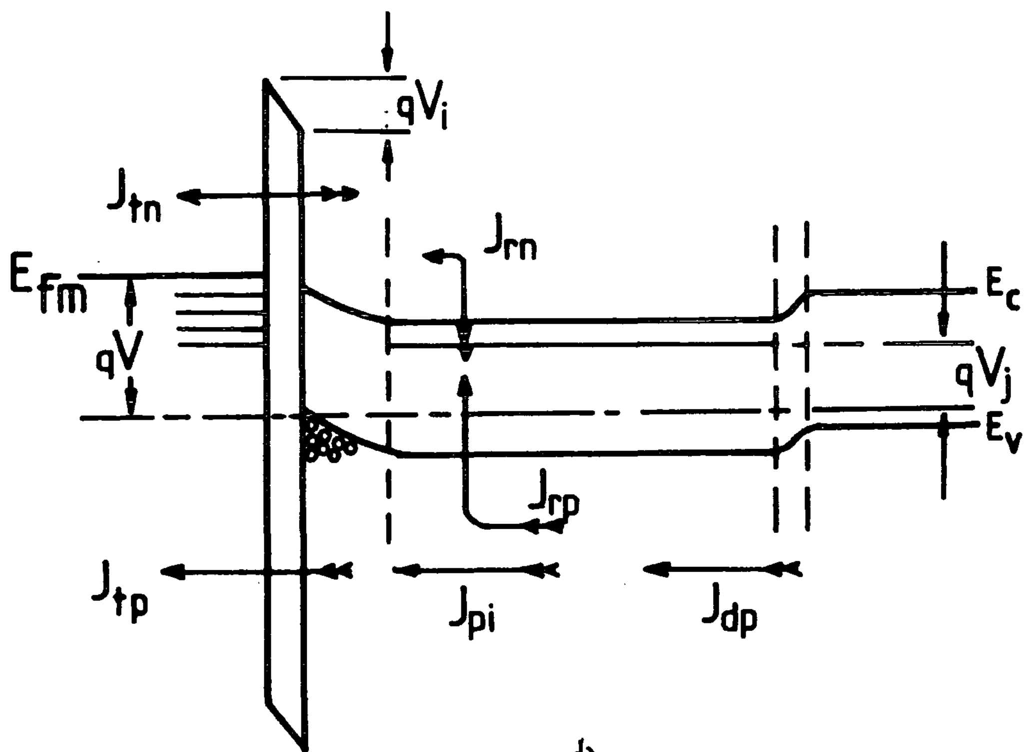


Figure 3.4 (cont.) Energy band diagram of the MISS, **c**) in the negative resistance region, **d**) in the low impedance state.

as shown in figure 3.4(b) and this phenomenon is known as punch-through. At punch-through the neutral region disappears completely so that the width of the depletion layer, X_{dp} can be written approximately as,

$$X_{dp} \simeq W_n - W_j \qquad 3.6$$

where W_n and W_j are the thicknesses of the n-type epitaxial layer and the junction depletion region respectively. Hence from equation 2.4 the surface potential at punch-through, ψ_{sp}, reachs a maximum value given by,

$$\psi_{sp} = \frac{qN_d}{2\epsilon_s}(W_n - W_j)^2 \qquad 3.7$$

Thus, the voltage across the device which is equal to the switching voltage, V_s may be written as,

$$V_s \approx \psi_{sp} = \frac{qN_d}{2\epsilon_s}(W_n - W_j)^2 \qquad 3.8$$

After punch-through has been reached a further increase in the applied voltage will appear across the junction and the semi-insulator. Since the injected hole current from the p^+-n junction depends exponentially on the junction potential ($J_{pj} \simeq J_s e^{qV_j/kT}$), a large number of holes are injected into the depletion region for a very small increment in the applied voltage. These holes travel to the semi-insulator semiconductor interface where they leak (tunnel) through the semi-insulator to the metal. When the rate at which holes reach the interface becomes greater than the rate at which ~~which~~ they can tunnel through the semi-insulator they will accumulate rapidly at the interface and the semiconductor surface will become inverted. As a consequence the potential across the depletion layer decreases and the electric field in the

semi-insulator increases allowing a larger electron tunnel current, J_{tn}, to flow from the metal into the semiconductor. Thus the p^{+}-n junction becomes more forward biased and it injects more holes into the n-type epitaxial layer.

This explains the transition to the highly conducting state in qualitative way. The process is a regenerative one and it can be simplified to

$$dJ_{pj} \rightarrow dJ_{tp} \rightarrow dJ_{tn} \rightarrow dJ_{rj} \rightarrow dJ_{pj} \qquad 3.9$$

where $J_{tn}(J_{tp})$ is the electron(hole) tunnel current, J_{pj} is the hole current from the p^{+}-n junction, and J_{rj} is the recombination current in the junction. These currents are shown in figure 3.4(b). The ratio of dJ_{tn} to dJ_{tp} is defined as the MIS gain, G_s, and the ratio of dJ_{pj} to $d(J_{rj} + J_{nj})$ is the p-n junction gain, G_j. Therefore, a total gain, $G(= G_s.G_j)$ of the current loop system can be written as,

$$G = \frac{dJ_{tn}}{dJ_{tp}} . \frac{dJ_{pj}}{d(J_{rj} + J_{nj})} \qquad 3.10$$

From the continuity of the currents

$$dJ_{tn} = dJ_{rj} - dJ_g + dJ_{nj} \qquad 3.11$$

and

$$dJ_{pj} = dJ_{tp} + dJ_g \qquad 3.12$$

where J_{nj} is the electron diffusion current of the junction. Hence

$$G = \frac{dJ_{rj} - dJ_g + dJ_{nj}}{dJ_{tp}} . \frac{dJ_{tp} + dJ_g}{d(J_{rj} + J_{nj})} \qquad 3.13$$

At the switching point, the depletion layer growth ceases, hence the rate of increase of the generation current J_g becomes zero. Hence $dJ_g = 0$ so that the total gain becomes unity, $G = 1$.

3.3.3 Switching in Avalanche Mode

The avalanche mode of switching will take place if the epitaxial layer is heavily doped. In this case the depletion layer will be thin and the electric field will be high. Extra carriers will then be produced by avalanche multiplication at a sufficiently high voltage. The magnitude of the switching voltage is then lower than the punch-through switching voltage because avalanching will occur first. The energy band structure for this case is shown in figure 3.5. When a negative voltage is applied to the metal electrode, the device first enters the high impedance state where the total current is dominated by the generation current as previously. However as the voltage rises the electric field at the insulator-semiconductor interface will exceed $10^5 V/cm$ [11] and the avalanching process begins with multiplication of the carriers generated in the depletion layer. Thus the generation current is given by [3],

$$J_{ga} = \frac{M_a n_i X_d}{2\tau_o} = \frac{M_a n_i}{\tau_o}\left(\frac{2\epsilon_s V}{qN_d}\right) \qquad 3.14$$

where M_a is the multiplication factor which is given by

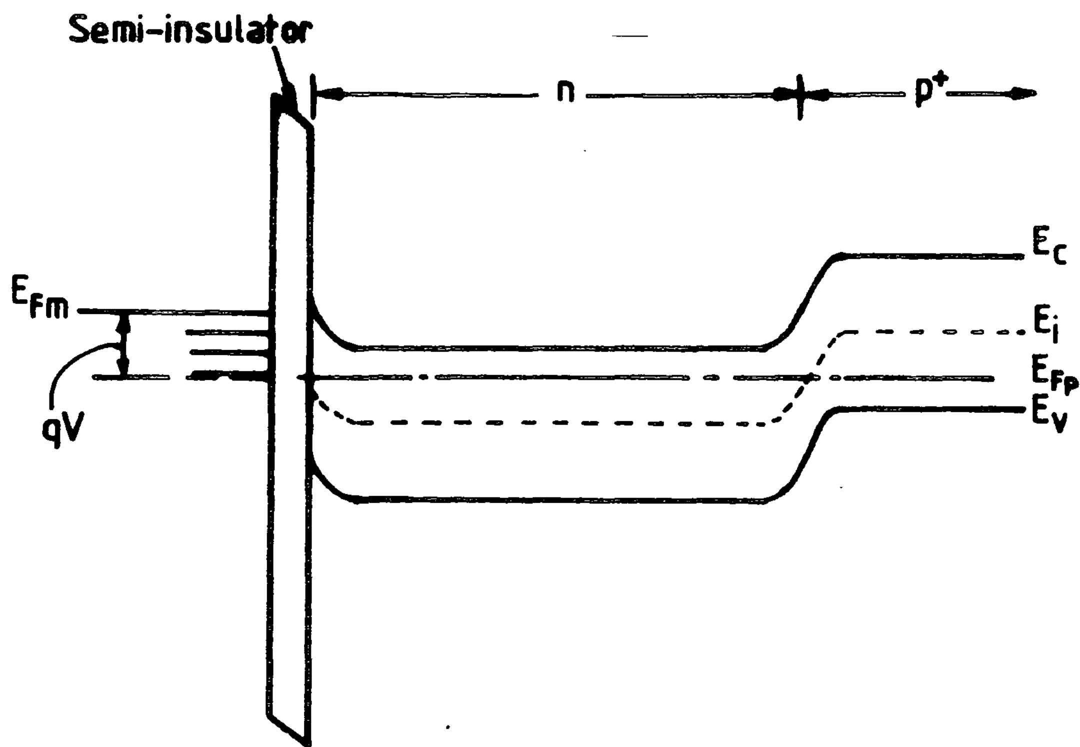
$$M_a = \frac{1}{1 - (V/V_a)^{1/2}} \qquad 3.15$$

where V_a is the avalanche breakdown voltage. As we can see the OFF current therefore increases more rapidly than in the punch-through mode.

The avalanche voltage of the n-type depletion layer is given by [9],

$$V_a \simeq 60\left(\frac{E_g}{1.1}\right)^{3/2}\left(\frac{N_d}{10^{16}}\right)^{-3/4} \qquad 3.16$$

where E_g is the semiconductor band gap in eV and N_d is the background doping



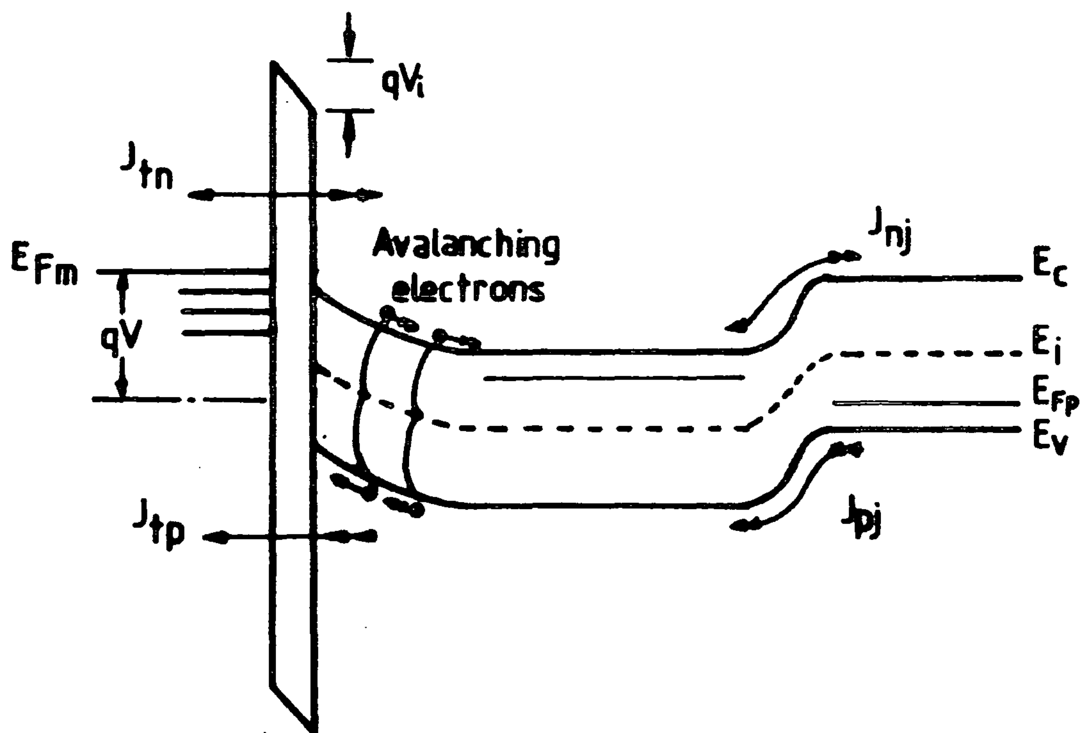


Figure 3.5 Energy band diagram for avalanche MISS a) before switching b) at the onset of switching.

density in cm^{-3}. At this voltage the current increases very rapidly and initiates the switching action as described previously. Therefore the switching voltage for the device by this mechanism is approximately equal to the avalanche voltage of the semiconductor [3].

$$V_s \approx V_a \qquad 3.17$$

Good agreement between theory and experiment has been shown with an epitaxial doping density of the order of $10^{17}cm^{-3}$ [4]. However, this type of switching mechanism is most unlikely to take place in the present device.

3.3.4 Switching in Generation Controlled Mode

In some cases neither punch-through nor avalanche can explain the switching behaviour of the MISS device. Sarrabayrouse et. al [6] show experimental data for MISS devices which have medium doping density ($10^{15}cm^{-3}$), where the switching voltage is well below that calculated for punch-through. This indicates a third possible mechanism based primarily on minority carrier generation in the depletion layer. They therefore defined the switching condition as the voltage that just produced inversion of the insulator- semiconductor interface as controlled by generation. This type of switching mechanism is called a generation controlled mode and, in fact, most of the MISS devices which we are dealing with here operate in this mode.

Many details of the electronic processes in the generation controlled mode of operation are the same as in the punch-through mode. The only difference is the mechanism which causes the device to switch. Under circumstances in which the semi-insulator is less leaky, a large part of the electron current is due to the electrons generated in the depletion region which are sufficient to turn on the p^+-n junction when they flow through it. The forward biased junction therefore injects holes from the p^+ into the n-epitaxial layer, increasing the interface charge. Raising the applied

voltage will increase the width of the depletion region so that the width of the neutral region becomes quite small and as a result the hole difusion current increases further. Due to a large flow of holes to the interface, the tunnelling mechanism through the semi- insulator reaches the tunnel-limited state and an inversion layer forms at the surface. As a result the field strength increases in the semi-insulator and the increased injection of electrons flowing from the metal to the semiconductor conduction band makes the p^+-n junction become even more forward biased. As the total gain of the internal system attains unity (see equation 3.10) the device begins to switch as before.

3.3.5 Negative Resistance and Low Impedance States

If the current is allowed to rise above the value at V_s the device enters the negative resistance state. The increment in the injected hole tunnel current, J_{tp}, will then increase the electron tunnel current, J_{tn}, and, since the flow of electrons is then large, some of them will neutralize the ionized donors and hence reduce the depletion region width, X_d, and the surface potential, ψ_s. At this point the deep depletion layer begins to collapse while allowing a larger terminal current to flow, and the voltage across the device decreases, as demonstrated in figure 3.4(c). As a result, the device exhibits S-type negative resistance in its I-V characteristics.

The decrease in the surface potential, ψ_s, in the negative resistance region will be greatly reduced when the surface becomes inverted at the value given by

$$\psi_s(inv) = \frac{2kT}{q}\ln\frac{N_d}{n_i} \qquad 3.18$$

Therefore the region where the current increases with decreasing voltage ceases at a certain minimum value V_h. Beyond this point most of the voltage drops across the p^+-n junction and the semi-insulator, the current increasing rapidly with small

increments of applied voltage. The device now enters the low impedance state in which the p$^+$-n junction is turned ON and the supply of holes is sufficiently high for the current through the device to be tunnel-limited (figure 3.4(d)).

The holding voltage for the non-ideal case is given by

$$V_h = V_{FB} + V_i + \psi_s(inv) + V_j \qquad 3.19$$

where V_{FB} is a flat-band voltage given by

$$V_{FB} = \phi_{ms} - \frac{Q_i}{C_i} \qquad 3.20$$

where Q_i is the total charge including fixed charge Q_f and interface charge Q_{is} as described in section 2.2. The voltage across the semi-insulator at the holding point is given by

$$V_i = \frac{Q_s}{\epsilon_i} d \qquad 3.21$$

where Q_s is the surface charge for the semiconductor per unit area. The voltage across the junction is then

$$V_j \simeq \frac{kT}{q} \ln \frac{J_{pj}}{J_s} \qquad 3.22$$

3.4 OPERATION OF DEVICES WITH SRO FILMS

The previous sections refer to MISS devices using very thin oxide films. Quantitatively the characteristics are determined by the conduction mechanism in the semi-insulator. In the present work this is silicon-rich oxide (SRO) and it is necessary to consider the conduction mechanism in this material. However it must be borne in mind that, this is not the main area of study in the present work.

3.4.1 Electronic Conduction in SRO

SRO films consist of crystalline silicon grains separated and surrounded by amorphous silicon and silicon dioxide [16]. Due to impurities such as oxygen shallow donor or acceptor states can exist in the silicon grains at 0.16 and 0.39eV below the conduction band edge [17]. The atomic percentage of oxygen in SRO is smaller than in the stoichiometric SiO_2 (33% of silicon, 67% of oxygen). However if the atomic percentage is too small, and approaching that of polysilicon, the film is more accurately called a semi-insulating polycrystalline silicon (SIPOS) or oxygen-rich polycrystalline silicon (ORPS) [14]. Depending on the atomic percentage of oxygen, the conduction mechanism in SRO has been ascribed to one of three different processes, a) a Symmetrical Schottky Barrier (SSB) mechanism, b) Fowler-Nordheim tunnelling, and c) Poole-Frenkel conduction [13].

Some workers [14,15,17] have assumed that the silicon crystallites form symmetrical Schottky barriers at the boundary with the surounding matrix. This model can be used if it is assumed that the separation between the grains is much smaller than the size of the grains, and that the material is then similar to polysilicon with grain boundaries controlling the current [17]. The second mechanism is the tunnelling of

electrons between potential wells associated with silicon crystallites in an SiO_2 matrix. The third conduction mechanism is the emission of electrons from the crytallites to the SRO conduction band.

Figure 3.6 shows an energy band diagram which demonstrates the Fowler-Nordheim and Poole-Frenkel conduction processes. Poole-Frenkel conduction is presumed to take effect if the percentage of Si in the SRO is small. This type of conduction has been found to occur in SRO with a silicon atomic percentage of less than 50% [13]. For SRO which contains Si of atomic percentage of greater than 50%, the conduction is believed to be controlled by the Fowler-Nordheim like tunnelling. Since the type of SRO used for the present work always contains a large percentage of Si (see Chapter 5), the SSB model and Fowler-Nordheim tunnelling processes are most relevant for consideration as the electronic conduction mechanism in our SRO. Therefore only these two mechanisms will be reviewed in the following section.

3.4.1.1 Symmetrical Schottky Barrier Mechanism

The grain boundary is composed of a shell with a high density of carrier traps distributed in the band gap which creates a space-charge region between the Si islands in the film. Tarng [14] developed the band structure by assuming that in equilibrium the Fermi levels in the silicon grain and the boundaries are aligned, causing charge redistribution and band bending. The band bending introduces a potential barrier of height, ϕ_b, for carrier transport across the boundary. Figure 3.7 shows the energy band diagram for SRO based on the SSB model. The band bending is a function of grain size, d, net doping of the grain, $N_g = (N_D - N_A)$, and trap concentration at the grain boundary, N_t per unit area. If $N_g d < N_t$, the space-charge region extends throughout the bulk of the grain [17] resulting in band bending everywhere except at the middle of the grain as shown in figure 3.7.

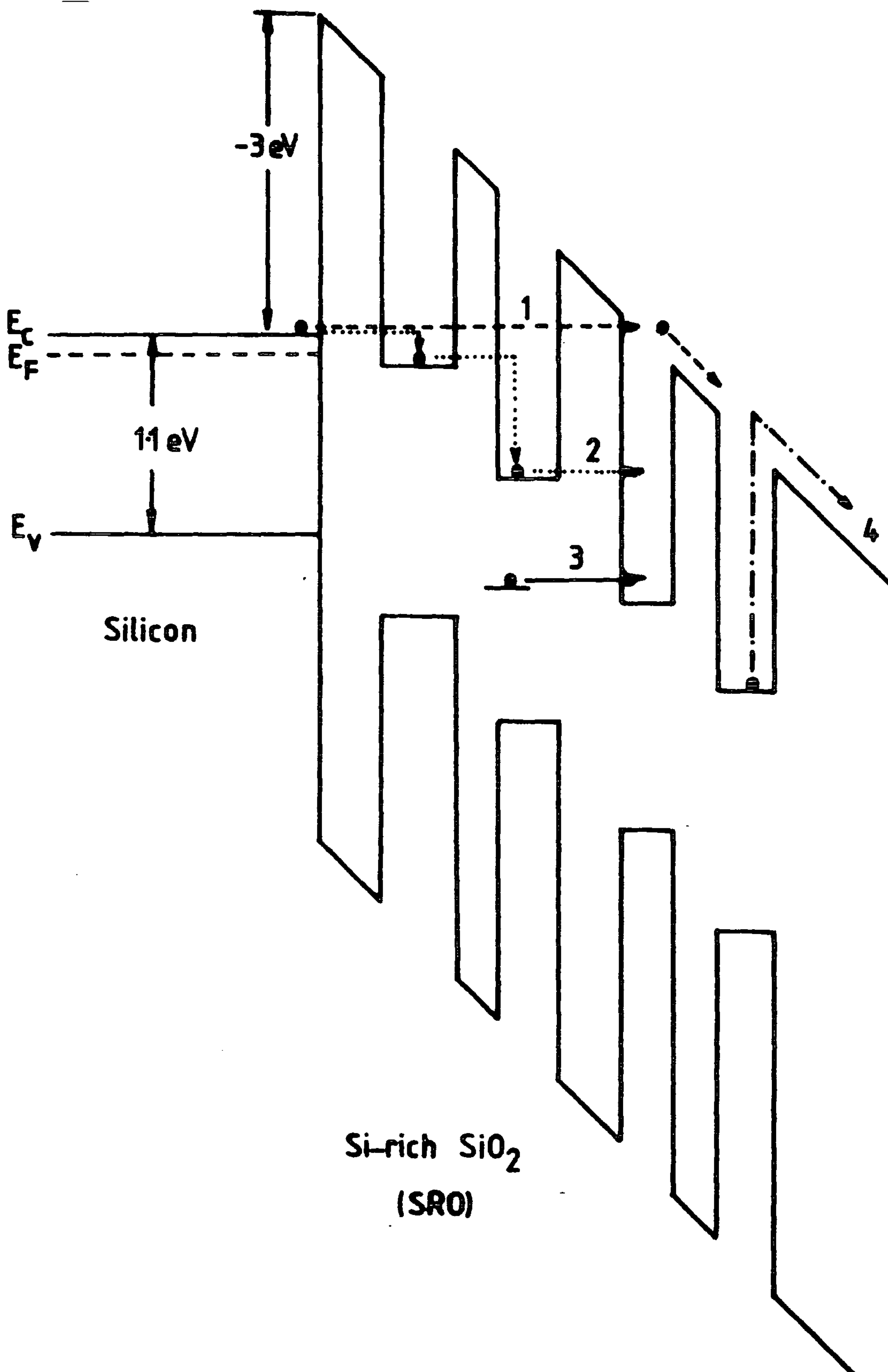
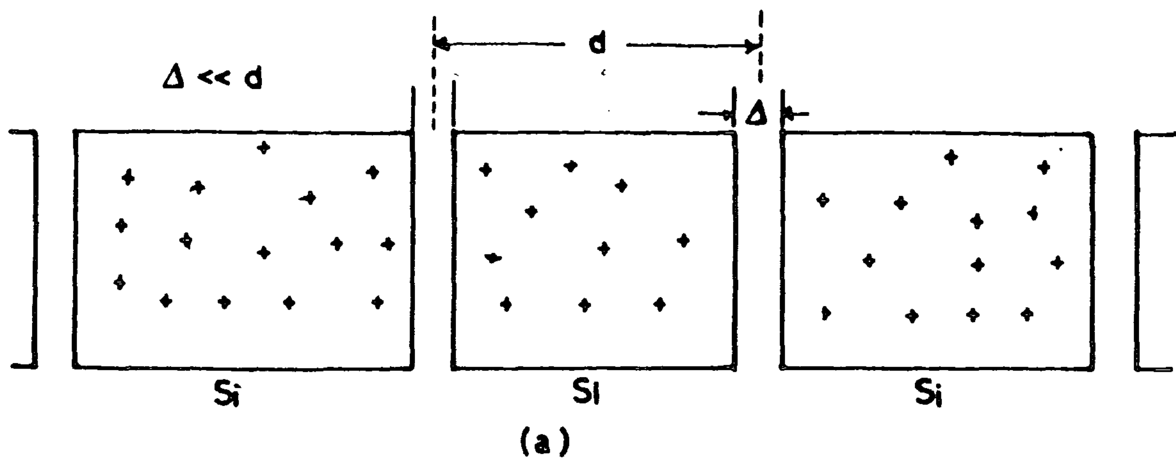


Figure 3.6 Energy band diagram of the interface between the silicon substrate and the SRO film showing direct tunnelling from silicon to SRO conduction band(dashed line 1), tunnelling from crystallite to crystallite (dotted line 2), tunnelling from deep level centres into the silicon crystallites (solid line 3) and Poole-Frenkel emission from the silicon crystallites to the SRO conduction band (dot-dashed line 4). (from ref. 13).



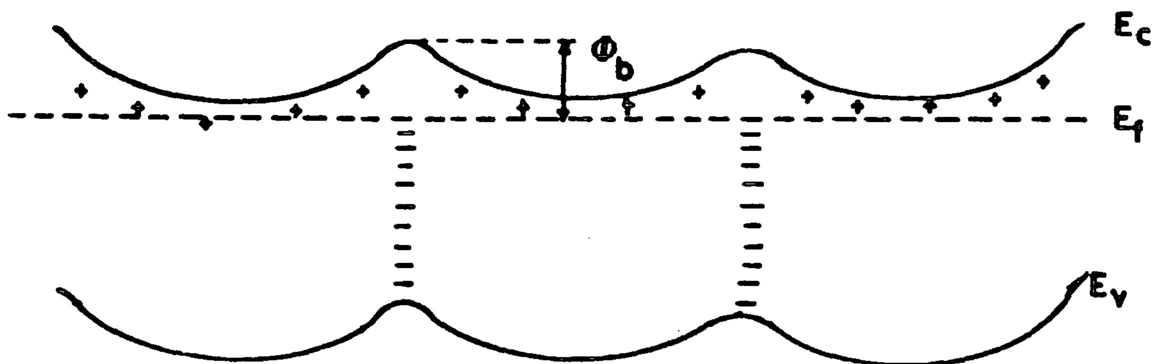


Figure 3.7 Schematic diagram of the symetrical Schottky barrier (SSB) formed by grain boundaries showing a) physical structure b) energy band diagram.

The current conduction in the SRO film can be treated by considering a series of one-dimensional symmetrical Schottky-barriers connected in series. By assuming that all grain sizes are equal, the applied voltage is divided equally between the grains. Since the structure has a symmetrical barrier, the net current through it is the sum of the current components flowing in both directions through the boundary. From the Schottky relation the current density component is given by

$$J_i = A^{**}T^2\exp(\frac{-q\phi_b}{kT})\exp(\frac{qV_g}{kT}) \qquad 3.23$$

where A^{**} is the calculated effective Richardson constant [9], V_g is the voltage drop across each grain and the relationship with total applied voltage is given by

$$V_g = V/2g \qquad 3.24$$

where g is the number of grains stacked in series, and all other symbols have their usual meaning. The factor 2 in equation 3.24 is due to the fact that only half of the voltage drop per grain occurs between the centre of the grain and the boundary. Thus the total net current density through the film is given by [14],

$$J = J_{so}\left[\exp(\frac{qV}{2gkT}) - \exp(\frac{-qV}{2gkT})\right] \qquad 3.25$$

or

$$J = 2J_{so}\mathrm{Sinh}(\frac{qV}{2gkT}) \qquad 3.26$$

where

$$J_{so} = A^{**}T^2\exp(\frac{-q\phi_b}{kT}) \qquad 3.27$$

Good agreement between theoretical and experiment results has been found by Tarng for a lateral conduction in a film with an oxygen atomic percentage of 10.5%.

Bolt and Simmons [15] have modified this model to use it for conduction through the thickness and they claimed that agreement between the Tarng's modified model and the experimental results (see table 3.1).

3.4.1.2 Fowler – Nordheim Tunnelling

The second model which has to be considered is a tunnelling mechanism between silicon islands or Fowler Nordheim tunnelling. The model was developed for SRO with an atomic percentage of 30 – 40% by assuming that the crystallites of silicon are of spherical form and equal in size [18]. The energy band system is represented by a potential well within the SiO_2 matrix as shown in figure 3.8. The energy U_e is the difference between the conduction band of the crystallite of silicon and of SiO_2, and U_h is the difference between the valence bands. and E_{gs} is the ground state for an electron in the potential well. The current flow in the system can be determined by a percolation treatment where the injected electrons tunnel from one island to another as demonstrated in figure 3.9. The current density in the bulk of the system is equal to the sum of the electronic charges crossing the imaginary plane perpendicular to the electric field per unit time i.e.,

$$J = q \sum_i \sum_j P_{ij} \qquad 3.28$$

where P_{ij} is the probability of tunnelling between potential wells, and i is summed over all potential wells on the left hand side of the unit plane and j over the wells on the right hand side provided that the line s_{ij} which connects the two wells(island) crosses the plane.

For a random distribution of silicon islands, the current density was found to be [18]

$$J = qN_w l \frac{E_{gs}}{\hbar} \sum_j \exp(-\zeta) \qquad 3.29$$

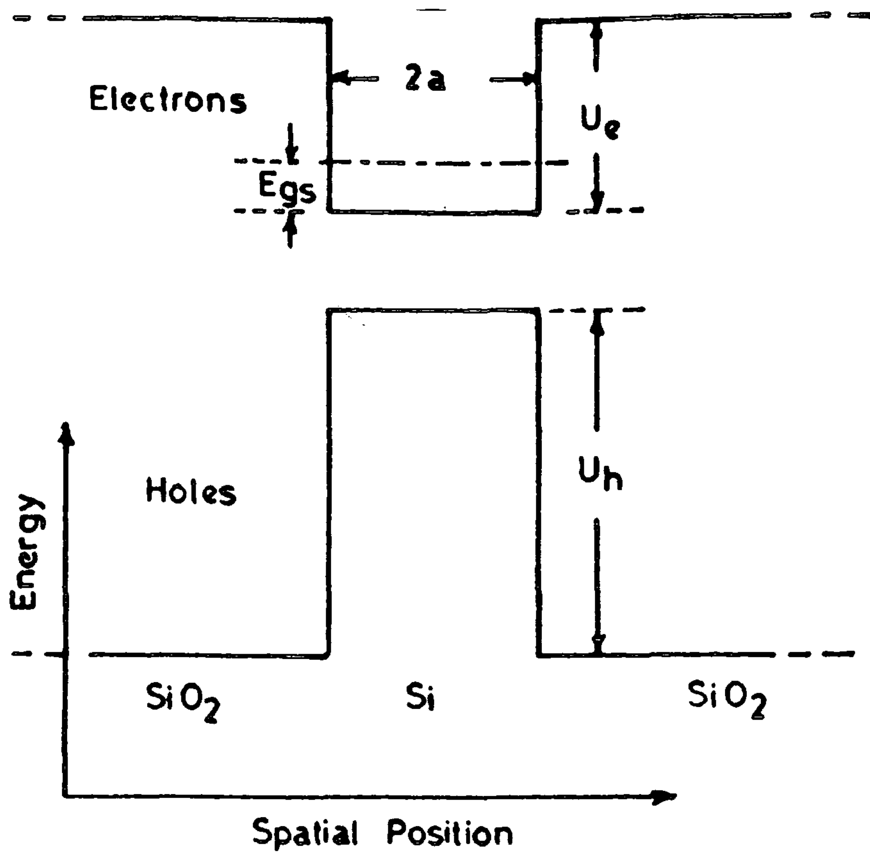


Figure 3.8 Schematic diagram of the potential of a well associated with a silicon island in an SiO_2.

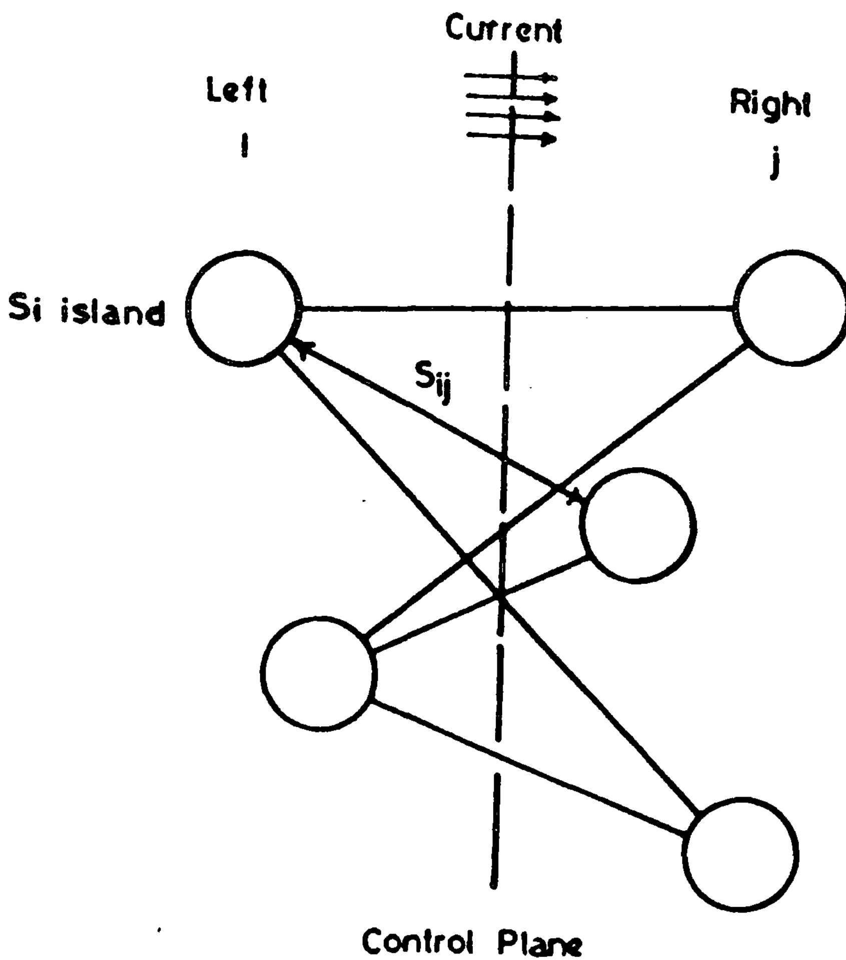


Figure 3.9 Schematic representation of the silicon island and currents

where N_w is the average number of wells per unit volume, l is the typical path length and ζ is a function derived from the tunnelling probabilities. By taking only the effective current strength between the islands the current density was found to be

$$J = CqN_w s_c \frac{E_{gs}}{\hbar} e^{-\overline{F}/F} \quad 3.30$$

where C is a numerical factor on the order of one, s_c is the critical length needed for a contribution to the current, F is the electric field strength and

$$\overline{F} = F_o \left[1 - \left(1 - \frac{q s_c F}{U_e - E_{gs}} \right)^{3/2} \right] \quad 3.31$$

where

$$F_o = \frac{4}{3} \left(\frac{2m^*}{q^2 \hbar^2} \right)^{1/2} \phi_B^{3/2}$$

and m^* is the effective mass and ϕ_B is the effective barrier height given by $(U_e - E_{gs})$. At high electric field, $\overline{F} \simeq F_o$, the current density expression becomes

$$J = K \exp\left(- \frac{4(2m^*)^{1/2} \phi_B^{3/2}}{3\hbar q F} \right) \quad 3.32$$

where

$$K = CqN_w s_c \frac{E_{gs}}{\hbar}$$

As we can see, the current density depends strongly on the barrier height and the electric field.

The thickness of the SRO layer used in the present work was 100-450 Å, and it consists of three layers with the SRO in between very thin films of atmospheric oxide. For this range of thickness it is believed that the atmospheric oxide layers also affects the conduction in the whole film. In contrast, the conduction mechanism study made by Bolt and Simmons [15] was based on SIPOS films with thicknesses

between 1200 to 5000Å so that the overall conduction was most probably dominated by the conduction in the bulk of the film. A preliminary investigation made by Pennington [19] has shown that the Fowler-Nordheim tunnelling mechanism seems to be responsible for conduction in the present type of SRO. Table 3.1 lists the investigations of SRO/SIPOS reported by a number of workers compared with the type of film used for the present work. As we can see, three different conduction mechanisms have been proposed. Since a lot of information is unavailable such as the percentage of oxygen, reactant gases ratio, R_o, film thickness and type of reactor used elsewhere, we are not certain which conduction mechanism can be applied to our film. We therefore speculate that the conduction in our SRO is by a combination of the SSB mechanism and Fowler-Nordheim tunnelling.

3.4.2 Bolt and Simmons's Model for SIPOS-MISS

The first qualitative and quantitative model of the SIPOS-MISS device with a low percentage of oxygen in the film has been proposed by Bolt and Simmons [12] who used the SSB process as the conduction mechanism in the film. This model does not necessarily apply to our present SRO-MISS device, however, since their films probably contained less oxygen, hence the name SIPOS, and they were certainly considerably thicker. Also these authors give no indication of how they avoided thin oxide layers on both sides of the SIPOS which could greatly influence the conduction. However, for completeness, their model for the electronic processes in their SIPOS-MISS devices will be briefly described in this section. In this model, the Fermi level was assumed to be pinned to the metal-SIPOS interface and hence the barrier height at the interface was neglected. The energy band diagram of the SIPOS-MISS which they proposed is shown in figure 3.10 for an equilibrium condition. The silicon surface is already

Table 3.1: Comparative results for SRO/SIPOS

Reference	Preparation	Oxygen at. %	Thickness	Properties	
				C-V	I-V
Author	Reactor: APCVD $R_o = 0.09 - 0.25$ Temp: 650^oC Time: 0.6 – 2.0 min.	–	100 – 500$\AA$	–	–
Buchanan (from ref. 13)	Reactor: APCVD $R_o = 0.25 - 1.0$ Temp: 625 – 650^oC Time: 5.0 – 10.0 min.	22.0 – 44.7%	191 – 634$\AA$	–	Poole-Frenkel
Buchanan & Pennington (from ref.19	Reactor: APCVD $R_o = 0.5 - 1.0$ Temp: 650^oC Time: 0.5 – 1.0 min.	–	186 – 600$\AA$	–	Fowler-Nordheim
Bolt & Simmons (from ref. 15)	Reactor: APCVD $R_o =$ — Temp: 650^oC Time: —	5.2 – 27.9%	1200 – 5000$\AA$	-ve charge at the interface	Symetrical Schottky barrier
DiMaria (from ref. 18)	Reactor: — $R_o = 3$ Temp: 700^oC Time: —	60 – 66%	–	–	Fowler-Nordheim
Zommer (from ref. 17)	Reactor: APCVD $R_o =$ — Temp: 750^oC Time: — Annealed at 930^oC	25.0%	250μm	–	Symetrical Schottky barrier
Tarng (from ref. 14)	Reactor: — $R_o =$ — Temp: 650^oC Time: – Annealed at 900^oC	10.5%	6μm	–	Symetrical Schottky barrier

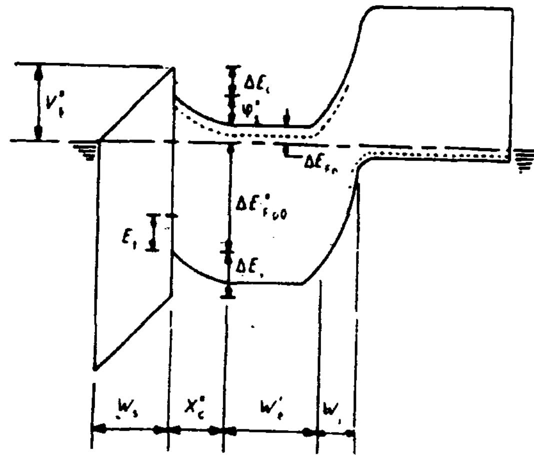


Figure 3.10 An energy band diagram for the SIPOS-MISS device at equilibrium (from ref. 12).

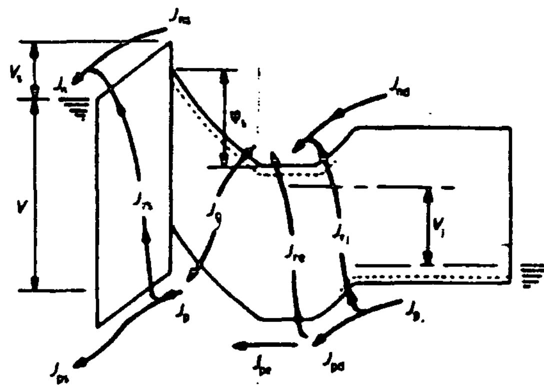


Figure 3.11 An energy band diagram for the SIPOS-MISS device under bias, showing the internal current components. J_{ns}, J_{ps}: electron and hole drift diffusion currents across the SIPOS layer. J_{rs}, J_{re}, J_{rj} : net recombination currents in the SIPOS layer, the neutral epilayer region and the depletion region of the p-n junction respectively. J_g: the generation current within the surface depletion region. J_{nd}, J_{pd}: electron and hole diffusion currents at the edge of the depletion region of the p-n junction respectively (from ref. 12).

depleted due to the presence of a negative charge at the interface [15]. As a result, at zero bias there is an initial voltage, V_i^*, dropped across the SIPOS layer and the initial surface potential is ψ_s^*, at the SIPOS-Si interface. ΔE_c and ΔE_v are the conduction and valence bands discontinuties at the SIPOS-Si interface respectively. In figure 3.11 the internal current components of the device under forward bias are shown.

At low forward bias (negative potential on the electrode) the silicon surface becomes more depleted and the total current is mainly due the generation of electron-hole pairs in the depletion region. As the applied voltage is increased the depletion layer width increases causing the generation current J_g to increase further. In order to accomodate the generated electron and hole current the voltage across the p^+-n junction, V_j, and the SIPOS, ΔV_i ($\Delta V_i = V_i^* - V_i$), increases by a small amount. Increasing V_j causes the hole current through the junction to increase and hence further increase the number of holes arriving at the SIPOS-Si interface. As a consequence the electron current from the metal through the SIPOS increases and this augments the electron component in the semiconductor and hence causes V_j to increase further which will induces more hole current to flow from the p^+-n junction. When the rate of hole flow to the interface is greater than that flowing through the SIPOS the free hole concentration at the interface increases.

As a result the SIPOS-Si interface potential moves from deep depletion to inversion and the voltage across the device decreases due to a decreasing semiconductor surface potential. The electric field across the SIPOS increases as a result of the build up of the inversion charge. More current passes through the SIPOS and hence the current through the device increases. In this region the device exhibits a negative differential resistance. Eventually, as the SIPOS-Si interface become fully inverted, the low impedance state is established and any further increment in applied voltage will then increase the voltage drop in the SIPOS and in the p^+-n junction.

3.4.3 Current Equations

In MISS devices three major components of current have to be considered, the p- n junction currents, the generation and recombination currents in the epitaxial layer, and the current through the semi-insulator. The first and the second are in the semiconductor and are common for all type of MISS. However, the third component is determined by the type of material used as the semi-insulator layer. For tunnel-oxide the current expressions are well established if represented by direct tunnelling between metal and semiconductor [5,6]. In the SIPOS layer, the electron and hole currents are comprised of diffusion and recombination components in [12]

$$J_n = J_{n_S} + J_{r_S} \qquad 3.33$$

and

$$J_p = J_{p_S} + J_{r_S} \qquad 3.34$$

where $J_{n_S}(J_{p_S})$ is the electron(hole) diffusion current and J_{r_S} is the recombination current in the SIPOS. Based on the SSB model the electron diffusion current can be written as

$$J_{n_S} = 2J_{nso}\sinh(\frac{qV}{4gkT}) \qquad 3.35$$

where J_{nso} is given in (3.27). The hole diffusion current is

$$J_{p_S} = 2J_{pso}\sinh(\frac{qV}{4gkT}) \qquad 3.36$$

where J_{pso} is different from J_{nso} because the rate at which holes can be supplied to the SIPOS-Si interface depends on the hole concentration, p_{ns} at the interface so that

$$J_{pso} = qv_p p_{ns}\exp(\frac{-\psi_s}{kT}) \qquad 3.37$$

where v_p is the thermal velocity of holes. Bolt et al proposed an expression for the recombination current in the SIPOS which is given by [12]

$$J_{r_S} = \frac{2qW_S n_{i_S}}{\tau_s} \left(\frac{p_{ns}}{p_o}\right) \sinh(\frac{qV}{8gkT}) \qquad 3.38$$

where W_S is the thickness of SIPOS layer, n_{i_S} is the intrinsic carrier concentration in SIPOS, τ_S is the carrier lifetime in SIPOS, and p_o is the hole concentration at equilibrium.

These equations were used by Bolt and Simmons to produce theoretical I-V characteristics that could be fitted quite well to their experimental results although they do not mention the two-dimensional effects that will be shown in Chapter 5 to control the characteristics.

3.5 SUMMARY

In the first part of this chapter a theoretical survey of MISS device operation was presented showing that three switching mechanisms were possible, the punch-through mode, avalanche mode and the generation controlled mode. The first mode applies for a very leaky semi-insulator, the second is for the MISS with high doping concentration in the epilayer, while the third is for the device with a less leaky semi-insulator. The details of each mechanism were reviewed based on the tunnel oxide MISS. The basic switching process for all MISS devices is the same regardless of the types of semi-insulator used. However the details of the device characteristics are strongly governed by the conduction mechanism in the semi-insulator. For the case our SRO Fowler-Nordheim tunnelling could be responsible for the carrier conduction although a symmetrical Schottky barrier mechanism is also possible as has been proposed by others [12]. However in explaining the electronic process in the SIPOS-MISS in this chapter only the SSB model was used for the electronic conduction since there is far less information is available about the alternative.

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CHAPTER FOUR

FABRICATION AND ELECTRICAL CHARACTERIZATION OF THE DEVICE

4.1 SEMI-INSULATING SRO FILMS

The work presented in this thesis is based on MISS devices which have been fabricated at Durham and Southampton Universities. The MISS structures which were fabricated at Southampton are more complicated and they required better fabrication facilities. However, the mask patterns were designed in Durham by P. Clifton in collaboration with Rutherford Laboratories. Both Durham and Southampton processes used the same semi-insulating films which were deposited in the Durham Microelectronics Clean Rooms †. This chapter is devoted to a description of the device fabrication process at Durham and the techniques used for characterization of the devices. Since the semi-insulating films used in this work are not as common as oxide films, this chapter commence with the general description of the film properties and the preparation technique.

The semi-insulating material used in this devices was silicon-rich-oxide (SRO)* which is slightly different from semi-insulating polycrystaline silicon (SIPOS). It is certainly a polycrystaline silicon but heavily doped with oxygen. The films are generally deposited by means of chemical vapour deposition using either a N_2O/SiH_4 system with N_2 carrier gas or a CO_2/SiH_4 system with H_2 carrier gas [8]. The macroscopic chemical composition of SRO can be expressed as SiO_x $(0 < x < 2)$. It has been

† Class 1000 clean rooms, well equipped for standard $10\mu m$ p-MOS process

* This term will be used throughout the thesis

shown that microscopically the SRO layer as deposited is made up of two phases, Si and SiO_2, with the Si being amorphous [1]. After annealing at $1,000^oC$ in a nitrogen ambient SRO becomes a mixture of silicon crystallites, amorphous silicon and silicon dioxide [2,3]. The size of the Si microcrystals, ($< 10\AA$) in SRO as deposited depends both on the deposition temperature and on the oxygen concentration. However, in heat-treated SRO the microcrystal size, ($50\AA - 100\AA$) depends on the annealing temperature and weakly on the annealing time. The conductivity of the SRO films depends upon the silicon content and the higher it is the higher the conductivity. The silicon content can be controlled by changing the gas phase reactant flow ratio R_o = (N_2O:SiH_4) to control the resistivity in the range of $10^8\Omega$cm – $10^{10}\Omega$cm [4]. The conductivity is highly non-ohmic and therefore a strong function of electric field.

Other properties of SRO which are superior to SiO_2 are its low permanent trapping of carriers, its high dielectric constant [10] and enhanced electron injection into oxide [6]. These features have given rise to the application of SRO layers as passivating layers in high voltage power transistor [16] and silicon planar devices [17], as electron injectors for Electrically-Alterable Read-Only Memories (EAROM) [6,7], and as a material to increase the capacitance and yield of storage capacitors in memory cells [10]. This material has also been used to make a heterojunction transistor with high current gain [18]. Recently, this film has been used for a heterojunction SRO-Si solar cell [19, 20] and a double heterostructure SRO:Si:SRO solar cell has been shown to generate 720mV open circuit voltage[20].

4.2 CHEMICAL VAPOUR DEPOSITION OF SRO

The deposition process where a film is deposited by mean of chemical reaction or pyrolytic decomposition in the gas phase is called Chemical Vapour Deposition (CVD). This process is widely used in the microelectronics industry for deposition

of silicon dioxide, silicon nitride, polysilicon and silicon-rich-oxide. The oxide films deposited by means of CVD have several advantages: thicker films can be obtained in a short time and at a lower temperature because the growth rate is quite high, about $500 - 1000\AA/\min$ [11], no silicon is consumed as in thermal oxidation, and the films can be produced on substrates other than silicon. There are four types of CVD reactor available for industrial and research applications. They are atmospheric pressure CVD, low pressure CVD, low temperature CVD, and plasma enhanced CVD.

The type of reactor used to deposit SRO for the purpose of the present studies at Durham is the atmospheric pressure chemical vapour deposition (APCVD). A simplified schematic diagram of the APCVD system is shown in figure 4.1, and the complete system is shown in figure 4.2. For this type of reactor the chemical reaction takes place in a cold wall reactor chamber which has the advantage of reducing the amount of wall deposit that can degrade the films due to particles falling. The wafers are laid horizontally on a carbon susceptor which has a large thermal mass so that the temperature remains stable during deposition. The reactor chamber is heated from below using an array of tungsten halogen lamps. The temperature in the chamber is measured and controlled by detecting the black body radiation from the susceptor.

The SRO films deposited in an APCVD reactor use silane, SiH_4, (commonly supplied in a low dilution in nitrogen because pure silane can burn and explode when exposed to air). In this work, a composition of 5% SiH_4/N_2 was used together with nitrous oxide, N_2O, and nitrogen, N_2 as the carrier gas. Deposition temperatures are generally between 620-700^oC, but for the present purpose a temperature of 650^oC was used. The phase ratio of the reactant gases R_o is given by,

$$R_o = \frac{flow\ rate\ of\ \mathrm{N_2O}}{flow\ rate\ of\ \mathrm{SiH_4}} \qquad 4.1$$

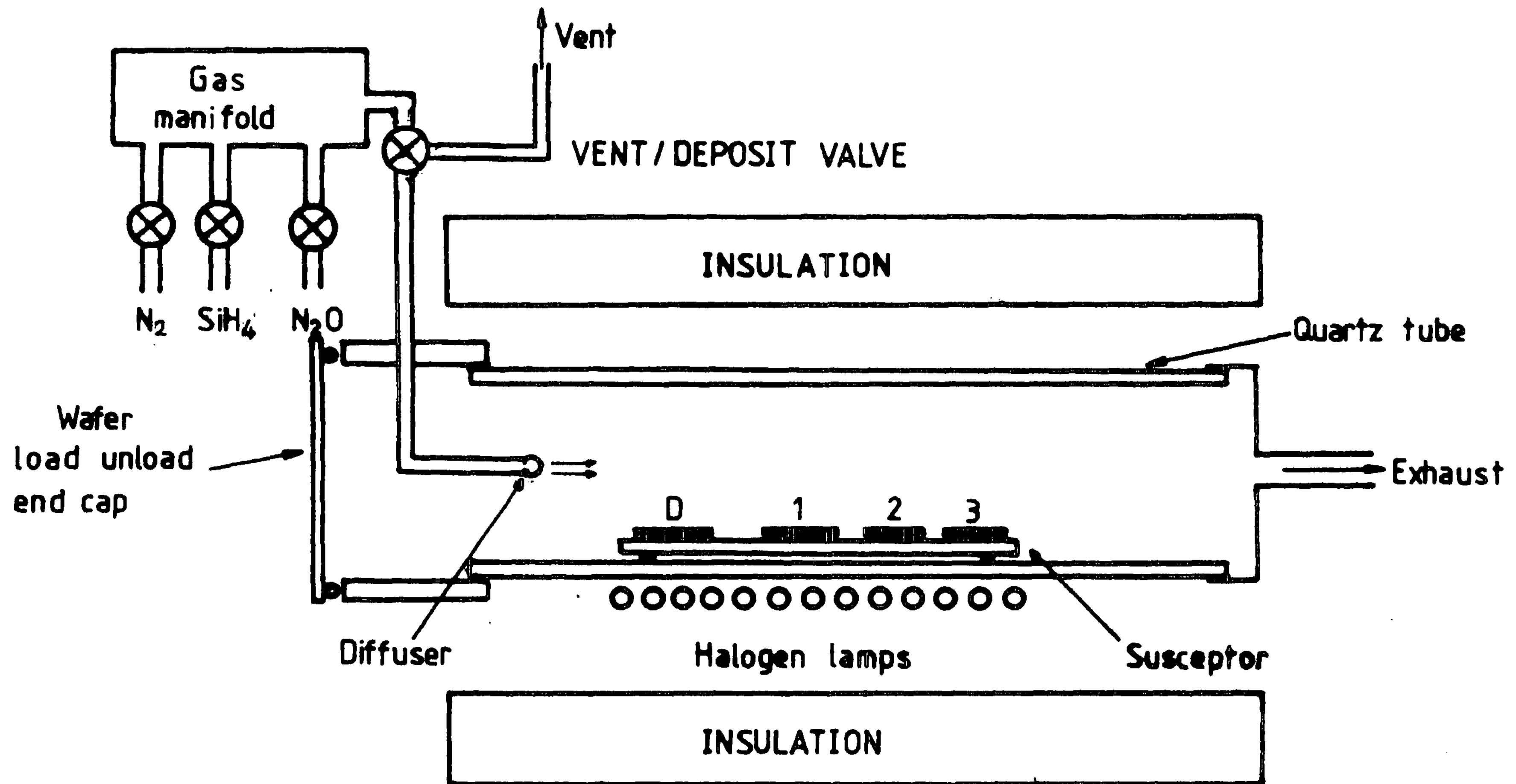


Figure 4.1 Simplified view of APCVD reactor

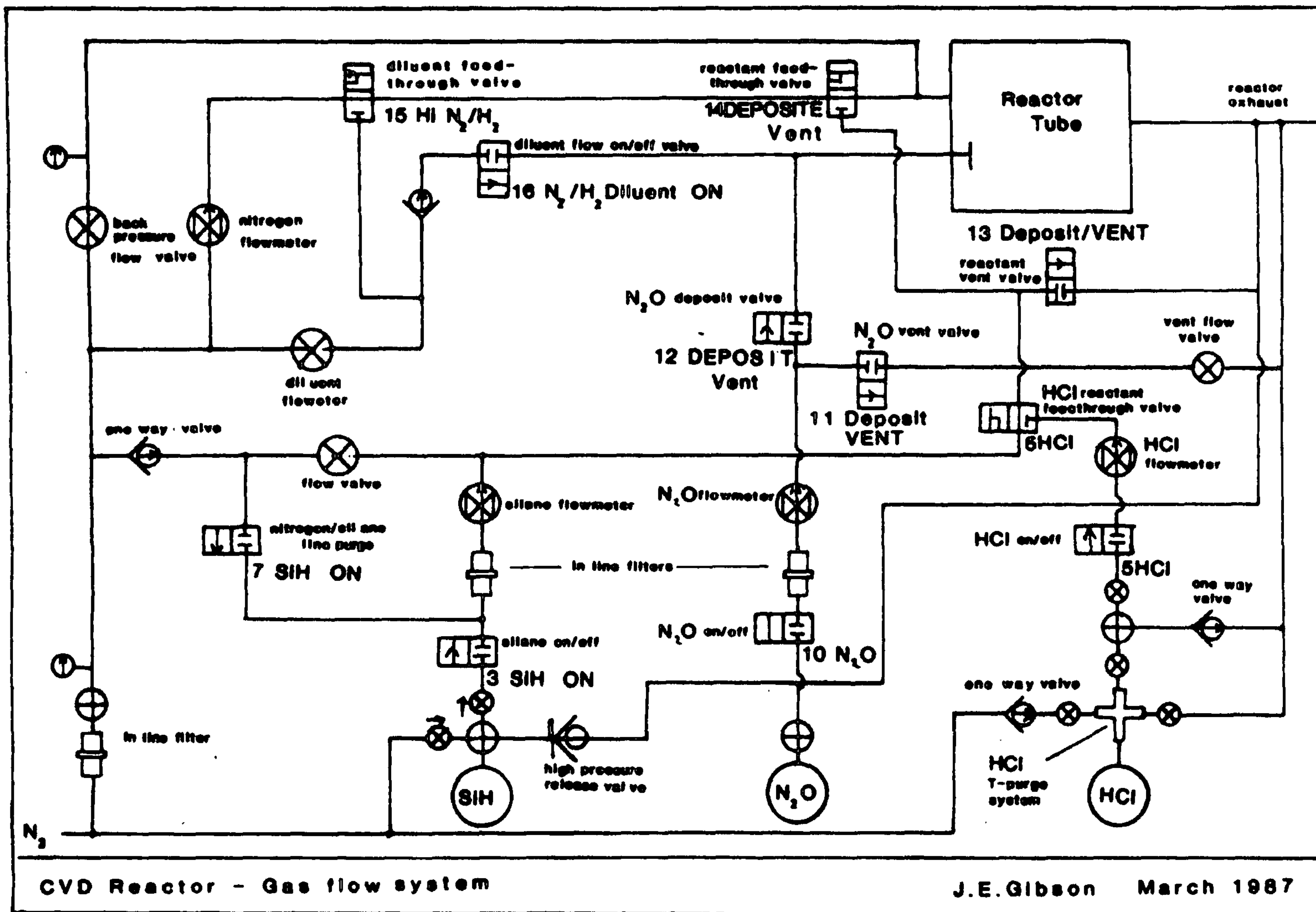


Figure 4.2 Complete system of APCVD

As the phase reactant ratio R_o increases the silicon content decreases. The relationship between the excess silicon content and R_o is not linear (figure 4.3) and it is also dependent on the deposition temperature [5,14]. The growth rate of the SRO films at a constant flow rate of SiH_4 has been shown to be dependent on R_o [15] and it decreases as R_o increases. However at constant R_o the growth rate increases with the SiH_4 flow rate. For the present purpose the flow of the carrier gas was maintained at 35 litres/minute, the flow rate of the N_2O was varied between 5 and 14 ml/min, and the silane flow was maintained at 61 ml/min.

Since SRO is a non-stoichiometric material, its depositon is difficult to control in cold-wall CVD reactor. An accurate control of both temperature and flow dynamics is very important. The latter has been improved by installing a new home-made gas diffuser as shown in figure 4.4(b) to replace the original T-type diffuser shown in figure 4.4(a). The new diffuser has improved the quality of the SRO films compared to those with the original diffuser. The uniformity of the films may still not be very good because the high flow rate of the carrier N_2 may cool the wafers. More recently, Kwark et al.[13] have successful improved the deposition quality for this type of reactor by preheating the carrier gas before it enters the reactor chamber. The position of the wafer on the susceptor also influences the uniformity of the films probably because the flow of gas is more turbulent towards the inlet and outlet. The usable areas of good deposition on two inch wafers were at positions 1 and 2 as shown in figure 4.1. A study made by E. M. Geake [12] has shown that SRO films deposited at position 2 are the most uniform with 6% and 5% variations in refractive index and thickness across the diameter respectively. Therefore, this position was used throughout the work.

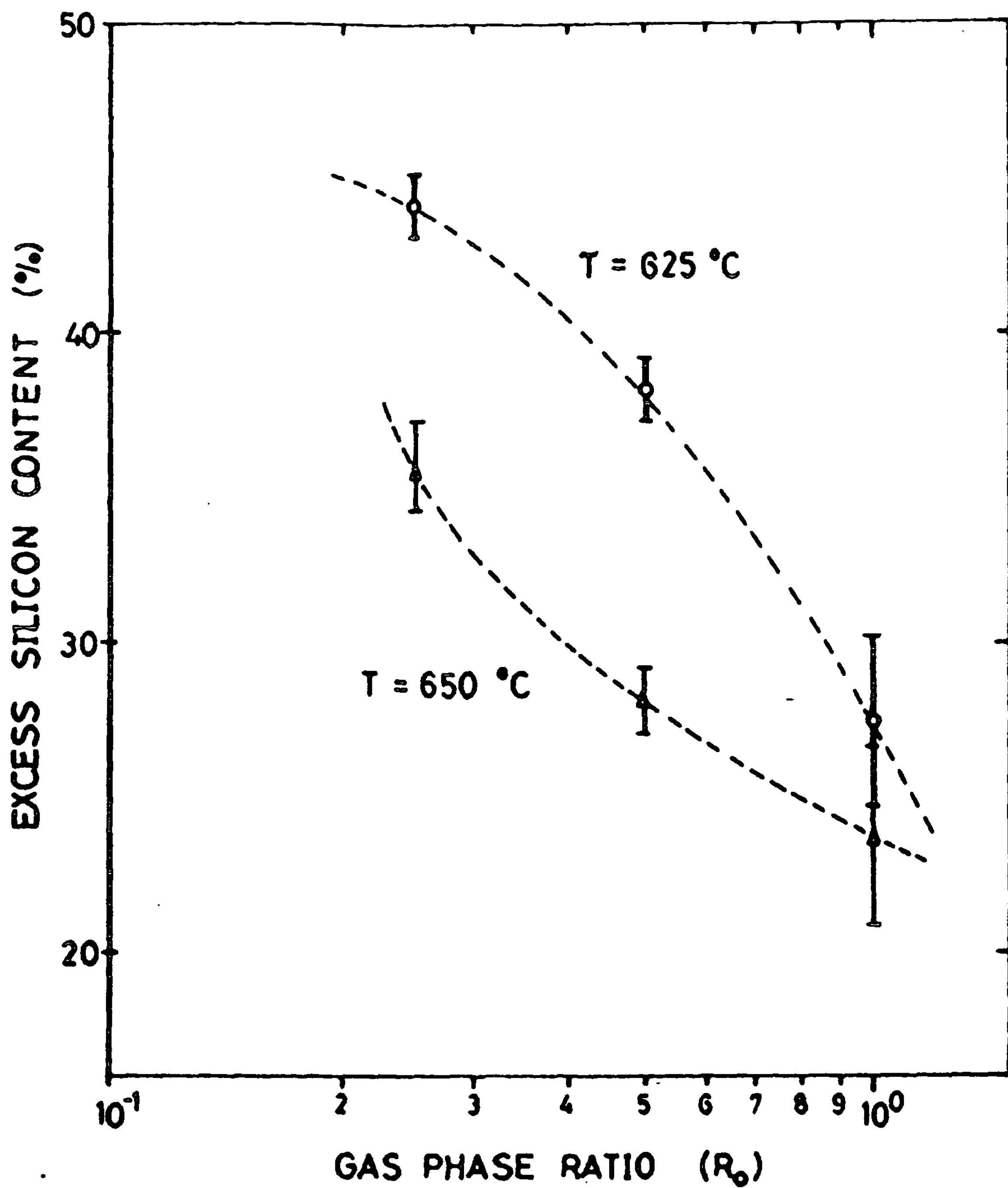


Figure 4.3 Excess silicon content (over stoichiometric silicon dioxide) as a function of gas phase ratio, R_o, for deposition temperature of 625°C and 650°C (from ref. 5).

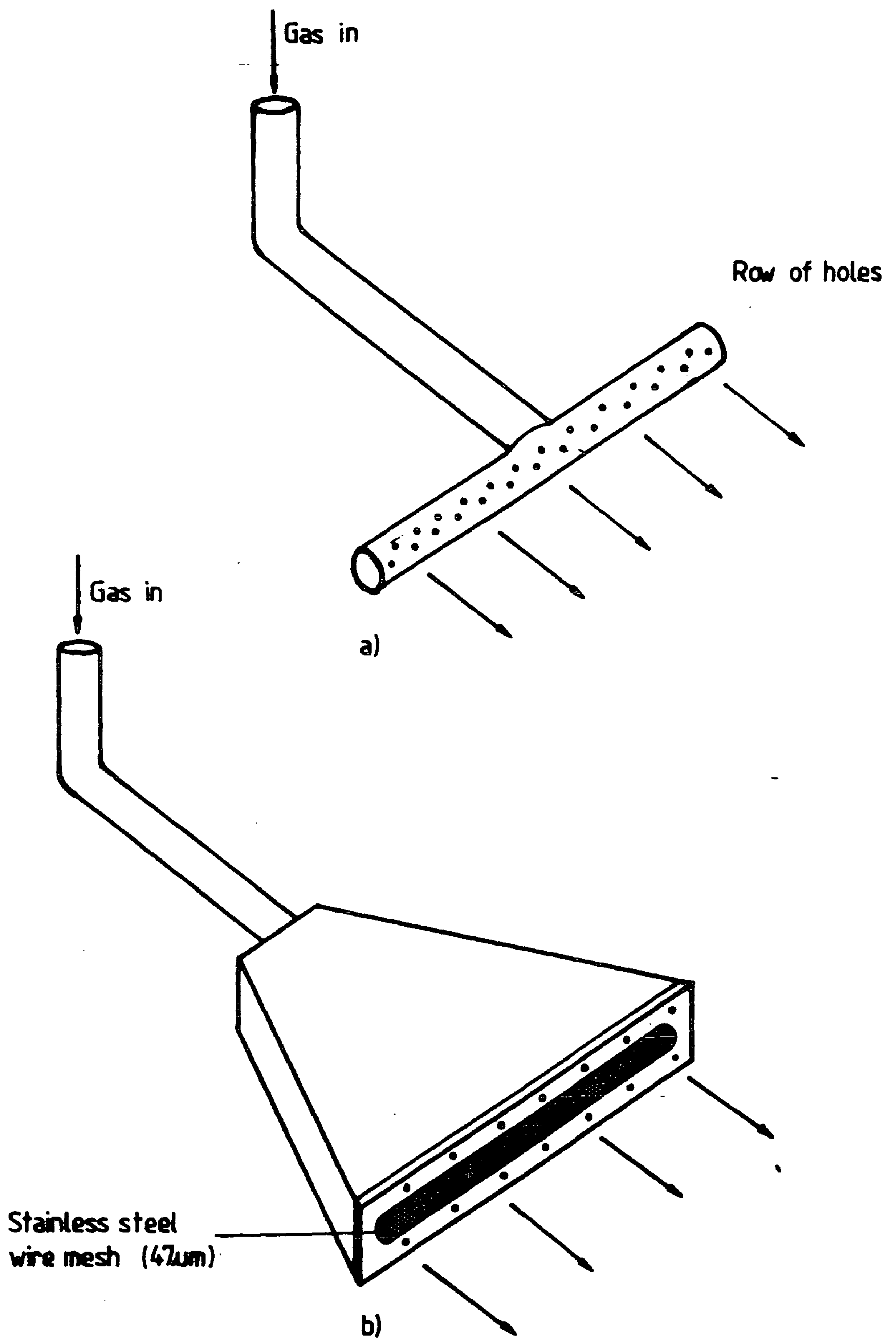


Figure 4.4 a) Original T-type diffuser

b) Home made diffuser

4.3 SAMPLE FABRICATION

The silicon used in these experiments was in the form of silicon wafers with a $4.4\mu m$ n-type epitaxial layer on a p^+ substrate with either $< 111 >$ or $< 100 >$ orientation. The resistivity of the epitaxial layer was 5.3Ω.cm, which corresponds to a doping concentration of 9×10^{14} cm^{-3}. The wafer size was two inches in diameter, and for the present purpose it was cut into four sections before film deposition in order to match with the size of the mask used later.

4.3.1 Cleaning the Wafer

Great care was taken with the cleaning of the silicon before film deposition. First, the wafer was boiled twice in Ultra grade trichloroethane for 5 minutes to remove grease. Then it was boiled in a strong oxidising agent ("bomb" ie; 1 : 1, H_2O_2 : H_2SO_4) for 30 minutes to remove organic contamination. This also oxided the surface and the oxide was removed by dipping the slice in 10% hydrofluoric acid, (10% HF) **. The slice was then rinsed thoroughly in ultrapure water before proceeding to the next stage of processing. The details of this procedure are explained in appendix B.

4.3.2 SRO Deposition Procedure

After the cleaning process, the wafer was again dipped in 10% HF, rinsed in

** Hydrofluoric acid (HF) is widely used for etching SiO_2. It is useful in silicon device fabrication because of its selectivity in etching silicon very much more slowly than SiO_2. It is commonly used in two forms, 10% HF (1 part 40% HF and 3 parts H_2O) and buffered HF (1 part 40% HF and 4 parts 40% ammonium fluoride). The latter is more selective, and will etch silicon only if its surface becomes oxidised.

deionized water, and blown dry immediately before loading into the CVD reactor. The ratio of N_2O to SiH_4 was set by adjusting the flow rate of both gases depending on the deposition parameters required and the composition of the SiH_4/N_2 gas. For the purpose of the present study ratios of 0.1 - 0.25 were used and the deposition times were between 0.6 and 2 minutes.

Immediately after deposition the thickness and index of refraction of the films were measured using an ellipsometer which was designed mainly for measurement on highly transparent films like SiO_2. As SRO absorbs some of the light, measurement of the thickness and refractive index are only reliable for index values from 1.4 to 3.2 [12]. The error in the measurement increase with increasing silicon content. Figure 4.5 shows the relationship of refractive index and film thickness with deposition time for $R_o = 0.2$.

Precise details of the deposition procedure are given in Appendix B.

4.3.3 Top Contact Preparation

Aluminum of 99.9995% purity was evaporated on the top of the film using an electron-beam evaporator. The vacuum system consist of two sorption and one ionization pump and in addition a diaphragm pump was installed to speed up the roughing process. Since no rotary pump was used the system is free from oil. Figure 4.6 shows the schematic diagram of the vacuum system of the electron beam evaporator. The evaporation chamber is made of metal with small glass window to estimate the thickness of the evaporated metal. The samples were placed in the sample holder with the SRO surface facing towards the source. Evaporation was performed at a pressure of 10^{-7} torr and the Al source was vaporized by focussing a high intensity electron beam onto it. The vaporization occurs at a small spot in the Al source only, so that the

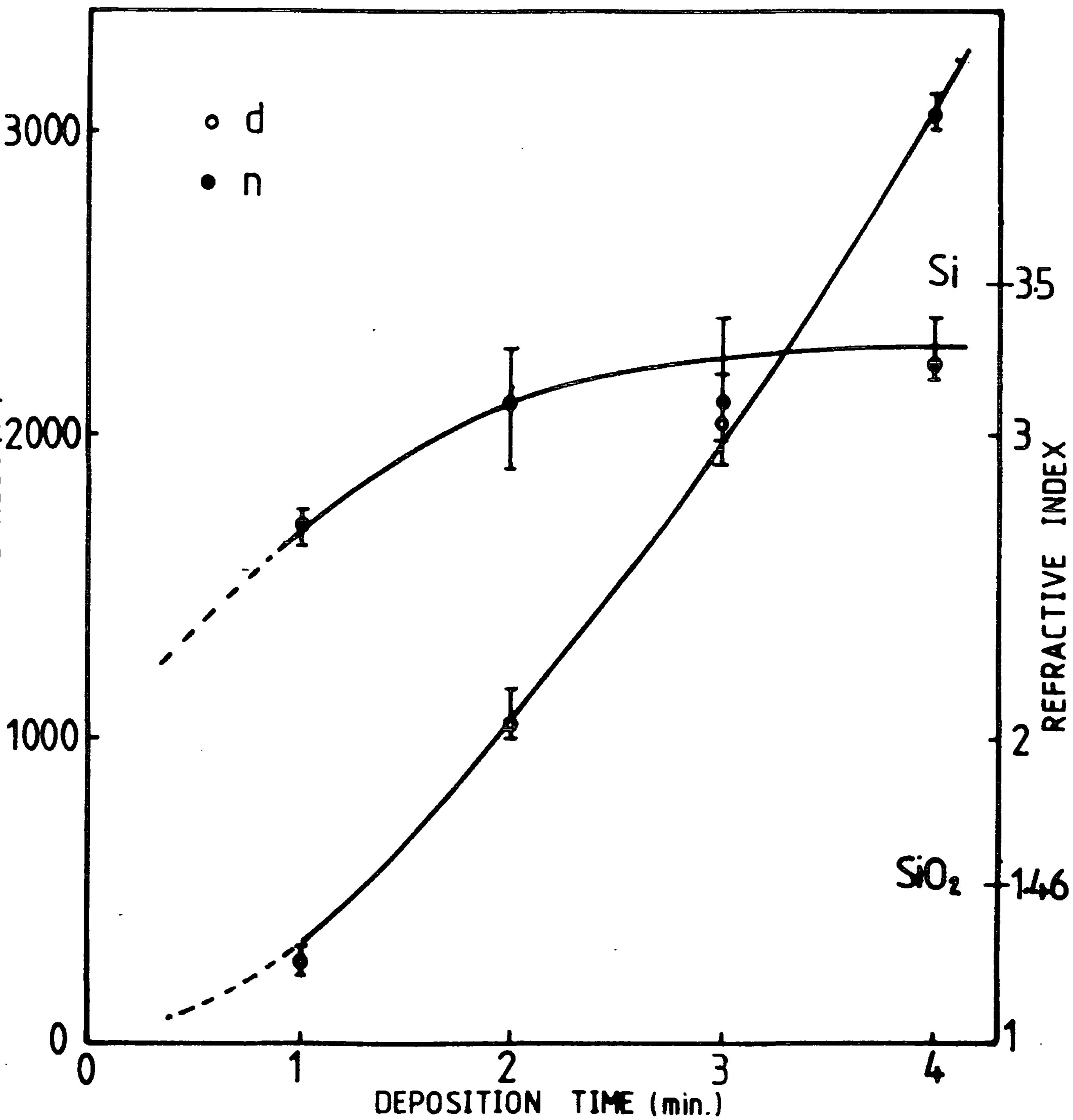


Figure 4.5 Refractive index and thickness of SRO as a function of deposition time.

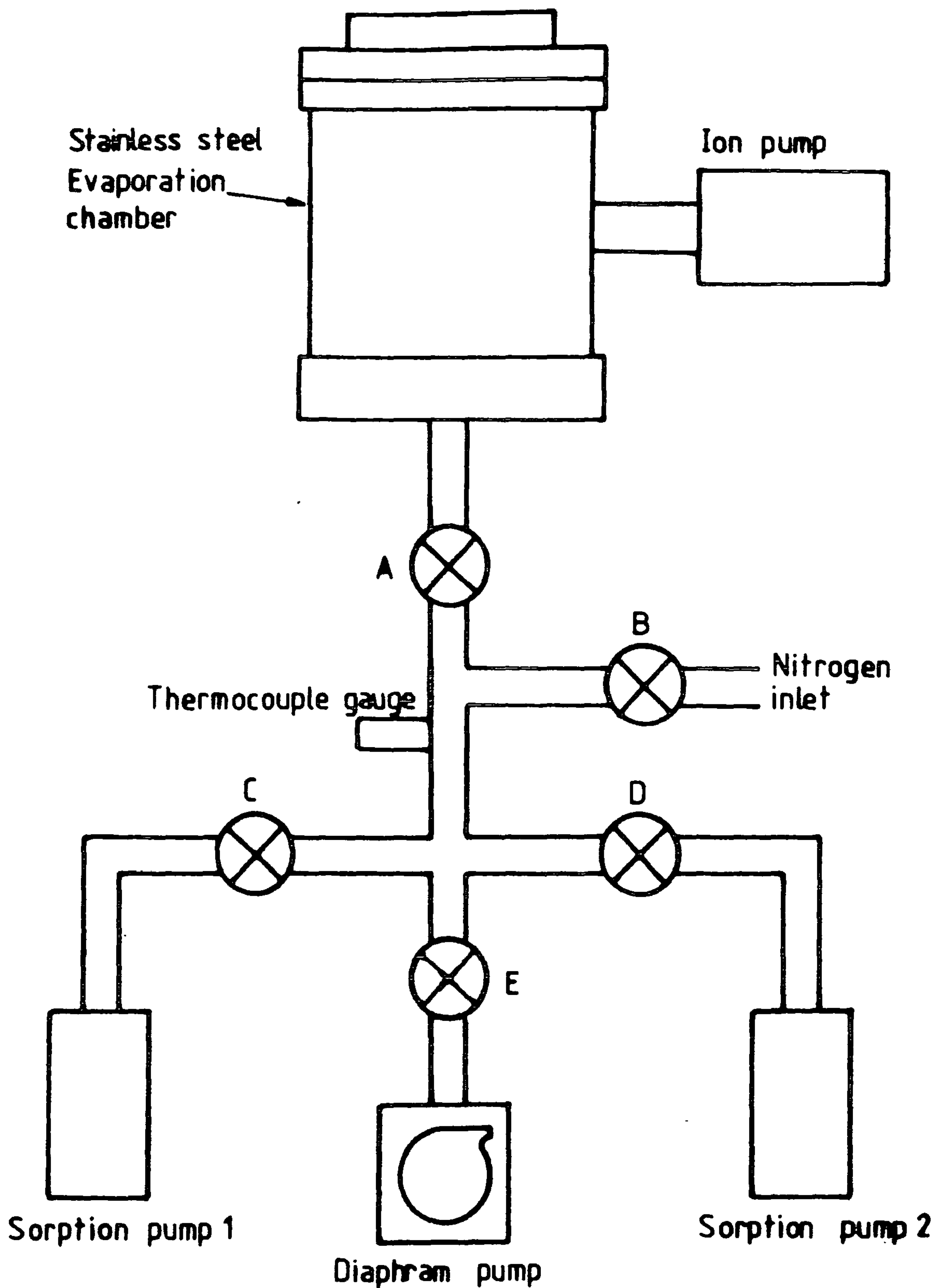


Figure 4.6 Schematic diagram of varian vacuum system for electron beam evaporator.

crucible is free from direct heat and hence does not emit unwanted contaminant atoms which would occurs in a thermal evaporation system. Since a voltage of the order of 4kV is applied to the electron gun the characteristic Al K-shell X-rays are generated, and this radiation penetrating the substrate surface and may cause damage to the SRO layer and degrade the film [9]. In order to avoid heating the sample too much the evaporation was carried out in several stages with a 5 second evaporation and a 10 minute interval before the next stage to allow the sample to cold down.

An electrode pattern was defined by standard photolithography. A mask with seven different sizes of dots was used in most of the work †, the smallest and largest being of $0.18mm^2$ and $2.36mm^2$ area respectively. A thin photoresist (Shipley Microposit 1350) was dropped onto the centre of the wafer and spun for 30 seconds or until the whole surface was covered evenly with photoresist. After baking for 10 minutes on a hot plate at a temperature of 80^oC, the wafer was exposed with UV light by means of a mask alignment machine. The exposed photoresist was removed by dipping it in 50% developer for 5 seconds. The unwanted Al was etched away in orthophosphoric-nitric acid (30:2:7 orthophosphoric:nitric acid:water), normally taking about 2 minutes. The photoresist remaining on the Al was removed with acetone in an ultrasonic bath and dried with propan 2 ol (IPA). This was done after lapping the back surface of the slice in order to protect the metal electrode during lapping.

4.3.4 Back Contact Preparation

A good electrical connection between the substrate and metal back contact is very important in device characterization. The back contact was made by evaporating gold onto the p^+ substrate by means of thermal evaporation in a conventional diffusion

† A mask with different shapes and guard rings was also used as will be discussed in the next chapter.

and rotary pump evaporator. The back of the slice may become covered with oxide during processing so that it was necessary to clean the back surface before making contacts. The back surface of the wafer was therefore lapped and etched to remove any oxide layer before gold evaporation. The details of the process are given in Appendix B.

The sample was then placed on an aluminum sample holder in the gold evaporation chamber. The sample holder also acts as a mask with two 5mm wide holes 5mm apart. A small quantity of gold of 99.999% purity, was placed in the boat. Evaporation was carried out at a pressure of 10^{-5} torr by turning on the current of 30A in the heating filament. Gold was deposited on the bare surface of the slice by opening the shutter for about 30 seconds. Two strips of gold were deposited so that the ohmic contact could be easily checked using a curve tracer. For a good ohmic contact the resistance between the two metal strips must be less than 100Ω.

4.4 CURRENT-VOLTAGE MEASUREMENT TECHNIQUE

The steady state current-voltage characteristics of the MISS are the main interest in the present study and two types of measurement technique were used, an analogue system and a computer controlled system. For some investigations only the switching and holding voltages were of interest, and they were measured easily using a Textronix curve tracer. Apart from the switching parameters, this thesis is also concerned with the negative resistance of the device which has been found to be stable if great care is taken during the measurement. The stability of the negative resistance of this device is a new phenomenon and very dependent on the external circuit.

The electrical connections to the device were made through a gold probe and a

conducting platform which provides the electrical contact to the back of the sample. A vacuum chuck was used to hold the sample firmly on the platform. The schematic diagram of the probe chamber is shown in figure 4.7.

The measurement techniques are explained in detail in the following section.

4.4.1 Analogue Measurement System

Figure 4.8 illustrates the analogue measurement system used. As will be shown in Chapter 7, it is necessary to have a high circuit resistance for stability in the negative resistance region. The MISS device was therefore connected in series with a high value of load resistance ($> 100k\Omega$), which is greater than the magnitude of the negative resistance of the device. The stray capacitance of the measurement circuit must also be as small as possible in order to stop circuit oscillation, enable the negative resistance region to be plotted, and the correct value of holding current to be measured (see section 7.2.1 in chapter 7). In the analogue system, a ramp generator and voltage multiplier were used as the voltage supply, and a Keithley electrometer Type 602 was used to measure the current.

The voltage across the device was applied to the analogue plotter through a buffer circuit. The reason of using the buffer, apart from its high input impedance, was to minimize the parasitic capacitance. The buffer circuit was designed to operate at high input voltages of up to 35 volts and this was achieved by using a high voltage buffer op-amp Type 2645. The circuit arrangement of this buffer is shown in figure 4.9. Two op-amps were used to improve the input impedance of the buffer circuit which was placed in the measuring box together with the MISS so that only a short wire was use for the electrical connection to the device and the effect of an external inteference was reduced.

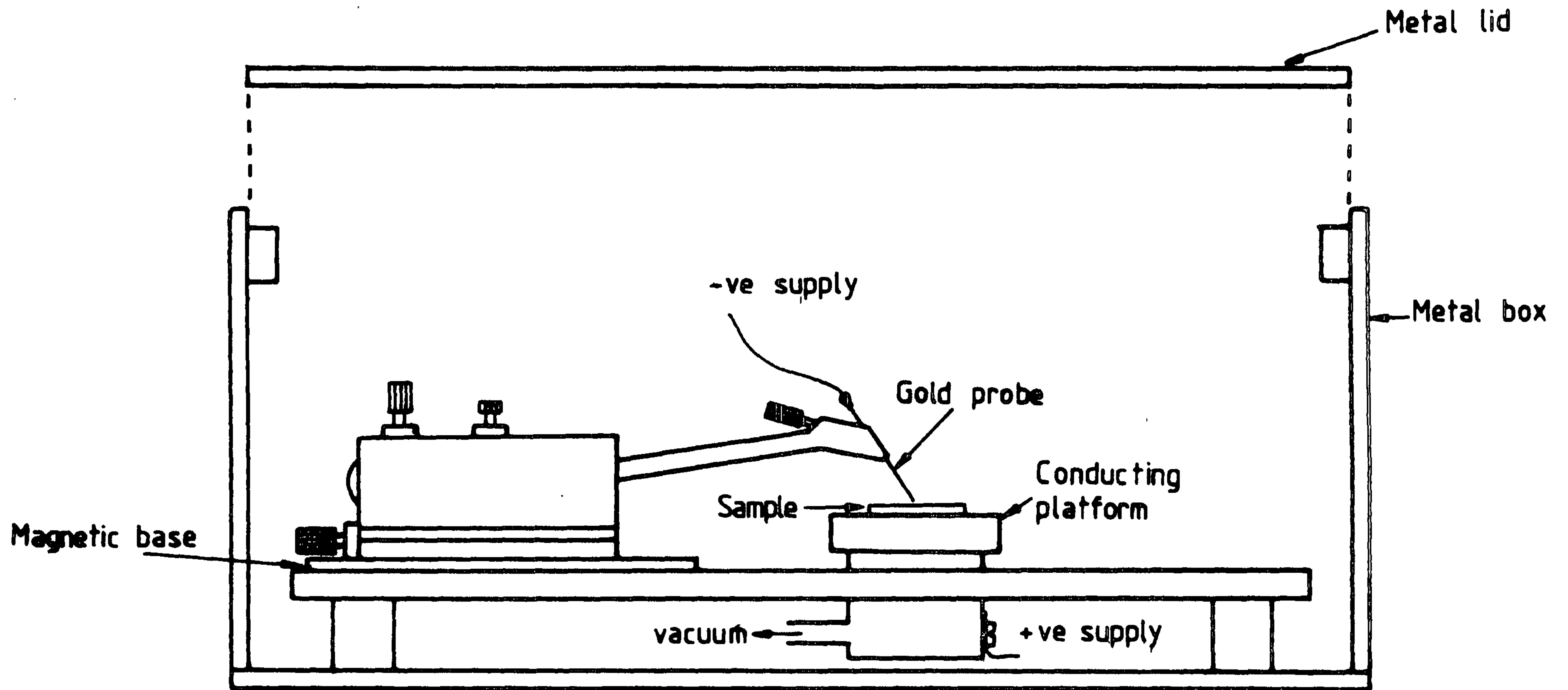


Figure 4.7 Schematic diagram of probing chamber.

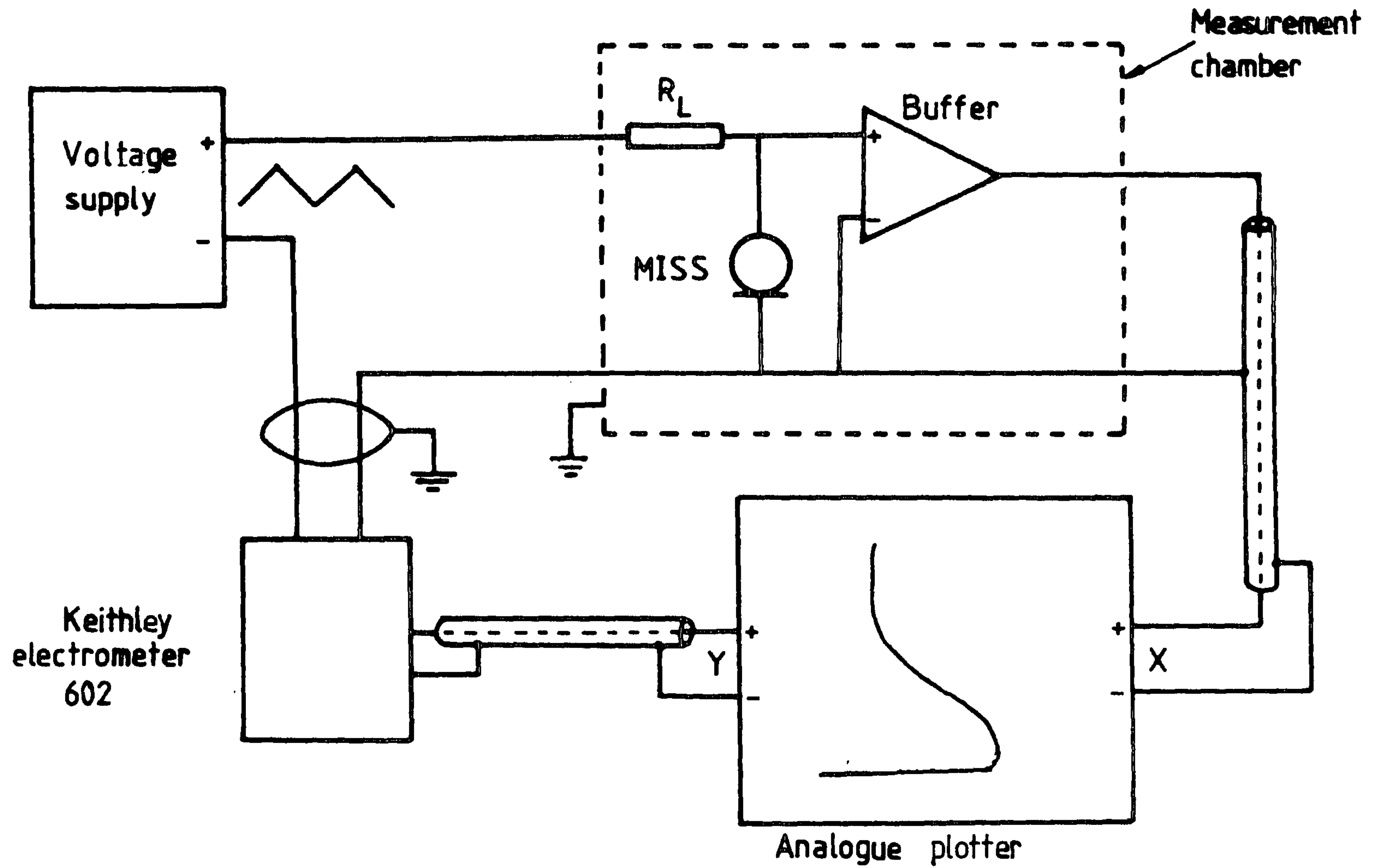
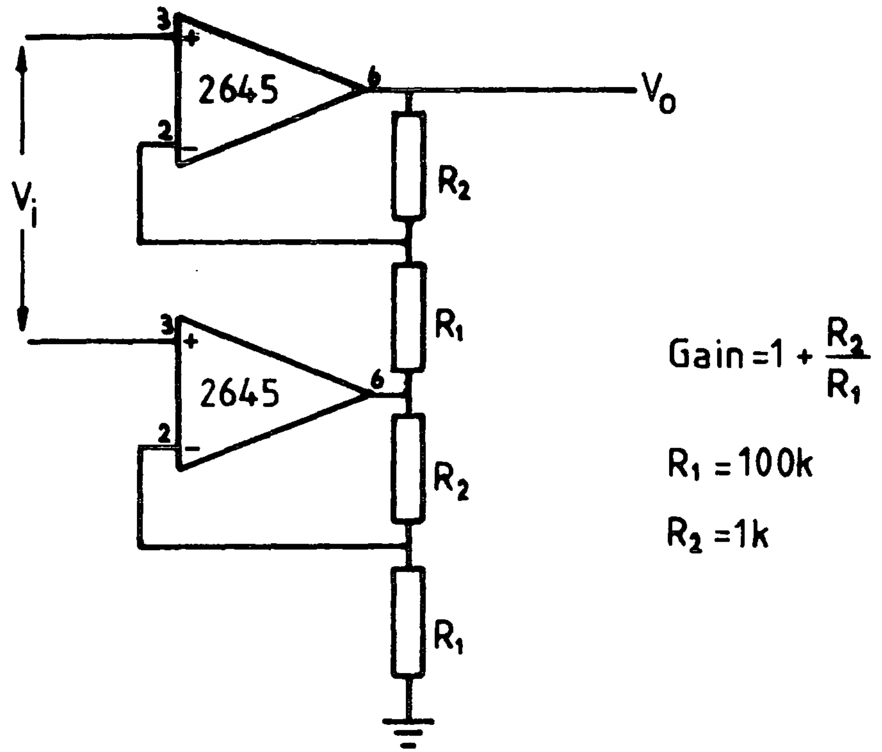


Figure 4.8 Analogue measurement system.



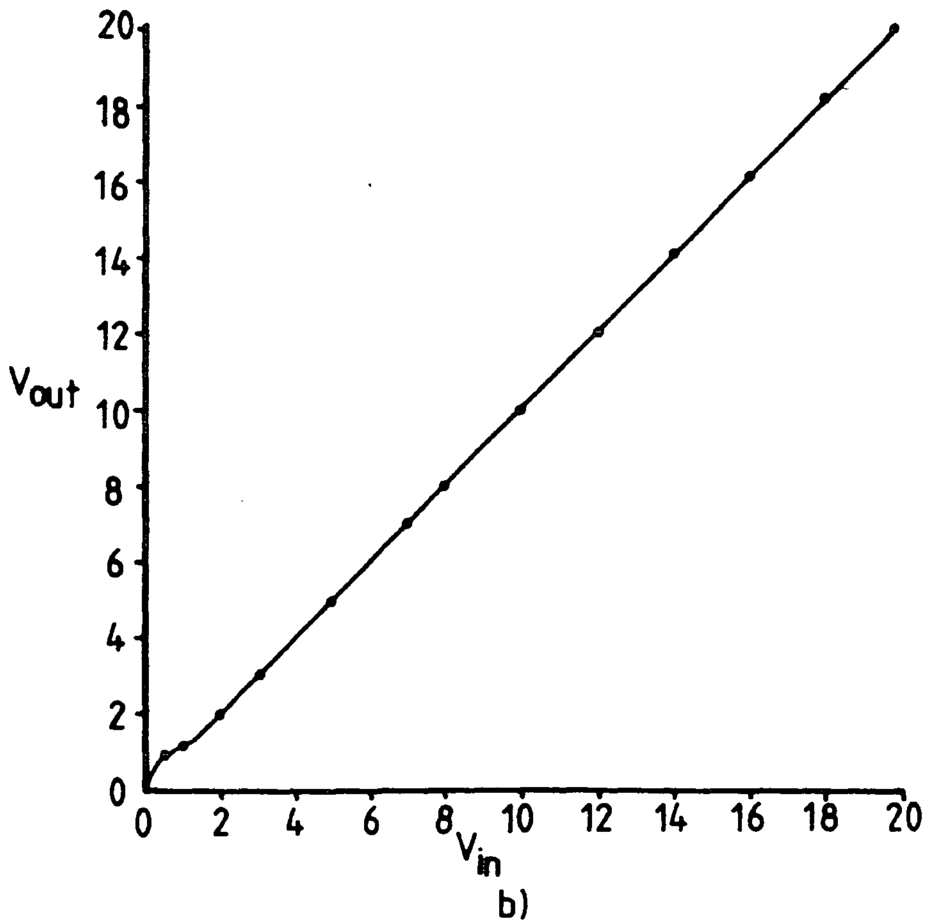


Figure 4.9 a) Circuit arrangement of high voltage buffer.
b) Transfer characteristic of the buffer.

4.4.2 Automated Measurement System

In the automated measurement system the HP9000 Series 200 Model 217 microcomputer was used as a system controller. Communication with external devices such as printer, disk drive, and measuring devices took place through the IEEE-488-1978 bus. The data and most of the commands in this standard are transmitted and received in parallel through eight data lines to which all devices are connected. There are three groups of signals on the bus, the data lines handle the bus information, and handshake and bus management lines ensure that proper data transfer and bus operation take place. Fortunately the built-in Hewlett-Packard Interface Bus (HPIB) does all the bus management functions. Any instrument can be assigned as a talker or a listener by sending an appropriate command.

The schematic diagram of the measurement system as shown in figure 4.10. Voltage steps were generated through the built-in voltage source of a Keithley electrometer Type 617 which is controlled by the computer. The maximum voltage and current which can be supplied by the 617 is limited to 100 volts and 2mA. Therefore, to obtain a high voltage supply, the output voltage was multiplied by either 25 times by using a home-made voltage multiplier circuit, or by 1000 times by using a Time Electronics Type 1013 multiplier to give output voltages of 250 or 1000 volts, so that a high load resistance could be used. The voltage drop across the device was measured using the same Keithley 617 programed to be a voltmeter, while the current was measured using a Keithley picoammeter Type 485. The measurements of current and voltage were stored on floppy-disks and they could be plotted on a Hewlett-Packard plotter.

This system was also designed to measure the switching parameters (V_s, V_h,

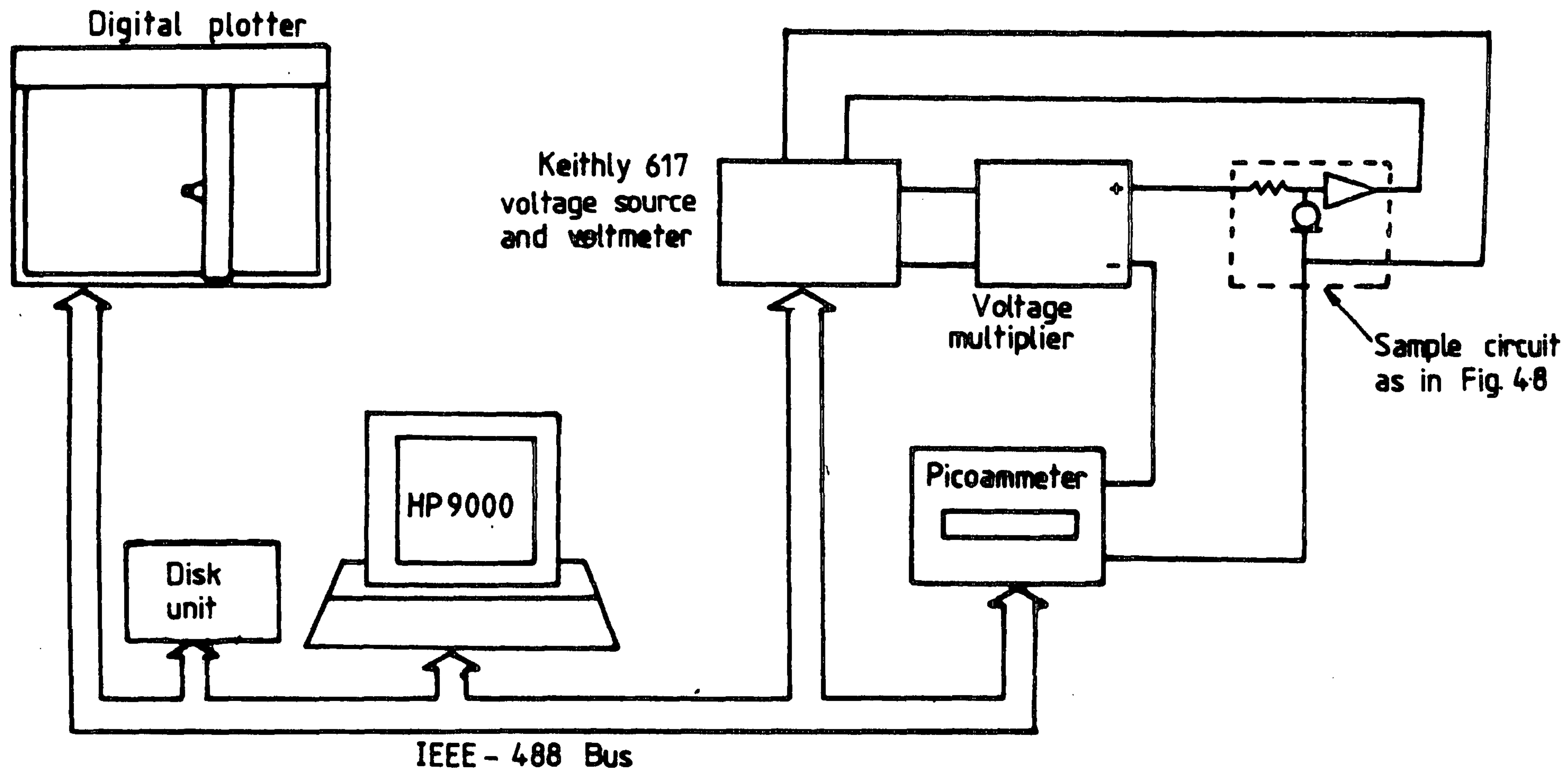


Figure 4.10 Automated measurement system.

I_o, I_s, I_h) of the devices automatically during the ramping up of the supply voltage. The switching point was detected by comparing the three consecutive readings of the voltage (V_{s1}, V_{s2}, V_{s3}) with the previous reading, (V_{so}). If all three readings are less than V_{so} then this value is considered to be the switching voltage, V_s, and the current at this point is the switching current I_s. After V_s has been detected the step voltage is increased by a factor of ten to speed up the measurement. The minimum sample voltage reached after the switching voltage is considered to be the holding point, (V_h, I_h) and these values are stored. This technique was used to measure the switching parameters of a large number of devices for the purpose of statistical analysis and histograms of the four switching parameters could be plotted. The listing of the computer program showing how the switching parameters are detected and stored is given in the appendix C.

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CHAPTER FIVE

SWITCHING CHARACTERISTICS OF THE SRO-MISS

5.1 INTRODUCTION

This chapter is devoted to the switching behaviour of two terminal SRO-MISS devices. Steady state and dynamic measurements were carried out to study the device characteristics. The results of this investigation are very important in understanding the switching and negative resistance behaviour of the device which will be discussed in detail in Chapter 7. The switching characteristic of the MISS has been found to be very dependent on various parameters such as epitaxial layer thickness, doping concentration and semi-insulating film thickness [6,10,19]. In summary, apart from the p-n junction ratio for holes and electrons, the switching behaviour of the MISS is strongly governed by the characteristic of the MIS structure which is determined by the conduction properties of the SRO and the surface hole concentration.

Although the MIS diode is not the main interest this work, a basic understanding of the electronic behaviour of the structure and the conduction mechanism in the SRO is very important. Therefore this Chapter commences with a brief study of the characteristics of the SRO-MIS diode and the following sections will be devoted to the electrical behaviour of the MISS device in various conditions.

5.2 CHARACTERISTICS OF SRO-MIS DIODES

5.2.1 Introduction

A preliminary study of the properties of metal-SRO-n-type semiconductor structures had been carried out prior to this work in order to identify the conduction mechanism of the SRO [27]. In this section the current-voltage characteristics of the SRO-MIS diode will be described. Since the diode is reverse biased for the MISS device operation, this characteristic has been investigated in more detail than that of the forward biased diode. For this purpose SRO-MIS diodes were fabricated on n-type silicon substrates with aluminum and gold as the top and back contact respectively.

5.2.2 Current-Voltage Characteristics

Figure 5.1 shows the typical current-voltage (I-V) charateristic of the metal-SRO-silicon (n-type) diode. The thickness and refractive index of the SRO films were 319$\AA$ and 2.76 respectively. As we can see, at low voltage, the current increases symmetrically in both reverse and forward bias. Since the silicon surface is in accumulation when it is forward biased, the I-V curve is determined by the conduction properties of the SRO film. At low reverse bias, the voltage is too small to form a depletion layer at the SRO-semiconductor interface. As a result the current flow through the device increases with the applied voltage. As the applied voltage rises further the semiconductor voltage becomes larger than that in the SRO layer. The total current through the MIS is then determined by the voltage division so that the current through the SRO and the generation current in the semiconductor are equal ($J = J_{SRO} = J_g$).

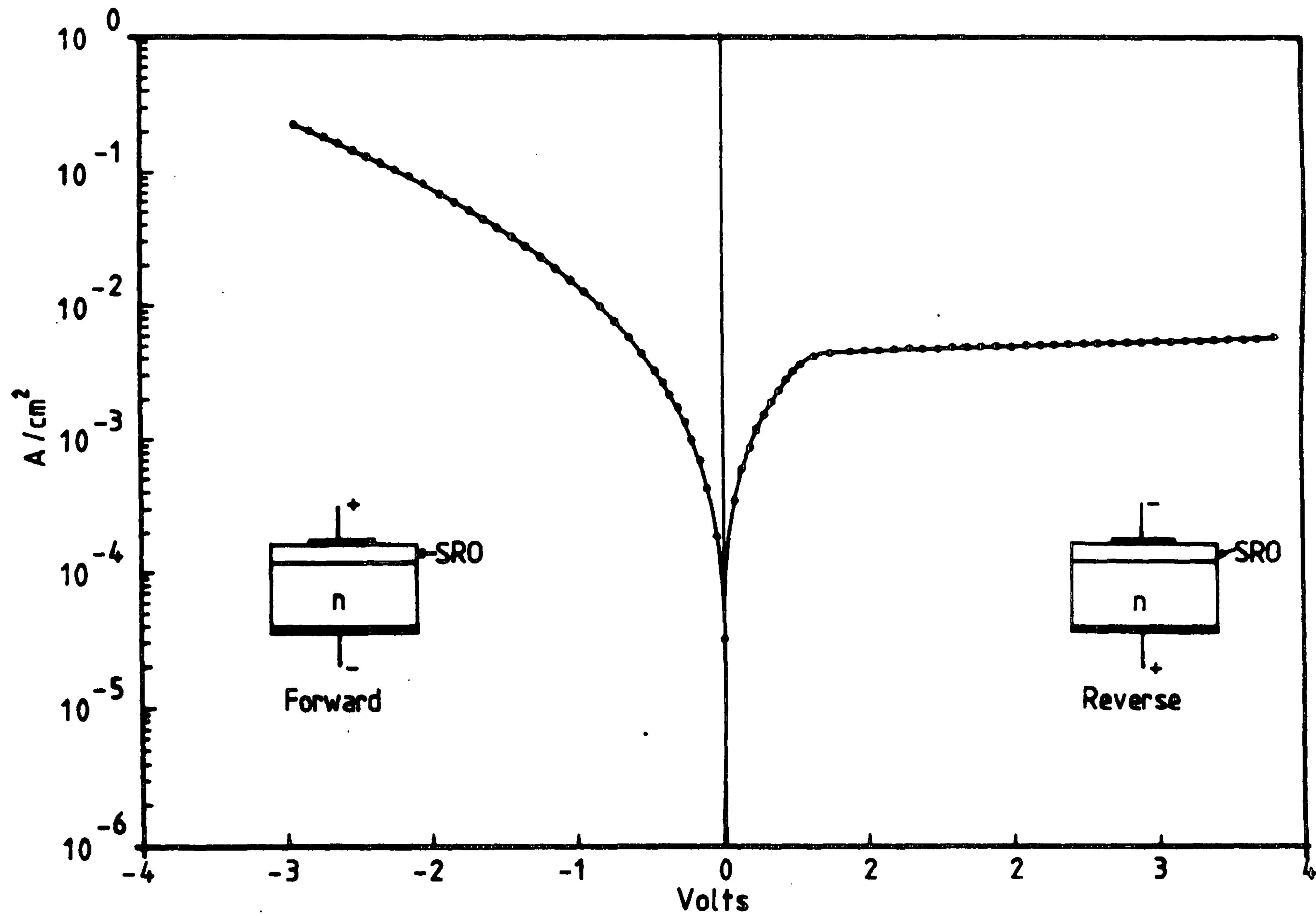


Figure 5.1 I-V characteristics of the Metal-SRO-Semiconductor(n-type), SRO type (d=319$\mathring{A}$, n=2.78).

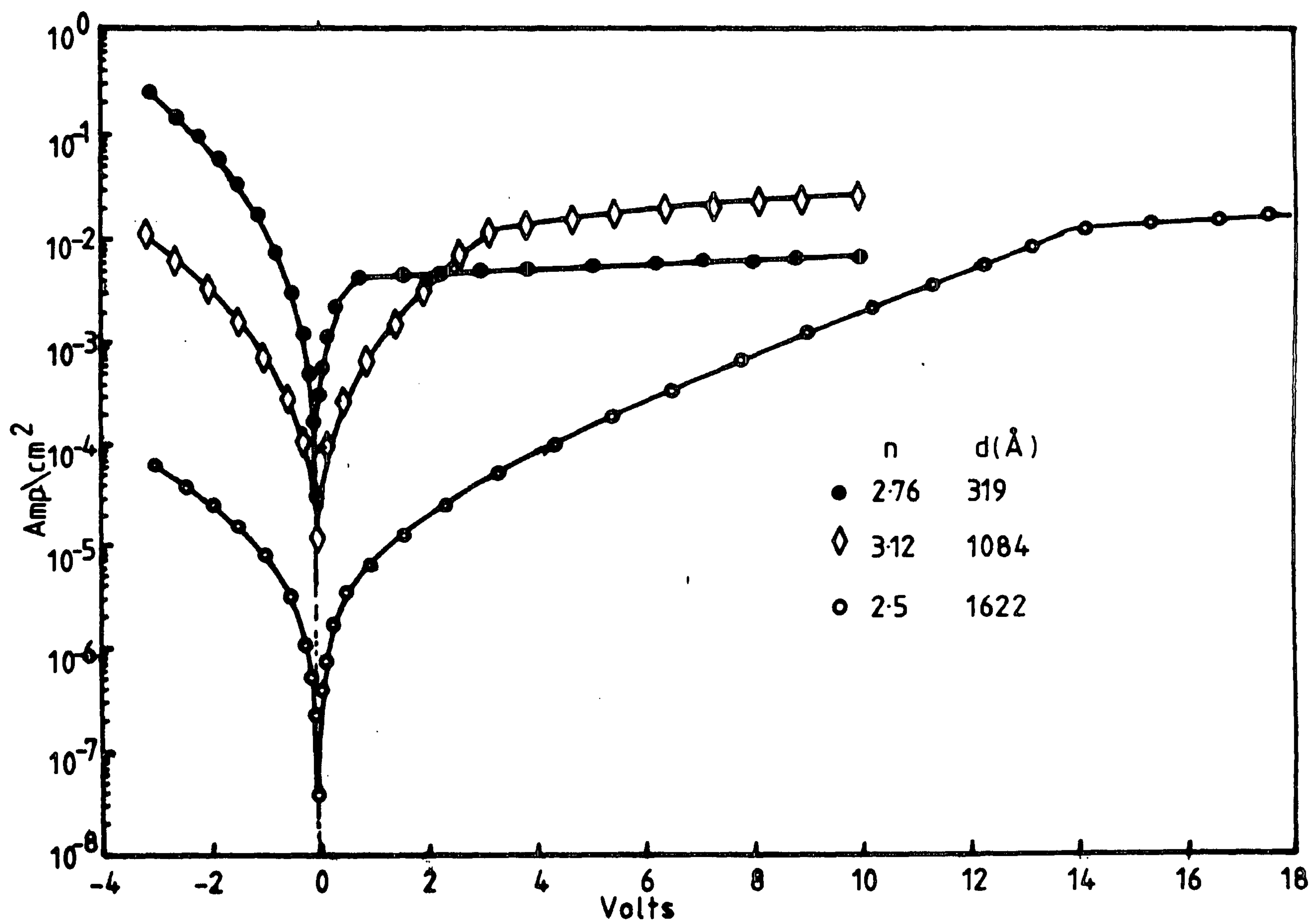


Figure 5.2 I-V characteristics of the SRO-MIS with different types of SRO.

Increasing the reverse bias voltage beyond a certain point the current flow becomes limited by the generation current in the semiconductor, and this condition is known as a semiconductor limited state (SLS). The voltage at which the semiconductor limited state takes place (reverse saturation voltage) depends on the conduction properties of the SRO films. When the SRO is less conductive a higher voltage has to be applied for the current to reach the saturation limit. Generally, the thicker the SRO layer the higher the voltage for SLS as clearlly demonstrated in figure 5.2. The differences in the reverse saturation currents were probably due to slight differences in doping density of the n-type substrates of the samples used.

Since the forward bias current is governed by the SRO type, then as we can see, when the SRO become more conductive, the current increases more rapidly with voltage. Figure 5.2 clearly shows that the thickness and refractive index of the SRO are the two important parameters which determine the conduction of the films. At a constant thickness, the conductivity of the SRO increases with refractive index, corresponding to the increase in silicon content.

5.2.3 Effect of Illumination

The rate of supply of holes can be increased by shining light on the sample with $h\nu > E_g$, the energy gap of the silicon. This experiment was carried out using a microscope lamp as a light source whose intensity could be varied. A light meter was used to measure the intensity in lux. Some of the incident light is absorbed in the depletion region where it creates electron-hole pairs which effectively increase the generation current. The electron-hole pairs are produced by the incident light at a rate $G(x)$ given by [3],

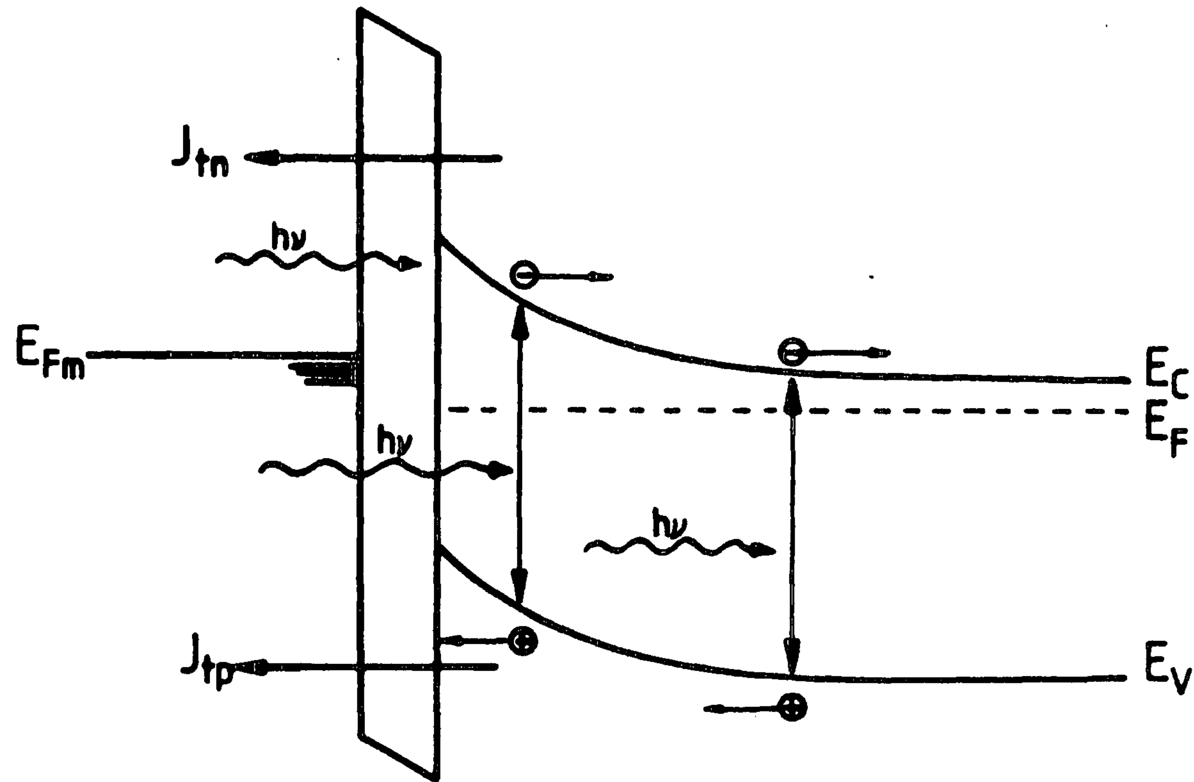


Figure 5.3 The energy band diagram of the MIS with light illumination.

$$G(x) = \Phi \varphi_o \alpha \exp(-\alpha x) \qquad 5.1$$

where Φ is the effective quantum efficiency which is the number electrons generated when one photon of that wavelength is incident upon it, φ_o is the total incident photon flux per unit area per second (photons/cm^2 s), and α is the absorption coefficient in cm^{-1}. Both Φ and α are functions of optical wavelength and the semiconductor material [3]. Figure 5.3 shows the energy band diagram of the MIS under light illumination. Figure 5.4(a) shows the variation of the reverse bias current of an SRO-MIS of electrode size 1.55mm^2 with light intensity. As the light intensity(lux) increases the reverse saturation current increases. The increase of reverse saturation current with light at a constant voltage is not linear for high illumination as shown in figure 5.4(b). Initially the voltage and hole current across the SRO will be the same as before, that is less than the supply rate of holes. The electron-hole pairs created by light increase the charge in the inversion layer and this increases the voltage across the SRO. This causes a voltage redistribution between the SRO and depletion region where the voltage drop in the SRO increases with a decrease in the voltage across the depletion region. Increasing the voltage across the SRO, and hence the electric field, enhances the hole current through the SRO until it is equal to the supply rate of holes and a new equlibrium steady-state condition is reached. As a result of the high electric field across the SRO layer there will be a higher injection of electron current into the semiconductor, and hence the total current across the MIS is higher than that without incident light. At a higher illumination the rate of supply of holes is high so that the surface concentration is increased. As a result the voltage drop across the SRO increases further, decreasing the width of the surface depletion region and hence reducing the generation current. Therefore, the current through the structure is not linear with illumination as initially expected.

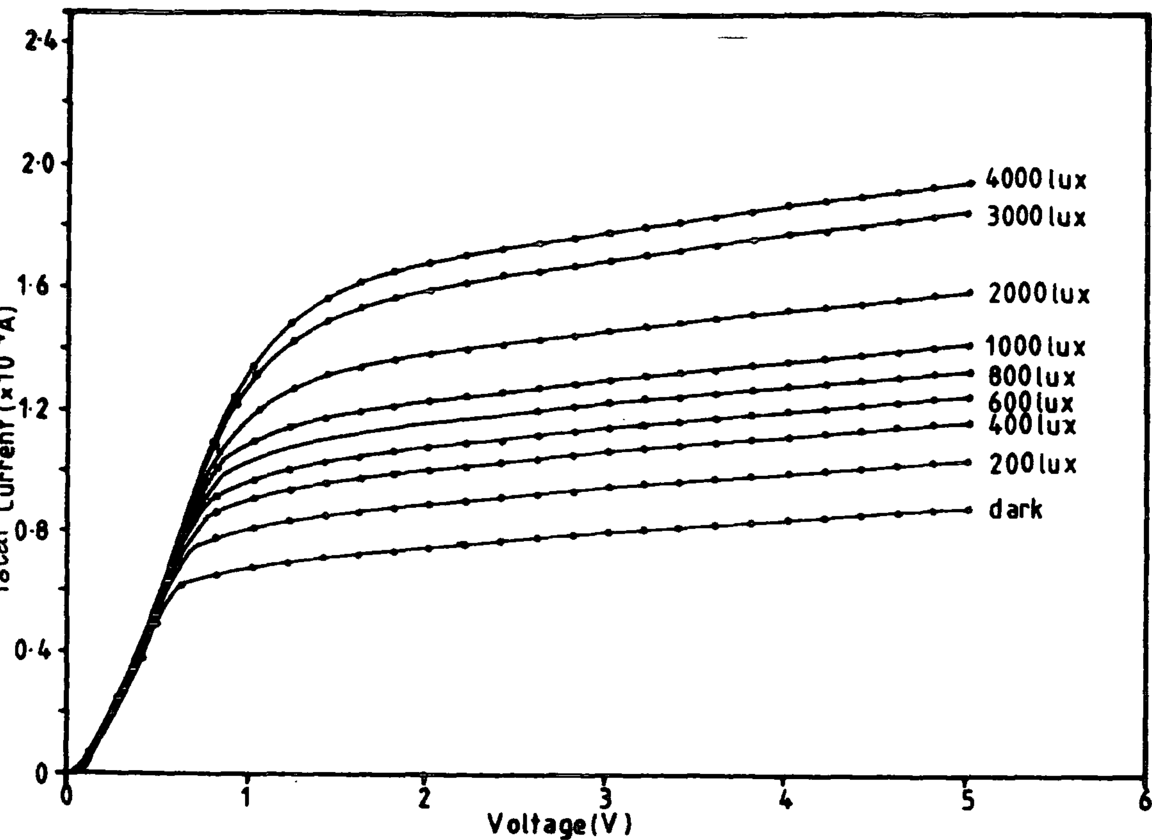


Figure 5.4 a) The reverse saturation current of the SRO-MIS illuminated with different light intensity. (Electrode area = 1.55mm^2, SRO type (d=319$\AA$, n=2.78).

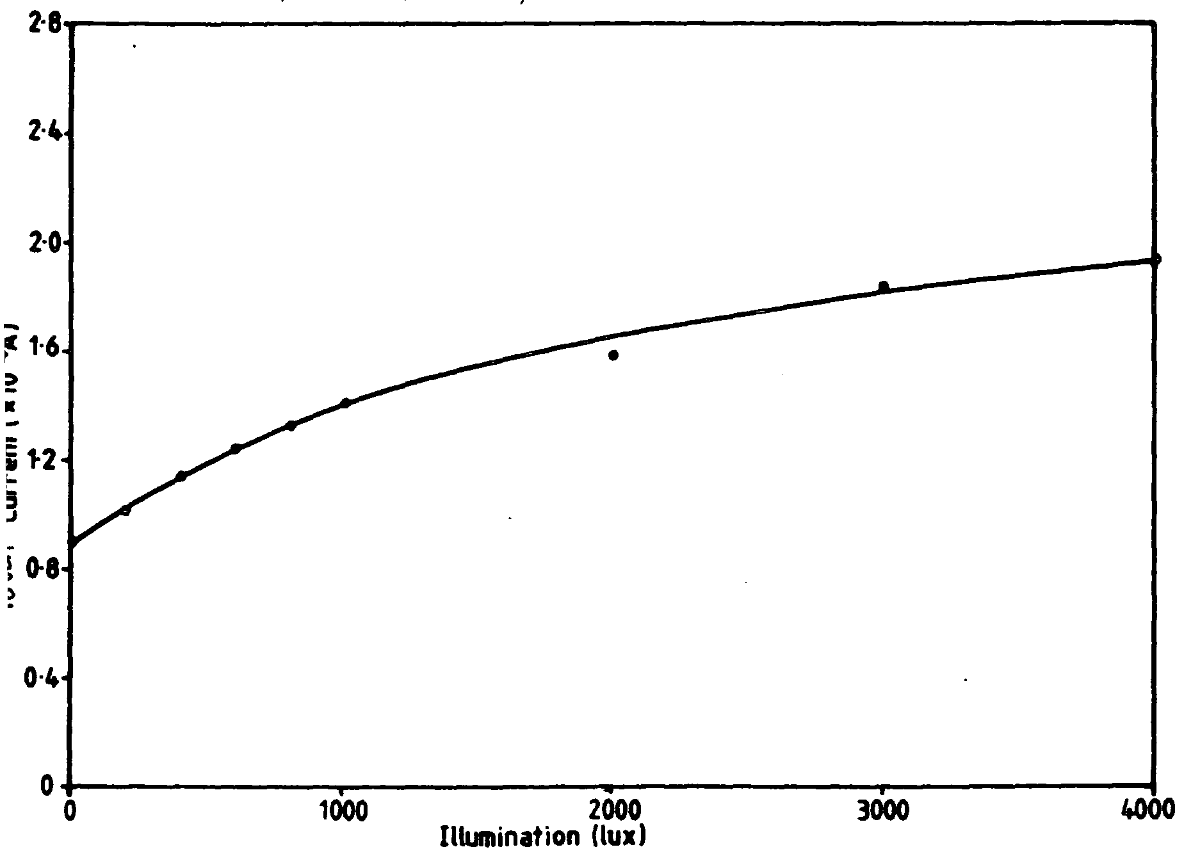


Figure 5.4 b) The reverse saturation current of the SRO-MIS at constant voltage as a function of illumination.

MIS devices with a different type of SRO were illuminated with the same light intensity and found to give different reverse saturation current. The SRO160 (index of refraction, n= 2.24, and thickness, d=178$\AA$) gives a total current of 190μA when illuminated under 600 lux of light and biased at 6 volts, whereas SRO122 (n=2.76, d=319$\AA$) gives only 128μA. This shows that the sensitivity of MIS to light depends on the type of SRO. Since the SRO122 film is less conductive than SRO160, the rate of which holes can pass through the layer is less, and hence the surface concentration of holes is higher. As a consequence, the voltage droppd in the SRO122 layer is greater than in SRO160. This result in a higher depletion layer width and hence generation current for the MIS with the SRO160 type of film.

Another factor which might contribute to this behaviour is that the SRO film becomes less transparent and its reflectance increases as the thickness and refractive index increase [25]. Thus fewer photons can reach the semiconductor, and a smaller number of electron-hole pairs are created. The MIS with the SRO122 layer would have a total reverse saturation current at a constant voltage which is smaller than with the SRO160.

5.2.4 Effect of Work Function Difference

In order to study the effect of work function on the MIS characteristics aluminum and gold electrodes were deposited on the same wafer using a metal mask since photolithography could not be used because gold does not stick very well to SRO * and wet processing causes the gold to come off the surface during the washing procedure. Figure 5.5 shows the reverse bias I-V characteristic of the MIS with aluminum and gold electrodes. Both were the same size (0.47 mm^2) and the thickness and refractive index of the SRO are 300$\AA$ and 2.9 respectively. As can be seen, the current for the

* This is probably because of gold has less affinity to oxide and SRO

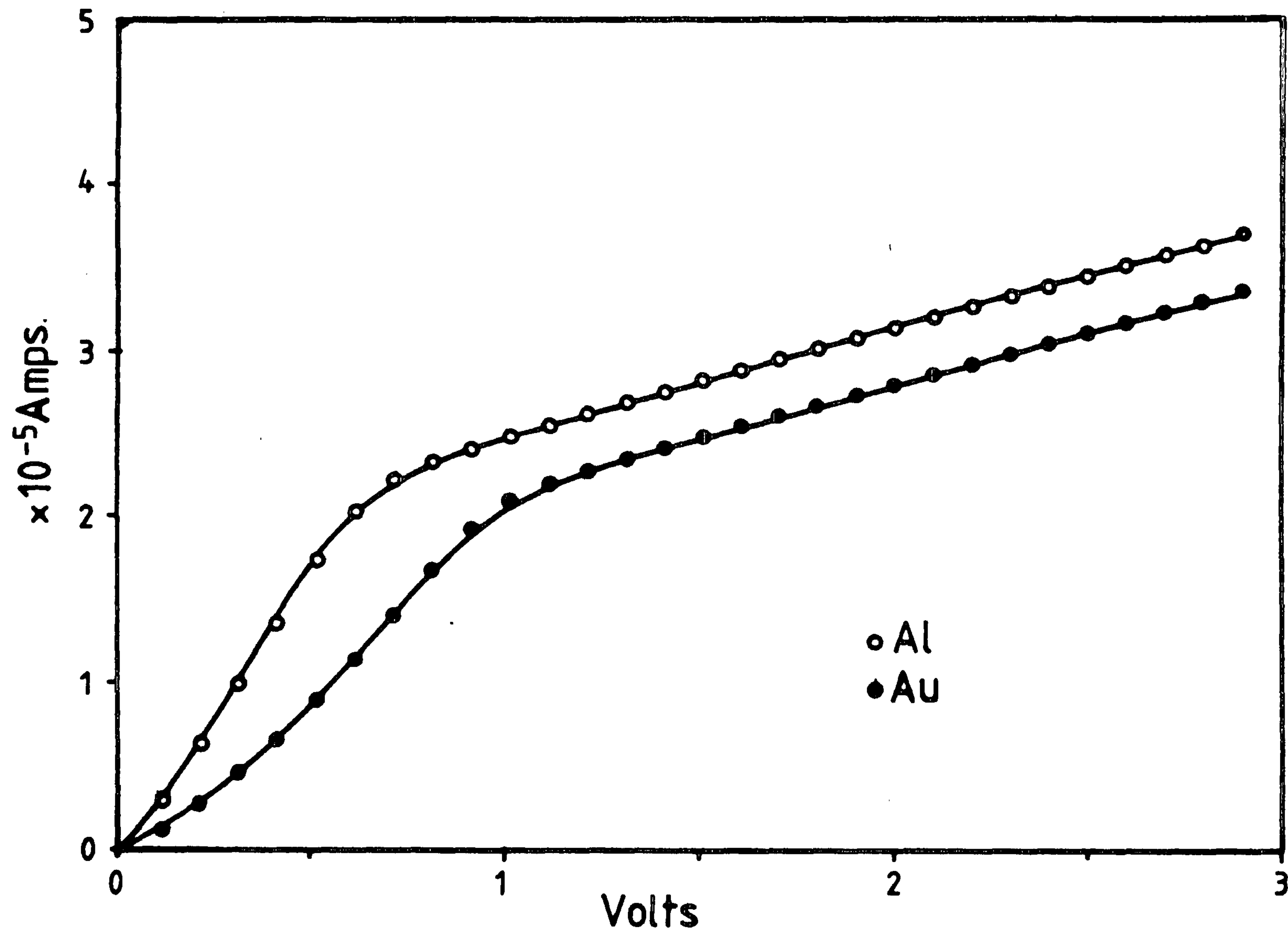


Figure 5.5 I-V characteristics of Al-SRO-n type and Au-SRO-n type in reverse bias. The area of both electrodes $=0.47\text{mm}^2$, SRO type ($d=300\mathring{A}$ and $n=2.9$).

aluminum electrode MIS is a little higher than the current for the gold electrode.

Since the gold work function is higher than that of the aluminum, a higher voltage is needed to lift the Fermi energy level to the same point as for the aluminum electrode so that the same amount of current can flow. Thus, the reverse current of the MIS with the gold electrode begins to saturate at a higher voltage than with the aluminum electrode. That is to say, the reverse saturation current of the Au-SRO-n is lower than for the Al-SRO-n at the same applied voltage. Bolt and Simmons have also found that the SIPOS-MIS with a gold electrode gives a lower value of the saturation current [21].

The reverse saturation current flowing through the MIS structure is a generation current given by

$$J_g = C_n \psi_s^{1/2} \qquad 5.2$$

where

$$C_n = \frac{n_i}{\tau_o}\left(\frac{2\epsilon_s}{2N_d}\right)^{1/2}$$

The voltage across the SRO-MIS can be written as

$$V = V_{SRO} + V_{FB} + \psi_s \qquad 5.3$$

where V_{SRO} is the voltage drop in the SRO layer and V_{FB} is the flat band voltage given by

$$V_{FB} = \phi_{ms} - \frac{Q_i}{C_i} \qquad 5.4$$

where ϕ_{ms} is the work function difference, Q_i is the interface charge per unit area and C_i is the semi-insulator capacitance per unit area. In terms of voltage division the surface potential can be written as

$$\psi_s = V - V_{SRO} - V_{FB} \qquad 5.5$$

At the same reverse saturation current for devices with Au and Al electrodes the surface potential must be the same. Hence, from equation 5.2 and 5.5

$$V_1 - V_{FB_1} = \left(\frac{J_g}{C_n}\right)^2 \qquad 5.6$$

for the aluminum electrode, and

$$V_2 - V_{FB_2} = \left(\frac{J_g}{C_n}\right)^2 \qquad 5.7$$

for the gold electrode where V_1 and V_2 are the voltages across the Al-SRO-n and Au-SRO-n respectively. The difference in voltage is

$$V_2 - V_1 = V_{FB_2} - V_{FB_1}$$

$$= \phi_{ms_2} - \phi_{ms_1} \qquad 5.8$$

where ϕ_{ms_2} and ϕ_{ms_1} are the work function differences for Au-SRO-n and Al-SRO-n respectively. Therefore the voltage required to give the same generation current for Au-SRO-n is ($\phi_{ms_2} - \phi_{ms_1} = 0.5$ volts) higher than that of Al-SRO-n. This value agrees with the result shown in figure 5.5 for a reverse current of 2.5×10^{-5}Amps.

This experiment shows that the current flow through both types of diode is governed by generation but it is also influenced by the metal contact. Since the MISS behaviour is governed by the MIS characteristics, the work function difference will also affect the I-V characteristics of the MISS.

5.3 TWO DIMENSIONAL EFFECTS IN SRO-MISS DEVICES

5.3.1 Introduction

For any integrated circuit application MISS devices have to be reasonably small in order to be competitive with the present VLSI technology. The tunnel oxide MISS

device has been found to be geometrically dependent [11,12], and the reason has not been clearly understood. Therefore the present investigation was intended to be more comprehensive for SRO-MISS devices and various structures were fabricated at both Durham and Southampton Universities. The studies on the two dimensional effects are divided into four groups to find the effects of electrode area, electrode perimeter or shape, junction area and guard ring voltage respectively.

5.3.2 Effect of Electrode Area - Large Devices

To investigate this effect, MISS devices with different sizes of aluminum electrode were fabricated on the same wafer with no isolation between them. The smallest and the largest circular electrodes were 0.41 and 2.73mm^2 area respectively. The switching voltage generally falls with area and for large areas it may become less than the holding voltage so that the device shows no switching at all. The switching behaviour also depends on the film composition. A series of fabrication runs using SRO films with different compositions was carried out in order to obtain the most suitable films for the purpose of this study. For studying the area effect it was preferable to obtain switching for all sizes of electrode. The peformance of the devices with different SRO types is summarized in table 5.1.

Figure 5.6 shows comparative I-V plots of the MISS devices of different sizes for sample SRO157 with a film thickness of 304$\mathring{A}$ and refractive index of 2.9. It shows, that as the area increases, the switching voltage, V_s, decreases, and for a very large electrode a p-n junction like characteristic can be observed equivalent to $V_h > V_s$. On the other hand, as the area decreases, V_s increases, and the holding voltage increases slightly.

Table 5.1: Switching peformance with different types of SRO

	CVD condition			Ellipsometry		Devices Sizes for switching						
Run no.	R_o	t(min)	T(^{o}C)	n	d($\AA$)	A	B	C	D	E	F	G
SRO123	0.25	1.0	650	2.5	275	X	X	X	S	S	S	S
SRO124	0.21	1.0	650	2.7	276	X	X	X	X	S	S	S
SRO155	0.15	1.5	650	3.1	310	X	X	X	S	S	S	S
SRO156	0.13	1.0	650	2.4	199	X	S	S	S	S	S	S
SRO157	0.10	1.0	650	2.9	304	S	S	S	S	S	S	S
SRO158	0.10	0.6	650	< 1.5	100	S	S	S	S	S	S	S
SRO159	0.10	0.8	650	2.4	194	X	X	X	X	S	S	S
SRO182	0.09	1.0	650	2.8	241	S	S	S	S	S	S	S

where,

A $= 2.36\text{mm}^2$ E $= 0.59\text{mm}^2$ X≡ Does not Switch (p-n junction like)

B $= 1.55\text{mm}^2$ F $= 0.37\text{mm}^2$ S≡ Switch, $V_s > V_h$

C $= 1.12\text{mm}^2$ G $= 0.18\text{mm}^2$

D $= 0.89\text{mm}^2$

The variation of the switching and holding voltages with electrode area is shown in figure 5.7, and the corresponding switching and holding currents are shown in figure 5.8. The switching process is generally controlled by the hole generation in the surface depletion region. High value of V_s for some of the samples may be due the to punch-through switching mechanism which occurs when the surface depletion layer reaches the p-n junction depletion layer. The punch-through voltage is

$$V_s = \frac{qN_d}{2\epsilon_s}(W_n - W_j)^2 \quad 5.9$$

where W_n is the n-type epilayer thickness, W_j is the p-n junction depletion width and

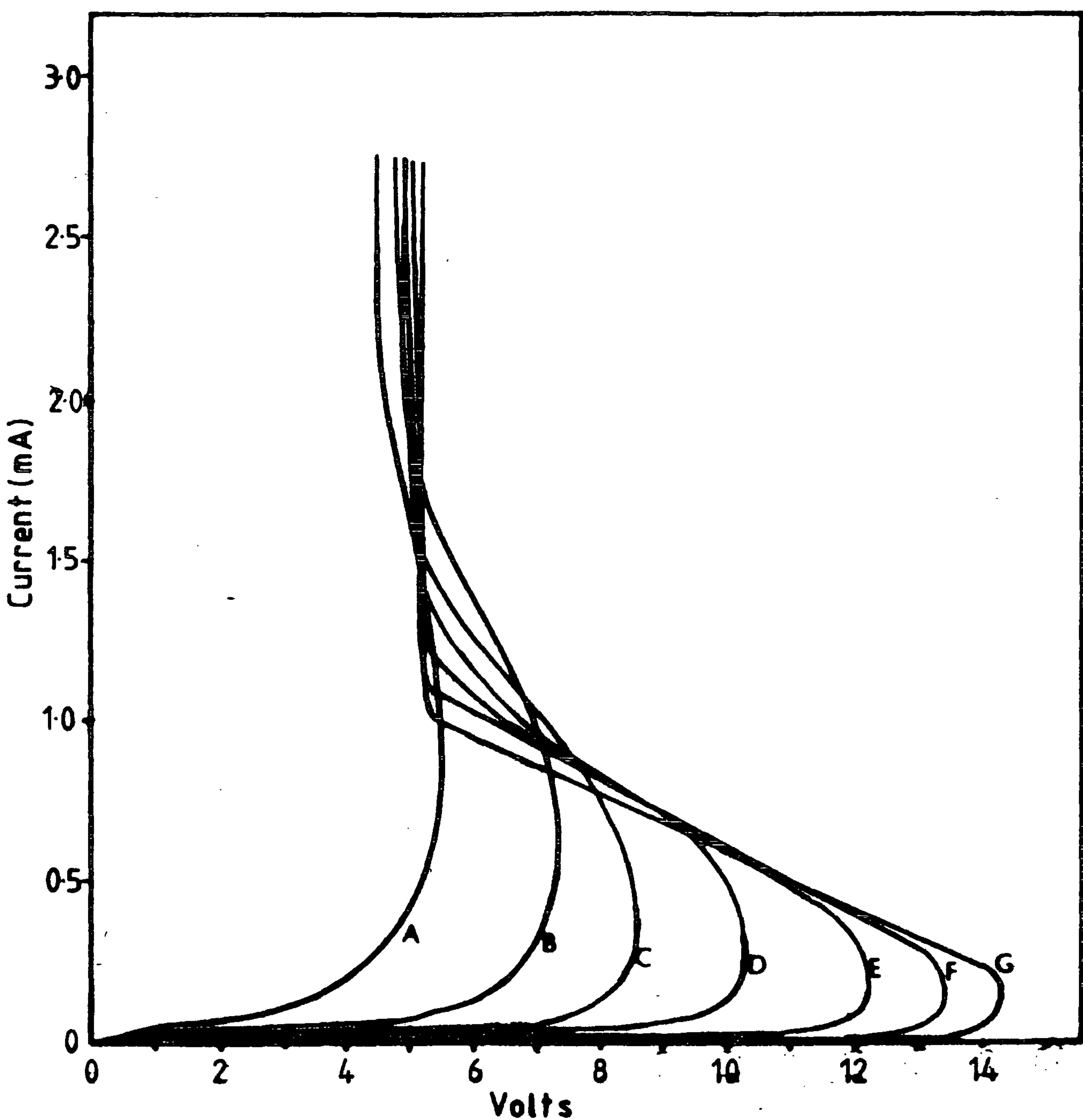


Figure 5.6 Comparative I-V plots illustrating the effects of electrode area for non-isolated SRO-MISS device (sample SRO157). A=2.36mm^2, B=1.55mm^2, C=1.12mm^2, D=0.89mm^2, E=0.59mm^2, F=0.37mm^2 and G=0.18mm^2.

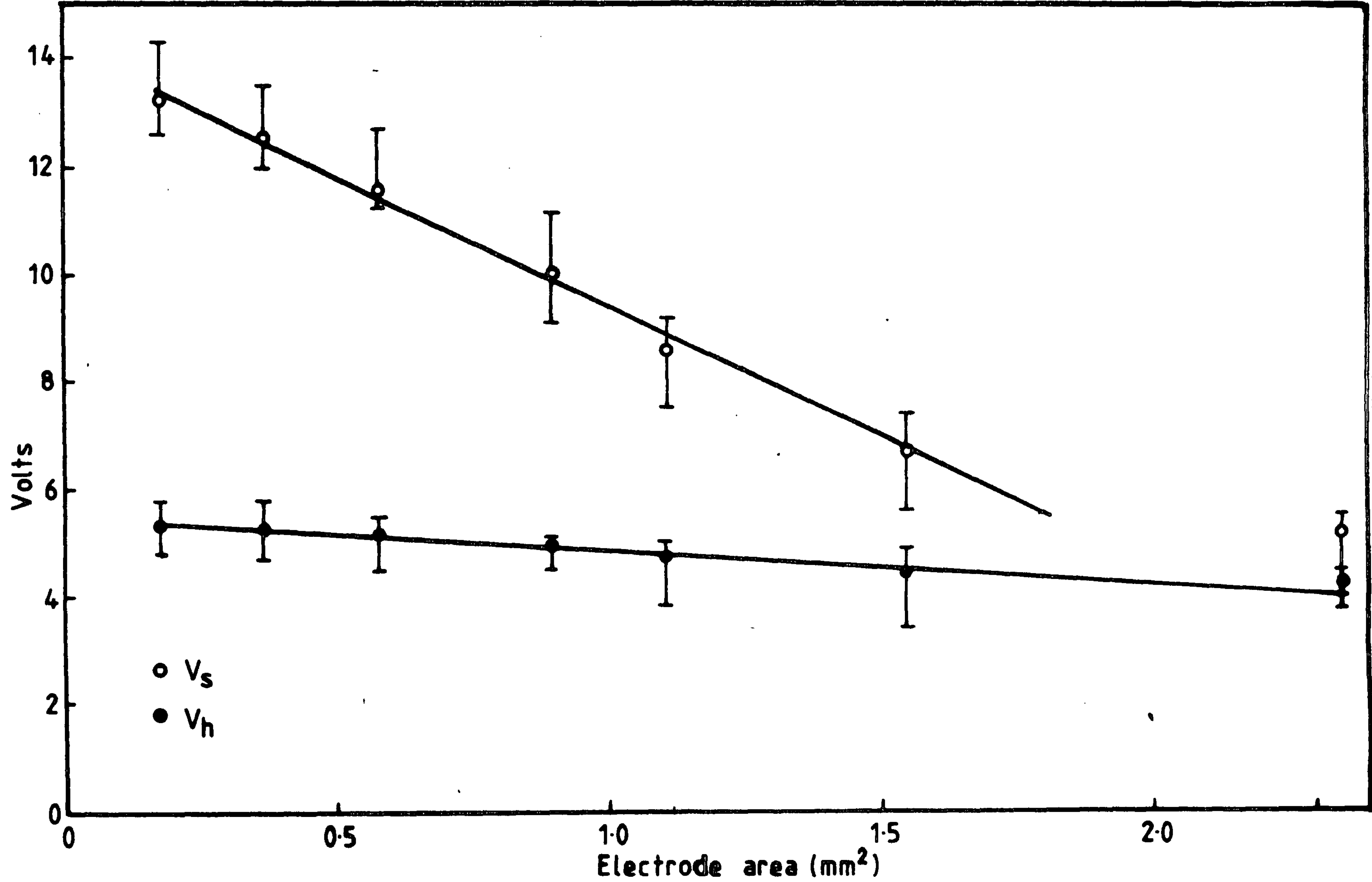


Figure 5.7 Variation of the switching and holding voltages with electrode area (sample SRO157).

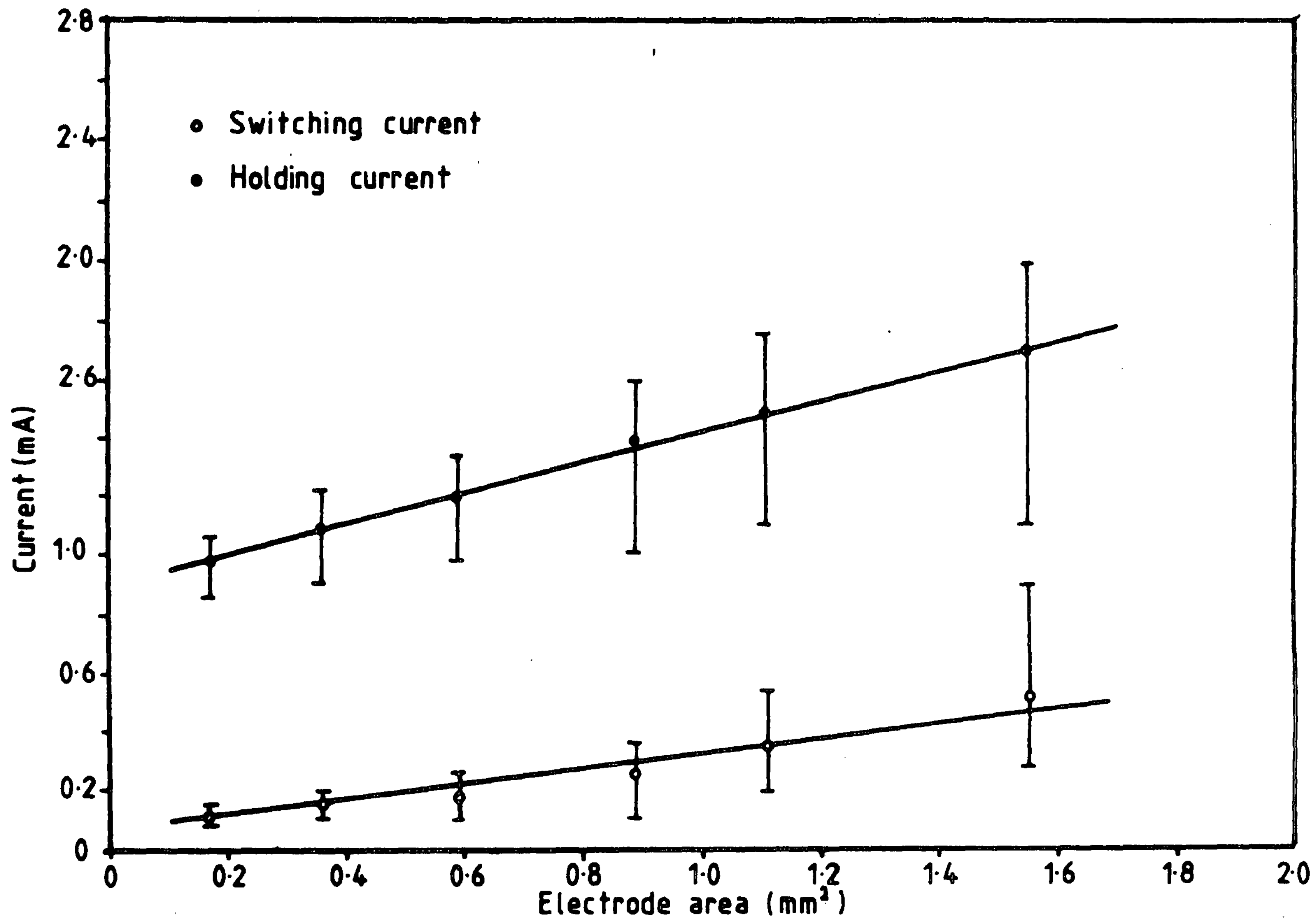


Figure 5.8 Variation of holding and switching currents with electrode area (sample SRO157).

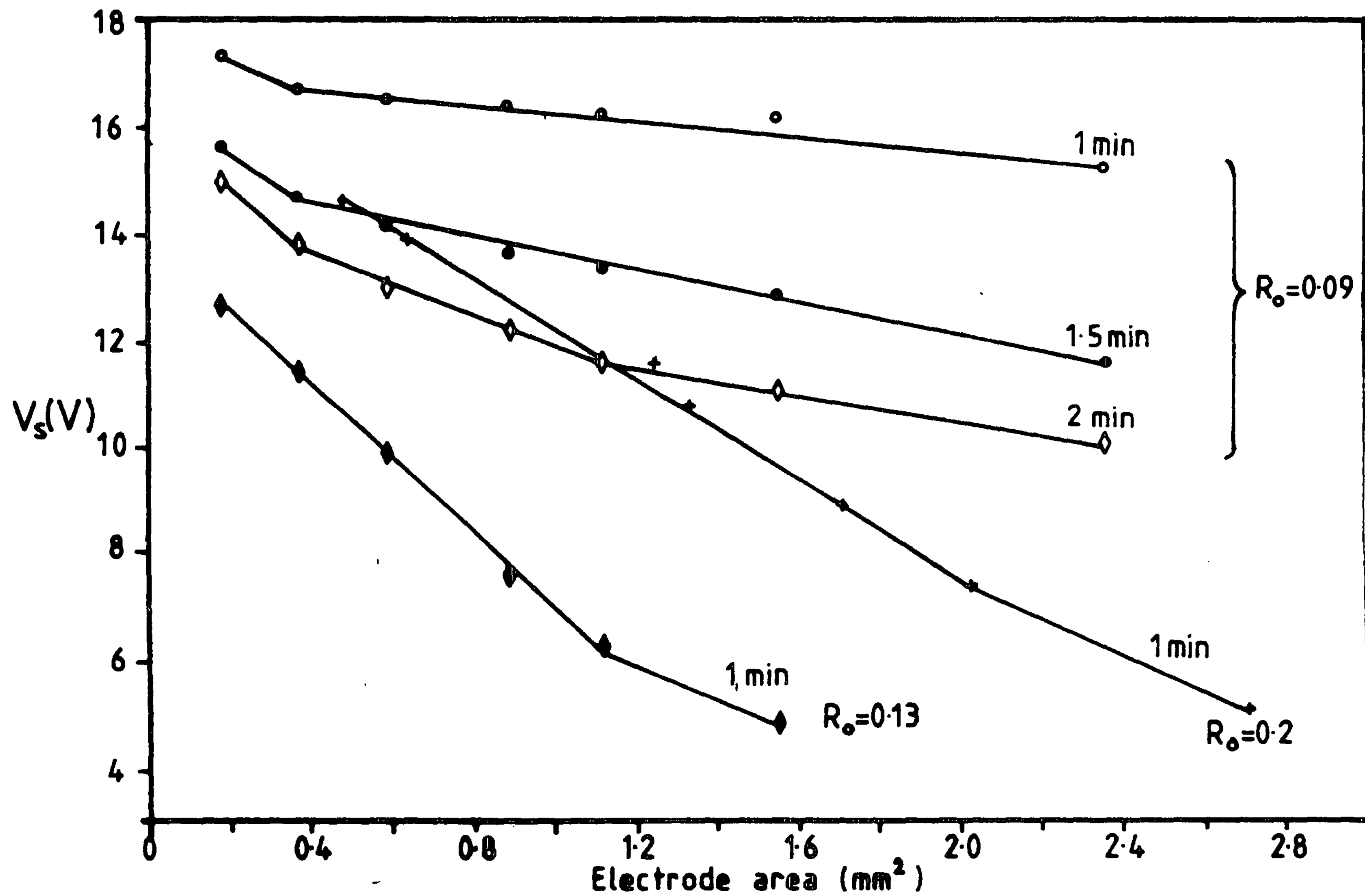


Figure 5.9 Variation of switching voltage V_s with electrode area for a different type of SRO.

N_d is the doping density of the epilayer. For the samples used in this experiment the calculated punch-through voltage is about 20 volts. The increase of V_s as the device size decreases will therefore be limited to the punch-through voltage.

The area dependence of the switching parameters is also governed by the conduction of the SRO films, ie. the composition and the thickness. This behaviour has also been found to occur in a tunnel-oxide MISS where the area dependence is governed by the oxide thickness [11]. The variation of switching voltage with area for different types of SRO film is shown in figure 5.9. As we can see, for a constant phase ratio, R_o, of the reactant gases the sensitivity of the area dependence of the switching voltage ($S_v = \Delta V_s / \Delta A$), increases with deposition time and for a constant deposition time, S_v increases as R_o increases. The area dependence therefore varies with the SRO composition, and the conduction of the films. It seems to be that for the less conductive film the higher is the sensitivity to area. As discussed in the previous Chapter the composition of the film is very difficult to control or estimate because it was critically dependent on the CVD parameters.

A similar investigation has also been carried out by Duncan and Tonner [11] for tunnel-oxide MISS samples with a square electrodes. They explained the dependence of switching voltage with area as due to a current fringing effect which becomes dominant when the electrode dimension is of the order of the epitaxial layer thickness. However in our investigation the area dependence is dominant even if the electrode size is 100 times greater than the epitaxial thickness. In spite of this it is believed that the area dependence of the switching parameters is still due to the current spreading in the device structure.

Current spreading will occur in a semiconductor structure if one of the terminals is much smaller than the other. In the MISS it is due to the fact that the p-n junction voltage cannot fall to zero suddenly at the electrode edge as shown in figure 5.10.

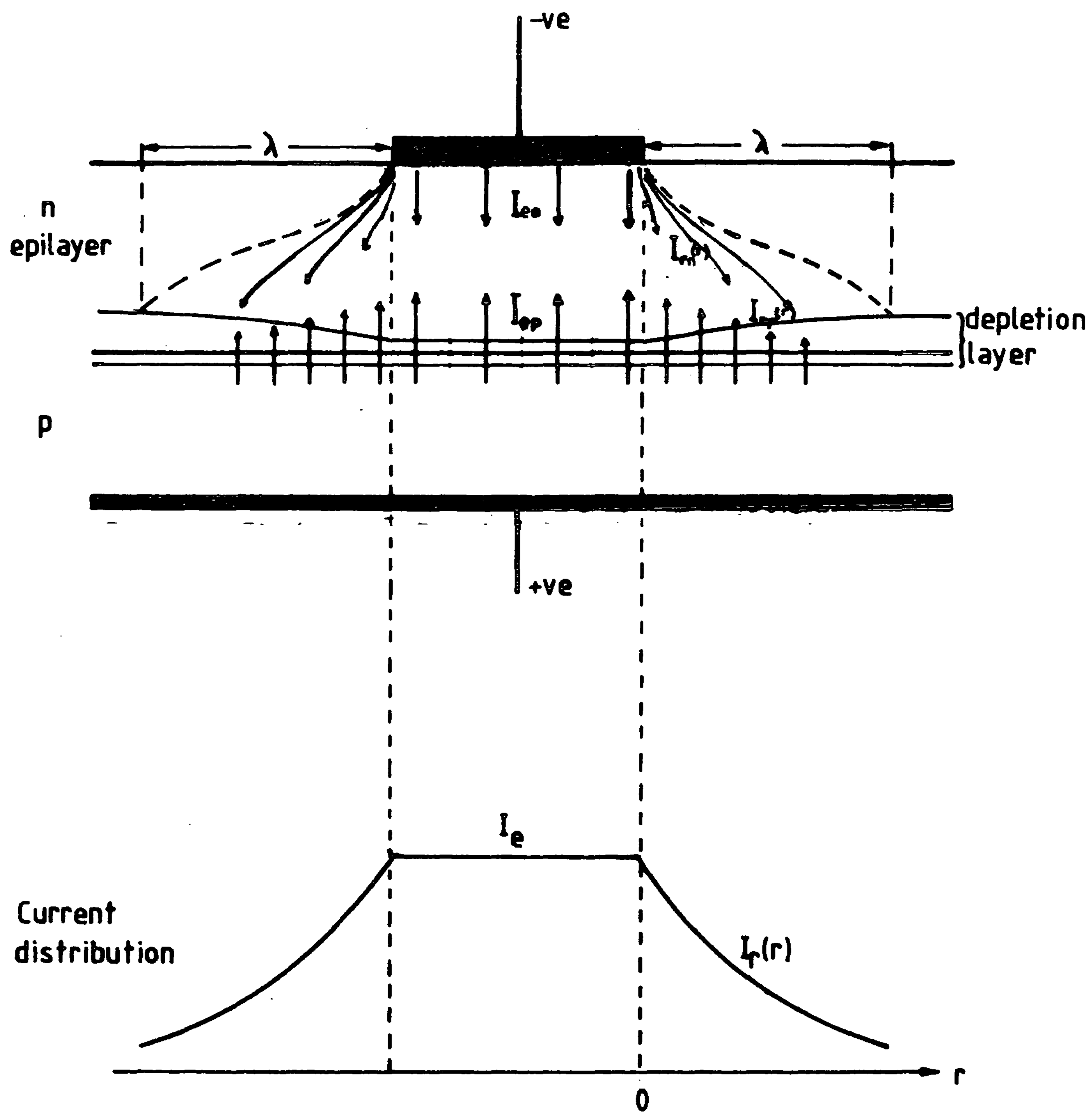


Figure 5.10 Current spreading in the p-n junction.

Hence there is a lateral electron flow in the epilayer and a lateral fall of voltage because of the resistivity of the material which has also been explained for a laser diode structure [14]. The total current flowing through the p-n junction can be written as,

$$I_t = I_{e_p} + I_{e_n} + I_{r_p}(r) + I_{r_n}(r)$$

$$I_t = I_e + I_r(r) \qquad 5.10$$

where $I_{e_p}(I_{e_n})$ is the uniform hole(electron) current under the electrode, and $I_{r_p}(r)$ and $I_{r_n}(r)$ are the total hole and electron spreading current respectively. The current through the elemental section dr is

$$dI_r(r) = dI_f(r) + dI'_f(r) \qquad 5.11$$

where

$$dI_f(r) = I_s \exp\frac{qV_j(r)}{kT}dr \qquad 5.12$$

and the recombination current

$$dI'_f(r) = I'_s \exp\frac{qV_j(r)}{2kT}dr \qquad 5.13$$

where I'_s depends on the quality of the epilayer. Therefore the total spreading current for a distant λ from the edge of electrode is

$$I_r(\lambda) = \int_0^{\lambda} (I_s \exp\frac{qV_j(r)}{kT} + I'_s \exp\frac{qV_j(r)}{2kT})dr \qquad 5.14$$

Therefore, the total current of each diode is controlled by the spreading current which has been shown to increase when the electrode area decreases [14]. This shows that the smaller the electrode the larger the total current needed to turn it on, and hence the higher the applied voltage for switching.

The experimental results show that the switching current of the MISS device is proportional to the electrode area so that the current density is constant. On the

other hand the holding current is not proportional to area, and the current density decreases as the electrode area increases. Hypothetically we can say that the holding current is proportional to the effective electrode area, A_{eff}.

$$I_h \quad \alpha \quad A_{eff} \qquad 5.15$$

If r is the radius of the electrode then the effective area is,

$$A_{eff} = \pi(r + \lambda)^2 \qquad 5.16$$

where λ is the additional effective radius due to the current spreading and the additional area is recognised as a spreading area. By substituting equation 5.16 into 5.15 we find

$$\sqrt{I_h} \quad \alpha \quad (r + \lambda) \qquad 5.17$$

The additional effective radius, λ, can therefore be obtained by extrapolating the plot of $\sqrt{I_h}$ vs r, or by using a linear regression. The plot is shown in figure 5.11. As we can see, at a constant area the holding current varries significantly with the SRO type and this implies that the spreading radius λ is also dependent on the type of film. From table 5.1 and figure 5.11 it can be seen that device with a small spreading radius will not switch at all for a large electrode. That is to say, the device will switch over a wide range of electrode areas only if the spreading radius is large. This type of current spreading is thought to be controlled by surface recombination which is believed to be governed by the composition and thickness of the film.

In order to check the effect of current spreading in the p-n junction, different sizes of electrode were made directly on n-p$^+$ wafer. The current-voltage characteristics for each electrode are shown in figure 5.12. The effective radius due to the current spreading in the p-n junction is estimated by plotting the square root of current against electrode radius as in figure 5.13. As we can see a similar trend occurs but

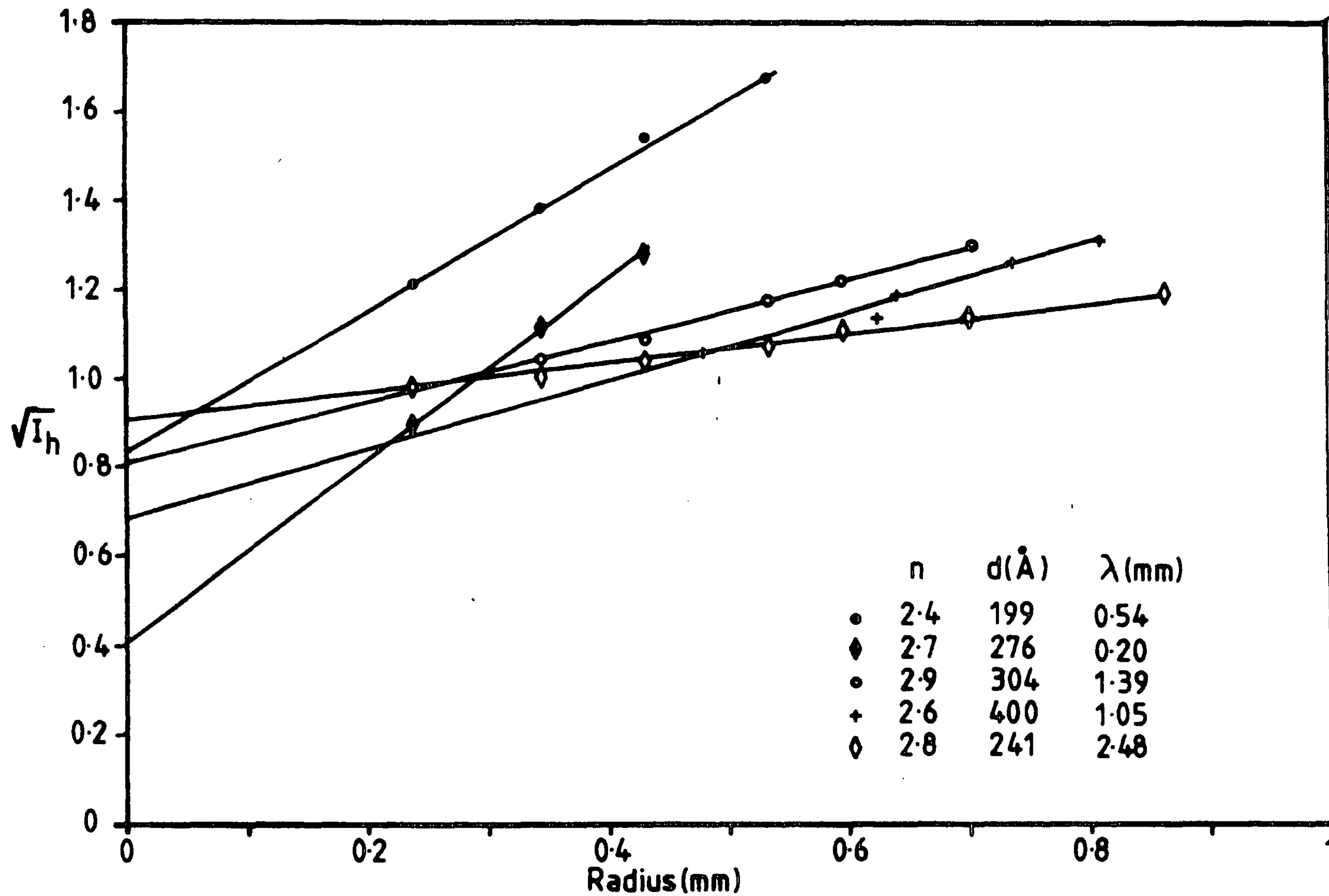


Figure 5.11 Square root of holding current versus electrode radius for different type of SRO film.

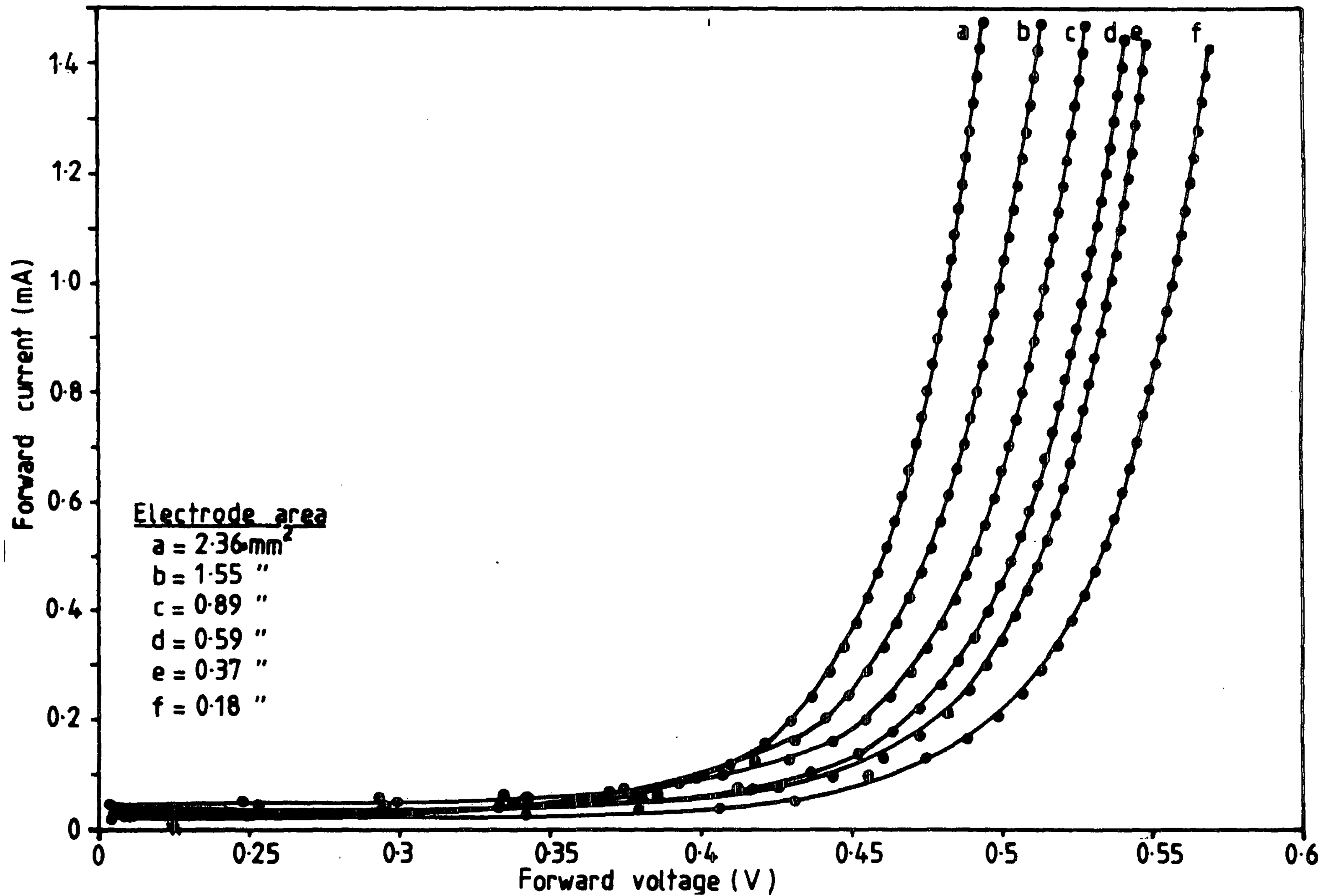


Figure 5.12 Current-voltage characteristic of p-n junction for a different electrode area.

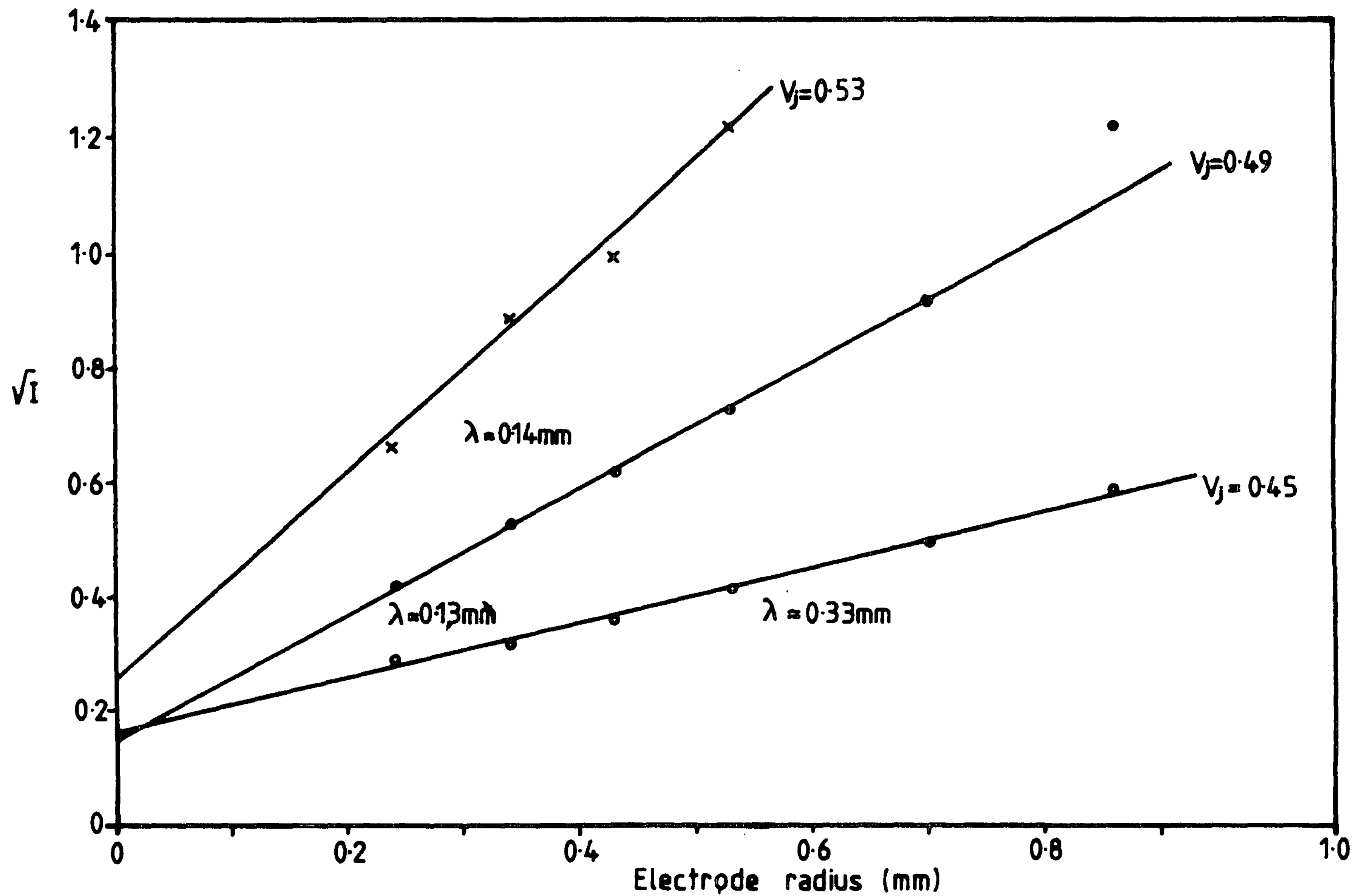


Figure 5.13 Square root of the p-n junction current versus electrode radius.

with rather a small value of λ which seems to depend on the junction voltage. This is because at low voltage the recombination at the junction is dominant and this gives rise to a higher value of λ than for larger voltages.

5.3.3 Effect of Electrode Area - Small Devices

For a more comprehensive study, a multi device chip containing various MISS structures such as isolated MISS devices, three terminal MISS devices, lateral devices, etc, was designed by P. Clifton and fabricated at Southampton except for the SRO deposition at Durham. The mask layout is shown in figure 5.14. The area effect studies were continued on this wafer which we will refer to as wafer no. 1. The thickness of the n-type epilayer on the initial wafer before processing was 7.3μm, but since high temperature processing was used for some of the structures the n/p$^+$ junction will have moved up toward the surface. Using grooving and staining techniques the epilayer thickness was measured on the final wafer as 2.95μm. The largest and smallest electrodes were $200 \times 200\mu$m and $5 \times 5\mu$m respectively. Measurements were made on ten different size devices on all 120 chips on a 3-inch wafer using a Textronix curve tracer so that it could be done quickly. For more accurate readings measurements were repeated on a few devices using the automated system as described in the preceding chapter. The overall switching voltage is below the calculated punch-through voltage which is about 48.0 volts. Therefore the device switches by the generation controlled mechanism as explained in Chapter 3.

The switching parameters of any particular size of the device on each chip were found to be inconsistent over the whole wafer. The switching parameters of the whole wafer were mapped in three dimensional plots, so that their variation with location on the wafer could be identified. As we can see from figure 5.15(a), V_s for devices with an electrode area of $160 \times 160\mu$m shown very different values at three main areas

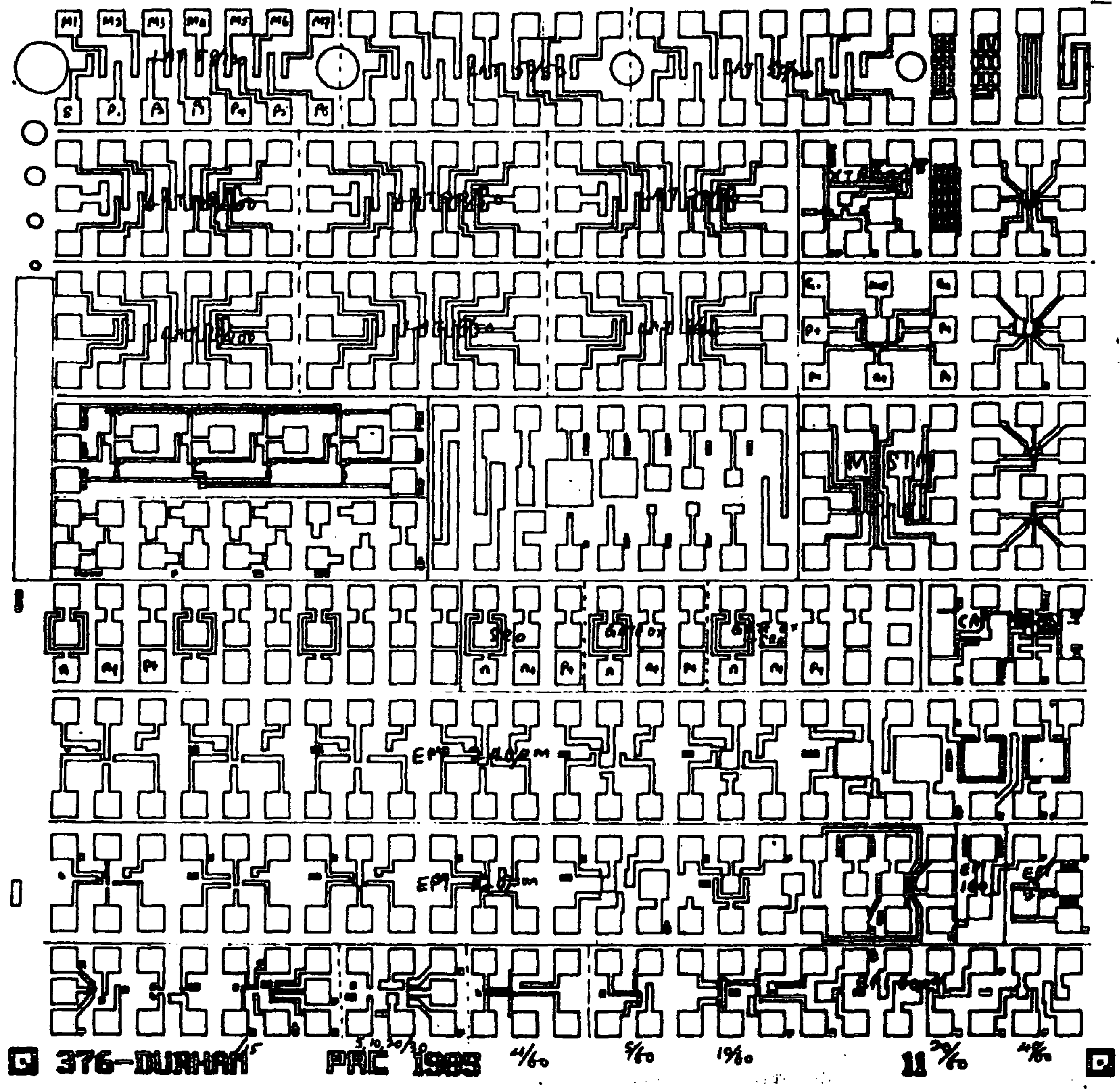
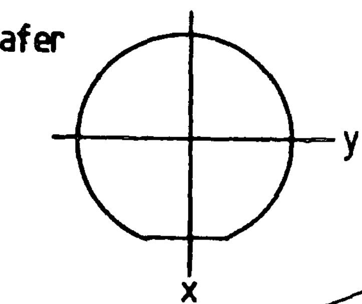


Figure 5.14 Mask pattern for the multi-structure chip designed by P. Clifton.

160×160µm²

Switching voltage



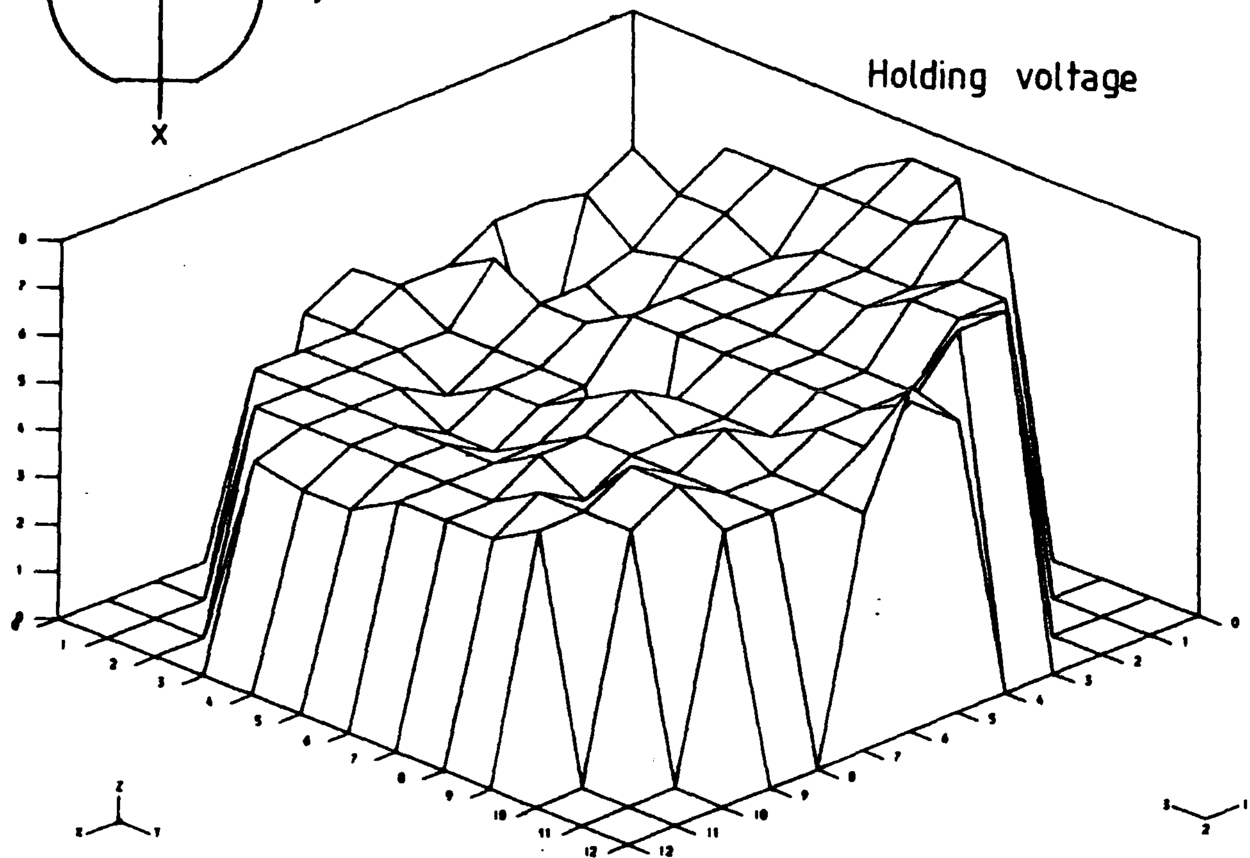


Figure 5.15 a) Three dimensional plot of the switching and holding voltages over the wafer for the non-isolated SRO-MISS device with electrode area of $160 \times 160 \mu m$. (row four column two of figure 5.14)

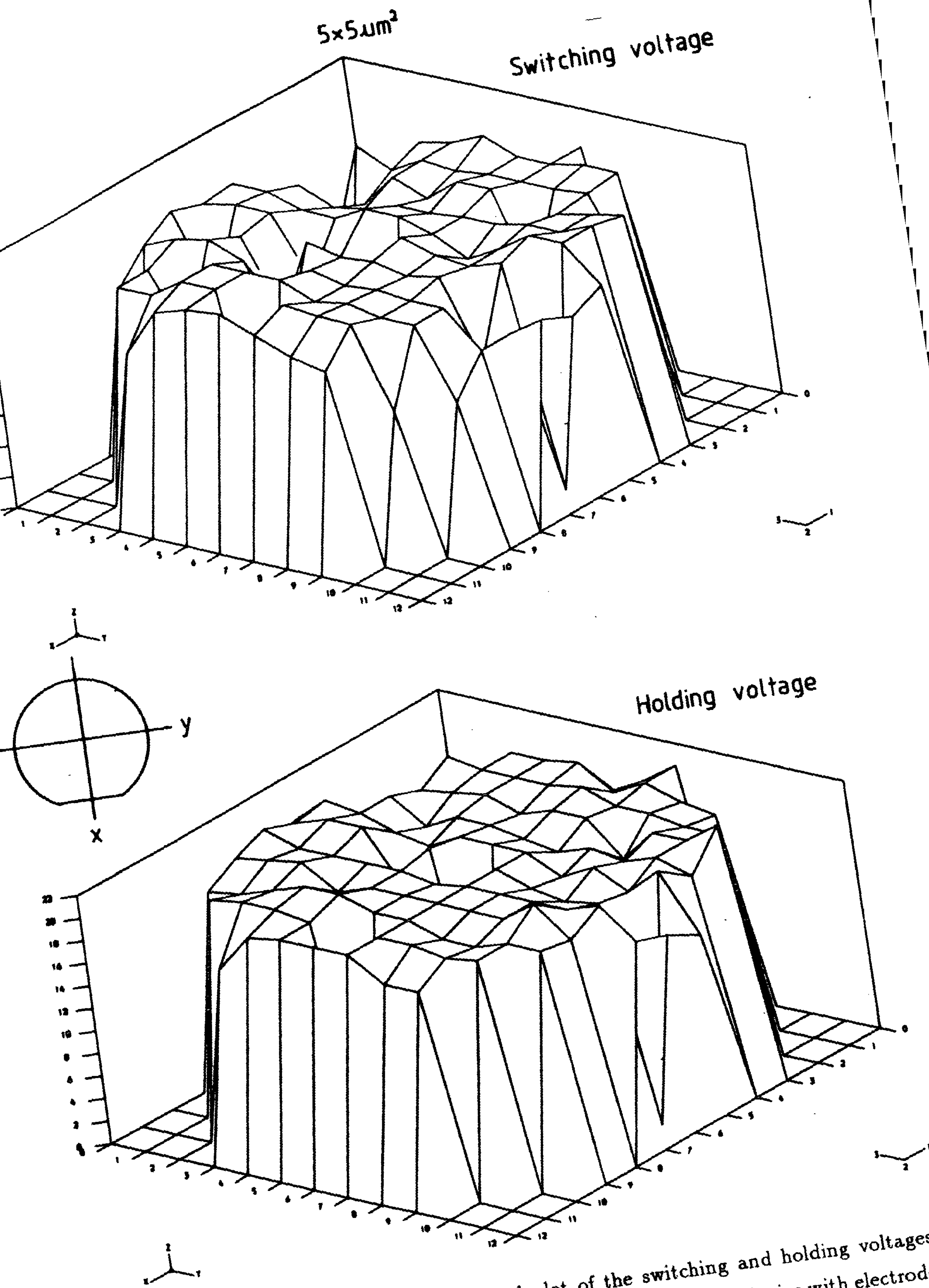


Figure 5.15 b) Three dimensional plot of the switching and holding voltages over the wafer for the non-isolated SRO-MISS device with electrode area of 5 × 5μm. (row four column two of figure 5.14)

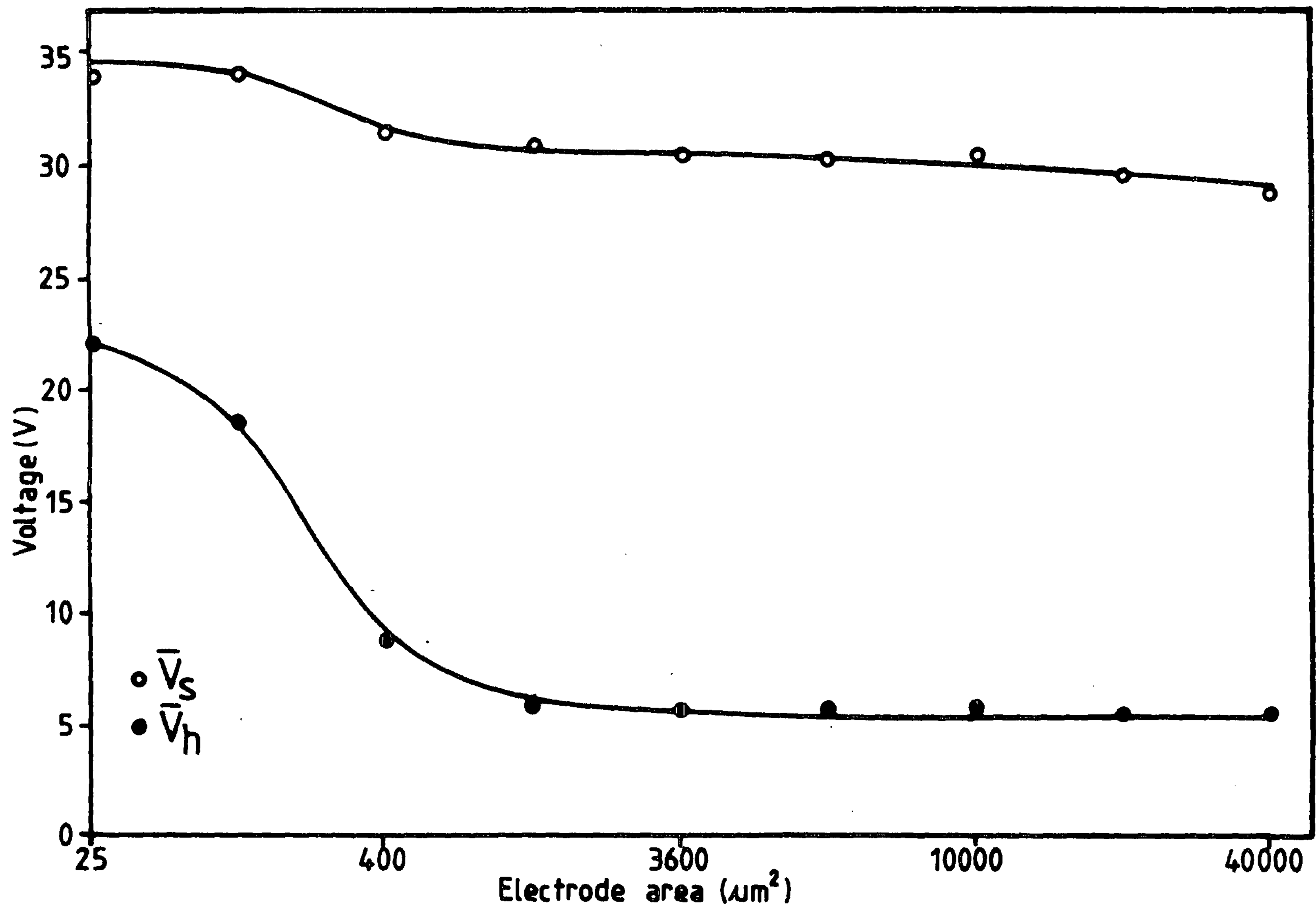


Figure 5.16 Variation of $\widehat{V}_s$ and $\widehat{V}_h$ with electrode area for the non-isolated small structure MISS (Southampton wafer no. 1).

on the wafer. However for the smallest device, $5 \times 5\mu m$, the switching voltage seems to be more consistent over the whole wafer as shown in figure 5.15(b). In general the variability was found to decrease with area between these typical results. This effect is probably due to several reasons; the uniformity of the deposited SRO layer was not very good especially on the 3 inch wafers, the resistivity of the epilayer was not uniform across the wafer, and surface and junction defects were present on the epilayer [13]. As the device area decreases, the probability of the defects being present is less than with a large electrode. The switching parameters therefore become more consistent over the wafer as the area decreases as demonstrated by the bar charts in Appendix D, figure D1 - D9.

The mean and standard division of the switching parameters are given in appendix D and their variation with electrode area is shown in figure 5.16. As can be seen, increasing the electrode area in the range of $5 \times 5\mu m$ to $20 \times 20\mu m$ causes the holding voltage to decrease very rapidly. However as the area increases further V_h becomes almost constant with area. The holding voltage of the smallest device ($25\mu m^2$) was about 21.8 volts and the holding current was 0.86mA which is equivalent to a current density of 3440 A/cm^2. At this value the p-n junction is in a very high-injection condition so that the potential drop on both sides of the junction may be very significant [3]. By assuming that most of the device voltage drop is in the SRO layer, the electric field will be $10.9 \times 10^6 V/cm$. Therefore, a steady state current-voltage measurement is most likely to end up with dielectric breakdown when it reaches the holding point. This occurred in many of the measurements.

5.3.4 Effect of Electrode Perimeter

To investigate the effects of spreading in more detail some devices with aluminum electrodes of equal size but different perimeters were fabricated. The elec-

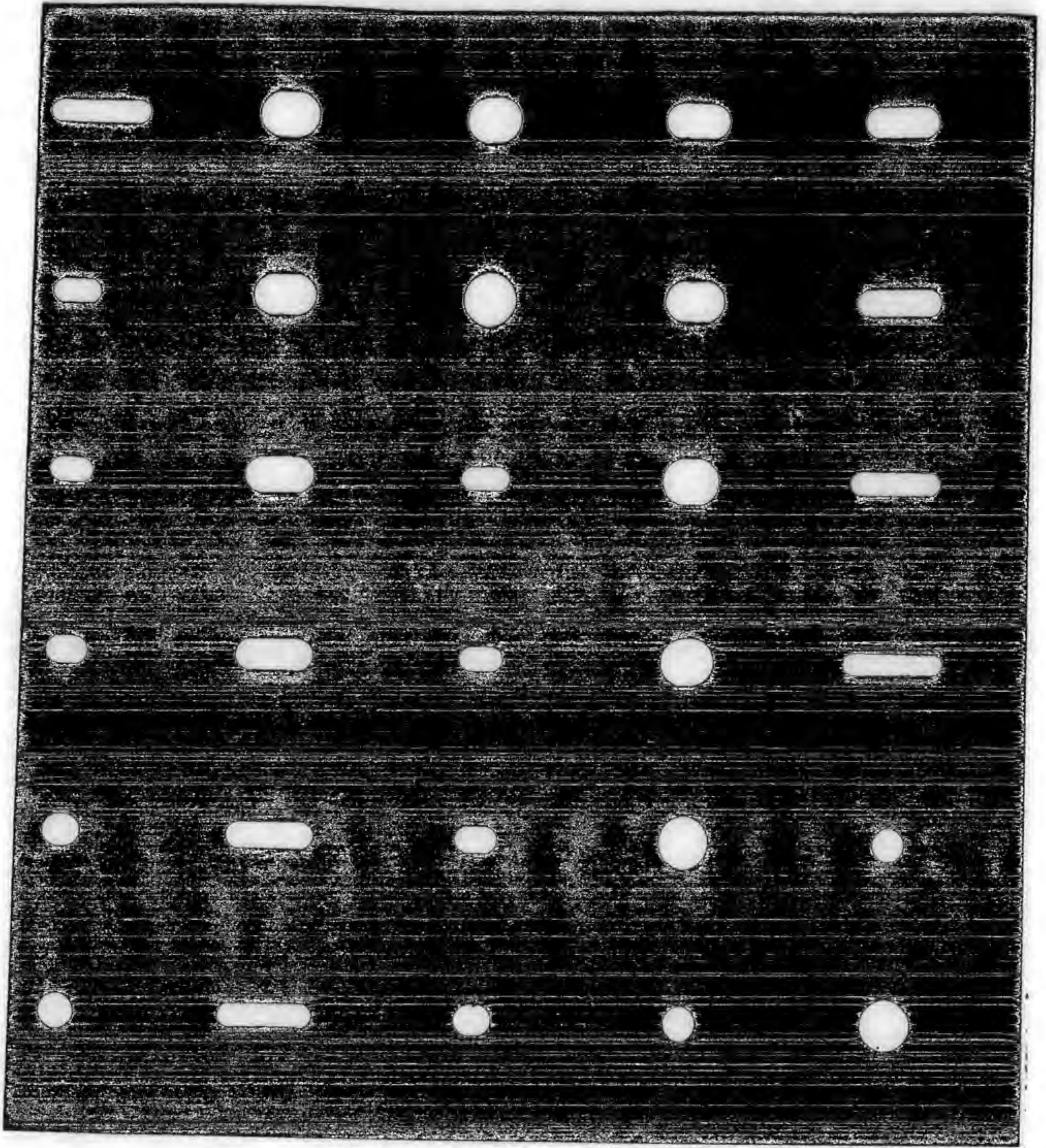


Figure 5.17 Optical mask pattern used to study the effect of electrode perimeter.

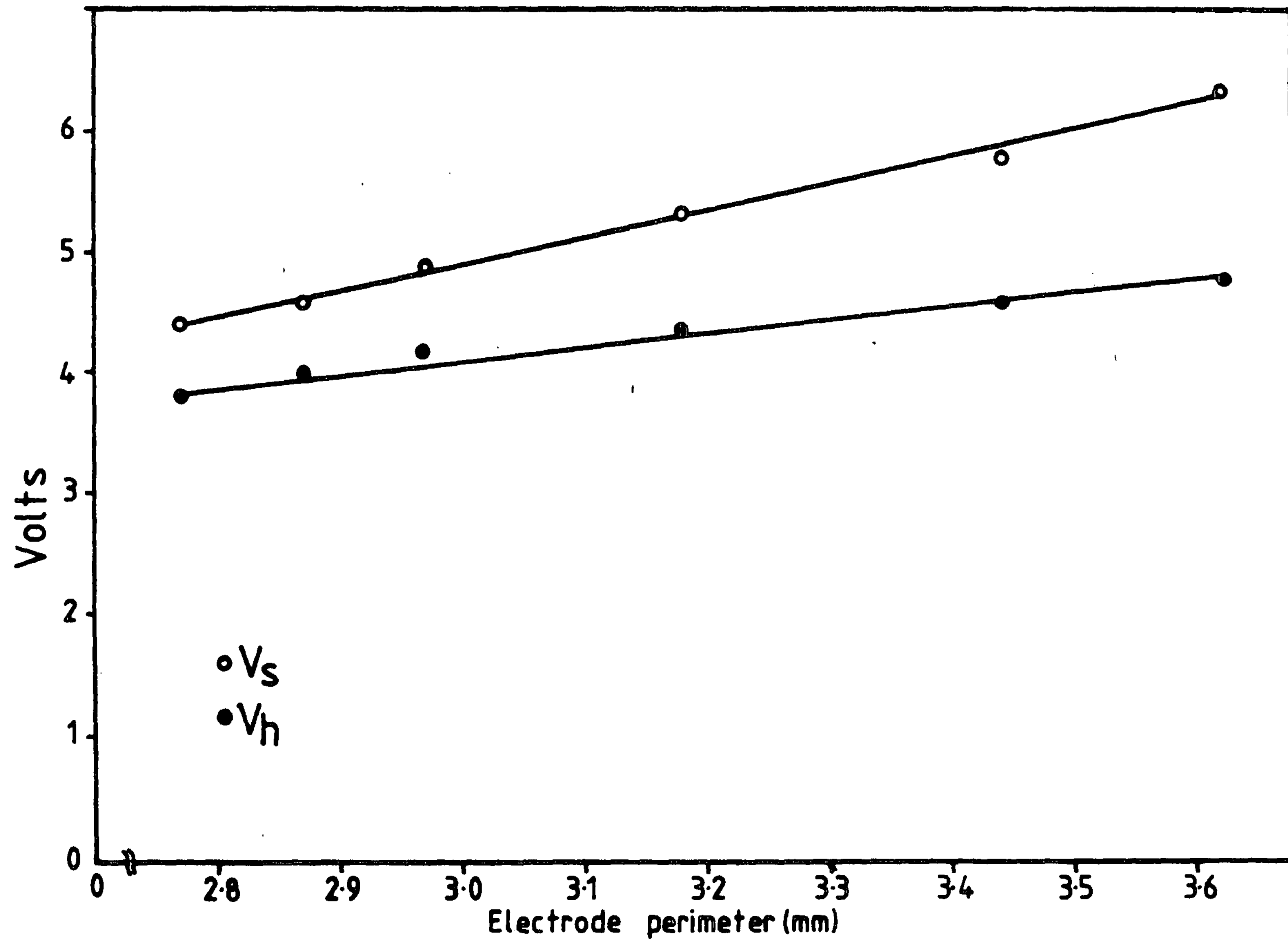


Figure 5.18 Variation of V_s and V_h with the electrode perimeter (electrode area=0.61mm^2)

trode pattern, shown in figure 5.17, avoided the use of sharp edge corners in order to be consistent with the round shape used in the previous study and also to avoid the crowding of current due to small radius at the sharp edges. Due to technical problems in cutting the mask, electrodes of only two different areas were made. The switching parameters were measured using the automated system and the result is shown in figure 5.18 for an electrode area of 0.61 mm^2. As we can see, the switching and holding voltages increase as the electrode perimeter increases. However the holding and switching current seem to be constant for all perimeters for electrodes of the same area. Similar results were obtained for the electrode area of 0.25 mm^2.

The increase of V_s with electrode perimeter provides more evidence that a current spreading effect is prominent in nonisolated MISS devices. The spreading current becomes greater if the edge or perimeter of the electrode is larger. Since the electrode area is constant, increasing its perimeter will narrow the width and increase the length. As a result, the spreading area increases as the perimeter increases as shown in Appendix E. Therefore the variation of switching voltage with device perimeter can be explained using the same argument as in section 5.3.2. It is believed that increasing the perimeter further will continuously increase the switching voltage until the punch-through condition is reached.

5.3.5 Effect of Junction Area

The p-n junction area can be defined separately from the electrode area by making an electrical isolation barrier around the device. There are three different ways in which electrical isolation can be made on monolithic devices:- junction isolation, V-groove isolation, and local oxidation of silicon (LOCOS). V-groove and junction isolated devices were fabricated at Southampton University. Unfortunately due to processing problems all the devices on the junction isolation wafers failed. Therefore

all the isolation studies were based on devices with V-grooves on wafer no.1. The cross sectional view of the isolated device is depicted in figure 5.19.

Since all the very small devices had faulty V-grooves, there are no results for a junction areas of less than $60 \times 60\mu m$. Based on measurements on a limited number of samples, seven devices on 20 to 40 chips, it was found that the magnitude of V_s increases with the junction area, A_j, as shown in figure 5.20. Similar studies made by Faraone et. al [12] shown that this trend is independent of semi-insulator thickness and the material parameters of the substrate. As the electrode to junction area ratio approaches one, the switching voltage decreases to the holding voltage. This is probably because the isolation has reduced the loss of electron current due spreading so the junction electron current density is increased. Therefore, the density of injected holes to the epilayer is also increased by reducing the area of the n-p$^+$ junction. As a result the switching voltage is reduced.

Chang et. al [23] have fabricated an isolated MIS-p-n$^+$ device with an n$^+$ diffused-shielding ring around the tunnel oxide window (MIS) so that the effect of current spreading near the surface became less significant. They also found that the switching voltage depended on the ratio of the tunnel window area to the junction area in the same way with the larger junction giving rise to a higher switching voltage. They suggested that the regenerative process becomes easier if $\partial V_j / \partial V_{ox}$ is large, and that

$$\frac{\partial V_j}{\partial V_{ox}} \ \alpha \ \frac{1}{dA_j} \qquad 5.18$$

where d is the oxide thickness. However, their model does not explain why the holding voltage increases for very small electrode areas especially if the ratio of $A_e/A_j \ll 0.1$ as in figure 5.20. Therefore we suggest that the effect is due to the combination of high current spreading and high injection in the p-n junction.

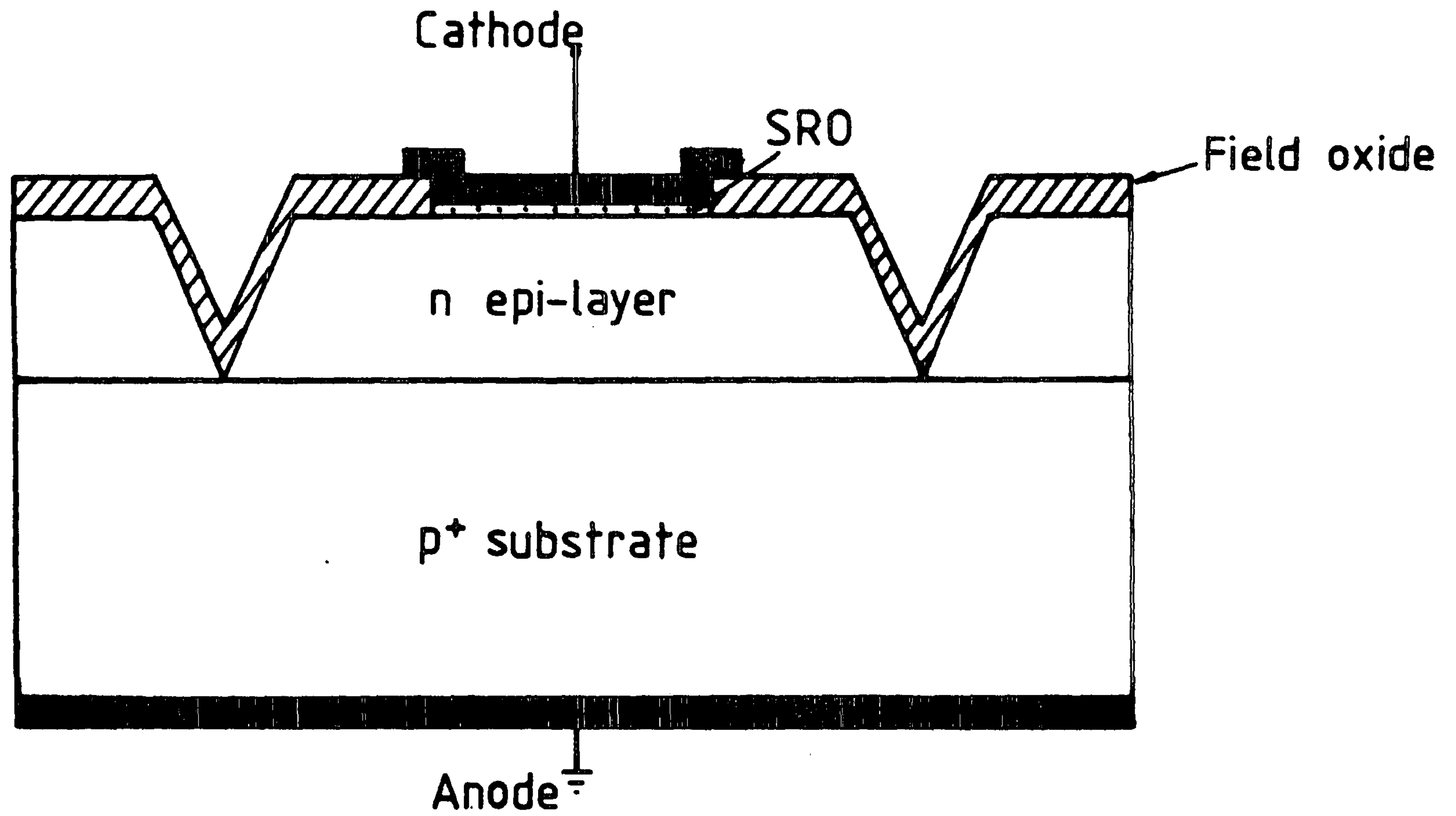


Figure 5.19 The cross-sectional view of MISS device with V-groove isolation barrier.

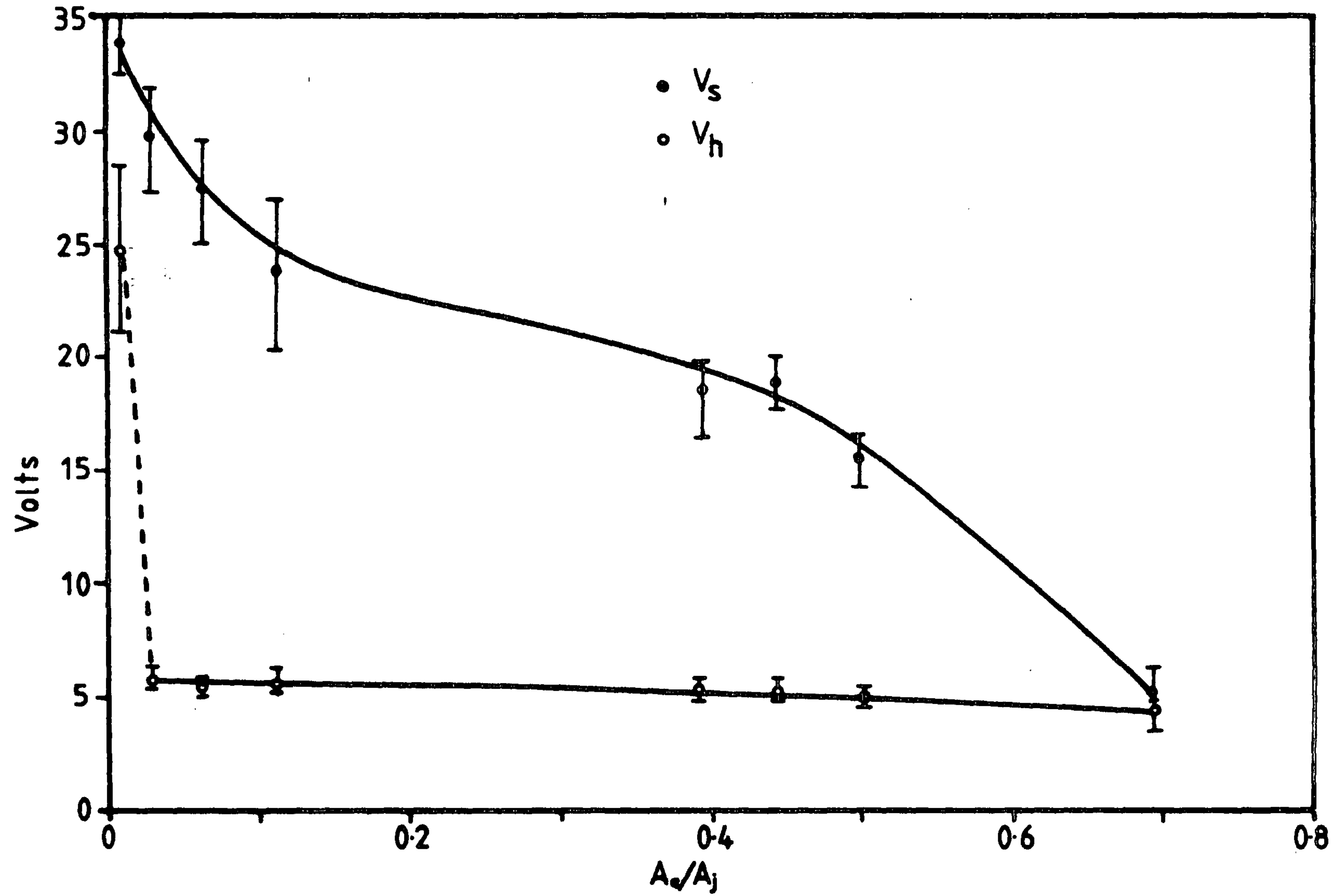


Figure 5.20 Switching voltage V_s and holding voltage V_h versus electrode area to junction area ratio (A_e/A_j) for the junction area of $120 \times 120\mu m$ to $240 \times 240\mu m$.

5.3.6 Effect of Metal Guard Ring

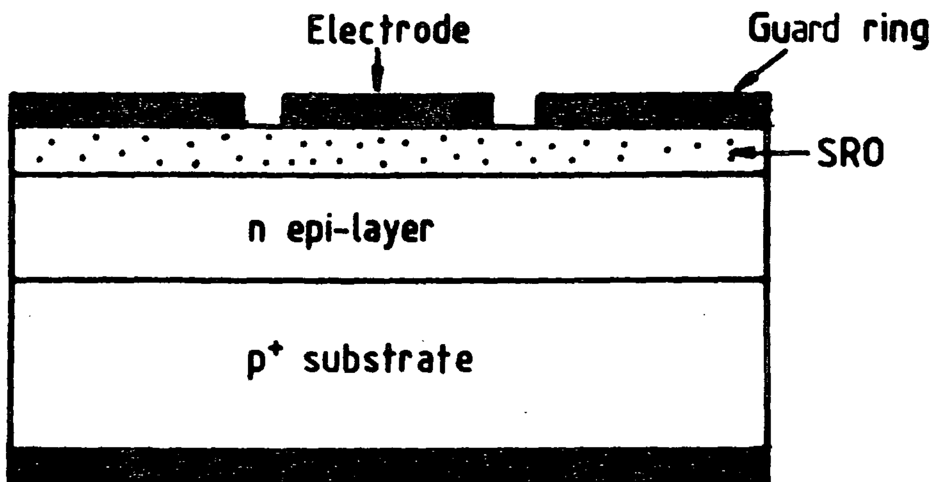
As has been demonstrated, the switching behaviour of the MISS is strongly influenced by the current spreading. Therefore, in order to reduce the effect of current spreading, a guard ring around the metal electrode was used. The electrodes were fabricated in the department using the mask shown in figure 5.21 where the electrodes have many different sizes from 0.395 to 1.48mm diameter. For technical reasons the gap between the electrode and the metal guard ring could not be made the same for all electrode areas and it has values between 0.095 to 0.158mm. The rest of the fabrication procedure was the same as before.

The variation of the switching voltage as a function of guard ring voltage for the device with an electrode diameter of 1.33mm and a gap of 0.14mm is shown in figure 5.22. As it can be seen, both positive and negative voltages on the guide ring cause the switching voltage to decrease. The variation of holding voltage was small (about 0.2 volts decrease per volt for both positive and negative voltages on the guard ring) compared with the variation of the switching voltage. When a positive potential is applied to the metal guard ring, the semiconductor surface around the device becomes accumulated with electrons. At the same time, the n-p^+ junction around the device is reverse biased, and the space charge layer will extend toward the surface more than in the active part of the device as the guard ring potential is increased. This will reduce the sideways spreading of the electrons into the surrounding area in much the same way as an isolation barrier. As the guard ring voltage is increased the isolation becomes more marked and the switching voltage falls. In addition, the accumulated electrons at the surface prevent the injected electrons from the electrode flowing laterally or spreading in the surface so forcing the majority of the electron current to flow within the actual device area.

For the case of negative potential on the guard ring the giant MISS device over

Aluminium

a)



b)

Figure 5.21 a) Optical mask used for the MISS with metal guard ring.
b) Cross-sectional view of the MISS with metal guard ring.

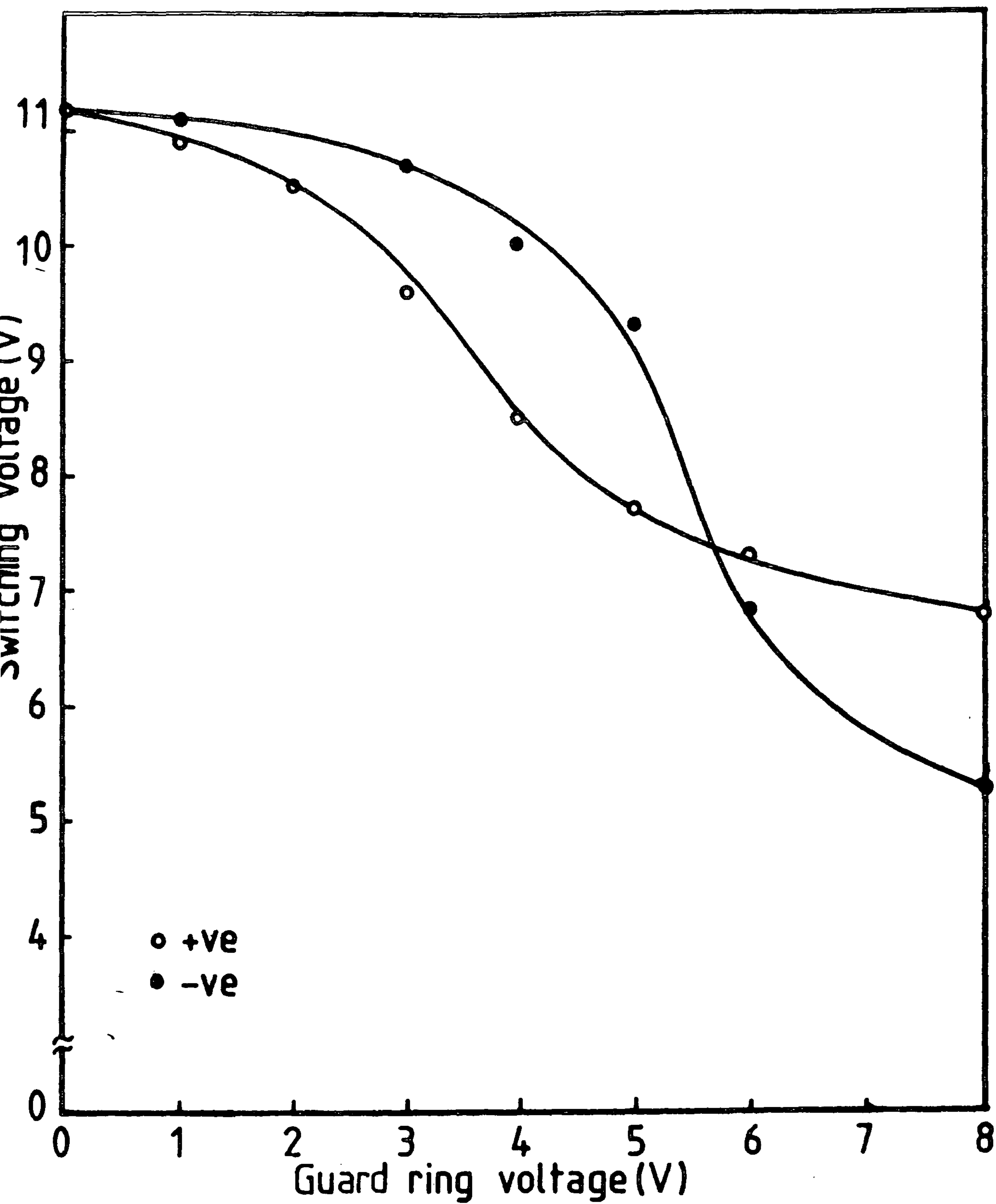


Figure 5.22 Switching voltage V_s versus guard ring voltage for the electrode area of 1.39mm^2.

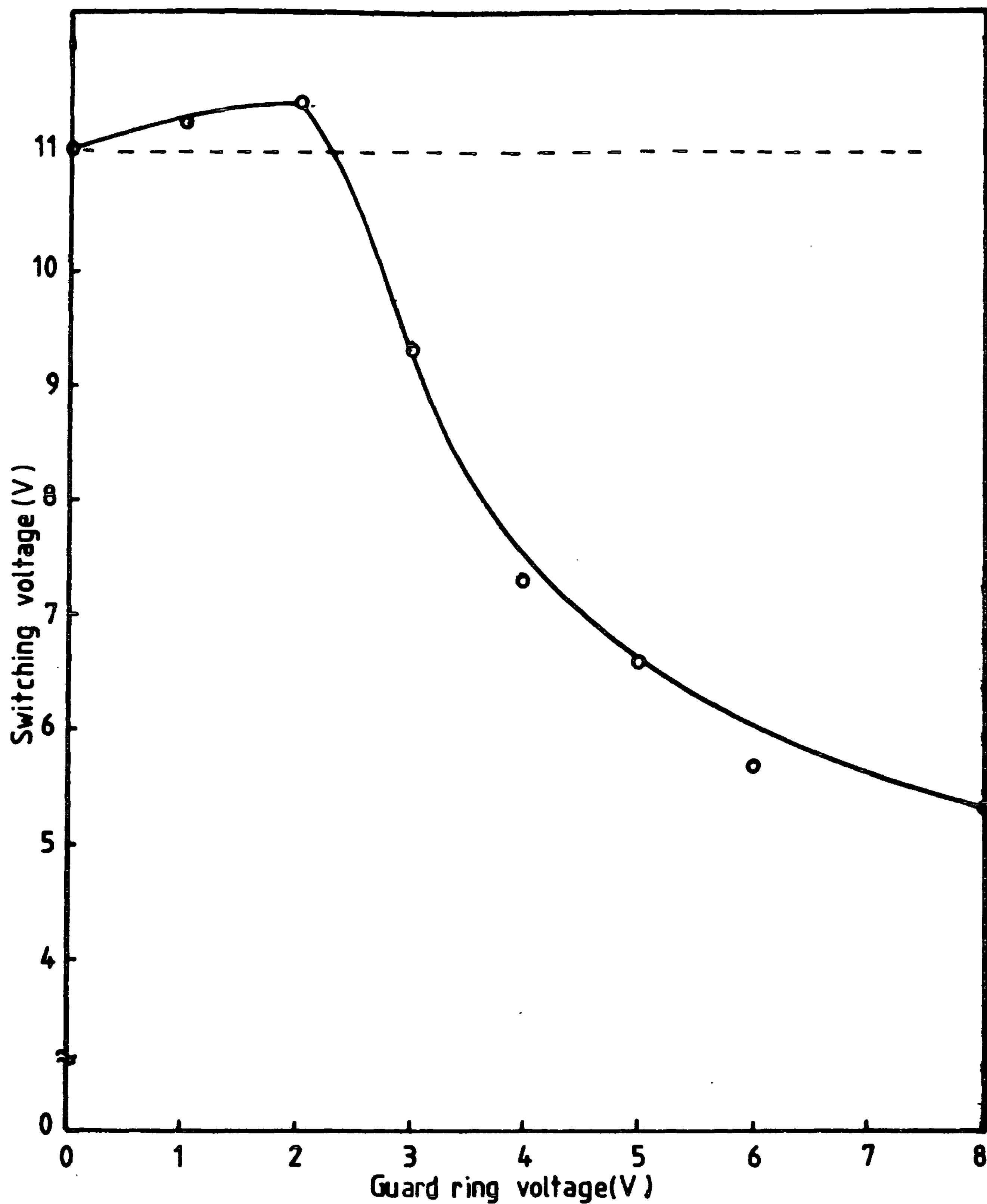


Figure 5.23 Switching voltage V_s versus guard ring voltage for the smaller electrode area of 0.23mm^2.

most of the wafer will be ON due to the area effect for all voltage above about 4V. Thus, the surface will be depleted for low guard ring voltages and then inverted for high voltages. The n-p$^+$ junction around the active devices will be forward biased everywhere. The holes from the inverted surface under the metal guard ring will be able to flow towards the SRO-semiconductor interface under the active device electrode and this will speed up the formation of the inversion layer there thus reducing the switching voltage. The effect will become more pronounced as the guard ring voltage is increased.

For the smallest device with the diameter of 0.54mm when the guard ring voltage was increased negatively the switching voltage at first increased above the initial V_s value (with zero potential on the guard ring) and then decreased drastically as shown in figure 5.23. Since the electrode is relatively small compared to the previous one, the field spreading effect is greater. As a consequence, the depletion layer under the electrode may extend further laterally towards the metal guard ring. However it is not clear how this can initially increase the value of the switching voltage as found. However, as the guard ring potential increases further the surface begins to invert, reducing the switching voltage as described previously.

5.3.7 Conclusion on Two-Dimensional Effects

The two dimensional effect on the MISS device has been investigated experimentally. The area dependence of the switching voltage is shown to be due to the current spreading in the epilayer. Measurements on a p-n junction with different electrode areas gave further evidence about the existence of current spreading in this type of structure. Spreading occurs as a result of the junction potential not falling suddenly at the edge of the electrode. The effect on the switching voltage was investigated further by looking at the effects of electrode perimeter, junction area and guard ring

voltage.

The effect of perimeter is that the switching voltage increases as the spreading area increases and it does not depend on the electrode area. The spreading area can be reduced by making an electrical isolation barrier to clearly define the p-n junction area. The result of this experiment is that the switching voltage decreases if the electrode to junction area ratio is decreased. This shows again that the switching voltage decreases with decrease of the spreading area. A similar result was also found for samples with a metal guard ring where the switching voltage decreases with increase of guard ring voltage again due to the change in the spreading area.

5.4 EFFECT OF SRO DEPOSITION TIME

5.4.1 Introduction

Since the SRO is non-stoichiometric in nature and the growth is not accurately controlled it was not possible to vary the thickness without changing the index of refraction which corresponds to the percentage of silicon in the film. As has already been shown in Chapter 4, increasing in the deposition time increases the thickness as well as the refractive index of the film. Therefore the preliminary investigation of film type was carried out merely to see the variation of the switching parameters with the deposition time at a constant gas phase ratio. For this purpose, the SRO deposition was carried out by keeping the flow rate of N_2O and SiH_4 constant at 6.5ml/min and 61.3 ml/minute respectively, and the deposition time was varied from 0.6 to 2.0 minute.

5.4.2 Results and Discussion

The apparent refractive index and thickness of the films used is shown in table 5.2.

Table 5.2: The ellipsometer readings of apparent refractive index and thickness with SRO deposition time

	Ellipsometer reading	
Deposition time (min)	n	d($\AA$)
0.6	< 1.5	100
0.8	2.4	194
1.0	2.9	304
1.5	3.1	310
2.0	1.3	120

As shown in figure 5.24 and 5.25, increasing in the deposition time from 1.0 to 2.0 minutes results in an increase of the switching parameters, V_s, V_h and I_s, whereas I_h is rather different. The variation of the switching current with deposition time appears to show a peak at 0.8 minute. The holding current was very high at 0.6 minute and it then decreases with time up to 1.0 minute and after this point it increases slightly with time as shown in figure 5.25.

The SRO films deposited on silicon under the present conditions have been shown to have a three layer structure. The first layer is the atmospheric oxide, about 15$\AA$, the second is the SRO, and the third is another layer of atmospheric oxide [27]. At a small deposition time, the measured refractive index was very close to the oxide value, and this is because the ellipsometer readings only give the average values of the total composition over the film thickness and oxide is more dominant in this case. As the deposition time increases, the measured refractive index and thickness increase because the SRO layer becomes dominant compared to the atmospheric oxides. At a larger deposition time (2 minute) the ellipsometer readings may give false values of refractive index and thickness because the SRO become less transparent due to the

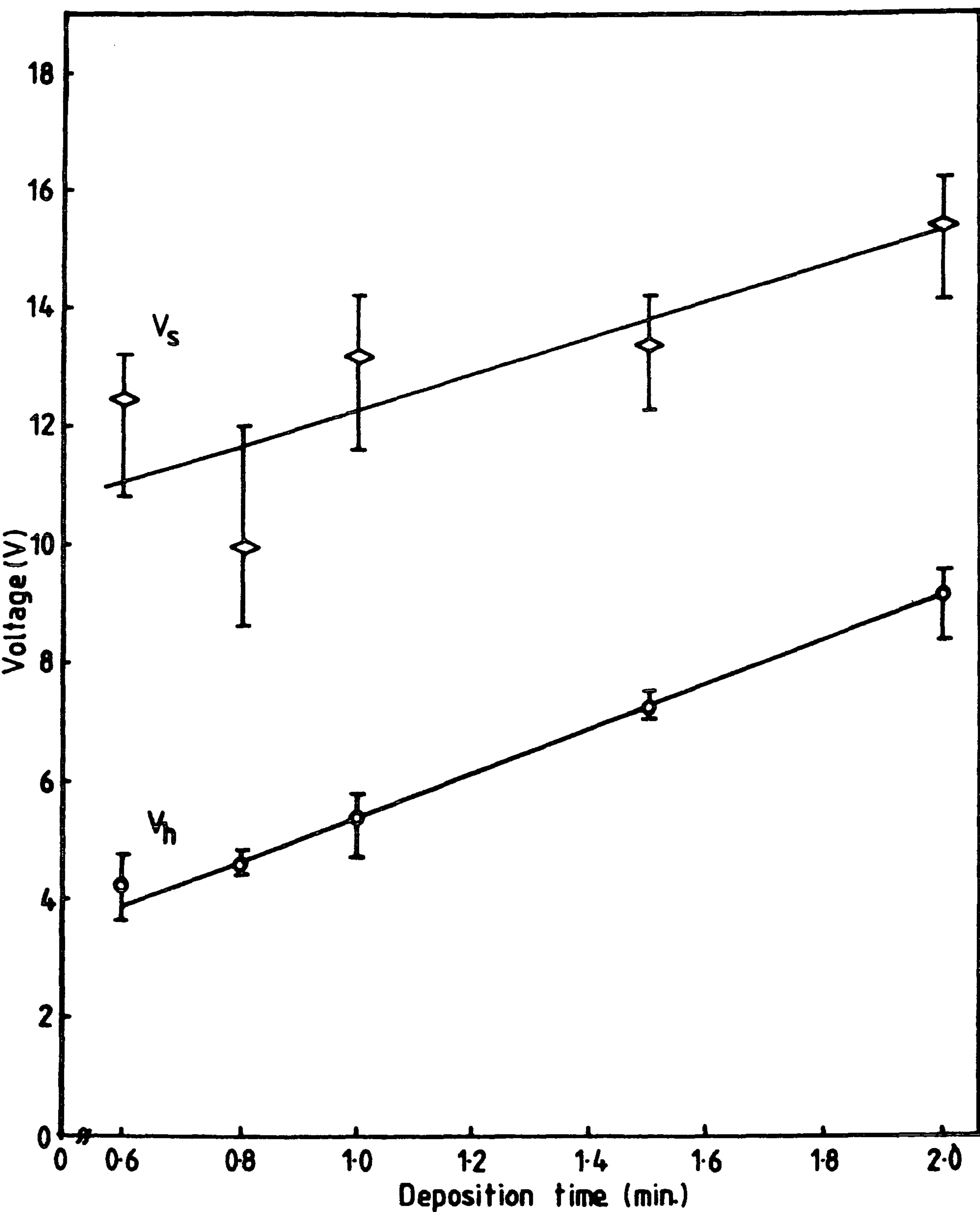


Figure 5.24 Switching voltage V_s and holding voltage V_h of the non-isolated MISS versus SRO deposition time (electrode area=0.18mm^2, number of sample=6).

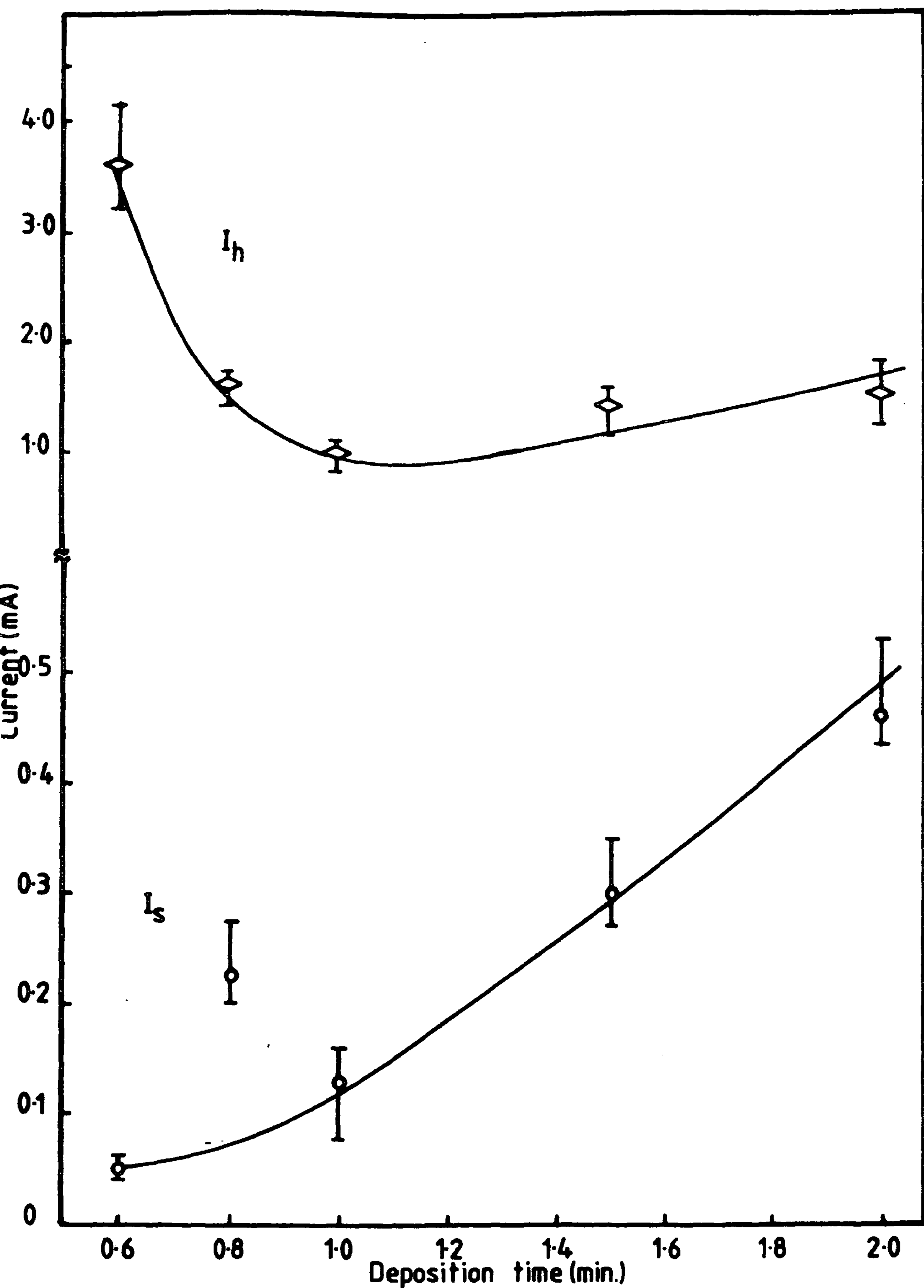


Figure 5.25 Switching current I_s and holding current I_h of the non-isolated MISS versus SRO deposition time (electrode area=0.18mm^2, number of sample=6)

increase in the silicon concentration.

Based on a symmetrical Schottky barrier (SSB) model as a conduction mechanism in SIPOS, Bolt and Simmons [10] have shown that the increase in oxygen concentration was equivalent to decreasing the effective Richardson constant, A^*, and increasing the barrier height between grains, φ_b. This resulted in the theoretical increase of V_s, V_h, I_s, and I_h, but in their model the thickness of the film was not taken into account. For the present SRO the apparent refractive index and hence the average silicon concentration increases with deposition time so that the switching parameters would be expected to fall. As they do the opposite, the effect of thickness must predominate. A rise of all the parameters with thickness would be expected from the general mechanism of a tunnel oxide device. This trend has been observed by other workers [2,16,28-30] for tunnel oxide, polysilicon and SIPOS-MISS devices.

The switching characteristic at a deposition time of less than 0.8min is probably governed by the oxide layer rather than the SRO so that it can be excluded in viewing the variation of the switching parameters with the SRO deposition time.

5.5 EFFECT OF HEAT TREATMENT ON SWITCHING CHARACTERISTICS

In order to study the effect of heat treatment on the switching characteristics of the MISS device, wafers with aluminum electrodes and gold back contacts were annealed in a nitrogen ambient at a temperature of 400^oC for 5 and 10 minutes. The I-V measurement was carried out before and after the heat treatment. It was found that the heat treated device gave lower holding and switching currents and lower switching and holding voltages. Table 5.3 shows the switching parameters of the as-made and heat treated-devices. The switching and holding currents of the

heat-treated devices decreased to more than half of the values for the as-made device.

Table 5.3: The effect of heat treatment on switching parameters

(Non-isolated devices. Electrode area of 0.18mm^2)

Annealing time	V_s(V)	V_h(V)	I_s(mA)	I_h(mA)
as-made	12.0	4.7	0.12	0.52
5 min.	8.0	4.4	0.068	0.268
10 min.	8.0	3.0	0.039	0.15

For the case of thermally grown oxide, heat treatment in the presence of an aluminum electrode will make the interfacial trapping centre disappear [18]. and for a tunnel oxide MISS device this has been shown theoretically to increase the switching voltage [26]. The changes in the switching parameters for the SRO-MISS as shown in table 5.3 are the opposite and probably due to the increase in the trap energy as a result of heat treatment [17] with this material. The position of traps in the band gap influences the charge storage and the barrier height which they produce. The larger the trap energy the lower the barrier height hence reducing the switching voltage and current [2,10]. The presence of traps in the heat treated SRO-MISS was confirmed using a technique used by H. K. Phan et. al [8] as will be discussed in section 5.10. The effect of high temperature annealing (800°C) on the switching parameters will be discussed in the following section.

5.6 EFFECT OF GOLD DIFFUSION

This investigation was carried-out in order to see the effect of a bulk recombination centre on the switching characteristics of the device. The effect on charge storage

was also studied and will be discussed in section 5.10.4. Gold has long been known as an impurity which can be used to reduce the minority carrier lifetime in semiconductor devices by forming deep levels in the energy bandgap. It has a relatively high solid solubility in interstitial and substitutional sites in silicon [1] and this has the advantage that its concentration can be controlled over a wide range of values. The recombination centre was introduced in the MISS devices by diffusion of a controlled amount of gold from the back of the sample.

5.6.1 Sample Preparation

The wafer was cut into four pieces and SRO deposition was carried out on all of them in one run so that each piece had the same type of film. Immediately after the deposition pure gold was evaporated on to the back of two of them. The slices with gold at the back were loaded into the gold annealing furnace together with a control slice without gold at the back because it is believed that the conductivity of SRO will be affected by heat treatment. The diffusion was carried out at a temperature of 800°C for 5 and 10 minutes for two pairs of samples and the nitrogen flow was keept constant at the rate of 2 litres/minute. The top electrode and back contacts were then made using the same technique as described in Chapter 4.

Since the gold diffusion follows complementary error function (erfc) diffusion, the impurity concentration at any given time and given distance is given by [1],

$$N(x,t) = N_o \mathrm{erfc}\left\{\frac{x}{2\sqrt{Dt}}\right\} \qquad 5.19$$

where N_o atoms/cm^2 is the amount of gold placed on the surface before diffusion, D is the diffusion coefficient in cm^2/sec, t the diffusion time in seconds, and x the diffusion distance in cm. It is very difficult to estimate accurately the gold concentration in

the device because its diffusivity is a strong function of defect concentration, doping level and temperature [1]. However, the gold concentration at 250μm from the surface (the thickness of the wafer) can be estimated using both interstitial and substitutional diffusion coefficients at 800^oC which are 4.0×10^{-6}cm^{2}s^{-1} and 9.0×10^{-12}cm^{2}s^{-1} respectively.The effective diffusion coefficient [31]

$$D_{eff} \approx 0.9D_i + 0.1D_s \tag{5.20}$$

$$= 3.6 \times 10^{-6}\text{cm}^2\text{s}^{-1}$$

By assuming $N_o = 5\times10^{15}$cm^{-2}, the gold concentration at 250μm from the surface is 3.1×10^{15}cm^{-2} and 3.9×10^{15}cm^{-2} for 5 and 10 minute annealing times respectively.

5.6.2 Results and Discussion

Their switching characteristics are summarized as in table 5.4.

Table 5.4: Effect of gold doping on the MISS characteristics

(Average results for 4 non-isolated devices)

Electrode size=1.73mm^2				
Annealing time	V_s(V)	V_h(V)	I_s(mA)	I_h(mA)
5 min (no gold)	13.4	5.1	0.12	0.8
5min (with gold)	14.7	6.8	0.42	1.0
10 min (no gold)	16.1	4.9	0.18	0.8
10 min (with gold)	14.2	6.4	0.08	0.55

Electrode size=0.96mm^2				
Annealing time	V_s(V)	V_h(V)	I_s(mA)	I_h(mA)
5 min (no gold)	13.7	4.7	0.09	0.6
5min (with gold)	14.6	6.9	0.3	1.04
10 min (no gold)	17	4.8	0.13	0.7
10 min (with gold)	14.8	6.2	0.06	0.47
Electrode size=0.47mm^2				
Annealing time	V_s(V)	V_h(V)	I_s(mA)	I_h(mA)
5 min (no gold)	16.2	5.6	0.05	0.5
5min (with gold)	15.4	7.4	0.2	0.93
10 min (no gold)	16.8	5.2	0.10	0.64
10 min (with gold)	15.1	6.9	0.10	0.55

As can be seen from table 5.4, for the 5 minute annealing all the switching parameters seem to be increased with gold on the back of the wafer. On the other hand, for 10 minute annealing, V_s, I_s, and I_h decrease but V_h increases if gold is present during the annealing. The increase in the switching parameters for the samples where there was no gold during annealing for 5 and 10 minutes was believed to be due to the increase of the interface state density [16]. The interface state density of SRO has been demonstrated by Tong et al [17] to increase if the SRO is annealed under the present conditions. The effect of interface state density on the I-V characteristic of the MISS has been shown theoretically to increase the V_s, I_s, I_h, and slightly increase the V_h [16], and the present experimental results also show a similar trend. The presence of interface states will develop an interfacial barrier which prevents or delays the formation of the inversion layer at the interface as the voltage is increased, hence increasing the switching voltage and current.

For the sample with 5 minute gold diffusion the gold concentration is probably small compared to the interface state density which might be present due to the annealing. As a result the I-V characteristics are predominantly determined by the type of SRO and the interface state density which increases during the annealing. However, for 10 minute diffusion the effect of the gold becomes dominant compared to the effect of the interface states.

The presence of recombination centres with a capture cross section for holes greater than for electrons [1] gives rise to an increase of recombination current, J_{rec}, in the n-region. As a consequence, the hole tunnel current ($J_{tp} = J_{pj} + J_{rec}$) increases, increasing the injection of electron tunnel current and hence turning the n-p$^+$ junction into more forward bias. Thus the switching voltage decreases. Since the rate of recombination is greater, a higher voltage is needed to maintain the inversion when the device is turned on, and this results in a higher holding voltage. Hence it is concluded that gold doping reduces, V_s, I_s and I_h, but increases the value of V_h. This is an agreement with the results in table 5.4.

5.7 EFFECT OF WORK FUNCTION DIFFERENCE ON THE MISS SWITCHING PARAMETERS

To study the effect of work function difference on the switching characteristics of the SRO-MISS gold which has a work function of 5.0 volts [3], was deposited as an electrode on the same wafer after the aluminum electrodes were deposited. Both electrode patterns were formed using a metal mask for the reason given in section 5.2.4. The switching parameters for both aluminum and gold electrodes are shown in table 5.5. The device with the gold electrode has a higher holding voltage compared to that with the aluminum electrode and the switching current with the gold electrode was about double that with the aluminum electrode. As we can see, the increase of

holding voltage is very significant for the SRO type A which is less conductive. The switching voltage of the Au-MISS is a little lower than that of the Al-MISS. However, for the SRO type B, the switching voltage of the Au-MISS is higher than that of the Al-MISS.

Table 5.5: Effect of work function difference

(Average results for 4 devices non-isolated. Electrode area= $0.42mm^2$)

SRO Type	Electrode	V_s(V)	V_h(V)	I_s(mA)	I_h(mA)
A: $n = 2.7$	Al	11.5	2.5	0.08	0.7
$d = 401\AA$	Au	11.1	6.8	0.19	0.65
B: $n = 2.82$	Al	7.3	3.1	0.15	0.49
$d = 285\AA$	Au	8.1	4.2	0.35	0.72

Habib and Simmons [19] have shown that a higher metal work function retards the formation on an inversion layer so that the switching voltage and current are shifted to higher values. The higher value of the holding voltage for the gold electrode can be explained by considering the voltage distribution in the MISS structure which can be expressed as

$$V_h = V_{FB} + V_{SRO} + \psi_s + V_j \qquad 5.21$$

where V_{SRO} is the voltage drops across the SRO layer, V_{FB} is the flat band voltage given by,

$$V_{FB} = \phi_{ms} - \frac{Q_i}{\epsilon_i} d \qquad 5.22$$

.The work function difference ϕ_{ms} can be expressed in terms of barrier heights as

shown in figure 2.1(a),

$$\phi_{ms} = \phi_{bn} - (\phi_{so} + \frac{E_g}{2} - q\psi_b) \tag{5.23}$$

where ϕ_{bn} is the difference between metal Fermi level and the conduction band edge of the semi-insulator(SRO), ϕ_{so} is the difference between the semiconductor and semi-insulator conduction band edges and the others symbols have their usual meanings.

For the purpose of comparison we take the values of work function difference in metal-oxide-semiconductor systems since not much information is available about the metal-SRO-semiconductor structure. For n-type silicon with an impurity concentration of 10^{15}cm^{-3}, the work function differences for Al-SiO_2-n and Au-SiO_2-n are -0.3 and 0.6 volts respectively [15]. Thus if the other voltage components in the MISS are constant, the holding voltage for the gold electrode should be 0.9 volt higher than for the aluminum electrode. As we can see from table 5.4, the increase of holding voltage of gold electrode MISS is considerably higher than this for the thicker SRO layer.

For the tunnel oxide MISS, Fiore De Mattos and Sarrabayrouse [6] have shown that the sensitivity of the switching voltage to the work-function difference depends on the thickness of the tunnel-oxide. For a thinner oxide the sensitivity is very small, but for the intermediate thickness (32Å) the sensitivity is quite pronounced in the range of 15 to 20 V/eV. However no theoretical results have been published about the dependence of holding voltage on the work function difference. For the case of SRO-MISS devices, the sensitivity seems to be dependent on the type of SRO film as shown in table 5.4. The reason for this is probably because in the Au-SRO-n structure the carriers which transport the current are mostly holes. For the less conductive film (SRO type A), the surface concentration of holes is greater than for type B because a smaller number of holes can pass through the film, and therefore the voltage drop across it is higher.

The shift of V_h due to work function difference can be utilized to make a two

phase MISS shift register [20].

5.8 EFFECT OF ILLUMINATION ON THE MISS

5.8.1 Theoretical Review

We consider the case where the device is illuminated with light. The rate at which electron-hole pairs are produced by the absorption of light is given by equation 5.1 in section 5.2.3. By assuming that all the light is absorbed below the metal electrode the rate of electron-hole pair generation as function of distance from the electrode can be described as in figure 5.26 [24]. Generation currents are produced in four regions, namely the interfacial and junction depletion regions where the current flows by drift, and the neutral n-type and the p^+ substrate where the current flows by diffusion. The electron-hole pairs generated in the interfacial depletion region will be immediately separated by the electric field in the depletion layer. The electrons are swept to the neutral region and they then diffuse towards the p^+-n junction where they recombine with the injected holes from the substrate. The holes are swept to the SRO-semiconductor interface and pass through the SRO to the metal. The photocurrent reaching the interface is given by [24],

$$I_{dL} = -qA_L \int_0^{X_d} G(x)dx \qquad 5.24$$

where A_L is the illuminated area, X_d is the width of the interfacial depletion region and $G(x)$ is the carrier generation rate given by equation 5.1. The photocurrents in the depletion region and the neutral region contribute to the off-current of the MISS and hence they reduce the switching voltage of the device. The switching process is basically identical to the normal electrical process, the only difference being

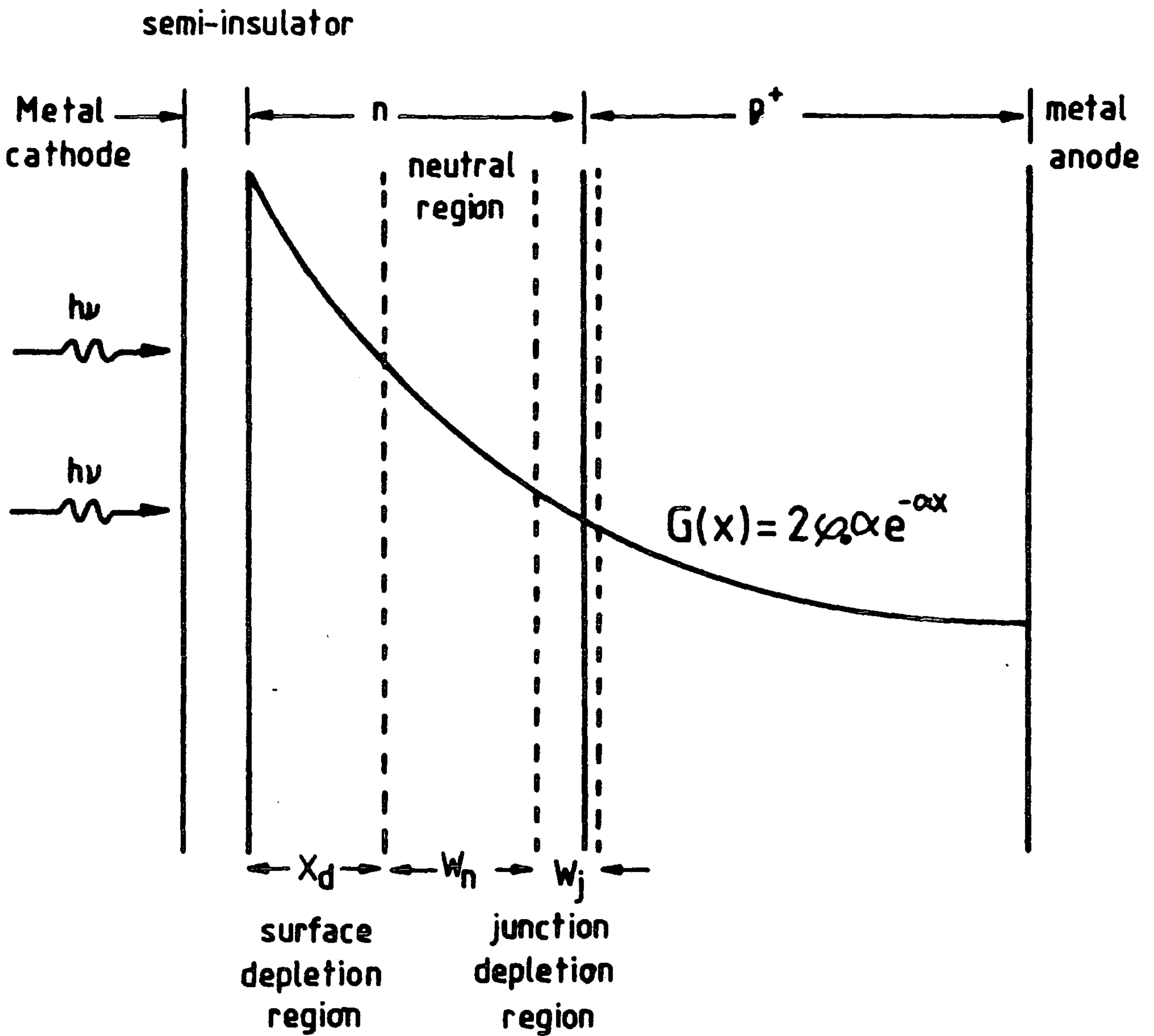


Figure 5.26 Rate of generation of hole-electron pairs in the MISS structure due to absorption of light (from ref. 24).

the mechanism by which the holes are generated to form the inversion layer at the interface. The optical generation of holes and electrons in the junction depletion region is small, and they are swept to the p^+ substrate and epitaxial layer respectively. Thus, they do not contribute significantly to the off-current.

5.8.2 Results and Discussion

The effect of light illumination on the switching behaviour was studied using a microscope lamp as has already been described in section 5.2.3 for the MIS experiments. The wafer SRO157 with an electrode area of 0.59mm^2 (see table 5.1) was used for this purpose. Since the Al electrode absorbed most of the incident light, the effects were probably due to the light passing through the SRO around the electrode. As we can see from figure 5.27, V_s decreases drastically at low intensities, up to 50 lux, and more gradually at higher intensities of light illumination. The switching current, off-current and the holding current all increase as light illumination is increased. As expected the increase of electron-hole generation rate by light causes the surface depletion layer to reduce and hence the surface potential to fall. As a consequence, the switching voltage decreases as the light illumination (lux) increases.

The sensitivity of the device to light was found to be dependent on the type of SRO as demonstrated in figure 5.28, where the ratio of V_s(light) to V_s(dark) is plotted against the deposition time. As it can be seen, the sensitivity seems to decrease with deposition time. This is probably bacause, as the deposition time increases, the SRO becomes thick and very silicon-rich. As a result, the film becomes less transparent or the reflectance increases [25] so that, the photon flux entering the semiconductor depletion region is less.

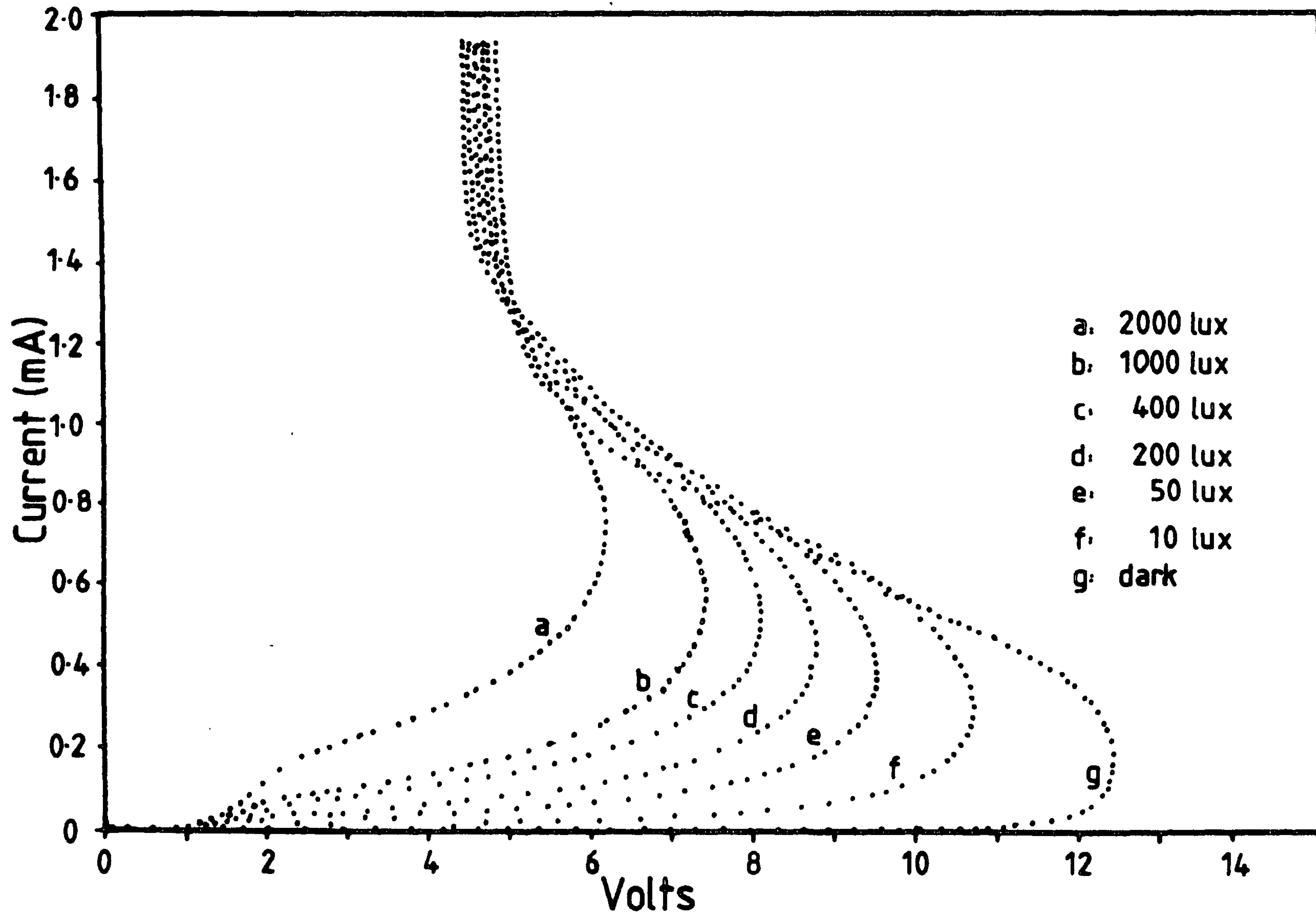


Figure 5.27 I-V characteristics of SRO-MISS with light illumination (sample SRO157, electrode area of $0.96 mm^2$).

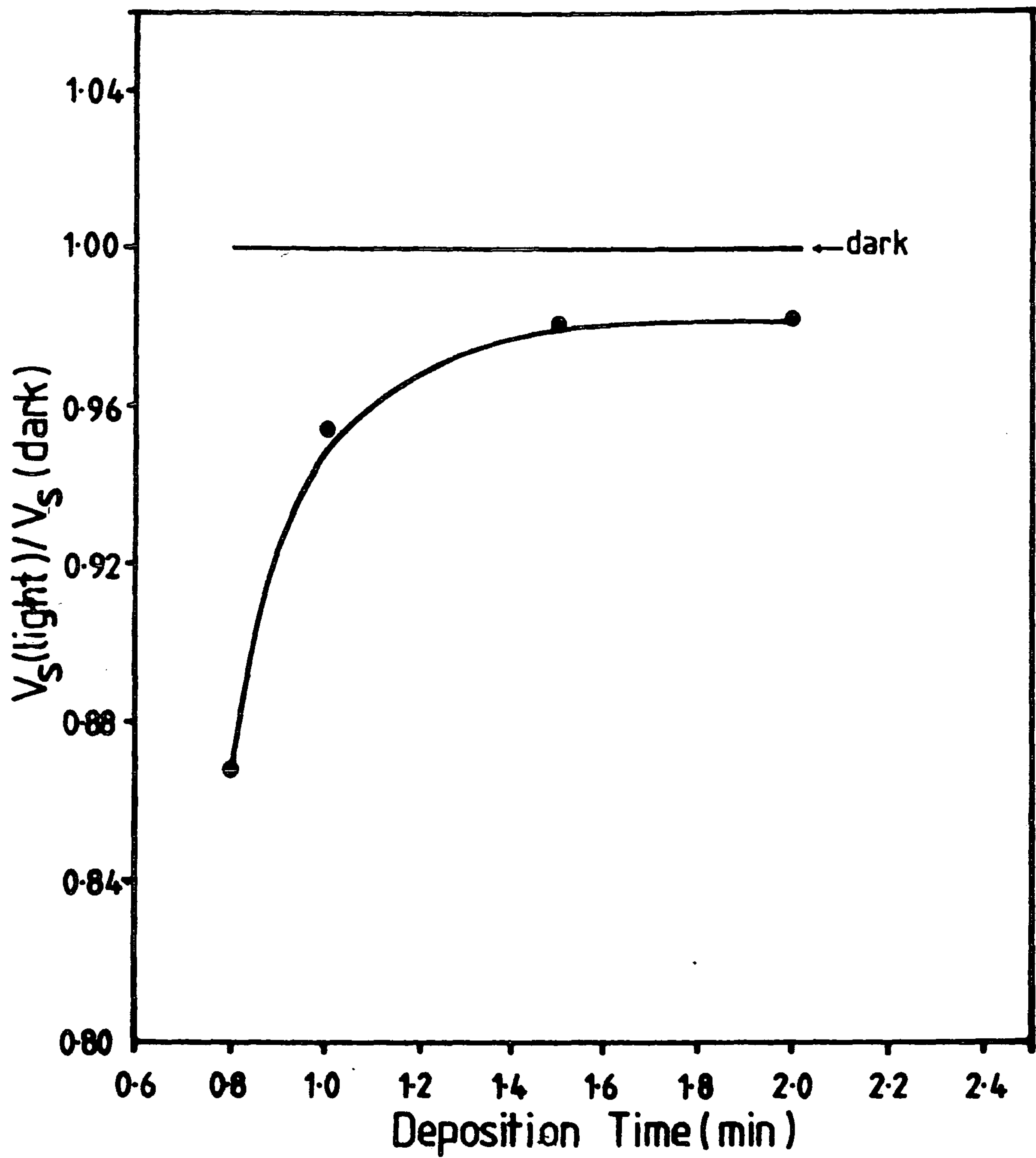


Figure 5.28 Sensitivity switching voltage with the light illumination of 50 lux of the non-isolated MISS versus SRO deposition time ($R_o = 0.2$).

5.9 DEGRADATION

5.9.1 Effect of SRO Film Ageing before Metallisation

In order to study the effects of film ageing on the switching perfomance of the MISS, the SRO was deposited on three slices of the same n-p^+ wafer with the same CVD conditions (R_o = 0.21, 1 minute deposition, T= 650°C). The electrode pattern was made immediately after deposition on one of the samples and the other two were left in clean room air for periods of 13 and 30 days before electrode deposition. Comparative plots of their I-V characteristics are shown in figure 5.29. The switching parameters seem to be decrease for the devices with the SRO surface exposed to the atmosphere. The ellipsometry reading of the film after deposition were n=2.6, d=383 Å, and 30 days later they were n=2.4, d=409Å. This indicated that an atmospheric oxide layer had grown on the top of the SRO. This oxide layer affects the average conduction of the SRO and it probably increases the average percentage of oxygen in the layer. As a result, it becomes less conductive hence reducing the switching parameters.

5.9.2 Device Degradation

The device degradation under the worst operating conditions was studied by biasing the device into the low impedance state. The voltage across the device was measured every 10 minutes for a period of 1000 minutes using a data logger in the Keithley Type 617 voltmeter and the microcomputer. The data was stored automatically in the HP mirocomputer floppy disk from which it could be plotted on the digital plotter. The plot of the voltage across the device against the elapsed time is shown in figure 5.30. After 1000 minutes of continuous operation the holding voltage has

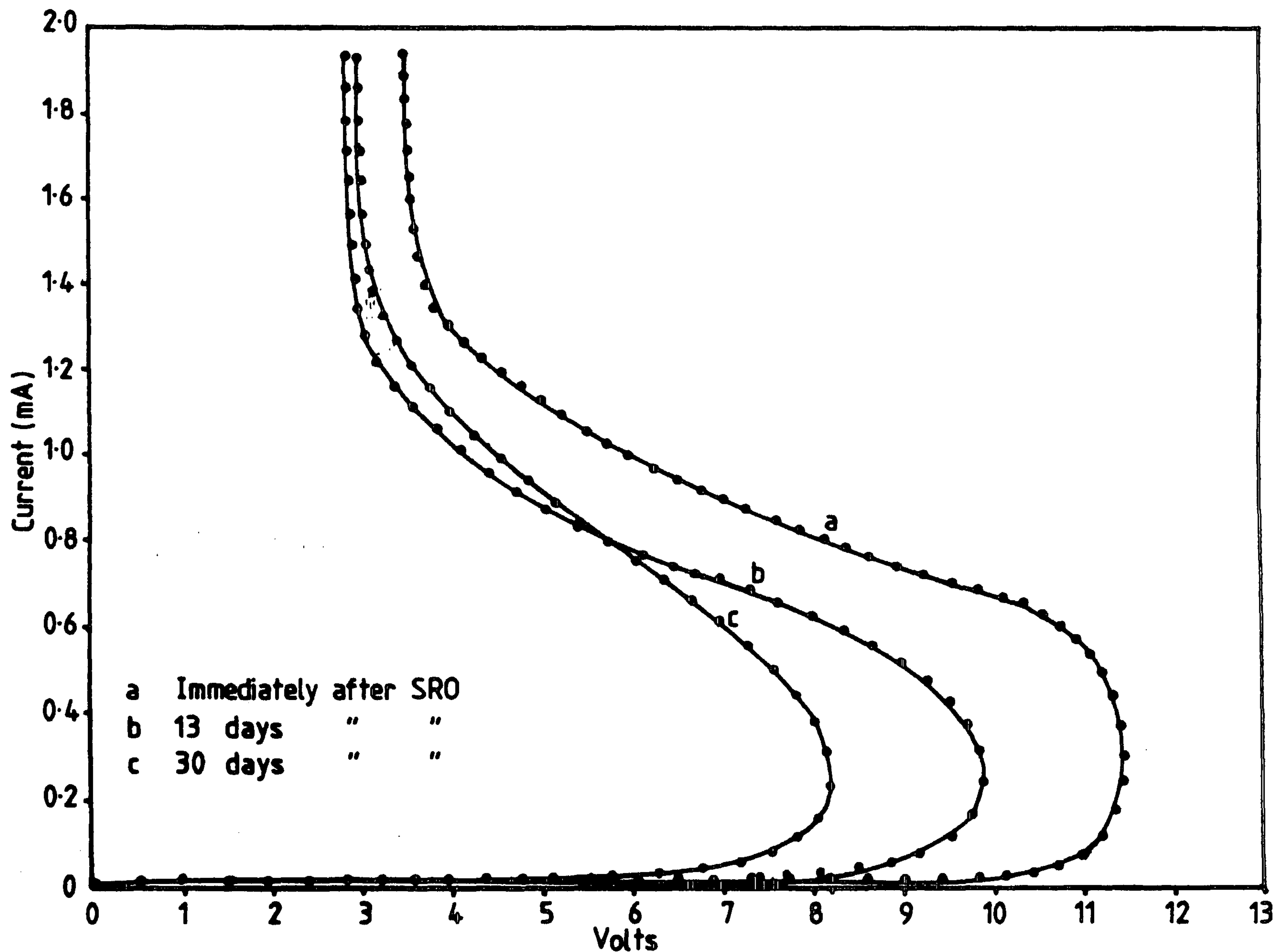


Figure 5.29 Effect of SRO film ageing before metallisation on the I-V characteristic of the non-isolated SRO-MISS device with electrode area of $0.96 mm^2$.

Figure 5.30 Holding voltage of the SRO155 MISS versus operating time. SRO type (d=310Å, n=3.1).

Figure 5.31 I-V characteristic of the SRO155 MISS device before and after 1000 minute of continous operation.

increased to about 0.3 volts from the initial holding voltage. Figure 5.31 shows the I-V characteristics of the device before and after 1000 minutes of continuous operation. As we can see only the holding voltage has changed and the other parameters were not affected. The reasons for this were not known but it was believed that a redistribution of an interface charge had taken place due to the high electric field when the device is biased in the low impedance state.

5.10 DYNAMIC CHARACTERISTICS

5.10.1 Introduction

When a voltage pulse with a magnitude greater than the switching voltage is applied to the MISS another phenomenon can be observed. Buxo et al [4] reported that there is a delay time before switching takes place. The delay time decreases as the applied pulse height increases. This dynamic response is nothing to do with the external circuit but it is controlled by the internal switching mechanism of the device. The switching voltage was also reported to be dependent on frequency and this phenomenon also has been attributed to a charge storage effects [5].

As the device is switched ON holes (minority carriers) are accumulated at the semiconductor–semi-insulator interface to form the inversion layer. The total storage charge in the ON state is also contributed by a diffusion charge in the epitaxial layer which is occupying most of the thickness of the epitaxial layer from the junction to the interface. When the injected current through the device is suddenly terminated the stored charge (holes) will not vanish immediately but it will decay with a certain relaxation time τ before reaching equilibrium as determined by the bulk and surface recombination rates. Thus the switching voltage measured for a second pulse at any

time in the interval $0 < t < 3\tau$ has a value less than that measured at $t = 0$. By assuming that the excess minority carrier concentration decays exponentially with time according to an effective lifetime τ_{eff}, the variation of V_s with time is given by [5,7]

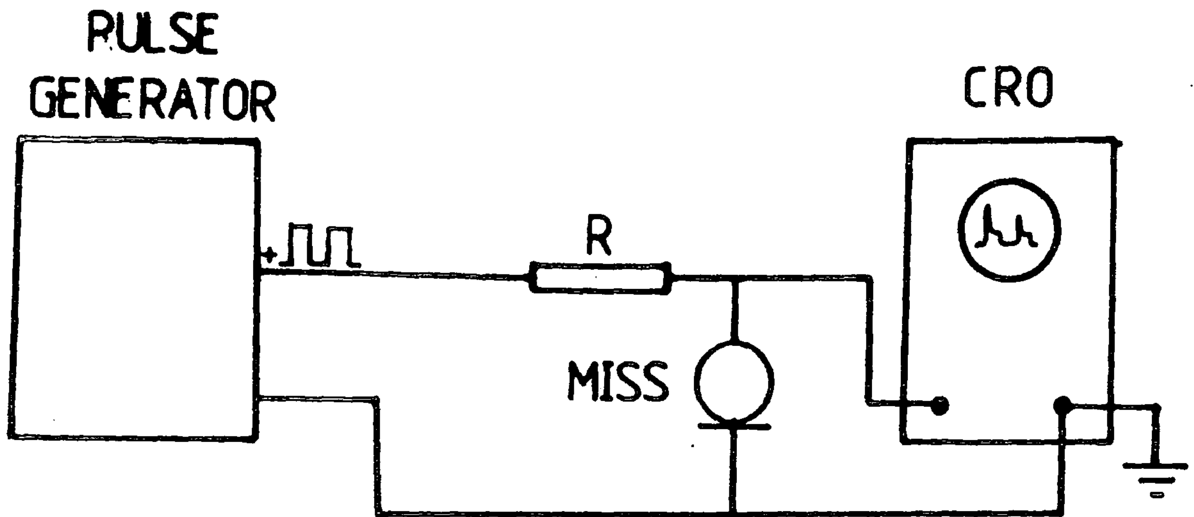
$$V_s = \frac{V_s(0)}{\left[1 + I_{inj} B \exp(\frac{-t}{\tau_{eff}})\right]^2} \qquad 5.25$$

where τ_{eff} is determined by both bulk and surface recombination terms, B is a constant which depends on device parameters, and I_{inj} is the injected current in the ON state. This expression is valid with the assumption that the generation and diffusion effects in the depletion layer are neglected.

5.10.2 Double Pulse Technique

The technique used by Phan et al [7] was employed to investigate the dynamic characteristics of SRO-MISS devices using double pulses of variable duration. Figure 5.32(a) shows a schematic diagram of the double pulse measurement technique. A pair of pulses was applied from a Philips Type PM5716 pulse generator, and the MISS device was connected in series with a 475Ω resistor. The amplitude of the pulses has to be higher than the static switching voltage in order to avoid the switching-on delay [4,9]. The output voltage, corresponding to the voltage across the MISS, was sent directly to a high speed oscilloscope where the switching voltage and the pulse separation time were measured.

Figure 5.32(b) shows a typical output on the oscilloscope displaying the switching voltage versus delay time. The switching voltage V_{s_2} measured by the second pulse was less than V_{s_1} measured by the first pulse. This is because after the end of



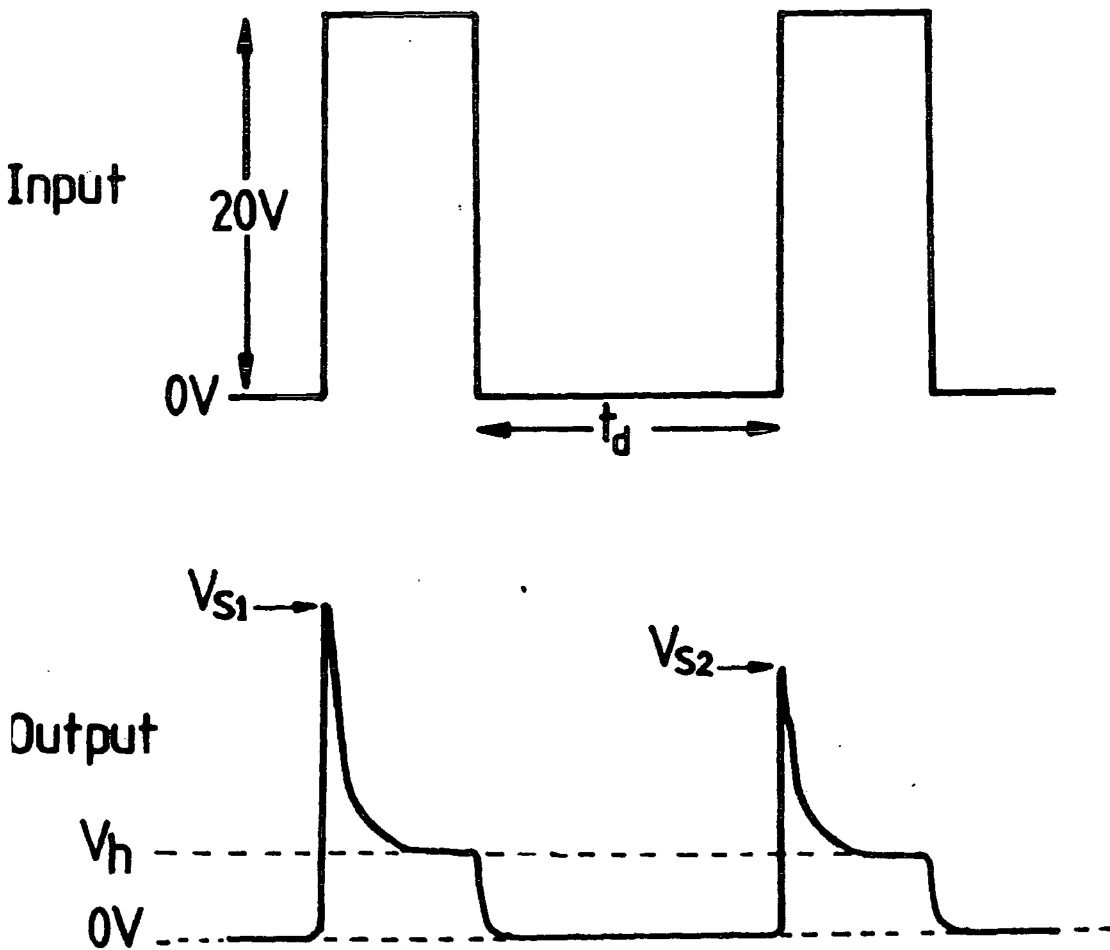


Figure 5.32 a) Double pulse measurement circuit.

b) Input and output waveform.

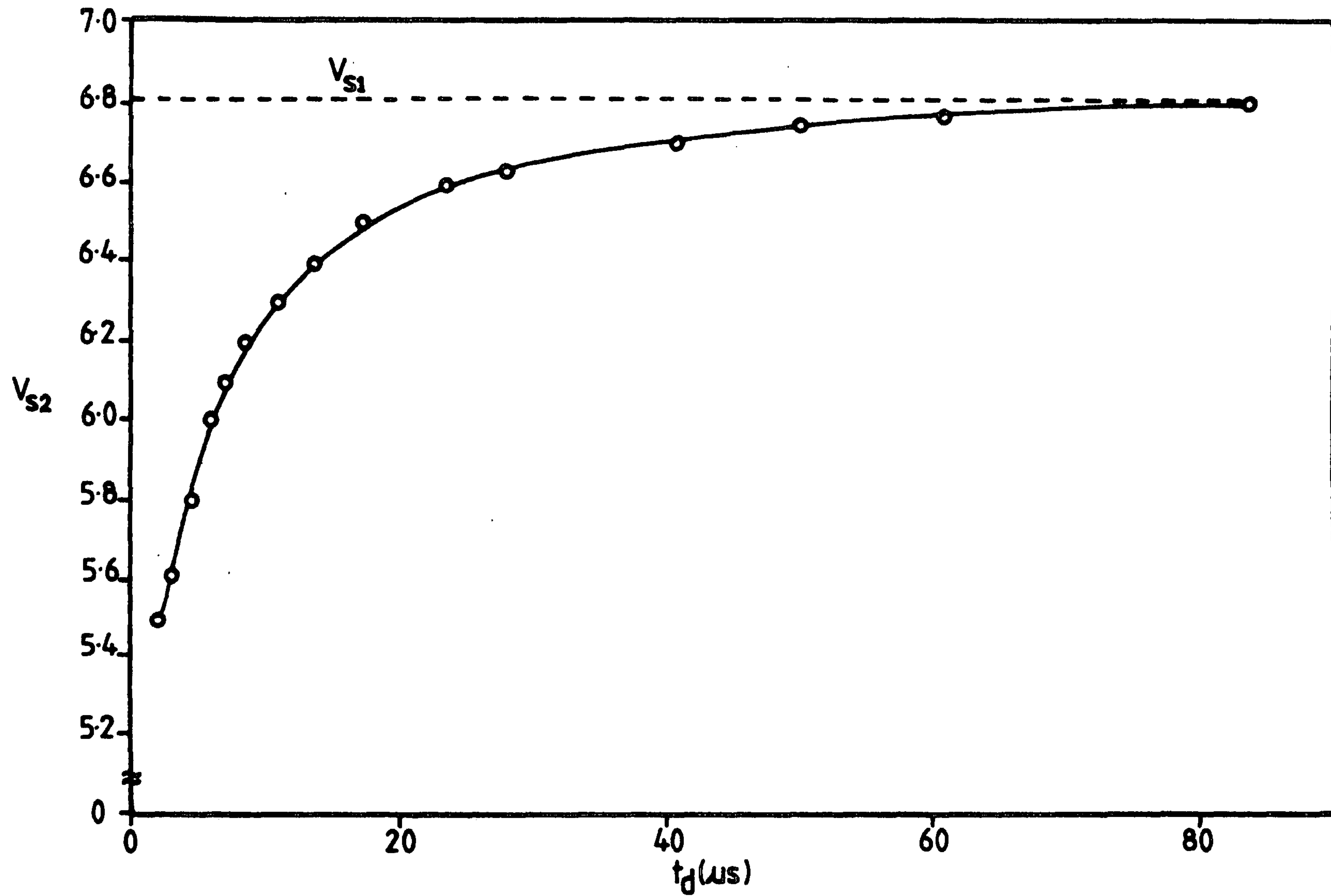


Figure 5.33 Switching voltage measured by second pulse V_{s_2} versus delay time between pulses.

the first pulse the holes are present at the interface which decay with the relaxation time. If the second pulse arrives while some of the accumulated holes are still present a smaller voltage is required to turn the device ON. Figure 5.33 shows a plot of the switching voltage as a function of delay time t_d for an SRO-MISS device with an electrode diameter of 1.06mm. The switching voltage V_{s_2} increases as the the separation between the two pulses is increased until $V_{s_2} = V_{s_1}$. This result was as expected.

5.10.3 Effect of Heat Treatment on Dynamic Characteristics

After the measurements had been done on the sample SRO123, giving the result shown at (a) in figure 5.34, it was annealed at 400°C for 5min in a nitrogen ambient. The measurement was repeated on the annealed sample and the result is at (b). On the annealed sample the switching voltage V_{s_2} was found to be less than V_{s_1} for only a short period ($< 1\mu s$), increasing very sharply and reaching a maximum value greater than V_{s_1}. It then decreases gradually until $V_{s_2} = V_{s_1}$. For comparison a similar measurement was done on a tunnel-oxide MISS and the same effect was also observed as shown in figure 5.35. A similar study made by Phan et al [8,10] who accounted for the effect in terms of electron traps at the insulator-semiconductor interface. This suggests that heat treatment on the sample with aluminum electrode causes interface states or traps to be formed.

The effect of electron traps can be seen with the aid of the energy band diagram of the MISS as depicted in figure 5.36. At equilibrium, all the interface states below the Fermi level are filled with electrons. With the arrival of the first voltage pulse of amplitude higher than the dynamic switching voltage the switching action takes place from the high to the low impedance state and the interface state above the Fermi level is partly filled with electrons (figure 5.36(b)). At the end of the first pulse the device is turned off but the hole concentration and the captured electrons do

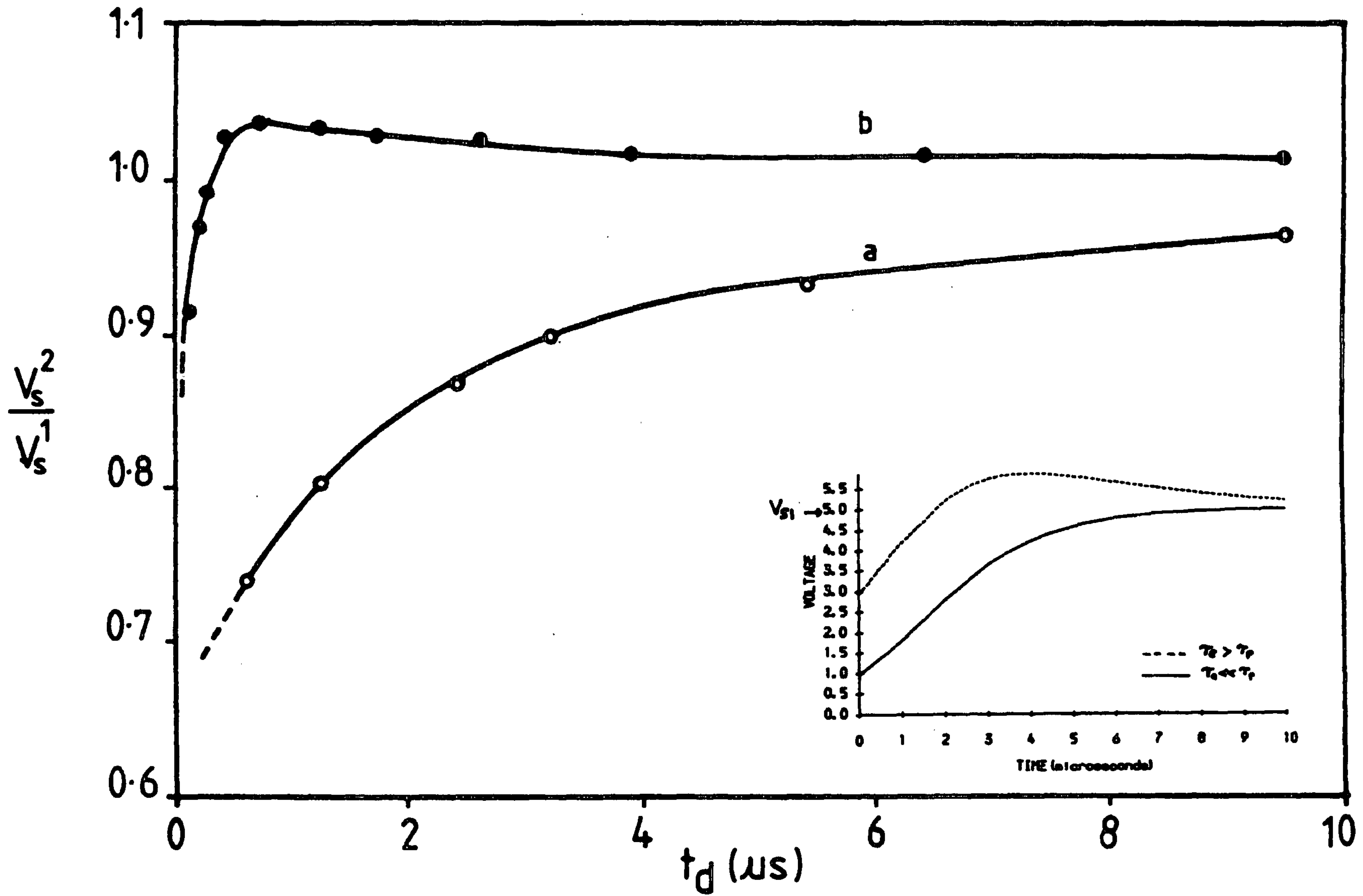


Figure 5.34 Comparison between double pulse results of the as-made (a) and annealed (b) MISS devices. The theoretical curve based on punch-through model is shown in the small diagram.

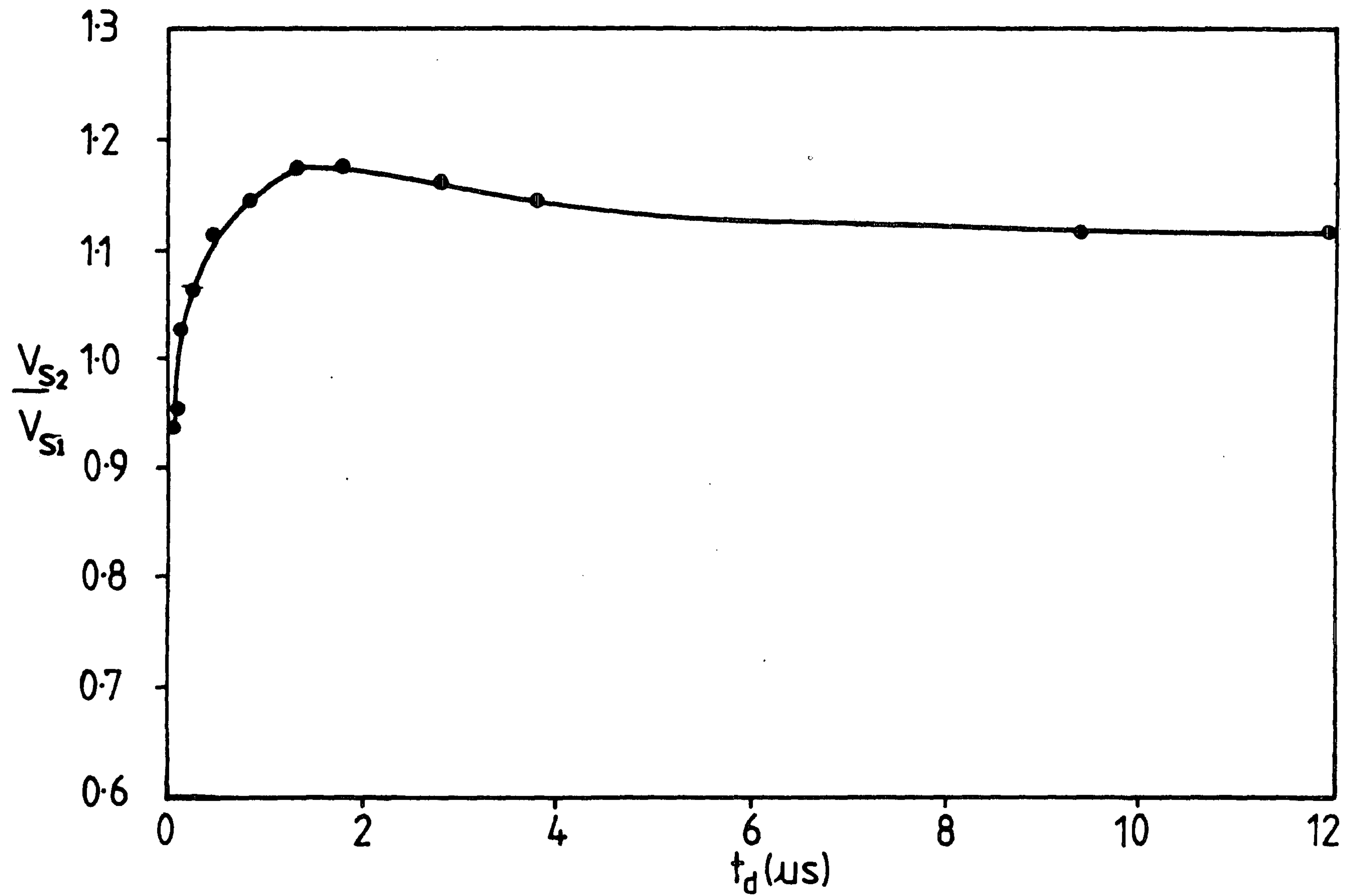


Figure 5.35 Double pulse result of the tunnel oxide MISS.

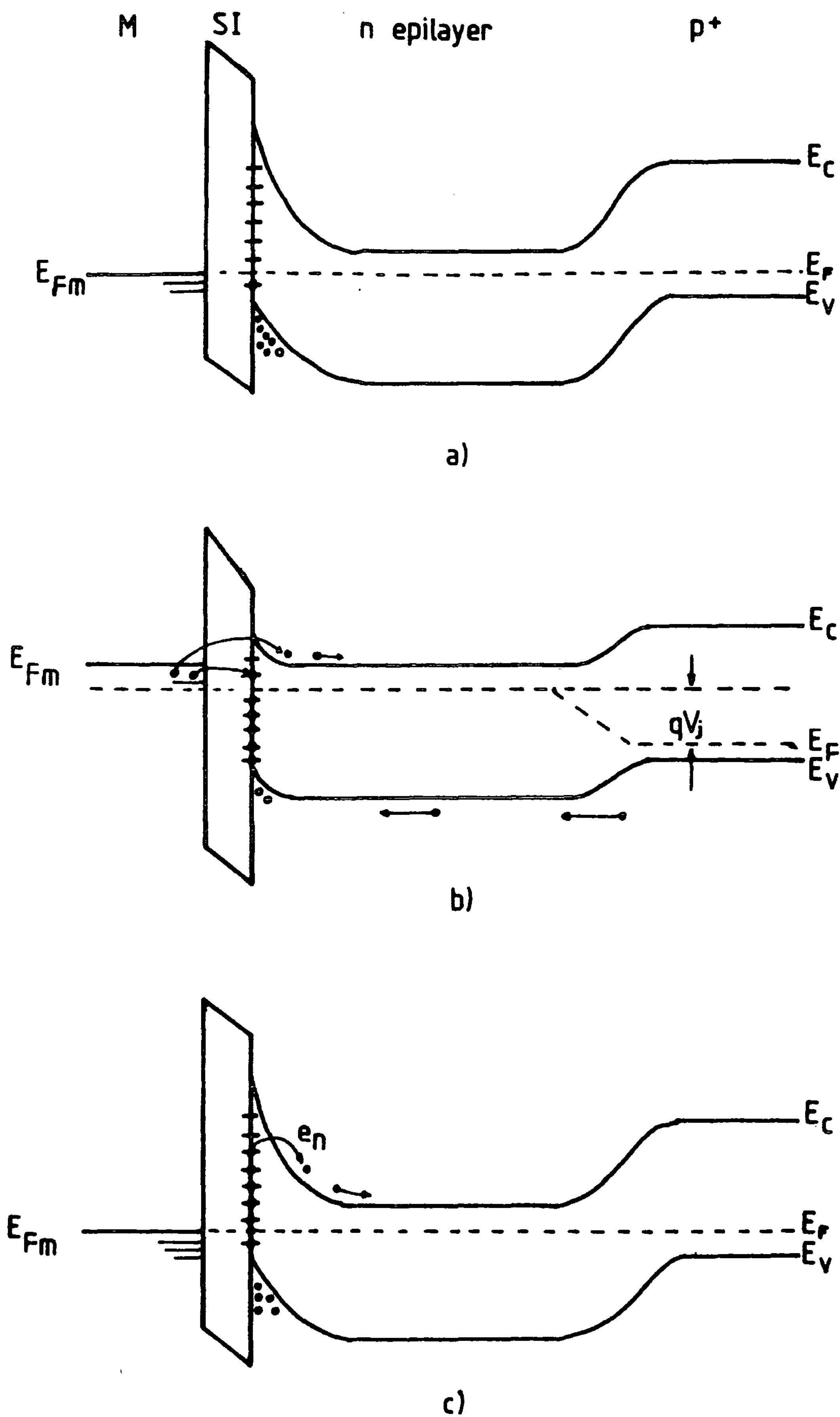


Figure 5.36 Energy band diagrams showing the effect of interface traps on dynamic switching voltage.

a) Interface traps are in equilibrium (steady state).

b) The MISS in On-state and traps are filled by electrons.

c) After termination of electrical pulse, the traps are in non-equilibrium state.

not dissapear instantly, but they take a certain relaxation time to return the system to equilibrium (figure 5.36(c)). Holes stored and electrons trapped in the n-region will cause the switching voltage as measured by the second pulse to be at first less and then higher than that measured by the first pulse. Based on the punch-through switching mechanism Phan et. al [6] have proposed an expression which shows the variation of V_{s_2} with t_d which can be written as,

$$V_{s_2} = \frac{qN_d}{2\epsilon_o\epsilon_s}\left[\frac{\epsilon_o\epsilon_s\xi + N_t\exp(-t_d/\tau_e)}{qN_d + p_{inj(o)}\exp(-t_d/\tau_p)}\right]^2 \qquad 5.26$$

where $p_{inj(o)}$ is the concentration of the holes injected during the on-state and ξ is the threshold field strength in the semi-insulating layer which is necessary to initiate the switching process [9], τ_p is the hole lifetime, and τ_e the electron emission time from the interface traps. This expression can be simplified to,

$$V_{s_2} = V_{s_1}\left[\frac{1 + \alpha\exp(-t_d/\tau_e)}{1 + \beta\exp(-t_d/\tau_p)}\right]^2 \qquad 5.27$$

For $t_d \gg \tau_p$, the hole storage effect is dominant so that V_{s_2} is less than V_{s_1} and it increases as t_d is increased. The maximum value of V_{s_2} depends on the trap concentration and the electron emission time [8]. If the electron emission time is greater than the hole lifetime, the maximum value of V_{s_2} will be greater than V_{s_1}. The number of electrons in the interface state gradually reduces by thermal detrapping and this will cause V_{s_2} to decrease until $V_{s_2} = V_{s_1}$. The theoretical curve plotted using equation 5.27 based on the punch-through model with $\tau_e = 2.8\mu s$ and $\tau_p = 1.5\mu s$ is shown at the bottom right of the figure 5.34. This gives strong evidence for trap formation due to heat treatment.

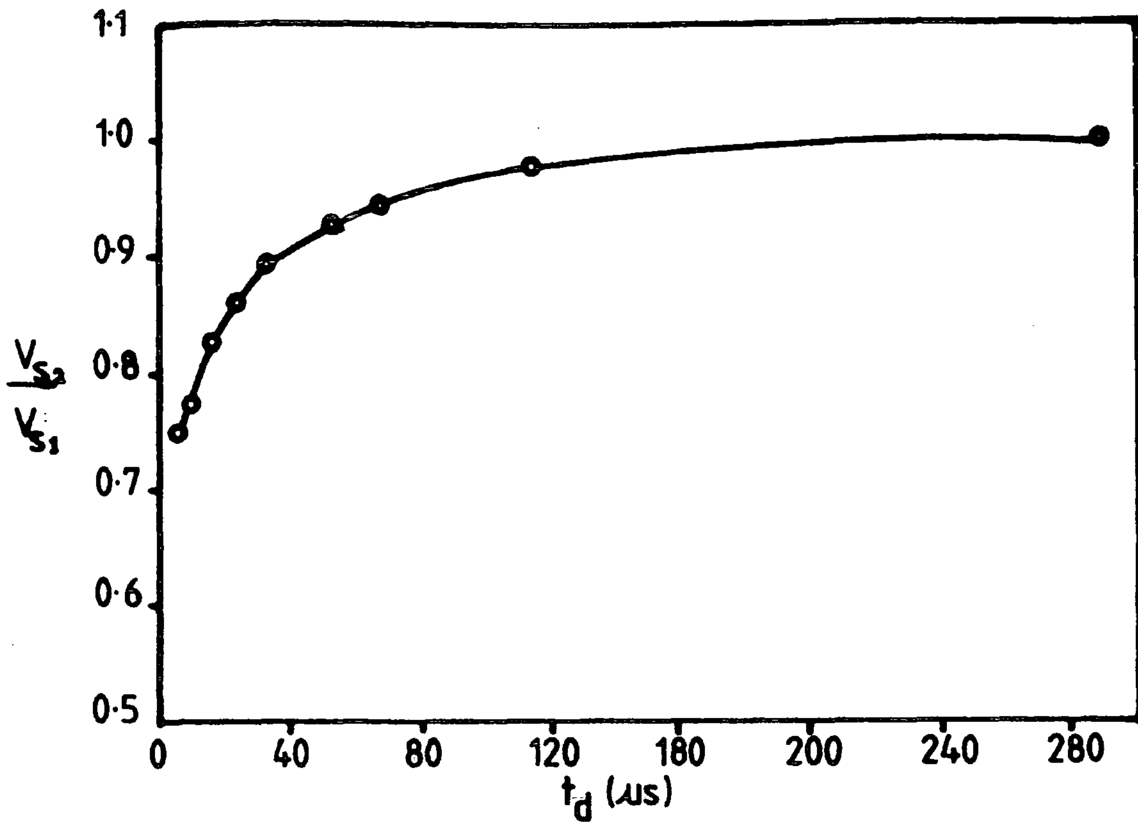
5.10.4 Effect of Gold Doping on Dynamic Characteristics

The effect of charge storage can be reduced by introducing a minority-carrier lifetime killer and this can be easily archieved by diffusing gold into the device. Using a double pulse technique the effect of gold recombination centres was investigated. The device with the electrode area of 2.73mm^2 was chosen from the sample SRO187 with a 10 minute gold diffusion because it has low V_s needed to cope with the maximum pulse height of 20 volts from the pulse generator. For comparison, the measurement was also performed on the device which has the same type of SRO but without gold doping. As we can see in figure 5.37, V_{s_2} for the device without gold doping takes about $280\mu s$ to be equal to V_{s_1}. However, V_{s_2} for the device with gold doping has a higher value than V_{s_1} at least at short delay times although it becomes equal to V_{s_1} at $12\mu s$. This shows that the diffusion treatment introduces interface traps and that the bulk recombination is greatly increased probably because of the gold. Hence by introducing the gold impurity into the device, the switching off time can be greatly speeded up.

5.10.5 Effect of Double Pulses with Negative to Positive Voltage Swing

As has been demonstrated previously, if the MISS device contains traps the switching voltage measured by the second pulse is higher than that measured by the first pulse. However it has also been found for the first time that if the input pulse voltage swings from a negative to a positive level *, the switching voltage measured by the second pulse was at first less than, and then higher, than that measured by the first pulse even if the device does not contain traps as shown in figure 5.38. In

* These are the voltages applied to the substrate at the MISS device with the top electrode earthed



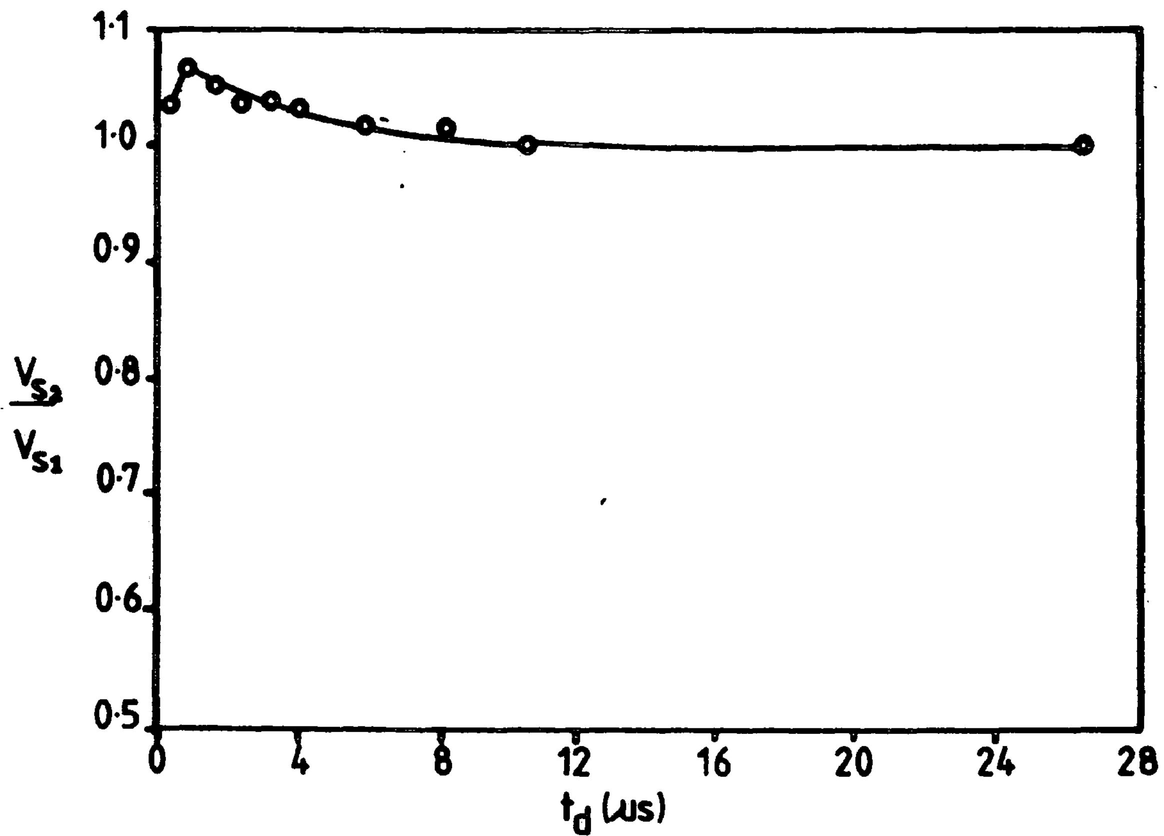


Figure 5.37 Switching voltage measured by second pulse, a) without gold doping and b) with gold doping.

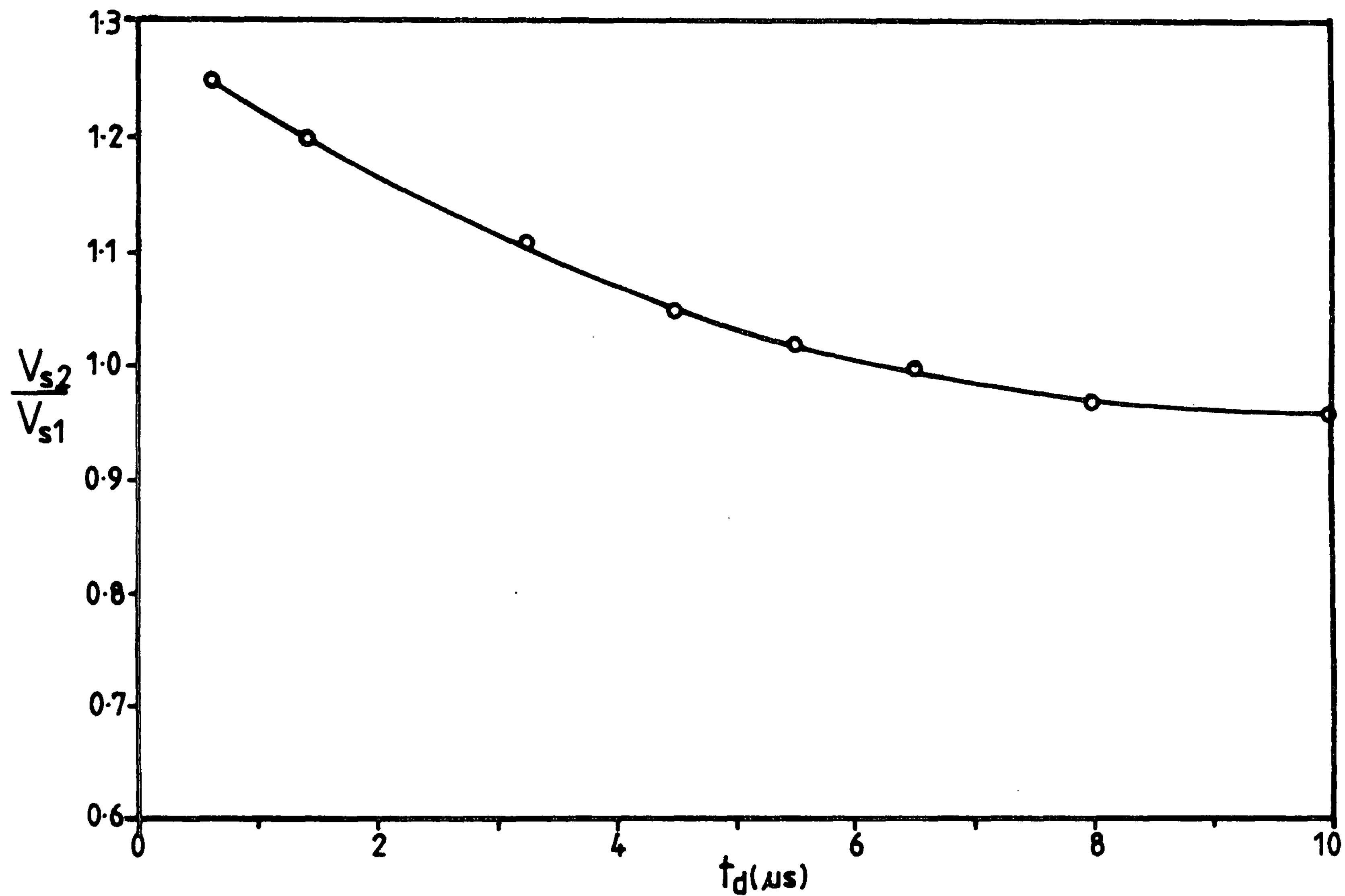


Figure 5.38 Effect of voltage swing from negative to positive in the double pulse measurement.

this experiment, sample SRO123 was used before heat treatment. This phenomenon is described as follows.

During the negative swing (positive potential on the electrode) the device is reverse biased and electrons are accumulated at the interface. When the pulse is positive (negative potential on the metal) the device is turned ON and, the accumulated electrons at the interface take a certain relaxation time to disappear. As a result, a relatively higher voltage is needed to turn the device ON from the reverse biased condition. This effect is the opposite to the case of the hole storage effect, where $V_{s_2} < V_{s_1}$. The increase of the switching voltage measured by the second pulse can be explained using the same argument as for the case of the electron trapping effect, i.e the electrons must be removed. In this case it is the accumulated electrons that contribute to the effect instead of the trapped electrons.

5.11 SUMMARY

In the first section of this chapter, the current-voltage relationship of the SRO-MIS diode was studied. The forward biased current of the SRO-MIS is strongly dependent on the SRO type while in the reverse biased case, the voltage at which the reverse saturation current becomes appreciable is also dependent on the SRO type. The reverse saturation current of the MIS is sensitive to light illumination because of the photogeneration of electrons and holes in the surface depletion region. The sensitivity also seems to be dependent on the SRO type. The current-voltage characteristics are found to be influenced by the metal contact and a gold contact gave a lower current than an aluminum contact.

In the second section, the switching behaviour of the MISS devices was studied as a function of the goemetrical shape. It was found that the MISS characteristics are

very dependent on the area of the electrode as well as the area of the p-n junction. If the ratio of the electrode area to the p-n junction area is decreased the switching voltage increases. This is because a fraction of the current through the electrode flows laterally (current spreading), and increases the switching voltage of the device. The effect of current spreading in the device was shown more convincingly in further experiments on isolation, the effect of a metal guard ring, and the effect of the electrode perimeter. The degree of the current spreading was found to be dependent on the conductivity of the SRO layer which alters the sensitivity of the switching parameters to the geometry.

The dependence of the switching characteristics of the MISS on others parameters such as SRO deposition time, gold diffusion, and light illumination was also studied. It was found that the thickness and composition of the SRO films strongly influences the switching of the MISS. Increasing the deposition time will increase the switching and holding voltages. As expected, the gold diffusion will reduce the switching voltage but increase the holding voltage.

Finally, the charge storage effect in SRO-MISS interfaces was studied by means of a double pulse technique. The experiments show that the effect of charge stored during the low impedance state delays the turn-off process. This effect can be reduced by gold doping which creates recombination centres in the epilayer region.

From the experimental results in this chapter we can reach the general conclusion that the MISS structure is a very complex device. Its behaviour is critically dependent on various parameters. However all the results are consistent with theoretical explanations including current spreading, the effect of metal work function and of interface states.

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CHAPTER SIX

ELECTRICAL CHARACTERISTICS OF THREE TERMINAL SRO-MISS DEVICES

6.1 INTRODUCTION

Any two terminal device becomes more useful in circuit applications if the electrical behaviour can be controlled by external electrical signals and the interaction with other devices can be made through a third terminal. The unijunction transistor (UJT) and SCR(thyristor) are examples of electronic switching devices in which the operation can be controlled from the third terminal. A certain amount of work has been done previously to study the switching behaviour including the switching speed of MISS devices with three terminals [1,2,5,6].

Through the third terminal the electrical characteristics of the MISS device in reverse and forward biased can be altered. When it is biased in the switching direction, it behaves like a thyristor where the switching action can be controlled by applying an external current or voltage pulse. This type of three terminal MISS device was named MIST for Metal-Insulator-Semiconductor Thyristor[6]. On the other hand, if reverse biased it has been shown that [1,2] that the device exhibits transistor-like characteristics. In this chapter the electrical behaviour of all the three terminal MISS devices that have been reported using tunnel oxide films will be examined in a preliminary way for SRO-based structures. It will be found that both forward and reverse bias characteristics are very similar. Some results on the effect of device area are new. In addition a new characteristic of the three terminal MISS in the reverse

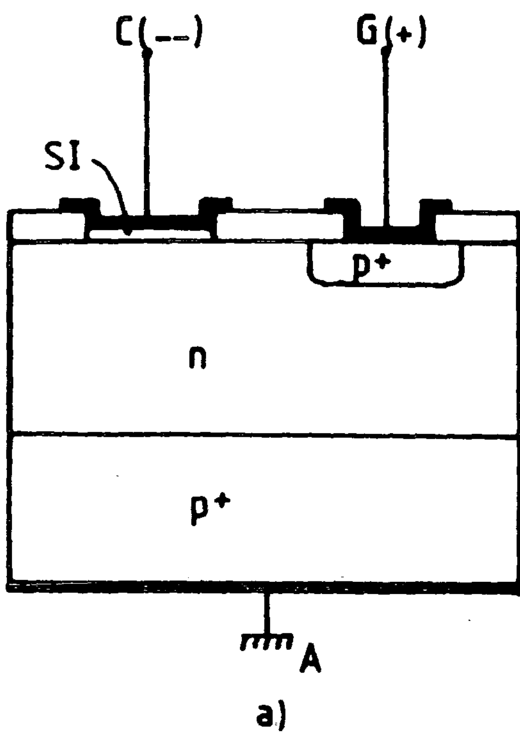
bias direction has been observed in the course of this work, where under certain circumstances the transistor characteristics contain an N-type negative resistance.

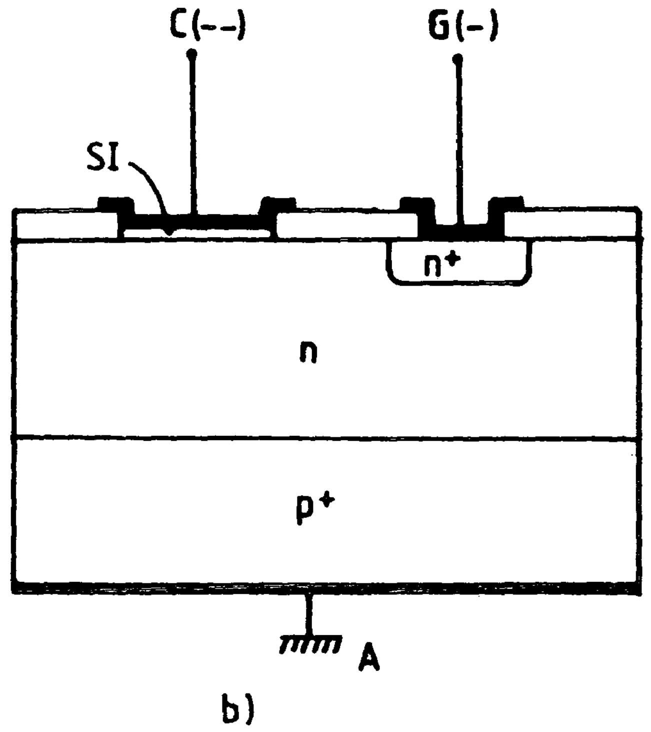
6.2 THE MIS-THYRISTOR (MIST)

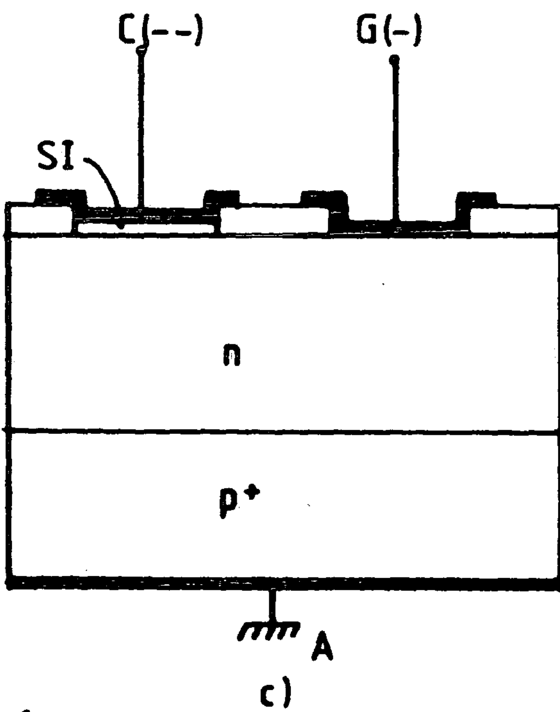
6.2.1 Introduction

The switching voltage of the MISS can be controlled by injecting extra minority or majority carriers into the depletion region. The former can be injected by means of a p^+ diffused region (figure 6.1(a)) and the latter through an n^+ diffused region (figure 6.1(b)) or through the Schottky barrier diode which can be formed on the epitaxial layer (figure 6.1(c)). In the first structure the holes (minority carriers) are injected directly from the forward biased p^+ diffused junction and they travel towards the semiconductor-insulator interface. In the second the hole injection from the substrate n-p^+ junction is enhanced by increasing the forward bias applied to the n^+ diffused region forming the third electrode and this has been called a majority carrier injection type of MIST. For both types of MIST, the metal electrode on the semi-insulator is referred to as an emitter, the epitaxial layer with the p^+ or n^+ diffusion as a base, and p^+ substrate as a collector.

El-Badry [8] suggested another way of triggering the switching of a MISS device, where an MOS gate was formed adjacent to the emitter electrode and used to control the p^+-n junction injection as shown in figure 6.1(d). Nassibian et al. [11,12] have shown that the switching voltage can also be controlled using an MOS gate in this way. This type of device offers a high impedance gate since almost no current flows through it and it is also a compact structure and provide a higher packing density if fabricated as an integrated circuit. However, the MIST of the majority carrier injection type has







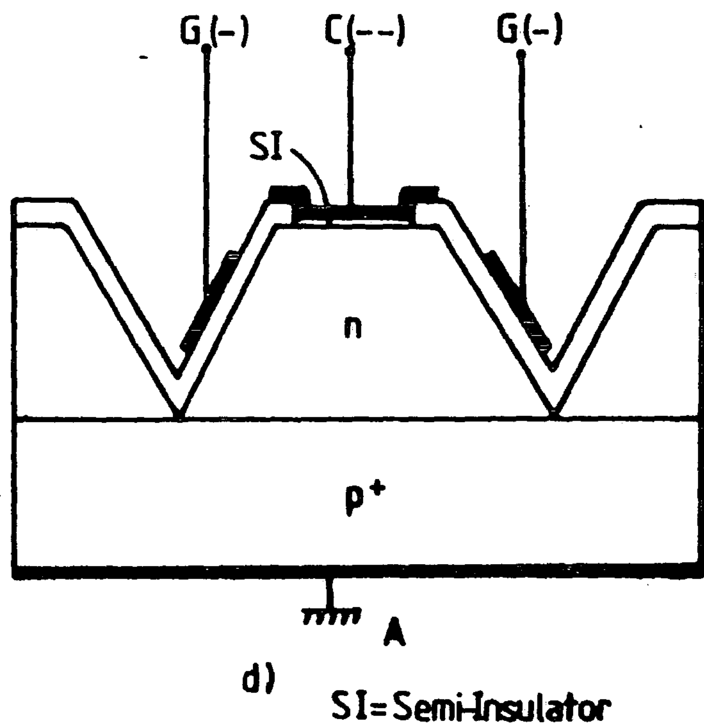


Figure 6.1 Type of gate control in the MIST (from ref. 7)

a) Minority carrier injector.

b) Majority carrier injector: n^+ diffusion.

c) Majority carrier injector: Schottky barrier.

d) Field gate.

been proved convincingly to be the most sensitive method of controlling the switching voltage [7].

6.2.2 Theory of Operation

Figure 6.2 shows the energy band diagrams which describe the operation of the MIST device shown in figure 6.1(b). The energy band diagram in the high impedance state with no base current flowing is shown in figure 6.2(a). When base current is introduced by applying a negative potential to the third terminal some of the electron current from the third terminal recombines with holes in the p^+-n (collector-base) junction and some of it diffuses through the junction towards the substrate, hence increasing the forward bias of the p^+-n junction (figure 6.2(b)). As a consequence the hole injection current from the junction increases and some of it travels to the interface. The increase of hole concentration at the interface induces more electron current from the metal electrode to flow in through the semi-insulator and when the total gain of the internal system becomes unity the device begins to switch at a voltage lower than that without the base current as in the two terminal device. Increasing the base current causes a relatively large number of holes to be injected from the p^+-n junction into the n-epilayer and induces a lot more electron current from the emitter electrode. As a result, the device enters the low impedance state. Once the device has switched to this state, removal of the base current will have no effect on it since the electron current is sufficiently large to keep the p^+-n junction ON (figure 6.2(d)).

The MIST device can be operated in two modes, a monostable mode if the third terminal is used only for turning the device ON, and a bistable mode if the device can be turned ON and OFF through the third terminal. Figure 6.3 shows the basic circuit arrangement and the bias point for both modes of operation. The switching

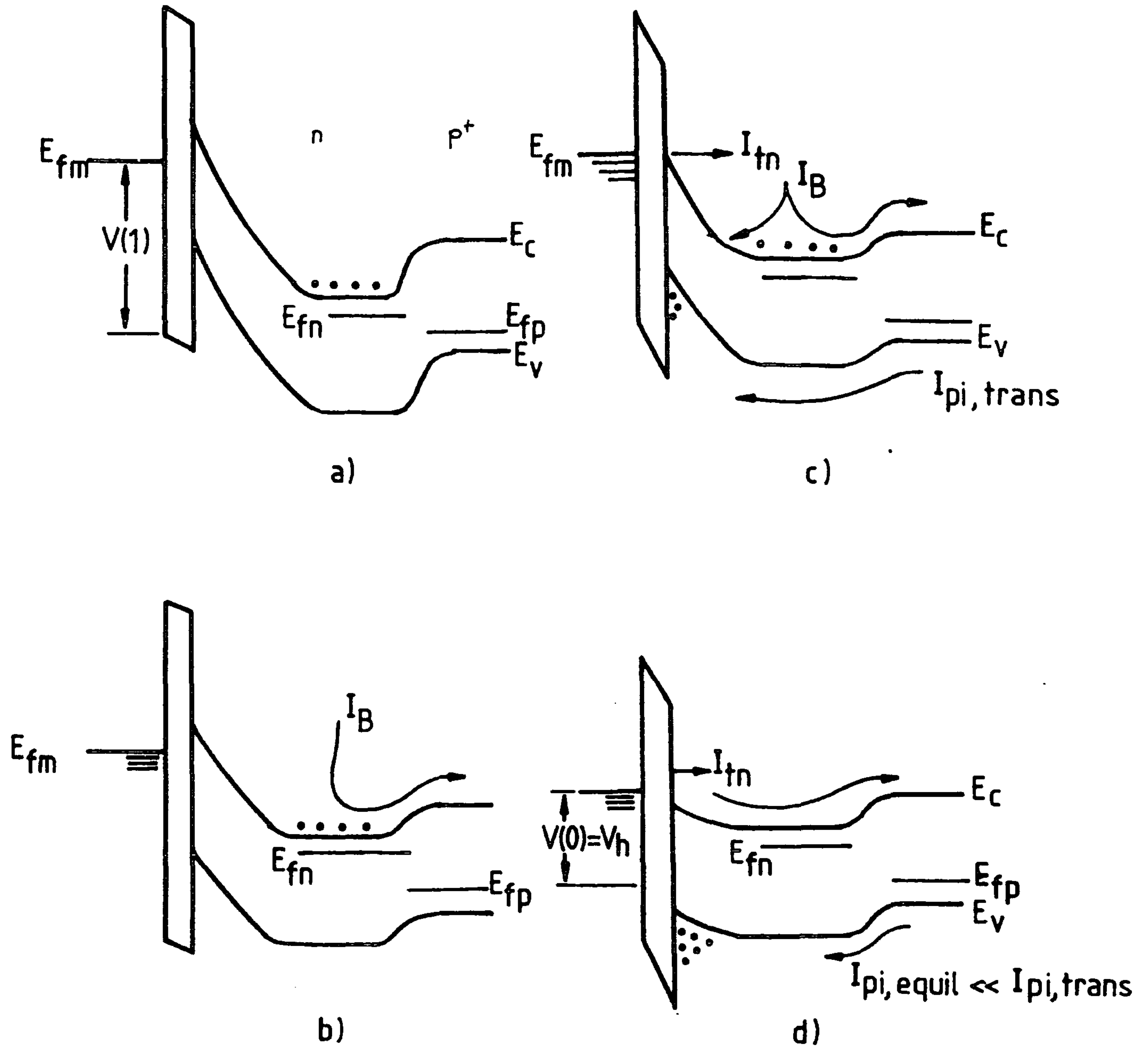
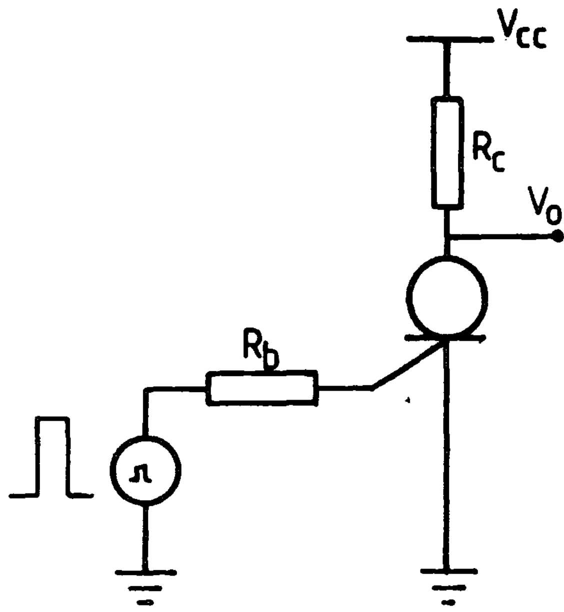
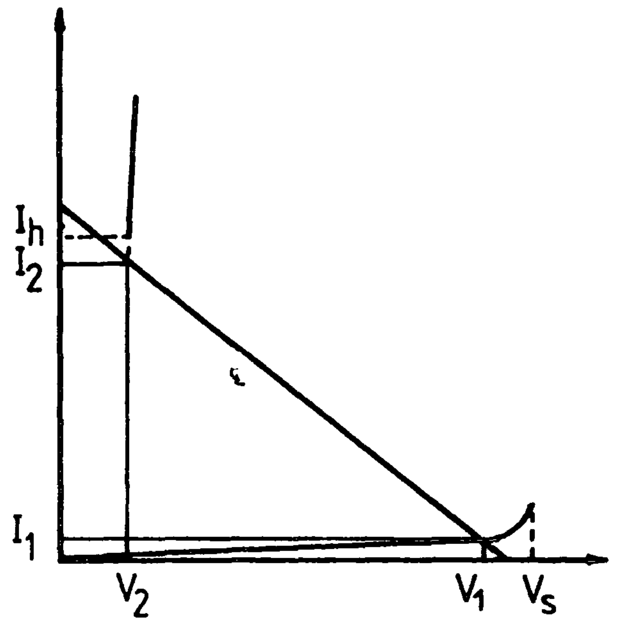
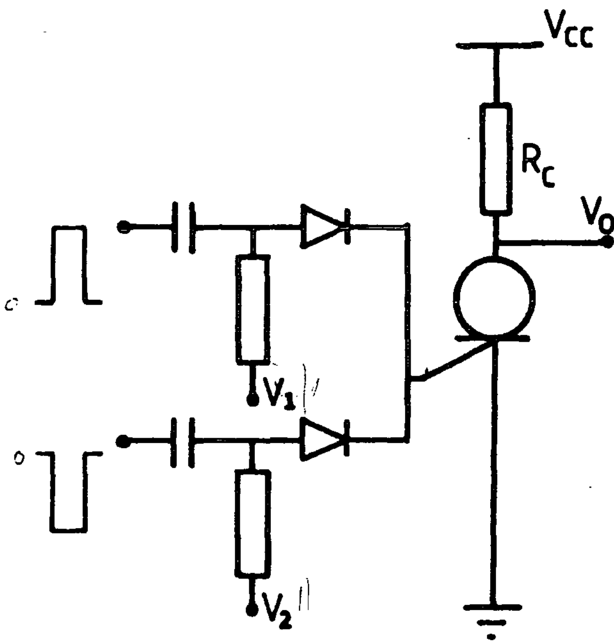


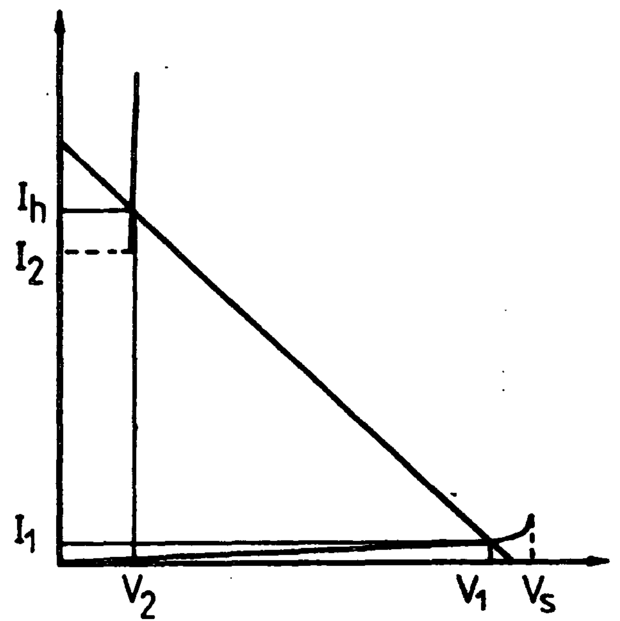
Figure 6.2 The energy band diagram of MIST **a)** in the off-state, **b)** base current is applied, **c)** onset of switching and **d)** in the on-state.





a)





b)

Figure 6.3 **a)** Monostable mode of operation, **b)** Bistable mode of operation.

transients in MIST circuits in both monostable and bistable modes have been analysed by Nassibian [9,10], who showed that the turn-on and turn-off times are sensitive to the driving base current and bias point. It was also shown that the turn-on delay time can be reduced by reducing the base width (epi-layer thickness) [2,9]. Kroger and Wegener [5] reported a 10 ns turn-on time for an epilayer thickness of 2-3μm. Simmons and Taylor concluded that the switching speed of the MIST device was too slow for memory applications [2]. However the control of the switching voltage is still important because the negative resistance and capacitance of the device are strongly dependent on the switching parameters (V_s, V_h, I_s, I_h).

6.2.3 Effect of Base Current on Switching Characteristics

Measurements were done on wafer no.1 of the Southampton process (see section 5.3) using MIST devices with the typical cross-sectional view shown in figure 6.4. These devices have gate electrodes G_1 and G_2 connected to p^+ and n^+ diffusions respectively to enable both types of triggering control to be investigated. Most of the measurements used the n^+ gate, G_2. The emitter areas were $20 \times 20\mu$m, $40 \times 40\mu$m, $80 \times 80\mu$m and $160 \times 160\mu$m, and the devices were isolated by V-grooves with an area of $240 \times 240\mu$m. The separation between the MISS electrode and the n^+ diffused region was 10μm. The device was characterised using a steady state technique with the Keithley Programmable Current Source 220 used to supply a constant base current. The measurement was performed in conjunction with the automated measurement system as described in Chapter 4 and the measurement circuit is shown in figure 6.5.

The switching characteristics of the device are shown in figure 6.6. The amount of a base current required to turn the device ON depends on the biasing voltage in the OFF state. The current triggering capability of the MIST can be interpreted by the term of *control efficiency*, which is defined as the incremental change in switching volt-

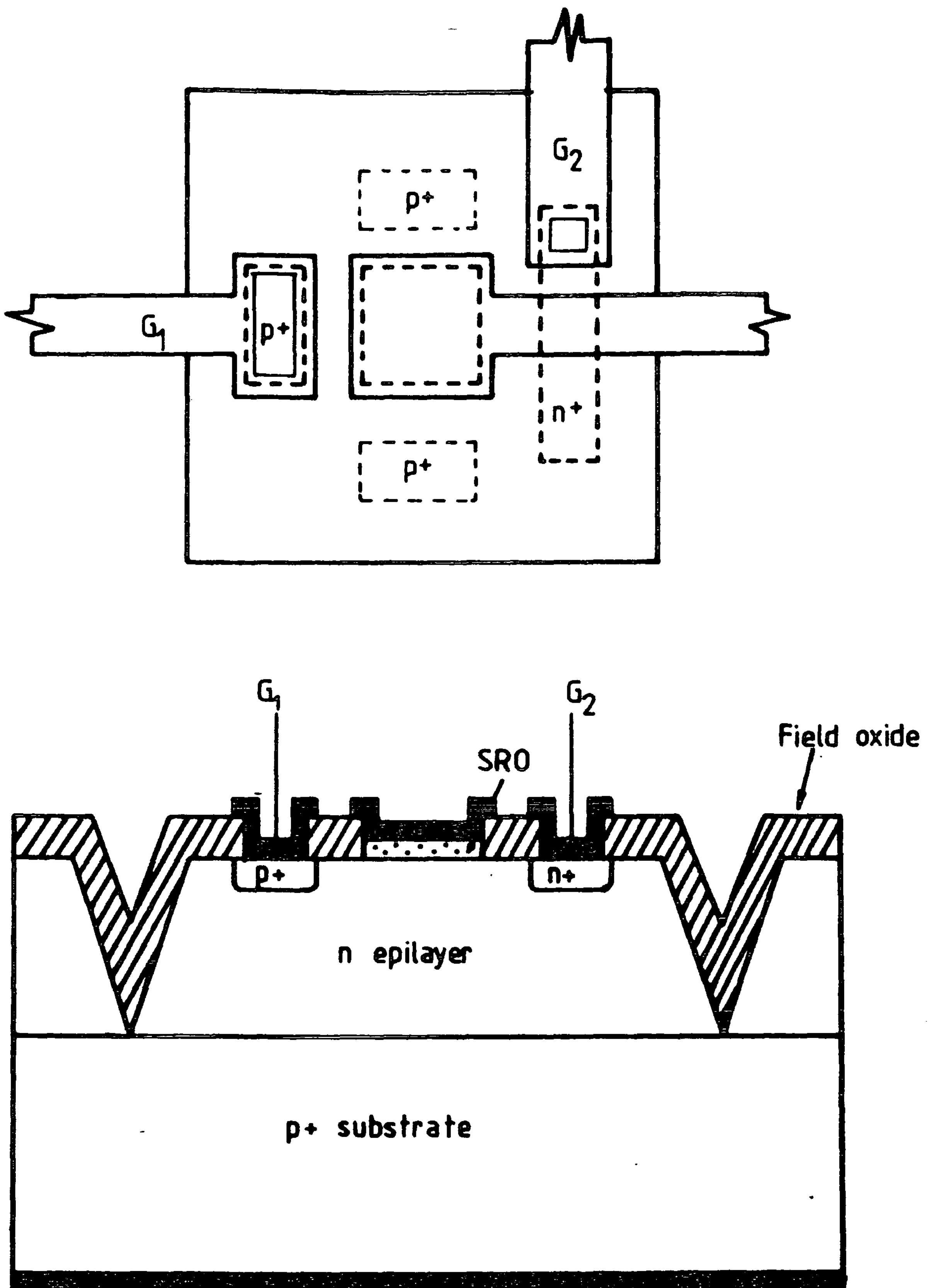
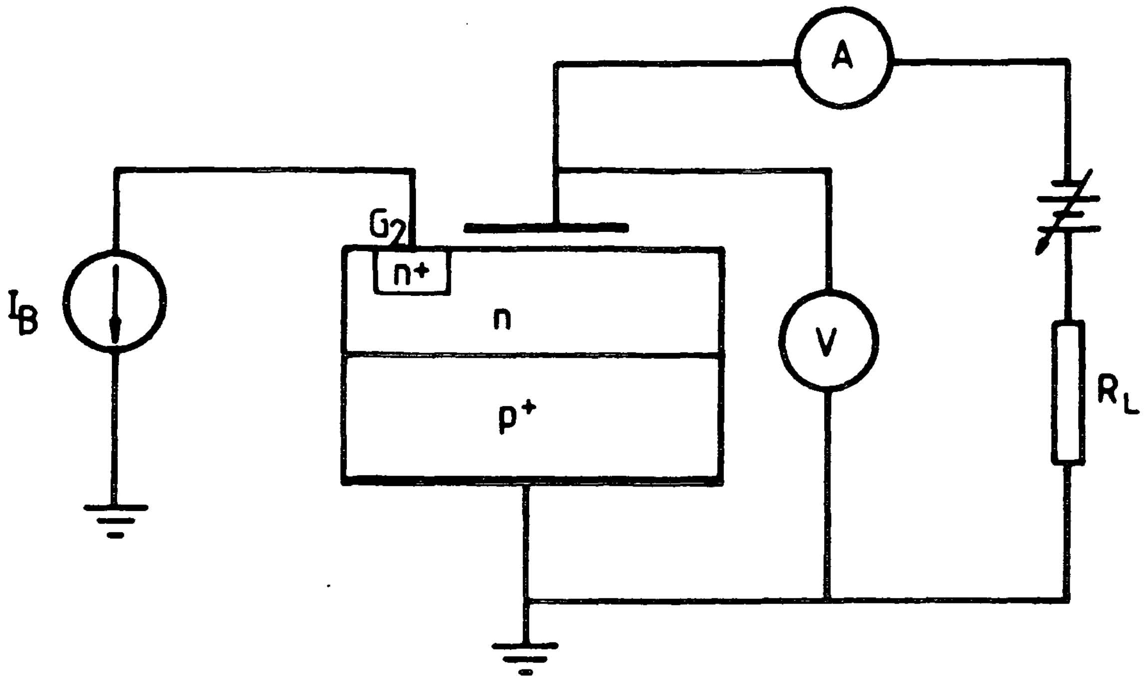


Figure 6.4 a) Top view and b) cross sectional view of the three terminal MISS with the V-groove isolation barrier.



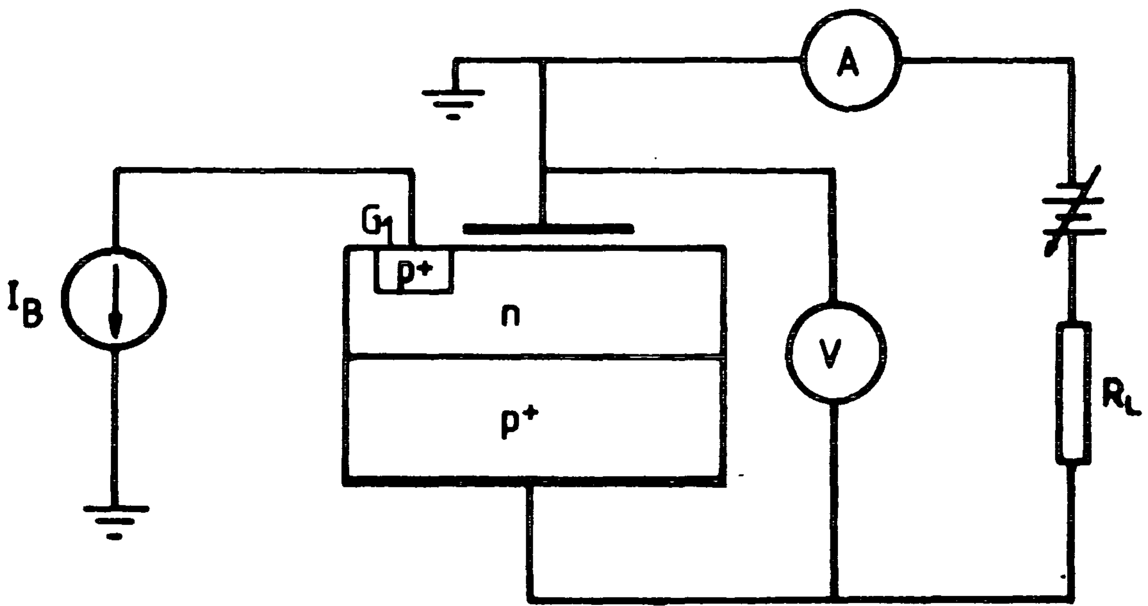


Figure 6.5 Measurement circuit of a) majority carrier injection MIST and b) minority carrier injection MIST.

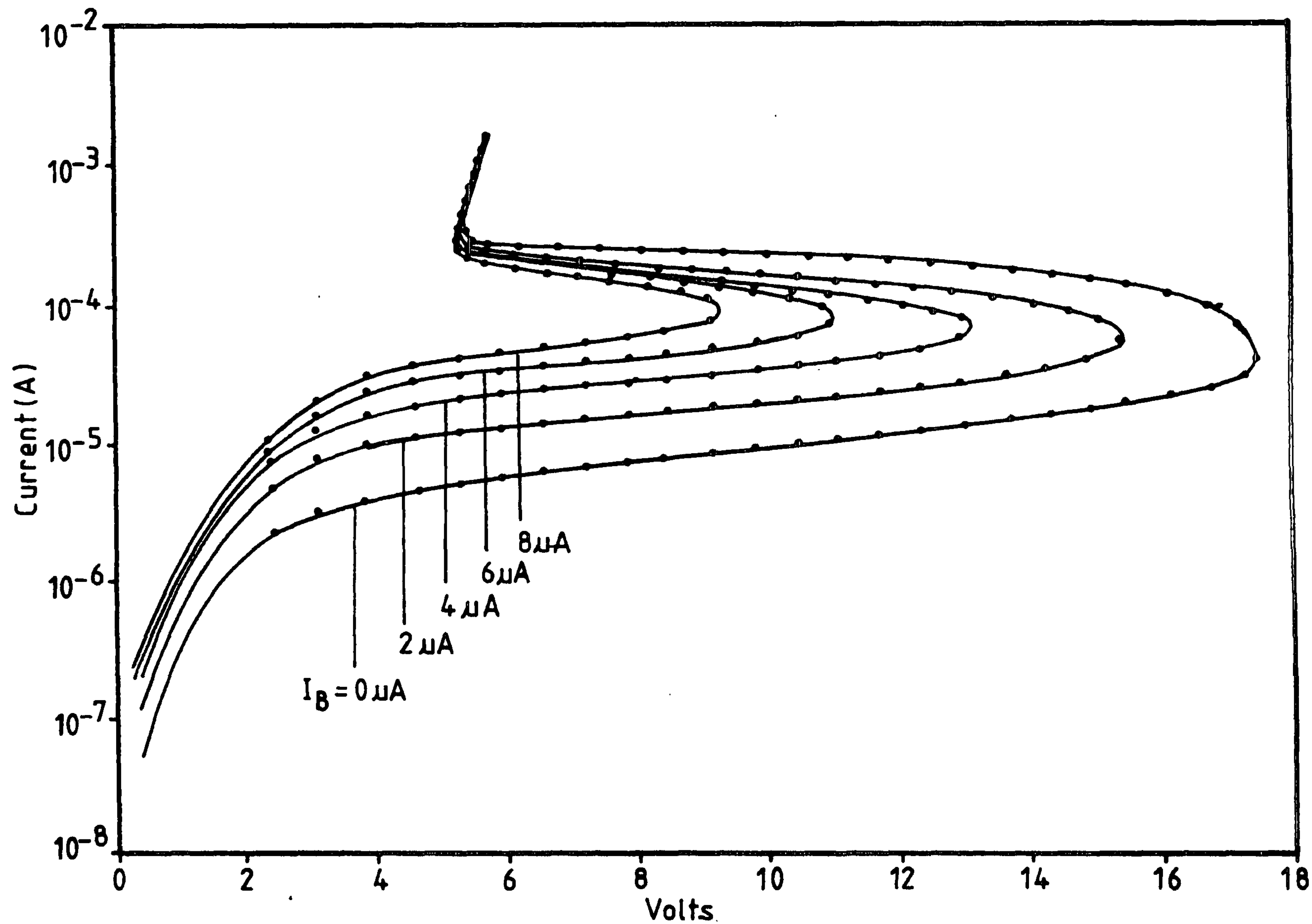


Figure 6.6 Typical I-V characteristic of the MIST (electrode area of $160 \times 160 \mu m$).

age as a function of base current [6]. The relationship between the normalised switching voltage and the base current is plotted in figures 6.7–6.10 for devices with emitter areas of $20 \times 20\mu$m, $40 \times 40\mu$m, $80 \times 80\mu$m, and $160 \times 160\mu$m respectively. The control efficiencies were compared at the point where the variation of the switching voltage with base current is almost linear. The control efficiency is $0.09V/\mu A$, $0.25V/\mu A$, $0.46V/\mu A$ and, $1.5V/\mu A$ for the four devices respectively.

One of the devices with the emitter area of $160 \times 160\mu$m had the n^+ region of the base terminal almost surrounding the emitter electrode as shown in figure 6.10. With this modification the switching becomes more sensitive with the smaller base current compared with the normal base shape, although the control efficiency does not change very significantly. From these plots it is clear that the control efficiency of the MIST depends on the emitter area for a constant p^+-n junction area. The device becomes more sensitive to the base current if the emitter area is increased.

A measurement was made of the control action using the p^+ gate for comparison. In this case the base current was injected through the p^+ terminal (injection of minority carriers) and the control efficiency was relatively small. For the same emitter area of $160 \times 160\mu$m the control efficiency for minority carrier injection MIST is about $0.14V/\mu A$ (figure 6.11) compared to that of the majority carrier injection MIST of $1.5V/\mu A$.

The increase of control efficiency for the larger emitter electrodes is presumably due to the two-dimensional effect as has been discussed in the preceeding chapter. The effect on the switching characteristic of the MIST could be described as follows. For the majority carrier injection MIST the injected electron current from the third terminal increases the forward bias of the collector-base (p^+-n) junction which injects more hole current into the base(n) region. Some of the injected holes recombine with the injected electrons from the third terminal and some of them travel to the interface.

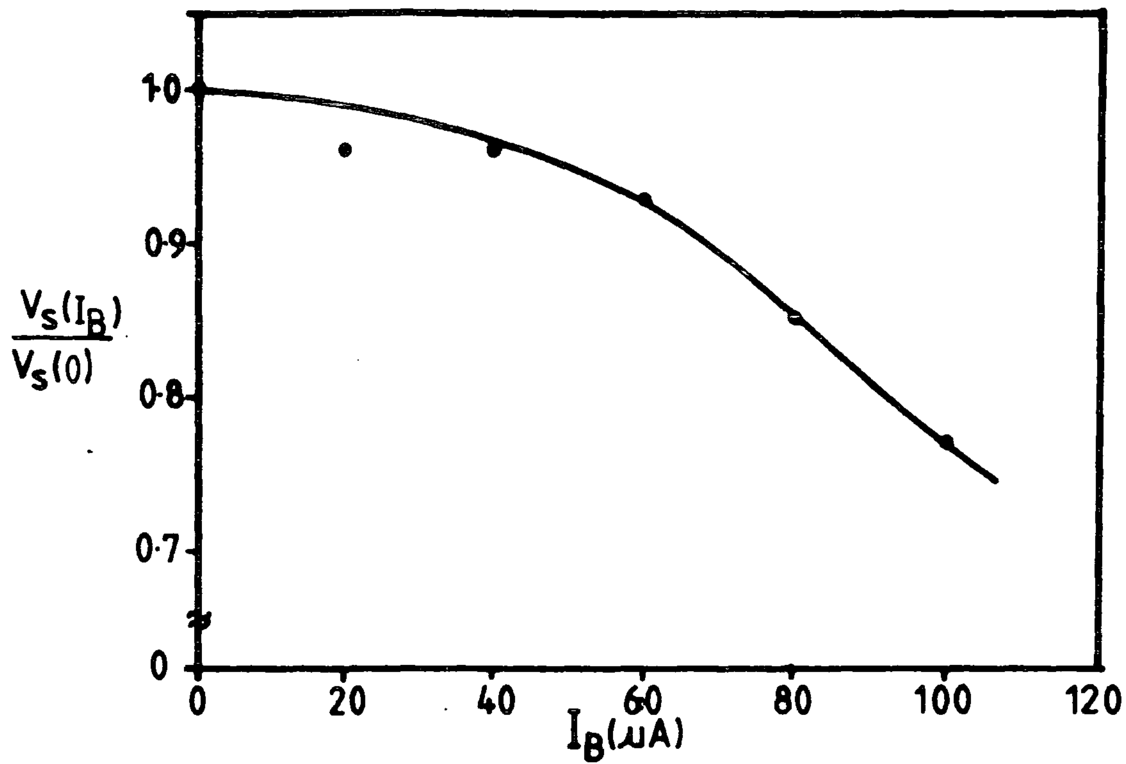


Figure 6.7 Normalised switching voltage versus base current for the majority carrier injection MIST with the electrode area of 20 × 20μm.

Figure 6.8 Normalised switching voltage versus base current for the majority carrier injection MIST with the electrode area of 40 × 40μm.

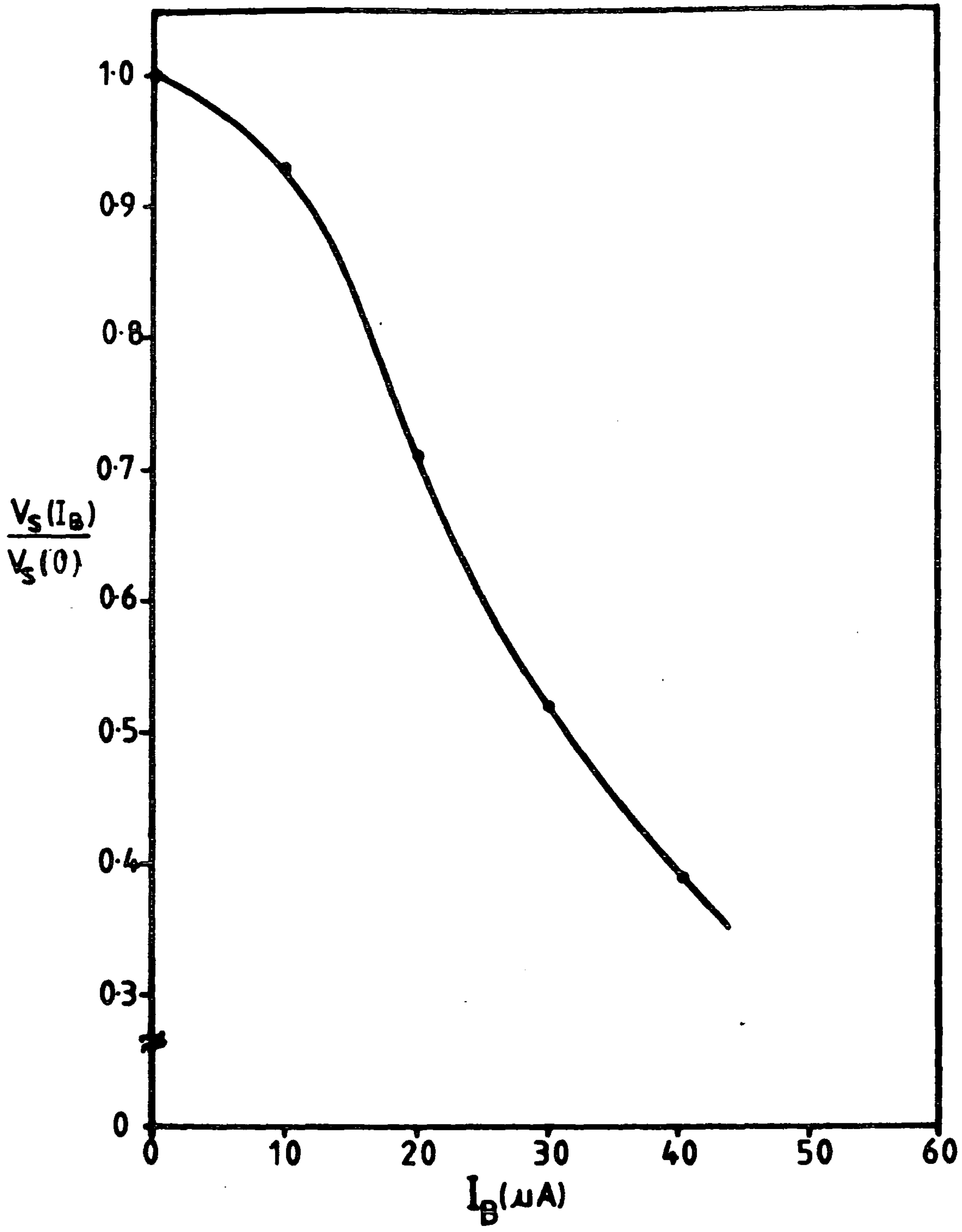


Figure 6.9 Normalised switching voltage versus base current for the majority carrier injection MIST with the electrode area of $80 \times 80\mu m$.

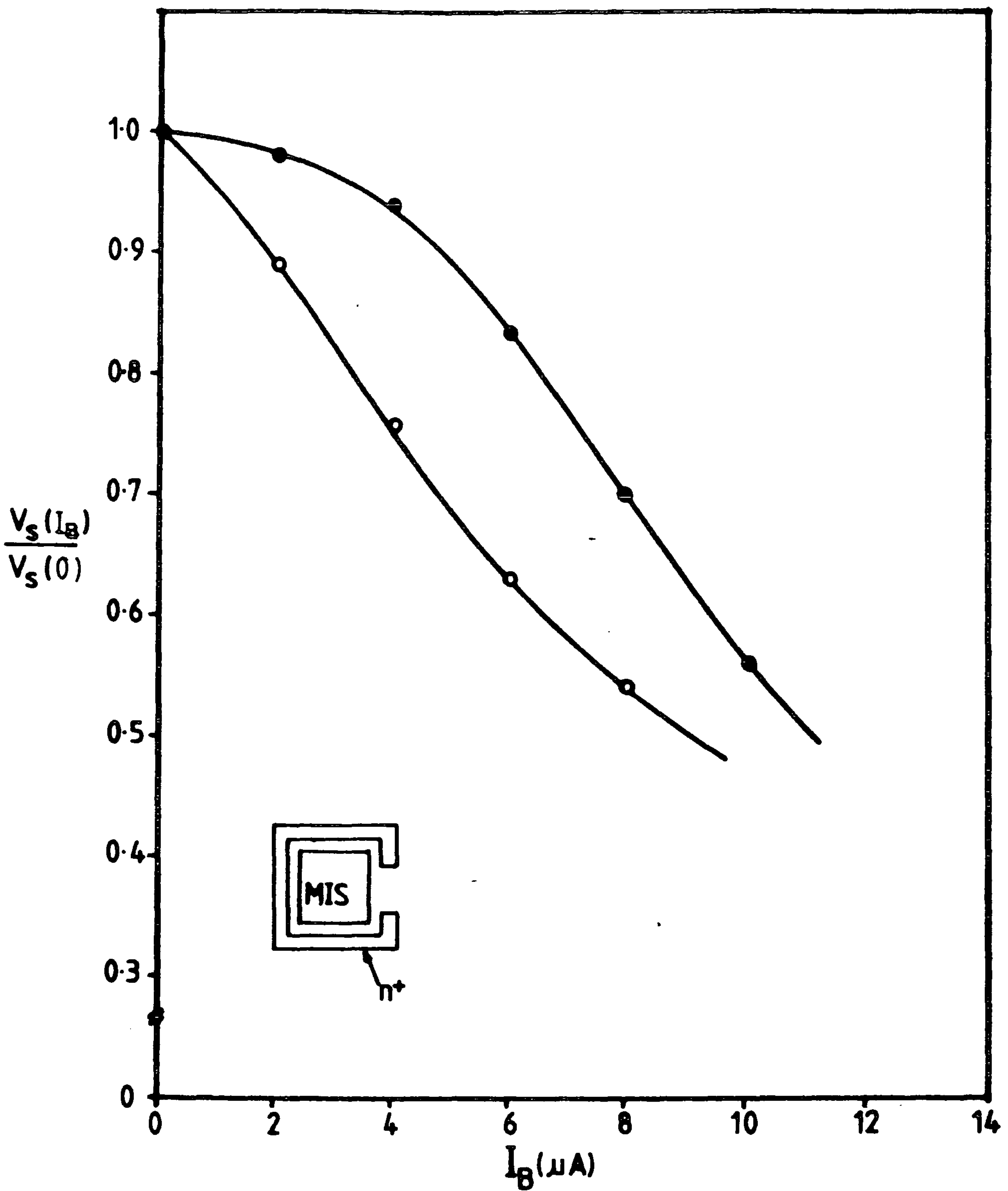


Figure 6.10 Normalised switching voltage versus base current for the majority carrier injection MIST with the electrode area of $160 \times 160\mu m$, (•) normal n^+ base shape (○) n^+ region surrounding the electrode.

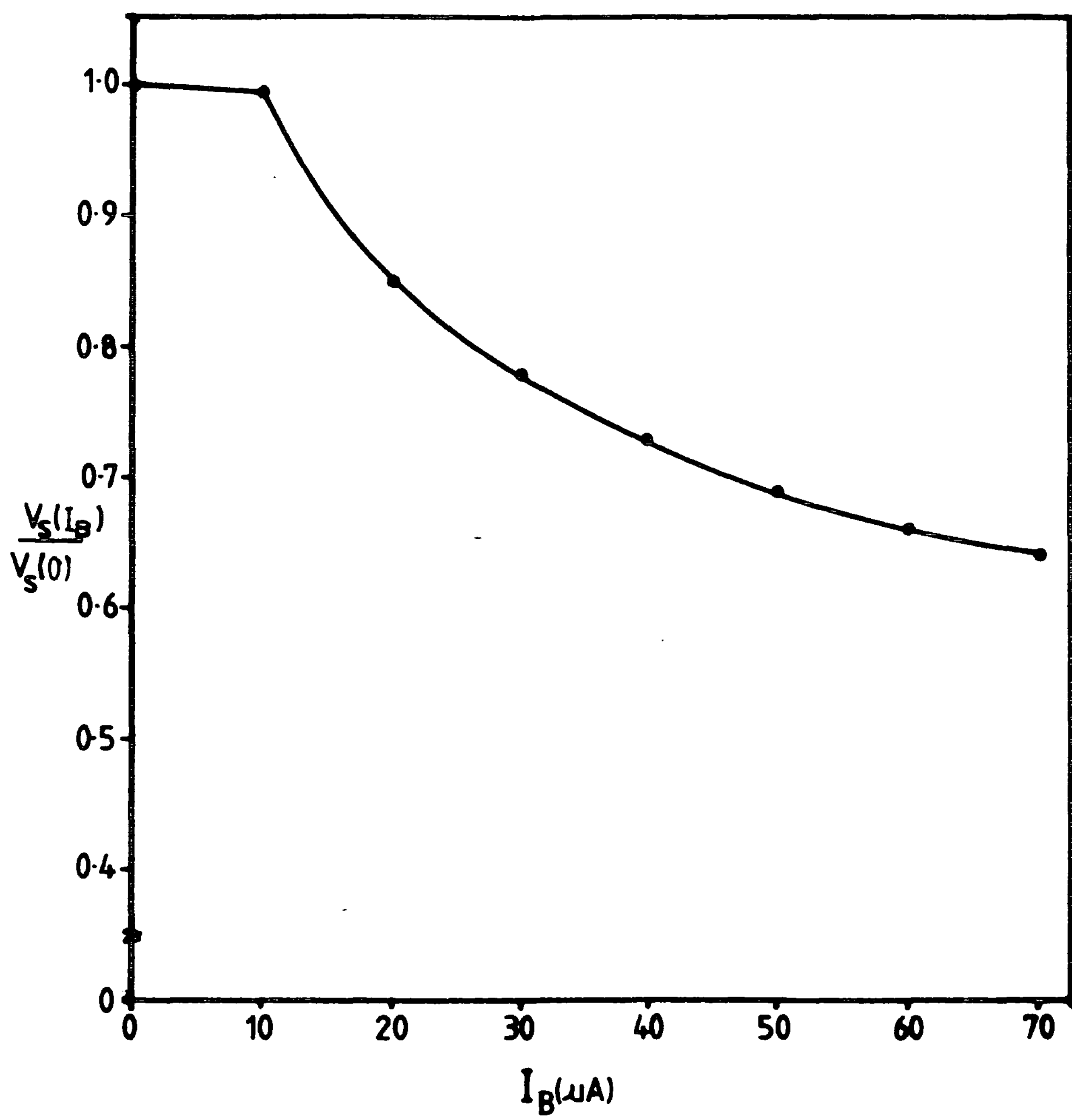


Figure 6.11 Normalised switching voltage versus base current for the minority carrier injection MIST with the electrode area of $160 \times 160\mu m$.

As has been discussed in Chapter 3 the presence of holes at the interface will induce an electron current from the emitter electrode. As the hole concentration at the interface is high enough to make the internal total gain become unity the switching process begins. If the emitter electrode is small the forward biased junction area is much larger than the emitter electrode area and therefore the amount of electron current flowing sideways from the emitter is larger. Therefore a higher electron current is needed to turn the junction fully on and this comes from the the third terminal. If the emitter electrode is surrounded by the n^+ region, the injection of electrons is optimum and hence, the control efficiency is increased.

For the case of the MIST with the p^+ region as the third terminal (minority carrier injection), the injected holes only increase the concentration of holes at the interface but they do not increase the forward bias of the collector- base junction. In addition, since the distance between the p^+ region and the electrode (20μm) is greater than the distance between the collector-base junction and the electrode (2.95μm), the injection of holes from the third terminal has less effect compared to that from the collector-base junction. Therefore the control efficiency of the minority carrier injection MIST is less than that of the majority carrier injection MIST.

6.2.4 Effect of Shunt Resistance

The I-V characteristics of the three terminal MIST change if a shunt resistance is placed between the base terminal and the p^+ substrate as in figure 6.12. In this case there is no external voltage applied to the gate. In the present experiments the shunt resistance was increased from 1kΩ to 1MΩ which caused all the switching parameters to decrease as shown in figure 6.13(a)–6.13(d).

With a high value of R_{sh} very little current will flow in the gate circuit and the

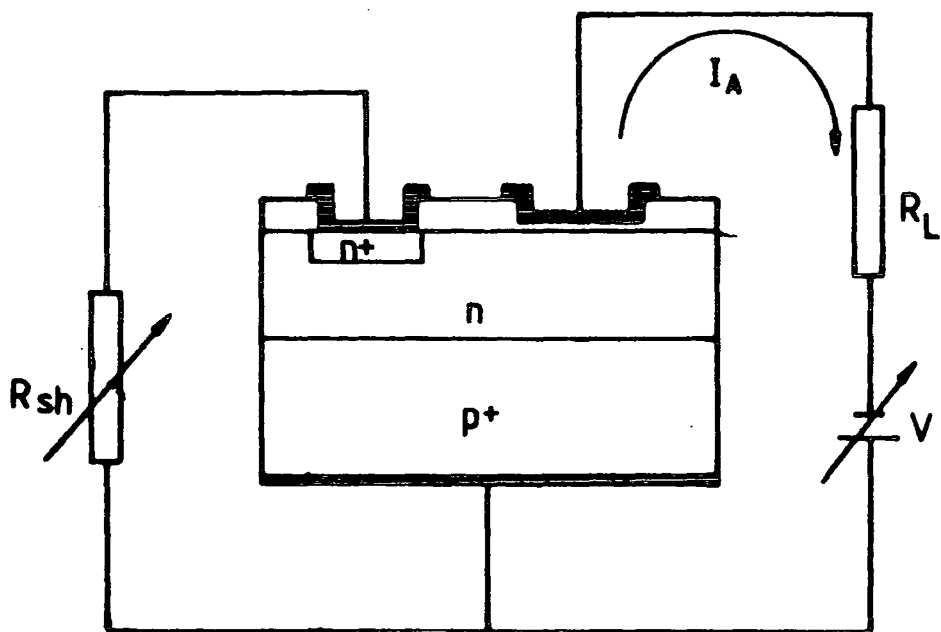


Figure 6.12 MIST circuit with a shunt resistance between base and collector.

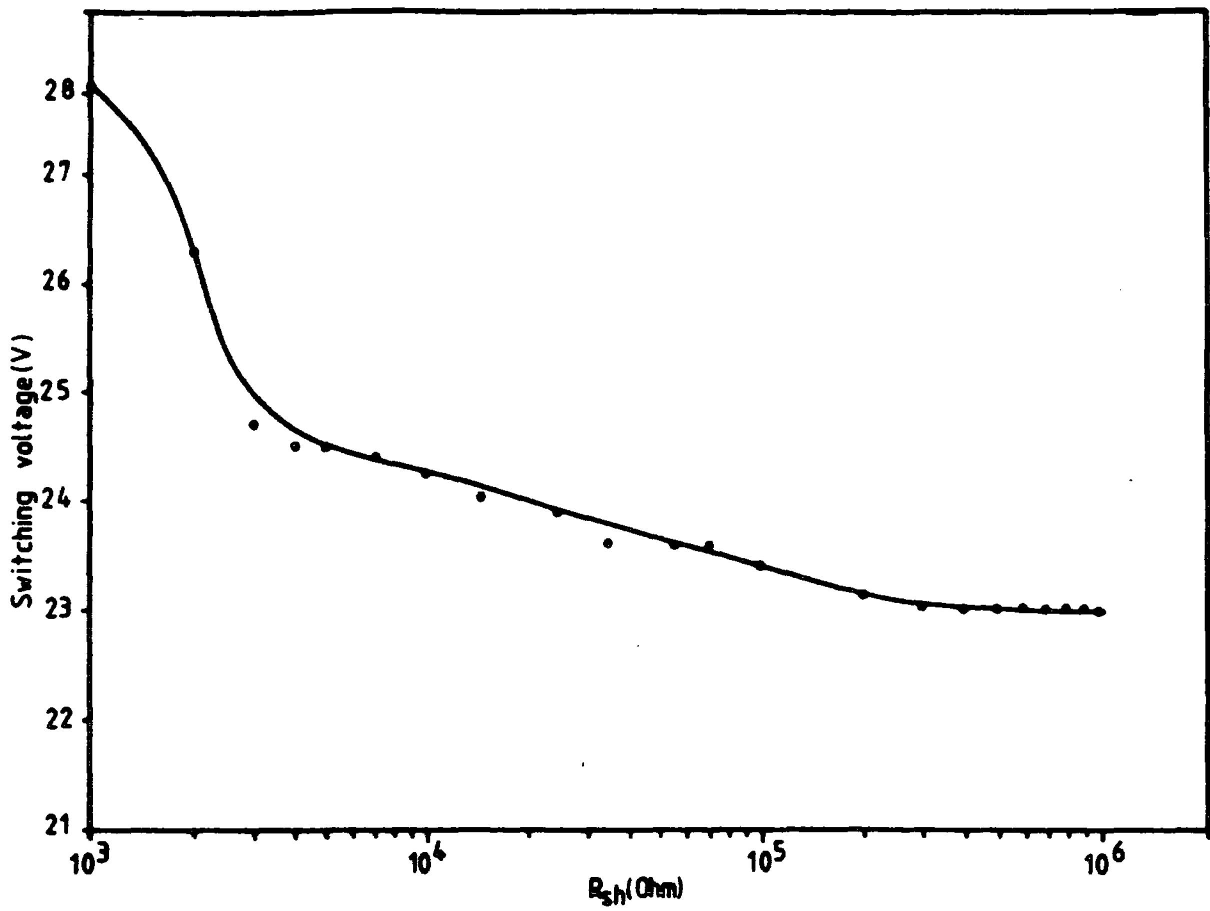


Figure 6.13 a) Switching voltage V_s versus shunt resistance R_{sh}.

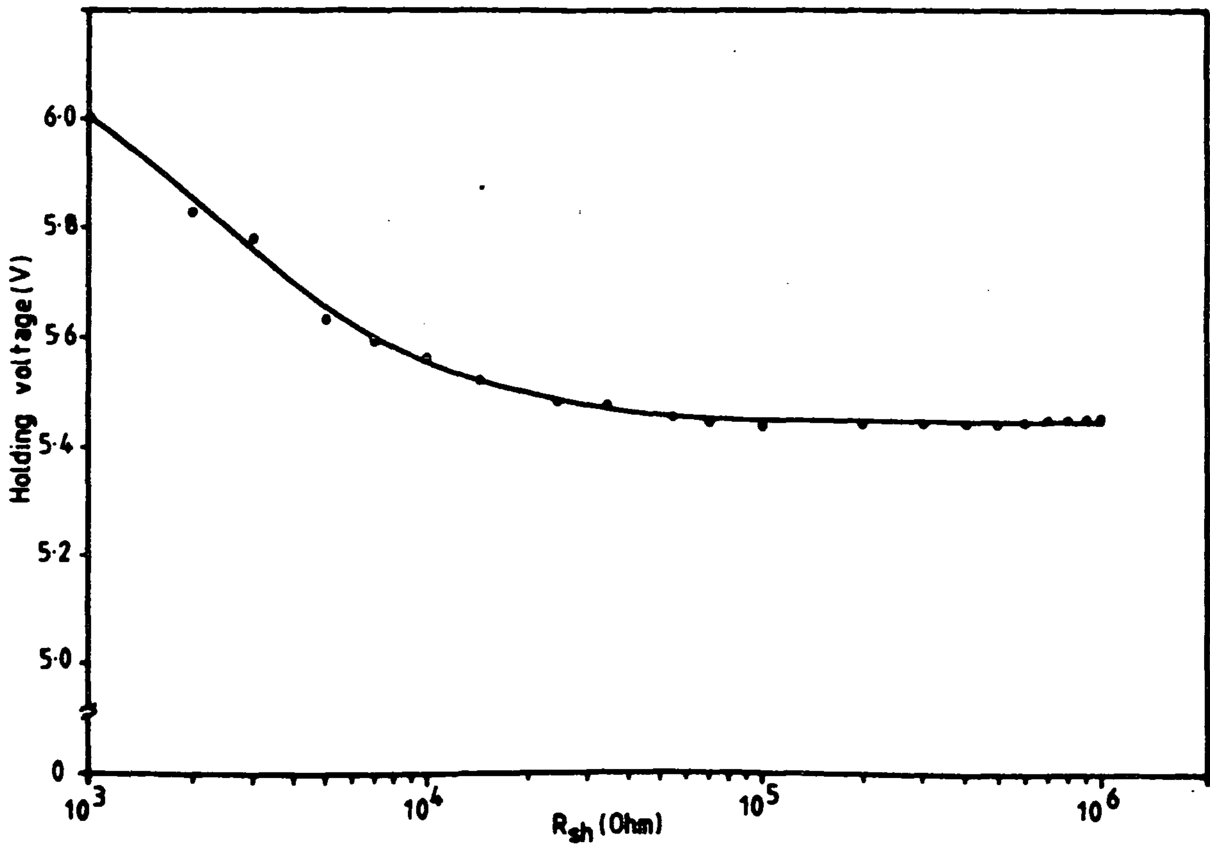


Figure 6.13 b) Holding voltage V_h versus shunt resistance R_{sh}.

Switching current(mA)
2·0
1·2
1·0
0·8
0·6
0·4
0·2
0
10^3
10^4
10^5
10^6
R_{sh}(Ohm)

Figure 6.13 c) Switching current I_s versus shunt resistance R_{sh}.

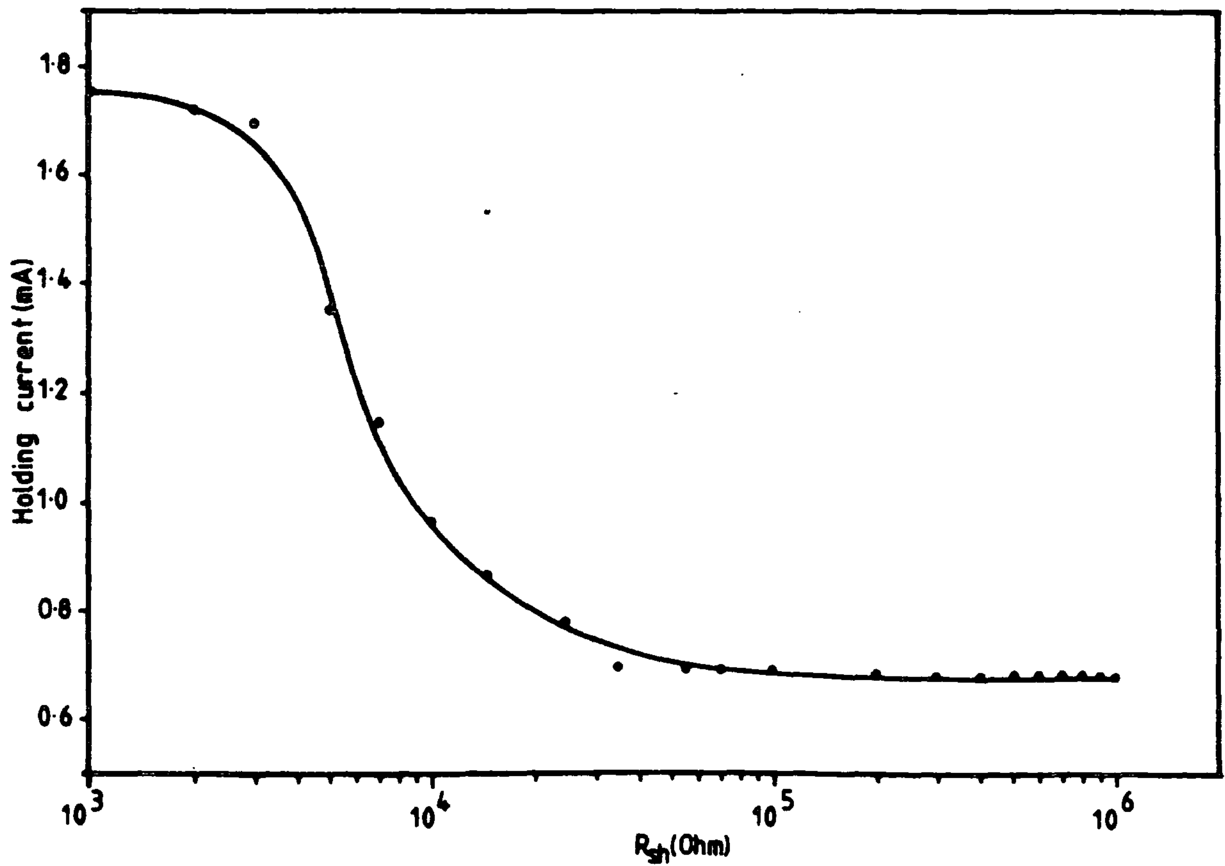


Figure 6.13 d) Holding current I_h versus shunt resistance R_{sh}.

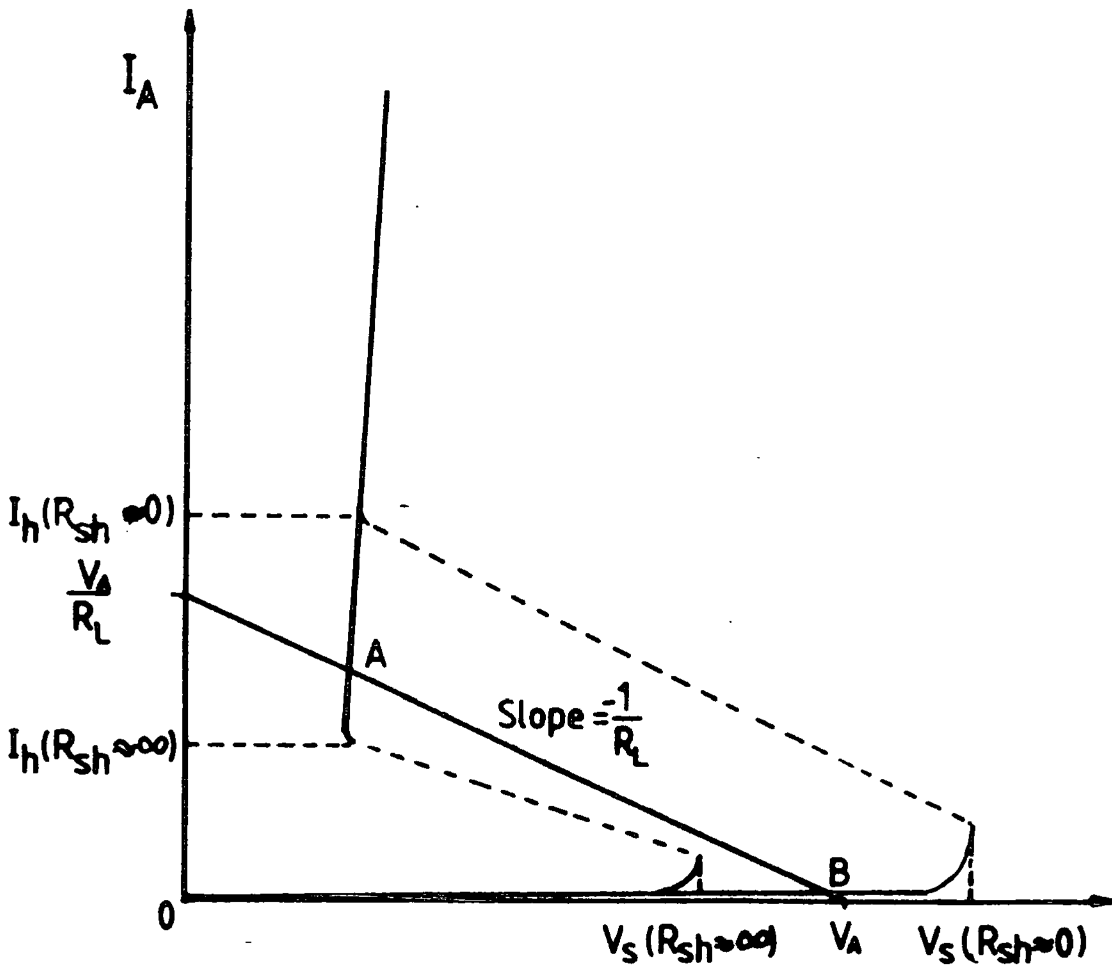


Figure 6.14 I-V characteristic of MIST with load line showing how the device is turned OFF by decreasing the shunt resistance (from ref. 5).

switching parameters will be similar to those of a two terminal MISS. Reducing R_{sh} enables an increasing current to flow out of the gate. This current is carried by the injection of holes from the p^+ substrate and the more current that flows the fewer holes will be available to form the inversion layer. Hence the switching voltage will be increased for low R_{sh} as found. Similar reasoning applies for the holding voltage. The effect of R_{sh} becomes important at a resistance of about 3kΩ which may correspond to a gate current of about 0.15mA at the switching point but in the absence of more detailed measurements this cannot be certain.

A similar behaviour has also been observed by Kroger and Wegener [5] for device structures using tunnel oxide and different epilayer thickness, doping density and isolation. They found a similar fall of V_s with R_{sh} but a very different sensitivity which is not surprising. Since the holding current increases if R_{sh} is reduced they suggested a practical application in which the device can be switched from the low to the high impedance state by changing R_{sh} only. The transition from the low to the high impedances state is described graphically in figure 6.14. The device is biased in the low impedance state with the operating point A when R_{sh} is high. As the shunt resistance is decreased the effective holding current becomes greater than the biasing current and the device switches to the high impedance state, operating point B. This has been confirmed experimentally.

6.3 MIS-EMITTER TRANSISTOR

6.3.1 Introduction

In Chapter 2 we have shown that the MIS tunnel diode will become electronically equivalent to a conventional p-n junction diode when a suitable semi-insulator film

is used. Therefore the M-I-n-p^+ structure is equivalent to a p-n-p transistor and the M-I-p-n^+ is equivalent to the n-p-n transistor where the MIS section acts as an emitter, the n(p)-region acts as a base, and the $p^+(n^+)$ substrate as a collector for the two device types respectively. This type of transistor is also known as a TETRAN for Tunnel-Emitter Transistor [1], although researchers have called it an MIS Heterojunction Emitter Transistor[3,4].

Since all reported MIS-emitter transistors [1,3,4] have used tunnel oxide as the semi-insulator some preliminary experimental work was carried out to see the perfomance of this type of transistor with SRO as a semi-insulating material. This also showed that, apart from switching and negative resistance characteristics, the MISS structure can also be used as a transistor if the device is carefully designed. All the measurements carried-out in the present work were based on devices in the wafer no. 1 which was fabricated at Southampton University.

6.3.2 Operation of MIS-Emitter Transistor

The structure of the MIS-emitter transistor is shown in figure 6.4 with the n^+ region as the base terminal. The p^+ gate G_1 is not used in this application. The biasing condition is similar to that of the bipolar transistor where the emitter-base junction is forward biased and the collector-base junction is reverse biased. These polarities are the opposite of those for the MIST. Figure 6.15 shows the energy band diagram of the MIS-emitter transistor under various biasing conditions. Since the MIS section is in forward bias, the electrons tend to accumulate at the semiconductor-semi-insulator interface. On the other hand, the p-n junction is reverse biased. Therefore, at zero base current, the only collector current is the generation current in the base-collector junction depletion region which is very small. As a consequence, most of the applied voltage drops across the p-n junction, and the voltage across the MIS section

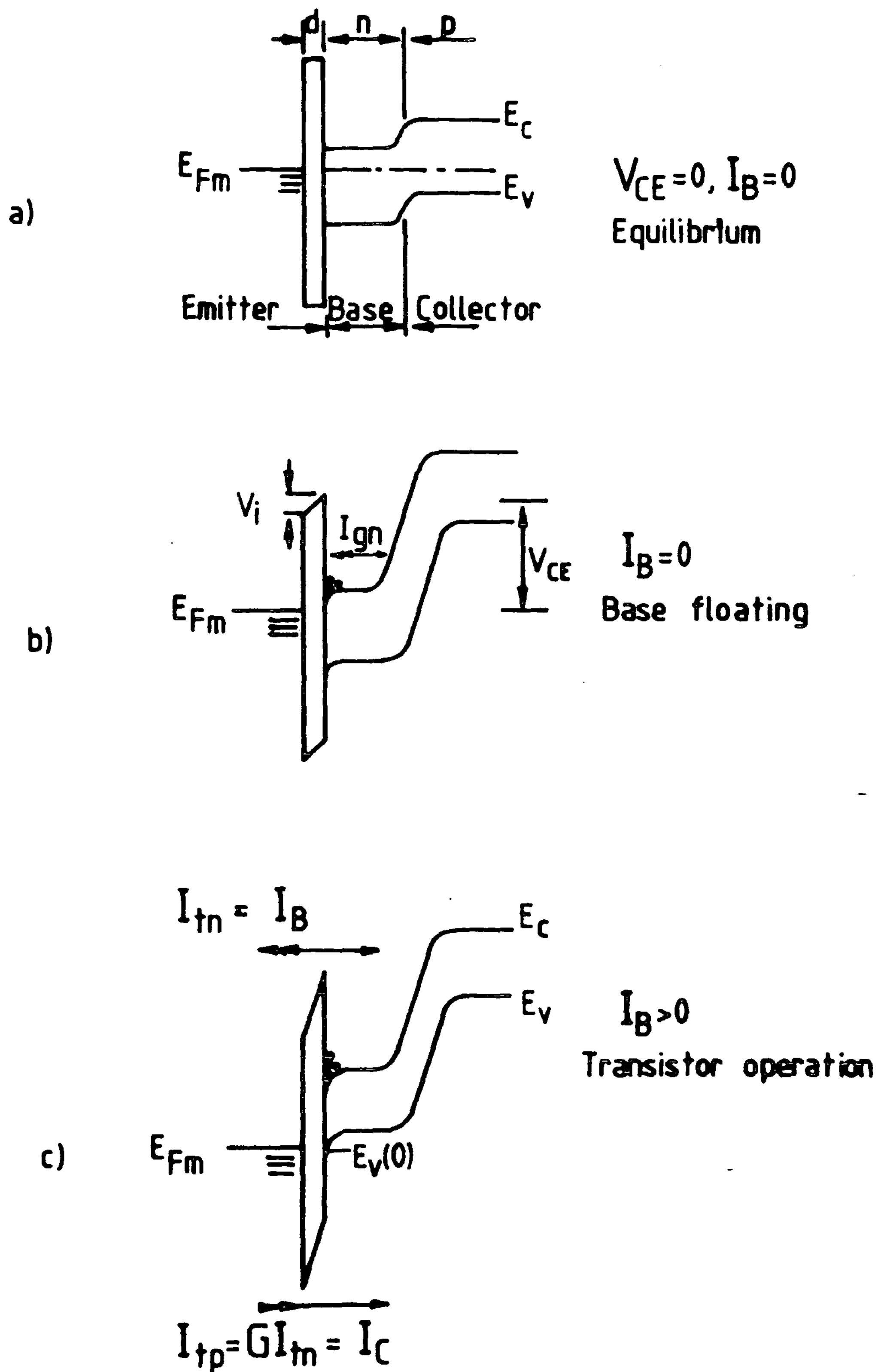


Figure 6.15 The energy band diagrams of the MIS-emitter transistor, **a)** in equilibrium, **b)** emitter-collector is biased with zero base current and **c)** emitter-collector is biased with base current greater than zero.

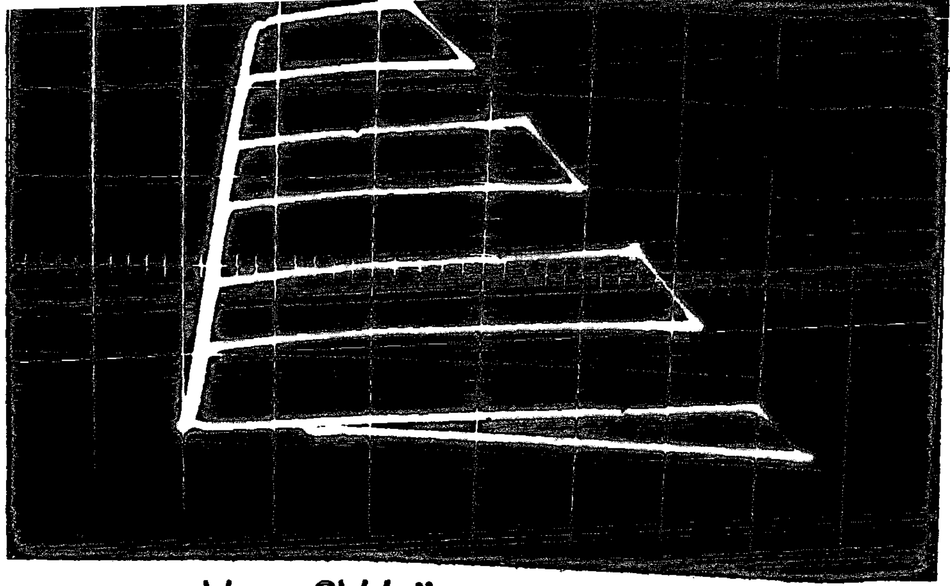
is very small allowing only a very small current to flow through the semi-insulating layer.

When the base current, I_B, is applied, it will only flow to the emitter electrode through the forward biased MIS structure because the reverse biased base-collector junction prevents the base current flow to the collector and thus $I_B = I_{tn}$ (figure 6.15(c)). For a sufficiently large base current a large number of electrons will accumulate at the interface and the voltage drop in the MIS structure increases. As a result the semiconductor valence band edge could be above the metal Fermi level ($E_{v(0)} > E_{Fm}$) and the hole tunnel current, I_{tp}, from the metal to the semiconductor becomes very high. This hole current diffuses to the edge of the p^+-n junction depletion region and drifts to the collector through the depletion region so that $I_C = I_{tp}$. Therefore, the d.c large signal gain of the MIS-emitter transistor, $G = I_C/I_B$, is the ratio of I_{tp} to I_{tn}, which has been shown to be very dependent on the electrical characteristics of the MIS [1,2].

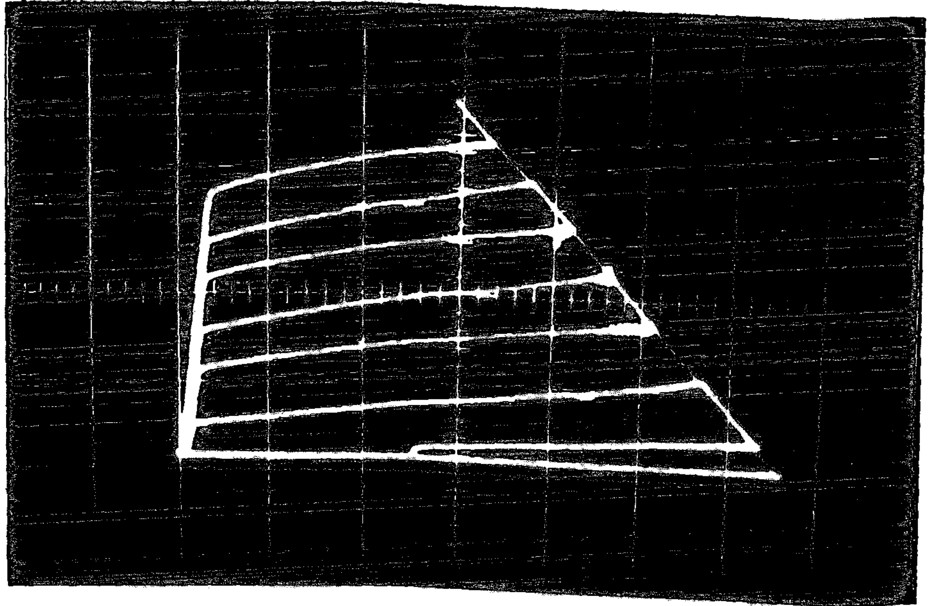
6.3.3 Transistor Characteristics

Figure 6.16 shows the characteristics of the transistor of different emitter area, as measured in the present work using a curve tracer. The devices used were isolated by V-grooves which also defines the p-n junction area for the present device at $240 \times 240\mu m$ while the base width, equal to the epitaxial layer thickness, was $2.95\mu m$. Various emitter areas were used, $4 \times 4\mu m$, $10 \times 10\mu m$, $20 \times 20\mu m$, $40 \times 40\mu m$, $60 \times 60\mu m$ and $80 \times 80\mu m$.

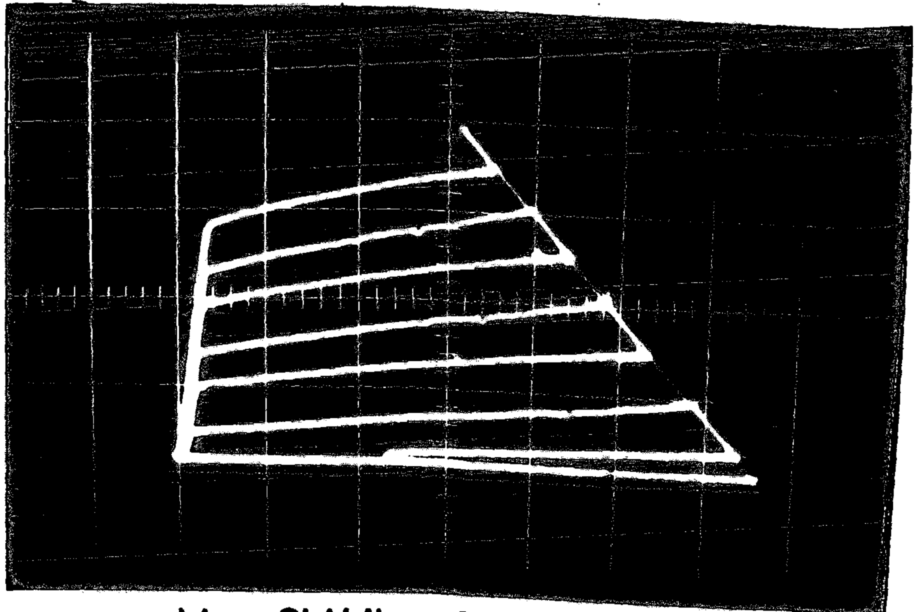
As we can see, the average gain of the transistor was small and it seems to be dependent on the emitter area. The current gain of the transistor with emitter areas of greater than $10 \times 10\mu m$ was about 3, and less than unity for emitter areas of smaller



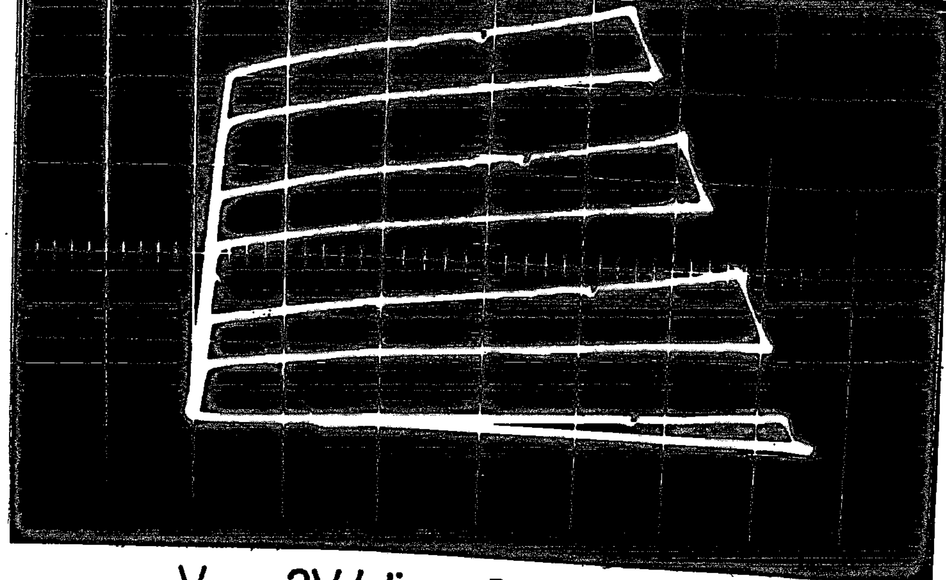
(a) Emitter size = 80x80 µm



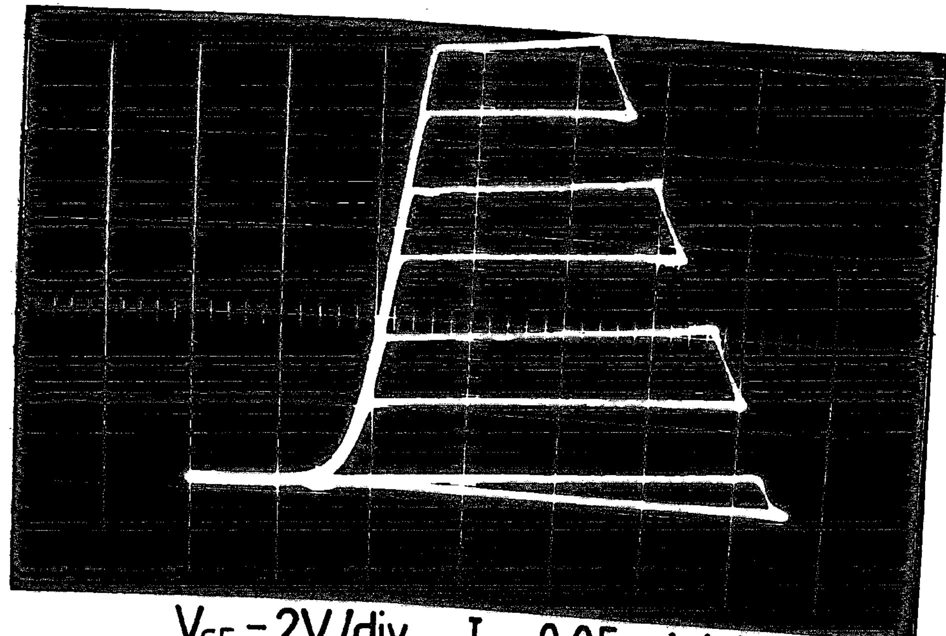
(b) Emitter size = 60x60 µm



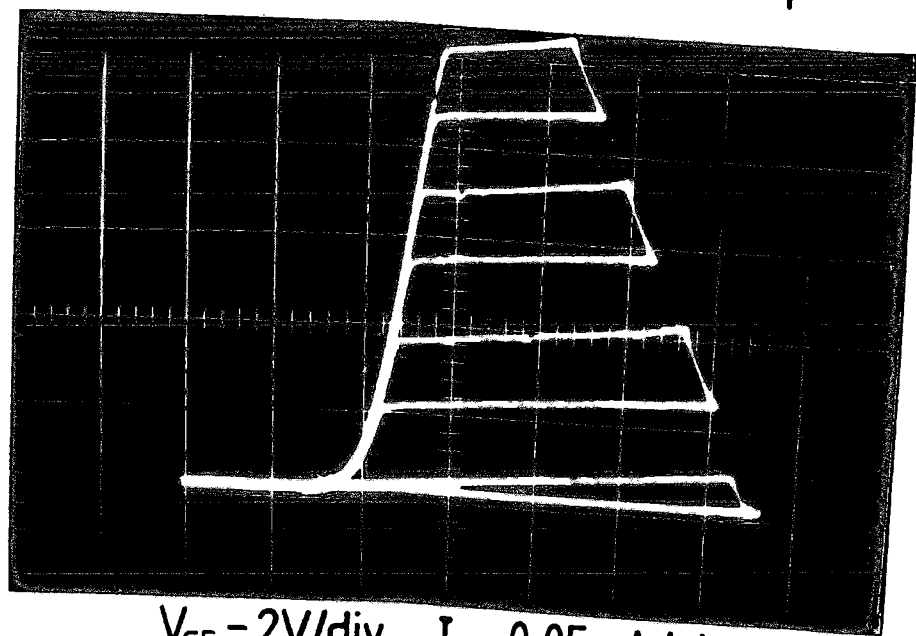
(c) Emitter size = 40x40µm



(d) Emitter size = 20x 20 µm



(e) Emitter size = 10x10 µm



(f) Emitter size = 4x4 µm

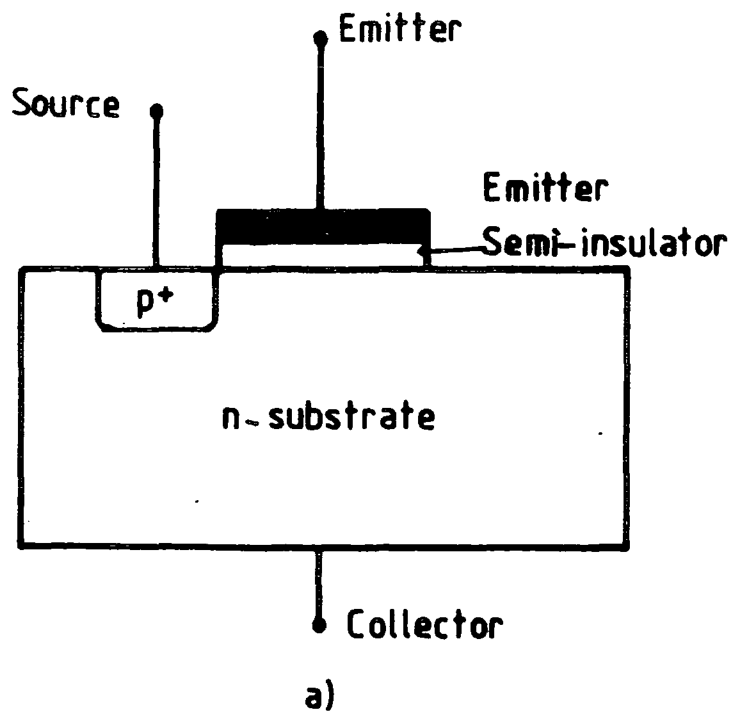
Figure 6.16 Characteristics of MIS-emitter transistor with a constant p-n junction area of $240 \times 240 \mu m$ and different emitter area of **a**) $80 \times 80 \mu m$, **b**) $60 \times 60 \mu m$, **c**) $40 \times 40 \mu m$, **d**) $20 \times 20 \mu m$, **e**) $10 \times 10 \mu m$, **f**) $4 \times 4 \mu m$. (row six of figure 5.14)

than $10 \times 10\mu$m. In addition to that, the active region of the transistor started at a relatively higher voltage as the emitter area decreased. This behaviour is probably related to the two- dimensional effects which become dominant as the emitter area decreases to the order of the base thickness. A similar effect has also been found to occur theoretically in the one dimensional MIS structure for a higher current density [18,19].

The gain of these transistors was found to be high. However, we have to bear in mind that the present devices were not purposely designed to be transistors. The performance of a transistor can be improved by increasing the injection efficiency of the emitter which can be quantified using the emitter Gummel number, G_e [13]. * It has been reported that a tunnel-oxide MIS-emitter transistor can give a very high gain of between 10,000 and 30,000 with a breakdown voltage of 25V to 33V [3,4]. The emitter Gummel number of this transistor was 3×10^{14}s.cm^{-4} which is greater than that of the conventional diffused transistor with G_e of below 5×10^{13}s.cm^{-4}. One of the criteria used to improve the transistor gain is that the base region must have a very high resistivity ie. low doping concentration (base Gummel number of the order of 10^{12}s.cm^{-4}) [3]. However, the present device has a doping concentration of the order of 10^{15}cm^{-3} which is too high for a high gain MIS-emitter transistor. This is one of the reasons why the gain is so small.

A new form of MIS-emitter transistor was proposed by Simmons and Taylor [1] in which the junction is self aligned to the tunnel emitter as shown in figure 6.17. This structure is very similar to the Bipolar Inversion-Channel Field- Effect Transistor (BICFET) [14 - 16], the only difference being the thickness of the semi-insulator. The

* The Gummel number is a parameter related to the number of impurities per unit area of the emitter junction. It is normally defined either by $\frac{qD_n n_i^2}{J_s}$ in cm^{-2} or by $\frac{qn_i^2}{J_s}$ in s.cm^{-4} where q is the electronic charge, D_n is the diffusion constant of an electron, n_i is the intrinsic concentration and J_s is the saturation density. A higher impurity concentration gives a higher current gain. However for the bipolar transistor if the doping of the emitter is beyond $10^{19} - 10^{20}$cm^{-3} the effect of band gap narrowing reduces the gain.



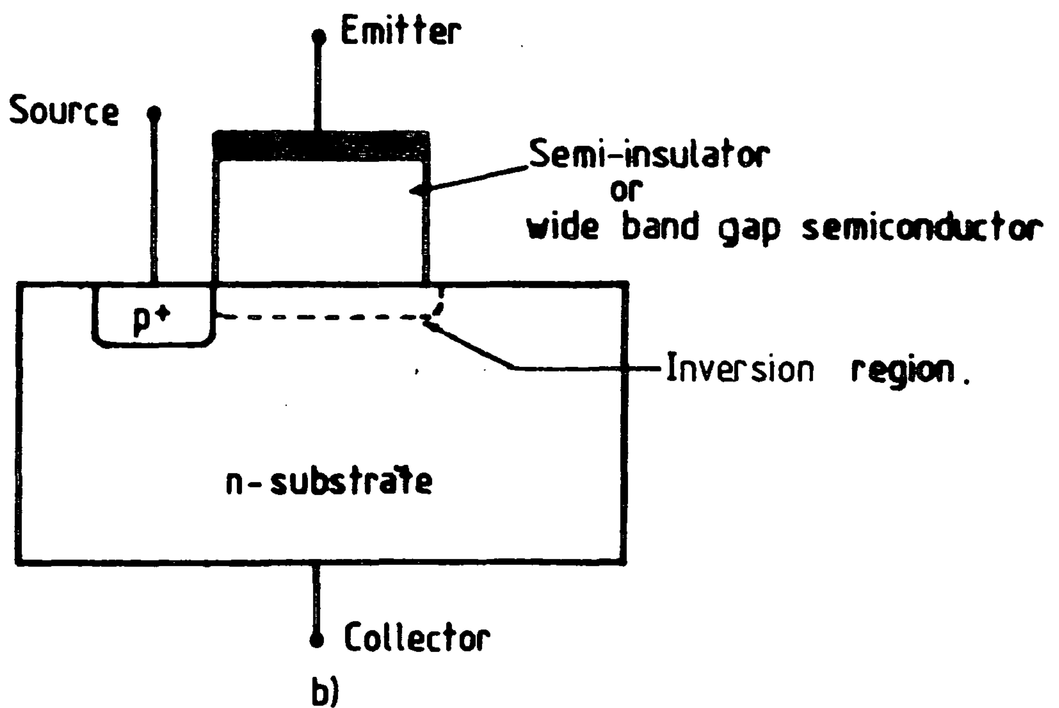


Figure 6.17 Schematic diagram of a) Tunnel Emitter Transistor (TETRAN) and b) Bipolar Inversion-Channel Field-Effect Transistor (BICFET) (from ref. 17).

BICFET has a thicker insulator layer ($\approx 300\AA$ for oxide) compared to the MIS-emitter transistor. The frequency performance of these transistor is governed by the input capacitance which is also determined by the thickness of the insulator. A thicker insulator (for the case of BICFET) has a smaller capacitance and therefore a higher operating frequency. The MIS-emitter transistor has been shown to be inferior to the BICFET. A small-signal analysis done by Chu and Pulfrey [17] has shown that the maximum operating frequency for the MIS-emitter transistor is about 1GHz while the BICFET has a maximum frequency of 10,000 GHz [15,16].

This brief study has demonstrated that SRO can be used as an alternative material for the MIS-tunnel emitter transistor. However, due to a very limited range of samples, it is difficult to say whether the use of SRO can improve the transistor performance.

6.4 N-TYPE NEGATIVE RESISTANCE TRANSISTOR

6.4.1 Observation

An interesting phenomenon has been observed for the first time during the characterisation of the MIS-emitter transistor. The current-voltage measurements were performed on a device from wafer no.8 which was intended to have an epitaxial layer thickness of 3.5μm, but due to the high temperature processing the neutral thickness shrank to 0.17μm as measured on the final wafer using a grooving and staining technique at Durham. The thickness and refractive index of the SRO layer were estimated by means of the ellipsometer before metallisation to be about $179\AA$ and 1.9 respectively. Figure 6.18 shows a schematic diagram of the measurement circuit. The base current was stepped from zero to $25\mu A$ in increments of $5\mu A$ using

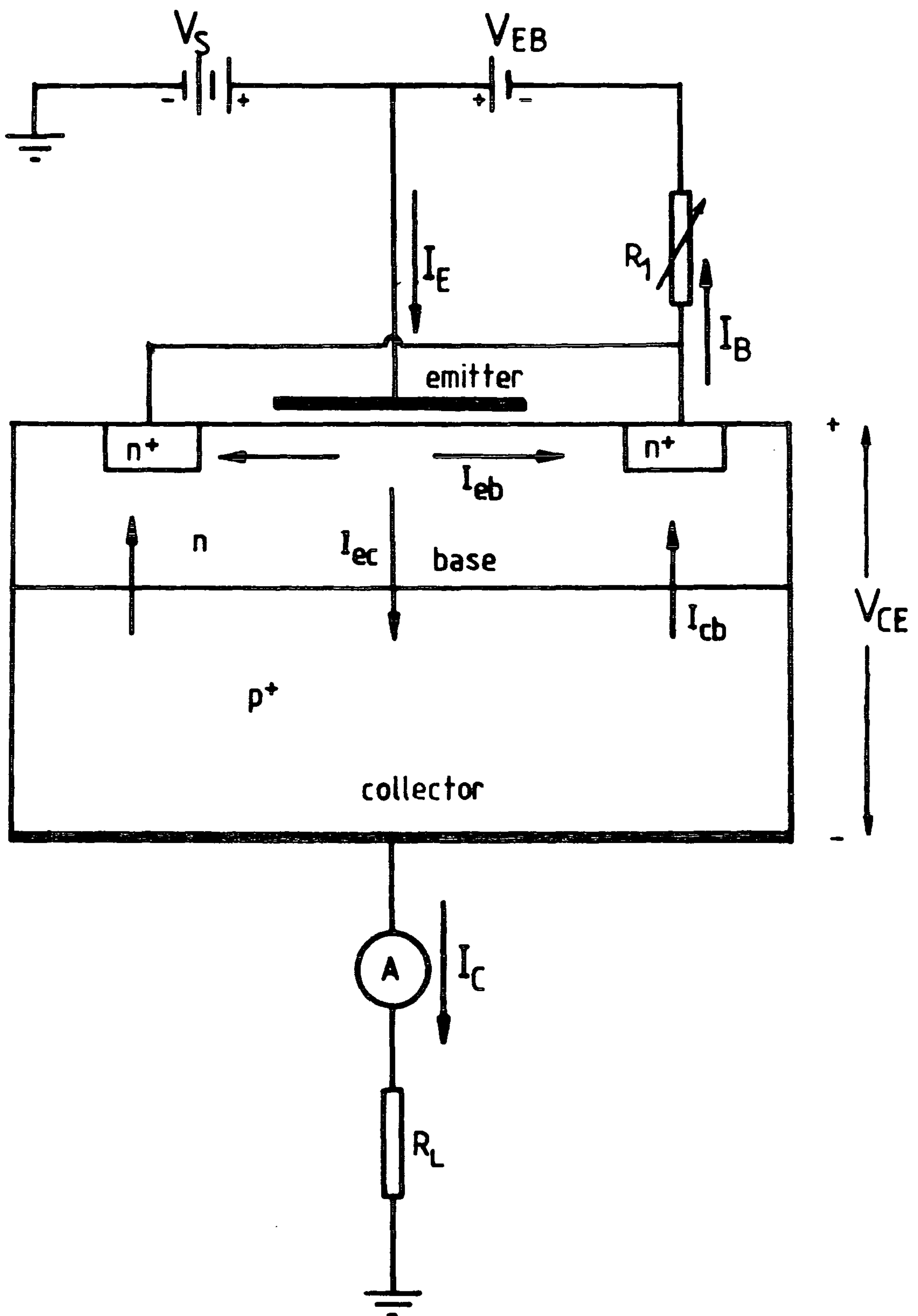


Figure 6.18 Circuit arrangement used to measure the MIS-emitter transistor characteristics

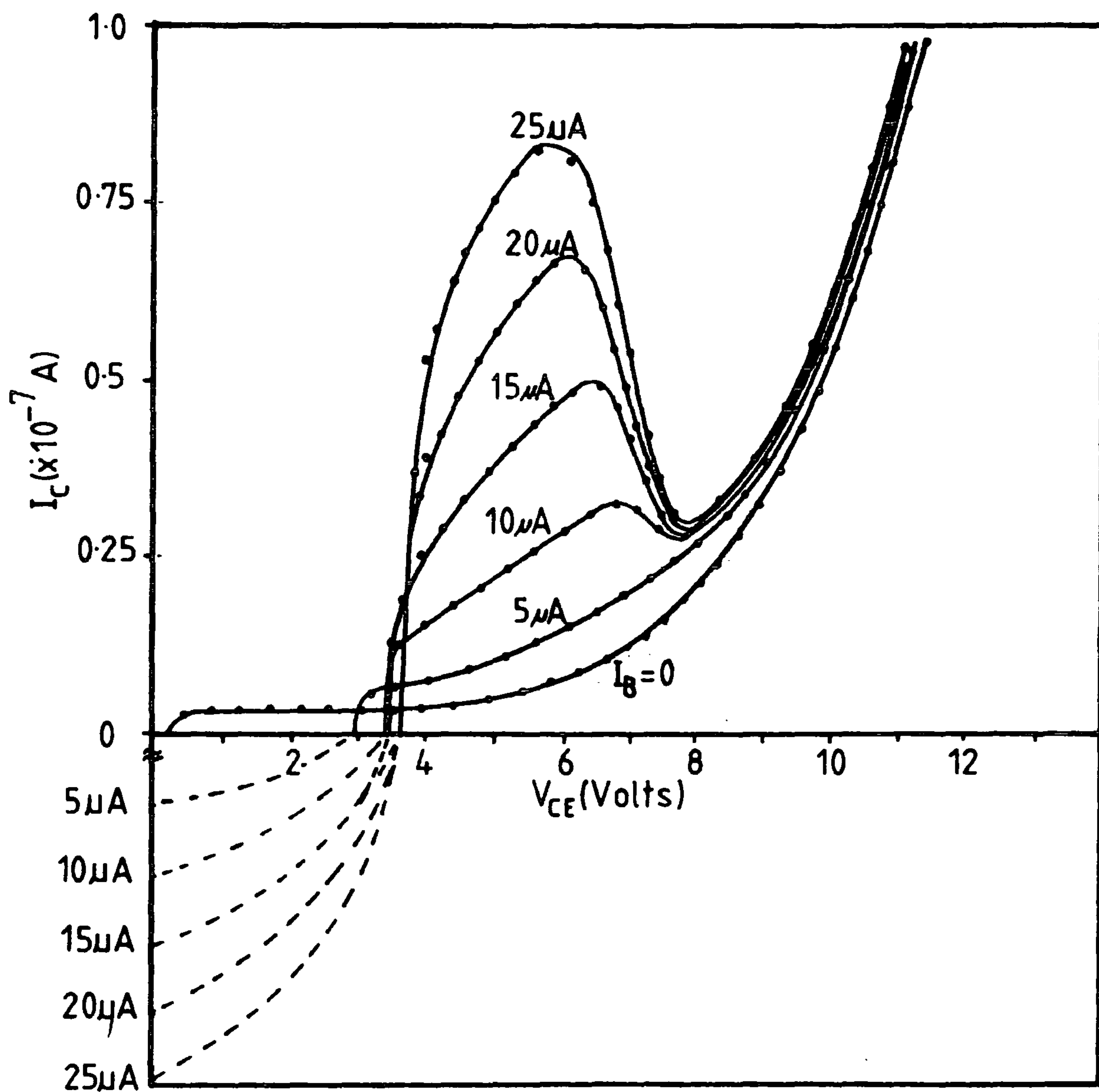


Figure 6.19 Characteristic of MIS-emitter transistor contain an N-type negative resistance. (Emitter area=$100\times100\mu$m).

a voltage supply and variable resistance R_s as shown or a Keithley Programmable Current Source 220. The polarities applied in this circuit are the same as used for the investigation of other MIS transistors as described in the previous section.

This particular MIS-emitter transistor was found to exhibit an N-type negative resistance in its $I_C - V_{CE}$ characteristic for base currents greater than $5\mu A$ and at the higher values of V_{CE} as shown in figure 6.19. The appearance of the negative resistance was confirmed by repeating the measurement several times and on different chips of the same wafer. An a.c. measurement was performed using a curve tracer where similar characteristics were also observed. The negative resistance region was perfectly stable in this measurement circuit. An oscilloscope showed no trace of circuit oscillation in the negative resistance region. These facts prove convincingly that the N-type negative resistance behaviour was related to the device structure and that it is not due to measurement errors.

6.4.2 Discussion

At zero base current, $I_B = 0$, increasing the applied voltage ~~voltage~~ across the device, V_{CE}, causes the p$^+$-n junction depletion layer width to increase. The current through the device, which is also called a collector current, I_C, is dominated by the generation current from the reverse biased base-collector junction. An increase in V_{CE} above a certain value will cause the depletion layer to extend to the interface and a punch-through mechanism occurs. Since the n-epitaxial layer thickness is very small this will happen at a relatively low voltage. As a result, the emitter current can flow directly to the collector and $I_C \approx I_E$, so that the current increases very rapidly as the applied voltage is increased further. This is clearly shown in figure 6.19 for $I_B = 0$.

Now let us consider the case when $I_B > 0$ with the base biased at a negative potential. Since the applied voltage V_s is increased positively with respect to the collector, as V_{CE} increases from zero the potential at the collector, V_C, is initially less negative than the potential at the base, V_{EB}. Therefore the collector-base junction is in forward bias so that the majority of the current flow through the device is from the collector to the base ($I_C \approx I_B$). Since the base current flows in the opposite direction from the collector current this gives rise to a negative value in the measured collector current.

When $V_C > V_B$, the base-collector junction is reverse biased and therefore the majority of the current flow to the collector terminal is the reverse saturation current of the p-n junction. Most of the emitter current flows to the base terminal since the MIS section is in forward bias. As the voltage between the collector and the emitter, V_{CE}, is increased further the channel width (the neutral region underneath the emitter electrode) decreases. This reduces the conductance between the base and the emitter so that the current flow from the emitter to the base (I_{eb}) is reduced as found experimentally, figure 6.19.

The terminal current equation can be written as,

$$I_C = I_E - I_B \qquad 6.1$$

where

$$I_E = I_{ec} + I_{eb} \qquad 6.2$$

and

$$I_B = I_{eb} + I_{cb} \qquad 6.3$$

I_{ec} and I_{eb} are the fractions of the emitter current that flow to the collector and the base respectively and I_{cb} is the fraction of the p-n junction current that flows to the base terminal as shown in figure 6.18.

The negative resistance device characteristics interact with the circuit if the voltage limit of the base current source is changed and this gives even more unusual characteristics. Figures 6.20(a) - 6.20(c) show the I-V characteristics of the same type of device with the voltage limit of the current source fixed at 5.0V, 6.0V, and 7.0V respectively. These characteristics demonstrate that there are now two N-type negative resistances present. The first, lower voltage, negative resistance is the same for all values of the voltage limit but the second one seems to be dependent on the voltage limit of the constant current source. This behaviour can be explained as follows.

As V_{CE} increases the depletion layer in the n-region extends toward the surface and reduces the channel conductance between the emitter and the base. This phenomenon is analogous to the channel shortening effect in a JFET. Hence the current flow between the emitter and the base, I_{eb}, decreases but, in order to keep I_B constant (supplied from a constant current source), the forward bias current, I_{cb}, of the p-n junction increases. Thus the collector current which is given by, $I_C = I_{ec} - I_{cb}$, decreases as V_{CE} increases, and this gives rise to a negative resistance characteristics in the $I_C - V_{CE}$ plots. Since the current through the p-n junction is strongly dependent on the applied voltage V_B is then forced to increase so that I_{cb} increases. As a consequence, the MIS becomes more forward biased and this increases the emitter current, and hence I_{ec} because I_{eb} has been reduced due to the increasing channel resistance. When the increase of I_{ec} is greater than the increase of I_{cb} the collector current, I_C, will increase as shown in figure 6.20. Since I_E and hence I_{ec} is dependent upon the MIS bias the increase of I_C occurs at the same applied voltage V_{CE}, 4 - 6 volts, for this device in all cases.

However, when the collector voltage exceeds the base voltage (at the voltage limit of the current source) the current source is unable to maintain the constant

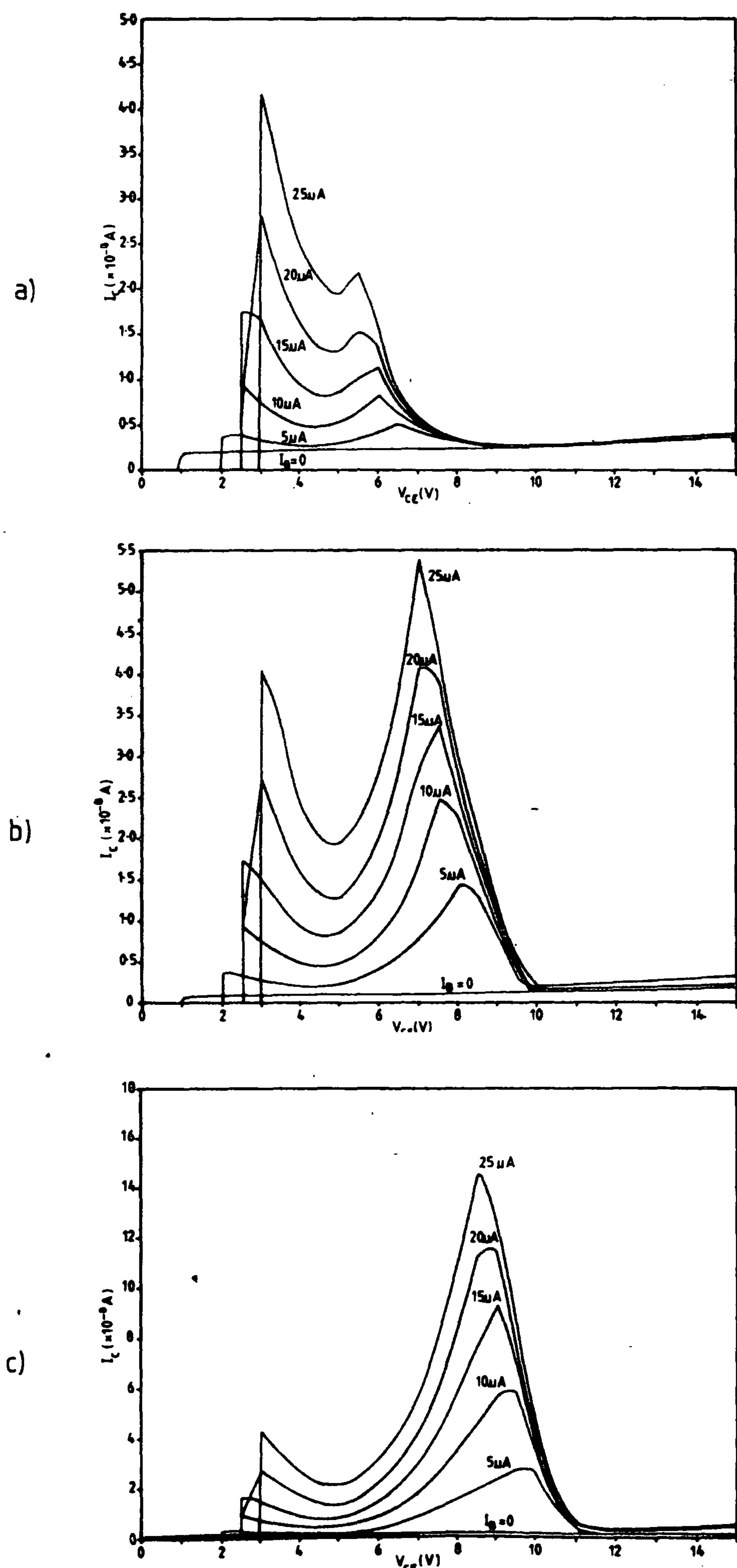


Figure 6.20 The dependence of the N-type negative resistance charateristic on the voltage limit of the constant current source, **a)** V_{lim} =5V, **b)** V_{lim} =6V and **c)** V_{lim} =7V.

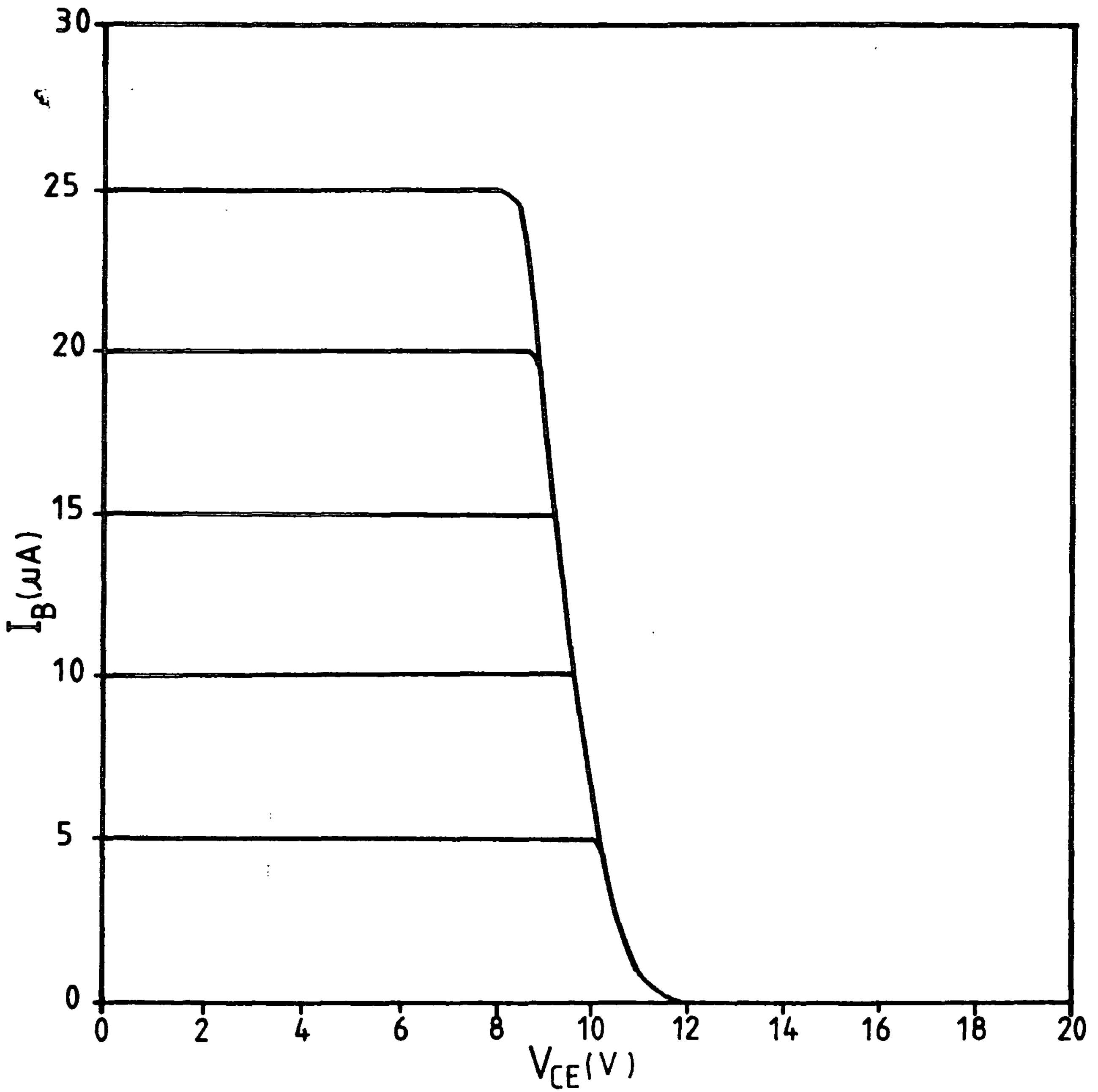


Figure 6.21 The base current drop to zero when V_{CE} exceeds the voltage limit $V_{B_{lim}}$ of the constant current source.

current through the base. The collector-base junction is then reverse biased and I_{cb} is limited by a generation current. As a result the base current drops to zero drastically as shown in figure 6.21. Now the whole system is in reverse bias so that the total current through the device, ie. the collector current, decreases to the value of the generation current.

6.5 CONCLUSION

The work reported in this chapter was on some of the characteristics of three terminal MISS devices which were fabricated at Southampton University. When a device is biased in the switching direction the three terminal MISS behaves like a thyristor. The MIST device is more sensitive to the injection of a majority carrier current from the third terminal rather than the injection of minority carriers. The control efficiency is also governed by a two- dimensional effect and a large emitter area gives a more sensitive control. An external shunt resistance across the p^+-n junction altered the switching characteristics and the switching parameters increase as the shunt resistance decreases. This behaviour may be used to turn the device OFF without lowering the biasing current.

MIS-emitter transistors using the present structure but reverse bias polarities have shown a small current gain and therefore they are not suitable for practical applications since conventional transistors can offer much better gain. If the base width is very thin and the doping concentration in the base region is relatively high, an N-type negative resistance appears in the I-V characteristics for base currents greater than zero. This is considered to be a new phenomenon since no similar behaviour has been reported before. With the exception of this the MIST and MIS-emitter transistors have shown generally the same type of characteristics when fabricated with SRO as previously reported for tunnel oxide structures.

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CHAPTER SEVEN

NEGATIVE RESISTANCE AND CAPACITANCE OF THE SRO-MISS DEVICE

7.1 INTRODUCTION

Negative resistance elements can be classified into two types corresponding to their appearance in the current-voltage characteristics. The negative resistance where the current decreases with increasing voltage is referred to as an N-type negative resistance or voltage-controlled negative resistance. In this case, for the load line AB (figure 7.1(a)) three values of voltage are possible. This device is said to be d.c. voltage stable, if a single operating point is determined by a stiff constant voltage source, as shown by load line CD. Another type of negative resistance is known as an S-type negative resistance where the current increases with decreasing voltage (figure 7.1(b)). Within the negative-resistance range for a load line such as AB, three values of current are possible. With a load line CD however, only one value of voltage is possible. Therefore this type of negative resistance device is said to be current stable or to have current controlled negative resistance (CCNR); i.e. its stable operating point is determined by an almost constant-current source.

This chapter is concerned with the S-type negative resistance of the MISS device. In earlier work in the department the negative resistance was found to be stable when an operating point in the negative resistance region is defined without any oscillation. This stability was not understood, since in all the literature in the field the S-type negative resistance had been described as an unstable process [1]. However, during

the course of this work, a reasonable explanation about the negative resistance was found. In this chapter we commence with the brief review of other mechanisms of the S-type negative resistance, followed by the stability analysis of the negative resistance circuit and its consequences ie. negative capacitance.

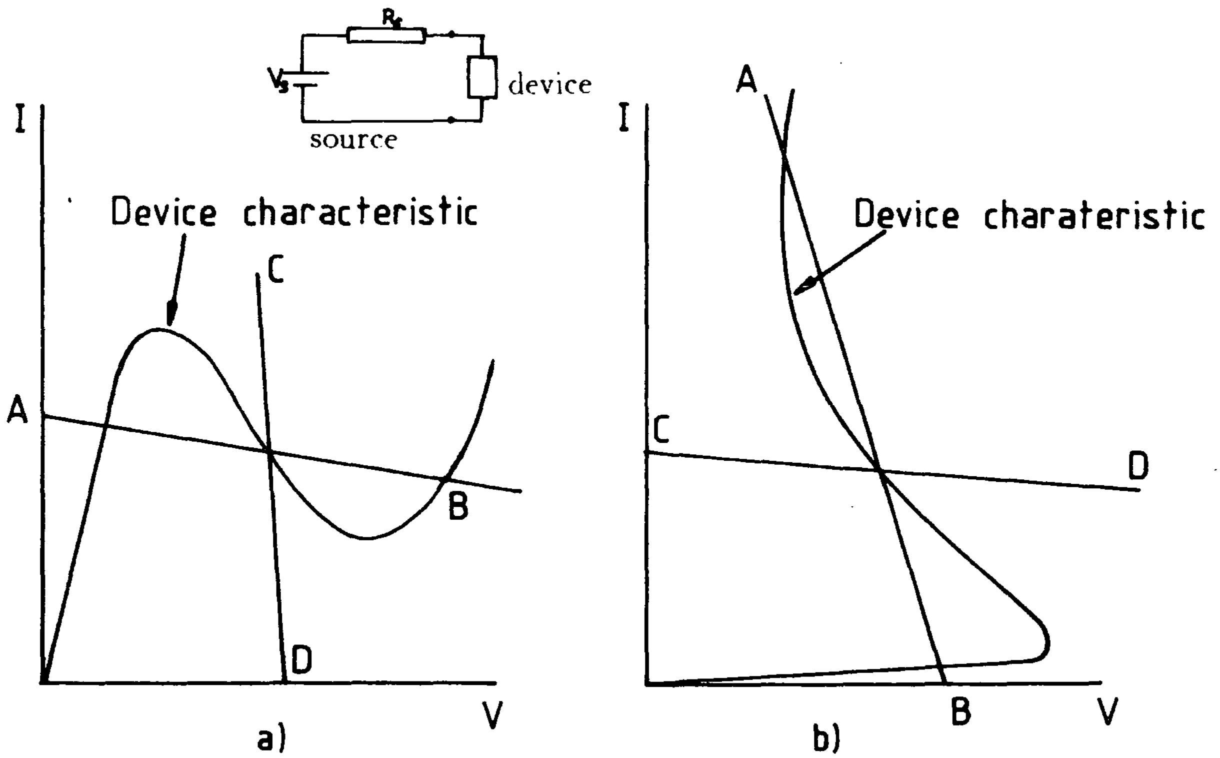

Figure 7.1 **a)** N-type negative resistance, **b)** S-type negative resistance. AB source characteristic with multi-valued operating point, CD source characteristic with single value operating point

7.2 ELECTRONIC MECHANISMS GIVING S-TYPE NEGATIVE RESISTANCE

Although this thesis is concerned with the stable S-type negative resistance of the MISS device, it is important to understand the mechanism for the unstable negative resistance of other devices so that a comparison can be made. The unstable S-type negative resistance which occurs in some devices can be explained by any

of three mechanisms:- double injection, conductivity modulation, or the negative resistance mechanism in a disorder material.

The negative resistance in the p-i-n diode is one example of the double injection mechanism. The important requirement for the mechanism to take place is the existence of a large density of trapping centres in the middle region of the band gap. The electrons and holes are injected from the cathode and anode respectively. At low voltage, the electrons can travel from cathode to anode since their lifetime is infinite. On the other hand, the lifetime of holes injected from the the anode is short, so that they are unable to traverse the bar. However at some critical voltage, the field across the bar is high enough to allow the holes to transit to the cathode, resulting in the filling of some of the hole traps. The hole lifetime begins to rise permitting more holes to transit the bar at a lower voltage. As a result the negative resistance is established [1].

An example of the conductivity modulation mechanism which results in a negative resistance is that of a unijunction transistor(UJT) (figure 7.2). The injected holes from the emitter into the n-type base region will increase the conductivity in the region between the emitter and the base terminal 1. As the conductivity increases, the effective resistance will decrease, and more current will flow in. Thus, the voltage dropped between the emitter and the base 1 decreases as the emitter current increases, and this will result an incremental negative resistance region in the I-V characteristics. The negative resistance region is a result of the variation of conductivity in the region between emitter and the base 1 due to high injection effects. The negative resistance will exist only if the injected minority carriers were sufficient to change the conductivity of the region.

The S-type negative resistance can also occur in a disordered material. The negative resistance phenomena in chalcogenide glass alloys was first observed by Ovshin-

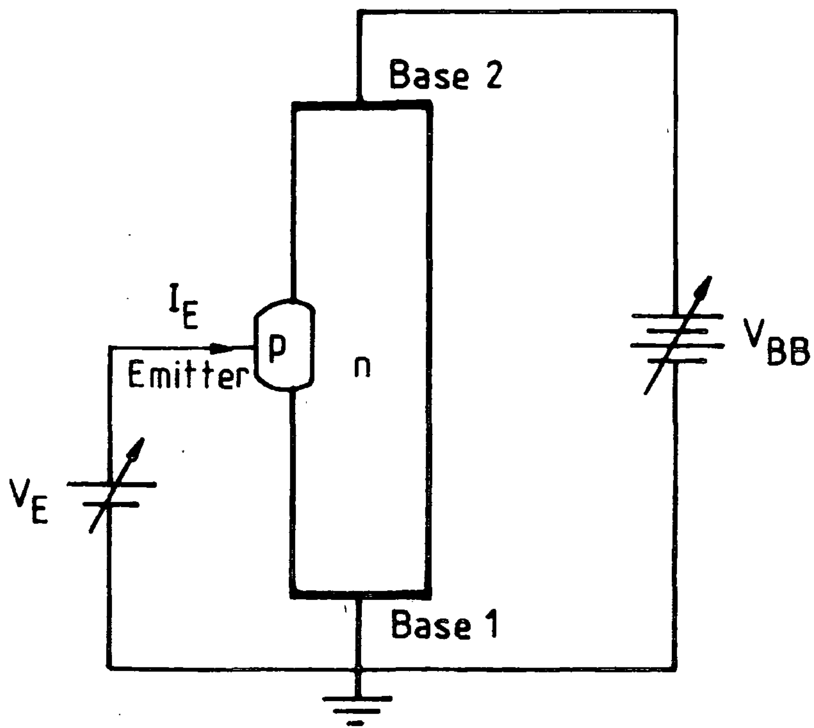

Figure 7.2 Schematic diagram of unijunction transistor.

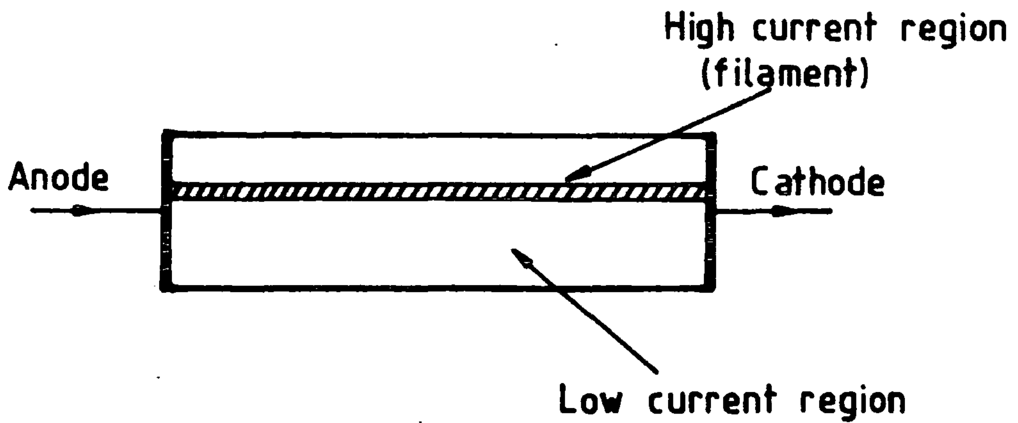

Figure 7.3 Filamentary current in bulk material.

sky [3]. At low applied voltage the conduction is ohmic with a resistance of the order of $10^5\Omega$. When the electric field exceeds a critical value of 10^5V/cm a rapid transition from the highly resistive to the conductive state occurs. The switching process is believed to be closely tied to the structure of the disordered and amorphous material [4].

Ridley [2] seems to suggest that, all the mechanisms for the current controlled negative resistance (CCNR) in the I-V characteristics will lead to current flow by means of filamentary conduction between the anode and cathode (figure 7.3). This is a general property of all bulk CCNR devices and does not depend on the specific way in which the characteristic arises. Most of the current flows through a small cross section a, whose resistivity is lower than that of the surroundings, because it has a higher current density. Such filaments in the p-i-n structure are flooded with holes and electrons in almost equal number over approximately 1-10μm in diameter [5]. Ridley also showed that the interaction between the filamentary device and an external circuit leads to instability [2]. These conclusions are not necessarily true of complex device structure such as the MISS which has a negative resistance due to the change of the voltage distribution.

In the following section we will discuse the stability of the negative resistance in a simple circuit.

7.3 STABILITY OF A NEGATIVE RESISTANCE CIRCUIT

The stability of the negative resistance can be realized by analysing the circuit using a Laplace transformation as proposed by Morant [6]. A physical system is said to be stable if any small perturbation in the operating condition produces a decreasing response of the system. An equivalent statement to this is that a system is stable if

every bounded input results in a bounded output, BIBO. Based on this definition the condition for BIBO stability is that all the poles of the system function must lie in
of the complex impedance.
the left half plane (l.h.p.); otherwise a step function (a bounded input) would initiate an unbounded response [7].

7.3.1 Stability Analysis

Let us consider the case of a negative resistance device in a measurement circuit with a series load resistance. The small signal a.c. equivalent circuit can be represented as shown in figure 7.4(a) where R_L and L are the load resistance and inductance of the external circuitry respectively, R_d is the negative slope resistance of the device and C_d is the total parallel capacitance of the device and the external circuit.

Figure 7.4(b) shows the I-V characteristics with load line bias in the negative resistance region. As we can see a small change in supply voltage of δV_s will give rise to a change δV_d in the device voltage. In other words a change in the input voltage results in a change in the output voltage. Therefore, the transfer function of the circuit can be expressed in the form of a Laplace transformation as in equation 7.1 (details of the analysis is given in appendix F),

$$\mathbf{H}(\mathrm{s}) = \mathbf{L}\left[\frac{\delta V_d(t)}{\delta V_s(t)}\right] = \frac{R_d}{1+\mathrm{s}R_dC_d}\left\{(R_L+\mathrm{s}L)+\frac{R_d}{1+\mathrm{s}R_dC_d}\right\}^{-1} \qquad 7.1$$

As shown in appendix F, this transfer function can be simplified to,

$$\mathbf{H}(\mathrm{s}) = \frac{1}{LC_d}\frac{1}{(\mathrm{s}+X+\frac{1}{2}\sqrt{Y})(\mathrm{s}+X-\frac{1}{2}\sqrt{Y})} \qquad 7.2$$

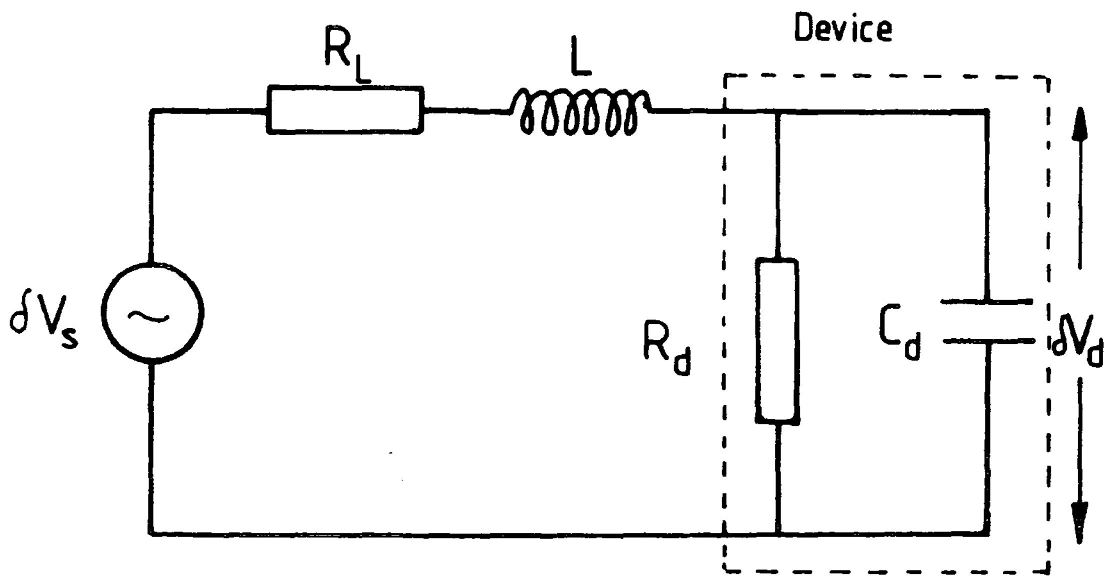

Figure 7.4 a) Small signal equivalent circuit of a negative resistance device.
b) Negative resistance and load line.

where,

$$X = \frac{L + R_d R_L C_d}{2LC_d R_d} \qquad \text{and} \qquad Y = \left(\frac{L + R_d R_L C_d}{LC_d R_d}\right)^2 - 4\frac{R_d + R_L}{LC_d R_d} \qquad 7.3$$

The inverse Laplace transform of equation 7.2 is given by,

$$\frac{\delta V_d(t)}{\delta V_s(t)} = \mathbf{L}^{-1}\mathbf{H}(\mathrm{s}) = \frac{1}{LC_d\sqrt{Y}}(e^{-(X+\frac{1}{2}\sqrt{Y})t} - e^{-(X-\frac{1}{2}\sqrt{Y})t}) \qquad 7.4$$

For Y *positive*, if $(X + \frac{1}{2}\sqrt{Y})$ and $(X - \frac{1}{2}\sqrt{Y})$ are positive all poles of equation 7.2 lie in the left hand plane or from equation 7.4 the response is a decaying function (figure 7.5). This shows that the system is stable. On the other hand if both or either $(X + \frac{1}{2}\sqrt{Y})$ or $(X - \frac{1}{2}\sqrt{Y})$ is negative, the poles will lie in the right hand plane, and the response will be a voltage growing exponentialy.

For Y *negative*, equation 7.4 can be written as,

$$\frac{\delta V_d(t)}{\delta V_s(t)} = \mathbf{L}^{-1}\mathbf{H}(\mathrm{s}) = \frac{1}{LC_d\sqrt{Y}}(e^{-(X+\frac{1}{2}j\sqrt{|Y|})t} - e^{-(X-\frac{1}{2}j\sqrt{|Y|})t}) \qquad 7.5$$

and can be represented as,

$$\frac{\delta V_d(t)}{\delta V_s(t)} = j\frac{2}{LC_d\sqrt{Y}}e^{-Xt}\sin(\frac{\sqrt{Y}t}{2}) \qquad 7.6$$

As we can see, if X is positive the response will be a decaying oscillation and if X is negative the response is a growing oscillation. If $X = 0$ for Y both positive and negative the response is a constant oscillation.

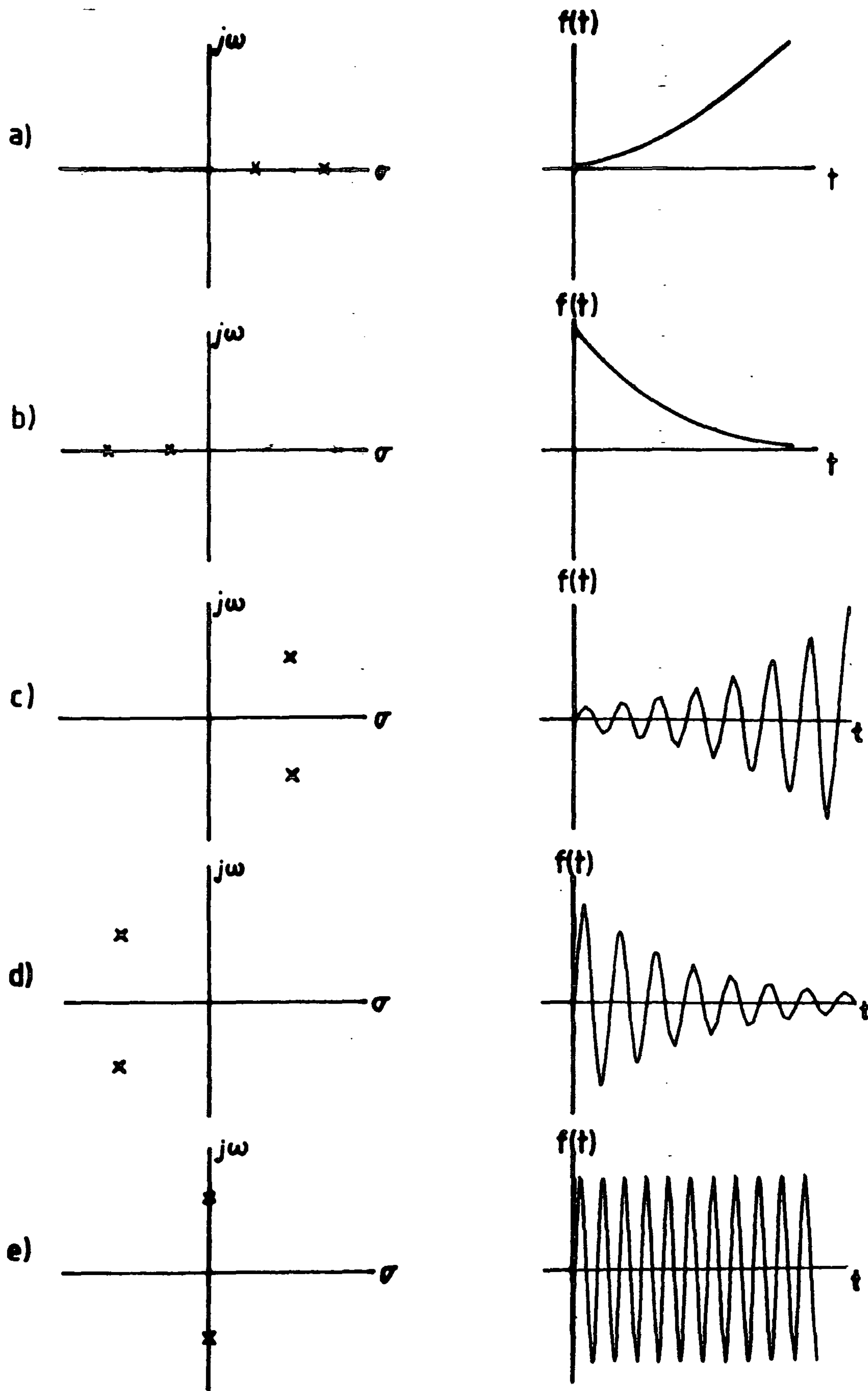

Figure 7.5 Poles position in a complex s-planes and its response.

7.3.2 Circuit Stability with Negative Resistance

Evaluating the above equations gives us the a.c. stability condition which corresponds to the value of load resistance as demonstrated in figure 7.6. Hines [8] produced a stability condition for a similar negative resistance circuit as shown in figure 7.7 which gives the same condition as in our analysis. These analyses show that the circuit will be unstable if the ratio of R_L to $|R_d|$ is either too small or too large. The value of load resistance for the stable state as shown in figure 7.6 is,

$$\frac{L}{|R_d|C_d} < R_L < |R_d| \qquad 7.7$$

Figure 7.7 also shows that the circuit stability depends on the ratio of capacitance to inductance. If the ratio is too large or too smalll the circuit will be unstable. This is the case if C_d has a normal positive value.

For an S-type negative resistance device there is no d.c. stability condition for $R_L < |R_d|$ because there is no unique operating point in the negative resistance region. Raising the voltage from zero will cause the operating point to stay in the low current region until the maximum voltage is reached after which the operating point will jump to the high current region. On the other hand reducing the voltage will cause the operating point to proceed along the high current part until the minimum voltage is reached, and the operating point then jumps to the low current region.

7.3.3 Circuit Stability with MISS Device

With MISS devices it was found experimentally that the circuit with a high value of $R_L(> |R_d|)$ gave a stable operating point. The d.c. stability is expected because the

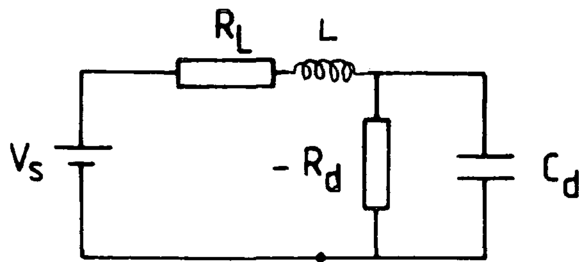

Figure 7.6 Stability condition of a negative resistance and positive capacitance supplied from a source of resistance R_L at a constant operating point.

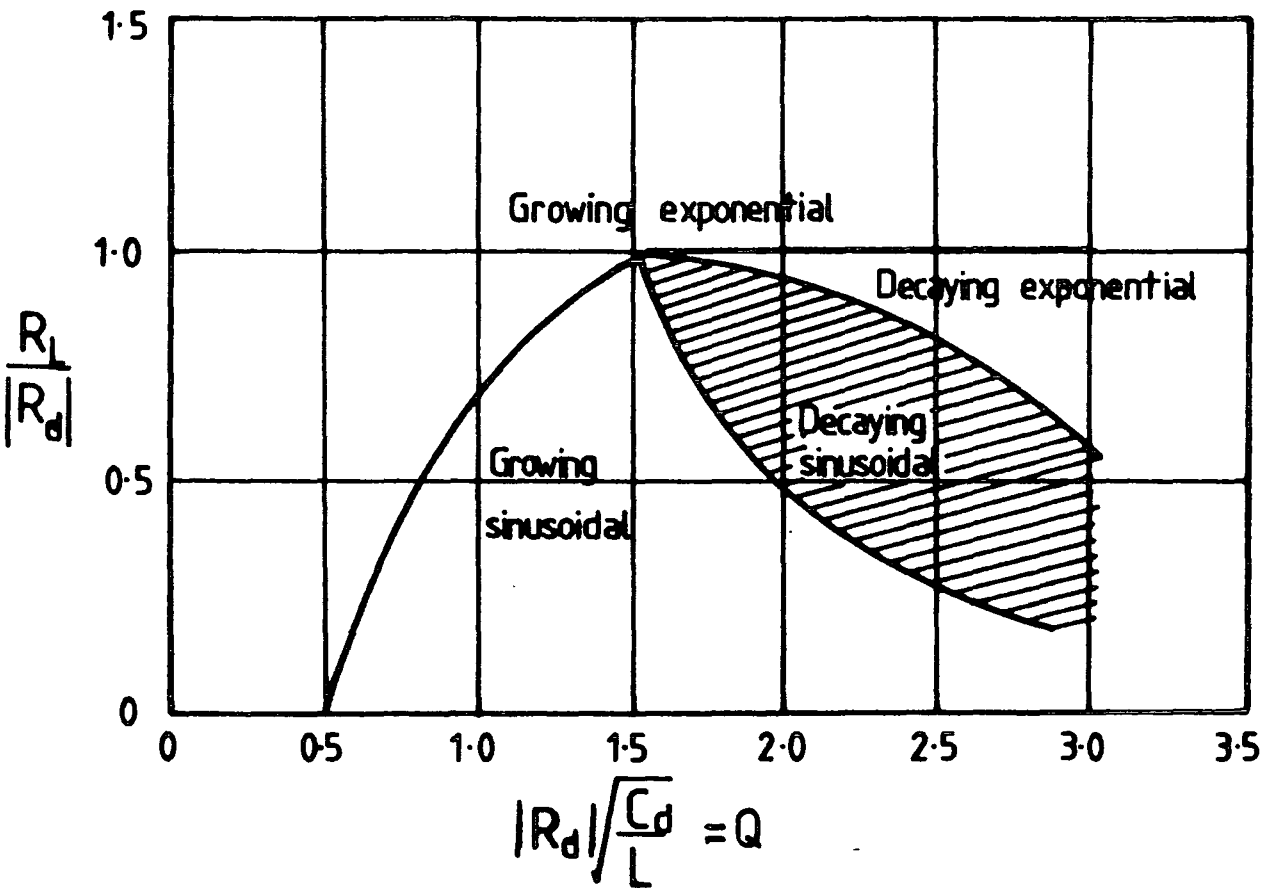

Figure 7.7 Stability condition of a negative resistance circuit produced by Hines [from ref. 8]

source and device characteristics only intersect at one point in the negative resistance region. However the analysis above shows that the circuit should be a.c. unstable with normal circuit components. The only explanation for the stability of the circuit is that the MISS device capacitance C_d must also be negative. Further justification for this conclusion will be given in section 7.4.1.

By substituting a negative value of C_d in the previous equation (see appendix F), the circuit is stable if the load resistance, R_L, is greater than the magnitude of the negative resistance, $|R_d|$, and there are no oscillation condition as long as the total capacitance is negative. The total capacitance is the sum of the negative device capacitance and the positive parallel stray capacitance of the circuit. If $R_L < |R_d|$ hysteresis occurs in the d.c. I-V characteristics, similar to the case of negative resistance with a positive capacitance, and the circuit is a.c. unstable only with a negative capacitance. From the definition, a negative capacitance means that the total charge decreases with increasing voltage and this phenomenon has been confirmed theoretically in MISS devices by parallel work in Durham [18].

7.3.4 Conclusion.

The stability of the negative resistance is determined by whether or not the device has an internal oscillation and also in its interaction with the external circuit. For the device with no internal oscillation, the only cause of unstability is due to the interaction with the circuit. A filamentary conduction mechanism as proposed by Ridley [2] does not necessarily apply for a device structure which exhibits the S-type negative resistance.

The interaction with an external circuit can be summarised as follows.

a) An S-type negative resistance with a positive capacitance cannot be obtained

both d.c. and a.c. stable in practice.

b) An S-type negative resistance can also be stable (and can be plotted) only if the device has a negative capacitance.

c) The series resistance of the measurement circuit must be greater than the magnitude of the negative resistance for (b) to hold.

d) For stability in (b) the circuit capacitance must be smaller than the magnitude of the negative capacitance of the device, so that the total capacitance of the circuit is negative.

7.4 MEASUREMENTS OF SMALL-SIGNAL NEGATIVE RESISTANCE OF THE SRO-MISS

7.4.1 Oscillation State

By graphical analysis it is clear that the negative resistance of the MISS can be traced if a sufficiently high value of load resistance

$$R_L > |R_d| \approx \frac{V_s - V_h}{I_h - I_s} \qquad 7.8$$

is used. Several researchers in the field have reported that some MISS devices exhibit an intermediate state which they considered as the third stable state in the negative resistance region [9,10,12]. The origin of that state was not clearly understood, but based on the regenerative positive feedback model, Habib and Simmons [11] appear to suggest that the so-called intermediate state is possible if the substrate doping is comparable to the epitaxial doping although this was not the case for all the devices reported to have an intermediate state.

Now we have proved that the negative resistance of the MISS can be stable, with no oscillation observed, and we account for this by the effect of the negative capacitance of the device. If the stray capacitance of the circuit is greater than $-|C_d|$, the total capacitance becomes positive and the circuit oscillates strongly. The effect of oscillation on the measured d.c. characteristic produces severe distortion in the measured d.c. negative resistance region. The so-called intermediate state which can be demonstrated in some device- circuit combinations is in fact due to the circuit oscillation. This oscillation is caused by the positive total effective capacitance of the circuit which determines its the frequency. Figure 7.8 shows a MISS characteristic which demonstrates the effect of external positive capacitance. The stable negative resistance measurement can be disturbed by putting an external capacitance across the device causing the so-called intermediate state to appear with an oscillation that can be observed with an oscilloscope. If the external capacitor is disconnected the oscillation ceases and the stable steady state negative resistance can again be plotted. The slope of the oscillation state depends on the magnitude of the external capacitance as shown in figure 7.9. As the capacitance is increased the slope of the apparent characteristic becomes more steep. This is because of the change in the frequency and waveform of the oscillation as the capacitance is changed. As can be seen, the existence of the oscillation state may give an apparent, but false, holding point in the measurement which seems to depend on the value of the external capacitance *.

This experiment has shown that the oscillation in the negative resistance circuit is due to the capacitance of the external circuitry. The so-called intermediate state is an unstable condition which results from the circuit oscillation. To obtain the true device characteristic it is important to ensure that the circuit is stable.

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* This is the reason why a good measurement circuit is necessary in order to get the accurate value of holding current

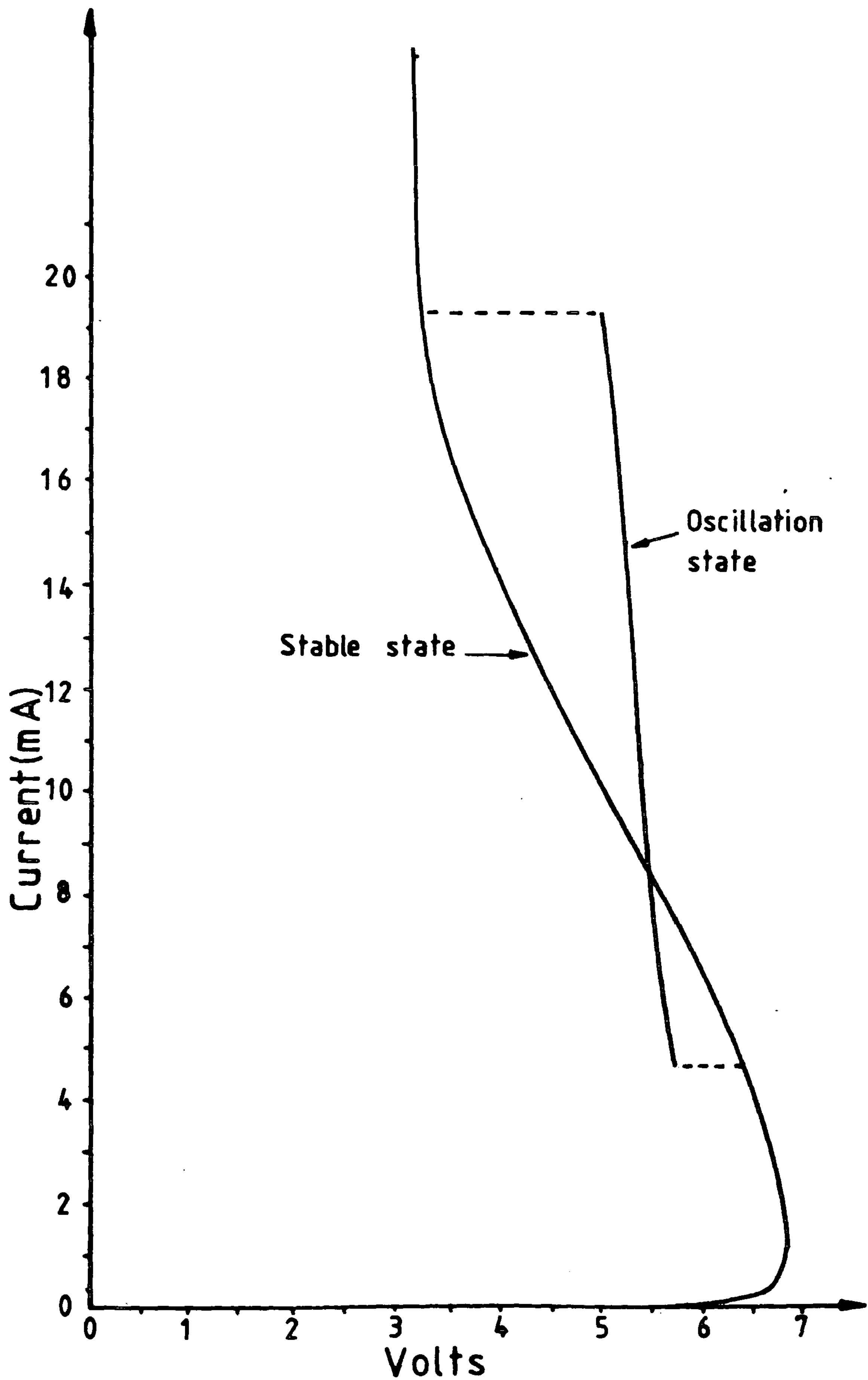


Figure 7.8 Effect of external capacitance on the stable negative resistance region of the MISS.

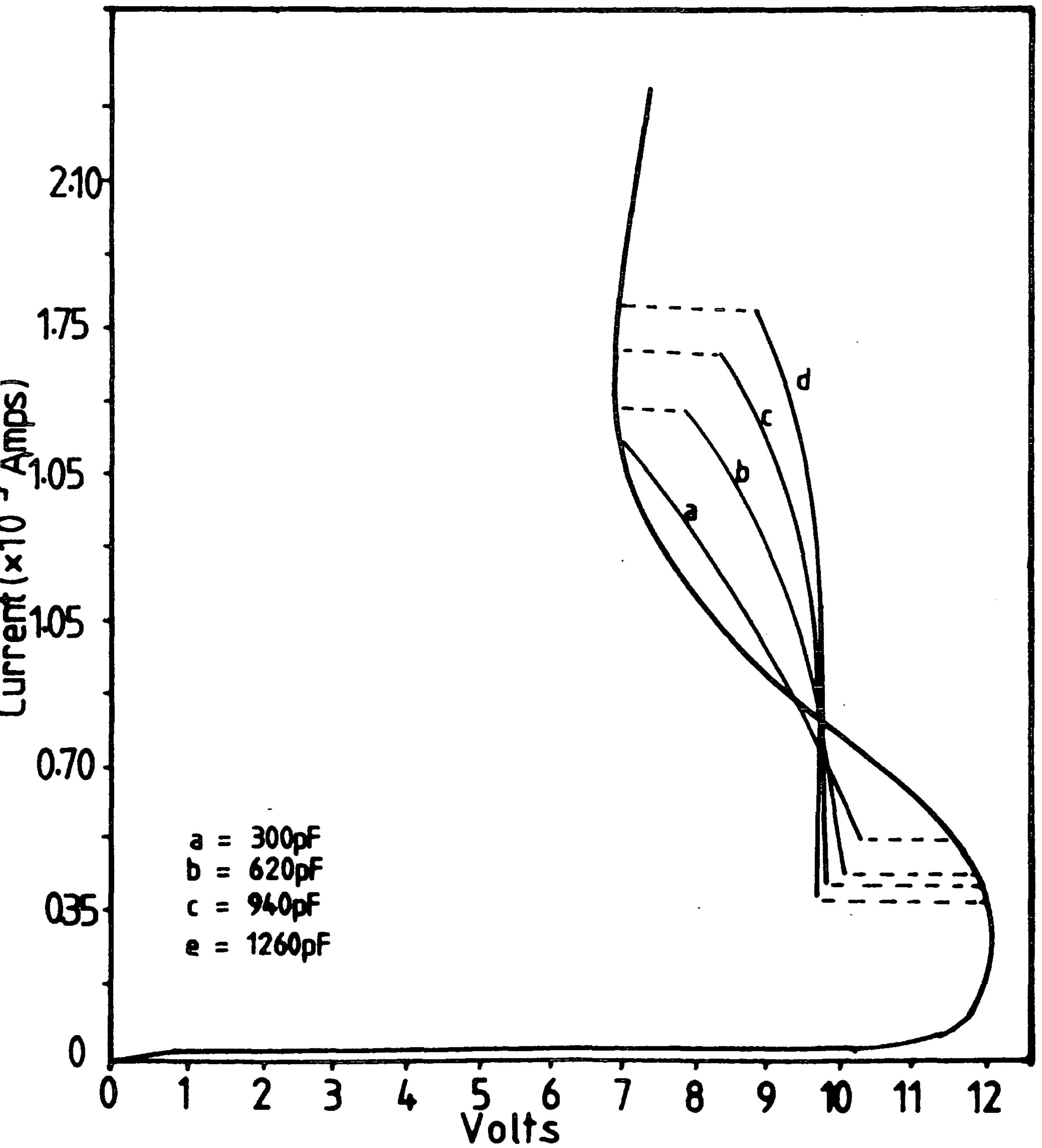


Figure 7.9 An oscillation states with different values of external capacitance.

7.4.2 A.C. Negative Resistance Measurement

The measurement circuit as described in Chapter 4 was used to obtain reliable stable characteristics for the MISS device. The negative differential resistance of the MISS can be calculated by measuring the tangent at every point along the negative resistance region. Figure 7.10 shows a plots of the a.c. negative resistance as a function of voltage of the MISS from the sample SRO17(A=0.89mm^2, d=245Å, n=3.0). The a.c. negative resistance increases as the voltage decreases from the switching point, it reaches a maximum value almost at the middle of the negative resistance region, and decreases again as the voltage approaches the holding point. At the switching and holding voltages the device a.c. resistance, $|R_d|$, is zero and beyond these points the resistance is positive. Therefore, we can define the switching and holding parameters from the points at which the differential resistance is zero.

Figure 7.11 shows comparative plots of $|R_d|$ against voltage for different size devices. As we can see the position of $|R_d|_{max}$ in the negative resistance region shifts closer to the switching voltage as the device size decreases. The variation of $|R_d|_{max}$ with device electrode area seems to show a linearly decrease as shown in figure 7.12. This is a direct consequence of the changes in V_s, I_s, V_h and I_h with electrode area as described in Chapter 5.

7.5 MEASUREMENTS OF THE NEGATIVE CAPACITANCE OF THE SRO-MISS

7.5.1 Introduction

Basically, the total small-signal capacitance of the MISS device can be written as,

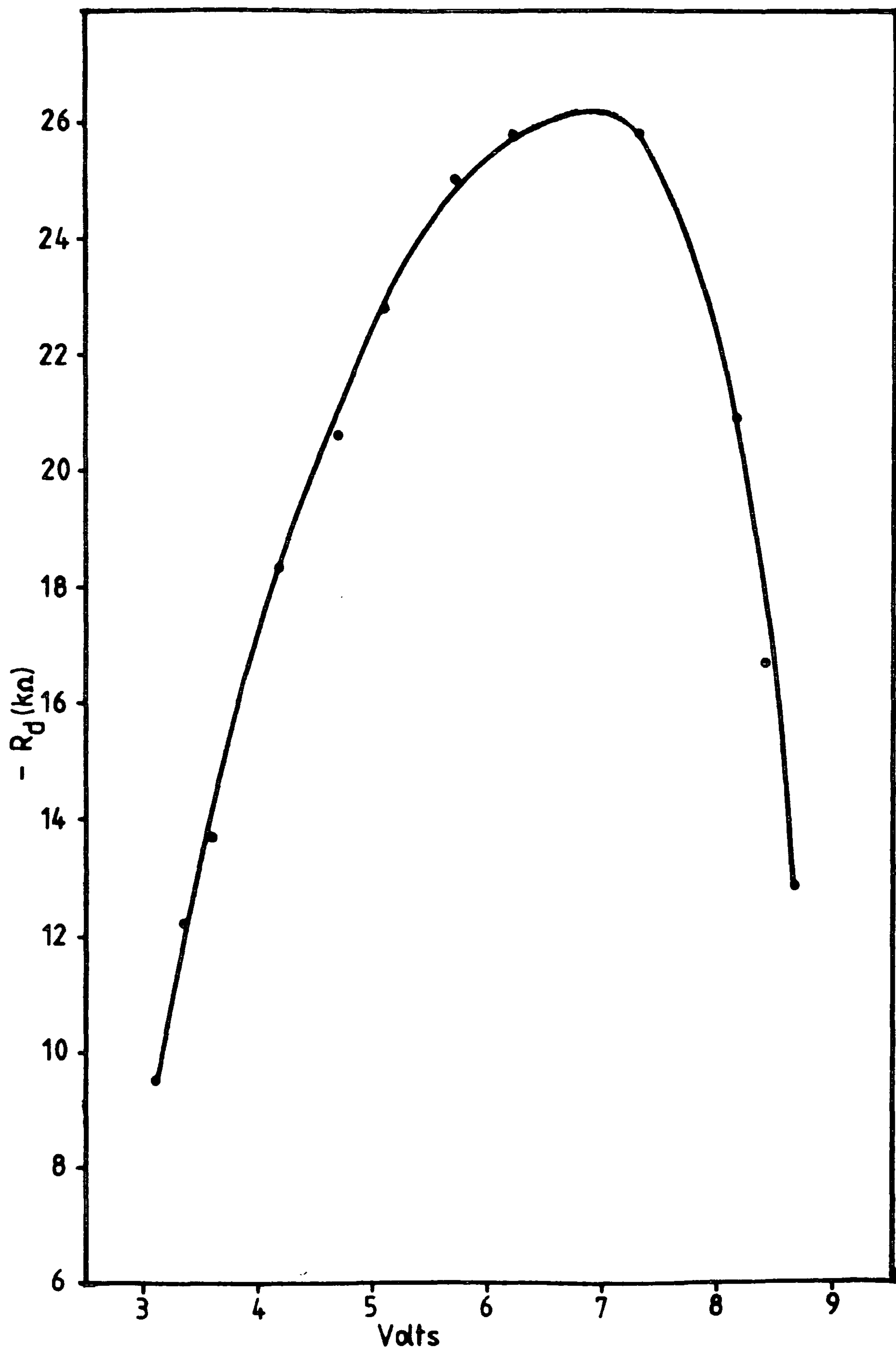


Figure 7.10 A.C. negative resistance as a function of voltage within the negative resistance region.

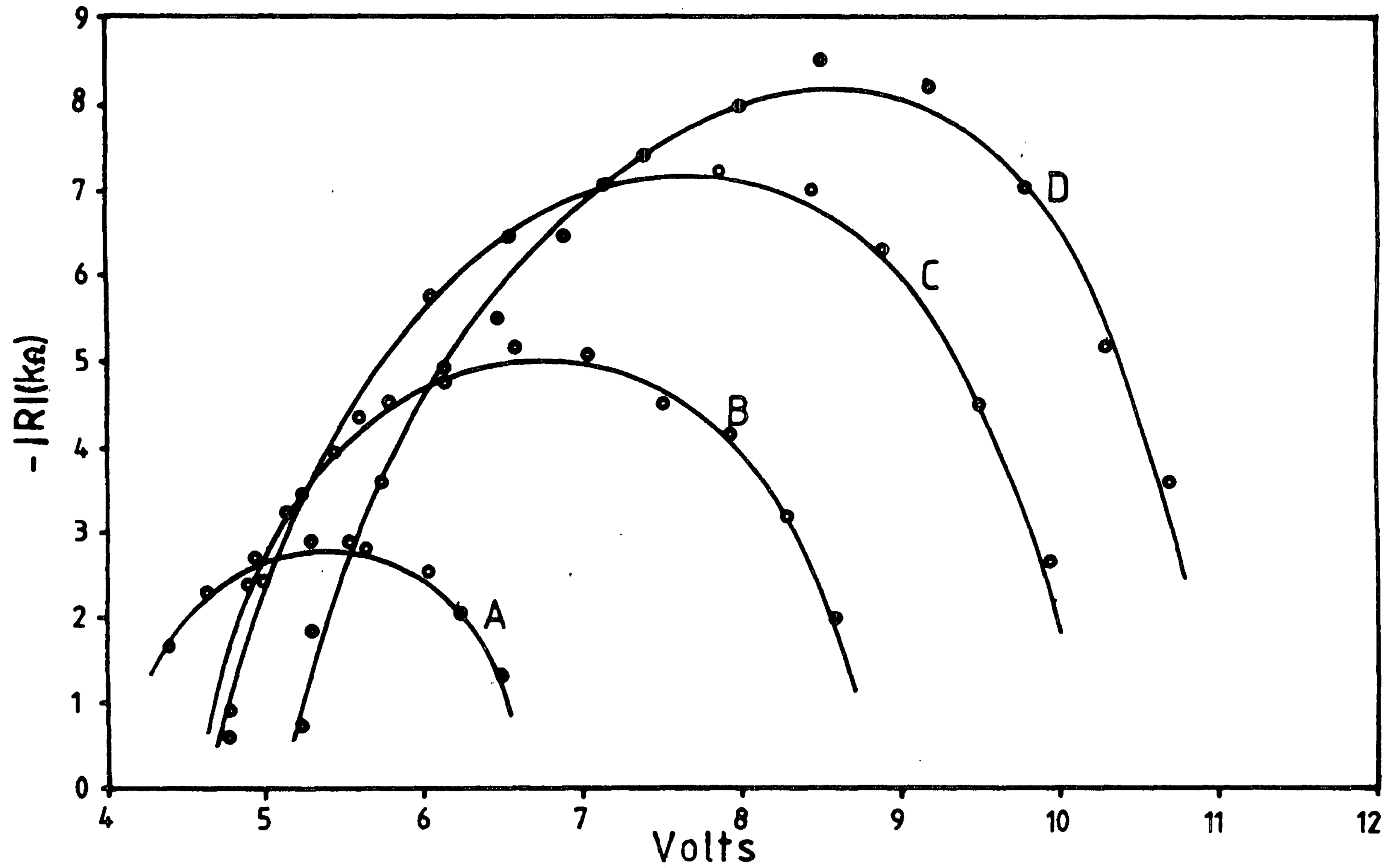


Figure 7.11 A.C. negative resistance of the MISS with a different electrode areas ($A=2.36mm^2$, $B=1.55mm^2$, $1.12mm^2$ and $D=0.89mm^2$)

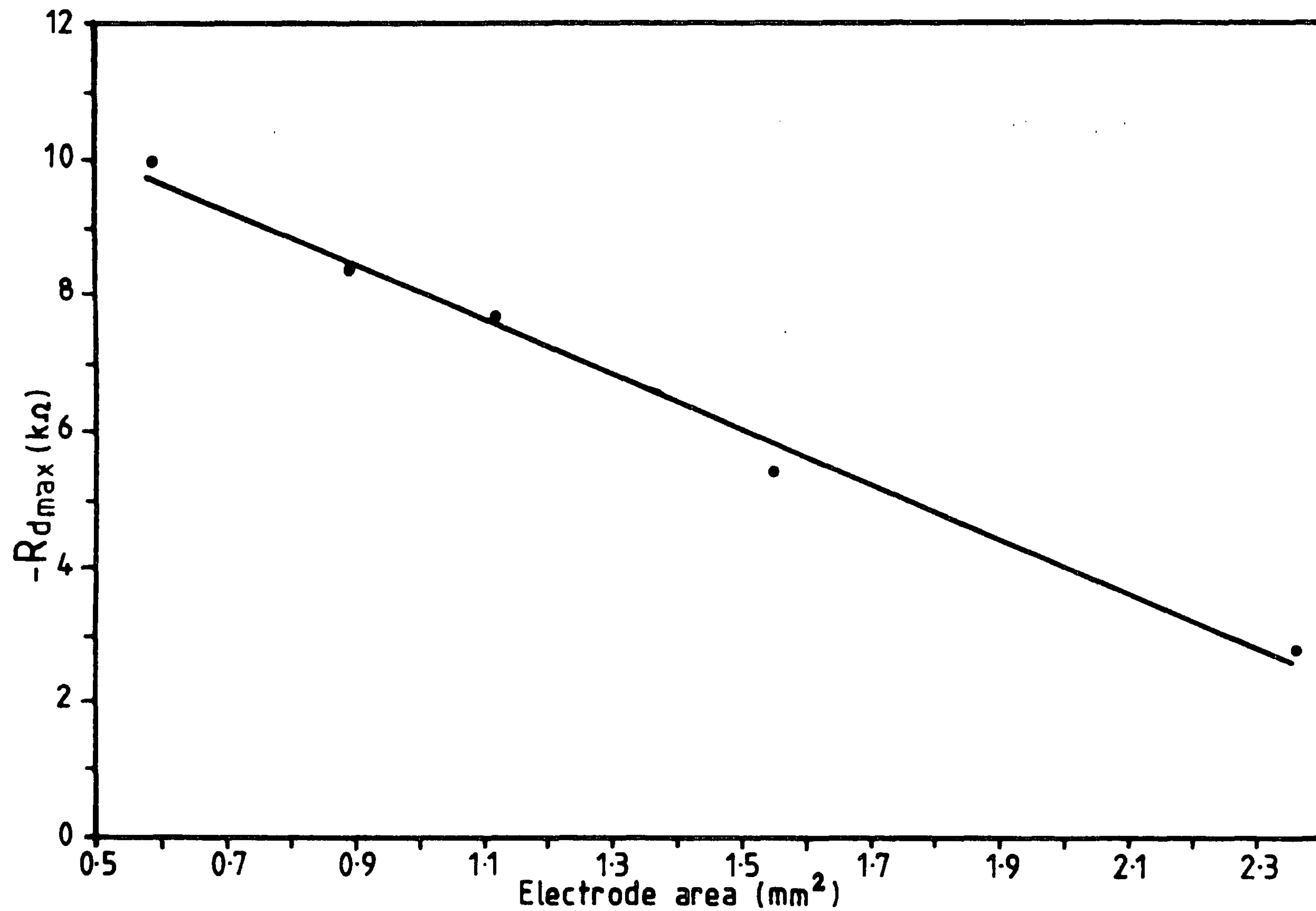


Figure 7.12 Variation of $|R_d|_{max}$ with electrode area.

$$\frac{1}{C_d} = \frac{1}{C_I} + \frac{1}{C_s} + \frac{1}{C_j} \qquad 7.9$$

where C_I, C_s and C_j are the capacitances of the semi- insulator, depletion region and n-p^+ junction respectively, and both C_j and C_s are voltage dependent. In the reverse biased MISS, the p-n junction is reverse-biased and the MIS is in the state of accumulation i.e. forward biased. Since most of the applied voltage drops across the reverse-biased p-n junction, C_j dominates the total capacitance which therefore decreases as the voltage increases. In the off-state of the forward biased MISS, C_s decreases as the the voltage is increased because the MIS junction goes into the depletion regime and dominates the total capacitance. These capacitances are positive, and can easily be measured using a standard C-V technique.

In the negative resistance region of the forward biased MISS a special technique is required to measure the device capacitance which has been shown in the previous section to have a negative value. This capacitance is different from that reported by Millan et al [13] where a negative value was reported in the off state. Recently, Bhosale et al [14] have reported that a thin film Al- V_2O_5-Al switching device also exhibited negative capacitance in the off- state.

7.5.2 Measurement Technique of the Negative Capacitance

The negative capacitance of the device cannot be measured using a standard capacitance-voltage measurement technique due to circuit instability in the negative resistance region, as was described previously. The negative resistance circuit has to be stable in practice if we want to measure the capacitance of the device in this region. Based on the circuit analysis Morant [6] has suggested the basic idea of how the negative capacitance could be estimated. The technique presented here has never

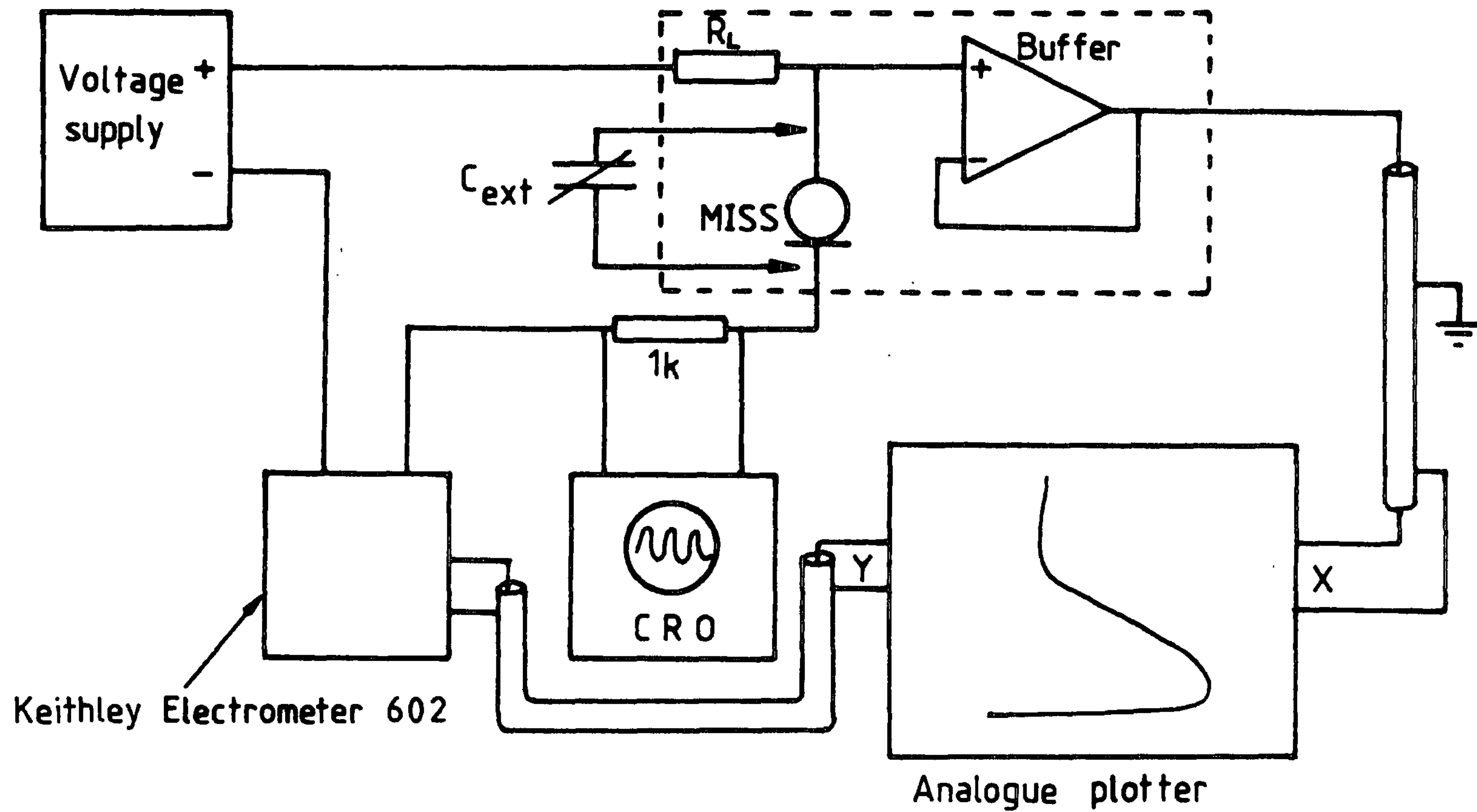


Figure 7.13 The circuit arrangement used to measure the negative capacitance of the MISS.

been carried out before, and to the best of our knowledge no previous work has been published on this technique.

It has been shown that a stable negative resistance can only be realized if the total capacitance across the device in the measurement circuit is negative. The only capacitance which can possibly be negative is that of the device. It was also shown that if the capacitance is positive and the load resistance is greater than the magnitude of the negative resistance, the circuit will oscillate. Therefore by putting an external variable capacitor in parallel with the device, the circuit can be made to oscillate by adjusting the value of the external capacitor until the total capacitance become positive, when the oscillation can be observed on the oscilloscope. This was first reported experimentally by Clifton [19]. In this measurement, two disc type tuning capacitors with ranges of 50pF to 2500pF and 10pF to 150pF were used. The schematic diagram of the measurement technique is shown in figure 7.13. The value of the external capacitor when the circuit begins to oscillate is very slightly greater than the magnitude of the negative capacitance of the device. Therefore by measuring the capacitance of the external capacitor removed from the circuit without changing the setting we can get the value of the negative capacitance. This measurement was made using a Boonton 72B capacitance meter which operates at 1MHz. Using this technique, the negative capacitance of the MISS device was measured at every point along the negative resistance region. This technique is difficult to perform if the device capacitance is less than 10pF, and in general the smaller devices were far more difficult to measure.

7.5.3 Variation of Negative Capacitance with Voltage

Figure 7.14 shows a plot of the negative capacitance as a function of device voltage for the MISS device from the sample SRO17 (A=0.89mm^2, d=245Å,n=3.0).

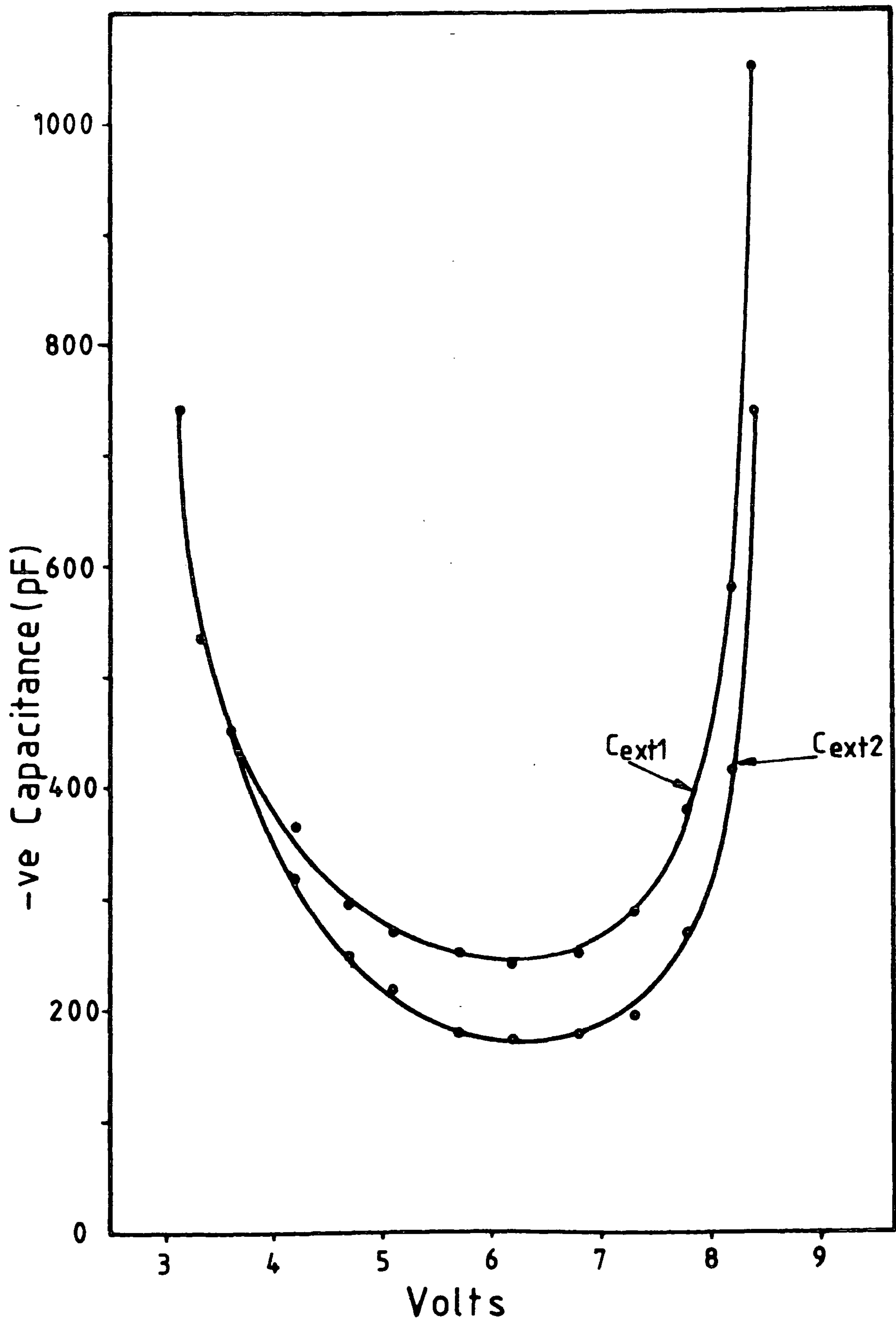


Figure 7.14 The negative capacitance of the MISS as a function of voltage in the negative resistance region.

The readings were taken by biasing the device in the negative resistance region and the external capacitor was adjusted until the oscillation appeared on the oscilloscope. The external capacitance then was reduced until the oscillation ceased. It was found that the capacitance required to stop the oscillation was slightly lower than the capacitance required to start it.

The circuit will oscillate when the total capacitance across the device becomes positive. When the capacitance C_{ext1} is just positive, the oscillation will start and grow rapidly until its amplitude reaches a maximum value with the device in the oscillation state as described in section 7.4.1. The total average voltage, V_{dt}, across the device is now changed by ΔV_d, due to the oscillation,

$$V_{dt} = V_d + \Delta V_d \qquad 7.10$$

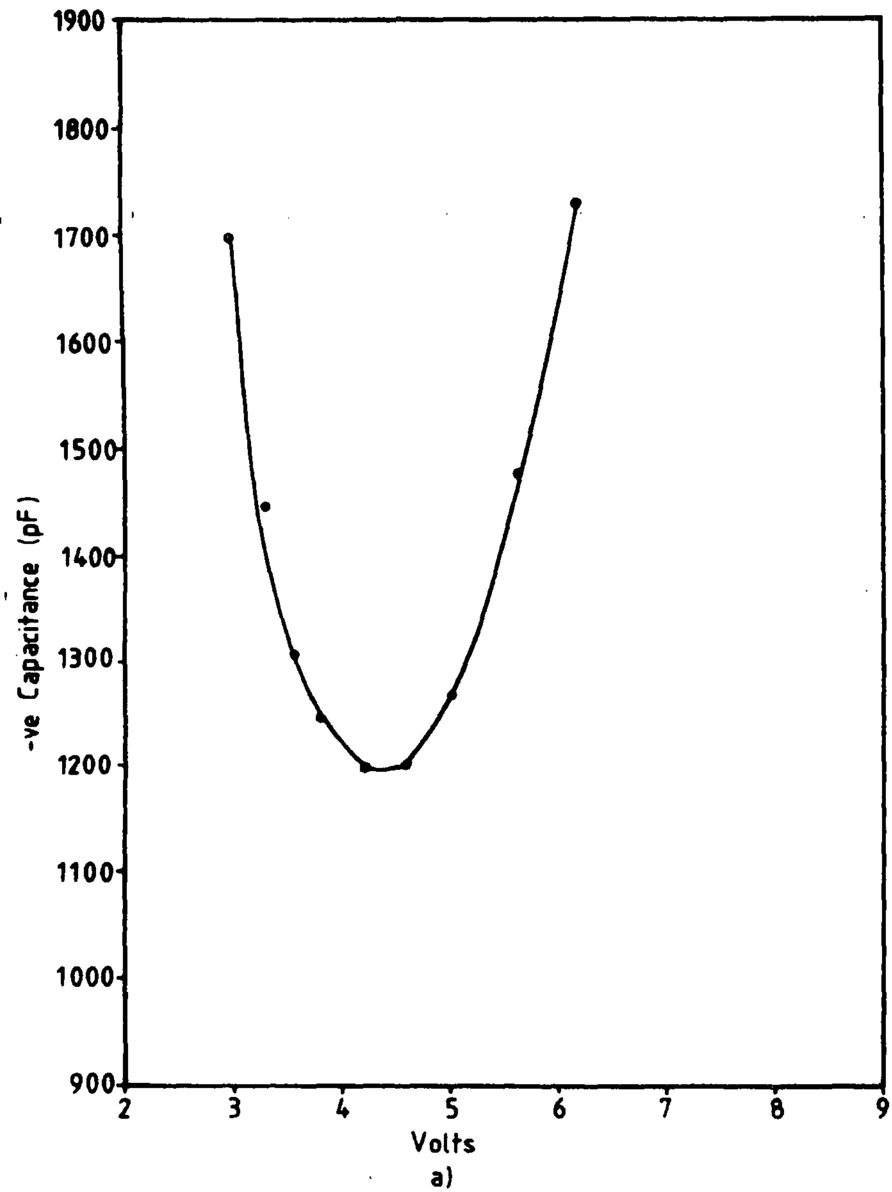
where V_d is the d.c. voltage across the device. From figure 7.9 in section 7.4.1, it was shown that V_{dt} jumped to a lower value when the oscillation started. Since the magnitude of the negative capacitance will first decrease as the voltage decreases, the new biasing point reduces the magnitude of the negative capacitance. As a result, the external capacitance, C_{ext2}, which was required to make the total capacitance negative and hence stop the oscillation is lower than that required to make the total capacitance positive, C_{ext1}. As it can be seen in figure 7.14, the difference between these two capacitances, $\Delta C = C_{ext1} - C_{ext2}$, decreases as the biasing point shifts towards the holding point. After the negative capacitance reaches its minimum value the shift of the biasing point is in the opposite direction, i.e. towards the switching voltage (figure 7.9) and ΔC decreases again. The true value of the negative capacitance is therefore seen to be the value of the capacitance at which the oscillation begins, that is to say $|C_d| \approx C_{ext1}$.

The capacitance in the negative resistance region can be defined as the ratio of the differential charge to the differential voltage. Therefore, the negative a.c. capacitance is the differential of a d.c. capacitance, Q/V, in which the charge increases while the voltage decreases. The current through the MISS in the negative resistance region is controlled by the distribution of the charge in the device. Therefore the negative capacitance is a function of dI/dV or $1/|R_d|$, and it is governed by the device parameters such as the conductivity of the SRO, device geometry (electrode and junction areas) and the doping concentration in the same way as R_d.

7.5.4 Effect of Electrode Area on Negative Capacitance

As been shown in Chapter 5 the switching parameters, V_s, V_h, I_s, and I_h are very dependent on the electrode areas. Since the magnitude of the negative capacitance is a function of these parameters the electrode area also has a very significant effect on the negative capacitance value. In this section the area dependence of the negative capacitance will be discussed.

Figure 7.15 shows comparative plots of the negative capacitance with different electrode areas. Since the negative capacitance is voltage dependent, and the range between the switching and the holding voltages varies for the different size devices, it is difficult to choose a reference voltage in which the value of the negative capacitance with different electrode areas can be taken. In the present case, the values of the negative capacitance near the holding voltage (about 10% from the holding voltage), and the minimum value were choosen as points for comparison.Figure 7.16 and 7.17 show the variations of the negative capacitance near the holding voltage and of the minimum values with electrode area. As we can see the negative capacitance decreases as the electrode area decreases, although the variation with area is not linear as it might have been expected. This phenomenon may be related to the two dimensional



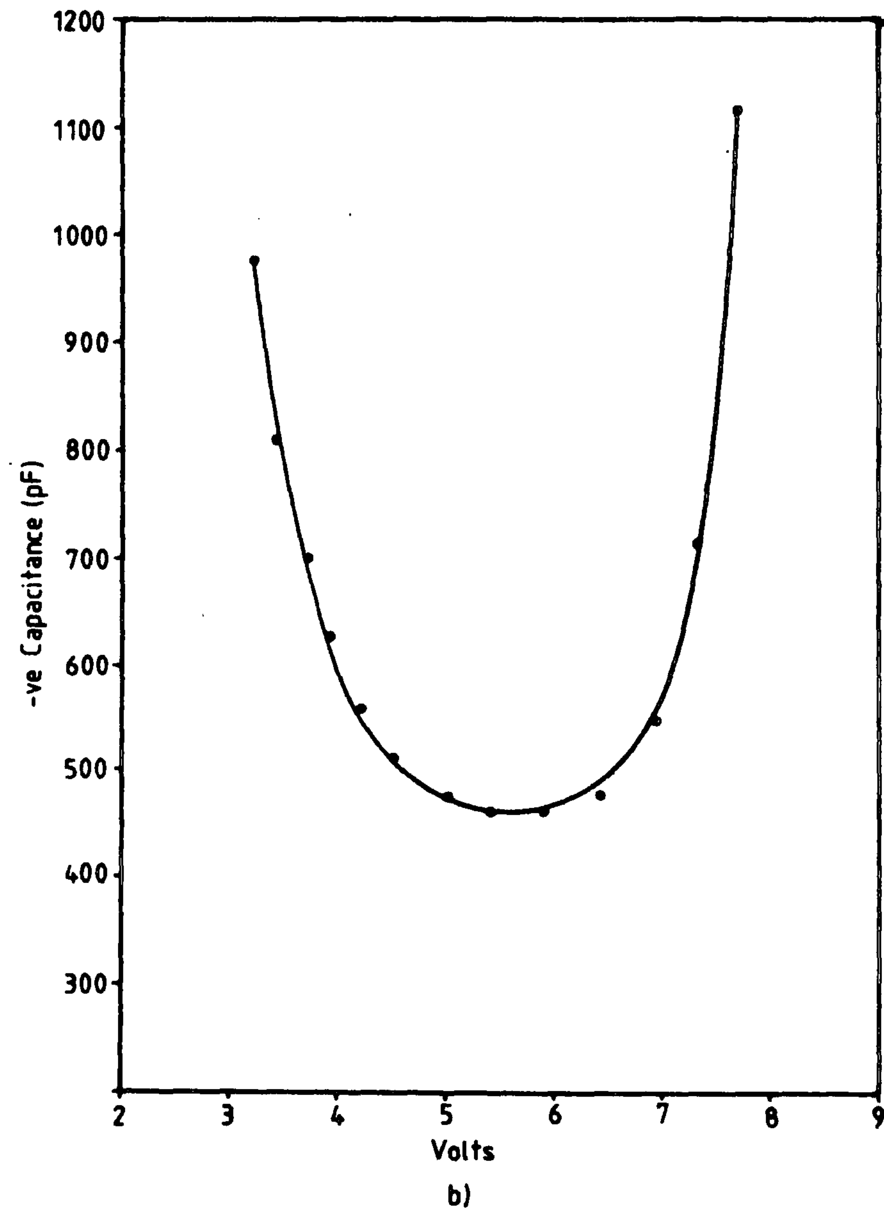


Figure 7.15 A plots of a negative capacitance with different electrode areas, a) $1.55mm^2$ and b) $1.12mm^2$. (Note: different vertical scale).

c) d)

Figure 7.15 (cont.) A plots of a negative capacitance with different electrode areas, **c**) 0.89mm^2 and **d**) 0.59mm^2. (Note: different vertical scale).

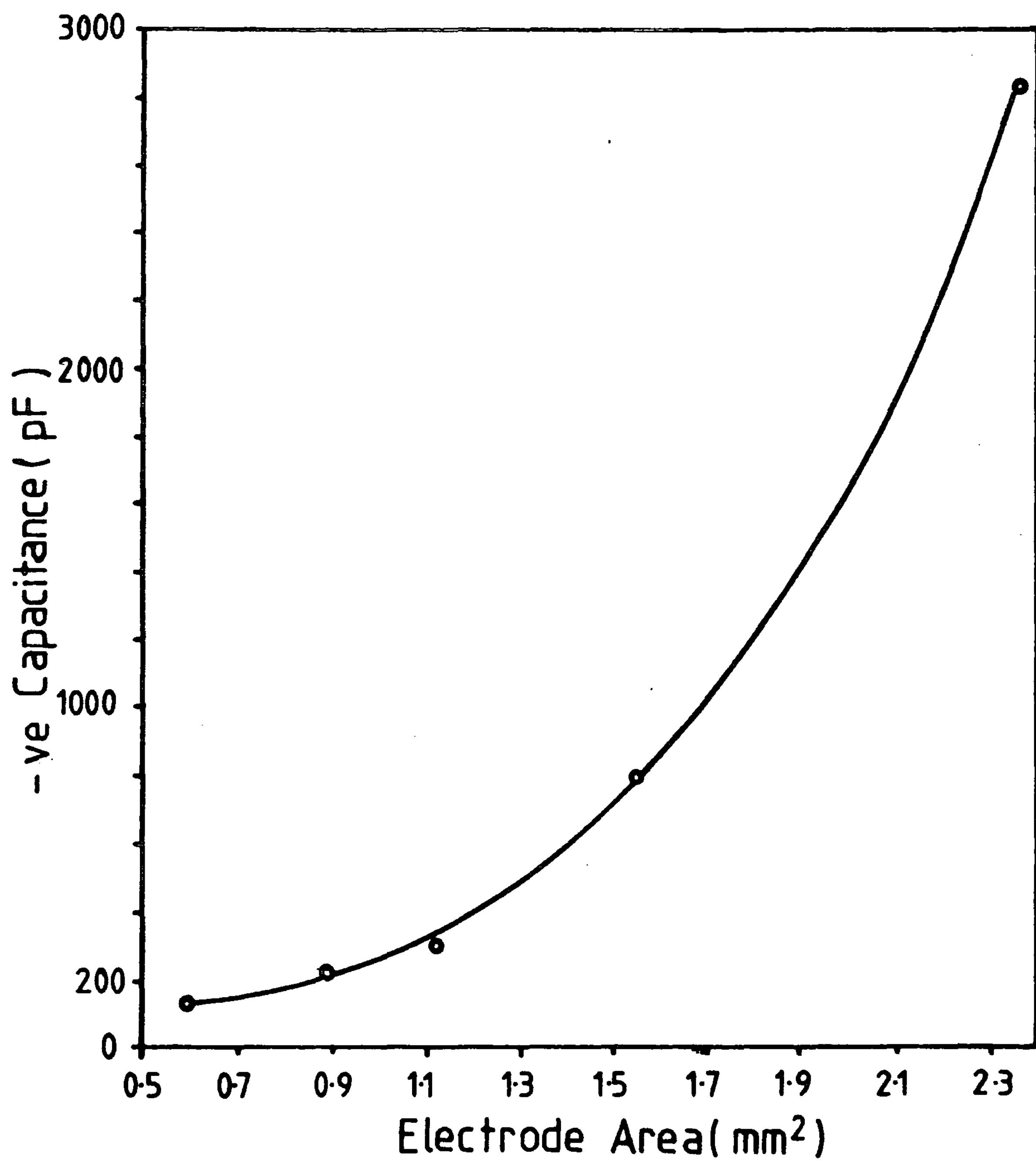


Figure 7.16 Variation of negative capacitance near the holding voltage with electrode area.

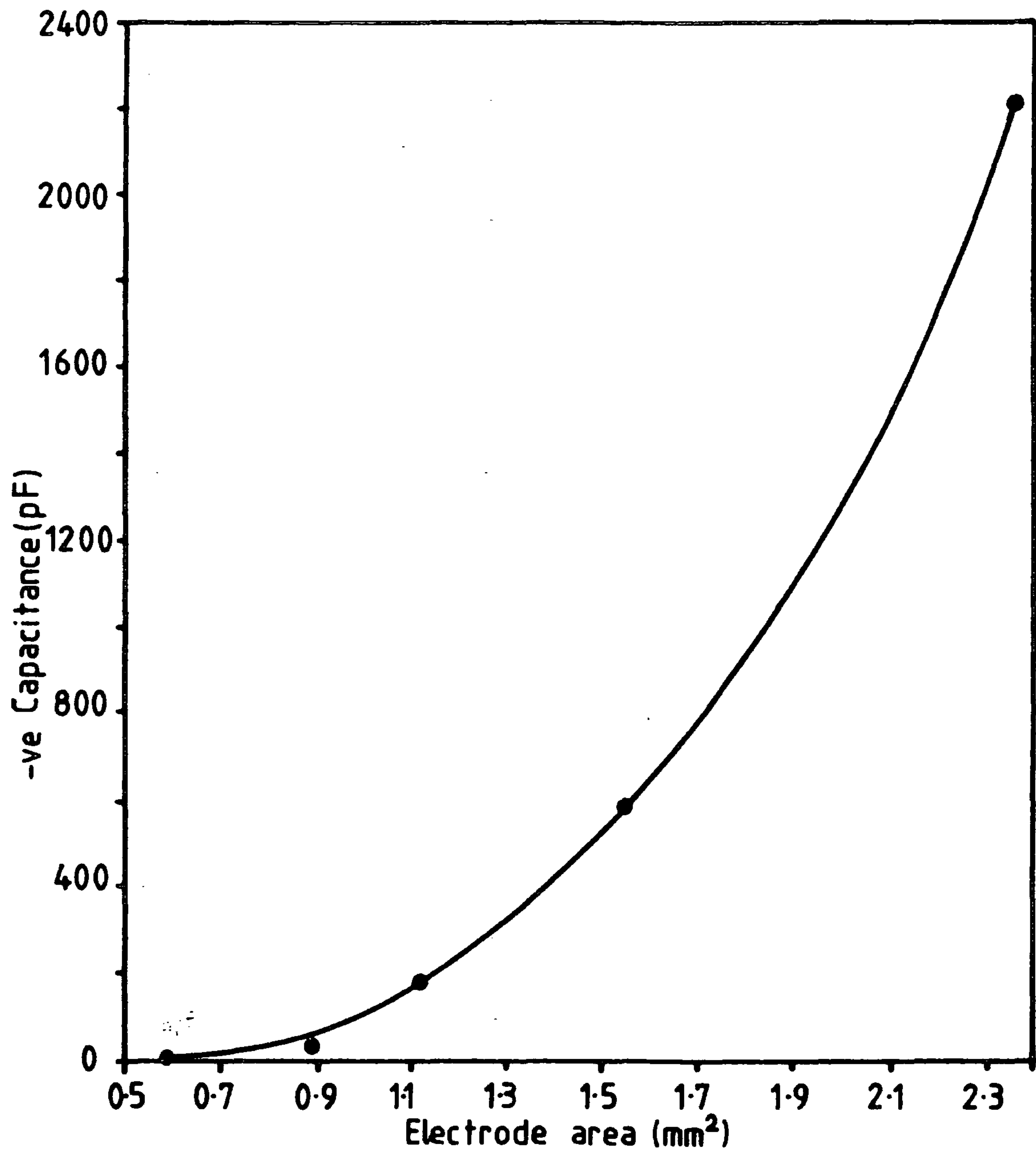


Figure 7.17 Variation of the minimum value of negative capacitance with electrode area.

effect and could be explained as follows.

The effective negative capacitance of the MISS is the total of the series capacitances of the semi-insulator, C_I, the depletion region, C_s, and the p-n junction, C_j, (equation 7.9). As C_j is very large it can be neglected. C_s is responsible for the negative value of the total capacitance, C_d, given by

$$C_d = -\frac{C_I|C_s|}{C_I - |C_s|} \qquad 7.11$$

In an ideal case C_I is linearly dependent on the electrode areas. However since all devices are nonisolated the variation of C_I is not linear with the area as shown by the measurements of a typical SRO layer capacitance for an MIS structure in accumulation as shown in figure 7.18, and this is due to the field spreading effect. By assuming that $|C_s|$ increases linearly with area, the total capacitance, C_d, can be calculated using the values of C_I from figure 7.18. A plot of the effective capacitance against area based on this calculation is shown in figure 7.19. As can be seen, the trend is similar to the experimental values as in figure 7.16 and 7.17. Therefore, it is strongly believed that, in ideal case where there is no spreading effect, the variation of the negative capacitance would be propotional to the electrode area.

As already shown, the magnitudes of both the negative capacitance and the negative resistance vary with voltage and they have a minimum and a maximum respectively in between the switching and holding voltages. The product of these values, C_dR_d, or the time constant therefore varies with voltage as shown in figure 7.20 for different electrode areas. As we can see, at a constant voltage the time constant increases with electrode area. The increase is not linear probably for the same reason as for the dependence of negative capacitance on area.

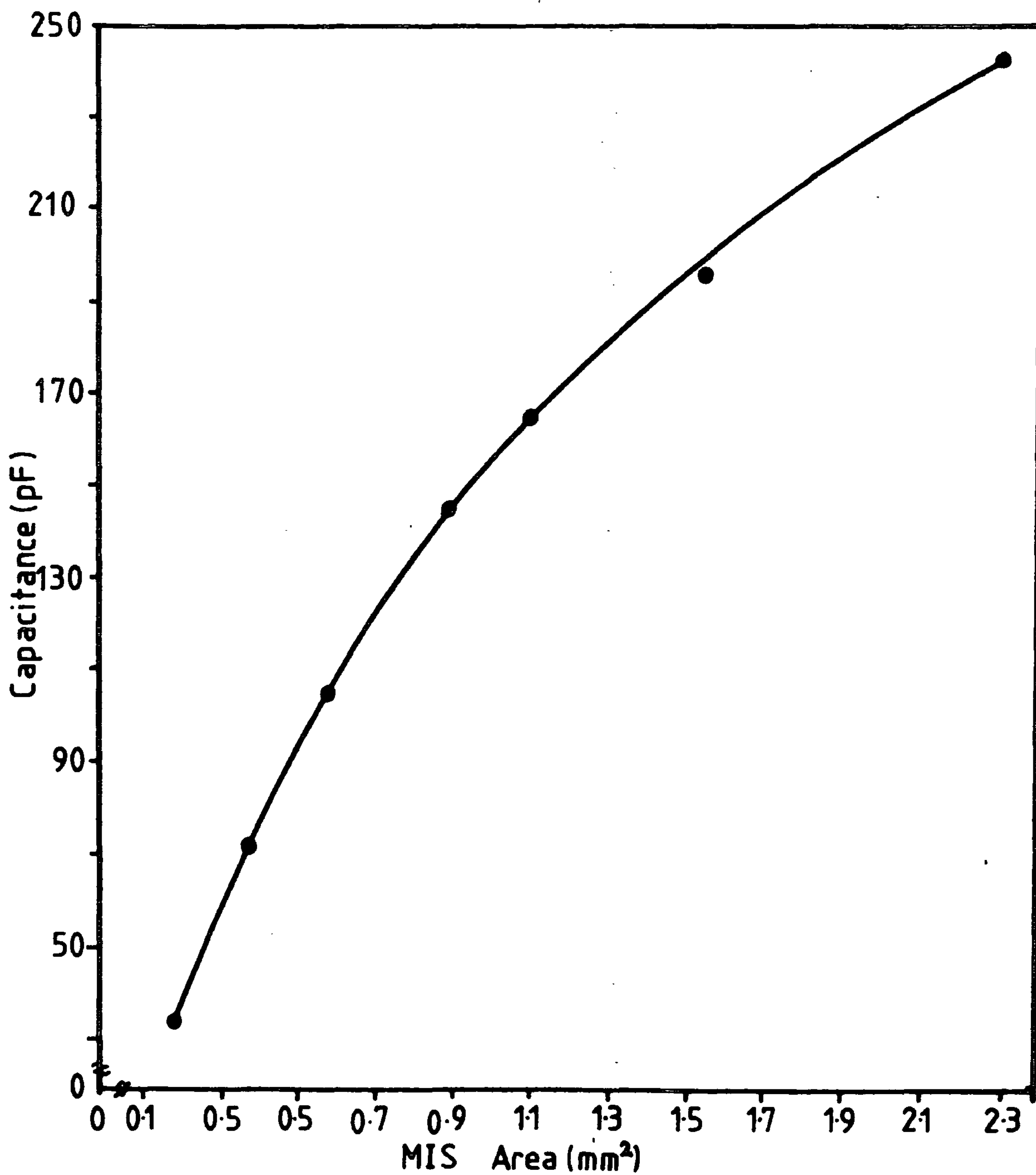


Figure 7.18 A typical SRO-MIS capacitance at accumulation as a function electrode area (SRO122: d=319$\mathring{A}$ and n=2.76)

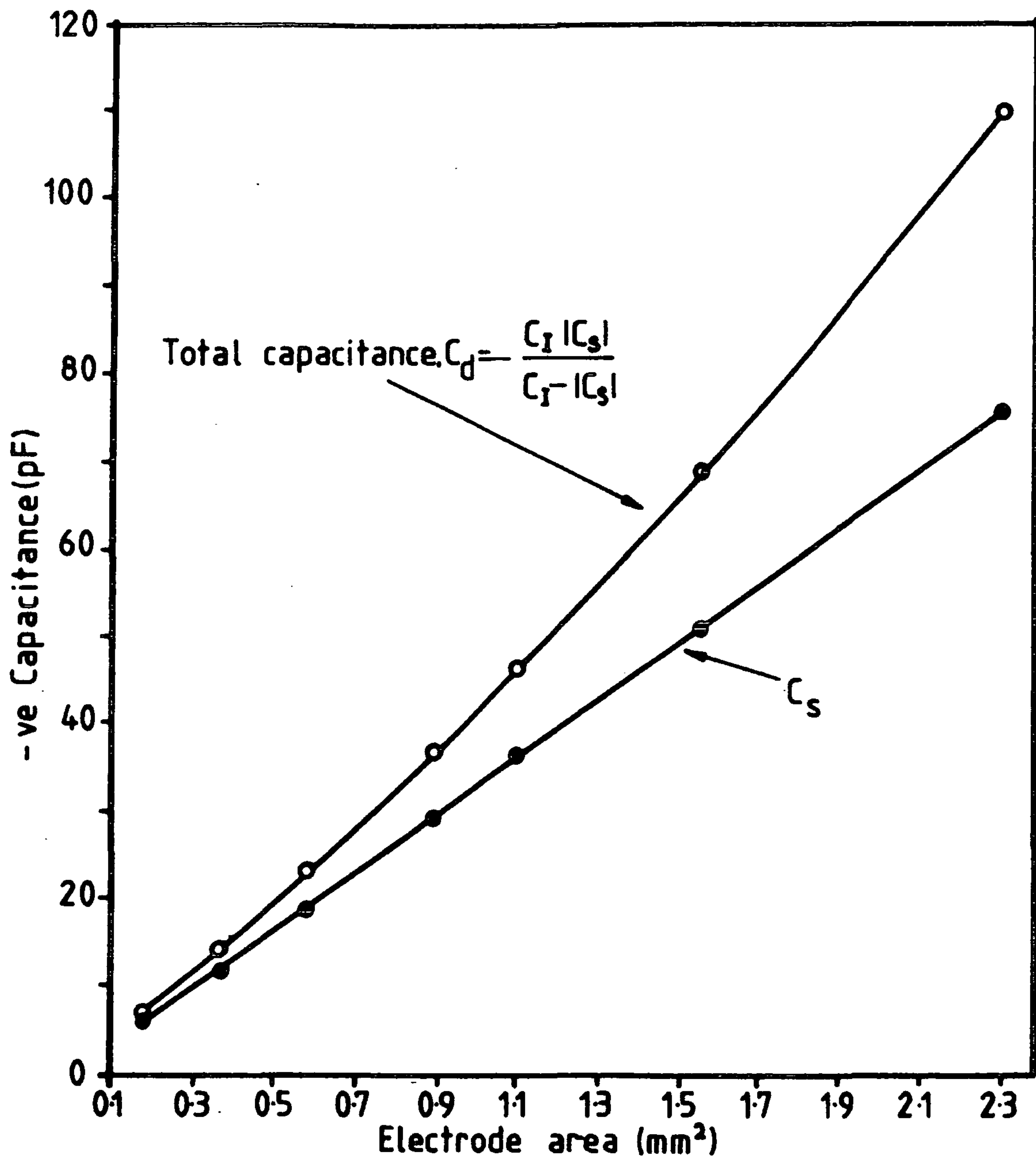


Figure 7.19 Variation of total negative capacitance with area, calculated by assuming that the depletion negative capacitance C_s is linear dependent with electrode area and using a typical measured MIS capacitance C_I.

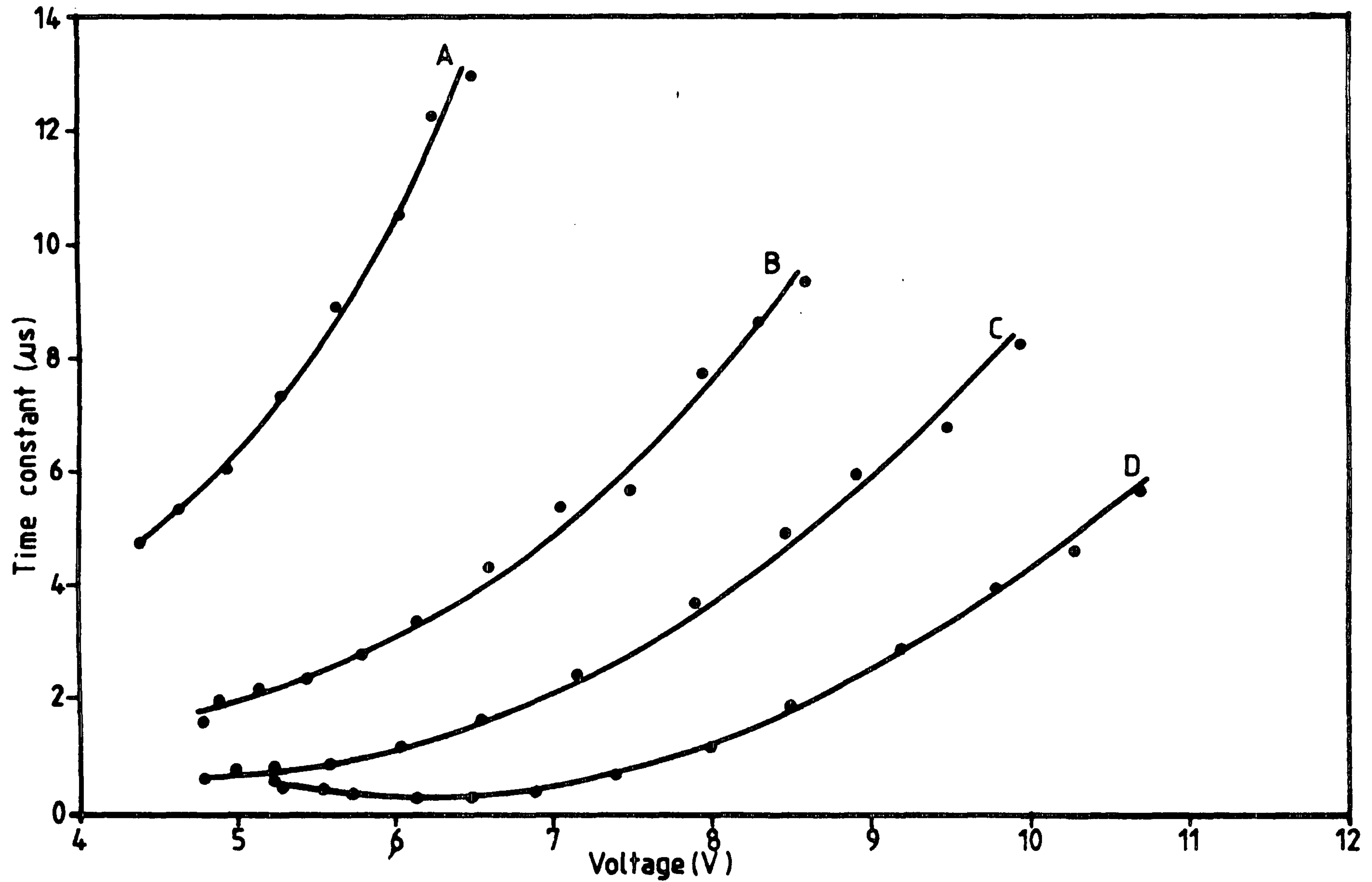


Figure 7.20 Time constant $R_d C_d$ of the MISS (SRO157) with different electrode areas. (A=2.36mm^2, B=1.55mm^2, C=1.12mm^2 and D=0.89mm^2).

7.5.5 Effect of SRO Type on Negative Capacitance

The dependence of the minimum value of the negative capacitance for devices with different SRO type, is summarised in table 7.1. As we can see, the negative capacitance seems to increase as the refractive index of the SRO decreases. This implies that the greater the percentage of oxygen in the SRO the greater is the negative capacitance. For comparison, we can see that a tunnel oxide MISS made by P. Clifton gives a higher negative capacitance value. It was also found that by exposing the SRO layer for a few weeks in the clean room ambient before metallisation produces a device with a higher negative capacitance compared with a device with the same type of SRO but not exposed to air.

Table 7.1: The negative capacitance with different types of SRO

SRO Types	n	d(Å)	Device Area	$-\|C_d\|$
SRO157	2.9	304	0.59mm^2	95pF
SRO123	2.5	275	0.59mm^2	300pF
SRO158	< 1.5	100	0.59mm^2	877pF
Oxide	1.46	–	0.89mm^2	1275pF

7.5.6 Effect of Light Illumination on Negative Capacitance

The MISS device on the sample SRO157 with an electrode area of 0.89mm^2 was used to study the effect of light on the negative capacitance again using the microscope lamp as the light source. Figure 7.21 shows the negative capacitance plots and figure 7.22 the I-V characteristics of the same device under illumination. As the illumination was increased, the negative resistance decreases, and the negative

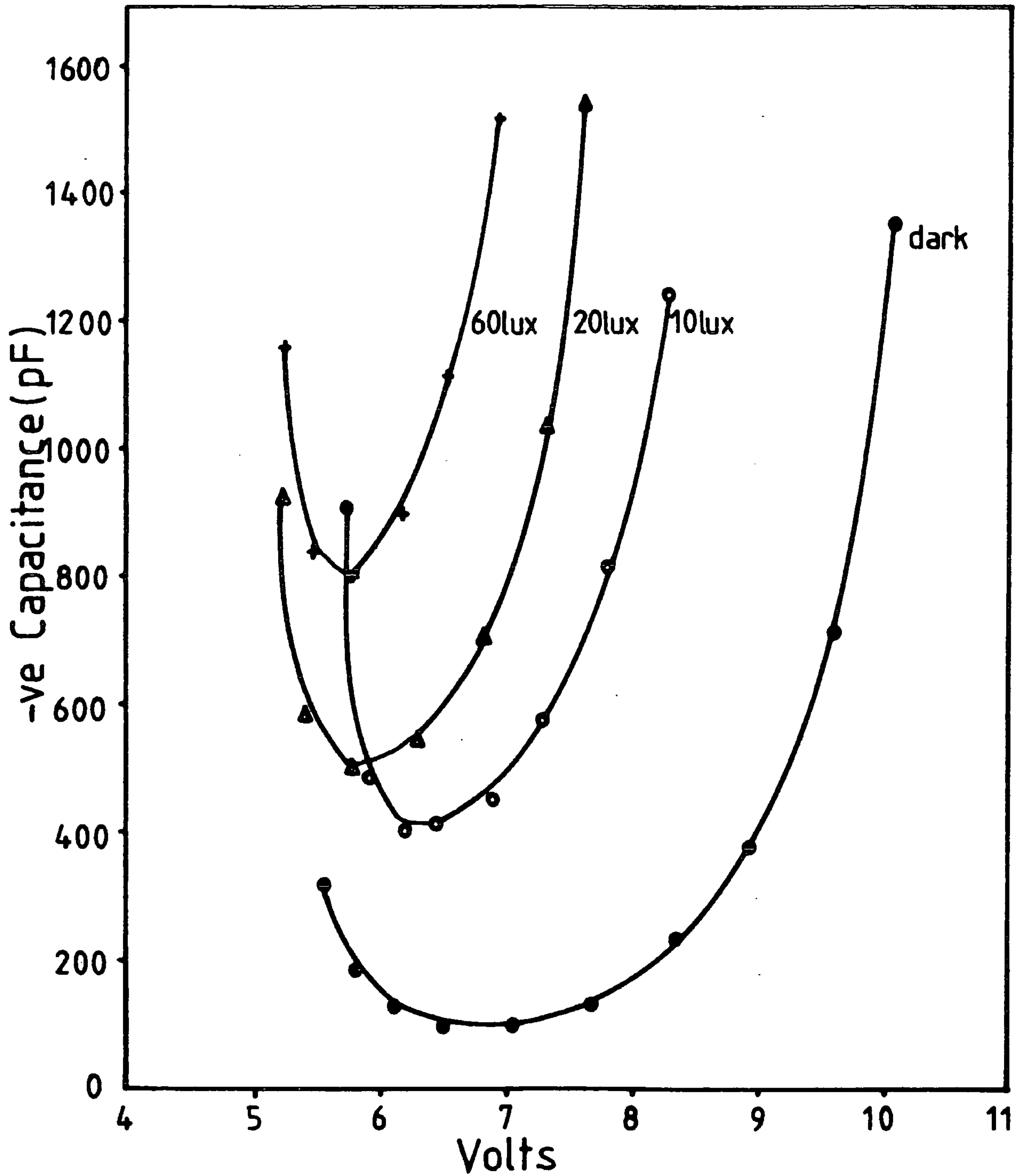


Figure 7.21 The negative capacitance of the MISS (SRO157, A=0.89mm^2) under light illumination.

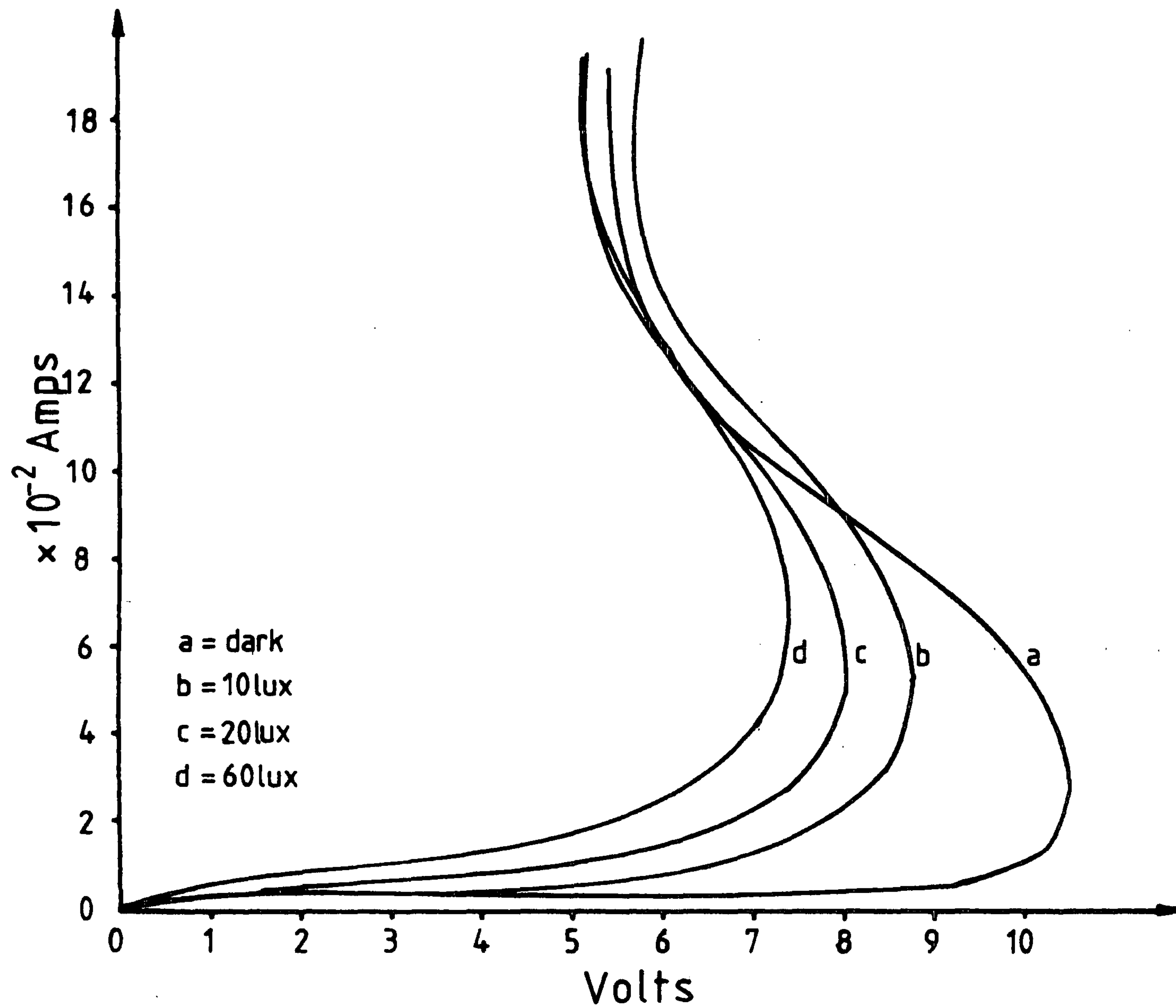


Figure 7.22 The I-V characteristic of MISS (SRO157, A=0.89mm^2) under light illumination.

capacitance at the same applied voltage increases. This is because, the negative capacitance is a function of dI/dV, so that changing the negative resistance also changes the negative capacitance. This effect is very similar to that of electrode area and we have shown that the time constant, $C_d R_d$, increases with area. Therefore, although the magnitude of the negative resistance decreases with light, the time constant increases.

The dependence of capacitance on light illumination can offer an application as a light controlled capacitor. A possible application could be as a tuning capacitor in an oscillator circuit.

7.6 MOS CIRCUIT APPLICATIONS OF NEGATIVE CAPACITANCE MISS DEVICES

7.6.1 Introduction.

Many applications of MISS devices in MOS transistor circuits (MOSMISS) have been proposed [15-17]. However, all of them are concerned with the switching action of the device. Here we are proposing another potential application of MOSMISS in which the stable negative resistance of the MISS is used.

The charging and discharging process in the output stage of an MOS inverter circuit is described in figure 7.23. The speed of the circuit depends on the time taken to charge and discharge the load capacitance. For the MOS inverter circuit, the time constant for charging is determined by the load resistance R_L and load capacitance C_L, and for discharging the time constant is determined by the ON resistance of the MOS transistor and the load capacitance.

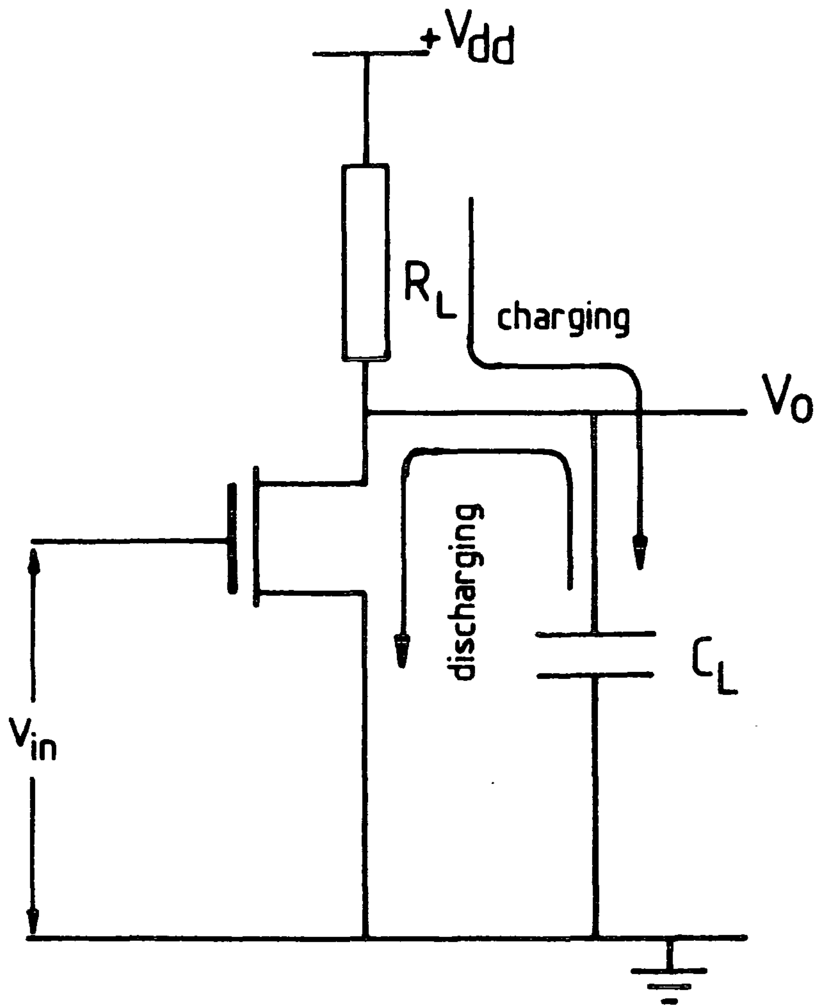


Figure 7.23 Charge flows during charging and discharging in ordinary MOS inverter circuit.

Morant [6] has suggested that the negative capacitance of the MISS can be used to reduce the total load capacitance in the MOS circuit so that the time constant can be reduced, hence increasing the speed of operation of the circuit. This can be implemented by using the MISS device as an active load to form an MOS inverter or buffer circuit. Whether or not the combination of the MOS and the MISS will behave like inverter or buffer, depends on the magnitude of the negative resistance and the circuit configuration.

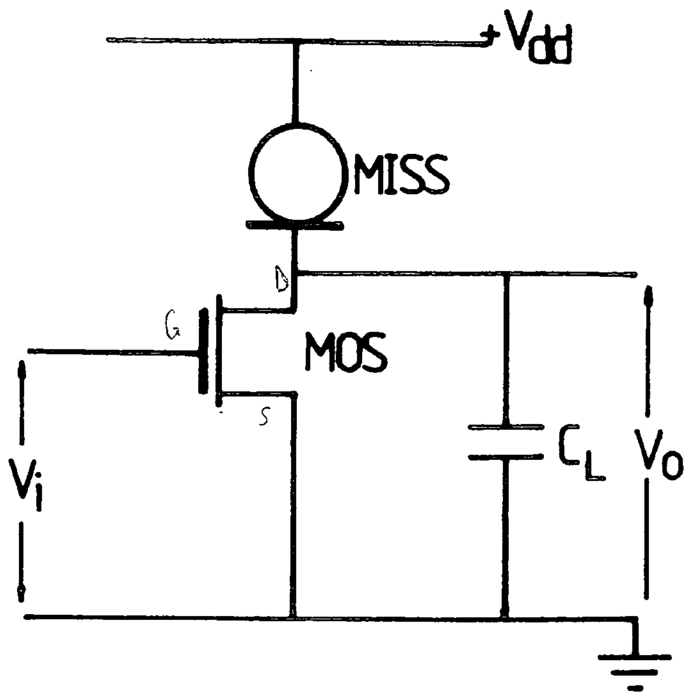
7.6.2 Negative Resistance Load Line.

There are two ways in which the MISS device can be connected as an active load in the MOS transistor circuit.

7.6.2.1 MOSMISS Common Source Configuration

In this configuration, the MISS device is placed between the drain and the supply line, V_{dd}, as shown in figure 7.24(a). The negative resistance load line in the output characteristics of the MOS is shown in figure 7.25(a). Figure 7.25(b) shows the transfer characteristics of this circuit configuration which was derived from figure 7.25(a). If the range of input voltage from zero to the switching voltage the output will be inverted, and this corresponds to the OFF state of the MISS. If the input voltage is in between the switching voltage and the holding voltage of the MISS, the circuit behaves like an amplifier, but for the MISS this region is a negative resistance region also has a negative capacitance. The third region in the transfer characteristic is the ON state of the MISS where the output voltage remains constant with increasing input voltage.

Now let us consider the effect of the negative capacitance on the total load capacitance. As shown in the small signal equivalent circuit figure 7.24(b) the total



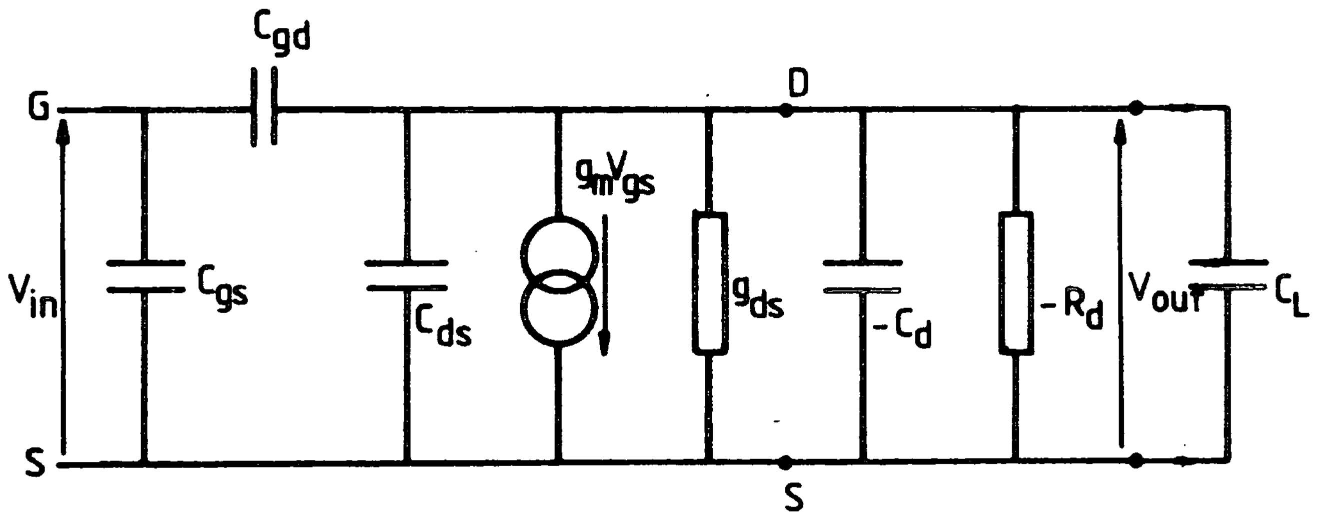


Figure 7.24 a) MOSMISS common source configuration,
b) Small-signal model of circuit (a).

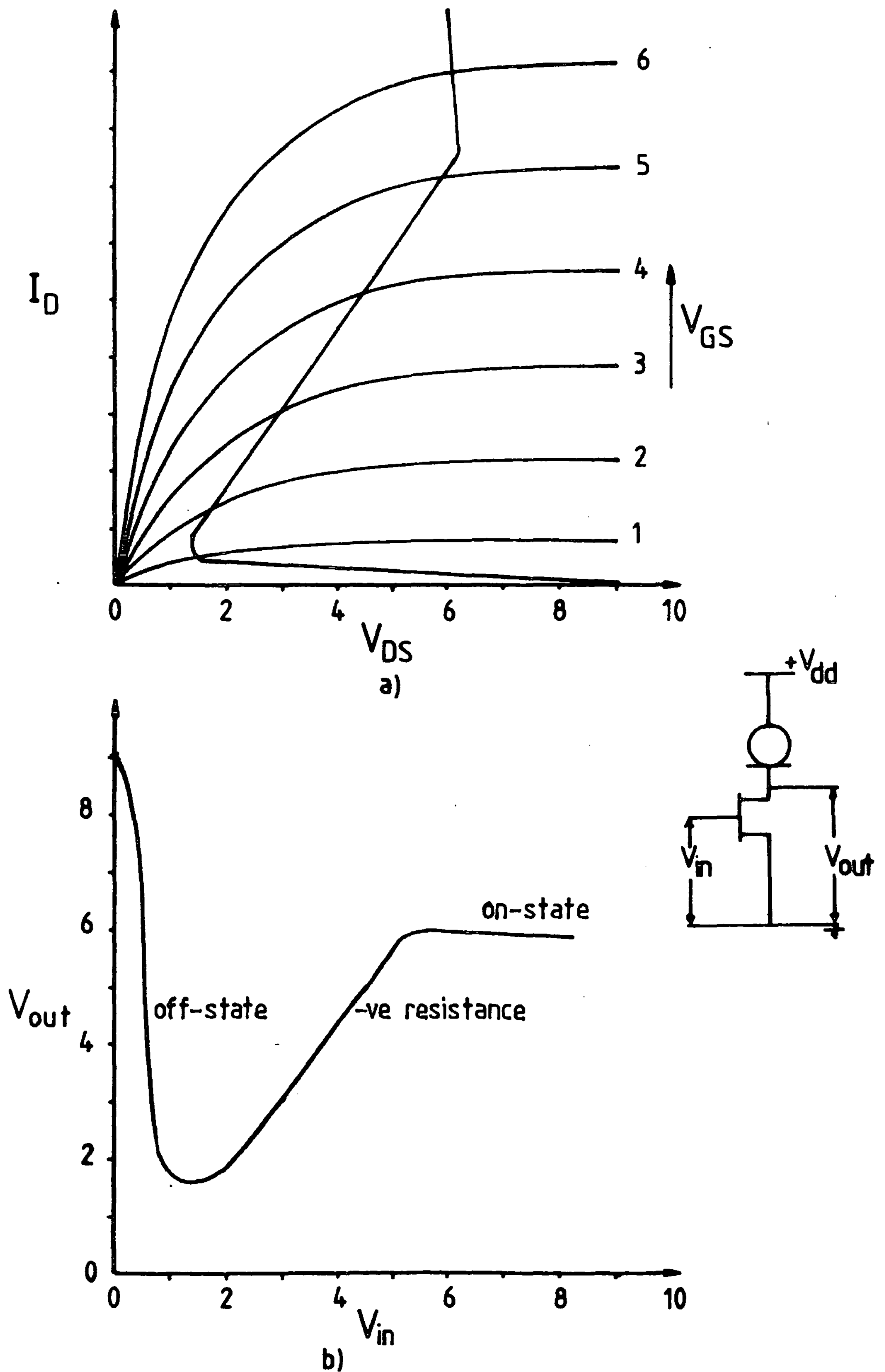


Figure 7.25 a) Output characteristic of MOST with MISS characteristic load line.

b) Transfer characteristic of MOSMISS common source configuration derived from (a).

capacitance C_T is approximately the sum of the load capacitance C_L and the negative capacitance $-|C_d|$, as the source-drain capacitance of the MOST is very small.

$$C_T = -|C_d| + C_L \tag{7.12}$$

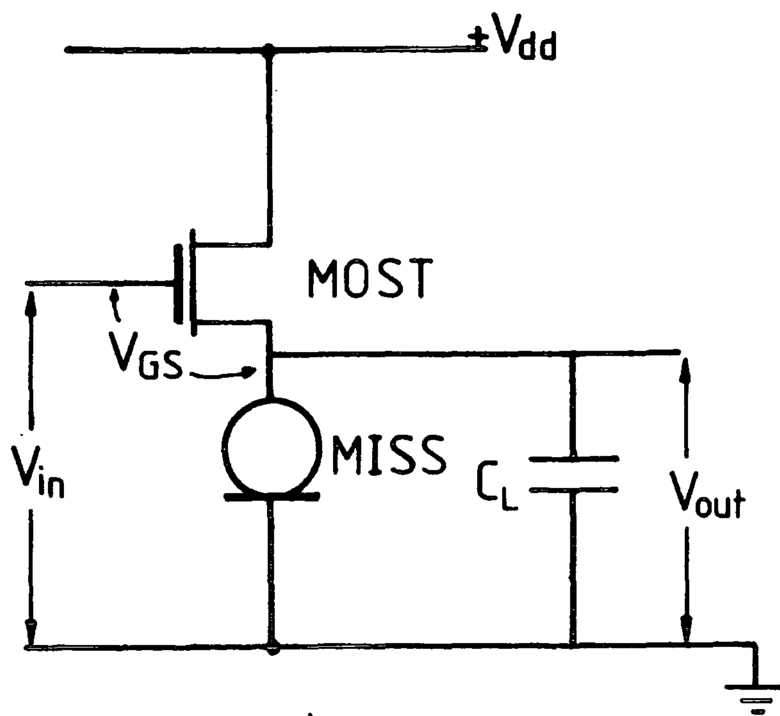
It is clear that, in order to keep the value of C_T negative, C_L must be smaller than $|C_d|$. The disadvantage of this configuration is that it does not exhibit an inverter characteristic which is neccesary in logic circuit applications.

7.6.2.2 MOSMISS Common Drain Configuration

Figure 7.26(a) shows a circuit configuration where MISS device is used as a load in common drain. The output voltage of this circuit is the voltage across the MISS. The transfer characteristics of the circuit are shown in figure 7.27(a) and 7.27(b) for different relative values of the negative resistance and the transistor characteristics. The transfer characteristic of figure 7.27(b) is more useful than that in figure 7.27(a) because it is an inverter when the input level is above the switching voltage of the MISS. Since the negative capacitance of the MISS is in parallel with the load capacitance as shown in figure 7.26(b), the total capacitance will be reduced to $(C_L - |C_d|)$ again. As a result, the transition time of the output voltage is reduced so that the operating speed of the circuit has been increased.

7.6.3 Graphical Analysis of a Negative Resistance Load Line

Whether or not the common drain configuration of the MOSMISS circuit will behave like an inverter depends on the magnitude of the negative resistance and the I-V characteristics of the MOS transistor. By graphical analysis this condition can be easily understood. From figure 7.26(a),



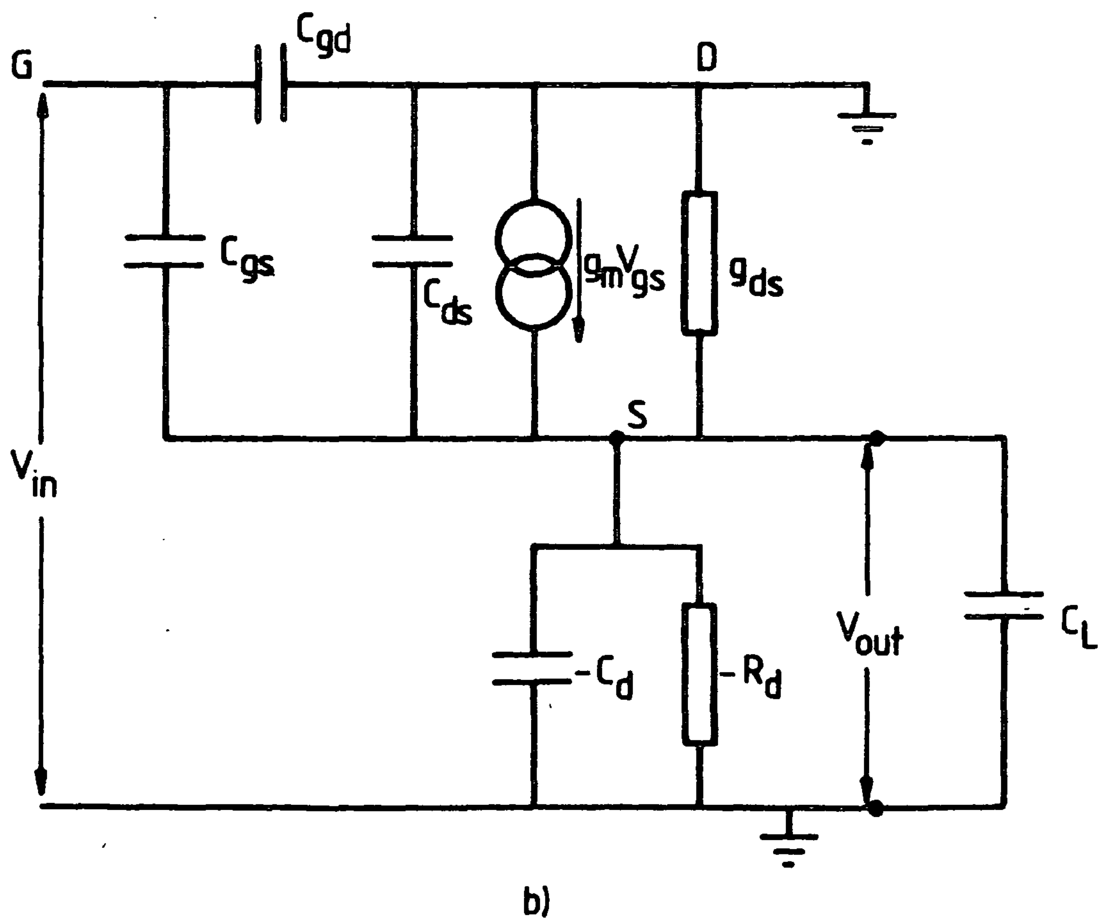
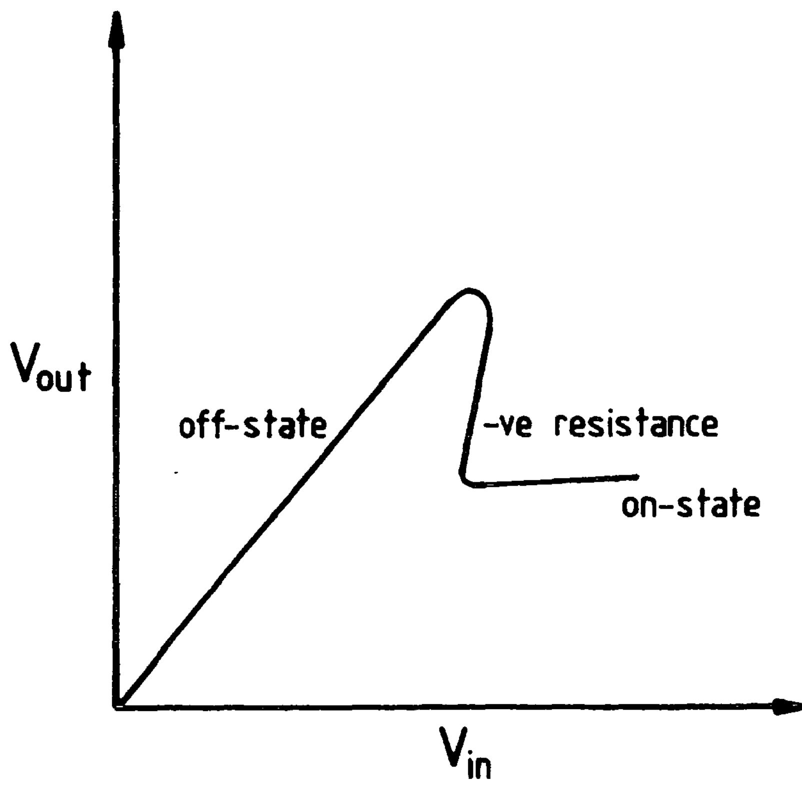


Figure 7.26 a) MOSMISS common drain configuration.
b) Small-signal model of circuit (a).



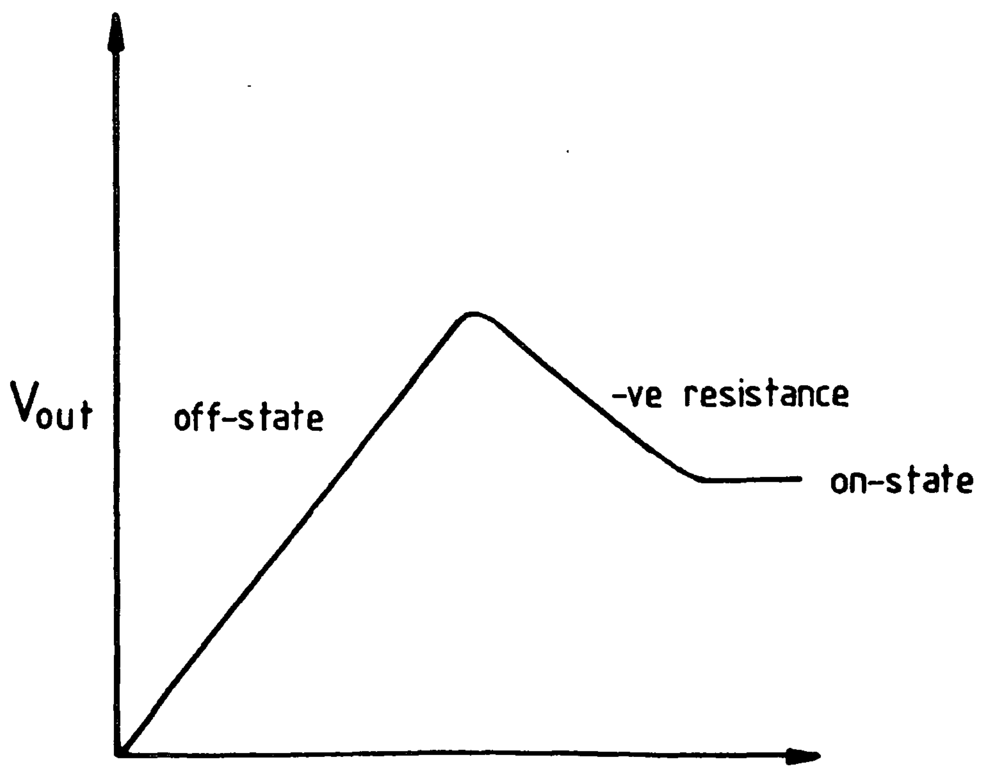


Figure 7.27 Transfer characteristic of the MOSMISS common drain circuit, **a)** non-inverting and **b)** inverting charateristics.

$$V_{in} = V_{MISS} + V_{GS} \quad 7.13$$

in general. For two values of input voltage the operating point will be determined as in figure 7.28(a), giving

$$V_{in_2} = V_{MISS_2} + V_{GS_2} \quad 7.14$$

and

$$V_{in_4} = V_{MISS_4} + V_{GS_4} \quad 7.15$$

Figure 7.28(b) shows that a transfer characteristic having a positive slope derived from figure 7.28(a). For an inverter the transfer curve must have a negative slope as shown in figure 7.28(c). The condition for this is,

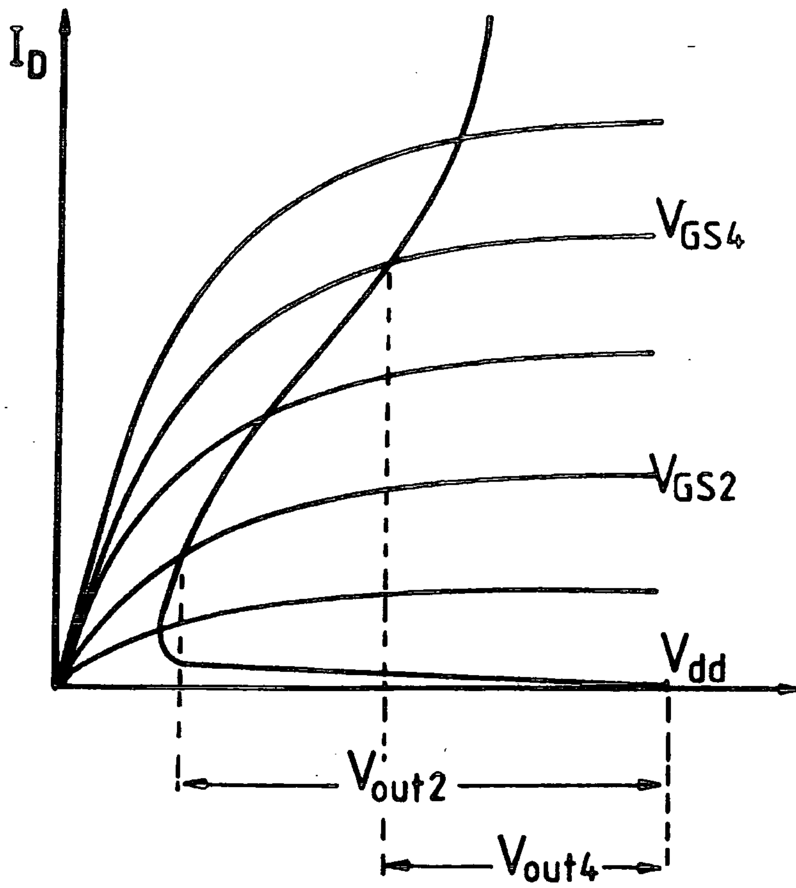
$$(V_{MISS_4} + V_{GS_4}) > (V_{MISS_2} + V_{GS_2}) \quad 7.16$$

$$(V_{GS_4} - V_{GS_2}) > (V_{MISS_2} - V_{MISS_4}) \quad 7.17$$

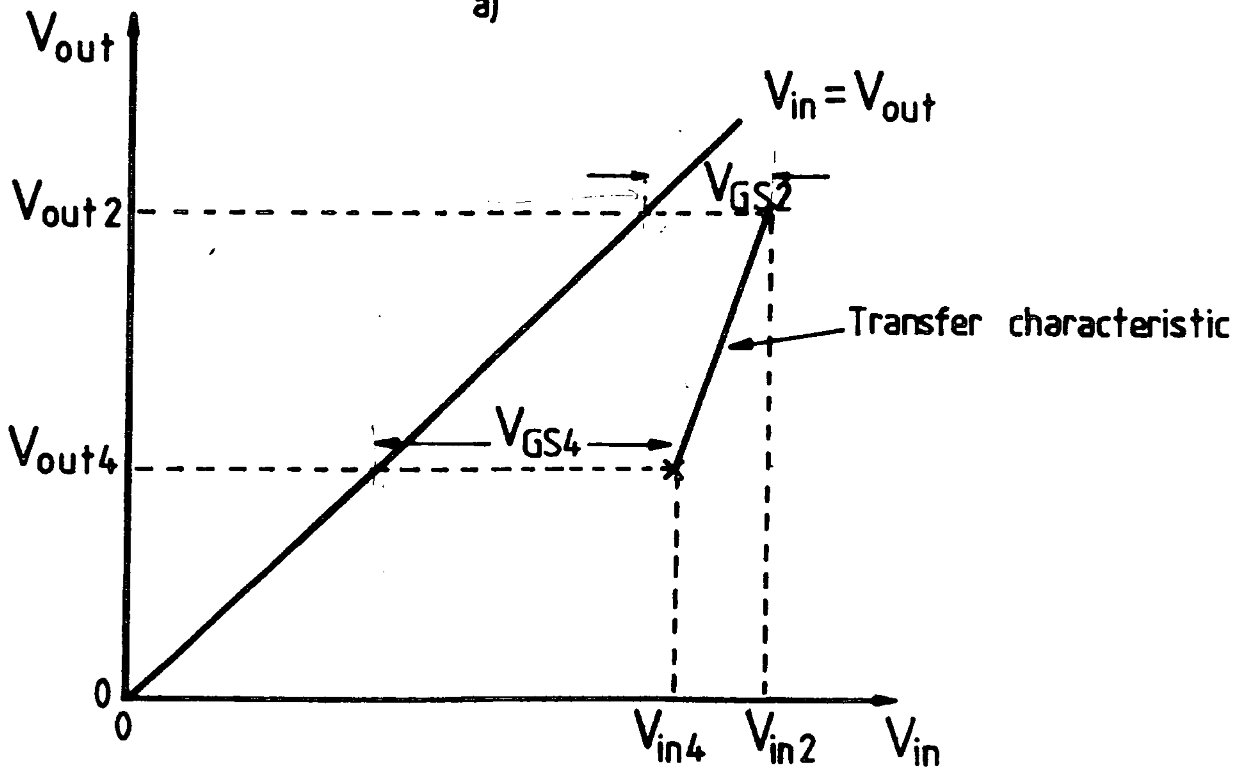
or

$$\Delta V_{GS} > \Delta V_{MISS} \quad 7.18$$

i.e. the negative resistance has to be small.



a)



b)

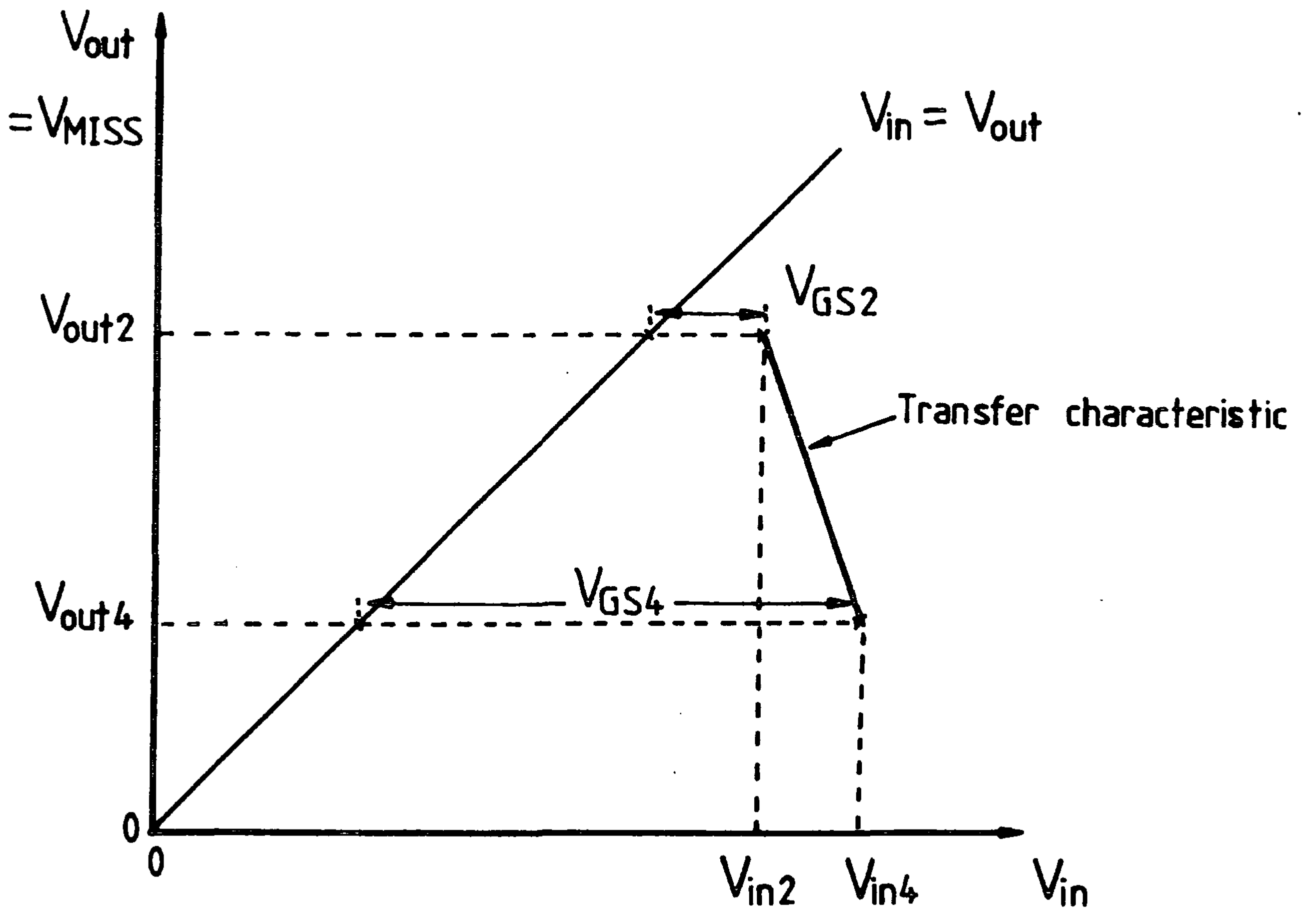


Figure 7.28 a) MOST characteristic with the MISS characteristic load line for the circuit of figure **7.26(a)**.

b) Transfer characteristic for (a) with $\Delta V_{GS} < \Delta V_{MISS}$, and c) Transfer characteristic for (a) with $\Delta V_{GS} > \Delta V_{MISS}$.

7.6.4 Results and Discussion

The MISS device on sample SRO158 was used in this experiment on the inverter circuit because it has a low magnitude of its negative resistance and a low switching current. The I-V characteristics of the MISS required a MOS transistor with the gain parameter, β, of $75\mu A/V^2$, and for this purpose a device on a test chip designed by M. J. Morant in the School of Engineering and Applied Science, Durham, was used. The current-voltage characteristics of the transistor are shown in figure 7.29. The transistor together with the MISS device were placed in the measurement box where they were connected to form a common drain circuit.

The transfer characteristic of the MOSMISS inverter circuit is shown in figure 7.30 for a MISS size of 0.89 mm^2. Since the inverter part of the characteristic begins at an input voltage of 13.0 volts, which is the switching voltage of the MISS, the lower (d.c.) level of the input signal must be greater than this. For this purpose, a Philips Type PM5716 pulse generator was used enabling the lower and upper levels of the input signal to be adjusted anywhere in the range of ± 20 volts. It was set to levels of 13.5 V and 17.5 V here. Figure 7.31 shows the input and output waveforms of the inverter for load capacitances of 330pF, 660pF, and 1000pF. Since the load capacitance is in parallel with the negative capacitance, increasing load capacitance reduces the total output capacitance, and hences it reduces the time constant.

The transition from high to low in the output voltage of the inverter corresponds to a shift of the operating point from the switching voltage towards the holding voltage and vice-versa for the voltage transition from low to high level. As we can see from figure 7.31 both the fall-time and rise-time decrease when the load capacitance is increased, but the fall-time, which is smaller in every case, is more sensitive. The

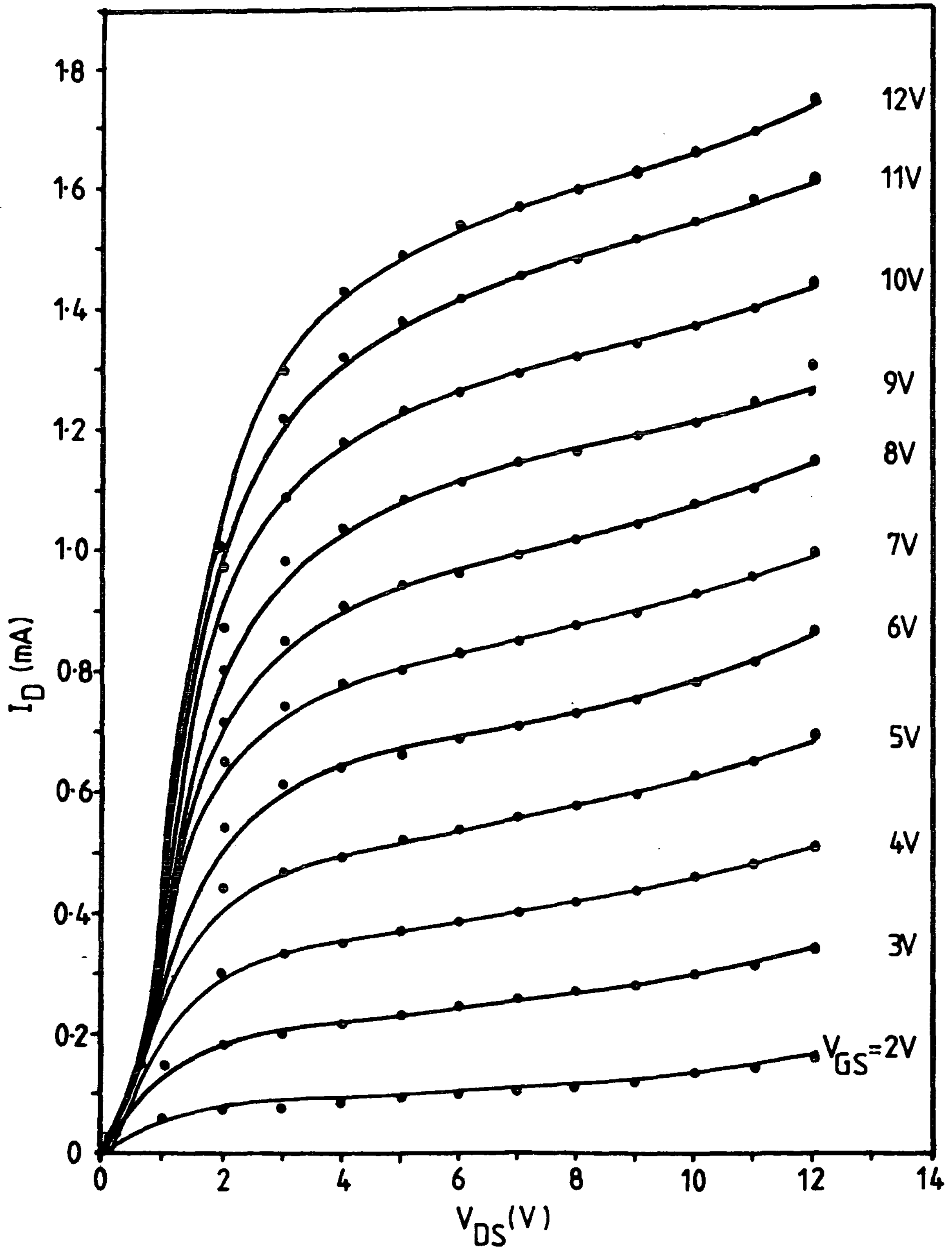


Figure 7.29 Output characteristic of the MOS transistor with $\beta = 75\mu A/V^2$.

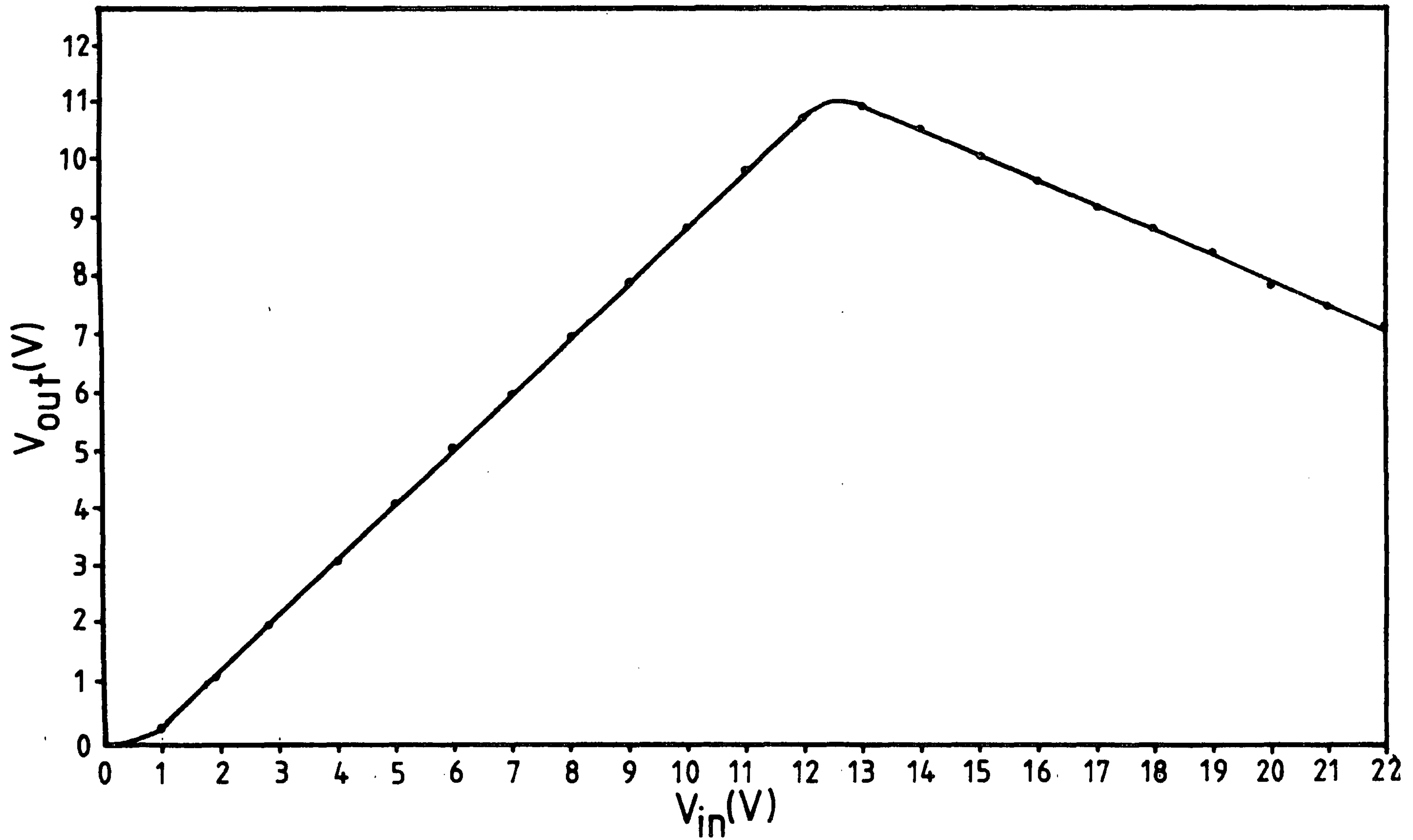


Figure 7.30 Transfer characteristic of the MOSMISS inverter circuit using SRO-MISS from sample SRO158 with electrode area of $0.89mm^2$.

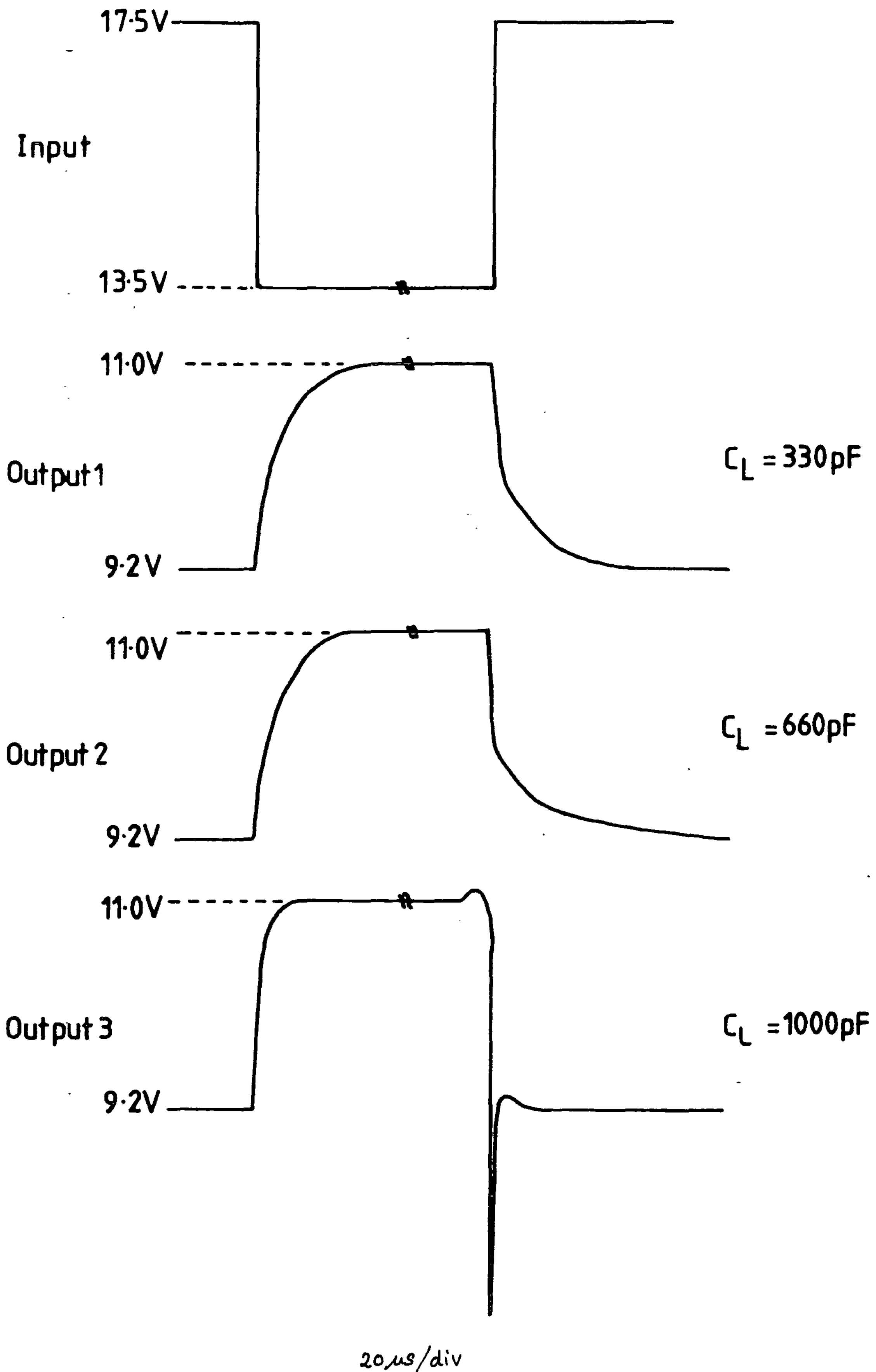


Figure 7.31 Input and output waveforms of the MOSMISS inverter circuit showing the effect of load capacitance.

difference in fall and rise-times occurs because of the nonlinearities of the negative capacitance and negative resistance. The transition from low to high in the output voltage it is accompanied by an increase in device negative capacitance. On the other hand, the negative capacitance decreases as the voltage moves from high to low levels. As a consequence, the effective negative capacitance $(C_L - |C_d|)$ decreases during the voltage transition from low to high and increases during the opposite transition. This gives rise to a decrease in the time constant for low to high transition and an increase during high to low transition.

As the effective capacitance becomes close to zero, the response in the high to low transition is very rapid resulting in overshoot and a damped oscillation as shown in figure 7.31. The negative spike could also be due to charge storage in the MISS. If the external capacitance is increased further, so that the total capacitance becomes positive, a modulated oscillation can be observed at the output, with two different frequencies similar to that in the frequency shift keying (FSK) output.

Figure 7.32 shows the plot of the time constant against the external capacitance, showing that the time constant decreases as the capacitance increases. The time constant decreases as the total negative capacitance, given by $(-|C_d|+C_L)$, decreases.

The variation of the rise-time and the fall-time with the external capacitance at an input level of 12V are shown in figure 7.33 and 7.34 respectively. Figure 7.35 and 7.36 show that both the rise-time and the fall-time of the MOSMISS inverter decrease when the input d.c. level was increased. Since $V_{in} = V_{GS} + V_{MISS}$, increasing V_{in} will increase V_{GS}, pushing the operating point towards the holding voltage where the negative capacitance is higher. Therefore, as the input d.c. level increases the effective negative capacitance $(C_L - |C_d|)$ decreases and reduces the time constant. However, the decrease in the time constant is followed by the a decrease in the amplitude of the output voltage swing as shown in figure 7.37. This is because the output swing is

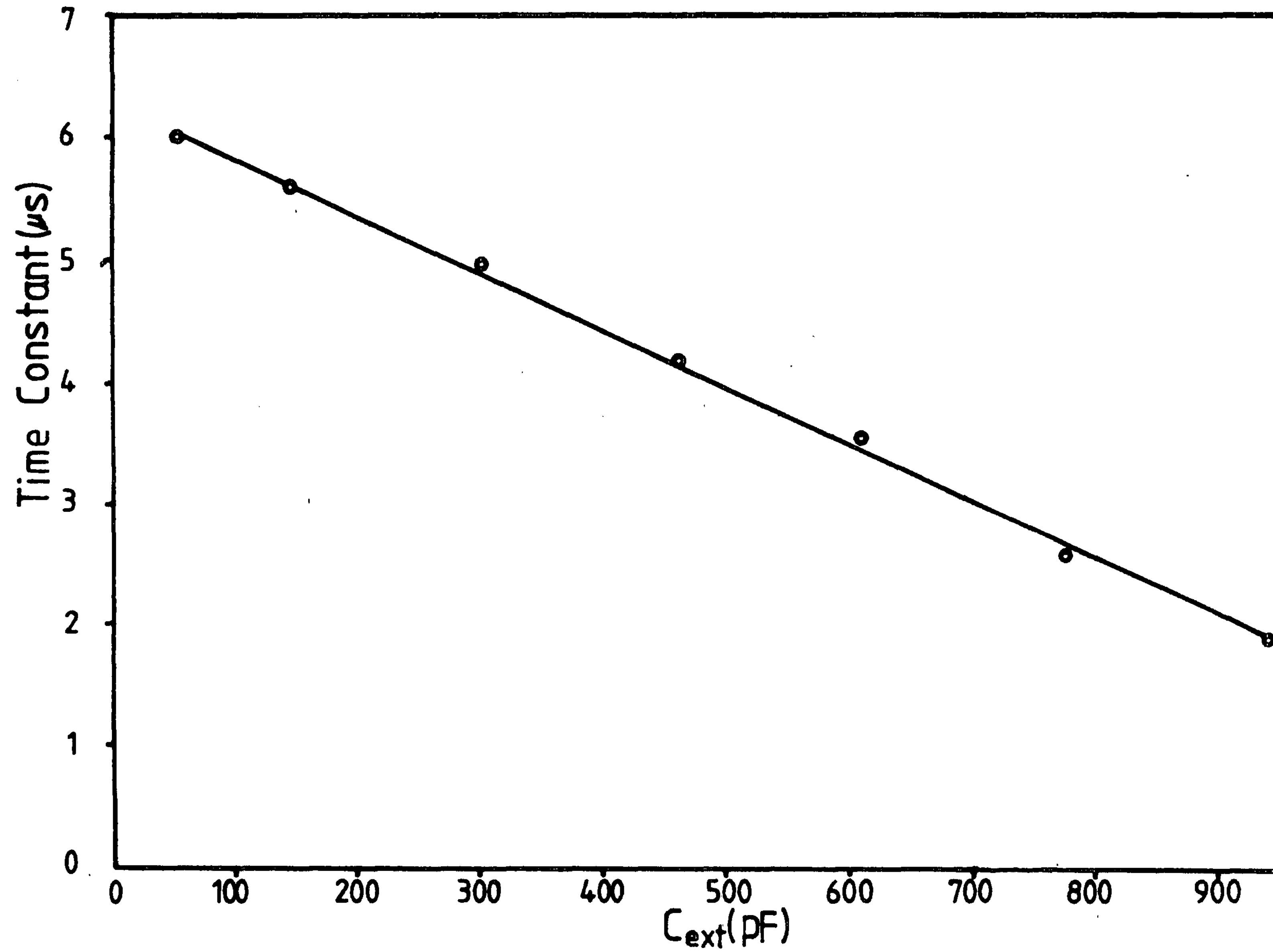


Figure 7.32 Time constant as a function of external capacitance.

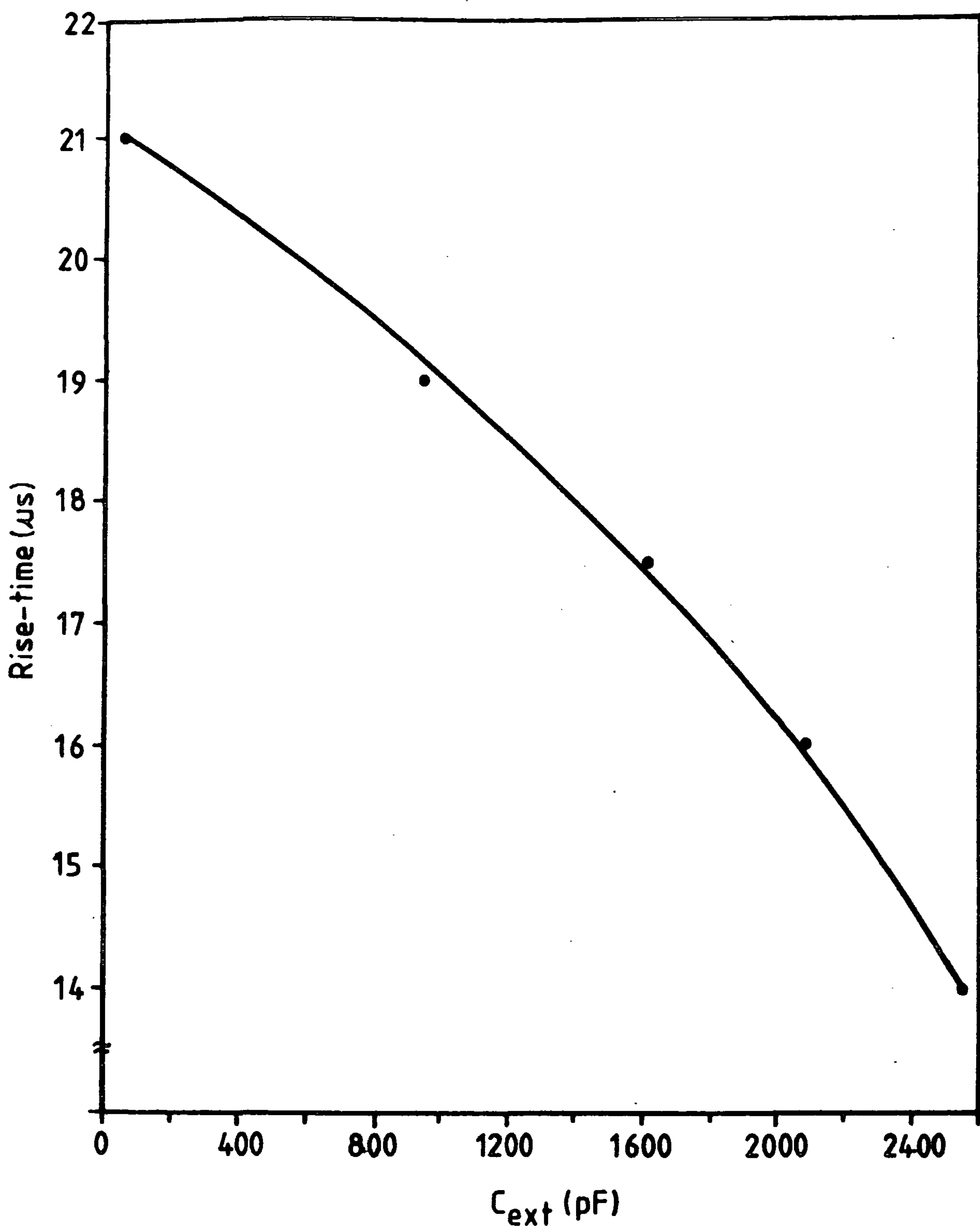


Figure 7.33 Variation of rise-time with external capacitance at input d.c. level 12V.

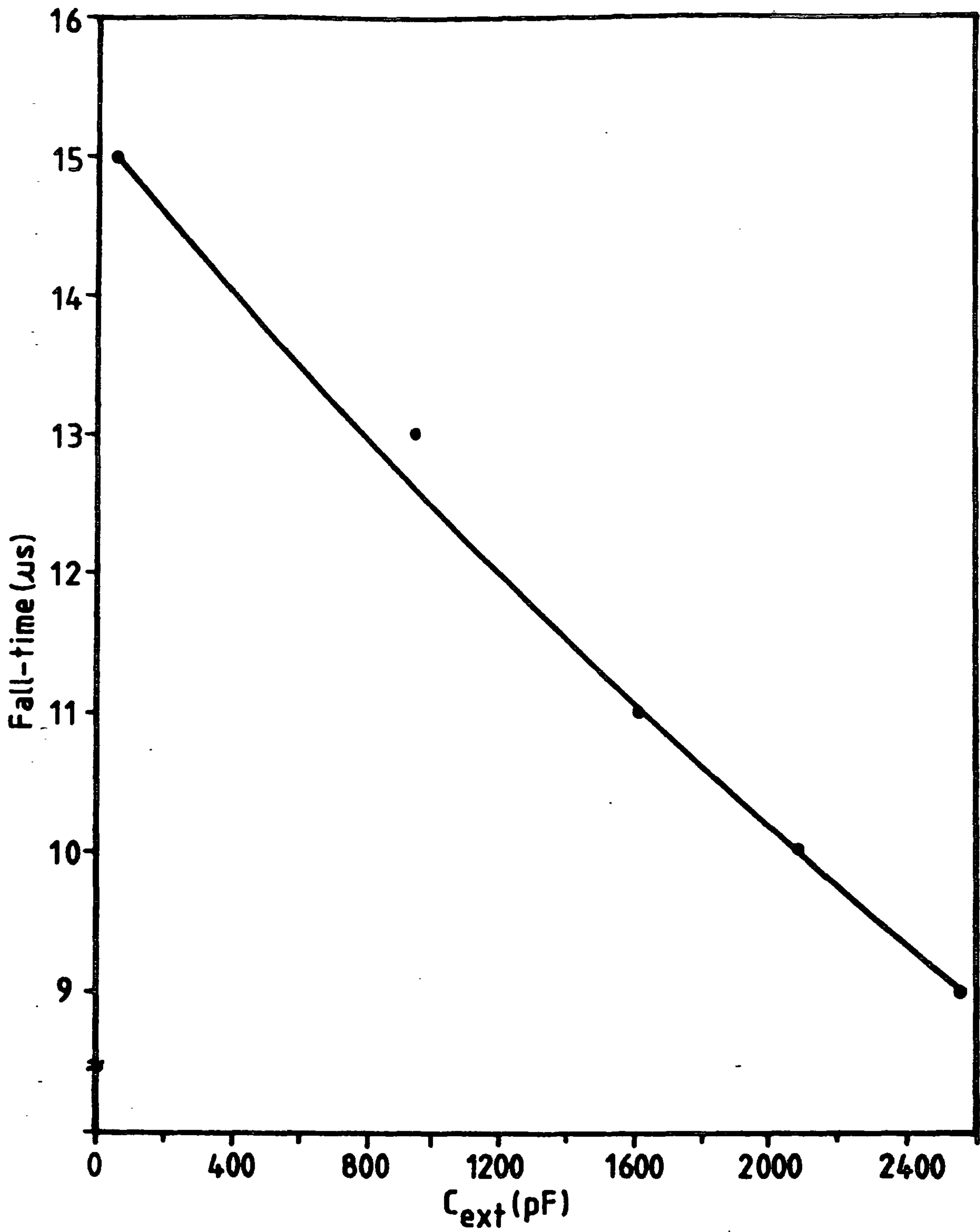


Figure 7.34 Variation of fall-time with external capacitance at input d.c. level 12V.

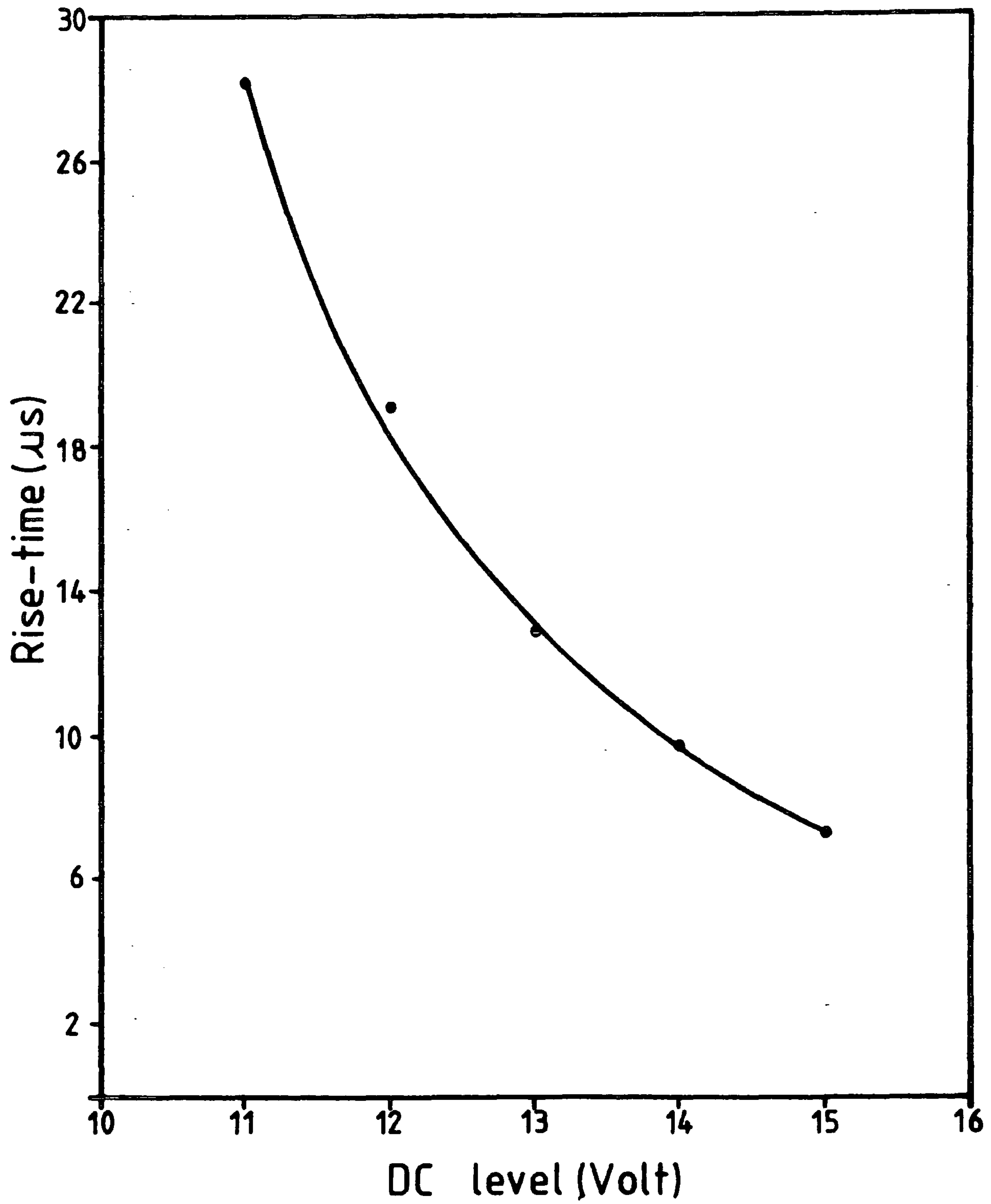


Figure 7.35 Variation of rise-time with input d.c. level.

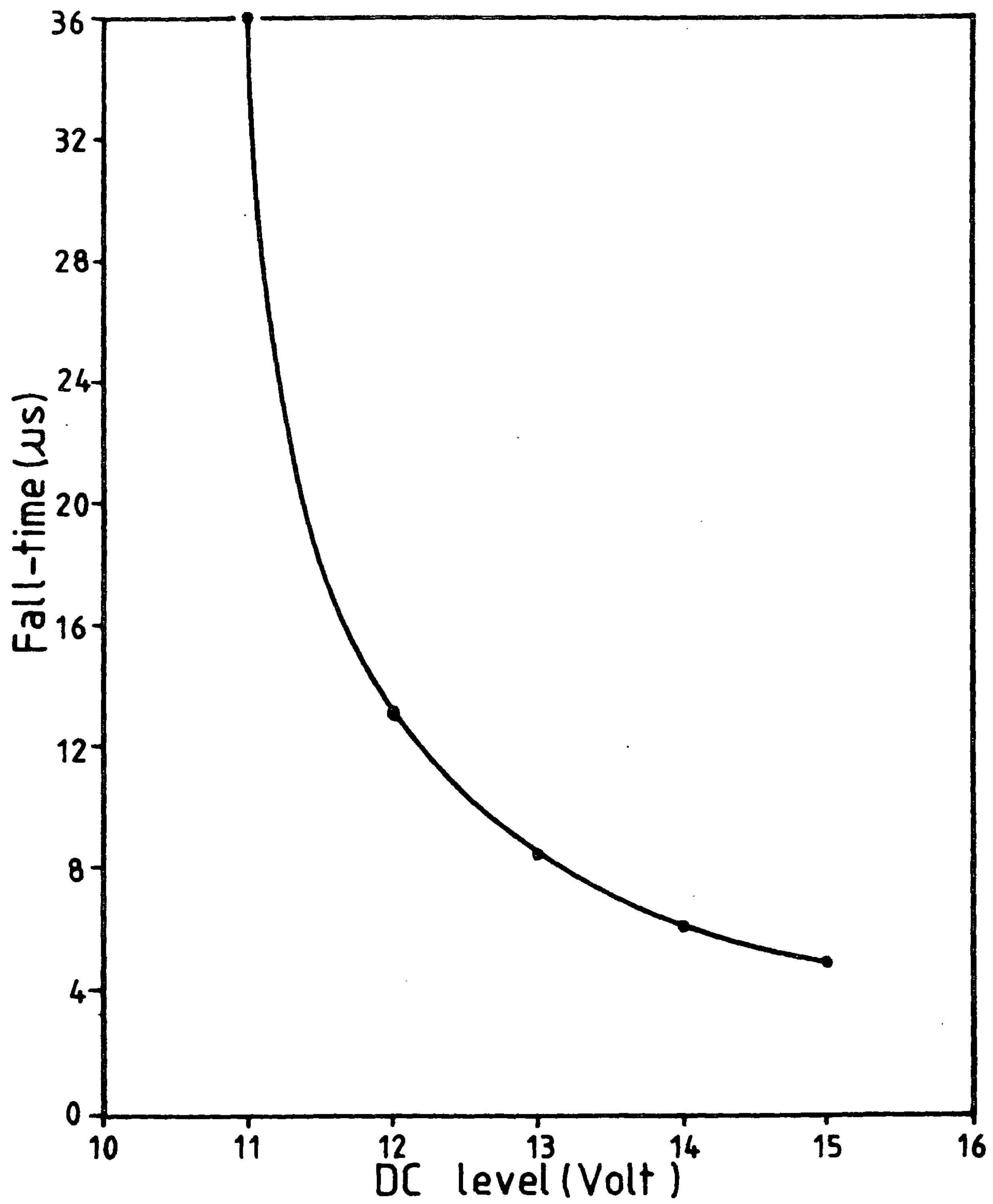


Figure 7.36 Variation of fall-time with input d.c. level.

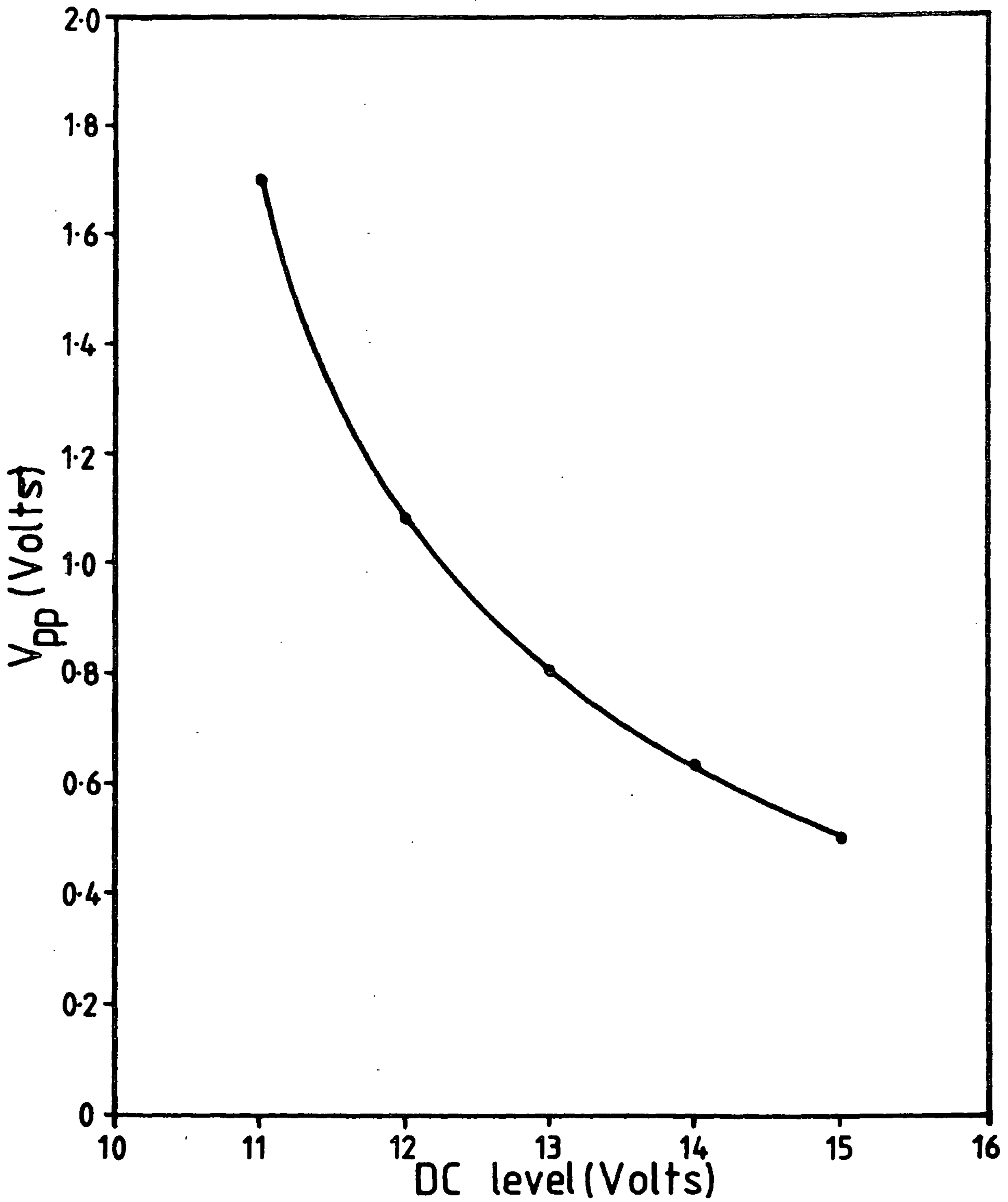


Figure 7.37 Variation of an output voltage, V_{pp}, of the MOSMISS inverter circuit with input d.c. level.

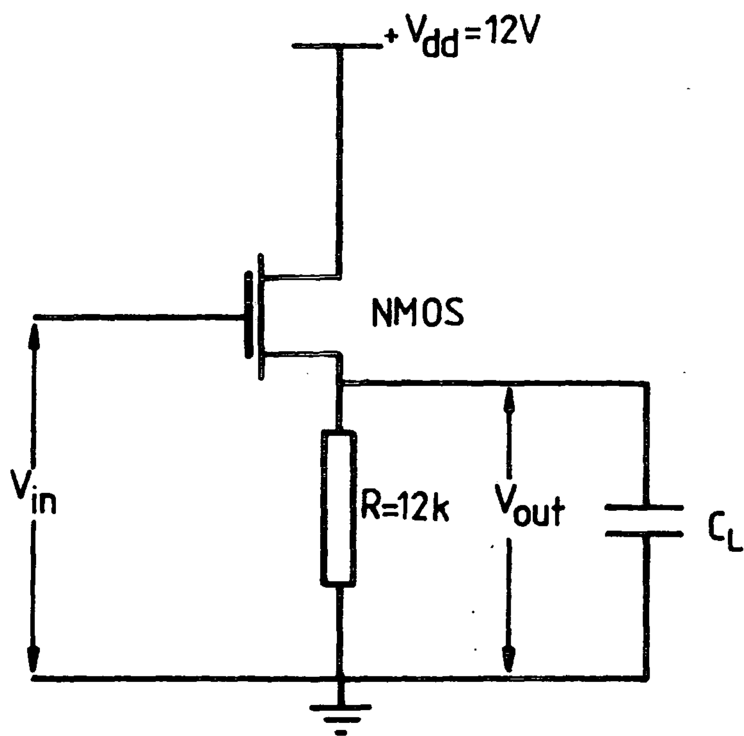


Figure 7.38 MOS emitter follower circuit.

limited by the holding voltage of the MISS. For these particular circuit components a very fast negative capacitance inverter can therefore be made if a low voltage swing is acceptable.

For the purpose of comparison, the rise-time and fall-times in the emitter follower circuit shown in figure 7.38 were measured with the emitter resistance chosen so that the current flow in the circuit was comparable with that in the MOSMISS inverter circuit. The rise-time and fall-time with a load capacitance of 1000pF were $10\mu s$ and $40\mu s$ respectively. For the MOSMISS inverter circuit the rise-time and the fall-time are 12μs and 0.4μs respectively. As we can see, the fall-time is 100 times smaller than that in ordinary emitter follower circuit, however, the rise-time is slightly greater.

7.7 SUMMARY

A general review of a negative resistance was given in the first section followed by a discussion of the stability of the negative resistance circuit. The circuit analysis has been carried out and it shows that a stable negative resistance only exists if the device capacitance is also negative. The stable negative resistance can be realized in practice by minimizing the circuit stray capacitances. An intermediate state, which was believed to exist in some MISS devices, has been proved to be false and its existence is not a device phenomenon but is due to the effect of circuit oscillation. A new technique has been introduced to measure the negative capacitance of the MISS.

It was found that the negative capacitance is a function of dI/dV in the negative resistance region. Its value is therefore voltage dependent and it has a minimum magnitude somewhere between the switching and holding voltages. The negative capacitance are not propotional to electrode area due do the two dimentional effect.

Since the negative capacitance is dependent on the slope of the negative resistance region, the conduction of the SRO films become very important in determining the magnitude of the negative capacitance. A less conductive film is found to produce a higher negative capacitance. However, this is accompanied with a reduction in the switching voltage. It was also found that the negative capacitance is very sensitive to light illumination, and it increases as the illumination was increased. All of these characteristics are strongly related to the changes in the current-voltage characteristics in the negative resistance region.

In the last section it has been shown that negative capacitance can be used to reduce the total capacitance in an MOS circuit and therefore it can be used to reduce the charging and discharging time of an inverter. However, due the nonlinearity of the negative capacitance, the charging and the discharging times are different and the charging time is higher than the discharging time. The time constants can be minimized if a suitable bias and a small input signal are used.

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CHAPTER EIGHT

CONCLUSION AND SUGGESTIONS FOR FURTHER WORK

8.1 SUMMARY OF RESULTS

The purpose of the work presented in this thesis was to study and explore the electrical behaviour of a new type of MISS device in a comprehensive way. The semi-insulating material used for the present device was SRO deposited using an APCVD reactor at a temperature of 650^oC. The phase ratio of the reactant gases, R_o was, varied from 0.09 to 0.25 and the deposition time from 0.6 to 2 minute. The SRO layer thickness was in the range of 100 to $500\AA$. The uniformity of the film in this range of thickness is far more easy to control compared to that of the tunnel oxide with a thickness of the order of 20 to $50\AA$. Therefore this material could be an alternative semi-insulating film for the MISS device in future. Another advantage of the SRO over the tunnel oxide for the MISS is that its conductivity can be controlled by changing the composition of the film.

The switching parameters of the MISS device were found to be very dependent on various parameters such as device geometry, SRO thickness, electrode metal, gold doping etc. The first two parameters are the most important in determining whether or not the device switches. We have found that the geometrical or two dimensional effect is due to the current spreading in the structure. The spreading effect was investigated by performing experiments on the effect of electrode area, junction area, electrode perimeter and guard ring voltage. All the results from these experiments

have shown the same trend which is that the switching voltage increases with the spreading area which in turn is increased by the electrode perimeter being increased. Increasing the SRO deposition time from 1 to 2 minutes with the gas phase ratio of 0.2 increased all the switching parameters except the holding current. Other effects such as a gold doping, heat treatment, work function difference and film ageing have also been explored. The switching voltage was found to decrease and the holding voltage increase if the sample is doped with gold. Heat treating the samples was found to decrease all the switching parameters. The gold electrode devices have shown quite a significant increase in the holding voltage. Finally, the switching voltage decreases if the SRO is exposed to air for long periods of time.

In dynamic operation the charge stored during the ON state of the MISS, delays the switching off process. A double pulse experiment was used to study the effect of heat treatment and gold doping on the dynamic operation. It was found that after heat treating the device at $400°C$ the switching characteristics are changed possibly due to the presence of electron traps at the interface. The gold doping was found to substantially reduce the effect of charge storage and it reduced the switching off time. However, the presence of gold atoms in the device also reduces the switching voltage. Another interesting phenomenon was also observed in the double pulse measurements. If a pulse swing from a negative to a positive level is applied to a device which does not contain traps, a similar effect is observed to that for the device containing an electron traps.

In the three terminal MISS, the switching characteristics become controllable and similar to those of a thyristor but with a stable negative resistance. Two types of three terminal MISS were made, controlled by majority and minority carrier injection respectively. The former is more sensitive to the base current than the latter. The control efficiency was found to increase with the emitter area. With the opposite

bias, the device exhibits a transistor-like characteristic with a small gain of between 1 and 3. A new phenomenon has been observed for the first time in which an N-type negative resistance is exhibited for base currents of greater than zero if the epilayer is very thin.

The most interesting and novel feature of the MISS device is the negative resistance region. Prior to the present work this region had been found to be stable. The stability of the negative resistance in the measurement circuit is shown to be due to the negative capacitance of the device. An intermediate state which was present in some MISS devices has been shown to be due to circuit oscillation that occurs when the total circuit capacitance is positive and the load resistance is greater than the magnitude of the negative resistance. The magnitude of the negative capacitance was found to be dependent on voltage within the negative resistance region. It has a minimum value somewhere between the switching and holding voltages. On the other hand the magnitude of the negative resistance has a maximum at about the same voltage as the minimum of the negative capacitance. The magnitude of the negative capacitance depends on the slope of the negative resistance region which is determined by the switching and holding points. Arcordingly, all parameters which governed the switching and holding points of the device, such as geometrical shape and size, SRO type, electrode metal etc, also affect the negative capacitance. It was also shown that light illumination increased the negative capacitance at a constant voltage.

The important feature of the negative capacitance of the MISS is its ability to cancel a positive capacitance in a circuit. This gives rise to possible applications in which the load capacitance of a digital integrated circuit can be reduced, so increasing the switching speed. This can be implemented with an MOS transistor in the form of an inverter circuit in which the MISS is used as an active load.

8.2 SUGGESTIONS FOR FURTHER WORK

Almost all the characteristics of the MISS device have been explored in this work. Due to a limited time available, the detailed investigation of most of the device characteristics has not been attempted. Therefore there are plenty of ways in which this work could be extended in future. Suggestion for future work are given in the following section.

SRO Conduction

The conduction property of the film used to make the device is very important to SRO-MISS operation and it needs to be understood. The conduction mechanism was not of particular interest in the present investigation but a thorough study of the conduction mechanism in the type SRO films which were used for the MISS should be carried out in future work. An effort should be made to improve the quality of the SRO films, and this includes modifying the present APCVD reactor so that good flow dynamics and a stable temperature can be obtained, and hence improved reproducibility. The conduction study can be carried out by performing I-V measurements on SRO-MIS structures with a constant thickness but different composition and vice versa. The effect of annealing can also be investigated. The MIS can be fabricated using different size electrodes and using n and p type substrates so that the effect of current spreading can also be investigated. A temperature study must also be performed so that the conduction model can be verified.

Switching Characteristics

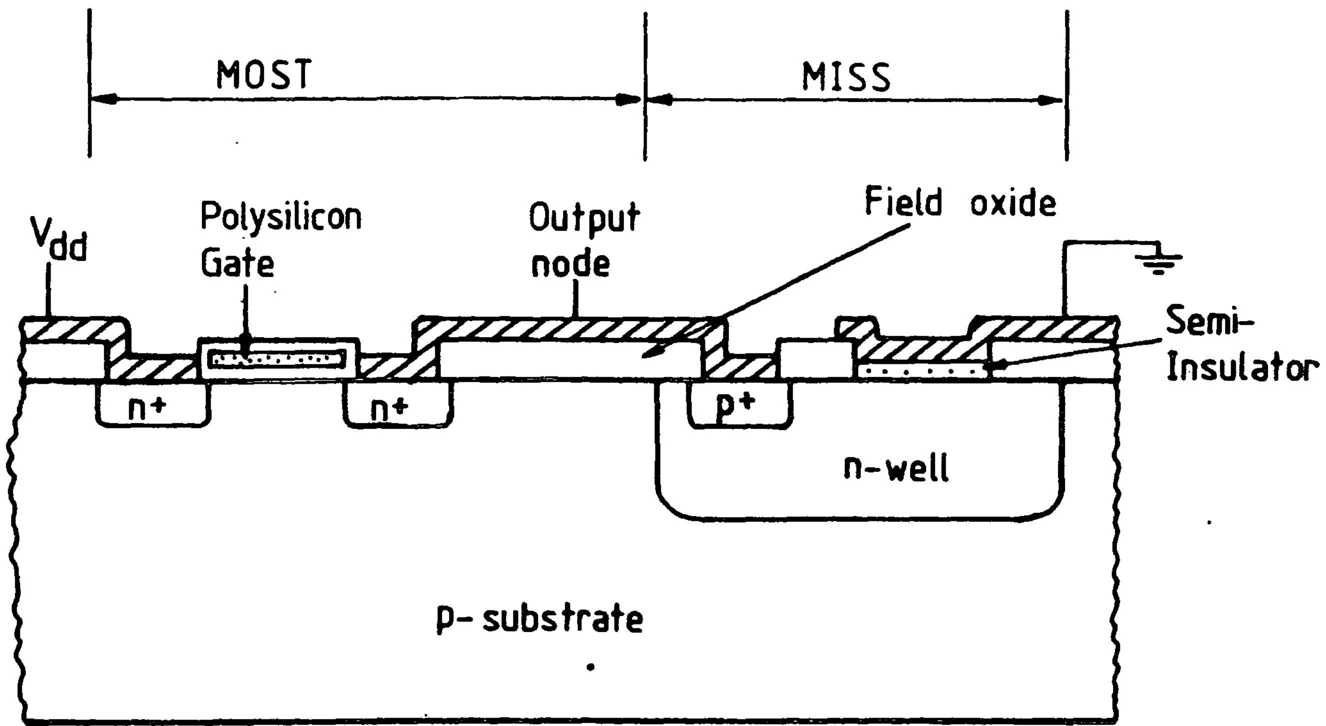
The geometrical dependence of the switching parameters could be further investigated for an electrode size down to $1\mu m^2$ with better electrical isolation so that

the junction area could be made as small as possible. Junction isolation made by ion implantation is believed to be the best technique to be implemented in future. The holding current has been shown theoretically to increase with the doping concentration in the epilayer. The effect of high current injection, which gives rise to a high holding voltage for a very small electrode device, could therefore be reduced by using an epilayer with low doping concentration. The effect of electrode perimeter could be further investigated by using a different shape of electrode so that the perimeter could be increased significantly. These experimental investigations need to be linked to a theoretical model which is already being developed. At present the model is quite advanced for tunnel oxide devices but it will need to be extended to allow for the conduction mechanism in SRO.

The SRO-MISS structure used throughout this work used an n/p^+ substrate. As has been indicated by some other workers a smaller holding voltage can easily be obtained if a p/n^+ substrate is used. Therefore this could be further investigated for the SRO-MISS. The effect of doping concentration of either n or p epilayer on p^+ or n^+ substrate could also be studied in future. The effect of work function difference could be further studied using other electrode metals such as molybdenum, and using a variety of types of SRO film . Another alternative electrode is a polysilicon layer which can easily made by closing the N_2O valve of the APCVD reactor at the end of the SRO deposition. This has the advantage that the problem of atmospheric oxide, which grows on the SRO layer before metallisation, could be reduced.

MIS – Emitter Transistor

The characteristic of the MIS-emitter transistor could be investigated further by using an n^+ instead of a p^+ collector, and a lower doping concentration in the base. This structure has been shown to give high current gain. Therefore this investigation could be extended to the use of SRO as the semi-insulator. The dependence of the



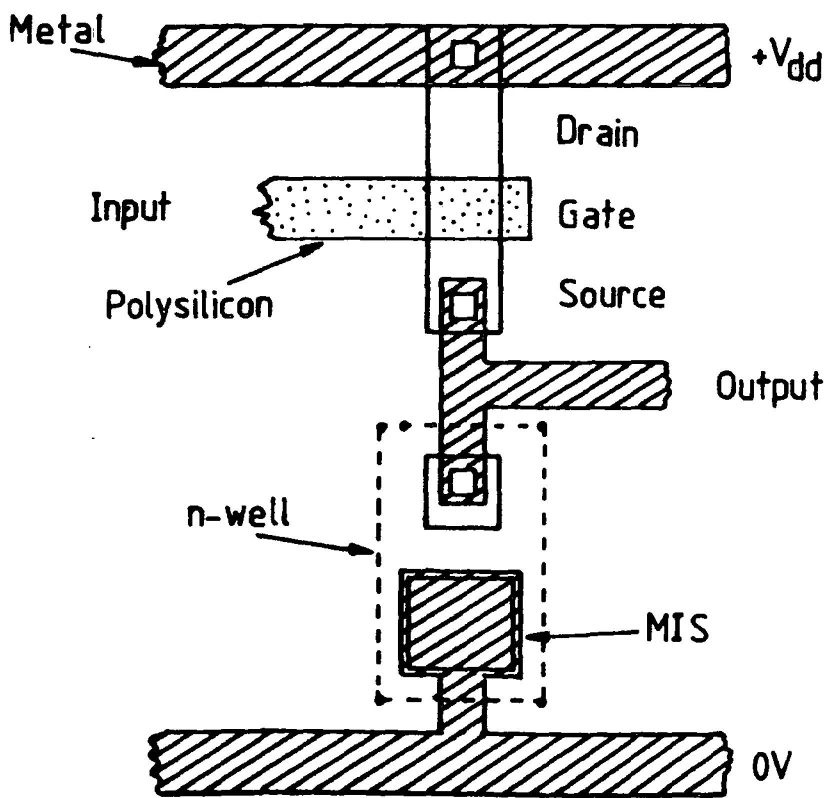


Figure 8.1 a) Cross-section of MOSMISS (not to scale) and b) IC layout.

transistor characteristics on the SRO type has not yet been investigated, and this could be done in future work. The peculiar N-type negative resistance behaviour for the structure with a very thin epilayer could be investigated.

Negative Capacitance

Since the negative capacitance characteristic is believed to be a new feature of the MISS, much of the work could be extended to investigate that behaviour in different device structures such as the lateral MISS. The dependence of the negative capacitance on the device geometry and the SRO composition could be investigated in more detail. For circuit applications, measurements on very small and lateral MISS devices are very important. Therefore the measurement technique has to be improved. The negative capacitance of a MIST has not been investigated in the present work. This could be done in future to see the effect of base current on the negative capacitance.

The inverter characteristic of the MOSMISS circuit could be further investigated. MISS devices with high doping concentrations have been shown to have a low switching voltage and a small magnitude of negative resistance, and these have an advantage when used in the MOSMISS inverter circuit. Therefore for future investigation a high doping concentration MISS device should also be used. Since the stray capacitance and inductance of the wiring affects the circuit response of the inverter circuit a monolithic MOSMISS circuit should be used. This could possibly be made by fabricating the layout shown in figure 8.1.

Other applications of the negative resistance are as a voltage controlled oscillator and as an optical variable capacitance. These two application could be investigated further in future.

The present work has shown that the SRO-MISS has some very interesting properties which could lead to exciting applications. The continuation of the work would establish the practical feasibility of these uses.

APPENDIX A

TUNNELLING BETWEEN METAL AND SEMICONDUCTOR

The tunnelling current between the semiconductor and the metal can be expressed as

$$J = \left(\frac{2mq}{\hbar^3}\right) \int_{E_x} \int_{E_T} |M_{sm}|^2 \rho_s \rho_m (f_s - f_m) dE_T dE_x \qquad A.1$$

where $|M_{sm}|^2$ is the matrix element for the transition from the semiconductor to the metal, ρ_s and ρ_m are the density of states, f_s and f_m are the Fermi functions (probability of occupation) in the semiconductor and metal respectively, E_x and E_T are the component energies due to perpendicular and transverse momenta to the tunnelling barrier.

Approximately [1]

$$|M_{sm}|^2 = \frac{1}{\rho_s \rho_m (2\pi)^2} e^{-\eta} \qquad A.2$$

where $\eta = e^{-\chi^{1/2} d}$

Substituting $A.2$ into $A.1$ gives

$$J = \frac{4\pi qm}{h^3} \int (f_s - f_m) dE \int e^{-\eta} dE_T \qquad A.3$$

and at $E_T = 0$

$$J = \frac{4\pi qm}{h^3} e^{-\eta} \int (f_s - f_m) E dE \qquad A.4$$

[1] H. C. Card and E. H. Rhoderick, J. Phys. D, 4, p.1589 (1971).

$$J = \frac{4\pi qm}{h^3} e^{-\eta} \int_0^\infty \left[\frac{E}{1+\exp(\frac{E-E_{Fm}}{kT})} - \frac{E}{1+\exp(\frac{E-E_{Fn}}{kT})} \right] dE \qquad A.5$$

let $x = \frac{E}{kT}$ or $E = xkT$

then

$$\int_0^\infty \frac{E}{1+\exp(E - \frac{E_{Fm}}{kT})} dE = kT^2 \int_0^\infty \frac{x\,dx}{1+\exp(x - \frac{E_{Fm}}{kT})} \qquad A.6$$

which is a Fermi Dirac integral of order 1,

$$F_1(a) = \int_0^\infty \frac{x dx}{1+\exp(x-a)}$$

equation $A.6$ can be writen as

$$(kT)^2 F_1\left(\frac{E_{Fm}}{kT}\right)$$

Similarly

$$\int_0^\infty \frac{E}{1+\exp(E - \frac{E_{Fn}}{kT})} dE = (kT)^2 F_1\left(\frac{E_{Fn}}{kT}\right)$$

Substituting these into $A.5$ we have

$$J = \frac{4\pi qm(kT)^2}{h^3} e^{-\eta} \left[F_1\left(\frac{E_{Fm}}{kT}\right) - F_1\left(\frac{E_{Fn}}{kT}\right) \right]$$

$$= AT^2 e^{-\eta} \left[F_1\left(\frac{E_{Fm}}{kT}\right) - F_1\left(\frac{E_{Fn}}{kT}\right) \right] \qquad A.7$$

where A is a Richardson constant given by

$$A = \frac{4\pi qmk^2}{h^3}$$

APPENDIX B

B.1 CLEANING PROCEDURE FOR SILICON

First, the silicon wafer is boiled in a powerful organic solvent to remove grease. Then it has to be boiled in a strong oxidising agent to remove organic contamination. However this process also causes oxide to grow on the surface of the silicon, and it can be removed by dipping the slice in hydrofluoric acid. The slice is then rinsed thoroughly in ultrapure water before proceeding to the next stage of processing.

The details of this procedure are as follows:-

1) The slice was boiled in trichloroethane for 5 minutes and repeated with fresh trichloroethane.
2) The slice was washed in trichloroethane in an ultrasonic bath for 1 minute.
3) The slice was rinsed in propan-2-ol and then in deionised water or blown-dry directly from trichloroethane.
4) The slice was boiled in "bomb" $(1 : 1, H_2O_2 : H_2SO_4)$ for 30 minutes.
5) The slice was washed in deionised water.
6) The slice was dipped in 10% HF for 2 minutes or until surface was hydrophobic.
7) The slice was washed in deionised water, and left it in recirculating deionised water for several hours until the resistivity of the water leaving the recirculator reached $10^7 \Omega cm$
8) The slice was now ready for next processing step.

B.2 DEPOSITION PROCEDURE FOR CVD REACTOR

In view of the importance of the exact deposition procedure in determining the properties of the films, the exact instructions are given here for later workers.

Outside the clean room.

1) First of all, the high pressure N_2 cylinder valve was turned on and the pressure was adjusted to 60 psi. Then the low pressure N_2 was turned on with the pressure adjusted to 30 psi. The clean room low pressure N_2 supply valve located below the drying columns was turned on.

Inside the clean room.

2) The main power switch located on the wall at the back of the machine was turned on.
3) The water supply was turned on until the water tank was full. Then the water pump was turned on.
4) The power switch located on the front panel of the machine was turned on. The vent/deposit switch should be in the vent mode. The N_2/H_2 switch should be in the N_2 mode. The auto/manual switch should be in manual mode. All the other gas switches (HCl, N_2O, SiH_4) should be off.
5) The N_2 pressure regulator on the front panel of the machine was set to 30 psi and adjusted to give a main N_2 flow rate to 15 litres/minute.
6) The high pressure N_2 inlet valve located on the top of the machine was opened
7) The flexible pipe to the back of the machine and to the fume cupboard was attached and then the fan in the fume cupboard was turned on.

Loading the Samples.

1) The reactor door was opened by depressing the button on the front panel.
2) The susceptor was removed using the pull-rod and loading stand.
3) The samples were placed on the susceptor at the appropriate positions and it was then pushed back into the reactor chamber so that the mark on the push-rod was at the edge of the reactor door. This centred the samples in the chamber.
4) The reactor door was closed.

Heating up and Gas Flow Setting.

1) The potentiometer dial on the front panel was set to the right value for the temperature required.

SetPoint	Temperature
270	700°C
220	650°C
170	600°C

2) The heater switch on the front panel was turned on.
3) The system was allowed to heat up for about 10 minutes and purged with N_2 in the vent mode.

During the 10 minute Purge :

4) The silane (SiH_4) and Nitrous Oxide (N_2O) cylinders were turned on. The SiH_4 line to the reactor chamber was opened and both SiH_4 and N_2O regulators were set to 20 psi.
5) The N_2O valve on the front panel was turned on and the flowrate was set to the required value, and then the valve was turned off again.

6) The SiH_4 valve on the front panel was turned on and the flowrate was set to the required value, and then the valve was turned off again.

After 10 minutes Purge :

7) Both N_2O and SiH_4 valves were turned on.

8) The main N_2 flowrate was adjusted to 35 litres/minute.

9) The system purged for 5 minutes.

Deposition

1) The deposition time was set using the counter on the front panel.

2) The manual/auto switch on the front panel was turned to auto mode.

3) The vent/deposit switch was turned to deposit mode.

4) After the required deposition time had elapsed, the vent/deposit switch was turned to vent mode and the manual/auto switch to manual.

5) The heater was turned off. The main N_2 was turned back to 15 litres/minute.

6) The system was allowed to cold down for 15 minutes before unloaded the samples.

7) The silane line was purged and the machine was turned off.

B.3 LAPPING THE BACK OF THE SAMPLE

The back of the slice may become covered with oxide during processing. It is therefore necessary to clean the back before making back contacts.

1) The slice was placed on a piece of PTFE tape.

2) A small quantity of diamond compound of $1\mu m$ grain size was squeezed onto the slice.

3) A small drop of lapping fluid was transferred onto the slice using a PTFE rod.

4) The slice was polished with the rod in the paste formed by the diamond compound and the lapping fluid until the lapping compound became grey in colour. The paste was then washed off with acetone.

5) The slice was continuously washed in acetone in an ultrasonic bath. This also removed the remaining photoresist on the metal electrode.

6) The lapped surface was etched by applying a few drops of 10% HF using a small brush until the hydrophobic condition was observed.

7) The slice was washed in deionised water several times and dried from propan-2-ol.

APPENDIX C

LISTING OF COMPUTER PROGRAMS

```
10    !*************************************************
20    !*  This program is to measure I-V characteristics   *
30    !*  and the switching parameters of MISS devices      *
40    !*                                                   *
50    !*                 B.Y.M 1986                         *
60    !*                                                   *
70    !*************************************************
80!
90     DIM Amp(1000),Volts(1000),V_s(120),V_h(120),I_s(120),I_h(120),
       I_o(120)
100    DIM Cell$(120)[10],Jam(120)[40]
110    C$=CHR$(255)&"K"
120    D=1
130    Ent=1 !Entry no:
140    Pflag=0  ! MISS parameters measurement
150    PRINT "                 MEASUREMENT MODE"
160    PRINT
170    PRINT " [1] ... CURRENT - VOLTAGE"
180    PRINT
190    PRINT " [2] ... MISS PARAMETERS"
200    PRINT
210    INPUT "Enter selection",Mod
220    OUTPUT 2 USING "#,K";C$   ! Clear screen
230    IF Mod=1 THEN Pflag=1      ! Current-voltage measurement
240    INPUT "Filename:",Filename$
250    INPUT "Drive number:(0 or 1)",Disk
260    IF Disk=1 THEN Msus
270    MASS STORAGE IS ":,700,0" ! Mass storage is set to drive 0
280    IF Pflag=0 THEN 320
290    GOTO Start
300 Msus:MASS STORAGE IS ":,700,1" !Set mass storage to drive 1
310    IF Pflag=1 THEN GOTO Start
320    INPUT "New data file ?",X$
330    IF X$="Y" OR X$="y" THEN 370
340    GOSUB Display
350    INPUT "Continue at Entry no. ?",Ent
360    GOTO Start0
370    CREATE BDAT Filename$,120,7*20 !Create file for MISS parameters
380    GOTO Start
390 Start0:D=Ent ! Entry no.
400    Start: !
410 !
420    Br=0
430    J=0
440    Count=0
450    Vcount=0
460    Vflag=0
470    Iflag=0
480    Vh=100
490    Vs=0
500    Is=0
510    Ih=0
520    Io=0
530    Imax=2.E-3  ! set maximum current
540 !
550    IF D>Ent THEN 690
560    GOTO 580 ! Using Electrometer 617 as a voltage source
570    INPUT "Enter CIL Channel No. (0,1,2,or 3)......",Chn
580    INPUT "Enter multiplier factor.....",Mult
590    INPUT "Starting voltage value(in volts)....",Sta_volt
```

```
600     INPUT "End voltage value(in volts)....",End_volt
610     INPUT "Voltage increment(in volts)....",Inc_volt
620     INPUT "Maximum current(RETURN for default value(2mA))",Imax
630     Rc=(End_volt)/Inc_volt
640     CREATE BDAT Filename$,2*Rc,3*8 ! create file for I-V data
650     IF Pflag=1 THEN 700
660     INPUT "Voltage defining OFF state current",Vo
670 !
680     INPUT "Factor for increasing voltage increment after Vs",Nvf
690     INPUT "CHIP I.D. (eg. G7)",Cell$(D)
700     IF Sta_volt=0 THEN 720
710     Sta_volt1=Sta_volt/Mult
720     Inc_volt1=Inc_volt/Mult
730     Inc_volt1_s=Inc_volt1*Nvf
740     Bveer=ABS(Inc_volt)
750     End_volt1=End_volt/Mult
760     Volt=Sta_volt1
770     WAIT .02
780     CALL Elctr617(Volts(*),Volt,B) !
790     CALL Pico485(Amp(*),Am) !
800!
801!
810     IF Am>=Imax AND Pflag=1 THEN GOTO Store_iv1
820     IF Am>=Imax AND Pflag=0 THEN GOTO 1430
830     Volts(J)=B
840     Amp(J)=Am
850     J=J+1
860     IF J<>50 THEN 710
870     GOSUB Brt
880     IFBr=1 THEN 1220
890     PRINT J,B,Am
900     IF Pflag=1 THEN Increment
910!    ..........................................
920!    Looking for switching parameter
930!    ..........................................
940      IF Iflag=0 THEN Off_current
950      IF Vflag=0 THEN Test1
960      IF B<Vh THEN Test2
970      GOTO Increment
980 Off_current:Io_test=ABS(B)-ABS(Vo)-ABS(Inc_volt)
990      IF Io_test=0 OR Io_test>0 THEN Test3
1000     Veer=ABS(B-Vo)
1010     IF Veer<Bveer THEN Test2
1020     GOTO Increment
1030 Test3:Iflag=1
1040     Inc_volt1_o=Inc_volt1*2
1050     GOTO Increment
1060 Test2:IF Iflag-1<0 THEN Test4
1070     IF Vflag-1<0 THEN Test5
1080     Vh=B
1090     Ih=Am
1100     GOTO Increment
1110 Test4:Bveer=Veer
1120     Io=Am
1130     GOTO Increment
1140 Test5:Vs=B
1150     Is=Am
1160     GOTO Increment
1170 Test1:IF B>Vs THEN Test2
1180     Vcount=Vcount+1
```

```
1190    IF Vcount<>3 THEN Increment
1200    Vflag=1
1210 Increment: !Increase voltage
1220        IF Pflag=1 THEN 1250
1230    IF Iflag=1 THEN Inc_volt1=Inc_volt1_o
1240    IF Vflag=1 THEN Inc_volt1=Inc_volt1_s
1250    Volt=Volt+Inc_volt1
1260! IF Volt>=End_volt1 THEN Inc_volt1=(-1)*Inc_volt1 ! voltage decrement
1270    IF Volt>=End_volt1 THEN 1300
1280! IF Volt<=Sta_volt THEN 1200
1290    GOTO 770
1300    FOR I=0 TO J-1
1310        PRINT Volts(I),Amp(I)
1320    NEXT I
1330    IF Pflag=0 THEN 1380
1340 Store_iv1: ASSIGN @File TO Filename$
1350    FOR I=1 TO J
1360         OUTPUT @File,I;Volts(I),Amp(I)
1370    NEXT I
1380 Reset_vso:  Volt=0
1390    WAIT 0.5
1400    CALL Source(Volt)
1410    IF Pflag=1 THEN 1680
1420    PRINTER IS PRT
1430    PRINT "Filename";Filename$,"CHIP I.D.:";Cell$(D),
        TIME$(TIMEDATE)&DATE$(TIMEDATE)
1440    PRINT "Vs:";Vs;" Vh:";Vh;" Is:";Is;" Ih:";Ih;" Io:";Io
1450    PRINTER IS CRT
1460    FOR I=5 TO 10
1470         BEEP 81.38,.06
1480    NEXT I
1490    INPUT "Write results to disc ?(Y/N)",X$
1500    IF X$<>"Y" THEN 1710
1510    V_s(D)=Vs
1520    V_h(D)=Vh
1530    I_s(D)=Is
1540    I_h(D)=Ih
1550    I_o(D)=Io
1560    Jam$(D)=TIME$(TIMEDATE)&DATE$(TIMEDATE)
1570 !........
1580 INPUT "Store I-V values on disc ?",A$
1590 IF A$="Y" OR A$="y" THEN GOSUB Store_iv
1600    INPUT "More measurements ?(Y/N)...<RETURN>",X1$
1610    IF X1$<>"Y" THEN 1640
1620    D=D+1
1630    GOTO Start
1640    ASSIGN @File TO Filename$
1650    FOR D=Ent TO D
1660 Output: OUTPUT @File,D;V_s(D),V_h(D),I_s(D),I_h(D),I_o(D),
     Cell$(D),Jam$(D)
1670    NEXT D
1680     ASSIGN @File TO * ! Close the file
1690     GOSUB Display
1700     GOTO 2010
1710     INPUT "More measurement ?(Y/N)...<RETURN>",X2$
1720     IF X2$="Y" THEN Start
1730     GOTO 1640
1740  STOP
1750 Store_iv:    !Store I-V values from mode 2
1760              INPUT "FILENAME:",Filename2$
```

```
1770 !  Filename2$=Filename$&Cell$(D)
1780     MASS STORAGE IS ":,700,1"
1790     CREATE BDAT Filename2$,300,2*8
1800       ASSIGN @Path TO Filename2$
1810       FOR I=1 TO J-1
1820       OUTPUT @Path,I;Volts(I),Amp(I)
1830       NEXT I
1840       ASSIGN @Path TO *
1850       MASS STORAGE IS ":,700,0"
1860      RETURN
1870 Display:  !
1880      ASSIGN @Path TO Filename$
1890      IMAGE DD,3X,ZZ.DD,3X,ZZ.DD,3X,D.3D,3X,D.2DE,3X,D.2DE,3X,4A,1X,20A
1900      ON END @File GOTO 1950
1910      FOR I=1 TO 120
1920         ENTER @File,I;V_s(I),V_h(I),I_s(I),I_h(I),I_o(I),Cell$(I)
1930         PRINT USING 1890;I;V_s(I),V_h(I),I_s(I),I_h(I),I_o(I),
             Cell$(I),Jam$(I)
1940      NEXT I
1950      RETURN
1960 Brt:  !
1970          IF ABS(B)>=ABS(20*Inc_volt1) THEN 2000
1980          Br=1
1990          PRINT "Device breakdown"
2000          RETURN
2010        END
2020  !*****************************************************
2030  !*        IEEE-488 subprograms                        *
2040  !*****************************************************
2050  !
2060  !
2070  !**************************************************
2080  !  Subprogram for CIL 20 (Digital to Analog Converter
2090  !**************************************************
2100        SUB Cil20(Volt,Chn,V)
2110             ASSIGN @Cil TO 712
2120             CLEAR @Cil
2130             TRIGGER @Cil
2140             ON TIMEOUT 7,.05 GOSUB Hpib
2150             OUTPUT @Cil;"A,WR1,WE1,OD0,OD2,OD3"
2160             SEND 7;UNL
2170             ABORT 7
2180             V=3276.7*Volt
2190             CLEAR @Cil
2200             ON TIMEOUT 7,.1 GOSUB Hpib1
2210             OUTPUT @Cil;"WV1";V;",1"
2220             ON TIMEOUT 7,.1 GOSUB Hpib1
2230             SEND 7;UNL
2240             Abort 7
2250             WAIT 1 ! Delay for 1 second
2260             CLEAR @Cil
2270             OUTPUT @Cil;"A,WR1,WE1,OD0,OD2,OD3"
2280             SEND 7;UNL
2290             ABORT 7
2300             GOTO 2380
2310 Hpib        STATUS 7,7;A
2320             IF BIT(A,4)=1 THEN CONTROL 7,3;16
2330             RETURN
2340 Hpib1:      STATUS 7,7;A
2350             IF BIT(A,4)=1 THEN CONTROL 7,3;16
```

```
2360            V=3276.7*Volt
2370            RETURN
2380    SUBEND
2390 !****************************************
2400 ! Subprogram for Keithly 485 Picoammeter
2410 !****************************************
2420    SUB Pico485(Amp(*),Am)
2430            ASSIGN @Pico TO 722 ! Assign to device address
2440            CLEAR @Pico
2450            REMOTE @Pico
2460            OUTPUT @Pico;"R0X" ! setr device to autorange mode
2470            OUTPUT @Pico;"G1X" ! do not send prefix
2480            ENTER @Pico;Am ! send data from device to controller
2490    SUBEND
2500 !****************************************
2510 ! Subprogram for Keithly 195 System DMM
2520 !****************************************
2530    SUB Dmm195(Amp(*),Am)
2540            ASSIGN @Dmm195 TO 719
2550            CLEAR @Dmm195
2560            REMOTE @Dmm195
2570            OUTPUT @Dmm195;"F3X" !Dc Ammeter
2580            OUTPUT @Dmm195;"R0X  !Auto mode
2590            OUTPUT @Dmm195;"G1X" !do not send prefix
2600            TRIGGER @Dmm195
2610            ENTER @Dmm195;Am !send data to controller
2620            WAIT .02
2630            GOTO 2680
2640 Hpib1:      STATUS 7,7;A
2650             IF BIT(A,4)=1 THEN 2670
2660             CONTROL 7,3;16
2670             RETURN
2680     SUBEND
2690 !****************************************************
2700 ! Subprograms for Keithly 617 Programmable Electrometer
2710 !****************************************************
2720 ! a) as a voltage source and voltmeter
2730 !----------------------------------------
2740    SUB Electr617(Volts(*),Volt,B)
2750            ASSIGN @Elc TO 711
2760            CLEAR @Elc
2770            REMOTE @Elc
2780            OUTPUT @Elc;"D1V";Volt;"O1X" !voltage source ON
2790            OUTPUT @Elc;"F0X" !function as a voltmeter
2800            OUTPUT @Elc;"R0X" !autorange
2810            OUTPUT @Elc;"C0X" !zero check off
2820            OUTPUT @Elc;"B0X" !read mode --electrometer
2830            OUTPUT @Elc;"G1X" !do not send prefix with data
2840            WAIT .08  !Delay
2850            ENTER @Elc;B !send data to controller
2860    SUBEND
2870 !
2880 !----------------------------------------------------
2890 !b) Electrometer 617 as a voltage source only
2900 !----------------------------------------------------
2910    SUB Source(Volt)
2920            ASSIGN @Source TO 711
2930            REMOTE @Source
2940            OUTPUT @Source;"D1V";Volt;"O1X"
2950            WAIT 1 !Delay for 1 second
```

```
2960    SUBEND
2970 !******************************************
2980 ! Subprogram for Keithly DMM 175
3000 !******************************************
3010     SUB Multi175(Amp(*),Am)
3020          ASSIGN @Multi175 TO 724
3030          REMOTE @Multi175
3040          ENTER @Multi175;Am !send data to controller
3050     SUBEND
```

```
10 !*********************************************************
20 !   This program AUTOTETRAN is to measure the common emitter *
30 !   characteristics of a transistor                          *
40 !                                                            *
50 !                    B.Y.M. Dec 1986                         *
60 !*********************************************************
70       DIM Amp(1000),Volts(1000),Curt(1000)
80       C$=CHR$(255)&"K"          !
90       OUTPUT 2 USING "#,K";C$  ! to clear screen
100      INPUT "Filename:",Filename$
110      INPUT "Drive number:(0 or 1)",Disk
120      IF Disk=1 THEN Msus
130      MASS STORAGE IS ":,700,0"
140      GOTO Create_file
150 Msus:     MASS STORAGE IS ":,700,1"
160 Create_file: CREATE BDAT Filename$,300,3*8 ! create file for I,V data
170 Start: !
180 !
190      J=0
200      Step_no=0
210      INPUT "Enter multiplier factor.......",Mult
220      INPUT "Starting voltage value(in volts)....",Sta_volt
230      INPUT "End voltage value(in volts).....",End_volt
240      INPUT "Voltage increment(in volts).....",Inc_volt
250      INPUT "Initial base current",Init_c
260      INPUT "Current step",C_step
270      INPUT "Number of step",No_step !number of base current steps
280      INPUT "Voltage limit",Vlim !voltage limit for the current source
290      IF Sta_volt=0 THEN 310
300      Sta_volt1=Sta_volt/Mult
310      Inc_volt1=Inc_volt/Mult
320      End_volt1=End_volt/Mult
330      Volt=Sta_volt1
340      Cur=Init_c
350      WAIT .02
360      CALL C_source(Curt(*),Cur,Vlim)
370      CALL Elctr617(Volts(*),Volt,B)
380      CALL Pico485(Amp(*),Am)
390!
400      J=J+1
410      Volts(J)=B
420      Amp(J)=Am
430      Curt(J)=Cur
440      PRINT J,B,Am,Cur
450      IF Volt>=End_volt1 THEN Step
460 Increment:   Volt=Volt+Inc_volt1
470              GOTO 370
480 Step: WAIT 1
490              Step_no=Step_no+1
500              Cur=Cur+C_step
510              IF Step_no>=No_step THEN 540
520              Volt=Sta_volt1
530              GOTO 350
540              FOR I=1 TO J
550              PRINT Volts(I),Amp(I),Curt(I)
560              NEXT I
570              Volt=0
580              CALL Source(Volt)
590              Cur=0
600              CALL C_source(Curt(*),Cur,Vlim)
```

```
610 !.......................................
620     ASSIGN @File TO Filename$
630     FOR I+1 TO J
640             OUTPUT @File,I;Volts(I),Amp(I),Curt(I)
650     NEXT I
660     ASSIGN @File TO *  !close the file
670     FOR I=5 TO 10
680         BEEP 83.14*I,.02
690     NEXT I
700  END
710  !*****************************************************
720  !*         IEEE-488 subprograms                      *
730  !*****************************************************
740  !
750  !
760  !***************************************
770  ! Subprogram for Keithly 485 Picoammeter
780  !***************************************
790    SUB Pico485(Amp(*),Am)
800           ASSIGN @Pico TO 722 ! Assign to device address
810           CLEAR @Pico
820           REMOTE @Pico
830           OUTPUT @Pico;"R0X" ! setr device to autorange mode
840           OUTPUT @Pico;"G1X" ! do not send prefix
850           ENTER @Pico;Am ! send data from device to controller
860    SUBEND
870  !**************************************************
880  ! Subprograms for Keithly 617 Programmable Electrometer
890  !**************************************************
900  ! a) as a voltage source and voltmeter
910  !==================================
920    SUB Elctr617(Volts(*),Volt,B)
930           ASSIGN @Elc TO 711
940           CLEAR @Elc
950           REMOTE @Elc
960           OUTPUT @Elc;"D1V";Volt;"O1X" !voltage source ON
970           OUTPUT @Elc;"F0X" !function as a voltmeter
980           OUTPUT @Elc;"R0X" !autorange
990           OUTPUT @Elc;"C0X" !zero check off
1000          OUTPUT @Elc;"B0X" !read mode —electrometer
1010          OUTPUT @Elc;"G1X" !do not send prefix with data
1020          WAIT .08  !Delay
1030          ENTER @Elc;B !send data to controller
1040   SUBEND
1050 !
1060 !==========================================
1070 !b) Electrometer 617 as a voltage source only
1080 !==========================================
1090   SUB Source(Volt)
1100          ASSIGN @Source TO 711
1110          REMOTE @Source
1120          OUTPUT @Source;"D1V";Volt;"O1X"
1130          WAIT 1 !Delay for 1 second
1140   SUBEND
1150 !**************************************************
1160 ! Subprogram for Keithly 220 Programmable current source
1170 !**************************************************
1180    SUB C_source(Curt(*),Cur,Vlim)
1190          ASSIGN @C_s TO 712
1200          CLEAR @C_s
```

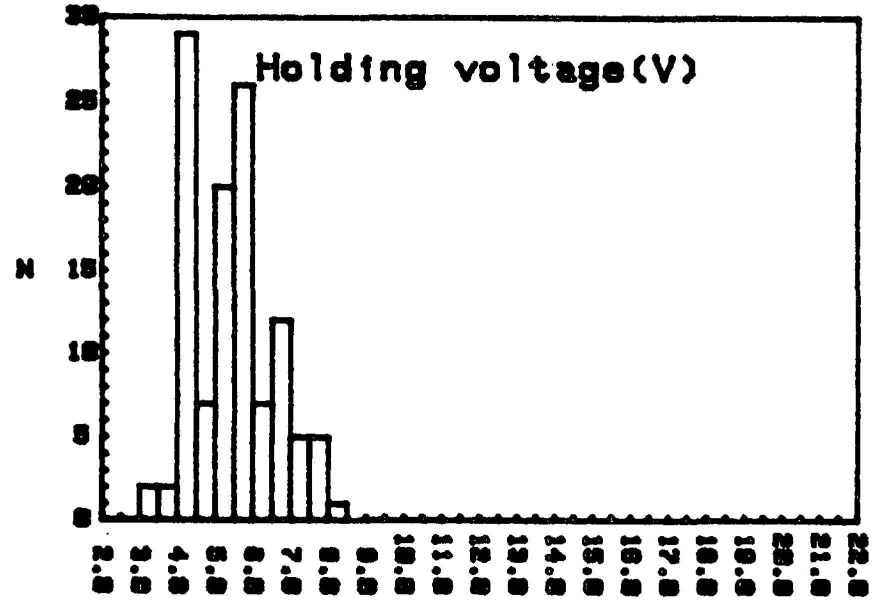
```
1210        REMOTE @C_s
1220        OUTPUT @C_s;"R0M1X"
1230        OUTPUT @C_s;"D1V";Vlim;"F1X"
1240        OUTPUT @C_s;"D0I";Cur;"F1X"
1250        WAIT .5
1260    SUBEND
```

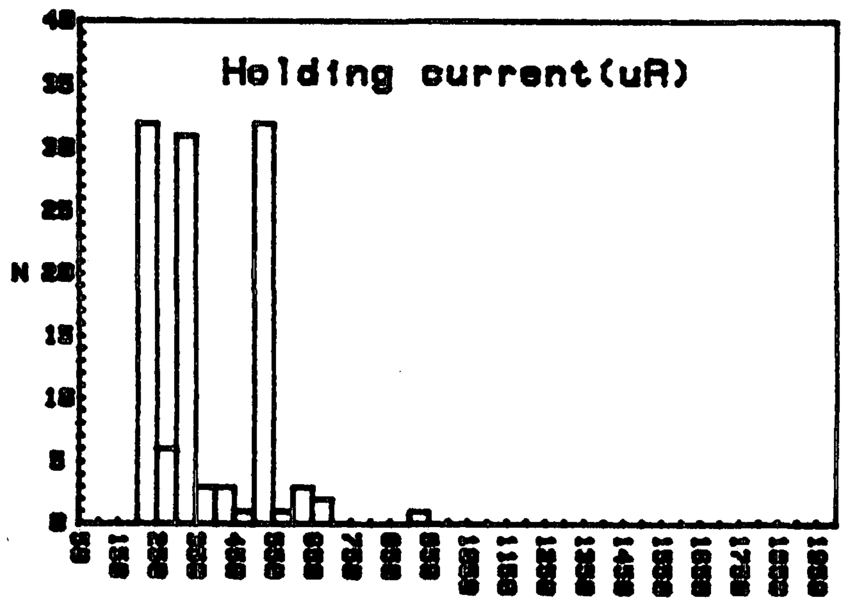
APPENDIX D

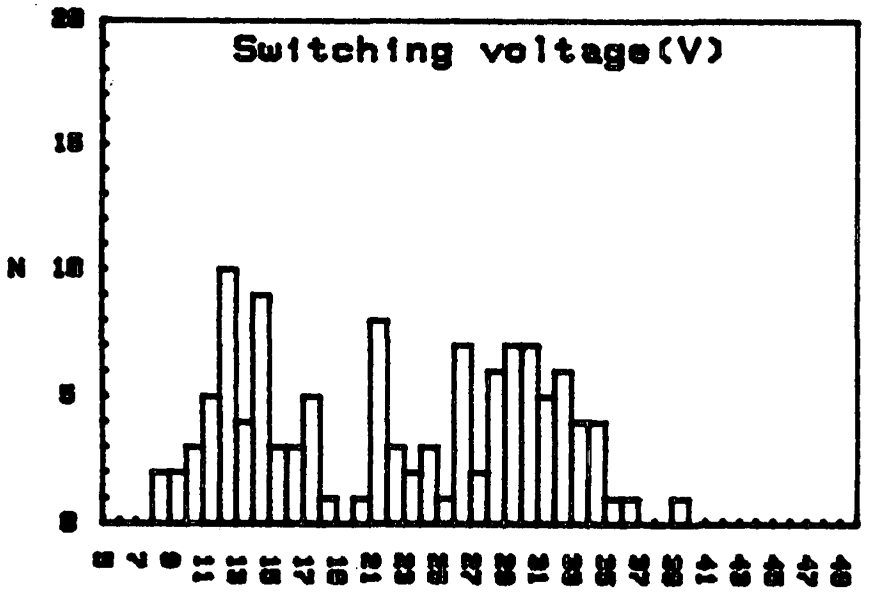
STATISTICAL RESULTS OF THE SWITCHING PARAMETERS

This appendix contain details of statistical result of V_s, V_h, I_s and I_h for the small MISS structure with different electrode sizes. All the switching parameters were measured by an automated system. The bar charts were plotted by a computer program called 'MISSHISTO' which was specially developed for this purpose and also calculate the mean, standard division and confidence of interval of the switching parameters.

Figure D1 to D9 is the bar charts of the switching parameters for MISS with an electrode sizes of $200\times200\mu$m, $160\times160\mu$m, $100\times100\mu$m, $80\times80\mu$m, $60\times60\mu$m, $40\times40\mu$m, $20\times20\mu$m, $10\times10\mu$m and $5\times5\mu$m respectively.







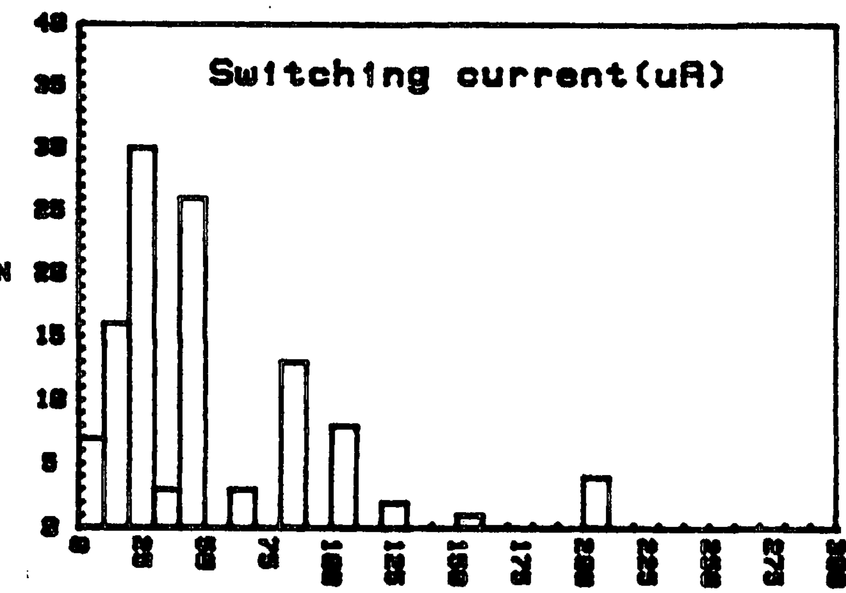
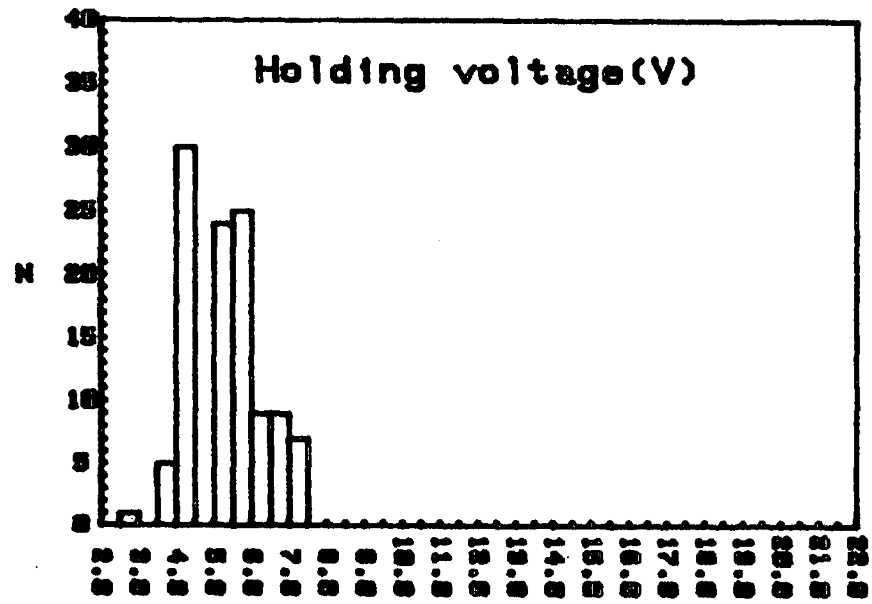
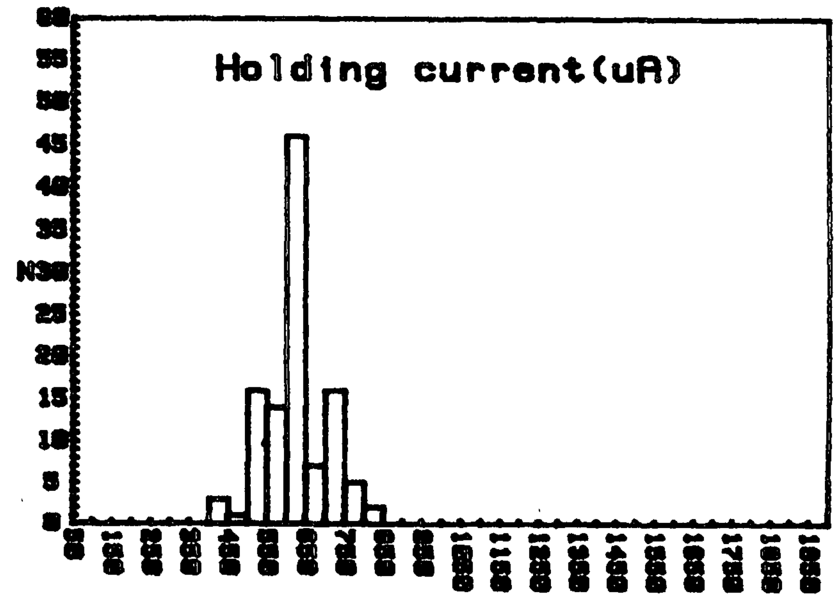
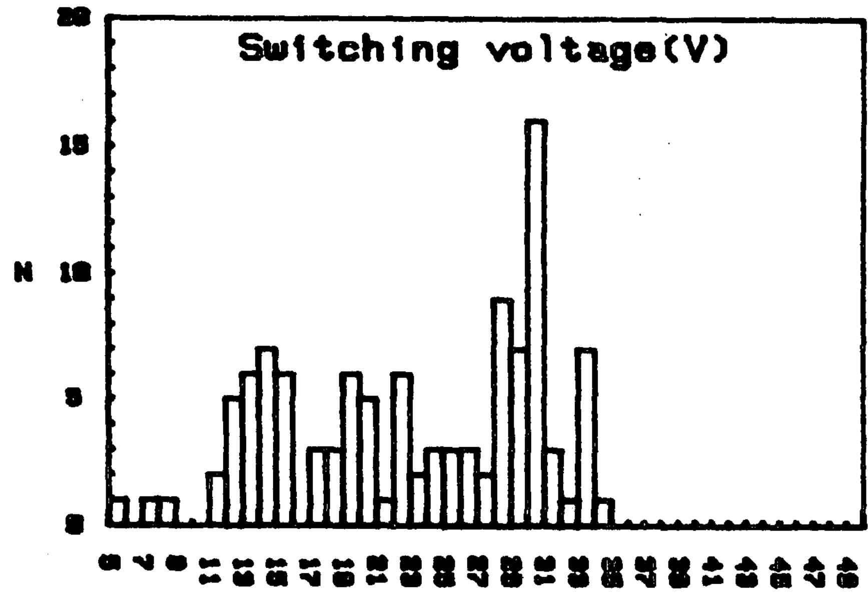


Fig. D1







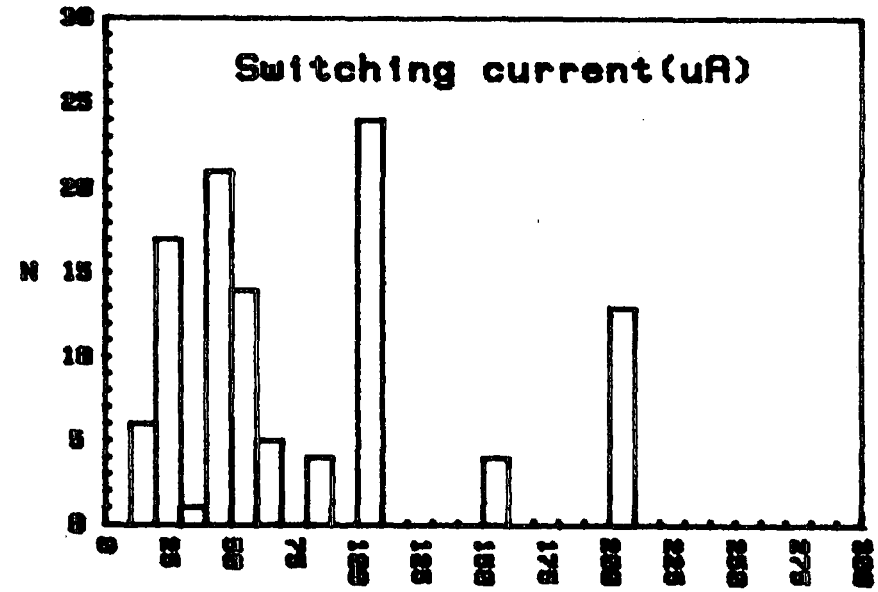
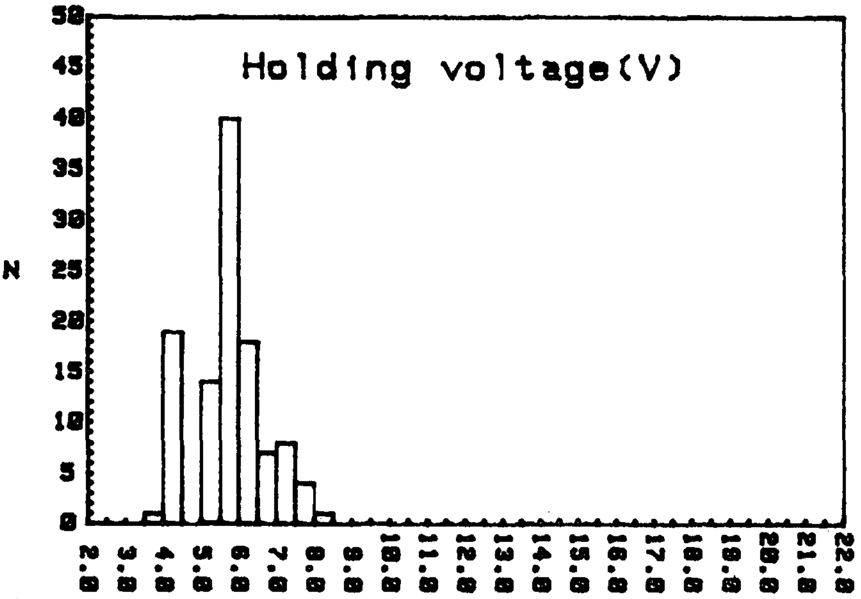
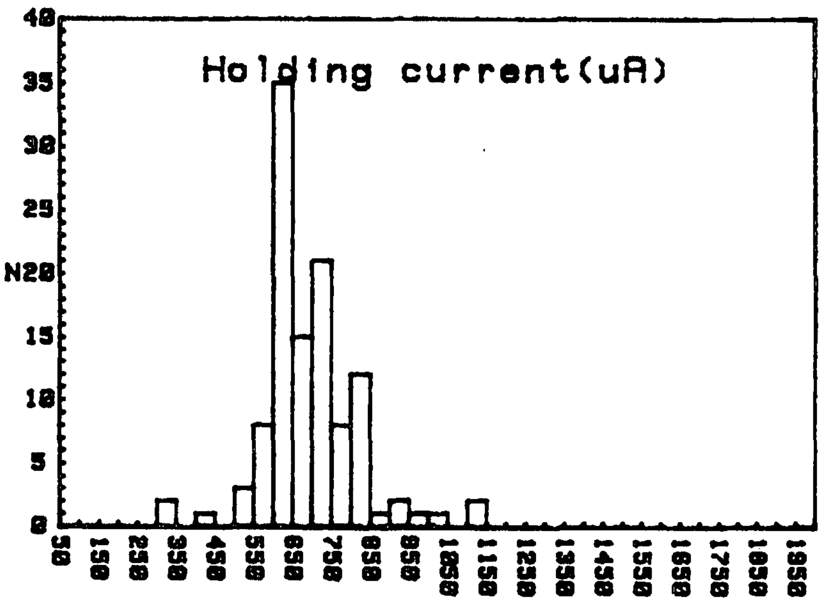
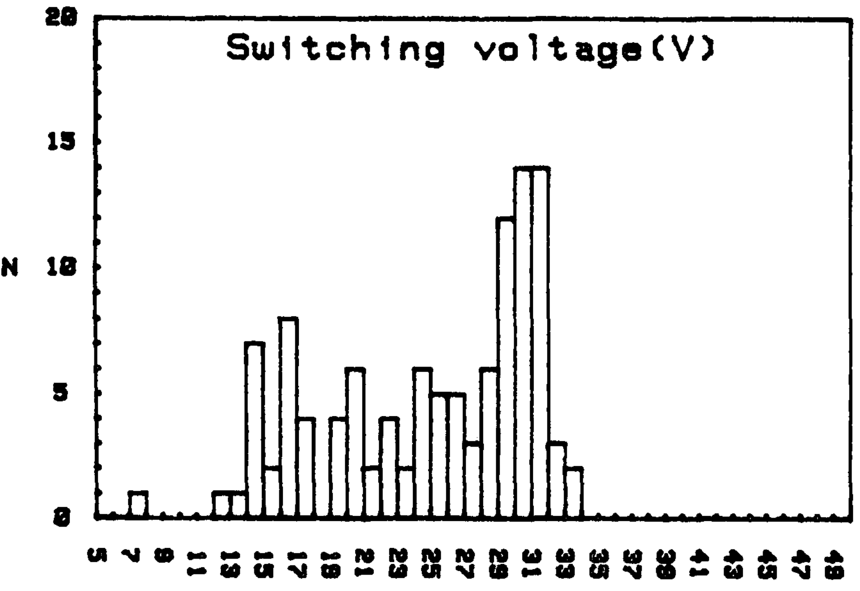


Fig. D2







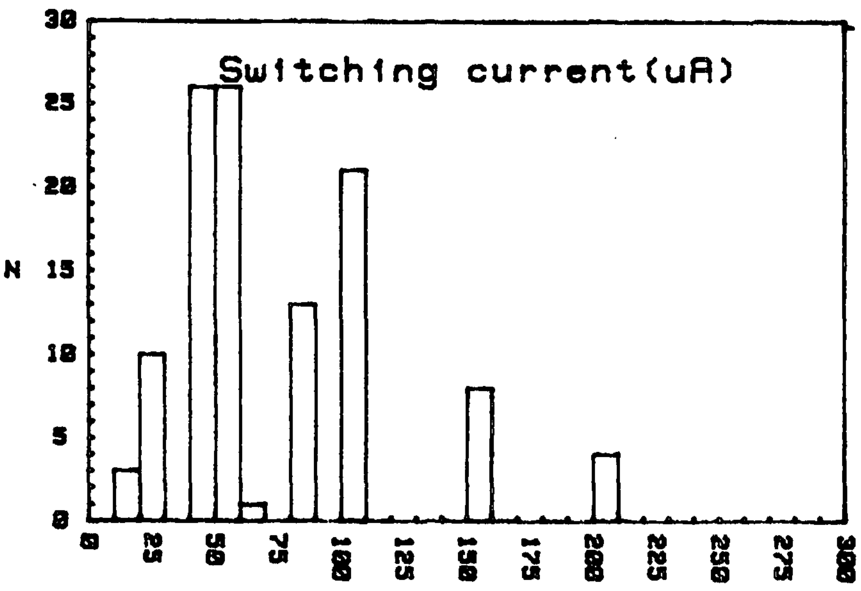
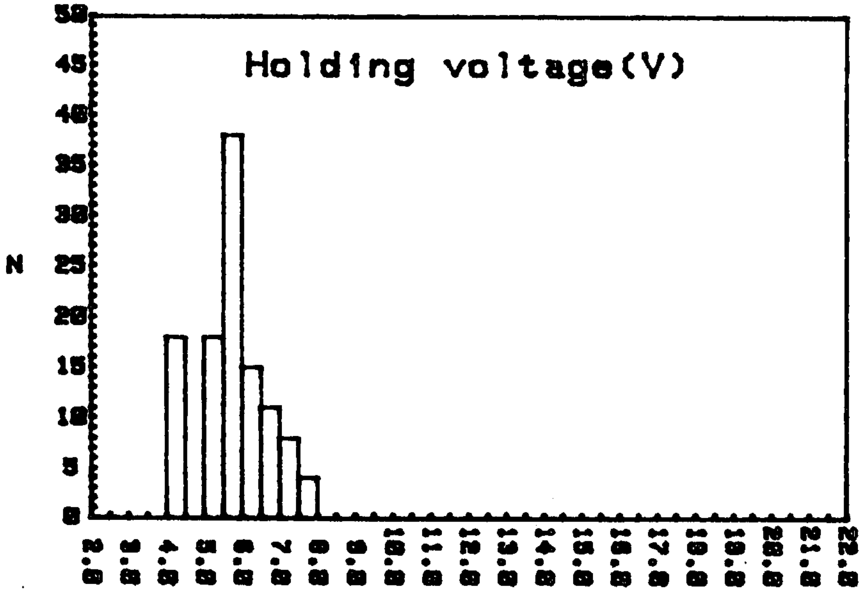
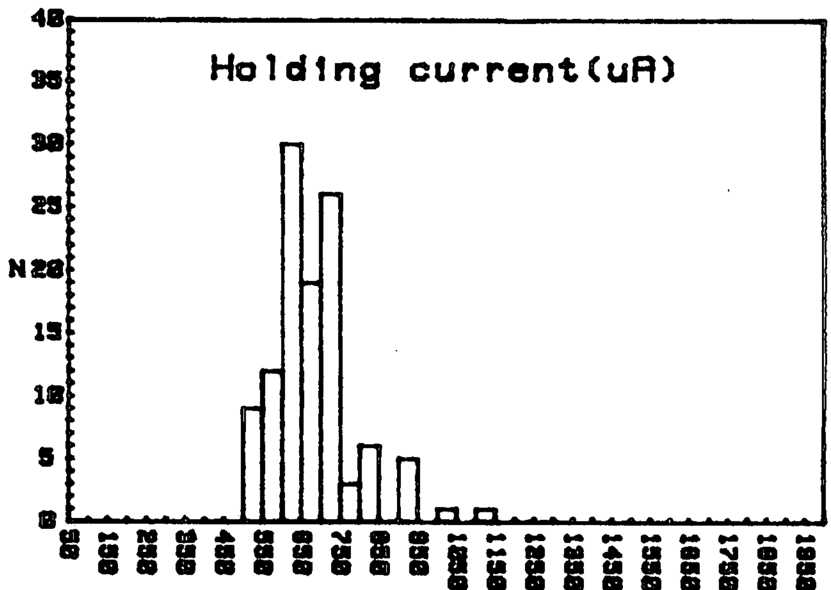
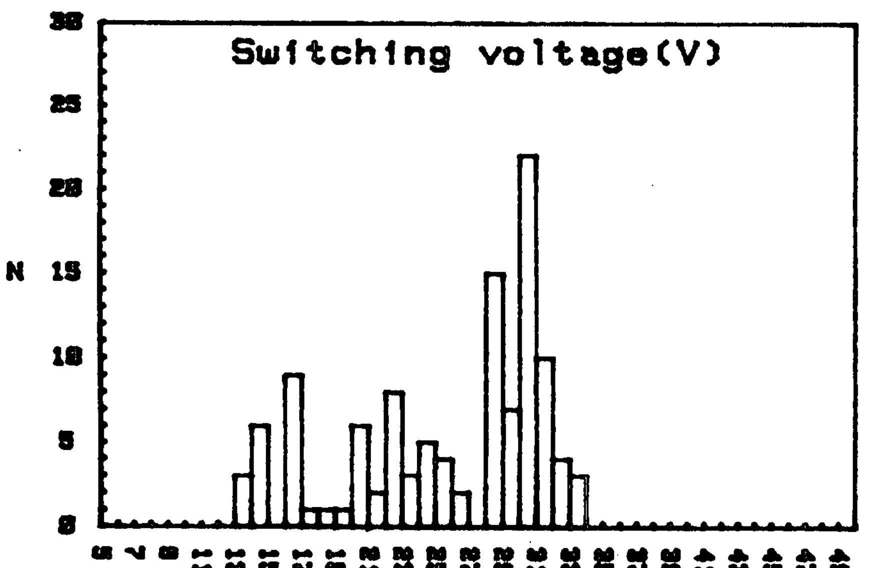


Fig. D3







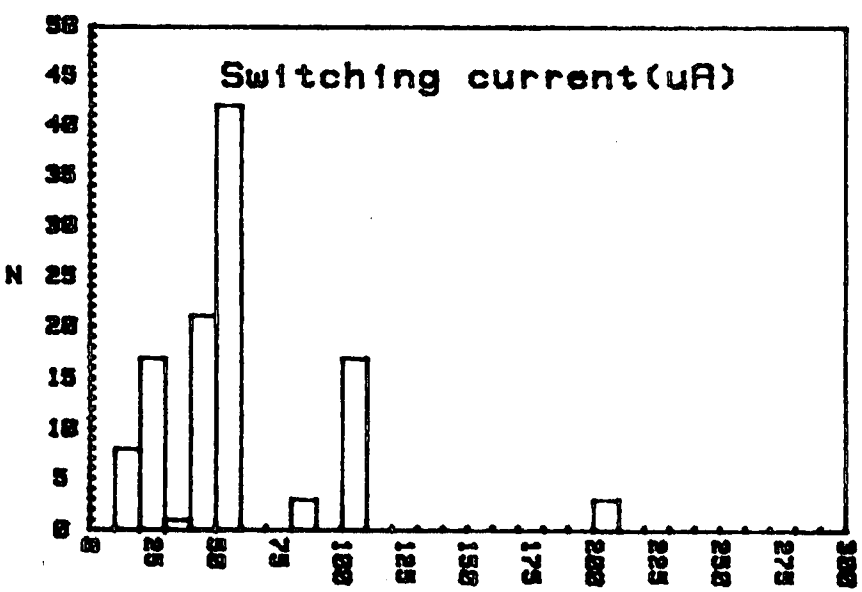
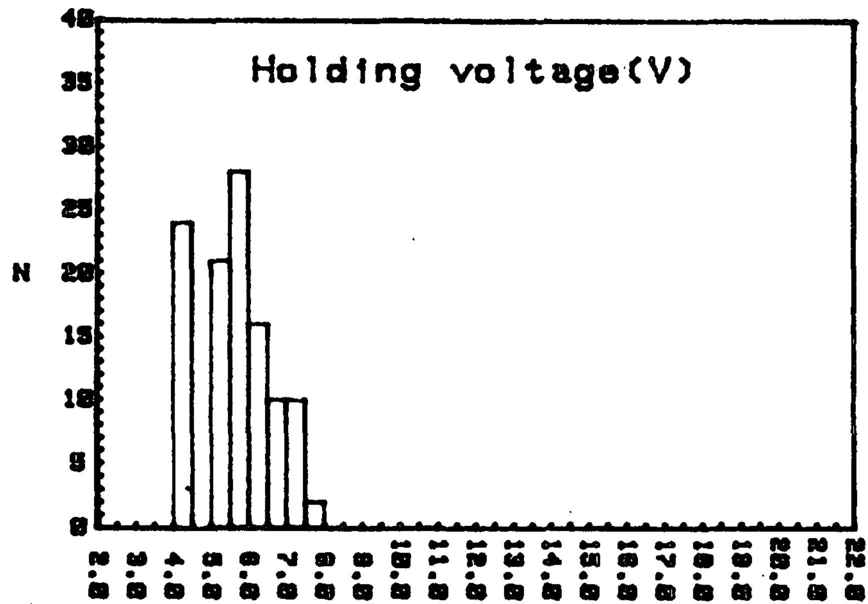
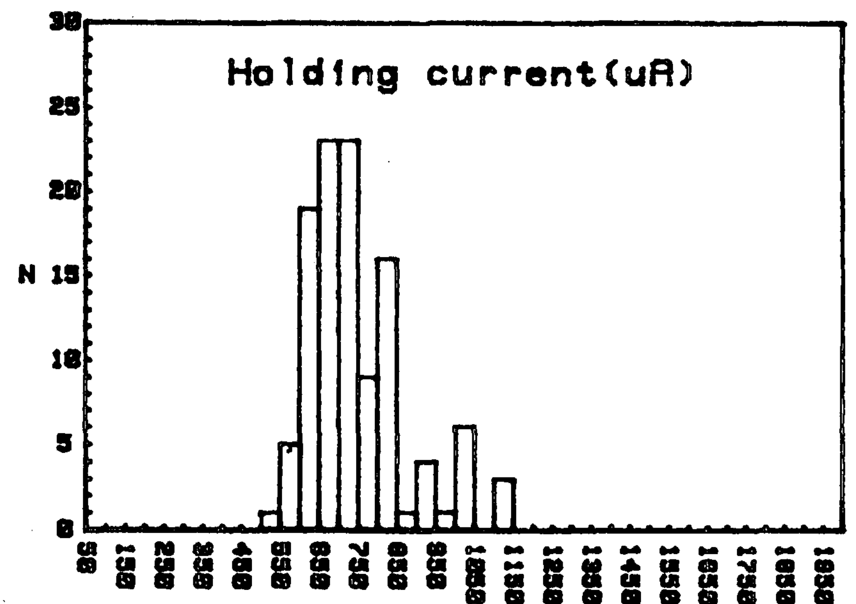
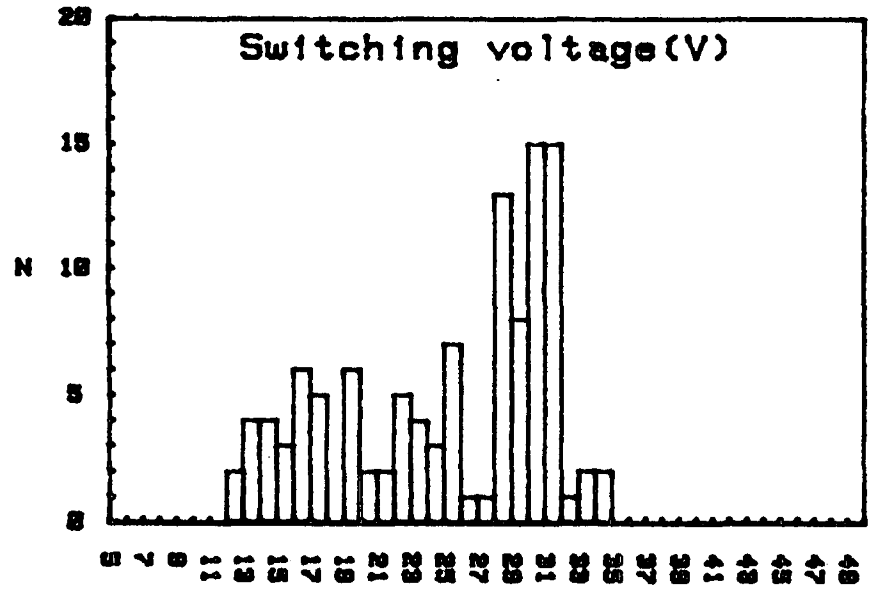
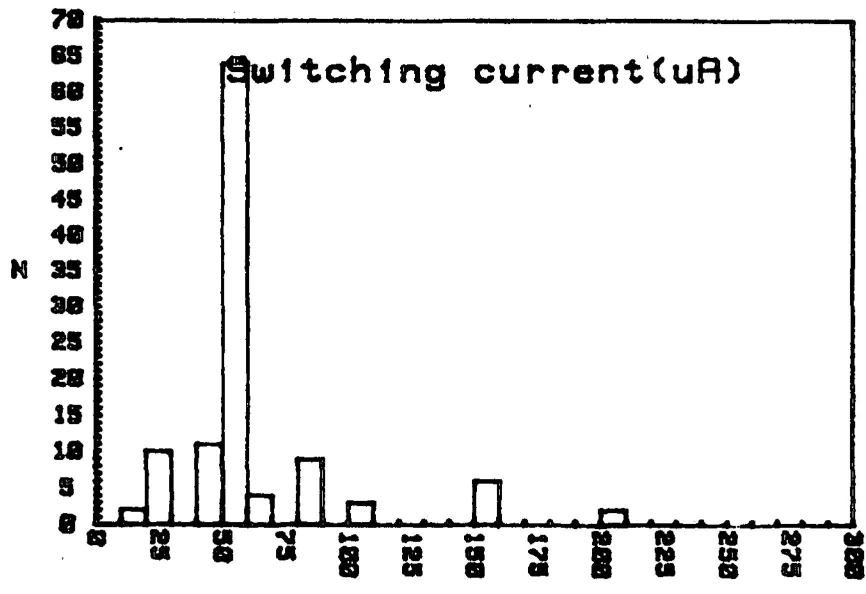


Fig. D4









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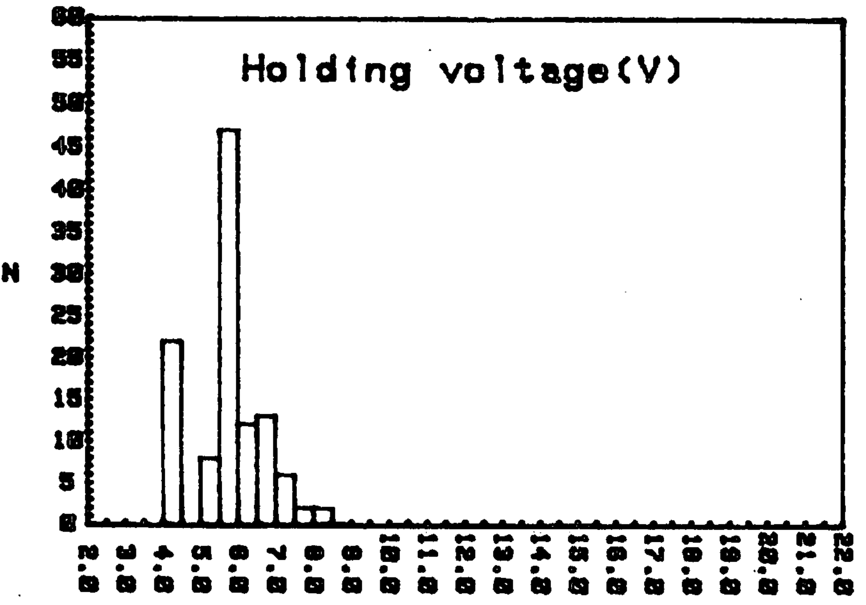
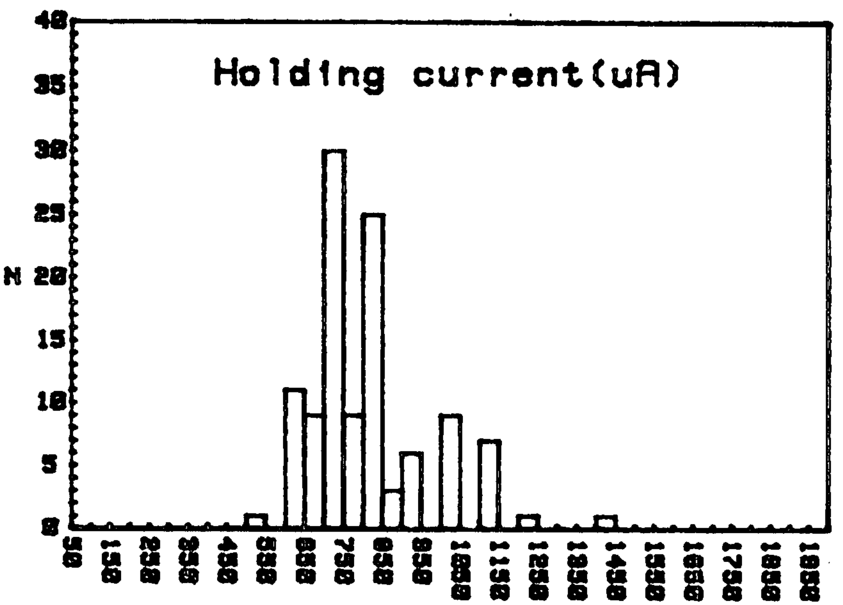
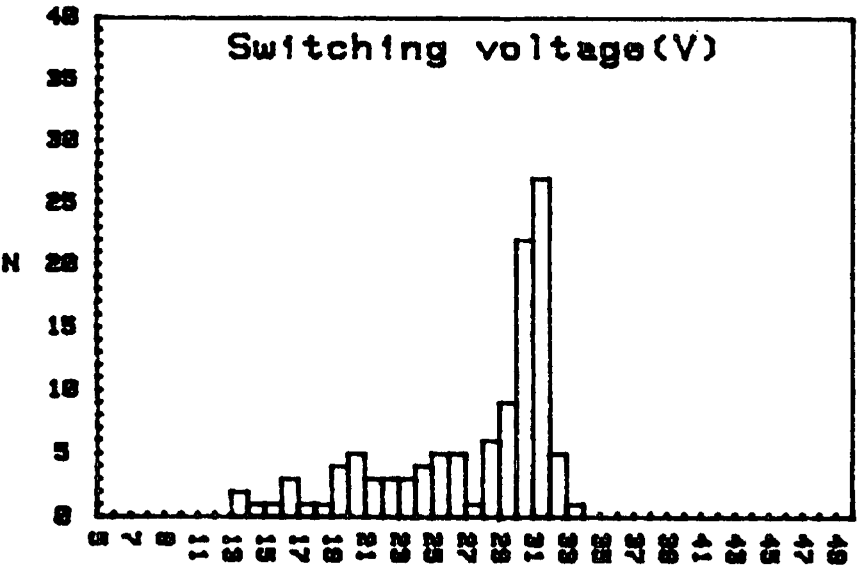






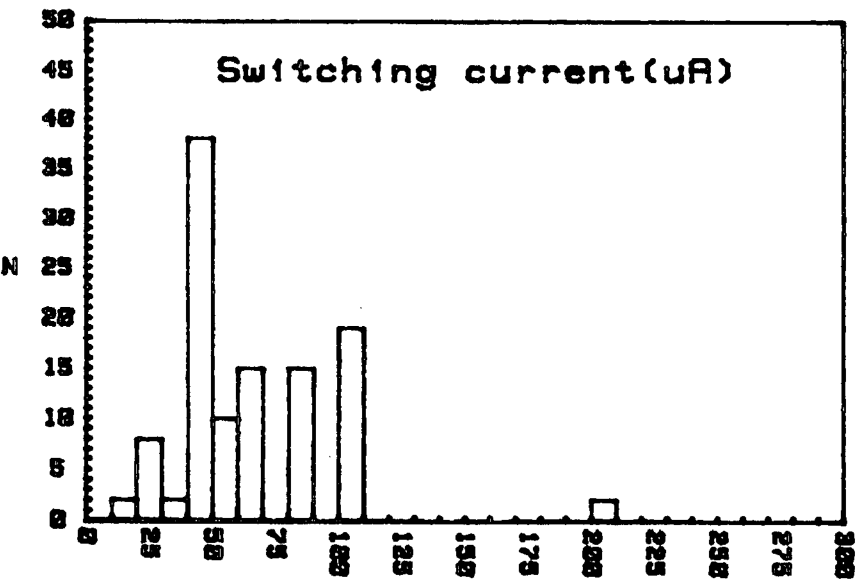
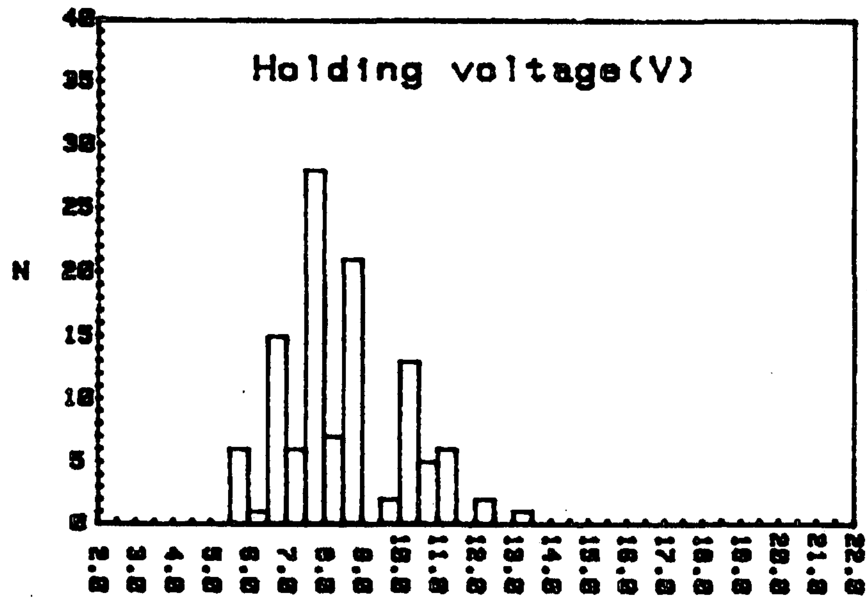
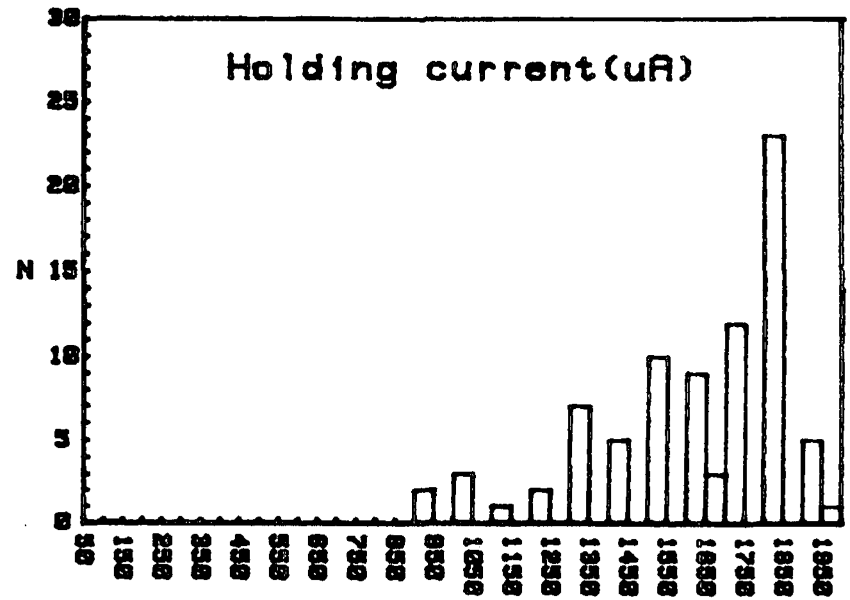
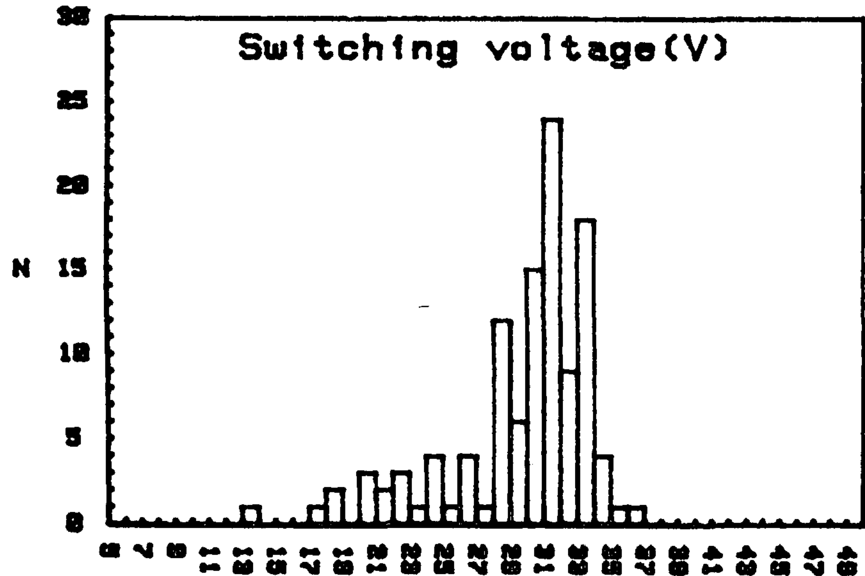


Fig. D6







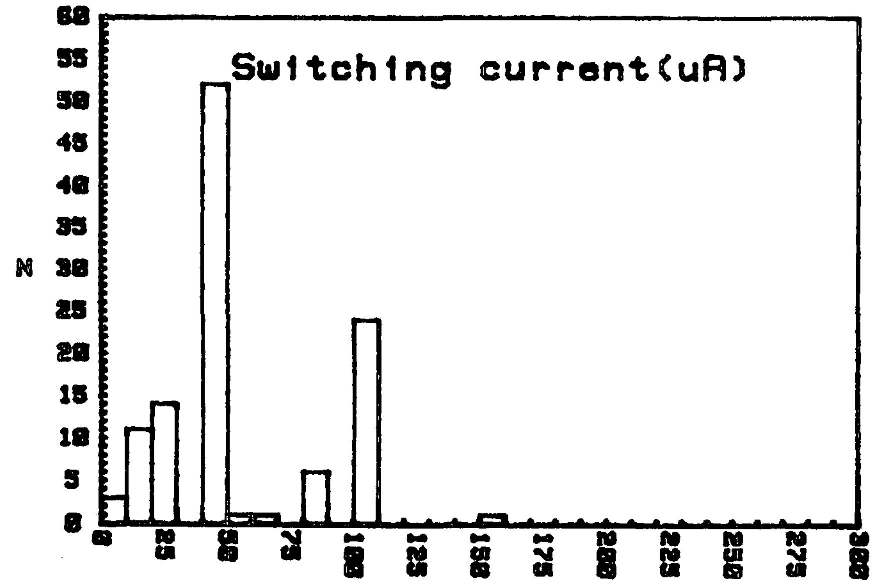
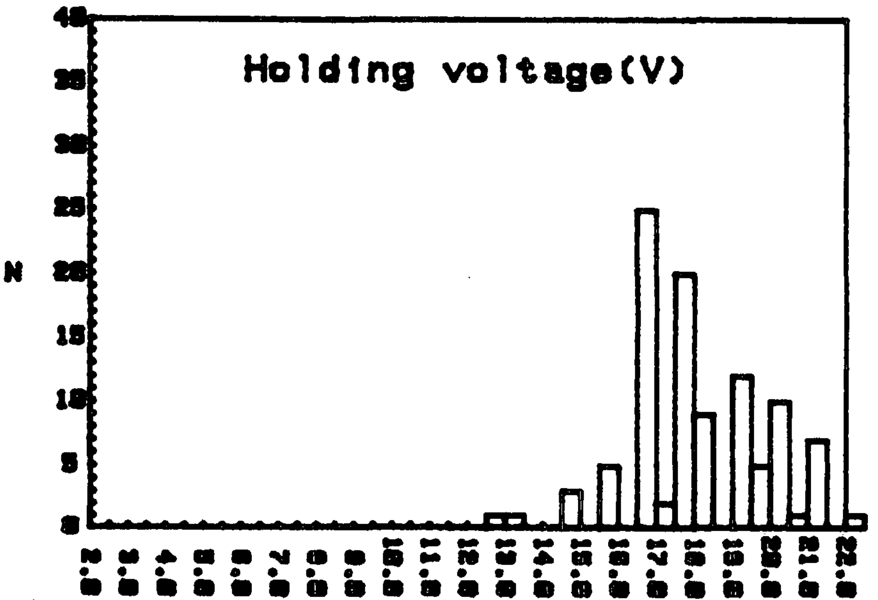
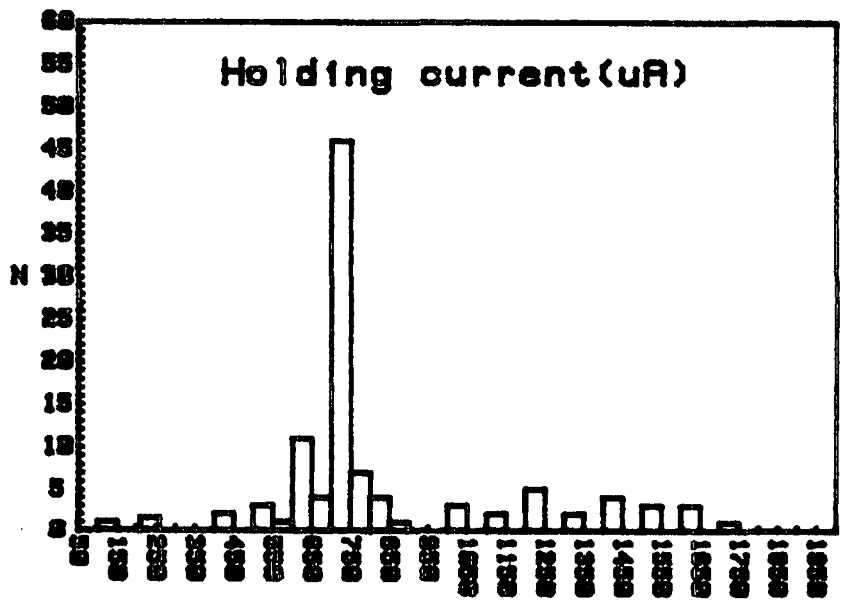
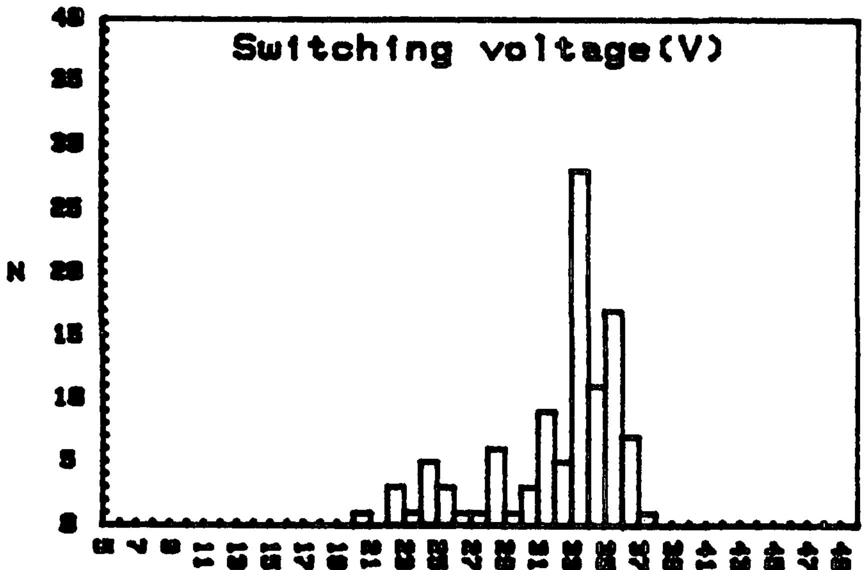


Fig. D7







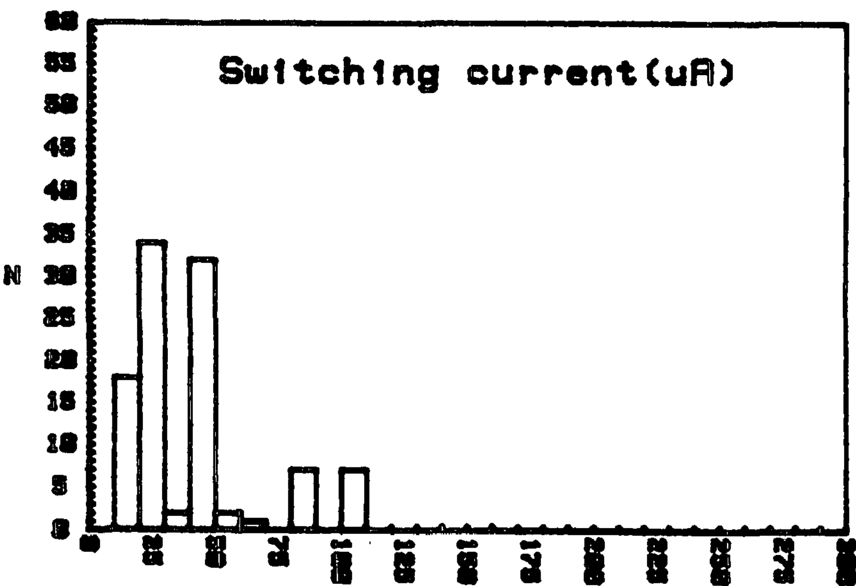
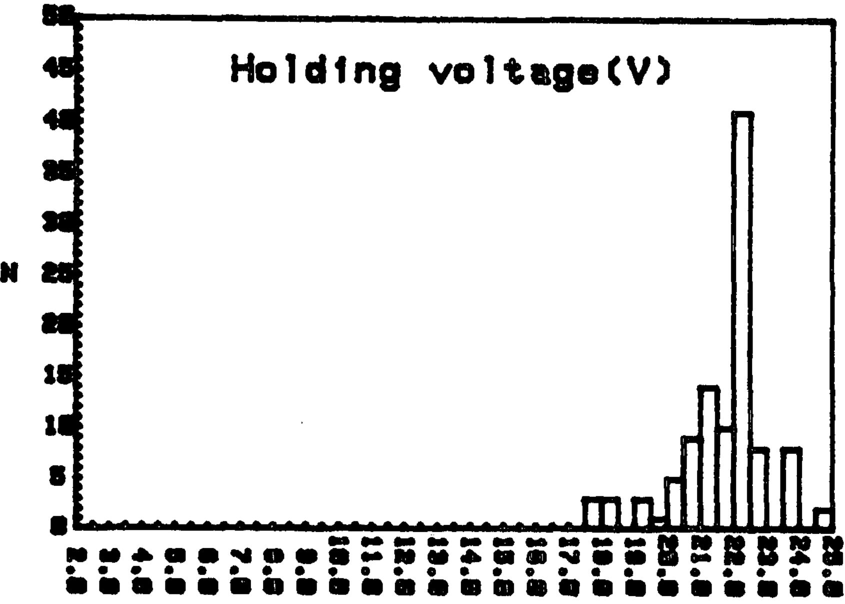
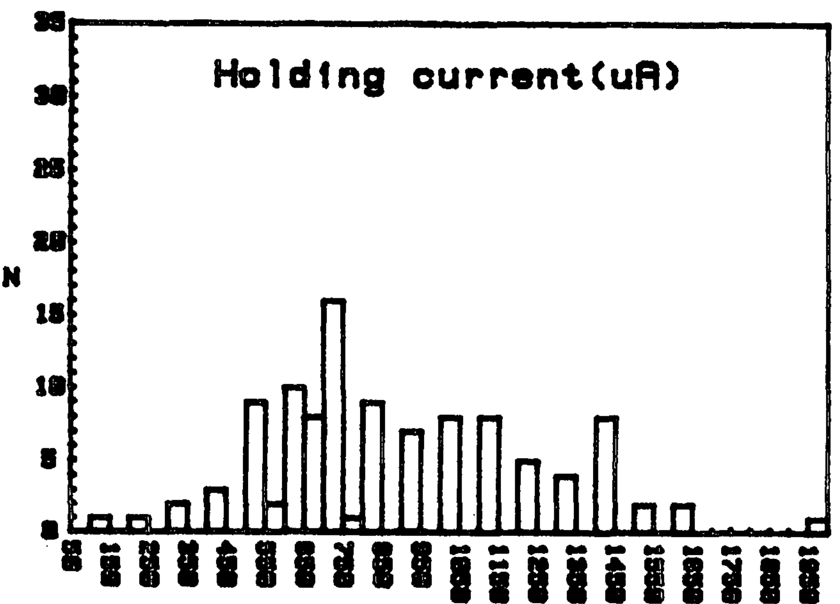
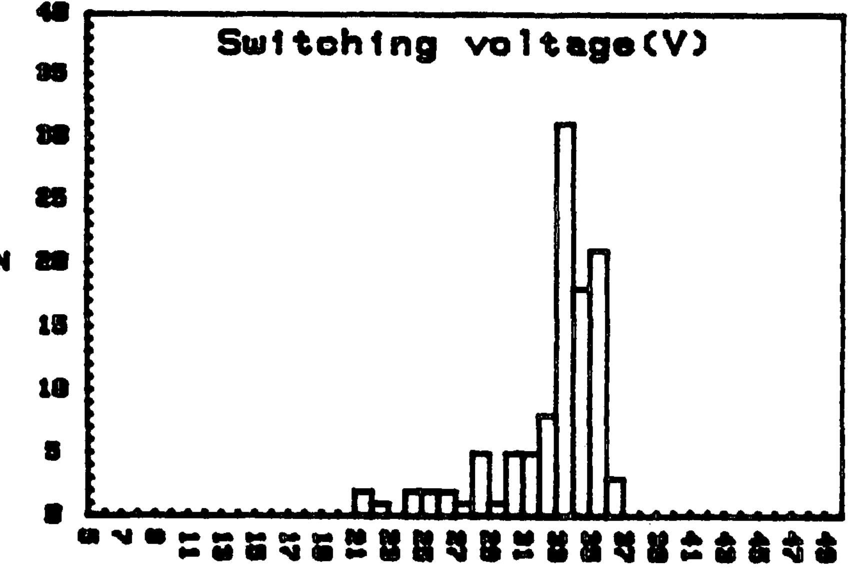


Fig. D8







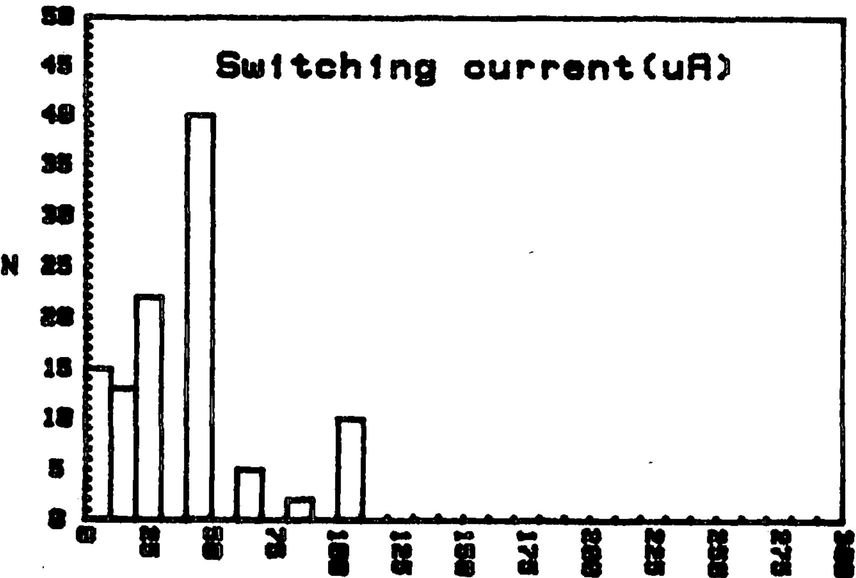


Fig. D9

Parameters	V_s(Volts)			V_h(Volts)			I_s(mA)			I_h(mA)		
Device Area	$\hat{V}_s$	Std. dev	Conf. intv	$\hat{V}_h$	Std. dev	Conf. intv	$\hat{I}_s$	Std. dev	Conf. intv	$\hat{I}_h$	Std. dev	Conf. intv
200×200μm	28.63	4.41	27.58-29.66	5.45	0.94	5.23-5.67	0.031	0.060	0.016 -0.044	0.359	0.131	0.328 - 0.39
160×160μm	28.65	3.44	27.81-29.49	5.43	0.82	5.23-5.62	0.037	0.018	0.033 -0.042	0.602	0.917	0.579-0.625
100×100μm	28.55	3.14	27.85-29.24	5.81	0.85	5.62-6.00	0.051	0.0258	0.045-0.056	0.678	0.132	0.648-0.707
80×80μm	28.38	3.28	27.68-29.08	5.78	0.82	5.60-5.95	0.038	0.016	0.035-0.042	0.656	0.106	0.633-0.678
60×60μm	28.57	3.31	27.84-29.30	5.57	0.83	5.39-5.75	0.045	0.014	0.042-0.048	0.726	0.128	0.698-0.754
40×40μm	29.14	3.02	28.53-29.75	5.67	0.86	5.50-5.85	0.054	0.025	0.049-0.059	0.79	0.144	0.761-0.82
20×20μm	30.37	3.18	29.76-30.97	8.51	1.57	8.21-8.81	0.047	0.03	0.041-0.052	0.176	0.341	0.169-0.182
10×10μm	32.40	3.77	31.67-33.13	18.21	2.04	17.82-18.61	0.035	0.025	0.03-0.04	0.82	0.30	0.762-0.879
5×5μm	32.75	3.32	32.12-33.38	21.77	1.37	21.51-22.03	0.034	0.027	0.029-0.039	0.857	0.343	0.792-0.922

Switching parameters of nonisolated MISS measured on wafer no. 1

Junction Area = 240 × 240μm												
Parameters	V_s(Volts)			V_h(Volts)			I_s(μA)			I_h(μA)		
Device Area	$\hat{V}_s$	Std. dev	Conf. intv	$\hat{V}_h$	Std. dev	Conf. intv	$\hat{I}_s$	Std. dev	Conf. intv	$\hat{I}_h$	Std. dev	Conf. intv
160 × 160μm	13.49	2.92	12.50-14.48	4.76	0.65	4.54-4.98	28.2	8.99	25.1 -31.2	3202	170	262-378
80 × 80μm	24.51	3.92	20.39-28.62	5.06	0.18	4.87-5.25	9.36	4.48	4.32-14.4	612	144	461-764
60 × 60μm	27.53	3.76	25.11-29.94	5.46	0.40	5.20-5.72	7.01	3.77	4.58-9.44	783	257	618-949
40 × 40μm	29.82	3.41	27.38-32.26	5.94	0.31	5.72-6.16	2.33	1.50	1.26-3.41	1500	227	1340-1660
20 × 20μm	33.84	2.11	32.33-35.35	24.75	4.97	21.20-28.31	0.736	0.436	0.425-1.05	162	118	782-247
Junction Area = 200 × 200μm												
Device Area	$\hat{V}_s$	Std. dev	Conf. intv	$\hat{V}_h$	Std. dev	Conf. intv	$\hat{I}_s$	Std. dev	Conf. intv	$\hat{I}_h$	Std. dev	Conf. intv
100 × 100μm	15.52	2.66	14.26-16.79	4.92	0.39	4.73-5.11	18.0	13.3	16.6 -24.3	303	74.4	267-338

Switching parameters of an isolated MISS of wafer no. 1

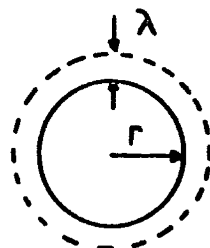
Junction Area = 160 × 160μm												
Parameters	V_s(Volts)			V_h(Volts)			I_s(μA)			I_h(μA)		
Device Area	$\hat{V}_s$	Std. dev	Conf. intv	$\hat{V}_h$	Std. dev	Conf. intv	$\hat{I}_s$	Std. dev	Conf. intv	$\hat{I}_h$	Std. dev	Conf. intv
100×100μm	18.44	2.59	16.77-20.10	5.14	0.47	4.84-5.44	12.5	3.42	10.3 -14.7	377	66.1	334-419
Junction Area = 120 × 120μm												
Device Area	$\hat{V}_s$	Std. dev	Conf. intv	$\hat{V}_h$	Std. dev	Conf. intv	$\hat{I}_s$	Std. dev	Conf. intv	$\hat{I}_h$	Std. dev	Conf. intv
100×100μm	5.1	0.561	3.78-6.49	4.43	0.39	3.46-5.40	8.79	1.87	4.14-13.4	94.1	17.8	49.9-138
80×80μm	19.02	5.36	17.75-20.28	5.21	1.44	4.87-5.55	11.0	24.0	5.35-16.7	389	174	348-430
40×40μm	23.82	4.97	20.27-27.37	5.81	0.50	5.46-6.17	7.8	9.3	1.15-14.5	1010	288	804-1210
20×20μm	29.67	3.10	27.28-32.06	23.00	4.84	19.27-26.72	1.14	0.48	0.77-1.51	191	96.8	117-266

Switching parameters of an isolated MISS of wafer no. 1

APPENDIX E

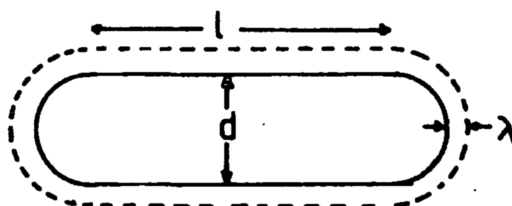
VARIATION OF SPREADING AREA WITH ELECTRODE PERIMETER

For a circular electrode of radius r the spreading area is



$$A_{sp} = \pi(r + \lambda)^2 - \pi r^2$$
$$= \pi\lambda^2 + 2\pi r\lambda \qquad E.1$$

For an elongated electrode of the same area, length l and width d as shown below



the spreading area is

$$A_{sp'} = 2\lambda l + \pi\lambda^2 + \pi d\lambda \qquad E.2$$

The spreading area as a function of l/d for contant electrode area is shown in table below.

l/d	$A_{sp'}/A_{sp}$
0	1
0.68	1.05
1.82	1.18
3.49	1.37
5.79	1.59
8.70	1.84
12.12	2.10

APPENDIX F

STABILITY OF A CIRCUIT CONTAINING NEGATIVE RESISTANCE

The Laplace transfer function of the small signal negative resistance circuit is shown in figure 7.4 can be written as,

$$\mathbf{H}(s) = \mathbf{L}\left[\frac{\delta V_d(t)}{\delta V_s(t)}\right] = \frac{R_d}{1 + sR_dC_d}\left\{(R_L + sL) + \frac{R_d}{1 + sR_dC_d}\right\}^{-1} \qquad F.1$$

where $\delta V_d(t)$ and $\delta V_s(t)$ are the perturbed voltages across the device and the supply respectively.

Simplifying,

$$\mathbf{H}(s) = \frac{R_d}{R_d + (R_L + sL)(1 + sR_dC_d)} \qquad F.1.1$$

$$= \frac{1}{1 + R_L/R_d + sL/R_d + sR_LC_d + s^2LC_d} \qquad F.1.2$$

Therefore,

$$\mathbf{H}(s) = \frac{1}{LC_d}\left\{s^2 + \frac{s(L + R_LR_dC_d)}{LC_dR_d} + \frac{R_d + R_L}{LC_dR_d}\right\}^{-1} \qquad F.2$$

The term in brackets { } can be factorised into,

$$(s + A)(s + B) = s^2 + s(A + B) + AB \qquad F.3$$

where,

$$AB = \frac{R_d + R_L}{LC_dR_d} \qquad F.3.1$$

and

$$A + B = \frac{L + R_d R_L C_d}{L C_d R_d}$$

then

$$B = \frac{L + R_d R_L C_d}{L C_d R_d} - A \qquad F.3.2$$

From $(F.3.2)$ and $(F.3.1)$

$$A\Big(\frac{L + R_d R_L C_d}{L C_d R_d} - A\Big) = \frac{R_d + R_L}{L C_d R_d}$$

$$A^2 - \Big(\frac{L + R_d R_L C_d}{L C_d R_d}\Big) A + \frac{R_d + R_L}{L C_d R_d} = 0$$

$$A = \frac{L + R_d R_L C_d}{2 L C_d R_d} \pm \frac{1}{2}\sqrt{\Big(\frac{L + R_d R_L C_d}{L C_d R_d}\Big)^2 - 4\frac{R_d + R_L}{L C_d R_d}} \qquad A.4$$

substituting $(F.4)$ into $(F.3.2)$,

$$B = \frac{L + R_d R_L C_d}{2 L C_d R_d} \mp \frac{1}{2}\sqrt{\Big(\frac{L + R_d R_L C_d}{L C_d R_d}\Big)^2 - 4\frac{R_d + R_L}{L C_d R_d}} \qquad F.5$$

Let

$$X = \frac{L + R_d R_L C_d}{2 L C_d R_d} \quad \text{and} \quad Y = \Big(\frac{L + R_d R_L C_d}{L C_d R_d}\Big)^2 - 4\frac{R_d + R_L}{L C_d R_d} \qquad F.6$$

then,

$$A = X + \frac{1}{2}\sqrt{Y} \quad \text{and} \quad B = X - \frac{1}{2}\sqrt{Y} \qquad F.7.1$$

or

$$A = X - \frac{1}{2}\sqrt{Y} \qquad \text{and} \qquad B = X + \frac{1}{2}\sqrt{Y} \tag{F.7.2}$$

The Laplace transfer function in $(F.2)$ can therefore be simplified to,

$$\mathbf{H}(s) = \frac{1}{LC_d}\{(s + A)(s + B)\}^{-1}$$

or

$$\mathbf{H}(s) = \frac{1}{LC_d}\left\{(s + X + \frac{1}{2}\sqrt{Y})(s + X - \frac{1}{2}\sqrt{Y})\right\}^{-1} \tag{F.8}$$

F.1 SOLUTIONS

In equation $F.8$, Y can have positive or negative values, and hence there are two possible solutions for the transfer function.

Case 1, Y positive.

The inverse Laplace transfer function in $F.8$ can be written as,

$$\frac{\delta V_d(t)}{\delta V_s(t)} = \mathbf{L}^{-1}\mathbf{H}(s) = \frac{1}{LC_d\sqrt{Y}}\left\{e^{-(X + \frac{1}{2}\sqrt{Y})t} - e^{-(X - \frac{1}{2}\sqrt{Y})t}\right\} \tag{F.9}$$

X As we can see, if both $(X + \frac{1}{2}\sqrt{Y})$ and $(X - \frac{1}{2}\sqrt{Y})$ in $(F.9)$ are positive, the voltage across the device, $\delta V_d(t)$, decreases with time (i.e. it is damped) and the

circuit is in a stable condition (figure 7.5(b)). However, if either $(X + \frac{1}{2}\sqrt{Y})$ and $(X - \frac{1}{2}\sqrt{Y})$ is negative, $V_d(t)$ grows exponentialy, and the circuit is unstable (figure 7.5(a)).

Case 2, Y negative.

Equation $F.9$ can be rearranged as,

$$\frac{\delta V_d(t)}{\delta V_s(t)} = \frac{-2}{LC_d\sqrt{Y}} e^{-Xt} \left(\frac{\epsilon^{+\frac{1}{2}\sqrt{Y}t} - \epsilon^{-\frac{1}{2}\sqrt{Y}t}}{2} \right)$$

$$= \frac{-2}{LC_d\sqrt{Y}} \epsilon^{-Xt} \sinh\left(\frac{\sqrt{Y}t}{2}\right) \qquad F.10$$

and for Y negative, $\sqrt{Y}$ can be written as $j\sqrt{Y}$, and from the trigonometric relation $\sinh j(at) = j\sin(at)$, equation $F.10$ can be written as,

$$V_d(t) = j\frac{2}{LC_d\sqrt{Y}} \epsilon^{-Xt} \sin\left(\frac{\sqrt{Y}t}{2}\right) \qquad F.11$$

From $(F.11)$ it is clear that if X is positive (poles in the left half plane) $V_d(t)$ is a damped oscillation as shown in figure 7.5(d), and if X is negative (poles in the right half plane) the voltage across the device is a growing oscillation, as shown in figure 7.5(c). That is to say the, circuit will be stable if X is positive and unstable if X is negative. However, if $X = 0$, $V_d(t)$ is a constant oscillation.

F.2 EVALUATION OF STABILITY CONDITIONS

The circuit parameters which determine the stability of the NDR circuit can be obtained by evaluating the stability conditions of the equations $F.9$ and $F.11$. We will first consider Case 2 and equation F.11 in which Y is negative.

Case 2, Y negative.

We have shown that the circuit is unstable if X is negative, and from ($F.6$), X can be expressed as,

$$X = \frac{1}{2C_d R_d} + \frac{R_L}{2L} \qquad F.12$$

a) Assuming C_d is positive and the device resistance is negative, $R_d = -|R_d|$, then ($F.12$) becomes,

$$X = \frac{-1}{2C_d|R_d|} + \frac{R_L}{2L}$$

Therefore, the circuit is **unstable** if,

$$\frac{1}{2C_d|R_d|} > \frac{R_L}{2L} \qquad F.13$$

or

$$R_L < \frac{L}{C_d|R_d|} \qquad F.13.1$$

and the circuit is **stable** if,

$$R_L > \frac{L}{C_d|R_d|} \qquad F.13.2$$

b) Assuming that the device capacitance is also negative, $C_d = -|C_d|$ and $R_d = -|R_d|$,

Then

$$X = \frac{1}{2|C_d||R_d|} + \frac{R_L}{2L}$$

is always positive. Therefore the circuit is always stable if C_d is negative.

For C_d positive the above conditions (equation $F.13.1$ and $F.13.2$) are true for X, where Y is negative. Therefore must also consider the circuit parameters required to make Y negative. The expression for Y in equation $F.6$ can be writen as,

$$Y = \frac{L^2 + 2LR_dR_LC_d + R_d^2R_L^2C_d^2 - 4(R_d + R_L)(LC_dR_d)}{L^2C_d^2R_d^2}$$

$$= \frac{L^2 + (R_dR_LC_d)^2 - 2R_LC_dR_dL - 4R_d^2C_dL}{(LC_dR_d)^2} \qquad F.15$$

Substituting $R_d = -|Rd|$ into equation $F.15$,

$$Y = \frac{L^2 + |R_d|^2(R_LC_d)^2 - 2R_LC_d|R_d|L - 4|R_d|^2C_dL}{(LC_d|R_d|)^2} \qquad F.16$$

or

$$Y = \frac{(L + |R_d|R_LC_d)^2 - 4|R_d|^2LC_d}{(LC_d|R_d|)^2} \qquad F.17$$

Then Y will be negative if,

$$4|R_d|^2 LC_d > (L + |R_d|R_L C_d)^2$$

or

$$2|R_d|\sqrt{LC_d} > L + |R_d|R_L C_d$$

or

$$R_L < 2\sqrt{\frac{L}{C_d}} - \frac{L}{|R_d|C_d} \qquad F.18$$

Therefore, the condition for Y $-ve$ and X $+ve$ if C_d $+ve$, are given by equation $F.13.1$ (condition for X) and in $F.18$ (condition for Y). If $L = 10\mu$H, $C_d = 100$pF, and $|Rd| = 10$kΩ then the condition for X is $R_L < 10\Omega$, and the condition for Y is $R_L < 600\Omega$.

Now let us see what will happen if C_d is negative. By substituting $C_d = -|Cd|$ in equation ($F.16$), Y can be expressed as,

$$Y = \frac{L^2 + |R_d|^2 R_L^2 |C_d|^2 - 2R_L|C_d||R_d|L + 4|R_d|^2|C_d|L}{(L|C_d||R_d|)^2} \qquad F.19$$

As we can see Y will only be negative if,

$$2R_L|Cd||Rd|L > L^2 + |Rd|^2 R_L^2 |Cd|^2 + 4|Rd|^2|Cd|L \qquad F.20$$

Using the previous values of L, $|C_d|$, and $|Rd|$, for $R_L = 1$kΩ, 1MΩ, and 100MΩ the left-hand side (L.H.S) is always less than the right-hand side (R.H.S.) as shown below.

$R_L(\Omega)$	L.H.S.	R.H.S.			
10^3	2×10^{-8}	10^{-6}	L.H.S. < R.H.S.	then	$Y \Longrightarrow +ve$
10^6	2×10^{-5}	10^0	L.H.S. < R.H.S.	then	$Y \Longrightarrow +ve$
10^8	2×10^{-3}	10^4	L.H.S. < R.H.S.	then	$Y \Longrightarrow +ve$

This shows that Y is never negative if C_d is negative. Therefore there is no oscillation condition for Y negative (case 2) if C_d negative.

Case 1, Y positive.

For the case of Y positive we have shown that the circuit is unstable if either $(X + \frac{1}{2}\sqrt{Y})$ or $(X - \frac{1}{2}\sqrt{Y})$ is negative.

a) Assuming C_d is positive,

$$X = \frac{-1}{2C_d|R_d|} + \frac{R_L}{2L}$$

From $(F.17)$ Y is positive if,

$$R_L > 2\sqrt{\frac{L}{C_d}} - \frac{L}{|R_d|C_d} \qquad F.21$$

The first term $(X + \frac{1}{2}\sqrt{Y})$ will be negative if X is negative (Y is positive by definition), and X will be negative if,

$$R_L < \frac{L}{C_d|R_d|} \qquad F.22$$

Now, what is the practical condition to make the L.H.S of equation $F.22$ less than the R.H.S.?. Using the values of $C_d = 100\text{pF}$, $|R_d| = 10\text{k}\Omega$ we can see from the table below that X will only be negative if L is very large. But in the practical measuring circuit $L \ll 0.1\text{mH}$, so the L.H.S is always greater than the R.H.S, that is to say, X is always positive for Y positive.

$L(H)$	L.H.S.	R.H.S.			
10^{-1}	10^4	10^5	L.H.S. < R.H.S.	then	$X \Longrightarrow -ve$
10^{-2}	10^4	10^4	L.H.S. = R.H.S.	then	$X \Longrightarrow -ve$
10^{-3}	10^4	10^3	L.H.S. > R.H.S.	then	$X \Longrightarrow +ve$
10^{-4}	10^4	10^2	L.H.S. > R.H.S.	then	$X \Longrightarrow +ve$

The second term $(X - \frac{1}{2}\sqrt{Y})$ will be negative if,

$$\frac{1}{2C_d|R_d|} + \frac{1}{2}\sqrt{Y} > \frac{R_L}{2L}$$

and

$$\sqrt{Y} > \frac{R_L}{L} - \frac{1}{C_d|C_d|R_d|}$$

then

$$Y > (\frac{R_L C_d|R_d| - L}{LC_d|R_d|})^2 \qquad F.23$$

Substituting Y from $F.17$ into $F.23$,

$$\frac{(L + |R_d|R_L C_d)^2 - 4|R_d|^2 L C_d}{(L C_d |R_d|)^2} > \frac{(R_L C_d |R_d|)^2 - 2L R_L C_d |R_d| + L^2}{(L C_d |R_d|)^2}$$

$$4L|R_d|R_L C_d > 4L|R_d|^2 C_d$$

or

$$R_L > |R_d| \qquad F.24$$

Therefore for the measuring circuit where L is very small ($\ll 0.1$mH), the term $(X - \frac{1}{2}\sqrt{Y})$ will be negative (unstable condition) if $R_L > |R_d|$, and the term $(X + \frac{1}{2}\sqrt{Y})$ is always positive. Hence, for C_d positive the condition for stability is given by expression $F.25$,

$$\frac{L}{|R_d|C_d} < R_L < |R_d| \qquad F.25$$

b) Assuming C_d is negative,

Then

$$X = \frac{1}{2|C_d||R_d|} + \frac{R_L}{2L}$$

$$Y = \frac{L^2 + (|R_d|R_L|C_d|)^2 - 2(|R_d|R_L|C_d|L + 4|R_d|^2 L|C_d|}{(L|C_d||R_d|)^2}$$

$$Y = \frac{(L - |R_d|R_L|C_d|)^2 + 4|R_d|^2 L|C_d|}{(L|C_d||R_d|)^2} \qquad F.26$$

The circuit is unstable if either $(X + \frac{1}{2}\sqrt{Y})$ or $(X - \frac{1}{2}\sqrt{Y})$ is negative,

$$(X + \frac{1}{2}\sqrt{Y}) = \frac{1}{2|C_d||R_d|} + \frac{R_L}{2L} + \frac{1}{2}\sqrt{Y} \qquad F.27$$

where Y is positive by definition. Therefore $(X + \frac{1}{2}\sqrt{Y})$ always positive.

$$(X - \frac{1}{2}\sqrt{Y}) = \frac{1}{2|C_d||R_d|} + \frac{R_L}{2L} - \frac{1}{2}\sqrt{Y} \qquad F.28$$

so $(X + \frac{1}{2}\sqrt{Y})$ will be negative if $\frac{1}{2}\sqrt{Y} > X$ or $Y > 4X^2$

$$\frac{(L - |R_d|R_L|C_d|)^2 + 4|R_d|^2 L|C_d|}{(L|C_d||R_d|)^2} > \frac{4(L + |R_d|R_L|C_d|)^2}{4(L|C_d||R_d|)^2}$$

$$4|R_d|^2 L|C_d| > 4L|R_d|R_L|C_d|$$

or

$$|R_d| > R_L \qquad F.29$$

Therefore, if C_d is negative the circuit will only be unstable for $R_L < |R_d|$

F.3 CONCLUSIONS

1. The negative resistance circuit with C_d positive is unstable for all values of R_L.
2. The circuit is unstable for any $R_L(< R_d)$ with the rising exponential type of response irrespective of the sign of C_d.
3. The circuit is stable if $R_L > R_d$ and C_d is negative.