Analogue filter networks: developments in theory, design and analyses

Sewell, J.I.

ANALOGUE FILTER NETWORKS: DEVELOPMENTS IN THEORY, DESIGN AND ANALYSIS

by

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for admission to the degree of

Doctor of Science

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Dedication

"Have you learned lessons only of those who admired you, and were tender with you, and stood aside for you? Have you not learned great lessons from those who braced themselves against you, and disputed the passage with you?"

Walt Whitman, 1819-1892

This work is dedicated to the female members of my family:

The late Dorothy Sewell - my mother: though denied personal access to scholarship, began my "disputed passage".

Ruth Sewell - my wife: having an appreciation of scholarship, maintains my "disputed passage".

Anna and Deborah Sewell - my daughters: as yet without an understanding of scholarship, seem set to continue my "disputed passage".

CONTENTS

1. Curriculum Vitae

CURRICULUM VITAE

1. General

Name:	JOHN ISAAC SEWELL
Date and Place of Birth:	13 May 1942. Kirkby Stephen, Cumbria.
Nationality:	British
Marital Status:	Married, two children
Present Address:	16 Paterson Place, Bearsden, Glasgow, G61 4RU.

2. General Education

Year	School
1947 - 51	Winton Primary School, Cumbria.
1951 - 53	Soulby Primary School, Cumbria.
1953 - 55	Appleby Grammar School, Cumbria.
1955 - 60	Kirkby Stephen Grammar School, Cumbria.

Examinations Taken

G.C.E. 'O' Level 1958	G.C.E. 'A' Level 1960
Passes in: Mathematics	Passes in: Physics
Physics	Chemistry
Chemistry	Mathematics
English Literature	
History	
Geography	
1959 English language	
French	

3. University Education

Date	College
October 1960 - June 1962	Sunderland Technical College University of Durham.
October 1962 - June 1963	King's College, University of Durham.
October 1963 - September 1966	University of Newcastle-upon-Tyne

Examinations taken

June 1963	-	B.Sc. in Electrical Engineering, Upper Second Class Honours.
October 1966	-	Ph.D. in Electrical Engineering. Title of thesis 'The application of Analogue Computing Techniques to the design of Active Filters'. The work was supported by an S.R.C. Studentship held for three years.

4. **Employment History**

Dates	
July - October 1963	System Computers Ltd., Gateshead. Research Engineer. Development of transistor circuitry for analogue computers.
October 1966 - September 1968	University of Newcastle-upon-Tyne. Senior Research Associate. The work was concerned with the application of digital computers in active network analysis and synthesis.
October 1968 - September 1976	University of Hull. Lecturer in the Department of Electronic Engineering.
October 1976 - September 1984	University of Hull Senior Lecturer in the Department of Electronic Engineering.
October 1984 - September 1985	University of Hull Reader in Integrated Electronic Systems, Department of Electronic Engineering.
October 1985 - present time	University of Glasgow. Professor of Electronic Systems, Department of Electronics and Electrical Engineering.
September 1990 - 1993	University of Glasgow Dean of the Faculty of Engineering.
May 1995 - July 1995	University of Toronto Visiting Research Professor.

5. **Professional Qualifications and Distinctions**

Fellow of the Institution of Electrical Engineers, Chartered Engineer.
Fellow of the Institute of Electrical and Electronic Engineers.
J.J. Thomson Premium Award, Institution of Electrical Engineers, 1992.

6. **University Teaching Duties**

1968-1985	Third Year Course	- Telecommunications 40 hrs/year
1969-1985	Fourth Year Courses	- Passive Network Synthesis 20 hrs/year
		- Active Network Synthesis 20 hrs/year
1968 - 1974) 1975 - 1978) 1984 - 1985)	Second Year Laboratory	- 156 hrs/year
1979 - 1983	First Year Laboratory	- 120 hrs/year
1968 - 1971) 1975 - 1976)	First Year Problems Class	- 24 hrs/year
1985 - 1986	Fourth Year Course - Control	- 20 hrs/year
	Laboratory	- 30 hrs/year
1986 - 1989	First Year Course - Electrical Engineering	- 20 hrs/year
1986 - 1994	Fourth Year Course- Signal Processing	- 20 hrs/year
	Laboratory	- 12 hrs/year
1989 - 1993	Second Year Course- Electrical Engineering	- 20 hrs/year
1988 - 1990	Engineering Applications Laboratory	- 4 hrs/year
1968 - 1990	Tutorials	
1969 - 1990	Final Year Project Supervision	

7. **University Research Duties**

Supervisor of the following research students:

C. Fridas	-	M.Sc. awarded 1973
		Ph.D. " 1976
L.G. Grant	-	Ph.D. " 1978
F.G.A. Coupe	-	Ph.D. " 1980
C. Lau	-	M.Sc. " 1982
C.K. Pun	-	Ph.D. " 1987
L.B. Wolovitz	-	Ph.D. " 1987
R.K. Henderson	-	Ph.D. " 1990
Li Ping	-	Ph.D. " 1990
D.H. Hossack	-	Ph.D. " current

Lu Yue	-	Ph.D.	"	current
Shang Z	-	Ph.D.	"	current

Supervisor of SERC computer programmer, P. Garbett	1981 - 82
Supervisor of research assistant, J. Barrass,	1983 - 84
Supervisor of post-doctoral research assistant D.J.Gilbert	1983 - 86
Supervisor of " " " " B.J.Wishart	1988 - 89
Supervisor of " " " " R.K.Henderson	1989 - 90

8. **University Departmental Duties**

Joint development of Second Year Electronics Laboratory.

Joint development of Second Year Computer Aided Design Course.

Colloquium Organisation 1969 - 71

Third Year Examination Organisation 1969 - 71

Timetable Organisation 1970 - 71

Departmental Admissions 1971 - 73

First Year Syllabus Committee 1971 - 73

Departmental Publicity (Admissions, Gouriet lectures, etc) 1973 - 80

Steering Committee for Degree in Mathematics and Electronic Systems 1973 - 79

Internal Examiner for Higher Degrees - Ph.D. 1970
- M.Sc. 1973

Chairman of Course Development Committee 1978 - 79

Joint development of First Year Electronics Laboratory

Steering Committee for Science Research Council Interactive Computing Facility Minicomputer Application 1980 - 81

Fourth Year Examination Organisation 1980 - 83

Enhanced Degree Coordinator 1983 - 85

Acting Head of Department August - November 1989

Convenor of Electronics and Electrical Engineering Advisory Committee 1987 - 1993.

Convenor of SWOT Committee (Strengths, Weaknesses, etc.) 1988-90.

Degree Accreditation 1987 - 1992.

Convenor of Rankine VAX Computer Management Committee 1986 - 89

Convenor of Publicity Committee 1985 - 89

Assessor of First Year Research Students 1986 - 91

Convenor of Ph.D Oral Examinations 1985 - present

Committee for negotiations with Paisley College of Technology 1989 - 90

9. **University Duties**

Science Safety Precautions Committee 1974 - 1976

Member of the Board of the Faculty of Science 1975 - 1977

Member of the Faculty of Science Planning Committee 1975 - 1977

Member of the Language Teaching Centre Committee 1978 - 1981

Member of the Computer Users Committee 1980 - 1985

Member of Working Party on University Computer Enhancement 1982

Member of the Board of the Faculty of Science 1983 - 1985

Member of Computer Evaluation Committee 1984

Member of various Computer Evaluation Committees 1986 - 1988

Member of Computer Communications sub-committee 1986 - 1989

Member of Faculty of Engineering Publicity Committee 1988 - 90

Convenor of Faculty of Engineering Computer Committee 1987 - 90

Member of Senate Business Committee 1989 - 90

Member of Committee of Review for Faculty Engineering 1987 - 90

10. **Published Work**

1. "Table for the voltage transfer functions of single amplifier double ladder feedback systems", Electronics Letters, May 1965, Vol.1, No.3, pp 70-71, (with A.G.J.Holt).

2. "Active RC filters employing a single operational amplifier to obtain biquadratic responses", Proc. I.E.E., December 1965, Vol. 112, No.12, pp.2227-2234, (with A.G.J.Holt)

3. "Synthesis of multi-loop feedback systems", I.E.E. Colloquium on Active Filters, London, January 1966, (with A.G.J. Holt).

4. "Table for the voltage transfer functions of single amplifier double ladder parallel feedback systems", I.E.E.E. Trans. C.T., September 1966, Vol. CT-13, pp.326-328, (with A.G.J. Holt).

5. "The Computer in electronics, Part I", Design Electronics, Oct. 1967, Vol.5, No.1, pp. 34-36, (with J.K. Fidler).

6. "The computer in electronics, Part II", Design Electronics, Nov. 1967, Vol.5, No.2, pp. 38-41, (with J.K. Fidler).

7. "Correction function techniques", I.E.E. International Conference on Computer Aided Design, Southampton, April 1969, I.E.E. Conference Publication No. 51, pp.515-526, (with C. Nightingale).

8. "Matrix tables for the generalised 5-terminal amplifier", The Radio and Electronic Engineer, April 1969, Vol. 37, No.4, pp.247-55, (with F.W.Stephenson).

9. "Synthesis of multi-loop feedback systems, Part I, International Journal of Control, May 1969, Vol.9, No.5, pp. 487-497, (with A.G.J. Holt).

10. "Synthesis of multi-loop feedback systems, Part II", International Journal of Control, May 1969, Vol.9, No.5, pp.499-508, (with A.G.J. Holt).

11. "A simple method for producing floating inductors", Proc. I.E.E.E. December 1969, Vol. 57, No.12, pp. 2155-2156.

12. "Accumulant theory and applications", International Journal of Control, March 1970, Vol. 11, No.3, pp.479-488.

13. "Synthesis of active devices", International Journal of Electronics, December 1970, Vol.29, No.6, pp. 501-511.

14. "A synthetic analysis of general active networks", I.E.E. International Conference on Computer Aided Design, Southampton, April 1972. I.E.E. Conference Publication No.86, pp.12-18, (with I. Walker).

15. "A course in computer-aided electronic circuit design for undergraduates", Computer Aided Design, April 1972, Vol 4, No.3, pp. 135-137, (with A.G. Martin).

16. "General synthetic analysis of active networks", Proc. Second International Symposium on Network Theory, Herceg-Novi, Yugoslavia, July 1972, pp. 61-69, (with C. Fridas).

17. "The multiterminal active transformer", International Journal of Control, July 1972, Vol. 16, No.1, pp. 171-175.

18. "Active circulator systems", International Journal of Electronics, December 1972, Vol.33, No.6, pp.677-679.

19. "Computer-aided engineering education", Proc. Conference on the Teaching of Electronic Engineering in Degree Courses, University of Hull, April 1973, pp.17/1 - 17/16. (with A.G. Martin and D. Midgley).

20. "Symbolic analysis for computer-aided circuit design - The interpolative approach", I.E.E.E. Trans. C.T., November 1973 Vol. CT-20, No.6, pp. 738-741. (with J.K. Fidler).

21. "A partition method for symbolic network analysis", I.E.E. Colloquium on Computer Aided Circuit Design, Colloquium Digest 1974 - 4, pp. 7/1 - 7/2 March 1974, (with C. Fridas).

22. "Digital realisation of linear and parametric networks", I.E.R.E. Colloquium on Signal Processing in Feedback Control Systems, London, April 1974, (with F.G.A. Coupe).

23. "Symbolic analysis of networks by partitioned polynomial interpolation", I.E.E.E. Trans. CAS, May 1974, Vol.CAS-21 No.3, pp. 345-347, (with C. Fridas).

24. "Correction to symbolic analysis for computer-aided circuit design - the interpolative approach", I.E.E.E. Trans. CAS, May 1974, Vol. CAS-21, No.3, P.462, (with J.K.Fidler).

25. "The design of variable immittance amplifiers", I.E.E. Colloquium on Amplifier Design - Theory and Practice, Colloquium Digest 1974 - 24, pp.11/1 - 11/2, May 1974, (with J.A. Neill and F.G.A. Coupe).

26. "Interpolative analysis for computer aided design",Proc. Summer School on Circuit Theory 1974, Prague, September 1974, Vol.2, pp. 217 - 223, (with C. Fridas).

27. "An adaptive electronic circulator for use in telephones", I.E.E.E. Trans. COM, July 1975, Vol. COM-23, No.7, pp. 728-731, (with R. Lodge).

28. "Error estimation and improvement in interpolative symbolic network analysis", Proc. Third International Symposium on Network Theory, Split, Yugoslavia, September 1975, pp. 121-129, (with C. Fridas).

29. "Network partition methods for use in symbolic analysis by interpolation", Proc. 1976 I.E.E.E. International Symposium on Circuits and Systems, Munich, April 1976, pp. 45-48 (with C. Fridas).

30. "A theory of equivalent active networks", Proc. 1976 I.E.E.E. International Symposium on Circuits and Systems, Munich, April 1976, pp. 497-500 (with L.G.Grant).

31. "A theory of equivalent active networks", I.E.E.E. Trans. CAS, June 1976, Vol. CAS-23, No.6, pp.350-354, (with L.G.Grant).

32. "Network partition methods for use in symbolic analysis by interpolation", Computer Aided Design, July 1976, Vol. 8, No.3. pp. 157-164, (with C. Fridas).

33. "Symbolic network sensitivities using partition methods", Int. Journal of Electronics, July 1976, Vol.41, No.1, pp.25-32, (with C. Fridas).

34. "Partitioned transformations in equivalent active network theory", Proc. 1976 European Conference on Circuit Theory and Design, Genoa, September 1976, pp. 232-238, (with L.G. Grant).

35. "On the evaluation of sensitivity polynomials in active equivalent network theory", Proc. I.E.E.E. Conference on Computer Aided Design of Electronic and Microwave Circuits and Systems, Hull, July 1977, pp.84-89, (with L.G. Grant).

36. "Sensitivity minimisation and partitioned transformations in active equivalent networks",I.E.E. Journal on Electronic Circuits and Systems, March 1978, Vol.2, No.2, pp.33-38, (with L.G.Grant).

37. "On sensitivity theorems in active equivalent network theory", Proc. 1978 I.E.E.E. International Symposium on Circuits and Systems, New York, May 1978, pp.1060-1063, (with J.Dunning-Davies and F.D. Faulkner).

38. "Some further sensitivity theorems in active equivalent network theory", I.E.E. Journal on Electronic Circuits and Systems, November 1978, Vol.2, No.6, pp. 193-198, (with J.Dunning-Davies and F.D. Faulkner).

39. "An improved adaptive electronic circulator for telephone applications", I.E.E.E. Trans. COM, August 1979, Vol. COM-27, No.8, pp. 1218-1224 (with H. Gazioglu and D.A. Homer).
40. "An adaptive electronic circulator for telephone hybrid applications", Proc. Fourth International Symposium on Network Theory, Ljubljana, September 1979, pp. 369-376, (with H. Gazioglu and D.A. Homer).

41. "Analysis of active switched-capacitor networks", Proc. I.E.E.E. February 1980, Vol. 68, No.2, pp. 292-293.

42. "A degree enhancement scheme in electronic engineering", Proc. Conference on Electronic Engineering in Degree Courses - Teaching for the 80's, University of Hull, April 1980, pp.21/1 -21/11.

43. "Inclusion of amplifier finite gain and bandwidth in analysis of switched-capacitor filters", Electronics Letters, June 1980, Vol.16, No.12, pp.462-463, (with C. Lau).

44. "Digital active network analysis", Proc. I.E.E., Part G, Electronic Circuits and Systems, August 1980, Vol.127, No. 4, pp. 181-186 (with F.G.A. Coupe).

45. "A degree enhancement scheme in electronic engineering", Int. J. Elect. Enging. Educ., January 1981, Vol.18, pp. 29-34.

46. "Computer analysis of switched-capacitor filters", I.E.E. Colloquium on Electronic Filters, Colloquium Digest pp. 4/1 - 4/8, April 1981, (with C. Lau).

47. "General computer analysis of switched-capacitor networks including non-ideal amplifiers", Proc. I.E.E.E. International Symposium on Circuits and Systems, Rome, May 1982, pp.17-20,(with C. Lau and N.J.Cutland).

48. "CAD tools for switched capacitor filter design", Proc. I.E.E.E. Workshop on Design and Fabrication of Integrated Circuit Filters, London, September 1982, pp. B1-B47.

49. "Compact matrix scheme for use in computer analysis of switched capacitor networks", Electronics Letters, September 1982, Vol. 18, No. 19, pp. 840-841, (with C. Lau).

50. "Software for switched capacitor filter design", I.E.R.E. Colloquium on Analogue Filters, Colloquium Digest 2pp. November 1983.

51. "Interpolative analysis of switched capacitor networks", I.E.E. Colloquium on Design Software, Colloquium Digest pp. 6/1 - 6/7, January 1984, (with D.G. Johnson and A.D. Meakin).

52. "Some improvement schemes for the interpolative symbolic analysis of switched capacitor networks", Proc. I.E.E.E. International Symposium on Circuits and Systems, Montreal, May 1984, 4pp, (with D.G. Johnson).

53. "Improved z plane polynomial interpolative analysis of switched capacitor networks", I.E.E.E. Trans. CAS, July 1984 Vol. CAS-31, No.7, pp. 666-668, (with D.G. Johnson).

54. "Analysis of active switched-capacitor networks", selected reprint in MOS Switched-Capacitor Filters: Analysis and Design, I.E.E.E. Press, 1984, pp. 85-86.

55. "On time-sharing and noise minimisation in switched-capacitor filters", I.E.E. Saraga Colloquium on Electronic Filters, Colloquium Digest, 6pp, May 1985, (with M. Powell and R.C.J. Taylor).

56. "Switched-capacitor filter transformations and optimisation", I.E.E. Saraga Colloquium on

Electronic Filters, Colloquium Digest, 5pp, May 1985, (with D.J. Gilbert).

57. "Symbolic analysis of ideal and non-ideal switched capacitor networks", Proc. I.E.E.E. International Symposium on Circuits and Systems, Kyoto, June 1985, pp.1165-1168 (with C.K. Pun).

58. "On the generation of equivalent switched capacitor networks", Proc. European Conference on Circuit Theory and Design, Prague, September, 1985 pp.697-700 (with D.J. Gilbert).

59. "Techniques for improving the efficiency of analysis of software for large switched-capacitor networks, Proc. 28th Midwest Symposium on Circuits and Systems, Louisville, August 1985, pp.390-393 (with A.D. Meakin and L.B. Wolovitz).

60. "Efficient computer techniques for the exact analysis of all non-ideal effects of switched-capacitor networks in the time domain", Proc. I.E.E.E. International Symposium on Circuits and Systems, San Jose, May 1986, pp. 373-376, (with L.B. Wolovitz).

61. "Application of equivalent network theory to strays insensitive switched capacitory filters", I.E.E Saraga Colloquium on Electronic Filters, Colloquium Digest pp. 3/1 - 3/8, May 1986, (with D.J. Gilbert).

62. "Multiphase equivalence theory for switched capacitor networks", Proc. 29th Midwest Symposium on Circuits and Systems, Lincoln, Na., August 1986, pp. 801 - 806, (with D.J. Gilbert).

63. "Noise analysis of switched capacitor networks in symbolic form", Proc. 29th Midwest Symposium on Circuits and Systems, Lincoln, Na., August 1986, pp 807 - 810, (with C.K. Pun and A.G. Hall).

64. "The LUD approach to switched-capacitor filter design", I.E.E. Saraga Colloquium on Electronic Filters, Colloquium Digest pp. 7/1 - 7/7, March 1987, (with Li Ping).

65. "Optimisation of switched capacitor networks using equivalence transformations", Proc. I.E.E.E. International Symposium on Circuits and Systems, Philadelphia, May 1987, pp. 730 - 732 (with D.J. Gilbert and G.L. Holden).

66. "The LUD approach to switched-capacitor filter design", I.E.E.E. Trans. CAS, Dec. 1987, Vol. CAS-34, No.12, pp.1611 - 1614 (with Li Ping).

67. "The SCNAP series of software for switched capacitor circuit design", I.E.E. Colloquium on Analogue IC Design, London, November 1987 pp. 10/1 - 10/5.

68. "Matrix methods for switched capacitor filter design", Proc. I.E.E.E. International Symposium on Circuits and Systems, Helsinki, June 1988, pp. 1021 - 1024 (with Li Ping and R K Henderson).

69. "General analysis of large linear switched capacitor networks", Proc. I.E.E. Part G, Electronic Circuits and Systems, June 1988, Vol. 135, No.3, pp. 119 - 124, (with L.B. Wolovitz).

70. "Filter realisation by passive network simulation", Proc. I.E.E. Part G, Electronic Circuits and Systems, August 1988, Vol. 135, No.4, pp. 167 - 176 (with Li Ping).

71. "Design and Optimisation of GaAs switched capacitor filter", I.E.E. Saraga Colloquium on Electronic Filters, London, May 1988, pp. 1/1 - 1/10 (with D.G.Haigh, C. Toumazou, S.J. Harrold).

72. "PANDDA : A program for advanced network design: digital and analogue", I.E.E. Saraga Colloquium on Electronic Filters, London, May 1988, pp. 4/1 - 4/8. (with R.K. Henderson and Li Ping).

73. "Digital filter realisation by passive network simulation", I.E.E. Saraga Colloquium on Electronic Filters, London, May 1989, pp. 8/1 - 8/8 (with Li Ping).

74. "On low sensitivity/noise digital filter structures", Proc. I.E.E.E. International Conference on Acoustics, Speech and Signal Processing, Glasgow, May 1989, pp. 845 - 848 (with Li Ping).

75. "A new filter approximation and design algorithm", Proc. I.E.E.E. International Symposium on Circuits and Systems, Portland, May 1989, pp. 1063 - 1066, (with Li Ping and R.K. Henderson).

76. "Design and optimisation of a GaAs switched capacitor filter", Proc. I.E.E.E. International Symposium on Circuits and Systems, Portland, May 1989, pp. 1449 - 1454 (with D.G. Haigh, C. Toumazou, S.J. Harrold and K. Steptoe).

77. "A design algorithm for all-pass delay equalisers," I.E.E. Saraga Colloquium on Electronic Filters, London, June 1989, pp. 11/1 - 11/8 (with R.K. Henderson).

78. "The TWINTOR in bandstop switched-capacitor ladder filter realisation," I.E.E.E. Trans. CAS, July 1989, Vol. CAS-36, No.7, pp. 1041 - 1044 (with Li Ping).

79. "The TWINTOR in bandstop switched-capacitor ladder filter realisation", Proc. European Conference on Circuit Theory and Design, Brighton, September 1989, pp. 27 - 31 (with Li Ping).

80. "Design program for digital and analogue filters: PANDDA", Proc. European Conference on Circuit Theory and Design, Brighton, September 1989, pp. 289 - 293 (with Li Ping and R.K. Henderson).

81. "High performance filter networks and symmetric matrix systems", Proc. I.E.E., Part G, Circuits Devices and Systems, Dec. 1989, Vol. 136, No.6, pp. 327 - 336, (with Li Ping).

82. "A unified approach to the design of canonic integrated ladder filters," Proc. I.E.E.E. International Symposium on Circuits and Systems, New Orleans, May 1990, pp.2272 - 2275 (with Li Ping and R.K. Henderson).

83. "Switched capacitor and active - RC allpass ladder filters," Proc. I.E.E.E. International Symposium on Circuits and Systems, New Orleans, May 1990, pp. 2833 - 2836 (with Li Ping).

84. "Design and testing of a GaAs switched capacitor filter", Proc. I.E.E.E. International Symposium on Circuits and Systems, New Orleans, May 1990, pp. 2825 - 2828 (with D.G. Haigh, C. Toumazou, S.J. Harrold, K. Steptoe and R. Bayruns).

85. "400 MHz switching rate GaAs switched capacitor filter" Electronics Letters, March 1990, No.7, pp. 460 - 461 (with D.G. Haigh, C. Toumazou, S.J. Harrold, K. Steptoe and R. Bayruns).

86. "Performance comparisons of switched-capacitor filter realisations", I.E.E. Saraga Colloquium on Digital and Analogue Filters and Filtering Systems, London, May 1990, pp.12/1 - 12/6 (with R.K. Henderson and Li Ping).

87. "Active and digital ladder-based allpass filters", Proc. I.E.E., Part G, Circuits Devices and Systems, December 1990, Vol.137, No.6, pp.439-445 (with Li Ping).

88. "Extended Remez algorithms for filter amplitude and group delay approximation", Proc. I.E.E., Part G, Circuits Devices and Systems, June 1991, Vol.138, No.3, pp.289-300 (with R. K. Henderson and Li Ping).

89. "Canonical design of integrated ladder filters", Proc. I.E.E., Part G, Circuits Devices and Systems, April 1991, Vol.138, No.2, pp.222-228 (with R.K. Henderson and Li Ping).

90. "Design, optimisation and testing of a GaAs switched capacitor filter", I.E.E.E.Trans. CAS, August 1991, CAS-38, No.8, pp.825-837 (with D.G. Haigh, C. Toumazou, S.J. Harrold, K. Steptoe and R. Bayruns).

91. "Matrix methods for the design of transconductor ladder filters", Proc. I.E.E.E.International Symposium on Circuits and Systems, Singapore, June 1991, pp.1355-1358 (with N.P.J. Greer, R.K. Henderson and Li Ping).

92. "Design of a switched-capacitor filter for voice band signals", Proc. I.E.E.E.International Symposium on Circuits and Systems, Singapore, June 1991, pp.1574-1577 (with Li Ping, R.C.J. Taylor and R.K Henderson).

93. "A methodology for integrated ladder filter design", I.E.E.E.Trans. CAS, August 1991, CAS-38, No.8, pp.853-868 (with Li Ping and R.K. Henderson).

94. "A 500 MHz GaAs second-order bandpass switched-capacitor filter", Proc. European Conference on Circuit Theory and Design, Copenhagen, September 1991, pp.1171-1177 (with S.J Harrold, D.G. Haigh, C Toumazou, K. Steptoe and R. Bayruns).

95. "Software for the design of transconductor-capacitor filters and equalisers", I.E.E. Saraga Colloquium on Digital and Analogue Filters and Filtering Systems, London, December 1991, pp.7/1-7/6 (with Lu Yue and N.P.J Greer).

96. "High performance front-end signal processing: system design aids", I.E.E. Colloquium on Circuit Theory and DSP, London, February 1992, pp.2/1-2/6.

97. "A method for the evaluation of multirate sigma delta systems", Proc. I.E.E.E. International Symposium on Circuits and Systems, San Diego, May 1992, pp.1328-1331, (with D.M. Hossack).

98. "Design of a switched-capacitor filter for a mobile telephone receiver", I.E.E.E. Journal of Solid State Circuits, September 1992, Vol. 27, No.9., pp.1294-1298 (with Li Ping, R.K. Henderson and R.C.J. Taylor).

99. "Ladder based transconductor-capacitor filter and equaliser design", I.E.E. Saraga Colloquium on Digital and Analogue Filters and Filtering Systems, London, November 1992, pp. 7/1 - 7/8, (with Lu Yue and N.P.J. Greer).

100. "Analog integrated filter compilation", Journal of Analog Integrated Circuits and Signal Processing", March 1993, Vol.3, pp.217-228 (with R.K. Henderson and Li Ping).

101. "A transconductor-capacitor video filter and equaliser design", Proc. I.E.E.E. International Symposium on Circuits and Systems, Chicago, May 1993, pp986-989 (with Lu Yue and, N.P.J Greer).

102. "Efficient sensitivity analysis for large non-ideal switched capacitor networks", Proc. I.E.E.E. International Symposium on Circuits and Systems, Chicago, May 1993, pp.1405-1407 (with Z.Q. Shang).

103. "Design of high order sigma-delta modulators with minimum weighted noise", Proc. I.E.E.E. International Symposium on Circuits and Systems, Chicago, May 1993, pp.180-183 (with D.M. Hossack).

104. "Computer-aided design of high order sigma-delta ADC's", I.E.E. Colloquium on Advanced A-D and D-A Conversion Techniques and Applications, London, May 1993, pp.2/1-2/5 (with D.M. Hossack).

105. "XFILT: an X-window based modern filter and equaliser design system", Proc. European Conference on Circuit Theory and Design", Davos, Switzerland, August 1993, pp.305-310 (with Lu Yue, R.K. Henderson).

106. "A comparison study of SC biquads in the realisation of SC filters", Proc. I.E.E. Saraga Colloquium on Digital and Analogue Filters and Filtering Systems, London, November 1993, pp.10/1-10/9 (with Lu Yue).

107. "Issues in the design of low oversampling ratio single bit sigma-delta modulators", Proc. I.E.E. Colloquium on Oversampling Techniques and Sigma-Delta Modulation, London, March 1994, pp.3/1-3/5 (with D.M. Hossack, J. Reid).

108. "Matrix methods for the design of transconductor ladder filters", Proc. I.E.E., Part G, Circuits Devices and Systems, April 1994, Vol. 141, No. 2, pp.89-100 (with N.P.J. Greer, R.K. Henderson, Li Ping).

109. "Efficient noise analysis methods for large non-ideal SC and SI circuits", Proc. I.E.E.E. International Symposium on Circuits and Systems, London, June 1994, pp.5/565-5/568 (with Z.Q. Shang).

110. "A comparison study of SC biquads in the realisation of SC filters", Proc. I.E.E.E. International Symposium on Circuits and Systems, London, June 1994, pp.5/711-5/714 (with Lu Yue).

111. "Canonical realisation of ladder based transconductor-capacitor filters", Proc. I.E.E.E. International Symposium on Circuits and Systems, London, June 1994, pp.5/265-5/268 (with Lu Yue and N.P.J. Greer).

112. "The application of redundant number systems to digital sigma-delta modulators", Proc. I.E.E.E. International Symposium on Circuits and Systems, London, June 1994, pp.2/481-2/484 (with D.M. Hossack).

113. "Efficient analysis of some non-linearities in SC and SI filter networks", Proc. I.E.E. Saraga Colloquium on Digital and Analogue Filters and Filtering Systems, London, November 1994, pp.10/1-10/5 (with Z.Q. Shang).

114. "First or second generation SI cells? A comparison of sensitivity from an SI filter system viewpoint", Proc. I.E.E. Saraga Colloquium on Digital and Analogue Filters and Filtering Systems, London, November 1994, pp.11/1-11/5 (with Lu Yue).

11. Grants

Science Research Council Grant 1975 -77	£ 3337
Science Research Council Grant 1975 -77	£ 6085
Royal Society Travel Grant 1978	£ 200
Imperial College/Admiralty Research Contract 1980	£ 1110
Science Research Council Grant 1980-84	£ 23800
Rutherford Laboratory Research Contract 1981-82	£ 19815

Science & Engineering Research Council Grant 1981-84	£ 56345
(Rutherford Computer Allocation	£ 37500)
Ministry of Defence Contract 1984-85	£ 31646
Ministry of Defence Contract 1985-86	£ 29126
Science & Engineering Research Council Grant 1983-86	£ 58738
(Rutherford Computer Allocation.	£ 69000)
Science & Engineering Research Council Grant 1986-89	£ 152280
(SERC Services	£ 62250)
Science & Engineering Research Council Grant 1989-92	£ 89680
IBM (UK) Ltd. 1990	£ 24159
IBM (UK) Ltd 1992-93	£ 29965
Science & Engineering Research Council Grant 1992-95	£ 118775
Engineering & Physical Research Council Grant 1995-1997	£ 242306 (with S.P. Beaumont)
Royal Society Travel Grant 1984	£ 598
Royal Society Travel Grant 1985	£ 1100
Royal Society Travel Grant 1990	£ 650
Royal Society Travel Grant 1991	£ 821
Carnegie Trust Travel Grant 1995	£ 1200
Numerous travel grants from various sources including British Council and I.E.E.E.	

12. **Other Activities and Interests**

Main interest is in Christian work and activities.

Sports activities include climbing and swimming.

Sub-Warden at a University Student House 1966-68.

Member of University Staff-Chaplaincy Advisory Committee 1966-68.

Part-time lecturer at Newcastle Polytechnic 1965-68.

Guest lecturer at the same college on "The use of a Digital Computer in the Design and Analysis of Networks" in a course on Modern Network Analysis and Synthesis.

Guest lecturer at the University of Leeds, Electronics Exhibition 1967, on "Computer Aided Design of Electrical Networks".

Lectures to Institution of Electrical Engineers Local Centre:

N.E. Graduate and Student Section 1967 - "Use of computers in Network Analysis and Synthesis".

N.E. Electronics Section 1968 - "ZY Analysis".

Presented paper at International Conference on Computer Aided Design, University of Southampton, April 1969. (Ref. 7)

Gave colloquium at University of Durham, March 1972.

Presented paper at International Conference on Computer Aided Design, University of Southampton, April 1972. (Ref. 14)

Presented paper at the Second International Symposium on Network Theory, Herceg-Novi, Yugoslavia, July 1972 (Ref.16)

Gave colloquium at University of Newcastle upon Tyne, April 1973.

Presented paper at Conference on Teaching Electronics in Degree Courses, University of Hull, April 1973. (Ref. 19)

Gave colloquium at University of Newcastle upon Tyne, April 1974.

Presented paper at I.E.E. Colloquium on Amplifier Design - Theory and Practice, London, May 1974. (Ref. 25)

Presented paper at the Fourth Summer School on Circuit Theory, Prague, Czechoslovakia, September 1974. (Ref. 26)

Gave colloguium at University of Newcastle upon Tyne, April 1975.

Presented two papers at I.E.E.E. International Symposium on Circuits and Systems, Munich, April 1976. (Refs. 29, 30)

Gave lecture to I.E.E.E. Circuits and Systems Chapter, London, May 1976.

Gave colloquium at University of Newcastle upon Tyne, March 1978.

Presented paper at I.E.E.E. International Symposium on Circuits and Systems, New York, May 1978. (Ref. 37)

Presented paper at I.S.H.M./I.E.R.E. Colloquium on Hybrid Realisations of Active Filters, London, November 1978.

Gave colloquium at University of Newcastle upon Tyne, April 1979.

Presented paper at Fourth International Symposium on Network Theory, Ljubljana, Yugoslavia, September 1979. (Ref. 40)

Presented paper at Conference on Electronic Engineering in Degree Courses - Teaching for the 80's, University of Hull, April 1980. (Ref. 42)

Gave colloquium at University of Newcastle upon Tyne, April 1980.

Gave colloquium at Rutherford Laboratory, September 1980.

Presented paper at I.E.E. Colloquium on Electronic Filters, London, April 1981. (Ref. 46)

Gave lecture at Conference for Sixth Formers held under the auspices of the Mathematical Association, Hull, April 1981.

Gave colloquium at University of Newcastle upon Tyne, April 1982.

Presented paper at I.E.E.E. International Symposium on Circuits and Systems, Rome, May 1982. (Ref. 47)

Gave colloquium at University of Newcastle upon Tyne, April 1983.

Presented paper at I.E.R.E. Colloquium on Analogue Filters, London, November 1983. (Ref. 50)

Presented paper at I.E.E. Colloquium on Design Software, London, January 1984. (Ref. 51)

Presented paper at I.E.E.E. International Symposium on Circuits and Systems, Montreal, May 1984. (Ref. 52)

Presented paper at I.E E. Colloquium on Electronic Filters, London, May 1985 (Ref. 55)

Presented paper at I.E.E.E. International Symposium on Circuits and Systems, Kyoto, June 1985 (Ref 57)

Presented paper at I.E.R.E. Colloquium on Analogue Filters, London, November 1985.

Presented paper at I.E.E. Colloquium on Analogue IC Design, London, November 1987 (Ref. 67)

Presented paper at I.E.E.E. International Symposium on Circuits and Systems, Helsinki, June 1988. (Ref. 68)

Presented paper at I.E.E.E. International Symposium on Circuits and Systems, New Orleans, May 1990 (Ref. 83)

Presented papers at I.E.E.E. International Symposium on Circuits and Systems, Singapore, June 1991 (Refs. 91,92)

Presented paper at I.E.E. Colloquium on Circuit Theory and DSP, London, February 1992 (Ref. 96)

Presented poster paper at I.E.E.E. International Symposium on Circuits and Systems, Chicago, May 1993 (Ref. 103)

13. Refereeing Duties

Referee for Institute of Electrical and Electronic Engineers Inc. (America) - Transactions on Circuits and Systems; Proceedings of the International Symposium on Circuits and Systems, Munich (1968), Montreal (1984), Helsinki (1988), Portland (1989), New Orleans (1990), Chicago (1993).

Referee for Institution of Electrical Engineers - Proceedings, Electronics Letters and Journal on Circuits, Devices and Systems.

Referee for International Journal for Numerical Methods in Engineering.

Referee for Computer Aided Design, journal.

Referee for T. Nelson and Sons, Macmillan and Prentice-Hall, publishers.

Referee for the European Conference on Circuit Theory and Design, Lausanne (1978), The Hague (1981), Brighton (1989), Istanbul (1995).

Referee for Journal of Analog Integrated Circuits and Signal Processing.

Book reviews - various.

14. **External Duties**

I.E.E.E. Committee on Circuits and Systems Chapter for the UK and Republic of Ireland - Member (1975 - present), Vice Chairman (1978 - 1980), Chairman (1980 - 1983).

I.E.E.E. Section Committee for the UK and Republic of Ireland - Member (1980 - 1983).

Member I.E.E. E10 Professional Group Committee (1983 - 1989).

General Chairman of the Organising Committee, I.E.E.E. Conference on Computer Aided Design of Electronic and Microwave Circuits and Systems, University of Hull, July 1977.

Member of the Organising Committee, I.E.E.E. Conference on Applications of Adaptive and Multivariable Control, University of Hull, July 1982.

Joint-organiser of I.E.E.E. Workshop on Design and Fabrication of Integrated Circuit Filters, London, September 1982.

Member of UGC ECAD Initiative, Working Party on Analogue Software, 1987-89.

I.E.E. representative on Organising Committee for CADCAM Conference, Birmingham, 1987.

Member of the Organising Committee, European Conference on Circuit Theory and Design, Brighton, September 1989.

Member of Technical Programme Committee, I.E.E.E. International Symposium on Circuits and Systems, New Orleans 1990.

Invited participant in I.E.E.E./N.S.F. CAS Workshop on Future Directions of Circuits, Systems and Signal Processing, New Orleans, May 1990.

Member of International Publicity Committee, I.E.E.E. International Symposium on Circuits and Systems, San Diego 1992.

Chair of Technical Programme Committee, I.E.E.E. International Symposium on Circuits and Systems, London, 1994.

Member of Technical Programme Committee, I.E.E.E. International Symposium on Circuits and Systems, Seattle 1995.

Member of the Editorial Board of the International Journal of Electronics 1989 - present.

Consultant to Plessey Research Ltd., Caswell.

External Examiner, University of Newcastle upon Tyne - Ph.D 1976

External Examiner, University of Birmingham - M.Sc. 1976

External Examiner, University of Birmingham - Ph.D. 1978

External Examiner, University of Bradford - Ph.D. 1980

External Examiner, University of Javadpur - Ph.D. 1980

External Examiner, University of Newcastle upon Tyne - Ph.D. 1981.

External Examiner, University of Essex - M.Sc. 1982

External Examiner, University of Edinburgh - Ph.D. 1983

External Examiner, Imperial College - Ph.D. 1984

External Examiner, Imperial College - Ph.D. 1985

External Examiner, University of Dundee - B.Sc. and M.Sc. 1986-89

External Examiner, University of Leeds - Ph.D. 1989.

External Examiner, University of Birmingham - B.Eng. and M.Eng. 1991-1994.

2. Publications Submitted

Published Work Submitted for Consideration

P - indicates postgraduate student co-author.

U - indicates undergraduate student co-author.

* - indicates 1992 I.E.E. J.J.Thomson Premium Paper.

† - indicates I.E.E.E. Press Selected Reprint.

(-%) - indicates my proportion of contribution.

1. "Table for the voltage transfer functions of single amplifier double ladder feedback systems", Electronics Letters, May 1965, Vol.1, No.3, pp 70-71, (with A.G.J.Holt). (50%)

2. "Active RC filters employing a single operational amplifier to obtain biquadratic responses", Proc. I.E.E., December 1965, Vol. 112, No.12, pp.2227-2234, (with A.G.J.Holt). (50%)

3. "Table for the voltage transfer functions of single amplifier double ladder parallel feedback systems", I.E.E.E. Trans. C.T., September 1966, Vol. CT-13, pp.326-328, (with A.G.J. Holt). (50%)

4. "Correction function techniques", I.E.E. International Conference on Computer Aided Design, Southampton, April 1969, I.E.E. Conference Publication No. 51, pp.515-526, (with C. Nightingale). (80%)

5. "Matrix tables for the generalised 5-terminal amplifier", The Radio and Electronic Engineer, April 1969, Vol. 37, No.4, pp.247-55, (with F.W.Stephenson). (50%)

6. "Synthesis of multi-loop feedback systems, Part I, International Journal of Control, May 1969, Vol.9, No.5, pp. 487-497, (with A.G.J. Holt). (50%)

7. "Synthesis of multi-loop feedback systems, Part II", International Journal of Control, May 1969, Vol.9, No.5, pp.499-508, (with A.G.J. Holt). (50%)

8. "A simple method for producing floating inductors", Proc. I.E.E.E. December 1969, Vol. 57, No.12, pp. 2155-2156. (100%)

9. "Accumulant theory and applications", International Journal of Control, March 1970, Vol. 11, No.3, pp.479-488. (100%)

10. "Synthesis of active devices", International Journal of Electronics, December 1970, Vol.29, No.6, pp. 501-511. (100%)

11. "A course in computer-aided electronic circuit design for undergraduates", Computer Aided Design, April 1972, Vol 4, No.3, pp. 135-137, (with A.G. Martin). (50%)

12. "The multiterminal active transformer", International Journal of Control, July 1972, Vol. 16, No.1, pp. 171-175. (100%)

13. "Active circulator systems", International Journal of Electronics, December 1972, Vol.33, No.6, pp.677-679. (100%)

14. "Symbolic analysis for computer-aided circuit design - The interpolative approach", I.E.E.E. Trans. C.T., November 1973, Vol. CT-20, No.6, pp. 738-741. (with J.K. Fidler). (50%)

15. "Correction to symbolic analysis for computer-aided circuit design - the interpolative approach", I.E.E.E. Trans. CAS, May 1974, Vol. CAS-21, No.3, P.462, (with J.K.Fidler). (50%)

16. "Symbolic analysis of networks by partitioned polynomial interpolation", I.E.E.E. Trans. CAS, May 1974, Vol.CAS-21 No.3, pp. 345-347, (with C. Fridas[P]). (50%)

17. "An adaptive electronic circulator for use in telephones", I.E.E.E. Trans. COM, July 1975, Vol. COM-23, No.7, pp. 728-731, (with R. Lodge[U]). (70%)

18. "A theory of equivalent active networks", I.E.E.E. Trans. CAS, June 1976, Vol. CAS-23, No.6, pp.350-354, (with L.G.Grant[P]). (50%)

19. "Network partition methods for use in symbolic analysis by interpolation", Computer Aided Design, July 1976, Vol. 8, No.3, pp. 157-164, (with C. Fridas[P]). (50%)

20. "Symbolic network sensitivities using partition methods", Int. Journal of Electronics, July 1976, Vol.41, No.l, pp.25-32, (with C. Fridas[P]). (50%)

21. "Sensitivity minimisation and partitioned transformations in active equivalent networks", I.E.E. Journal on Electronic Circuits and Systems, March 1978, Vol.2, No.2, pp.33-38, (with L.G.Grant[P]). (50%)

22. "Some further sensitivity theorems in active equivalent network theory", I.E.E. Journal on Electronic Circuits and Systems, November 1978, Vol.2, No.6, pp. 193-198, (with J.Dunning-Davies and F.D. Faulkner[P]). (40%)

23. "An improved adaptive electronic circulator for telephone applications", I.E.E.E. Trans. COM, August 1979, Vol. COM-27, No.8, pp. 1218-1224 (with H. Gazioglu[U] and D.A. Homer[U]). (40%)

24. "Analysis of active switched-capacitor networks", Proc. I.E.E.E. February 1980, Vol. 68, No.2, pp. 292-293. (100%)

25. "Inclusion of amplifier finite gain and bandwidth in analysis of switched-capacitor filters", Electronics Letters, June 1980, Vol.16, No.12, pp.462-463, (with C. Lau[P]). (50%)

26. "Digital active network analysis", Proc. I.E.E., Part G, Electronic Circuits and Systems, August 1980, Vol.127, No. 4, pp. 181-186 (with F.G.A. Coupe[P]). (50%)

27. "A degree enhancement scheme in electronic engineering", Int. J. Elect. Enging. Educ., January 1981, Vol.18, pp. 29-34. (100%)

28. "Compact matrix scheme for use in computer analysis of switched capacitor networks", Electronics Letters, September 1982, Vol. 18, No. 19, pp. 840-841, (with C. Lau[P]). (50%)

29. "Improved z plane polynomial interpolative analysis of switched capacitor networks", I.E.E.E. Trans. CAS, July 1984, Vol. CAS-31, No.7, pp. 666-668 (with D.G. Johnson[P]). (50%)

30[†]. "Analysis of active switched-capacitor networks", selected reprint in MOS Switched-Capacitor Filters: Analysis and Design, I.E.E.E. Press, 1984, pp. 85-86. (100%)

31. "Symbolic analysis of ideal and non-ideal switched capacitor networks", Proc. I.E.E.E. International Symposium on Circuits and Systems, Kyoto, June 1985, pp.1165-1168 (with C.K. Pun[P]). (50%)

32. "On the generation of equivalent switched capacitor networks", Proc. European Conference on Circuit Theory and Design, Prague, September, 1985 pp.697-700 (with D.J. Gilbert). (50%)

33. "Efficient computer techniques for the exact analysis of all non-ideal effects of switched-capacitor networks in the time domain", Proc. I.E.E.E. International Symposium on Circuits and Systems, San Jose, May 1986, pp. 373-376, (with L.B. Wolovitz[P]). (50%)

34. "Optimisation of switched capacitor networks using equivalence transformations", Proc. I.E.E.E. International Symposium on Circuits and Systems, Philadelphia, May 1987, pp. 730 - 732 (with D.J. Gilbert and G.L. Holden[U]). (33%)

35. "The LUD approach to switched-capacitor filter design", I.E.E.E. Trans. CAS, Dec. 1987, Vol. CAS-34, No.12, pp.1611 - 1614 (with Li Ping[P]). (50%)

36. "General analysis of large linear switched capacitor networks", Proc. I.E.E. Part G, Electronic Circuits and Systems, June 1988, Vol. 135, No.3, pp. 119 - 124, (with L.B. Wolovitz[P]). (50%)

37. "Filter realisation by passive network simulation", Proc. I.E.E. Part G, Electronic Circuits and Systems, August 1988, Vol. 135, No.4, pp. 167 - 176 (with Li Ping[P]). (50%)

38. "The TWINTOR in bandstop switched-capacitor ladder filter realisation," I.E.E.E. Trans. CAS, July 1989, Vol. CAS-36, No.7, pp. 1041 - 1044 (with Li Ping[P]). (50%)

39. "High performance filter networks and symmetric matrix systems", Proc. I.E.E., Part G, Circuits Devices and Systems, Dec. 1989, Vol. 136, No.6, pp. 327 - 336, (with Li Ping[P]). (50%)

40. "400 MHz switching rate GaAs switched capacitor filter" Electronics Letters, March 1990, No.7, pp. 460 - 461 (with D.G. Haigh, C. Toumazou, S.J. Harrold, K. Steptoe and R. Bayruns). (17%)

41[*]. "Active and digital ladder-based allpass filters", Proc. I.E.E., Part G, Circuits Devices and Systems, December 1990, Vol.137, No.6, pp.439-445 (with Li Ping[P]). (50%)

42*. "Extended Remez algorithms for filter amplitude and group delay approximation", Proc. I.E.E., Part G, Circuits Devices and Systems, June 1991, Vol.138, No.3, pp.289-300 (with R. K. Henderson[P] and Li Ping[P]). (33%)

43*. "Canonical design of integrated ladder filters", Proc. I.E.E., Part G, Circuits Devices and Systems, April 1991, Vol.138, No.2, pp.222-228 (with R.K. Henderson[P] and Li Ping[P]). (33%)

44. "Design, optimisation and testing of a GaAs switched capacitor filter", I.E.E.E.Trans. CAS, August 1991, CAS-38, No.8, pp.825-837 (with D.G. Haigh, C. Toumazou, S.J. Harrold, K. Steptoe and R. Bayruns). (17%)

45. "A methodology for integrated ladder filter design", I.E.E.E.Trans. CAS, August 1991, CAS-38, No.8, pp.853-868 (with Li Ping[P] and R.K. Henderson[P]). (33%)

46. "A method for the evaluation of multirate sigma delta systems", Proc. I.E.E.E. International Symposium on Circuits and Systems, San Diego, May 1992, pp.1328-1331, (with D.M. Hossack[P]). (50%)

47. "Design of a switched-capacitor filter for a mobile telephone receiver", I.E.E.E. Journal of Solid State Circuits, September 1992, Vol. 27, No.9., pp.1294-1298 (with Li Ping[P], R.K. Henderson[P] and R.C.J. Taylor). (25%)

48. "Analog integrated filter compilation", Journal of Analog Integrated Circuits and Signal Processing", March 1993, Vol.3, pp.217-228 (with R.K. Henderson[P] and Li Ping[P]). (33%)

49. "Efficient sensitivity analysis for large non-ideal switched capacitor networks", Proc. I.E.E.E. International Symposium on Circuits and Systems, Chicago, May 1993, pp.1405-1407 (with Z.Q. Shang[P]). (50%)

50. "Design of high order sigma-delta modulators with minimum weighted noise", Proc. I.E.E.E. International Symposium on Circuits and Systems, Chicago, May 1993, pp.180-183 (with D.M. Hossack[P]). (50%)

51. "Issues in the design of low oversampling ratio single bit sigma-delta modulators", Proc. I.E.E. Colloquium on Oversampling Techniques and Sigma-Delta Modulation, London, March 1994, pp3/1-3/5 (with D.M. Hossack[P], J. Reid). (33%)

52. "Matrix methods for the design of transconductor ladder filters", Proc. I.E.E., Part G, Circuits Devices and Systems, April 1994, Vol. 141, No. 2, pp.89-100, (with N.P.J. Greer, R.K. Henderson[P], Li Ping[P]). (25%)

53. "Efficient noise analysis methods for large non-ideal SC and SI circuits", Proc. I.E.E.E. International Symposium on Circuits and Systems, London, June 1994, pp.5/565-5/568 (with Z.Q. Shang[P]). (50%)

54. "A comparison study of SC biquads in the realisation of SC filters", Proc. I.E.E.E. International Symposium on Circuits and Systems, London, June 1994, pp.5/711-5/714 (with Lu Yue[P]). (50%)

55. "The application of redundant number systems to digital sigma-delta modulators", Proc. I.E.E.E. International Symposium on Circuits and Systems, London, June 1994, pp.2/481-2/484 (with D.M. Hossack[P]). (50%)

Papers under Review

56. "Efficient design of ladder-based active filters and equalisers", submitted to Proc.I.E.E. (with Lu Yue[P] and N.P.J.Greer). (33%)

57. "Accurate semi-symbolic analysis of large non-ideal switched linear networks", accepted for Proc.I.E.E.E. International Symposium on Circuits and Sytems, Seattle, May 1995 (with Z.Q.Shang[P]). (50%)

58. "A systematic approach for ladder based switched-current filter design", accepted for Proc. I.E.E.E. International Symposium on Circuits and Sytems, Seattle, May 1995 (with Lu Yue[P]). (50%)

59. "Multirate SC and SI filter system design by XFILT", accepted for Proc. I.E.E.E. International Symposium on Circuits and Sytems, Seattle, May 1995 (with Lu Yue[P]). (50%)

3. Statement on Contribution and Originality

3. Statement of Contribution and Originality

The motivating forces behind the research and scholarship described in my publications in the learned society literature are quite diverse: some are pure research, some are responses to an industrial problem requiring a solution or an improvement to that which currently exists; others reflect the quest to close obvious gaps created by the progress of technology or the need to convey knowledge as an educator. As an engineer my ultimate goal has always been to find solutions to real problems, in the hope that some of these might translate through to commercial products or facilitate the design of electronic apparatus that will ultimately redound to the benefit of mankind.

A selection of my published work is presented under the following headings:

Active Filter Synthesis and CAD (Section 4)

Network Analysis and CAD (Section 5)

Communication Circuit Design (Section 6)

Analysis and Design of Sigma-Delta Modulator Systems (Section 7)

Educational Papers (Section 8)

Papers under Review (Section 9)

I acknowledge the fruitful collaboration with colleagues and postgraduate students over many years, resulting in publication under joint authorship. Whilst it is impossible to delineate precisely the balance of contribution, I was responsible in general for the conception and initiation of the major themes of the work and have carried the task of maintaining the continuity of topics over an extended period of time. All the work undertaken by my research students and assistants was supervised by me at all times. Proportions of contribution have been attributed in summary list. I adopted the principle of listing authors alphabetically, though occasionally where one student has contributed significantly more than another student, he has been given precedence.

3.1 Active Filter Synthesis and CAD (Section 4)

(Papers 2, 6,7, 8, 10, 12, 18, 21, 22, 32, 34, 35, 37, 38, 39, 40, 41, 42, 43, 44, 45, 47, 48, 52, 54, 56, 58, 59).

The origins of active filter theory emerge from classified work carried out during World War II, though it was not until demands on circuit size were imposed by Space exploration that the real stimulus for serious work appeared. The whole topic gained new impetus from the requirements imposed by IC developments, a demand which persists to the present time. The initial designs were committed to low frequency and audio band operation, but this expanded over the years so that the range of frequencies being covered now extends from below 1 Hz to 500 MHz and beyond. In the development of synthesis techniques, the aim has been towards general applicability rather than specific solutions for a particular frequency range or building block. However, various examples are given in the works cited, where application to certain problems with specified fabrication technologies have required a particularisation of certain general theories to good advantage.

The early papers [2, 6, 7] address the design of multi-loop feedback active filters, the development of a general synthesis theory and the production of a number of new circuit implementations. These realisations employed the voltage operational amplifier as the basic active element. This has transpired to be a very significant operational element in the whole of active filter work and whereas early work on analysis anticipated the emanation of other amplifiers, it was many years before some of these were actually utilised. Three more early papers [8, 10, 12] show further development of synthesis theories and various operational amplifier configurations, in the realisation of basic elements such as floating inductors or more hierarchical devices such as active circulators and transformers.

A major contribution to the theory of active equivalent networks is represented by three papers [18, 21, 22]. Prior to this, such theory had been limited to classical passive networks and the only attempt at the extension to active topologies proved to be very restricted. These papers develop the rigorous mathematics for the general equivalence transformation in active networks containing operational amplifiers. When used in conjunction with a general constrained nonlinear optimisation routine, significant

improvements in practical realisation parameters such as component spread and total sum, together with minimisation of component sensitivity, were reported. At a later date these principles were developed further in the context of switched capacitor networks [32, 34] and again significant improvements to network implementation costs were demonstrated.

With the advent of switched-capacitor (SC) implementations of filter networks in integrated circuit form, a major step forward was apparent in the design of filters for the mass communication market. This technology has proved to be most reliable and extremely robust. The initial designs were very closely linked to existing active-RC solutions and could be classified as cascades of biquadratic sections or leapfrog ladder approaches. The former had an early attraction because of ease of design in a mathematical sense. It had been established many years earlier, that active filter realisations, derived from a passive ladder prototype circuit, could demonstrate superior sensitivity properties. However SC ladder-based synthesis was troubled by inexact simulation of termination resistances and by the requirement for a strays-free realisation, in order to avoid the deleterious effects of stray capacitance which is invariably present in the integrated circuit realisation. A series of papers [35, 37, 38, 39, 41, 42, 43, 45, 47, 48, 52, 54, 56, 58] began to address the above problems in the general synthesis of ladder-based SC filters. It rapidly became apparent that not only was there a good solution to the difficulties associated with the existing ladder approach (leapfrog), but a completely general matrix scheme could be formulated to describe the whole synthesis process. Furthermore, many new realisations were forthcoming merely by applying standard matrix decomposition techniques. The general theory was equally applicable to active-RC and digital ladder-based filters [37, 39] and many new realisations followed. Later, the same general theory was also found to be applicable to transconductance-C [52, 56] and switched-current (SI) ladder-based filters [58]. Simultaneously, two other important developments were taking place. The first was the extension of the realisation of ladder-based allpass filters from purely digital configurations to active ones [41]. This circumvented the need for lattice type or differential structures and retained the essential low sensitivity ladder property; a further benefit was that these realisations were also encompassed within the matrix formulation. A second major

breakthrough was the development of a completely arbitrary approximation theory [42] which could include all the properties of existing classical approximations, together with a new high order touch point concept and general template weighting functions. The general theory could be used to approximate to any set of specifications - commonly amplitude or group delay. These developments not only allow a designer the freedom to explore many unusual approximations whilst maintaining realisability of the circuit, but other very important practical consequences follow. Many low frequency stop-band zeros can be forced to the origin, thus reducing the number of large time constants required in circuit realisation. Specific, sharp notches produced by high order zeros can be incorporated to shape the characteristic and remove particular frequencies. Non-switched capacitance feedthrough paths can be eliminated, thus breaking long delay free paths that cause restricted settling times when many amplifiers appear in series connection. High order touch points can be used within the passband to create "smoother" ripples which are particularly helpful at the band edges in reducing circuit sensitivity and group-delay equalisation requirements. Ripple characteristics can be tapered to reduce circuit sensitivities. Weighted passbands can be developed to satisfy the frequency characteristics demanded by other processes within a communication system and to absorb or equalise the amplitude characteristics of transmission lines. Most importantly, a new form of optimisation was now available in which the order of the search space was not dictated by the number of circuit components, but simply by the original order of approximation. Optimisation could be used to offset the effects of non-idealities in the circuit (amplifier gain/bandwidth, switch resistance, integrator imperfections in switched-current (SI) realisations). It could also counter the effects of numerical truncation due to quantisation introduced by the assembly of components such as capacitors and even transistors from combinations of unit-sized elements in integrated circuit layout. Thus a unified scheme based on the iterative Remez method was applicable to both filter approximation and optimisation. A combination of various ideas also enabled progress on the realisation of canonic ladder-based structures, when a modified function is actually synthesised and then input circuitry of the resultant filter is adjusted to return the original response [43, 56]. The climax of this work was a seminal paper on the methodology for

integrated ladder filter design [45] and the application of many of these principles to industrial problems. One design [47] has been of noted commercial success with large volume sales. The group of papers [41, 42, 43] were awarded the 1992 IEE J.J. Thompson Premium.

The philosophy behind the software suite which incorporates the general synthesis theories was outlined [48] and developed to a commercial level as XFILT software. The control of accuracy during the synthesis of high order networks is assured by methods conventional and novel. Recent extensions include multirate SC and SI systems design [59], when more attractive solutions can often be obtained for filters with particularly demanding specifications, for example very narrow band ones. Powerful network analysis software [49, 53] has been incorporated and the suite can deliver full sensitivity and noise analysis to aid the design task. A wide range of biquadratic sections has been added to provide a comprehensive synthesis tool. A typical application might require the comparison of numerous possible solutions to a set of filter specifications on a sensitivity basis [54].

Two other papers on filter design [40, 44] have been included in this section. These describe the combined work of a team of investigators including the author, which produced, in 1990, the highest frequency SC filter known to date. GaAs fabrication technology was employed and many design obstacles needed solution. My contribution was extensive circuit simulation using software outlined in the following section. The simulations revealed limitations due to initial amplifier and switch designs and it was possible to incorporate certain improvements prior to fabrication.

3.2 Network Analysis and CAD (Section 5)

(Papers 1, 3,4, 5, 9, 13, 14, 15, 16, 19, 20, 24, 25, 26, 28, 29, 30, 31, 33, 36, 49, 53, 57).

Network analysis is the handmaiden of circuit synthesis and design. Traditionally the linear analysis methods consisted of general matrix or topological techniques together with a "bag full of tricks" - simplifying transformations, symmetry considerations, equivalent network and superposition theorems. Certain networks, such as ladders, lent themselves to closed form solutions. Before the advent of computers, the circuit designer was forced into a

selection of special techniques and approximations for his analysis tools. Over the past 30 years, as computing power has become more readily available, it has been possible to observe the move away from the analysis magician towards general matrix methods which are capable of providing analysis to whatever degree of detail and accuracy is required by the designer. The papers selected herein reflect this general trend quite accurately. The forward progress has not always been a smooth transition from particular to general, as evidenced in the case of SC networks. During the peak of activity in their development throughout the early 1980's, a variant on the traditional approach appeared, when methods for computer analysis of such networks were divided into ideal and non-ideal. The former assumed ideal devices (switches and operational amplifiers) within the network and permitted straightforward and quick solution for the first pass in design. When non-idealities (finite switch resistance, finite GB values for the amplifiers) were allowed in the device macromodels, then approximations, gross or otherwise, were required to produce any answers in a finite computing time. And how accurate were these solutions anyway? The techniques and routines have been refined to such an extent that the user of a modest workstation or PC can now expect to obtain reliable answers for complex noise or sensitivity analysis of switched networks, within a realistic time frame.

The work represented is mainly concerned with linear networks though, more recently, extensions have been made into the analysis of dominant nonlinear effects in switched networks.

The development of closed form solutions [1, 3, 9] for multi-loop feedback networks containing an operational amplifier represents a classical approach to the analysis of a certain class of network when the operational device is assumed ideal. The networks were important active filters, whose synthesis is outlined in the papers of Section 4. A hybrid ideal/nonideal solution [4] for these networks when non-ideal marcromodels for the amplifiers were assumed, presented interesting principles for computer analysis that could be extended to many other classes of network. Early work on the derivation of admittance matrices for all four basic types of operational amplifier [5] pre-dated much of the application and design work that has followed from many authors. An interesting manipulation of matrix

descriptors for networks of active circulators [13] provided not only a simple analysis tool but also gave a compact method for examining novel interconnection strategies.

Symbolic analysis has been the *bête noir* of a considerable number of researchers for many years. It is universally acknowledged that the production of fully symbolic transfer functions of networks by computer, in terms of the constituent circuit components and parameters, could provide very attractive insight for the designer and the generation of differentials for sensitivity and optimisation studies. But it was realised at an early stage, by a large majority of investigators, that the exponential (or worse) growth in size of expression and the associated storage requirements would render the technique impractical for all but small circuits. A number of researchers still continue such an approach and even with "gardening" and truncation, the restriction to circuits of modest size persists. A number of rather more realistic variations on symbolic techniques have been proposed and I have been involved in the development of a semi-literal interpolative approach to considerable effect [14, 15, 16, 19, 20, 29, 57]. In this case the results of computer analysis are polynomials in s or z or both variables, whose coefficients are numeric (though a small number of symbolic components can be included at the cost of repeating the whole procedure for each element). The first significant step was to establish the general application of interpolation techniques to the efficient analysis of active networks [14, 15]. As the size of network was increased, problems of accuracy arose and major progress towards resolving this issue was produced by partitioned polynomial interpolation [16]. This utilises sample points located in a circular manner and involves circles of different radii or sets of samples on the same circle with different initial set angles or combinations of both. The work was important for two reasons; it was an elegant solution to the accuracy problem and secondly the choice of circular samples prompted other investigators to realise that the Fast Fourier Transform (FFT) was the exact implementation of the interpolation scheme when a circle of unit radius was used. This meant that all of the highly efficient FFT routines could be used as the basic numerical engine for semi-literal interpolative analysis, a situation which prevails to the present time. Other techniques, such as network partition methods [19, 20] were developed to cope with the problems of large networks. These contributed to further improvements in accuracy and

storage improvements, together with features useful in the computation of symbolic network sensitivities. With the advent of SC networks, the application of interpolative schemes to their ideal semi-symbolic analysis proved to be successful, although analysis of networks of modest size by interpolation in the z domain, raised more severe accuracy concerns than had been experienced previously with active RC networks. A combined conformal transformation of the plane and partitioned polynomial interpolation again proved to be very successful in maintaining accuracy during the analysis of high order SC networks [29]. The extension of semi-symbolic analysis to include non-ideal effects in SC networks was not at all straightforward. An early attempt using a Kader sequence for matrix inversion [31] enjoyed some success, but application was limited to circuits of moderate order because of the computing resources needed. The system was considered as a general one with polynomials in s and z. The problem has been reconsidered very recently [57], when an interpolative approach has once again been used to advantage in the general analysis of non-ideal SC and SI networks. Essentially there is no closed form symbolic expression for the transfer function of a non-ideal switched network, since the computation of an extended state transition matrix is implicit to all solutions and at best this can only be approximated in a numerical manner. However, using an over-interpolation scheme, modified polynomials in z, of slightly higher order than those expected in the ideal case, are produced to describe exactly the network behaviour [57]. Accuracy has been maintained during the analysis of large non-ideal SC and SI networks. It is also shown that significant advantages can result when this technique is used in noise analysis of switched networks with 2 clock phases. All the aliasing effects of wide band noise are easily computed by numerical substitution of a large number of frequency values into the polynomials. Unfortunately such advantages are quickly eroded when the number of clock phases increase in multirate circuits.

As already indicated, the introduction of SC networks during the late 1970's and early 1980's brought great demands for comprehensive analysis. Initially many schemes abounded, even for ideal networks, and I was able to make contributions to the early work [24]. This paper was also chosen as a selected reprint [30] by IEEE Press for a volume on significant papers in the subject. Translation of analytical techniques into CAD tools was an

obvious development, but the success story associated with SC filters in particular encouraged designers to be more ambitious in extending their requirements to high order circuits. This quickly brought about the demise of much of the less durable analysis software and triggered the search for improved mathematical and algorithmic routines. A compaction scheme [28] was very effective in coping with multi-phase higher order SC networks. A preliminary attempt to include some circuit non-idealities proved to be limited to simple circuits [25]. A series of papers [33, 36, 49, 53] made a serious attack on the efficient computation of all non-idealities in large linear switched networks. A whole compendium of numerical techniques were fully exploited, including sparse matrix methods, optimal ordering, interpretive code generation, Hessenberg techniques, extensive frequency independent pre-processing, polynomial approximation of excitations and full discretisation of the non-ideal switched network description. The resultant software has gained a reputation for speed, accuracy and robustness, the current version of SCNAP4 is in use at a number of industrial and university sites around the world and negotiations for full commercial exploitation are in hand with two companies. The analysis of the largest known multi-rate switched networks to give frequency responses, sensitivity behaviour and noise performance can now be accomplished on modest work stations and PCs in very realistic computational times.

An investigation into the description and design of digital active networks [26] produced very interesting results. However these have been largely superceded by the irrepressible development of digital filters and DSP on the one hand and by SC and SI networks on the other.

3.3 Communication Circuit Design (Section 6)

Papers (17, 23).

These two papers report work on practical circuit design for telephone applications. In many telephone networks worldwide, problems occur when matching the wide variations in local subscriber lines caused by different line lengths, line material (Cu or Al), conductor dimensions and mixtures of all of these in different proportions. In rural areas the length of

local lines can aggravate the problem. In urban districts the runs are shorter and approximately equivalent in length, but the actual lines may have been modified so often with odd pieces of cable of such random specifications that the resultant line characteristics often exhibit considerable variations. The adaptive electronic circulator was developed for use in these situations, as an effective means for providing isolation between transmit and receive signals and a constant level of side-tone for user comfort. Basic problems of voice switching were addressed by extra feedback. The initial work was confined to resistive matching only. In the second paper, a more general adaptive impedance match was successfully demonstrated, low and high frequency pilot tones being used to derive error signals for two term control. The voice switching problem was eliminated and good adaptive performance was demonstrated over a wide frequency range for a great variety of subscriber lines and loads.

The advantage of these circulator circuits over traditional passive hybrids was their ease of realisation as part of any integrated circuitry associated with a modern telephone set.

3.4 Analysis and Design of Sigma-Delta Modulator Systems (Section 7)

(Papers 46, 50, 51, 55)

In recent years there has been an explosion of interest in over-sampling data converters. Such circuits offer highly attractive solutions to the analogue/digital/analogue interface problems, they permit shaping of the noise characteristic, provide multi-bit conversion and above all they can be realised in integrated circuit form without the need for highly accurate passive components.

One of the major problems in this area of work is the complexity of simulating the behaviour of multirate sigma delta systems. A general behavioural simulator was developed [46] with an emphasis on providing a user-friendly interface. The software FUNSIM has been used extensively in one industrial establishment. It has also facilitated studies in the design of high order sigma-delta modulators with tailored noise characteristics [50] suitable for high quality digital audio applications.

Studies on the design of low over-sampling ratio sigma-delta modulators [51] have utilised techniques for adaptive step size to give companding and have developed ideas on noise gating. It was also shown that when these ideas are applied to the problem of speech coding/decoding, the resultant system can give significant performance improvement over existing linear PCM techniques.

More recent work has been concerned with digital sigma-delta modulators [55], the speeds of which are limited by latency in loop filters. An interesting solution has been developed by employing a redundant number system instead of a traditional two's complement number system. There seems to be scope for many further developments and some of these are curre ıtly under investigation.

3.5 Educational Papers (Section 8)

(Papers 11, 27)

These papers describe two course developments in which I was involved. In the early 1970's the introduction of CAD into the teaching of electronic circuits began to receive attention. Unfortunately many of the schemes were piecemeal and somewhat ad hoc. The first paper [11] details a scheme to integrate a student's acquisition of theoretical knowledge from lectures, with his practical experience from laboratory work and attempts to force a convergence of these skills through the medium of a 4 week design project. Further motivation derived from the use of analysis software to evaluate designs in a controlled manner. The whole exercise proved to be very successful with students and ran with early analysis software for a period of 10 years, until more general software became common place.

The second paper [27] describes a different educational initiative. In the late 1970's there were numerous high level reports on how to improve the quality of engineering graduates. At the University of Hull, I chaired a working party which had the task of producing a realistic scheme for an enhanced degree in electronic engineering. The scheme enjoyed considerable success over a number of years. However, it is interesting to note that many of the premises on which that initiative was based have been eroded over the

intervening years and many of the caveats mentioned at the conclusion of the paper have been ignored. The standard of education of electronic engineers in UK might well be sinking below the international "electronic Plimsoll line".

3.6 The Future

This set of collected papers covers a period of 30 years, during which electronics has developed from an advanced art into a highly sophisticated one. Surely it must be one of the few experiences of modern existence, when after such a length of time, more functionality can be obtained at less cost. Furthermore, there is no sign that these trends have run their course; more is yet to come.

And more is in store across the landscape presented in this work. The human form operates almost exclusively in an analogue mode and relates to a largely analogue, physical world by analogue means. Yet the most powerful forms of collecting data, processing information and stimulating response lines reside firmly in the digital domain. The way forward is not by a frantic search for remaining "analogue gaps" and the development of electronic solutions for these niche areas only. It must be via fully engineered interfaces between analogue and digital environments and technologies - completely integrated designs where the advantages of each domain are utilised to maximum effect. As the possibilities of truly mixed-mode design unfold, the demands for new simulation facilities increase, which in turn reveal new avenues for optimisation and creative design.

Many of the techniques reported in this work and the resultant software packages have been applied to the design of signal conditioning circuits whose frequencies of operation lie in the frequency range 1 Hz to 500 MHz. We are already addressing the problems associated with designs operating at 1 GHz and in the near future 12 GHz should be within reach. The challenge is to develop proper engineering design techniques and supporting simulation software to meet these demands.

"Si jeunesse savait; si vieillesse pouvait"

(if only youth knew; if only age could)

Les Prémices, Henri Estienne, 1531-1598

4. Active Filter Sythesis and CAD

Page

PAPER 2

Active *RC* filters employing a single operational amplifier to obtain biquadratic responses

A. G. J. Holt, Ph.D., A.M.I.E.E., and J. I. Sewell, B.Sc., Graduate I.E.E.

Synopsis

In this paper, networks are presented in tabular form to simplify the design of *RC* active filters having magnitude responses characterised by pass-band attenuation ripples and stop-band transmission zeros. The responses of these networks may be described by biquadratic rational functions. In all, the form and element values for 11 different networks are tabulated.

The basic network discussed in the paper is an operational amplifier with multiloop feedback in cascade with a passive *RC* circuit and having a second-order response. Higher-order responses than the second may be obtained by cascading second-order stages of the tabulated networks, with suitable isolating stages when necessary.

Two different forms of passive circuit are given, together with their design formulas. Both low-pass and high-pass filters are considered; these can be cascaded to give band-pass or band-stop characteristics.

The operational amplifier is assumed to have infinite input and zero output impedance; the effects of departure from these ideal conditions on the filter response is considered.

List of symbols

D = general transfer function
D_A = transfer function of active section
D_p = transfer function of passive section
p = Laplace-transform variable
a_0 = numerator polynomial coefficient of overall transfer function
b_0, b_1 = denominator polynomial coefficients of overall transfer function
$B_0, B_1, \ldots B_n$ = numerator coefficients of general active section
$b_0, b_1, \ldots b_n$ = denominator coefficients of general active section
Y_1, Y_2, Y_3, Y_4, Y_5 = admittances of active-section components
$y_{11}, y_{12}, y_{21}, y_{22}$ = admittance parameters of 2-port network
$q(p)$ = arbitrary divisor polynomial
K_0, K_1 = coefficients of arbitrary divisor polynomial
r_3' = unscaled series resistive element in high-pass ladder section
$F(p)$ = numerator polynomial of active section
u = parameter in passive synthesis procedure
α = constant attenuation coefficient for passive network
α_1 = constant attenuation coefficient for Guillemin network
α_2 = constant attenuation coefficient for network design from Reference 15
D_{HP} = high-pass transfer function
M = amplifier open-loop gain

1 Introduction

Filters having responses described by biquadratic rational functions are well known in passive-*LC*-network design. These networks may have transmission zeros (often known as poles of attenuation) at finite frequencies which lie on the imaginary axis of the p plane. The responses of certain classes of these networks may be described by the elliptic functions.

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Responses of the biquadratic form may also be obtained with active *RC* filters employing operational amplifiers and inductor-free passive feedback networks. The use of active networks in filter design is of increasing importance with the introduction of integrated circuits, in which it is difficult to obtain satisfactory inductors. Active filters are also used to deal with the very low-frequency signals which arise in control applications. The size and cost of the inductors which would be required in conventional *LC* filters become prohibitive at these frequencies.

Amplifier circuits which may have biquadratic responses have been described in the literature,[1-5] but these either require a number of amplifiers, sometimes used as integrators, or if only one amplifier is used, employ at least two parallel ladder networks.

It will be shown that for a second-order stage only one parallel ladder network is required, together with a single operational amplifier having multiple-loop feedback. The sensitivity of the circuit to changes in amplifier gain is made small by the feedback applied. Responses of the biquadratic form may also be obtained with circuits employing negative-impedance convertors and gyrators. Synthesis procedures for negative-impedance-convertor circuits have been described by Linvill[16] and by Yanagisawa;[17] a set of design Tables for second- and fourth-order filters employing the Yanagisawa procedure has been presented by Holt and Stephenson.[18] It is known that parallel ladder networks may be somewhat difficult to adjust, and a method which reduces their number, while yielding the same form of response, would appear to be advantageous.

The methods of design described in this paper are intended to provide networks having responses described by elliptic functions of the second order; other biquadratic responses may be obtained by the same method. Responses described by higher-order functions may be obtained by cascading second-order stages.

2 Principles

The derivation of all transfer functions considered in this paper is based on the cascaded sections shown in Fig. 1. An operational amplifier and multiloop feedback circuit, as shown in Fig. 2, are included in the active network. It is

assumed that the input impedance of the amplifier is infinite and its output impedance is zero, conditions which are easily approached in practice (deviations from ideal-impedance conditions are considered later).

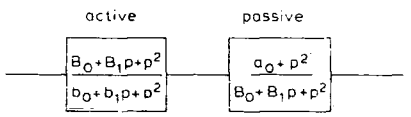

Fig. 1
Arrangement of active and passive sections

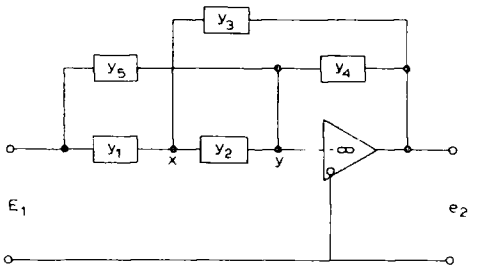

Fig. 2
Basic active multiloop feedback section

The biquadratic function having transmission zeros on the imaginary axis of the p plane is given by eqn. 1:

$$D = \frac{p^2 + a_0}{p^2 + b_1 p + b_0} \quad \ldots \quad (1)$$

It can be shown that the active circuits used produce transfer functions of the form

$$D = \frac{B_0 + B_1 p + B_2 p^2 + \ldots + B_n p^n}{b_0 + b_1 p + b_2 p^2 + \ldots + b_n p^n} \quad \ldots \quad (2)$$

Thus, if an active circuit of this type is used to produce the denominator of eqn. 1, the resultant transfer function of the active section has the form

$$D_A = \frac{B_0 + B_1 p + p^2}{b_0 + b_1 p + p^2} \quad \ldots \quad (3)$$

In order to obtain the complete transfer function of eqn. 1, it is necessary to place in cascade a network having the transfer function

$$D_P = \frac{a_0 + p^2}{B_0 + B_1 p + p^2} \quad \ldots \quad (4)$$

This latter function can be realised as a passive RC network provided the polynomial $B_0 + B_1 p + p^2$ has only real roots.

The active network used to produce the function has the general form shown in Fig. 2. The circuit is of the form used by Taylor.[12]

It is found that, for any transfer function of the type under consideration, all branches of the active network may be single resistors or capacitors except one which is a series or parallel RC circuit.

The general transfer function obtained using the idealisations mentioned in the first paragraph of this Section is

$$D_A = \frac{Y_1 Y_2 - Y_5(Y_1 + Y_2 - Y_3)}{Y_2 Y_3 + Y_4(Y_1 - Y_2 + Y_3)} \quad \ldots \quad (5)$$

In choosing the elements such that eqn. 5 has the form of eqn. 3, many possibilities exist; one combination which yields a simple result is with a parallel RC network and $Y_1 = 1/R_1$, $Y_2 = pC_2$, $Y_3 = pC_3$, $Y_4 = 1/R_4$ and $Y_5 = pC_5 + 1/R_5$.

The transfer function becomes

$$D_A = \frac{\frac{1}{R_1 R_5} - p\left(\frac{C_2}{R_1} - \frac{C_5}{R_1} - \frac{C_2}{R_5} - \frac{C_3}{R_5}\right) - p^2 C_5(C_2 + C_3)}{\frac{1}{R_1 R_4} - p\left(\frac{C_2 - C_3}{R_4}\right) - p^2 C_2 C_3} \quad \ldots \quad (6)$$

Equating coefficients between eqns. 6 and 3 gives

$$b_0 = \frac{1}{R_1 R_4}, \; b_1 = \frac{C_2 C_3}{R_4}, \; C_2 C_3 = 1 \quad \ldots \quad (7)$$

In order to use as many standard components as possible, and using normalised values, all capacitors are set to unity:

$$C_5 = C_3 = C_2 = C = 1$$

This gives

$$R_4 = \frac{2}{b_1}, \; R_1 = \frac{b_1}{2b_0} \quad \ldots \quad (8)$$

If $R_5 = 1$, the transfer function becomes

$$D_A = \frac{2\left\{\frac{b_0}{b_1} - p\left(\frac{2b_0}{b_1} - 1\right) + p^2\right\}}{b_0 + b_1 p + p^2} \quad \ldots \quad (9)$$

A passive network is required with a transfer function

$$\frac{a_0 - p^2}{\frac{b_0}{b_1} - p\left(\frac{2b_0}{b_1} - 1\right) + p^2} \quad \ldots \quad (10)$$

This may be synthetised by the Guillemin parallel-ladder method, provided the function has only real poles;

i.e. $$\left(\frac{2b_0}{b_1} - 1\right)^2 > \frac{4b_0}{b_1} \quad \ldots \quad (11)$$

This condition ensures that the response described by eqn. 10 is obtainable with a passive RC network and gives the limits to the range of functions realisable with configuration 5 from Table 1.

The parallel-ladder synthesis may be performed in two ways: one[14] yielding a terminated structure, and the other[13] an unterminated structure. There is little to choose between the two methods. The latter usually produces a network with a lower output impedance; this is important in cascaded systems if isolating stages are to be avoided. It has the disadvantage of using one more component.

3 Active-section configurations

There is an abundance of solutions for active sections of the type under consideration. Unfortunately only a limited number can be used to synthetise second-order functions having coefficients of the elliptic function without negative elements being required in the feedback network. Two classes of configuration emerge: those having one parallel RC element, and those with one series RC element.

3.1 Circuits with one parallel element

Table 1 shows useful solutions of this class. These keep to a minimum the number of components which have a nonunity normalised value. All elements are normalised to unity unless they are listed under the heading of variable.

Table 1

SOLUTIONS FOR ACTIVE SECTION WITH ONE PARALLEL COMBINATION

Parallel admittance	Declaration of circuit elements Y_1	Y_2	Y_3	Y_4	Y_5	Transfer function	Variable components	Realisability conditions
1 $Y_1 = pC_1 + \frac{1}{R_1}$	—	pC_5	pC_2	$\frac{1}{R_4}$	$\frac{1}{R_5}$	$\frac{\frac{1}{R_1R_5} + p\left(\frac{C_2}{R_1} + \frac{C_1}{R_5} + \frac{C_2}{R_5} + \frac{C_3}{R_5}\right) + p^2C_1C_2}{\frac{1}{R_1R_4} + p\left(\frac{C_1}{R_4} + \frac{C_2}{R_4} + \frac{C_3}{R_4}\right) + p^2C_2C_3}$	$R_4,\ R_1$ $R_4 = 3/b_1,\ R_1 = b_1/3b_0$	Nil
2	—	$\frac{1}{R_2}$	$\frac{1}{R_3}$	pC_4	pC_5	$\frac{\frac{1}{R_1R_2} + p\left(\frac{C_1 + C_5}{R_2} + \frac{C_5}{R_1} + \frac{C_5}{R_3}\right) + p^2C_1C_5}{\frac{1}{R_2R_3} + p\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)C_4 + p^2C_1C_4}$	$R_3,\ R_2,\ C_4$ $R_3 = \{(1/R_1 - b_1) + \sqrt{[(1/R_1 - b_1)^2 - 4b_0C_4]}\}/2b_0C_4$ $R_2 = 1/(b_0R_3C_4)$	$\left(\frac{1}{R_1} - b_1\right)^2 > 4b_0C_4$ $b_1 < \frac{1}{R_1}$
3 $Y_2 = pC_2 + \frac{1}{R_2}$	$\frac{1}{R_1}$	—	pC_3	$\frac{1}{R_4}$	pC_5	$\frac{\frac{1}{R_1R_2} + p\left(\frac{C_2}{R_1} + \frac{C_5}{R_1} + \frac{C_5}{R_2}\right) + p^2C_5(C_2 + C_3)}{\frac{1}{R_4}\left(\frac{1}{R_2} + \frac{1}{R_1}\right) + p\left(\frac{C_2}{R_4} + \frac{C_3}{R_2} + \frac{C_3}{R_4}\right) + p^2C_2C_3}$	$R_1,\ R_2,\ R_4$ $R_2 = \{(1/R_1 - b_1) + \sqrt{[(1/R_1 - b_1)^2 - 4(2b_0 - b_1/R_1)]}\}/2(2b_0 - b_1/R_1)$ $R_4 = 2/(b_1 - 1/R_2)$	$b_1 < 1/R_1$ $(1/R_1 - b_1)^2 > 4(2b_0 - b_1/R_1)$
4	pC_1	—	$\frac{1}{R_3}$	pC_4	$\frac{1}{R_5}$	$\frac{\frac{1}{R_5}\left(\frac{1}{R_2} + \frac{1}{R_3}\right) + p\left(\frac{C_1}{R_2} + \frac{C_1}{R_5} + \frac{C_2}{R_5}\right) + p^2C_1C_2}{\frac{1}{R_2R_3} + p\left(\frac{C_4}{R_2} + \frac{C_4}{R_3} + \frac{C_2}{R_3}\right) + p^2C_4(C_1 + C_2)}$	$C_1,\ R_2,\ R_3$ $R_3 = \frac{b_1 + \sqrt{\left(b_1^2 - 8b_0\left(1 + C_1\right)\right.}}{2b_0}$ $R_2 = 1/[b_0R_3(1 + C_1)]$	$b_1^2 > 8b_0/(1 + C_1)$
5 $Y_5 = pC_5 + \frac{1}{R_5}$	$\frac{1}{R_1}$	pC_2	pC_3	$\frac{1}{R_4}$	—	$\frac{\frac{1}{R_1R_5} + p\left(\frac{C_2}{R_1} + \frac{C_5}{R_1} + \frac{C_2}{R_5} + \frac{C_3}{R_5}\right) + p^2C_5(C_2 + C_3)}{\frac{1}{R_1R_4} + p\left(\frac{C_2 + C_3}{R_4}\right) + p^2C_2C_3}$	$R_1,\ R_4$ $R_4 = 2/b_1,\ R_1 = b_1/2b_0$	Nil
6	pC_1	$\frac{1}{R_2}$	$\frac{1}{R_3}$	pC_4	—	$\frac{\frac{R_2R_5}{R_2 + R_5} + p\left(\frac{C_1 + C_5}{R_2} + \frac{C_1}{R_5} + \frac{C_5}{R_3}\right) + p^2C_1C_5}{\frac{1}{R_2R_3} + p\left(\frac{R_2R_3}{R_2 + R_3}\right)C_4 + p^2C_1C_4}$	$R_2R_3C_4$ $R_3 = \frac{\frac{1}{C_4b_0} + \sqrt{\left\{\left(\frac{1}{C_4b_0}\right)^2 - \frac{4b_1^2}{C_4b_0}\right\}}}{2b_1}$ $R_2 = 1/(C_4R_3b_0)$	$(1/C_4b_0)^2 > 4b_1^2/C_4b_0$

Some solutions require the choice of an arbitrary variable to satisfy realisability conditions.

Configurations 1 and 5 in Table 1 give simple solutions, having four standard elements using only two resistive elements with nonunity normalised values.

3.2 Example using four standard elements

Fig. 3C shows the measured response obtained when solution 5 from Table 1 is used to realise the typical example of a second-order function:

$$D = \frac{p^2 + 7{\cdot}464}{p^2 + 0{\cdot}6075p + 0{\cdot}7559} \quad \ldots\ldots \quad (12)$$

Fig. 3A shows the passive networks. In the active section, the calculated element values are $R_4 = 3{\cdot}921$, $R_1 = 0{\cdot}4019$ (to four significant figures).

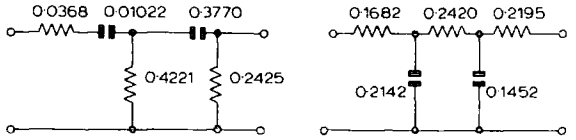

Fig. 3A

High- and low-pass ladder sections before combination and denormalisation

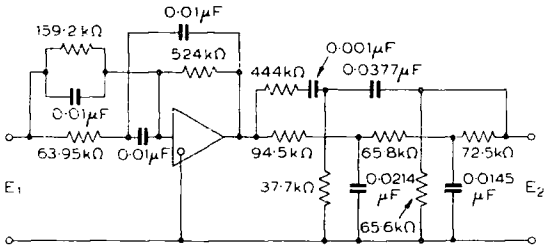

Fig. 3B

Complete circuit for example of Section 3.2

3.3 Denormalisation

It is frequently advantageous to denormalise the active and passive sections to different impedance levels. This enables the designer to obtain convenient component values and also avoid distortion due to drawing large currents from the amplifier. Fig. 3B shows the circuit designed for a cutoff frequency of 100c/s: $R = 159{\cdot}2\text{k}\Omega$, $C = 0{\cdot}01\,\mu\text{F}$ for the active section, and $R = 15{\cdot}92\text{k}\Omega$ and $C = 0{\cdot}1\,\mu\text{F}$ for the passive section.

3.4 Example using three standard elements

Consider alternative 4 (Table 1). Let $C_1 = 20\mu\text{F}$, and, for the function of eqn. 12, $R_3 = 0{\cdot}5902\text{k}\Omega$ and $R_2 = 0{\cdot}1067\text{k}\Omega$.

The numerator

$$F(p) = 0{\cdot}5532 - 10{\cdot}4203p + p^2 \quad \ldots\ldots \quad (13)$$

choosing

$$q(p) = (p + 0{\cdot}1)(p + 20) \quad \ldots\ldots \quad (14)$$
$$= p^2 + K_1p + K_0$$

and proceeding through the synthesis of Reference 13 gives the network of Fig. 4. This is denormalised for the passive section $R = 15{\cdot}92\text{k}\Omega$ and $C = 0{\cdot}1\,\mu\text{F}$; for the active section $R = 159{\cdot}2\text{k}\Omega$, $C = 0{\cdot}01\,\mu\text{F}$.

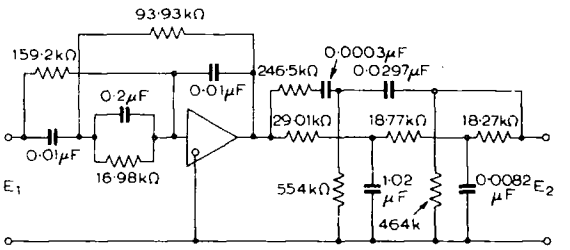

Fig. 4

Complete circuit for example of Section 3.4

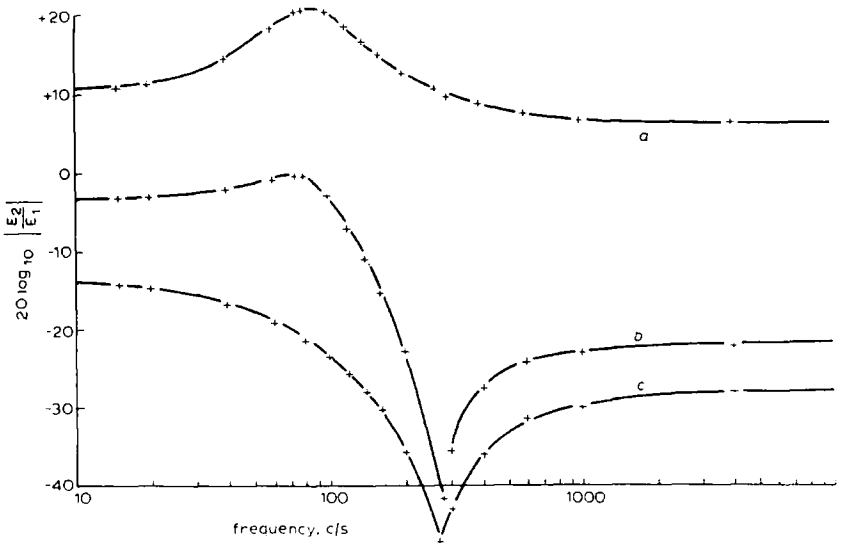

Fig. 3C

Response of active, passive and combined sections of example of Section 3.2

a Active section
b Resultant response
c Passive section

The transfer function for the passive section is

$$D = \frac{p^2 - 7{\cdot}464}{p^2 - 10{\cdot}4203p - 0{\cdot}5532} \quad \ldots\ldots (15)$$

With these coefficients, it is convenient to use the synthesis technique of Reference 15.

For

$$D_p = \frac{a_0 - p^2}{B_0 - B_1 p + p^2} \quad \ldots\ldots (16)$$

the components of the circuit shown in Fig. 5 become

$$\left.\begin{aligned} R_1 &= \left(\frac{2}{a_0} - \frac{2}{u}\right) & C_1 &= \frac{1}{2 - \frac{2}{u}} \\ R_2 &= \frac{2}{u} & C_2 &= 0{\cdot}5u \\ R_3 &= \frac{2 - \frac{2}{u}}{a} & C_3 &= \frac{u}{2 - \frac{2a_0}{u}} \\ & & C_4 &= \left(\frac{a_0}{2B_0} - 0{\cdot}5\right) \end{aligned}\right\} \quad \ldots\ldots (17)$$

where $u = \frac{a_0}{2B_0}(B_1 - 1) + 0{\cdot}5$

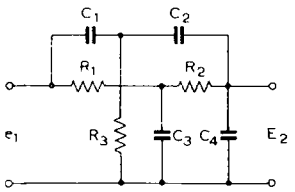

Fig. 5

Basic canonical form of the synthesis procedure of Reference 15

The second network produces a response with a slightly greater gain; this is due to the different constant multiplier produced by each synthesis method.

The passive function produced by these methods has the form

$$D_p = \alpha \frac{a_0 - p^2}{B_0 + B_1 p - p^2} \quad \ldots\ldots (18)$$

For the first (Guillemin) network,

$$\alpha = \alpha_1 = \frac{r_3' B_0}{B_0 - r_3' a_0} \quad \ldots\ldots (19)$$

where

$$r_3' = \left(1 - \frac{B_0}{K_0}\right) - \frac{(K_0 B_1 - K_1 B_0)/K_0}{K_1 - \frac{K_0^2}{K_0 B_1 - K_1 B_0} - \frac{B_0 K_0}{K_0 B_1 - K_1 B_0}}$$

For the second network,

$$\alpha = \alpha_2 = \frac{B_0}{a_0} \quad \ldots\ldots (20)$$

The ratio α_2/α_1 gives the gain difference, for this example

$$\alpha_2/\alpha_1 = 1{\cdot}148$$

i.e. 1·208 dB.

The complete filter consisting of feedback amplifier in cascade with the loaded twin-T network is shown in Fig. 6.

3.5 Circuits with one series RC element

Table 2 shows solutions which are applicable for the range of functions under consideration.

Some solutions are more complex than others and require the choice of one or more arbitrary variable components in order to satisfy realisability conditions.

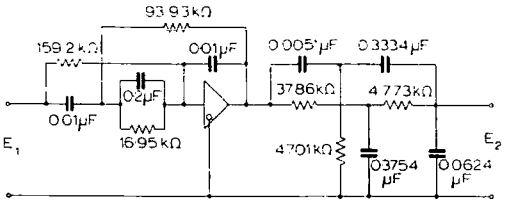

Fig. 6

Complete circuit for the filter using method of Reference 15 for the passive network

For example, taking alternative 3, again the required transfer function is

$$D = \frac{p^2 + 7{\cdot}464}{p^2 - 0{\cdot}6075p + 0{\cdot}7559} \quad \ldots\ldots (21)$$

Substitution of $R_4 = 4\,\text{k}\Omega$ and $C_2 = 1\,\mu\text{F}$ gives $R_1 = 0{\cdot}3174\,\text{k}\Omega$ and $R_3 = 0{\cdot}1684\,\text{k}\Omega$; setting $R_5 = 1\,\text{k}\Omega$ the numerator polynomial of the active section is

$$F = 0{\cdot}8322(2{\cdot}3408 + 5{\cdot}5429p + p^2) \quad \ldots\ldots (22)$$

factorising (disregarding the constant multiplier)

$$F = (p + 0{\cdot}515)(p + 5{\cdot}04) \quad \ldots\ldots (23)$$

choosing the polynomial as $(p + 1)(p + 6)$ ensures realisability. The parameters are

$a_0 = 7{\cdot}464$
$B_0 = 2{\cdot}3408$
$B_1 = 5{\cdot}5429$
$K_0 = 6$
$K_1 = 7$

Continuing the synthesis yields the network shown in Fig. 7. The passive section is denormalised to $R = 15{\cdot}92\,\text{k}\Omega$, $C = 0{\cdot}1\,\mu\text{F}$, and the active section to $R = 159{\cdot}2\,\text{k}\Omega$, $C = 0{\cdot}01\,\mu\text{F}$.

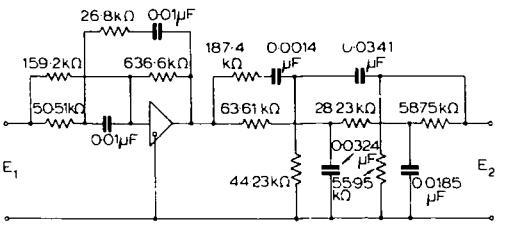

Fig. 7

Complete circuit diagram for the active-section configuration using one series combined element

The response of this configuration is identical with previous methods, apart from a constant gain factor.

3.6 Effect of finite input and nonzero output impedances of amplifier on filter response

As stated in Section 2, the theory presented in this paper was derived on the assumptions that the input impedance of the operational amplifier is infinite, and its output

Table 2

SOLUTIONS FOR ACTIVE SECTION WITH ONE SERIES COMBINATION

Series admittance	Declaration of circuit elements					Transfer function	Variable components	Realisability condition
	Y_1	Y_2	Y_3	Y_4	Y_5			
1 $Y_1 = \dfrac{pC_1}{1+pC_1R_1}$	—	pC_2	$\dfrac{1}{R_3}$	$\dfrac{1}{R_4}$	$\dfrac{1}{R_5}$	$\dfrac{\dfrac{1}{R_3R_5}+p\left(\dfrac{C_1}{R_5}+\dfrac{C_2}{R_5}+\dfrac{C_1R_1}{R_5R_3}\right)+p^2\left(1+\dfrac{R_1}{R_5}\right)C_1C_2}{\dfrac{1}{R_3R_4}+p\left(\dfrac{C_1}{R_4}+\dfrac{C_2}{R_4}+\dfrac{C_1R_1}{R_3R_4}+\dfrac{C_2}{R_3}+\dfrac{C_1R_1}{R_3}\right)+p^2C_1C_2R_1\left(\dfrac{1}{R_4}+\dfrac{1}{R_3}\right)}$	$C_1R_1R_3$, R_4 $R_4=\dfrac{1}{R_1}-1\left\{\left(1+\dfrac{1}{C_1}\quad b_1\right)+R_1\right\}$ $R_3=1/b_0C_1-R_4$	$R_4>0$ $R_4<1/(b_0C_1)$
2 $Y_2 = \dfrac{pC_2}{1+pC_2R_2}$	pC_1	—	$\dfrac{1}{R_3}$	$\dfrac{1}{R_4}$	$\dfrac{1}{R_5}$	$\dfrac{\dfrac{1}{R_3}+p\left(\dfrac{C_1}{R_5}+\dfrac{C_2}{R_5}+\dfrac{C_2R_2}{R_3R_5}\right)+p^2C_1C_2\left(1+\dfrac{R_2}{R_5}\right)}{\dfrac{1}{R_3R_4}+p\left(\dfrac{C_1}{R_4}+\dfrac{C_2}{R_4}+\dfrac{C_2R_2}{R_3R_4}+\dfrac{C_2}{R_3}\right)+p^2C_1C_2\dfrac{R_2}{R_4}}$	R_2, C_2, R_3, R_1 $R_2=\dfrac{(R_4-b_1)\pm\sqrt{\left\{(a_4-b_1)^2-4C_2b_0\left(\dfrac{1}{R_2}+C_2\right)\right\}}}{2C_2b_0}$ $R_3=1/C_1R_2b_0$	$b_1>R_4$ $(R_4-b_1)^2>4C_2b_0\left(\dfrac{1}{R_2}+C_2\right)$
3 $Y_3 = \dfrac{pC_3}{1+pC_3R_3}$	$\dfrac{1}{R_1}$	pC_2	—	$\dfrac{1}{R_4}$	$\dfrac{1}{R_5}$	$\dfrac{\dfrac{1}{R_1R_5}+p\left(\dfrac{C_2}{R_1}+\dfrac{C_3R_3}{R_1R_5}+C_2+C_3\right)+p^2C_3R_3\left(C_2+\dfrac{C_2}{R_1}\right)}{\dfrac{1}{R_1R_4}+p\left(\dfrac{C_3R_3}{R_1R_4}+\dfrac{C_2}{R_4}+\dfrac{C_3}{R_4}\right)+p^2C_2C_3\left(1+\dfrac{R_3}{R_4}\right)}$	$R_1C_2R_3R_4$ $R_1=\dfrac{\left(R_4+\dfrac{b_1}{b_0}\right)\pm\sqrt{\left\{\left(R_4+\dfrac{b_1}{b_0}\right)^2-\dfrac{4(C_2+1)}{b_0C_2}\right\}}}{2(C_2+1)}$ $R_3=1/(b_0R_1C_2)-R_4$	$\left(R_4+\dfrac{b_1}{b_0}\right)^2>\dfrac{4(C_2+1)}{b_0C_2}$ $R_4<1/(b_0R_1C_2)$
4 $Y_4 = \dfrac{pC_4}{1+pC_4R_4}$	pC_1	$\dfrac{1}{R_2}$	$\dfrac{1}{R_3}$	—	$\dfrac{1}{R_5}$	$\dfrac{\dfrac{1}{R_5}\left(\dfrac{1}{R_2}+\dfrac{1}{R_3}\right)+p\left(\dfrac{C_1}{R_2}+\dfrac{C_1}{R_5}+\dfrac{C_4R_4}{R_2}+\dfrac{C_4R_4}{R_3}\right)+p^2C_1C_4R_4\left(\dfrac{1}{R_2}+\dfrac{1}{R_5}\right)}{\dfrac{1}{R_2R_3}+p\left(\dfrac{C_4R_4}{R_2R_3}+\dfrac{C_4}{R_2}+\dfrac{C_4}{R_3}\right)+p^2C_1C_4}$	C_1, R_2, R_3, R_4 $R_2=\dfrac{\left(R_4-\dfrac{b_1}{b_0}\right)\pm\sqrt{\left\{\left(R_4-\dfrac{b_1}{b_0}\right)^2\quad\dfrac{4}{C_1b_0}\right\}}}{2}$ $R_3=1/b_0C_1R_2$	$\left(R_4-\dfrac{b_1}{b_0}\right)>0$ $\left(R_4-\dfrac{b_1}{b_0}\right)^2>\dfrac{4}{C_1b_0}$
5 $Y_5 = \dfrac{pC_5}{1+pC_5R_5}$	$\dfrac{1}{R_1}$	$\dfrac{1}{R_2}$	pC_3	$\dfrac{1}{R_4}$	—	$\dfrac{\dfrac{1}{R_1R_2}+p\left(\dfrac{C_5R_2}{R_1R_2}+\dfrac{C_5}{R_1}+\dfrac{C_5}{R_2}\right)+p^2C_3C_5}{\dfrac{1}{R_4}\left(\dfrac{1}{R_1}+\dfrac{1}{R_2}\right)+p\left(\dfrac{C_3}{R_2}+\dfrac{C_3}{R_4}+\dfrac{C_5R_5}{R_1R_4}+\dfrac{C_5R_5}{R_2R_4}\right)+p^2C_3C_5R_5\left(\dfrac{1}{R_2}+\dfrac{1}{R_4}\right)}$	R_4, R_5, C_5 $R_5=\dfrac{1}{C_5}-b_1$ $R_4=2/b_0-1$	Nil

impedance is zero. It is of interest to consider the effect of departure from these ideal conditions on the response of the filters.

The input impedance of the amplifier used was found to be of the order of tens of megohms and its output impedance to be approximately 50Ω. The open-loop voltage gain was approximately 10000. An experimental check was carried out on the effects of changing these impedance values. First a variable resistor was connected between amplifier input terminals and the response measured. Fig. 8 shows the

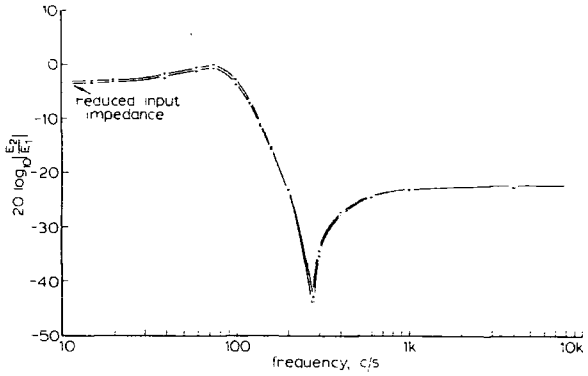

Fig. 8

Effect of reducing amplifier input impedance on filter response

measured response of the filter circuit of Fig. 3B when the amplifier input impedance is 50kΩ, together with the curve for the unmodified amplifier. It is clear from these curves that an input impedance as low as 50kΩ has very little effect on the response. Another test was carried out to find the effect of increasing the output impedance. A resistor was connected in series with the amplifier output at the position marked A in Fig. 3B. No measurable effect on the filter response was observed until this resistor was increased to about 10kΩ. It was concluded that departures from the ideal values of input and output impedances have little effect on the filter response.

The results discussed above were obtained with an amplifier circuit using valves. A transistor amplifier may be expected to have a lower input impedance than a valve amplifier. In order to reduce the effects of low input impedance of such an amplifier on the filter response, it is possible to lower the impedance level of the feedback network by choice of the denormalising factor. Another possibility arises from noting that the effect of an amplifier input resistance R_{in} may be cancelled by removing a conductance $1/\{(1 - M)R_{in}\}$ from y_4 in Fig. 2. Thus the effect of a known input resistance may be reduced or removed by adjustment of the value of the feedback resistor.

4 Alternate order of cascade

So far, an active section followed by a passive section has been considered; frequently this is satisfactory because the operational amplifier has small output impedance and presents a voltage source to the passive network. If the reverse order of cascade is required, precautions must be taken to prevent one section from loading the other. A simple method of overcoming this difficulty is to denormalise the passive network to much lower impedance level than that of the active section. This was done using the terminated Guillemin network, which has a lower output impedance, with the passive network denormalised to R = 1·592kΩ, C = 1μF, and the active network to R = 159·2kΩ, C = 0·01μF. The results obtained show very little difference with the passive network preceding or following the active section. Greatest error occurred at high frequencies, where, owing to the higher impedance of the high-pass ladder, the loading effect of the active section will be greater: the error rises to about 0·5dB.

5 High-pass filter

Considering eqn. 1,

$$D = \frac{a_0 - p^2}{b_0 - b_1 p - p^2}$$

substituting the high-pass transformation $p = \frac{1}{p}$

$$D_{HP} = \left(\frac{a_0}{b_0}\right) \frac{\left(\frac{1}{a_0} - p^2\right)}{1 - \frac{b_1}{b_0} p - p^2} \quad \ldots\ldots\ldots (24)$$

Following the procedure outlined in Section 3, and taking alternative 5 (Table 1) gives, for the active section,

$$R_4 = \frac{2b_0}{b_1}, \; R_1 = \frac{b_1}{2} \quad \ldots\ldots\ldots (25)$$

Substituting the coefficients gives the numerator

$$F = 1·6458 - 4·2916p + p^2$$
$$= (p - 3·87)(p - 0·4261) \quad \ldots\ldots\ldots (26)$$

using an arbitrary polynomial,

$$q = (p - 1)(p - 5) \quad \ldots\ldots\ldots (27)$$

and continuing the synthesis gives the network shown in Fig. 9.

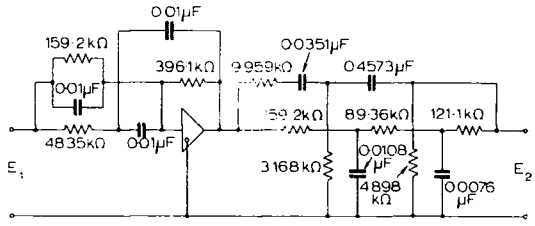

Fig. 9

Circuit diagram for high-pass filter

6 Conclusions

It has been shown that second-order responses may be produced by cascading an active section, using an operational amplifier with multiple feedback loops, and a passive section. A number of solutions have been tabulated, from which the coefficients of the elliptic response may be obtained. The general pattern emerging shows there are two simple solutions, using four standard elements in the active section, and a number of more complex solutions. Two different passive networks have been used in conjunction with the active sections derived, and, for simple responses, the method of Holt and Reineck yields the best results, as far as numbers of elements and gain are concerned. The Guillemin synthesis method becomes more useful when functions of greater complexity than the second order are considered.

The sections may be arranged with the active section preceding the passive, as shown in Fig. 1; alternatively the passive section may be placed first. When the latter method is adopted, high-order functions may be synthetised by cascading second-order stages without interaction taking place.

7 Acknowledgments

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PAPER 6

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Synthesis of multiple loop feedback systems Part I†

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This paper presents a general synthesis method for multiple loop feedback systems which is applicable to the realization of all the known configurations together with others resulting from this investigation. The active device may be an amplifier of any type, gain or phase characteristics.

The basic method utilizes an extended node introduction synthesis theory, which facilitates the generation of many possible realizations for a given function.

Although the theory developed is used to synthesize RC multi-loop feedback structures, it is equally applicable to the synthesis of RLC multi-loop feedback systems.

Rules for the numbers of active and passive node introductions are given, and a number of examples illustrate the implementation of the technique and the various transformations required.

Synthesis of various functions is considered, emphasis being laid upon the realization of those which provide filter characteristics.

1. Introduction

Multiple loop RC feedback systems in which the constraining device is a single amplifier have eluded rigorous synthesis for some time. A considerable number and variety of circuits belonging to this class of system have been reported in the literature (Aggarwal 1963, Bridgman and Brennan 1957, Nichols and Rauch 1954, Shumard 1960, Wadhwa 1962). The majority of papers so far, with the exception of (Hazony and Joseph 1964, Mitra 1967, Pande and Shukla 1965) have been directed towards obtaining these networks by a trial and error method based on analysis; a network form having been assumed *a priori* and then formulae for the network elements to simulate various transfer functions developed. This approach has many obvious drawbacks and a systematic synthesis procedure for these systems would undoubtedly be a great improvement.

The methods outlined in Hazony and Joseph (1964), Mitra (1967), Pande and Shukla (1965) present techniques applicable only to individual systems and rely upon an analysis step which reduces the problem to one of passive synthesis.

The synthesis procedure to be described is capable of producing networks having useful filter responses and provides a general synthesis method for systems constrained with one amplifier irrespective of its type, gain, or phase characteristic. This embraces all the present known single amplifier feedback type filters and others produced as a consequence of this investigation, which include systems

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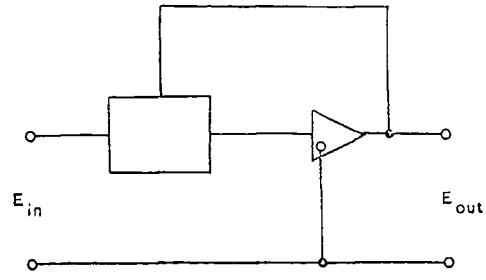
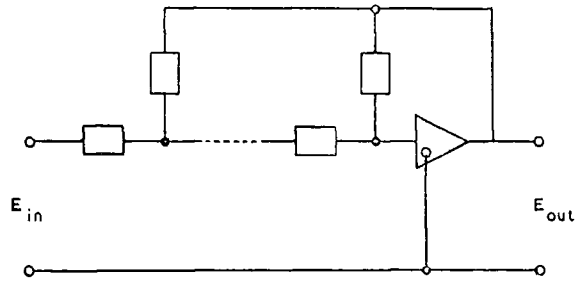
Fig. 1

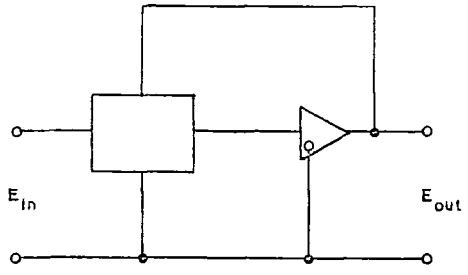


General structure.

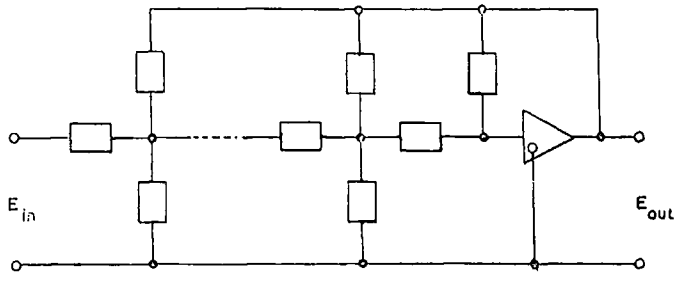


One practical realization.

(*a*)



General structure.



One practical realization.

(*b*)

(*a*) Single ladder active multi-loop structure. (*b*) Double ladder active multi-loop structure.

having feedback that is wholly negative, wholly positive or hybrid. The general form of the systems are shown in fig. 1 (a, b). Emphasis is laid upon the synthesis of RC multi-loop feedback systems, but the general theory is equally applicable to the active LCR case.

2. Node introduction synthesis

In the general work on synthesis by node introduction, Piercey (1962) has outlined a method whereby passive, and certain active networks can be synthesized by a matrix expansion technique. However, this theory is not immediately applicable to the synthesis of multiple loop structures (Sewell 1966). The reasons for this, and the modifications of the theory to overcome these difficulties, are as follows.

2.1. *The* 2×2 *node matrix*

Consider any multi-loop feedback network, constrained with, for instance, an ideal voltage amplifier at the output port of the network. The two port admittance matrix for any such network will contain entries of infinite value. It is therefore not possible, as in conventional synthesis, to commence by identifying a 2×2 matrix containing the relevant or given characteristic functions, with the two port admittance matrix of the network. Suppose the function to be synthesized is of the form:

$$G(p) = \frac{N(p)}{D(p)}, \tag{1}$$

where $N(p)$ and $D(p)$ are polynomials in p.

Normally it is possible to write a matrix

$$Y = \begin{array}{c} \\ 1 \\ n \end{array} \begin{array}{c} \begin{array}{cc} 1 & n \end{array} \\ \begin{bmatrix} y_{11} & y_{1n} \\ y_{n1} & y_{nn} \end{bmatrix} \end{array} = \begin{array}{c} \\ 1 \\ n \end{array} \begin{array}{c} \begin{array}{cc} 1 & n \end{array} \\ \begin{bmatrix} y_{11} & y_{1n} \\ \dfrac{N(p)}{Q(p)} & \dfrac{D(p)}{Q(p)} \end{bmatrix} \end{array}, \tag{2}$$

$Q(p)$ being some arbitrary divisor polynomial.

For the present systems the two port matrix will assume a general form:

$$Y = \begin{array}{c} \\ 1 \\ \\ n \end{array} \begin{array}{c} \begin{array}{cc} 1 & n \end{array} \\ \begin{bmatrix} y_{11} & y_{1n} \\ \vdots & \\ \infty & \infty \end{bmatrix} \end{array} \tag{3}$$

and the identification of polynomials and admittance parameters as in (1), (2) cannot be achieved.

To overcome this dilemma, consider another matrix, say Y^* which characterizes the performance between nodes 1 and k of an n node network, i.e.

$$Y^* = \begin{array}{c} \\ 1 \\ \\ k \end{array} \begin{array}{c} \begin{array}{cc} 1 & k \end{array} \\ \begin{bmatrix} y_{11} & y_{1k} \\ \vdots & \\ y_{k1} & y_{kk} \end{bmatrix} \end{array}, \tag{4}$$

where k is the internal pivot or reference node $1 < k < n$. Before this matrix can be utilized it is necessary to be able to determine the relationship between matrices Y and Y^*. Because of the type of network under consideration, namely networks with many loops from nodes in the forward signal path to the output node, the signal at any node in the forward path will have some simple direct relationship to the signal at the output node, i.e.

$$y_{kk} = f_1(i_k, v_k) = f_2(i_n, v_n).$$

For single and double ladder systems this linear relationship can be simply expressed by a suitable divisor polynomial, i.e. the following identification from (4), (1) is possible:

$$Y = \begin{array}{c} \\ 1 \\ k \end{array} \begin{array}{c} \begin{array}{cc} 1 & k \end{array} \\ \begin{bmatrix} y_{11}^* & y_{1k} \\ y_{k1} & \dfrac{D(p)}{Q(p)} \end{bmatrix} \end{array}, \tag{5}$$

where $Q(p)$ is some divisor polynomial. As $Q(p)$ determines the relationship between nodes k and n it is not an arbitrary function and therefore cannot be chosen as such. The choice of $Q(p)$ cannot be undertaken prior to synthesis, but must be delayed until the node introduction mechanism displays the explicit form of polynomial required.

2.2. *Expansion of the Y^* matrix*

Normally in node introduction synthesis it is necessary to expand the matrix by introduction of internal nodes, but here a slightly different approach is adopted. As the characterizing matrix represents the response of some internal part of the network and the final expanded matrix is required to represent the response at the output node, nodes are introduced which are internal as far as the Y^* matrix is concerned, but one of which will form the output node of the overall network.

For convenience k is often taken as 2, and the matrix (4) expanded node by node from 1 to n, to give:

$$Y_{n\times n} = \begin{array}{c} \\ 1 \\ 2 \\ \\ \\ \\ n \end{array} \begin{array}{c} \begin{array}{cccc} 1 & 2 & & n \end{array} \\ \left[\begin{array}{cccc} y_{11}' & y_{12}' & \cdots & y_{1n}' \\ y_{21}' & y_{22}' & \cdots & y_{2n}' \\ \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot \\ y_{n1}' & y_{n2}' & \begin{array}{cc} y'_{n-1,n-1} & y'_{n-1,n} \\ y'_{n,n-1} & y'_{nn} \end{array} \end{array}\right] \end{array}. \tag{6}$$

(The bottom right-hand 2×2 matrix includes the active (infinite) parameters.)

Hence

$$Y = Y_s + Y_u$$

where Y_s is a symmetric matrix realizable by passive means and in particular in this case is RC realizable. Y_u is an unsymmetric matrix realized by the active device. If the synthesis is performed for systems with infinite output

Fig. 2

$Y_{011}+\dfrac{(g_{12}-\theta_{12}-Y_{12})(g_{21}-\theta_{12}-Y_{21})(g_{33}+Y_{33})}{(g_{32}-\theta_{23})(g_{23}-\theta_{23})}$	$g_{12}-\theta_{12}$	$\dfrac{(g_{12}-\theta_{12}-Y_{12})(g_{33}+Y_{33})}{g_{32}-\theta_{23}}$
$g_{21}-\theta_{12}$	$Y_{022}+\dfrac{(g_{32}-\theta_{23})(g_{23}-\theta_{23})}{g_{33}+Y_{33}}$	$g_{23}-\theta_{23}$
$\dfrac{(g_{21}-\theta_{12}-Y_{21})(g_{33}+Y_{33})}{g_{23}-\theta_{23}}$	$g_{32}-\theta_{23}$	$g_{23}+Y_{33}$

(*a*)

$Y_{011}+Y_{33}\dfrac{\lambda_{12}\lambda_{21}}{\lambda_{23}\lambda_{32}}+\dfrac{\lambda_{12}\lambda_{21}\lambda_{33}}{\lambda_{23}\lambda_{32}}\left\{\dfrac{\theta_{23}}{\lambda_{23}}+\dfrac{\theta_{23}}{\lambda_{32}}\right\}$ $-\dfrac{\lambda_{33}}{\lambda_{23}\lambda_{32}}(\lambda_{12}[\theta_{12}+Y_{21}]+\lambda_{21}[\theta_{12}+Y_{12}])$	$-\theta_{12}$	$\dfrac{1}{\lambda_{32}}(\lambda_{12}Y_{33}-\lambda_{33}[\theta_{12}+Y_{12}])+\dfrac{\theta_{23}\lambda_{12}\lambda_{33}}{\lambda_{32}^{2}}$
$-\theta_{12}$	$Y_{022}-\dfrac{1}{\lambda_{33}}(\lambda_{23}\theta_{23}+\lambda_{32}\theta_{23})-\dfrac{Y_{33}\lambda_{32}\lambda_{23}}{\lambda_{33}^{2}}$	$-\theta_{23}$
$\dfrac{1}{\lambda_{23}}(\lambda_{21}Y_{33}-\lambda_{33}[\theta_{12}+Y_{21}])+\dfrac{\theta_{23}\lambda_{21}\lambda_{33}}{\lambda_{23}^{2}}$	$-\theta_{23}$	Y_{33}

+

$\dfrac{K\lambda_{12}\lambda_{21}\lambda_{33}}{\lambda_{23}\lambda_{32}}$	$K\lambda_{12}$	$\dfrac{K\lambda_{12}\lambda_{33}}{\lambda_{32}}$
$K\lambda_{21}$	$\dfrac{K\lambda_{32}\lambda_{23}}{\lambda_{33}}$	$K\lambda_{23}$
$\dfrac{K\lambda_{21}\lambda_{33}}{\lambda_{23}}$	$K\lambda_{32}$	$K\lambda_{33}$

(*b*)

(*a*) Passive node introduction. (*b*) Active node introduction.

admittance it is necessary for the last introduction to unconditionally generate an infinite parameter term in the nn position. None of the existing node introductions (Piercey 1962) are applicable in such circumstances, and it is necessary to develop introductions (type III after Piercey) to satisfy these demands (see Appendix). The appropriate passive and active introductions are shown in fig. 2 (a, b).

It will be noticed that no attention is being paid to the numerator of the original function $N(p)$. With this method of synthesis emphasis is laid primarily upon obtaining the required denominator function, and realization of the numerator function is included at a later stage.

2.3. *Number of introductions rule*

A second phenomenon which occurs in the synthesis of these multiple loop systems is concerned with the types of amplifier encountered. Piercey outlined the method by which active devices may be incorporated in node introduction synthesis, and a straightforward application of this theory is sufficient for the synthesis when the amplifier required has a matrix containing infinite terms of order no higher than unity. In many cases doubly infinite, or even triply infinite parameters occur and at first sight it may appear that new types of active node introduction are required. However, these are not necessary, since the required terms can be generated by applying the active introduction an appropriate number of times. The number of active and passive introductions required in the synthesis of single and double ladder networks are given by the following rule.

Rule 1. *If an active device, having a* 2×2 *admittance matrix containing infinite terms the highest order of which is* q, *is required in the synthesis of a rational function whose denominator is of order* m; *then the number of active introductions will be* q *and the number of passive introductions* $m-q$, *where* $q \geqslant 3$.

An exception to this rule occurs when it is required to generate a compact network in which there are fewer node introductions permissible than the order of the infinite parameters. In this case it is necessary to use an introduction having higher-order infinite parameters. If $q > 3$ then multiple-order infinite parameter introductions are also required.

3. Synthesis of finite and infinite gain amplifier systems

The developed theory embraces the synthesis of all multiple loop amplifier systems. This may be demonstrated by synthesizing some well-known amplifier filter circuits.

3.1. *Synthesis of a Sallen and Key circuit*

Synthesize the function $H/(p^2+b_1p+b_0)$ as a voltage transfer ratio using a unity gain voltage amplifier of non-reversing phase characteristic, and an RC multi-loop structure (i.e. after Sallen and Key (1955).

The amplifier has an admittance matrix:

$$Y = \begin{bmatrix} 0 & 0 \\ -K & K \end{bmatrix}_{K=\infty}. \tag{7}$$

Applying Rule 1, $m=2$, $q=1$; hence one passive and one active introduction only will be required.

Commencing with the two port admittance matrix Y and deriving the 2×2 node matrix Y^* with $k=2$.

A passive introduction is performed first, where $Y_{011}=y_{11}$; $Y_{12}=y_{12}$; $Y_{21}=y_{21}$ and are arbitrary in this example; $Y_{022}=(p^2+b_1p+b_0)/Q(p)$.

Assuming that there is no node bridging in the forward path, the 13 and 31 terms (fig. 2 (*a*)) should be zero. This can be ensured by setting $g_{12}-\theta_{12}=Y_{12}$ and $g_{21}-\theta_{12}=Y_{21}$ giving the matrix:

$Y_{3\cdot 3}=$

	1	2	3
1	Y_{011}	$g_{12}-\theta_{12}$	0
2	$g_{21}-\theta_{12}$	$Y_{022}+\dfrac{(g_{32}-\theta_{23})(g_{23}-\theta_{23})}{g_{33}+Y_{33}}$	$g_{23}-\theta_{23}$
3	0	$g_{32}-\theta_{23}$	$g_{33}+Y_{33}$

The active node introduction is then performed on the bottom right-hand 2×2 matrix. Inspection of the active matrix of the active node introduction fig. 2 (*b*) shows that in order to generate the active matrix required, all of its terms must approximate or be equal to zero except the 32 and 33 terms. To ensure this, the following identifications are made, $\lambda_{33}=1$, $\lambda_{21}=\lambda_{12}=0$, $0<\lambda_{23}\ll 1$; (if $\lambda_{23}=0$ indeterminate terms appear).

Applying this introduction gives:

$Y_{4\cdot 4}=$

	1	2	3	4
1	Y_{011}	$g_{12}-\theta_{12}$	0	0
2	$g_{21}-\theta_{12}$	$Y_{022}+\dfrac{(g_{32}-\theta_{23})(g_{23}-\theta_{23})}{g_{33}+Y_{33}}$	$-\theta_{12}'$	$\dfrac{-1}{\lambda_{32}}(\theta_{12}'+Y_{12}')$
3	0	$-\theta_{12}'$	$g_{33}+Y_{33}-\lambda_{32}\theta_{23}'$	$-\theta_{23}'$
4	0	$\dfrac{-1}{\lambda_{23}}(\theta_{12}'+Y_{21}')$	$-\theta_{23}'+\lambda_{32}K$	$Y_{33}'+K$

This matrix is of the correct form (6) and if it could be made symmetric (apart from the active terms) the object would be achieved. Symmetry around node 2 can be ensured by setting $g_{12}=g_{21}=0$. The remaining unsymmetric passive terms 24, 42, may be made symmetric as follows. If $\theta_{12}'=-Y_{21}'$ the 42 term is removed and, for convenience, set $\theta_{12}'+Y_{12}'=-\theta_{23}''$. Multiplying column 4 by $-\theta_{23}''/K$ and adding to column 2, setting $\theta_{23}'=0$ and $\lambda_{32}=-1$ gives the characteristic nodal admittance matrix of a Sallen and Key circuit.

$Y_{4\cdot 4}$

	1	2	3	4
1	Y_{011}	$-\theta_{12}$	0	0
2	$-\theta_{12}$	$Y_{022}+\dfrac{(g_{32}-\theta_{23})(g_{23}-\theta_{23})}{g_{33}+Y_{33}}$	$-\theta_{12}'$	$-\theta_{23}''$
3	0	$-\theta_{12}'$	$g_{33}+Y_{33}$	0
4	0	$-\theta_{23}''$	$-K$	$Y_{33}'+K$

(8)

For RC realizability main diagonal terms can be no more complex than first-order factors, this may be ensured by setting $Q(p)=g_{33}+Y_{33}=q_1p+q_0$. Let $(g_{32}-\theta_{23})=1$ and, assuming indefinite dominance

$$\left(a_{ii}=\sum_{\substack{j=1\\ j\neq i}}^{n}|a_{ij}|\right) \quad \text{(where each } a \text{ is a matrix element)}$$

at node 2, the 22 term is:

$$\frac{p^2+p(b_1+\theta_{23})+b_0-g_{23}}{q_1p+q_0}=\theta_{12}+\theta_{12}'+\theta_{23}''. \tag{9}$$

Various restrictions on component spread and size may now be imposed. For instance, if it is required to have all unity normalized resistors, this will give $q_0=1$.

Now,

$$g_{23}-\theta_{23}=Y_{12}'=-(\theta_{23}''+\theta_{12}'). \tag{10}$$

Let θ_{23}'', θ_{23} be frequency dependent terms, and these are equal because of indefinite dominance, i.e.

$$\theta_{23}''=f(p)=\theta_1p=\theta_{23}.$$

Hence, from eqn. (10) $g_{23}=-\theta_{12}'$. Thus (9) becomes:

$$\begin{aligned}p^2+p(b_1+\theta_{23}'')+b_0-g_{23}&=(q_1p+q_0)(\theta_{12}+\theta_{12}'+\theta_{23}'')\\&=q_1\theta_1p^2+p(\theta_1+q_1[\theta_{12}-g_{23}])+\theta_{12}-g_{23}.\end{aligned} \tag{11}$$

Comparing coefficients of (11) gives:

$$q_1\theta_1=1, \tag{12a}$$

$$b_1+\theta_{23}''=\theta_1+q_1[\theta_{12}-g_{23}], \tag{12b}$$

$$b_0-g_{23}=\theta_{12}-g_{23}. \tag{12c}$$

If

$$G(p)=\frac{1}{1+1\cdot62p+p^2}.$$

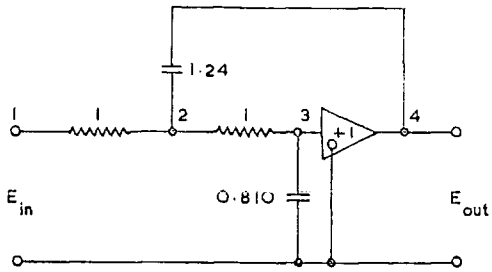
Setting $\theta_{23}=-1$ and solving 12 $(a-c)$ gives the following matrix:

$Y_{4\cdot4}=$

	1	2	3	4
1	1	-1	0	0
2	-1	$2+1\cdot24p$	-1	$-1\cdot24p$
3	0	-1	$1+0\cdot81p$	0
4	0	$-1\cdot24p$	$-K$	$1\cdot24p+K$

which gives the circuit of fig. 3.

Fig. 3



Second-order Sallen and Key circuit. For all circuit realizations the element values are in mhos and farads.

3.2. *Synthesis of a third-order multi-loop network*

Synthesize the third-order function:

$$G(p)=\frac{1}{p^3+2p^2+2p+1},$$

using a voltage operational amplifier and an RC multi-loop structure.

Applying Rule 1 with $m=3$, $q=2$ reveals that one passive and two active introductions are required. The method of synthesis is as before, one point to note is that when multiple active introductions are performed the penultimate one is of special significance. It is termed the 'K alignment node introduction' and its function is to provide infinite parameter terms in the last column of the matrix, prior to the final amplifier introduction. These terms are necessary to ensure a correct matrix when the multiple order infinite terms appear. The natural order of introductions is passive, K alignment and then the amplifier.

The 2×2 node admittance matrix Y^* ($k=2$) is:

$$Y^*=\begin{array}{c} \\ 1 \\ 2 \end{array}\begin{array}{c} \begin{array}{cc} 1 & 2 \end{array} \\ \begin{bmatrix} y_{11}^* & y_{12}^* \\ y_{21}^* & \dfrac{p^3+b_2p^2+b_1p+b_0}{Q(p)} \end{bmatrix} \end{array}. \tag{13}$$

For node introductions in (13) $Y_{011}=y_{11}^*$, $Y_{12}=y_{12}^*$, $Y_{21}=y_{21}^*$:

$$Y_{022}=\frac{p^3+b_2p^2+b_1p+b_0}{Q(p)}.$$

Applying a passive introduction with $Y_{12}=g_{12}-\theta_{12}$, $Y_{21}=g_{21}-\theta_{12}$ gives:

$$Y_{3\cdot 3}=\begin{array}{c} \\ 1 \\ 2 \\ 3 \end{array}\begin{array}{c} \begin{array}{ccc} 1 & 2 & 3 \end{array} \\ \begin{bmatrix} Y_{011} & Y_{12} & 0 \\ Y_{21} & Y_{022}+\dfrac{(g_{32}-\theta_{23})(g_{23}-\theta_{23})}{g_{33}+Y_{33}} & g_{23}-\theta_{23} \\ 0 & g_{23}-\theta_{23} & g_{33}+Y_{33} \end{bmatrix} \end{array}.$$

A K alignment introduction is now to be performed on the bottom right-hand 2×2 matrix. As transformations are necessary on the final matrix before the network realization, it is convenient to carry out some of these at this stage of the proceedings.

Concentrating on the introduction, which is an active type with $\lambda_{12} = \lambda_{21} = 0$ and $\lambda_{32} = \alpha/K$ where $K \gg \alpha$ the basic introduction matrix is then:

$$Y_K = \begin{array}{|c|c|c|} \hline Y_{011} & -\theta_{12} & -\frac{\lambda_{33}K}{\alpha}[\theta_{12} + Y_{12}'] \\ \hline -\theta_{12} & Y_{022} - \frac{\lambda_{23}\theta_{23}}{\lambda_{33}} + \frac{\alpha\lambda_{23}}{\lambda_{33}} & -\theta_{23} + K\lambda_{23} \\ \hline 0 & -\theta_{23} + \alpha & Y_{33} + K\lambda_{33} \\ \hline \end{array}$$

Let $Y_{12} = -\theta_{12} + \beta/\lambda_{33}$, hence the 13 entry is $(-K\beta/\alpha)$. Multiply column 3 by $-(\alpha/\lambda_{33}K)$ and add to column 2, multiply the bottom line by $(K\gamma/Y_{33} + K\lambda_{33})$ $(\alpha \gg \gamma)$ and add to row 1: $\beta/\lambda_{33} = (\theta_{23}\gamma/\lambda_{33})$. As $\alpha \gg \gamma$ the term $(K\beta/\alpha)$ can be subsequently neglected. The resultant matrix is now used as the node introduction giving:

$$Y_{4\times4} = \begin{array}{|c|c|c|c|c|} \hline & 1 & 2 & 3 & 4 \\ \hline 1 & Y_{011} & Y_{12} & 0 & 0 \\ \hline 2 & Y_{21} & Y_{022} + \frac{(g_{32} - \theta_{23})(g_{23} - \theta_{23})}{g_{33} + Y_{33}} & -\theta_{12}' & K\gamma \\ \hline 3 & 0 & -\theta_{12}' & g_{33} + Y_{33} - \frac{\lambda_{23}\theta_{23}'}{\lambda_{33}} & -\theta_{23}' + K\lambda_{23} \\ \hline 4 & 0 & 0 & -\theta_{23}' & Y_{33}' + K\lambda_{33} \\ \hline \end{array}$$

The final active introduction is performed on the bottom right-hand 2×2 matrix, with $\lambda_{12} = \lambda_{21} = 0$, $\lambda_{33} = 1$, $0 < \lambda_{23} \ll 1$. After further transformation the matrix of eqn. (14) results.

$$\begin{array}{|c|c|c|c|c|c|} \hline & 1 & 2 & 3 & 4 & 5 \\ \hline 1 & Y_{011} & Y_{12} & 0 & 0 & 0 \\ \hline 2 & Y_{21} & Y_{022} + \frac{(g_{32} - \theta_{23})(g_{23} - \theta_{23})}{g_{33} + Y_{33}} & -\theta_{12}' & 0 & -\gamma \\ \hline 3 & 0 & -\theta_{12}' & g_{33} + Y_{33} - \frac{\lambda_{23}\theta_{23}'}{\lambda_{33}} & -\theta_{12}'' & -\lambda_{23} \\ \hline 4 & 0 & 0 & -\theta_{12}'' & Y_{33}' & -\theta_{23}'' \\ \hline 5 & 0 & -\gamma & -\lambda_{23} & -\theta_{23}'' + K^2 & Y_{33}'' + K \\ \hline \end{array} \quad (14)$$

Setting $Y_{12} = Y_{21} = y_{12}$ and collecting the various parameter relationships:

$$g_{23} - \theta_{23} = Y_{12}' = -\theta_{12}' + \frac{\beta}{\lambda_{33}},$$

$$g_{23} = \frac{\beta}{\lambda_{33}}, \quad \theta_{12}' = \theta_{23}, \quad g_{32} - \theta_{23} = Y_{21}',$$

let

$$g_{32}=0,$$

$$\beta=\theta_{23}\gamma, \quad \lambda_{33}=\theta_{23}'', \quad \theta_{12}''=\theta_{23}'.$$

Now examine the dominance conditions at the appropriate nodes.

Node 4

This is the amplifier input node, i.e. a virtual earth point and therefore indefinite dominance is desired, thus:

$$Y_{23}'=\theta_{12}''+\theta_{23}''. \tag{15}$$

Node 3

Definite dominance

$$\left((a_{ii}>\sum_{\substack{j=1\\ j\neq i}}^{k}|a_{ij}|\right) \quad \text{(where each } a \text{ is a matrix element)}$$

is possible here; introduce a term θ' to allow for this:

$$g_{33}+Y_{33}-\frac{\lambda_{23}\theta_{23}'}{\lambda_{33}}=\theta_{12}'+\theta_{12}''+\lambda_{23}+\theta'. \tag{16}$$

Node 2

Definite dominance is also possible here; introduce a term θ'' to allow for this:

$$Y_{022}-\frac{\theta_{23}(\beta/\lambda_{33}-\theta_{23})}{g_{33}+Y_{33}}=\theta_{12}'+\gamma+y_{12}+\theta''. \tag{17}$$

Substituting in (16) from (17) for the term $g_{33}+Y_{33}$ gives:

$$Y_{022}-\frac{\theta_{23}(\beta/\lambda_{33}-\theta_{23})}{\theta_{12}'+\theta_{12}''+\lambda_{23}+\theta'+(\lambda_{23}\theta_{23}'/\lambda_{33})}=\theta_{12}'+\gamma+y_{12}+\theta''. \tag{18}$$

At this point there are a number of alternative methods for producing a final circuit. One method, which yields an already known circuit form, is to divide the fraction of (18) top and bottom by $\lambda_{23}\theta_{23}'/\lambda_{33}$: as $\theta_{23}=\theta_{12}'$ this gives:

$$Y_{022}-\frac{(\theta_{12}'\beta-\lambda_{33}\theta_{12}'^{2})/\lambda_{23}\theta_{23}'}{(\lambda_{33}/\lambda_{23}\theta_{23}')(\theta_{12}'+\theta_{12}''+\theta'+\lambda_{23})+1}=\theta_{12}'+\gamma+y_{12}+\theta''. \tag{19}$$

Choose $Q(p)$ to be equal to the denominator of the fraction, thus:

$$\frac{p^3+b_2p^2+b_1p+b_0-(\theta_{12}'\beta-\lambda_{33}\theta_{12}'^{2})/\lambda_{23}\theta_{23}'}{(\lambda_{33}/\lambda_{23}\theta_{23}')(\theta_{12}'+\theta_{12}''+\lambda_{23}+\theta')+1}=\theta_{12}'+\gamma+y_{12}+\theta''. \tag{20}$$

Synthesis continues by making the following simple assumptions:

(i) As the function is characteristic of a low pass filter, the excess dominance terms are the frequency dependent ones.

(ii) To complete a second-order factor necessary for cancellation, let:

$$\lambda_{33} = f(p) = k_{33}p.$$

(iii) All resistances in the final network are equal in value, i.e.

$$y_{21} = \theta_{12}' = \theta_{12}'' = \lambda_{23} = \gamma = \Theta.$$

Equation (20) then becomes:

$$p^3 + b_2p^2 + p\left(b_1 + \frac{k_{33}\Theta^2}{\lambda_{23}\theta_{23}'}\right) + b_0 - \Theta$$

$$= \left\{p^2\frac{\theta' k_{33}}{\lambda_{23}\theta_{23}'} + 3p\frac{k_{33}\Theta}{\lambda_{23}\theta_{23}'} + 1\right\}\left\{3\Theta + p\theta''\right\}.$$

Simplifying and dividing the right-hand side by $(\theta'\theta'' k_{33}/\lambda_{23}\theta_{23})$ (θ', θ'' are now assumed to be multipliers of p), gives:

$$p^3 + b_2p^2 + b_1p + b_0 = k\left[p^3 + \frac{p^2}{\theta'\theta'' k_{33}}\{3\theta'' k_{33}\Theta + 3\Theta\theta' k_{33}\}\right.$$

$$+ p\frac{\lambda_{23}\theta_{23}'}{\theta'\theta'' k_{33}}\left\{\theta'' + 9\frac{\Theta^2 k_{33}}{\lambda_{23}\theta_{23}'} - \frac{k_{33}\Theta^2}{\lambda_{23}\theta_{23}'}\right\}$$

$$\left. + 4\frac{\Theta\lambda_{23}\theta_{23}'}{\theta'\theta'' k_{33}}\right].$$

Disregarding the constant multiplier and equating coefficients gives:

$$b_0 = \frac{4\Theta\lambda_{23}\theta_{23}'}{\theta'\theta'' k_{33}}, \tag{21}$$

$$b_1 = \frac{\lambda_{23}\theta_{23}'}{\theta' k_{33}} + \frac{8\Theta^2}{\theta'\theta''}, \tag{22}$$

$$b_2 = 3\Theta\left\{\frac{1}{\theta'} + \frac{1}{\theta''}\right\}. \tag{23}$$

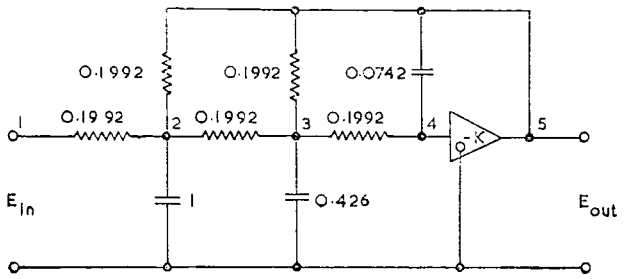
For the numerical function given, θ'' is chosen as unity. Solving eqns. (15), (21)–(23) then yields the matrix:

$Y_{5\cdot5} =$

	1	2	3	4	5
1	0·1992	−0·1992	0	0	0
2	−0·1992	$p + 0{\cdot}5976$	−0·1992	0	−0·1992
3	0	−0·1992	$0{\cdot}426p + 0{\cdot}5976$	−0·1992	−0·1992
4	0	0	−0·1992	$0{\cdot}1992 + p0{\cdot}0742$	$-p0{\cdot}742$
5	0	−0·1992	−0·1992	$-0{\cdot}0742p + K^2$	$0{\cdot}0742p + 0{\cdot}3984 + K$

This gives the circuit shown in fig. 4, a third-order multi-loop feedback filter (Wadhwa 1962).

Fig. 4



Third-order multi-loop circuit.

There are many possible variations of this synthesis process, particularly regarding the choice of divisor polynomial, realizability constants and non-excess dominance terms.

4. Conclusion

The synthesis technique outlined provides a method whereby multi-loop feedback systems may be synthesized in a rigorous manner. As the method requires the determination of one or more roots of a polynomial of order equal to the denominator of the characteristic function, high-order network functions demand the use of a digital computer. With increase in order, the number and complexity of node introductions increase and the transformation work is also multiplied.

The synthesis technique permits the inclusion of any type of amplifier, e.g. voltage, current transadmittance, transimpedance, finite or infinite gain, as the constraining device of a multi-loop feedback network. Whether the device is ideal or not is of no consequence as it is possible to incorporate the non-idealities in the synthesis.

The method is applicable to the realization of both transfer ratios and driving point imittances.

Constraints concerning component ratios have been used here, but the introduction of others determining sensitivity is also a feasible extension.

As with many synthesis techniques there are usually numerous physical realizations of a specific function, the examples shown here illustrate some realizations of various transfer functions. It was indicated at various points during the synthesis of these networks that, had other identifications been made, different networks would result. The method does not restrict realization to one particular form, but can be used to display different ones.

The functions synthesized here all have constant numerators, and therefore no emphasis was laid upon numerator realization. Numerator inclusion is the subject considered in a further communication.

Acknowledgment

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Appendix

The derivation of the required node introductions is presented here. Following the normal derivation (Piercey 1962), i.e. commencing with a 2×2 matrix:

$$Y_{2\cdot 2} = \begin{bmatrix} Y_{011} & Y_{12} \\ Y_{21} & Y_{022} \end{bmatrix},$$

using a 1-node introduction gives:

$$Y_{3\cdot 3} = \begin{array}{|c|c|c|} \hline Y_{011}+a_1A_1 & Y_{12}+a_2A_1 & a_3A_1 \\ \hline Y_{21}+a_1A_2 & Y_{022}+a_2A_2 & a_3A_2 \\ \hline a_1A_3 & a_2A_3 & a_3A_3 \\ \hline \end{array}. \tag{24}$$

$$\left.\begin{aligned} a_3A_3 &= g_{33} + Y_{33}, \\ a_2A_3 &= g_{32} - \theta_{23}, \\ a_3A_2 &= g_{23} - \theta_{23}, \\ a_2A_1 &= g_{12} - \theta_{12} - Y_{12}, \\ a_1A_2 &= g_{21} - \theta_{12} - Y_{21}, \end{aligned}\right\} \tag{25}$$

where the g's are frequency independent terms, θ's and Y's can be functions of the complex frequency variable.

By substitution the remaining unknowns may be determined:

$$a_2A_2 = \frac{(g_{32}-\theta_{23})(g_{23}-\theta_{23})}{g_{33}+Y_{33}},$$

$$a_1A_3 = \frac{(g_{21}-\theta_{12}-Y_{21})(g_{32}-\theta_{23})(g_{33}+Y_{33})}{(g_{32}-\theta_{23})(g_{23}-\theta_{23})},$$

$$a_3A_1 = \frac{(g_{12}-\theta_{12}-Y_{12})(g_{23}-\theta_{23})(g_{33}+Y_{33})}{(g_{32}-\theta_{23})(g_{23}-\theta_{23})},$$

$$a_1A_1 = \frac{(g_{12}-\theta_{12}-Y_{12})(g_{21}-\theta_{12}-Y_{21})(g_{33}+Y_{33})}{(g_{32}-\theta_{23})(g_{23}-\theta_{23})}.$$

Substituting in (24) yields the passive node introduction as shown in fig. 2(*a*).

Active devices can be taken account of by the introduction of infinite parameters, these are obtained by setting $g_{ij} = \lambda_{ij}K$, $(K \to \infty)$. The resulting expressions are then expanded in a Taylor series and any term which is divided by K or higher powers of K is neglected. The frequency independent constraint on g_{ij} is now removed, i.e. λ_{ij} may be a function of frequency; K is a real constant.

Equations (25) now become:

$$\begin{aligned} a_3A_3 &= \lambda_{33}K + Y_{33}, \\ a_2A_3 &= \lambda_{32}K - \theta_{23}, \\ a_3A_2 &= \lambda_{23}K - \theta_{23}, \\ a_2A_1 &= \lambda_{12}K - \theta_{12} - Y_{12}, \\ a_1A_2 &= \lambda_{21}K - \theta_{12} - Y_{21}. \end{aligned}$$

After expansion

$$a_2A_2 = \frac{K\lambda_{23}\lambda_{32}}{\lambda_{33}} - \frac{(\lambda_{23}\theta_{23}+\lambda_{32}\theta_{23})}{\lambda_{33}} - \frac{Y_{33}\lambda_{32}\lambda_{23}}{\lambda_{33}^2},$$

$$a_3A_1 = \frac{K\lambda_{12}\lambda_{33}}{\lambda_{32}} + \frac{1}{\lambda_{32}}(\lambda_{12}Y_{33} - \lambda_{33}[\theta_{21}+Y_{12}]) + \frac{\theta_{23}\lambda_{12}\lambda_{33}}{\lambda_{32}^2},$$

$$a_1A_3 = \frac{K\lambda_{21}\lambda_{33}}{\lambda_{23}} + \frac{1}{\lambda_{23}}(\lambda_{21}Y_{33} - \lambda_{33}[\theta_{21}+Y_{21}]) + \frac{\theta_{23}\lambda_{21}\lambda_{33}}{\lambda_{23}^2},$$

$$a_1A_1 = \frac{K\lambda_{12}\lambda_{21}\lambda_{33}}{\lambda_{23}\lambda_{32}} - \frac{\lambda_{33}}{\lambda_{23}\lambda_{32}}(\lambda_{12}[\theta_{12}+Y_{21}]+\lambda_{21}[\theta_{12}+Y_{12}])$$
$$+ \frac{\lambda_{12}\lambda_{21}\lambda_{33}}{\lambda_{23}\lambda_{32}}\left(\frac{\theta_{23}}{\theta_{23}} + \frac{\theta_{23}}{\lambda_{32}}\right) + \frac{Y_{33}\lambda_{12}\lambda_{21}}{\lambda_{23}\lambda_{32}}.$$

These terms are substituted in the matrix of eqn. (24), and separating the terms in K into a separate (active) matrix, leaving the finite parameters in the passive matrix, gives the required active node introduction as shown in fig. 2(*b*).

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PAPER 7

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Synthesis of multiple loop feedback systems Part III†

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Synthesis of all-pole functions has already been demonstrated. The paper describes the extension of the method to realize various types of rational functions which are used in filter networks.

The method is demonstrated on known networks and in the synthesis of a new class of parallel systems. The technique of numerator inclusion by choice of divisor polynomial and 'branch introduction' are shown.

The transformation from the nodal matrix to the node matrix for the parallel systems is formulated and Number of Introductions Rule for such systems is given.

1. Introduction

The general method of synthesis of multi-loop feedback systems has already been described (Holt and Sewell 1968), with particular emphasis on the synthesis of functions with constant numerators. Many useful network functions have numerators that are polynomials and it is therefore necessary to include the realization of a numerator polynomial in the synthesis.

2. Numerator polynomial inclusion

As can be appreciated there is not complete liberty to synthesize any conceivable numerator polynomial with any particular denominator polynomial when dealing with these multi-loop systems. For, although in certain circumstances the denominator is not affected by the numerator, the numerator is never totally independent of the denominator. There are a number of ways of including the numerator polynomial according to the form of the function.

2.1. *Numerator inclusion by choice of divisor polynomial*

If the numerator consists of a single term, which is not simply a constant, the method is to proceed through the synthesis as outlined for realizing the given denominator function. Then by suitable choice of the divisor polynomial $Q(p)$, the required numerator is produced.

Consider the synthesis of the function

$$G(p) = \frac{Hp}{p^2 + 3p + 3}$$

by a multi-loop network using an infinite gain voltage amplifier. Applying Rule 1 (Holt and Sewell 1968), $m = 2$, $q = 2$, thus all introductions are of the active

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type. Performing these as shown previously will yield a matrix:

$$Y_{4\cdot4}=\begin{array}{c|cccc} & 1 & 2 & 3 & 4 \\ \hline 1 & Y_{011} & -\theta_{12} & 0 & 0 \\ 2 & -\theta_{12} & Y_{022}-\dfrac{\lambda_{23}\theta_{23}}{\lambda_{33}} & -\theta_{12}' & -\lambda_{23} \\ 3 & 0 & -\theta_{12}' & Y_{33} & -\theta_{23}' \\ 4 & 0 & -\lambda_{23} & -\theta_{23}'+K^2 & Y_{33}'+K \end{array} \qquad (1)$$

As the numerator function contains a term in p, the appropriate co-factor should produce this term. Setting $\theta_{12}=p$ will achieve this end. Examine dominance conditions: assuming indefinite dominance at node 3, and since no excess dominance term is required to supply frequency dependent terms, indefinite dominance at node 2 is possible.

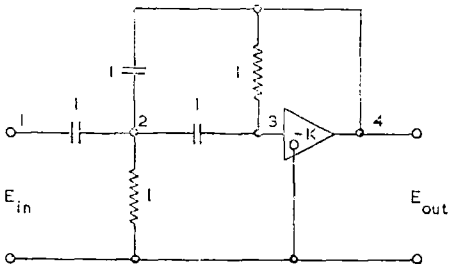
With $\lambda_{33}=k_{33}p$, $Q(p)=p$ the realization equation at node 2 is:

$$\frac{p^2+3p+3-\lambda_{23}\theta_{23}/k_{33}}{p}=p+\theta_{12}'+\lambda_{23}.$$

Setting $(\lambda_{23}\theta_{23}/k_{33})=3$ will give $\lambda_{23}+\theta_{12}'=3$. if $\theta_{12}'=\theta_{23}$ then $\lambda_{23}^2-3\lambda_{23}+3k_{33}=0$; $k_{33}=\frac{5}{12}$ gives convenient roots yielding $\lambda_{23}=\frac{1}{2}$ or $\frac{5}{2}$. $\theta_{12}'=\frac{5}{2}$ or $\frac{1}{2}$. Taking the first root yields the circuit shown in fig. 1.

Other numerator functions of this type may be realized in a similar manner.

Fig. 1



Multi-loop circuit for a function having a second-order denominator and first-order numerator.

2.2. *Branch introduction*

When the numerator function is a complete polynomial of the same order as the denominator, the method of synthesizing the denominator is again followed. Suitable terms can then be added into the matrix which have a desired modifying effect on the numerator but have no effect on the denominator. For example:

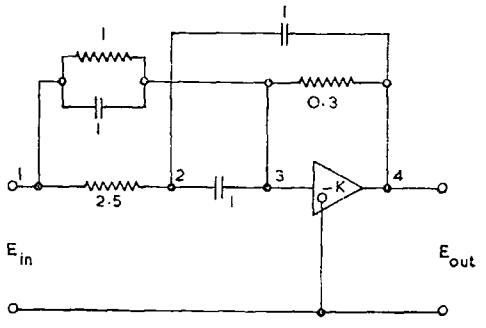
$$\text{synthesize the function } G(p)=\frac{1\cdot25+3\cdot5p+p^2}{0\cdot76+0\cdot6p+p^2}.$$

Synthesis of the denominator function proceeds as before (§ 2.1). The numerator is of the same order as the denominator, so that the divisor polynomial $Q(p)$ need only be a constant, e.g. $Q(p)=k$, also let $\lambda_{33}=k$. Examining dominance conditions at node 2 gives:

$$\frac{0{\cdot}76+0{\cdot}6p+p^2-\lambda_{23}\theta_{23}}{k}=\theta_{12}+\theta_{12}{}'+\lambda_{23}.$$

To permit reduction, let $\lambda_{23}=\theta_{23}=p$ and $\theta_{12}{}'=\theta_{23}$ thus yielding $k=0{\cdot}3$ and $\theta_{12}=2{\cdot}5$. If the numerator co-factor is now evaluated it appears to fail to produce the required function. Examining the matrix again, it is seen that if a term is introduced in the 13, 31 positions, the denominator co-factor is unaltered but the numerator may be affected at will. If this term is $(1+p)$ the required numerator function is realized. The circuit is shown in fig. 2. This last step is known as 'branch introduction' and is extremely important in the realization of multi-loop systems characterized by rational functions.

Fig. 2



Multi-loop realization of a biquadratic function.

The question of synthesizing functions having imaginary and right-half plane zeros now arises. The latter has been dealt with elsewhere (Sewell 1966) and the former problem will be dealt with in the next section.

3. Parallel system synthesis

The general systems so far described cannot produce imaginary axis zeros unless some degree of positive feedback is introduced. For sensitivity and stability it is often advisable to avoid such a step and the following shows how this is achieved.

Consider a general rational transfer function:

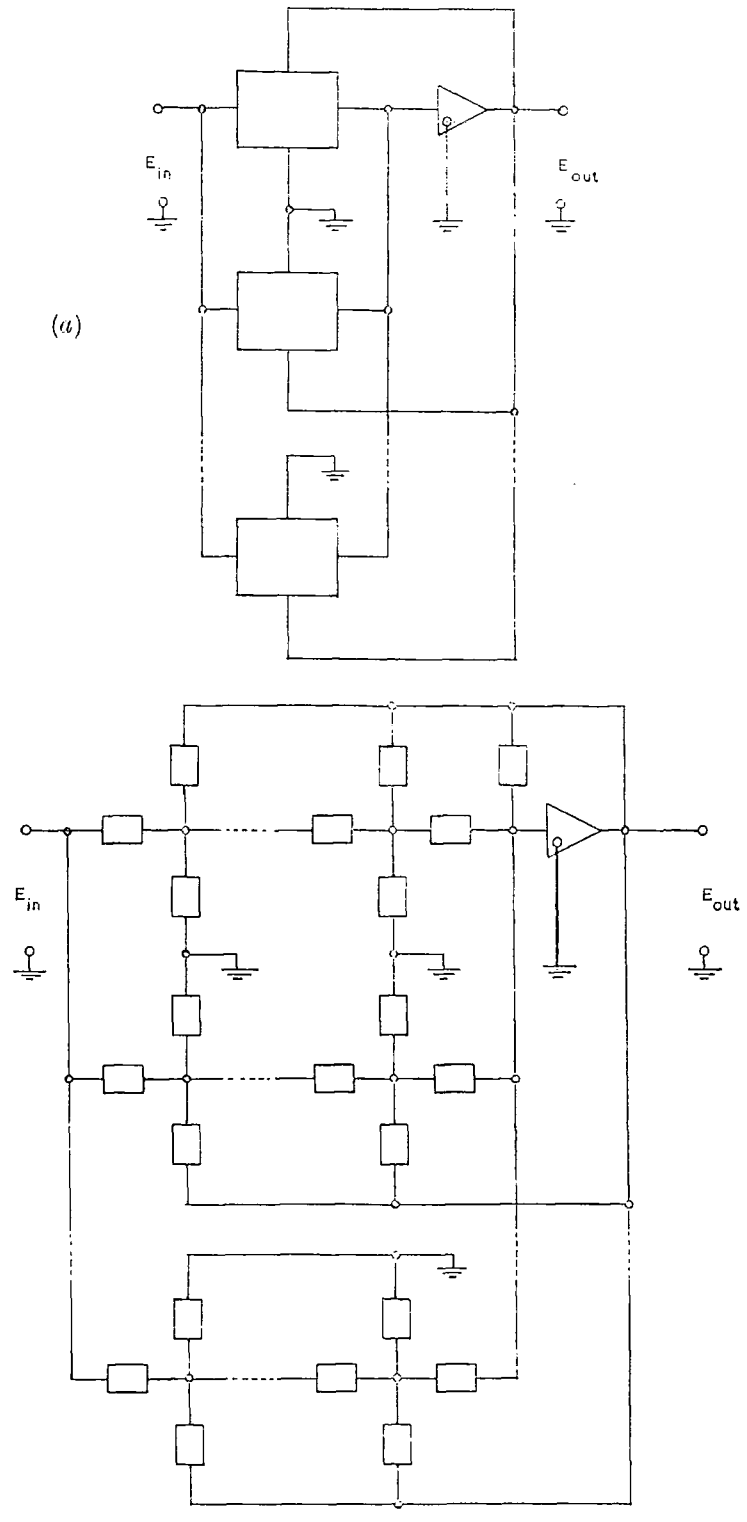
$$G(p)=\frac{N(p)}{D(p)}$$

this may be written as:

$$G(p)=\sum_{i=1}^{r}\frac{N_i(p)}{D(p)},$$

where N_i are single or groups of numerator terms, r being their number.

Fig. 3



Double ladder active multi-loop structure. (*a*) General structure. (*b*) One realization.

This suggests a parallel ladder synthesis method and the form of system which results is shown in fig. 3. This approach therefore presents a method of realizing numerator functions not included by the previous techniques.

In the work presented here the following assumptions are made:

(i) The array of elements in the system will be of a symmetrical form, i.e. each passive ladder has the same number of nodes.

(ii) Each ladder is responsible for one term of the numerator function.

With these constraints, the following rule is postulated.

3.1. *Number of introductions rule*

Rule 2. If an active device, having a 2 × 2 admittance matrix containing infinite terms the highest order of which is q, is required in the synthesis of a rational function whose denominator is of order m, and r is the number of terms in the numerator polynomial: the number of active introductions required will be q and the number of passive introductions is $m-q+(m-1)^{r-1}$.

Where $q \geqslant 3$, and for $q=3$ it is again possible, and occasionally necessary, to use the multiple-order infinite parameter introductions.

3.2. *The 2 × 2 node matrix*

The only alteration required in the synthesis procedure to incorporate these parallel systems is connected with the determination of the Y^* matrix. In the cases of single and double-ladder systems the transformation was accomplished via a simple divisor polynomial, whereas here subtractive terms are necessary to effect the transformation.

Thus the Y^* matrix becomes:

$$Y^* = \begin{array}{c} \\ 1 \\ k \end{array} \begin{array}{c} \begin{array}{cc} 1 & k \end{array} \\ \begin{bmatrix} y_{11}^* & y_{1}{}_{k}^* \\ y_{k1} & \dfrac{D(p)}{Q(p)} - \displaystyle\sum_{i=1}^{r-1} f_i(p) \end{bmatrix} \end{array}$$

where $D(p)$ is the denominator of the rational function, and $Q(p)$ a divisor polynomial. The $f_i(p)$ functions are determined during synthesis and depend upon the characteristics of the individual ladders, i.e. they express the relationship between the voltage and current at the reference node in one ladder and those at various nodes in other ladders.

The following example illustrates the method.

3.3. *Synthesis of a second-order elliptic function*

Synthesize a second-order elliptic function:

$$G(p) = \frac{p^2 + a_0}{p^2 + b_1 p + b_0}, \tag{2}$$

as a voltage transfer ratio, employing an RC multi-loop feedback circuit and a voltage operational amplifier.

With $k=2$ the matrix is:

$$Y^* = \begin{array}{c} \\ 1 \\ 2 \end{array} \begin{array}{c} \begin{array}{cc} 1 & 2 \end{array} \\ \begin{bmatrix} y_{11}^* & y_{12}^* \\ y_{21}^* & \dfrac{p^2+b_1p+b_0}{Q(p)} - f_1(p) \end{bmatrix} \end{array}.$$

If

$$Y_{022} = \frac{p^2+b_1p+b_0}{Q(p)} \quad \text{and} \quad Y_{022}^* = Y_{022} - f_1(p),$$

then the matrix from which synthesis proceeds is:

$$Y^* = \begin{array}{c} \\ 1 \\ 2 \end{array} \begin{array}{c} \begin{array}{cc} 1 & 2 \end{array} \\ \begin{bmatrix} Y_{011} & Y_{12} \\ Y_{21} & Y_{022}^* \end{bmatrix} \end{array},$$

$y_{11}^* = Y_{011}$, $y_{12}^* = Y_{12}$, $y_{21}^* = Y_{21}$. Rule 2 ($m=2$, $q=2$ and $r=2$), shows that one passive and two active introductions are required.

Performing the passive introduction with $g_{12}=g_{21}=0$ and $\theta_{23}'=0$ gives:

$Y_{3\cdot3} =$

	1	2	3
1	$Y_{011} + \dfrac{(\theta_{12}+Y_{12})(\theta_{12}-Y_{21})(g_{33}+Y_{33})}{g_{23}g_{32}}$	$-\theta_{12}$	$-\dfrac{(\theta_{12}-Y_{12})(g_{33}-Y_{33})}{g_{32}}$
2	$-\theta_{12}$	$Y_{022}^* + \dfrac{g_{23}g_{32}}{g_{33}+Y_{33}}$	g_{23}
3	$-\dfrac{(\theta_{12}+Y_{21})(g_{33}+Y_{33})}{g_{23}}$	g_{32}	$g_{33}+Y_{33}$

Applying a K alignment introduction to the bottom right-hand 2×2 matrix, with $\lambda_{12}=\lambda_{21}=\theta_{12}=0$:

$Y_{4\cdot4} =$

	1	2	3	4
1	Y_{011}'	$-\theta_{12}$	$-\dfrac{(\theta_{12}+Y_{12})(g_{33}-Y_{33})}{g_{32}}$	0
2	$-\theta_{12}$	$Y_{022}^* + \dfrac{g_{23}g_{32}}{g_{33}-Y_{33}}$	0	$-\dfrac{\lambda_{33}g_{23}}{\lambda_{32}}$
3	$-\dfrac{(\theta_{12}+Y_{12})(g_{33}-Y_{33})}{g_{23}}$	0	$g_{33}+Y_{33}-\dfrac{\lambda_{23}\theta_{23}'}{\lambda_{33}}-\dfrac{\alpha\lambda_{23}}{\lambda_{33}}$	$-\theta_{23}'+K\lambda_{23}$
4	0	$-\dfrac{\lambda_{33}g_{32}}{\lambda_{23}}$	$-\theta_{23}'+\alpha$	$Y_{33}+K\lambda_{33}$

Performing the matrix manipulation outlined for the third-order K alignment (Holt and Sewell 1968), multiplying the bottom row by $-g_{32}\lambda_{23}K$ and adding to row 2 gives a matrix in which a final active introduction yields the matrix shown in eqn. (3) (see p. 506).

For symmetry, $\lambda_{33}'' = K$, $\theta_{23}'' = \lambda_{33}$, $\theta_{12}'' = \theta_{23}'$:

$$\frac{(\theta_{12} + Y_{12})(g_{33} + Y_{33})}{g_{32}} = \frac{(\theta_{12} + Y_{21})(g_{33} + Y_{33})}{g_{23}} = \theta_{13}.$$

examining dominance conditions at nodes 2, 3, 4.

Node 2

Here definite dominance is possible:

$$Y_{022}{}^{*} + \frac{g_{23}g_{32}}{g_{33} + Y_{33}} - \frac{g_{32}\gamma}{\lambda_{23}} = \frac{\lambda_{33}g_{32}}{\lambda_{23}} + \gamma + \theta_{12} + y_{22}. \tag{4}$$

Node 3

Again definite dominance is possible:

$$g_{33} + Y_{33} - \frac{\lambda_{23}\theta_{23}'}{\lambda_{33}} = \theta_{12}'' + \lambda_{23} + \theta_{13} + y_{33}. \tag{5}$$

Node 4

This is the virtual earth node and thus only indefinite dominance is practical:

$$Y_{33}' = \theta_{23}'' + \theta_{12}'' + \frac{\lambda_{33}g_{32}}{\lambda_{23}}. \tag{6}$$

At the output node:

$$Y_{33}'' = \gamma + \lambda_{23} + \theta_{23}''.$$

Now $f_1(p)$ expresses the relationship between the variables at nodes 2 and 3, a convenient choice for $f_1(p)$ which not only fulfils this requirement but simplifies (3) is:

$$f_1(p) = \frac{g_{23}g_{32}}{g_{33} + Y_{33}} + \frac{\lambda_{23}\theta_{23}'}{\lambda_{33}}.$$

Equation (4) becomes:

$$Y_{022} - \frac{g_{32}\gamma}{\lambda_{23}} - \frac{\lambda_{23}\theta_{23}'}{\lambda_{33}} = \frac{\lambda_{33}g_{32}}{\lambda_{23}} + \gamma + \theta_{12} + y_{22}.$$

If $Q(p) = p$, $\lambda_{33} = k_{33}p$ and $\lambda_{23} \to \lambda_{23}p$. Then

$$\frac{p^2 + b_1 p + b_0}{p} - \frac{g_{32}\gamma}{\lambda_{23}p} - \frac{\lambda_{23}\theta_{23}'}{k_{33}} = \frac{k_{33}g_{32}}{\lambda_{23}} + \gamma + \theta_{12} + y_{22}.$$

If $b_0 = (g_{32}\gamma)/\lambda_{23}$, then:

$$p + b_1 - \frac{\lambda_{23}\theta_{23}'}{k_{33}} = \frac{k_{33}g_{32}}{\lambda_{23}} + \gamma + \theta_{12} + y_{22}. \tag{7}$$

	1	2	3	4	5
1	Y_{011}'	$-\theta_{12}$	$-\dfrac{(\theta_{12}+Y_{12})(g_{33}+Y_{33})}{g_{32}}$	0	0
2	$-\theta_{12}$	$Y_{022}^{*}+\dfrac{g_{32}g_{23}}{g_{33}+Y_{33}}-\dfrac{\lambda_{32}g_{32}\gamma}{\lambda_{23}\lambda_{33}}$	0	$-\dfrac{\lambda_{32}g_{32}}{\lambda_{23}}$	γ
3	$-\dfrac{(\theta_{12}+Y_{21})(g_{33}+Y_{33})}{g_{23}}$	0	$g_{33}+Y_{33}-\dfrac{\lambda_{23}\theta_{23}'}{\lambda_{33}}$	θ_{12}''	λ_{23}
4	0	$-\dfrac{\lambda_{32}g_{32}}{\lambda_{23}}$	θ_{12}''	Y_{33}'	θ_{23}''
5	0	$-\gamma$	$-\lambda_{23}$	$\theta_{23}''+K^2$	$Y_{33}''+K^2$

(::)

Now the function under consideration will require at least one high-pass and one low-pass ladder in a parallel configuration. For the low pass branch the periodic term is associated with the excess dominance term as usual, thus from (7):

$$b_1 = \theta_{24} + \gamma + \theta_{12} + \frac{\lambda_{23}\theta_{23}'}{k_{33}}.$$

where $\theta_{24} = (k_{33}g_{32})'\lambda_{23}$ or

$$b_1 = \theta_{24} + \gamma + \theta_{12} + \frac{b_0\lambda_{23}\theta_{23}'}{\theta_{24}\gamma}. \tag{8}$$

For a symmetrical network, and to ensure cancellation of unwanted numerator terms, it is necessary that eqns. (4) and (5) are equal.

In the high-pass branch the periodic term is associated with the series elements, thus:

$$b_1 = y_{33} + \lambda_{23} + \frac{b_0\lambda_{23}\theta_{23}'}{\theta_{24}\gamma}. \tag{9}$$

Substituting for γ in (8) gives:

$$b_1 = \theta_{24} + \frac{b_0\lambda_{23}\theta_{23}'}{b_1 - (y_{33} + \lambda_{23})} + \theta_{12} + b_1 - (y_{33} + \lambda_{23}). \tag{10}$$

If the numerator co-factor Δ_{15} of the matrix is evaluated, then provided the above cancellation conditions are valid, the numerator is:

$$N(p) = \theta_{12}\theta_{24} + \theta_{13}\theta_{23}'. \tag{11}$$

It has already been determined that θ_{13}, θ_{23}' are frequency dependent, thus let $\theta_{13} \to \theta_{13}p$, $\theta_{23}' \to \theta_{23}'p$. Thus from (11) and (2) (neglecting any constant multiplier produced):

$$a_0 = \frac{\theta_{12}\theta_{24}}{\theta_{13}\theta_{23}'} \quad \text{or} \quad \theta_{12} = \frac{a_0\theta_{13}\theta_{23}'}{\theta_{24}}. \tag{12}$$

For symmetry of the circuit components it is convenient to let:

$$\theta_{13} + \theta_{23}' = 1.$$

Substituting for θ_{13} in (12) gives:

$$\theta_{12} = a_0\theta_{23}'(1 - \theta_{23}')'\theta_{24}.$$

Substituting in (10) for θ_{12} yields:

$$\theta_{24}^2(b_1 - [y_{33} + \lambda_{23}]) + \theta_{24}(b_1 - [y_{33} + \lambda_{23}])(-[y_{33} + \lambda_{23}]) + a_0(1 - \theta_{23}')\theta_{23}'(b_1 - [y_{33} + \lambda_{23}]) + b_0\lambda_{23}\theta_{23}' = 0. \tag{13}$$

Solutions of this equation are possible for elliptic functions. Take the numerical example:

$$G(p) = \frac{p^2 + 7{\cdot}464}{p^2 + 0{\cdot}6975p + 0{\cdot}7559}.$$

It is advantageous to have as many equal components as possible, hence choose $y_{33}=\lambda_{23}=0{\cdot}1$ and $\theta_{23}'=0{\cdot}001$ then (13) becomes:

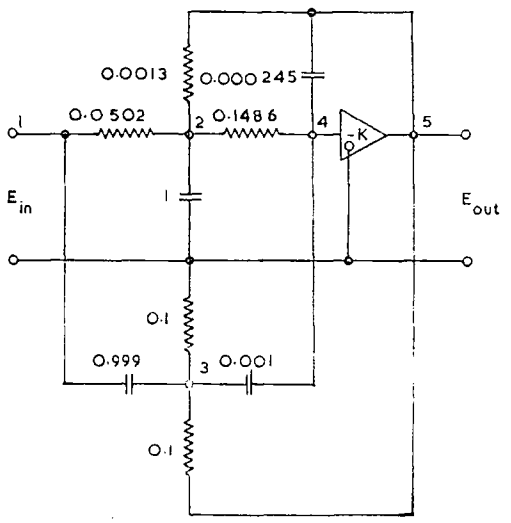
$$0{\cdot}4075\theta_{24}^2-0{\cdot}0815\theta_{24}+0{\cdot}0031141=0.$$

One solution of this equation is $\theta_{24}=0{\cdot}14855$, which gives:

$$\theta_{12}=0{\cdot}050196,$$
$$\theta_{13}=0{\cdot}999.$$
$$\gamma=1{\cdot}2487\times10^{-3},$$
$$k_{33}=2{\cdot}45397\times10^{-4}.$$

The resulting circuit is shown in fig. 4.

Fig. 4



Multi-loop circuit realizing a second-order elliptic function. For all circuit realizations the element values are in mhos and farads.

4. Conclusion

It has been demonstrated how various numerator polynomials can be included in the synthesis of multi-loop feedback systems. This increases the range of functions which may be synthesized using these systems.

The method of synthesis for parallel systems may be extended to include circuits of order n and rank m (Holt and Sewell 1966). There is, of course, increased complexity associated with the realization of such networks.

Acknowledgments

The authors wish to thank the Science Research Council for financial support.

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PAPER 8

A Method of Power Measurement

Abstract—A method of measuring the power injected into a network is described. Either input current or voltage which are both complex waveforms, must be electrically integrable and phase-locked to the other. The method is particularly applicable to cases where one of the variables is sinusoidal.

Fig. 1(a) represents the general case of a one-port network with a current $i(t)$ injected by a voltage generator $v(t)$. The periodic voltage and current waveforms may be of any form with the stipulation that one must be electrically integrable and phase-locked to the other. Suppose $v(t)$ can be integrated to give $v_1(t)$. The closed curve of Fig. 1(b) may be assumed to represent the resulting plot of $i(t)$ against $v_1(t)$. The total area enclosed is given by the line integral of current around the curve. Thus.

$$A = \oint i dv_1 \tag{1}$$

but

$$v_1 = \int_0^t v dt. \tag{2}$$

Substituting (2) into (1) gives

$$A = \int_0^T iv dt \tag{3}$$

where T is the time taken for one excursion around the closed contour of Fig. 1(b).

The integral on the right-hand side of (3), and hence the area enclosed by the curve of Fig. 1(b), is directly proportional to the average power flowing into the circuit.

This method is particularly applicable to the case where one of the variables is sinusoidal. Integration can then be performed by imposing a 90° phase shift on the sinusoidal waveform.

The power flowing into a network N was measured using the experimental layout illustrated in Fig. 2. The input voltage was sinusoidal and of frequency $f_V = 50$ kHz. The input current waveform was periodic and it consisted of a number of sinusoidal frequency components which were all multiples of a fundamental frequency f_f. Frequency f_V was an integral multiple of f_f; otherwise, the power input would have been zero. Thus, in this case, T equaled $1/f_f$.

The resistance–capacitance network provided the necessary 90° phase shift. The integral of the driving voltage was displayed on the X plates of the oscilloscope and the input current on the Y plates. The resulting Lissajou figure then corresponded to the general plot of Fig. 1(b). The trace on the CRO was photographed and the negative was placed in an enlarger. The area enclosed by the magnified image was measured using a planimeter.

For the purpose of calibration, network N was replaced by a standard resistance and, for the same camera and enlarger setting as above, an area corresponding to a known power was found. The power flowing into network N was obtained by comparing the area enclosed by the unknown curve with that of the calibration curve. The inherent errors in measurement thus tended to cancel out, since they were characteristic of both curves.

A more direct approach of determining the power flowing into the network would be to multiply $i(t)$ and $v(t)$ and integrate the result. The product of $i(t)$ and $v(t)$ is generated in a multiplier which is a costly and complex piece of equipment with severe limitations on accuracy especially at high frequencies. To integrate the product of $i(t)$ and $v(t)$, which is a complex waveform, would require a much more sophisticated circuit than the phase shifter used to integrate the sinusoid in the method described here. An alternative method of measuring the input power would entail the measurement of the amplitudes of components of voltage and current waveforms and their relative phase displacement at the frequency of the sinusoidal waveform. This would involve filtering out the required frequency component of the complex waveform which, as a result, would preclude an exact determination of phase angle.

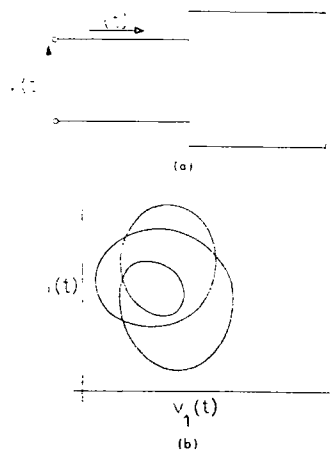

Fig. 1. (a) General one-port network. (b) Input current versus integral of input voltage for general one-port network.

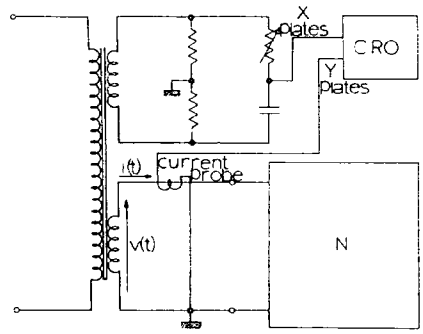

Fig. 2. Experimental circuit for measurement of input power.

The above method of power measurement lends itself particularly to cases where either the current or the voltage waveforms are easily integrable; for example, sinusoidal and exponential waveforms. It makes possible the accurate measurement of power in parametric amplifiers, harmonic and subharmonic oscillators, and other forms of frequency converters.

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A Simple Method for Producing Floating Inductors

Abstract—A simple method for producing ungrounded inductors using a gyrator is described. Floating inductors may be obtained from either grounded or ungrounded capacitors. The technique has an advantage in the low number of amplifiers required.

The problem of realizing floating inductors using gyrators and capacitors has led to some ingenious solutions [1]–[3] and has provoked interest in using other devices such as circulators [4] to overcome the difficulty. In a recent report [5], a technique for simply producing an ungrounded inductance was indicated and the general method can be established as follows. Consider a parallel connection of two 5-terminal

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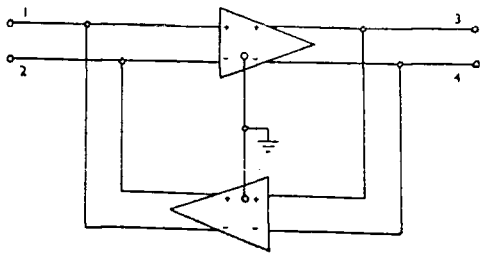

Fig. 1. Gyrator circuit using 5-terminal amplifiers.

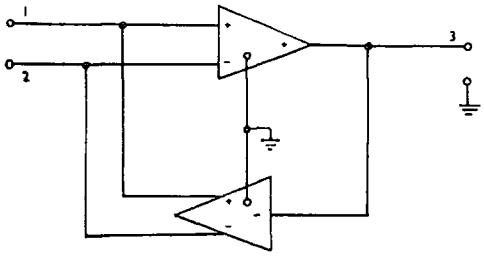

Fig. 2. Gyrator circuit producing a floating inductor from a grounded capacitor.

transadmittance amplifiers [6] (voltage-controlled current sources) as shown in Fig. 1. The amplifiers are ideal and have a transconductance g. The definite admittance matrix for such a circuit is

$$\begin{bmatrix} 0 & 0 & g & -g \\ 0 & 0 & -g & g \\ -g & g & 0 & 0 \\ g & -g & 0 & 0 \end{bmatrix}$$

which can be partitioned as

$$\left[\begin{array}{c|c} 0 & G \\ \hline -G & 0 \end{array}\right].$$

This matrix has precisely the same form as that of the common two-port gyrator.

If a capacitor is connected between nodes 3 and 4, it can be easily shown by pivotal condensation that the matrix describing the input port (nodes 1 and 2) represents an inductor of value C/g^2 connected between these nodes.

The negative sign of one of the G matrices can be obtained by appropriate connections of amplifier inputs or outputs.

It is possible, however, to progress further and produce an ungrounded inductor from a grounded capacitor using this type of circuit. The gyrator circuit shown in Fig. 2 has an admittance matrix

$$\left[\begin{array}{cc|c} 0 & 0 & g \\ 0 & 0 & -g \\ \hline -g & g & 0 \end{array}\right].$$

A capacitor connected between node 3 and ground will produce a floating inductor between nodes 1 and 2. There are two other methods of realizing gyrators which are inherently capable of producing floating inductors. The connection of two transimpedance amplifiers (current-controlled voltage sources) in series is one of these, but one which uses ungrounded amplifiers. This circuit will give a floating inductor from a floating capacitor, or with one amplifier grounded, the circuit will give a floating inductor from a grounded capacitor. The gyrator produced by a negative impedance convertor (NIC), negative impedance invertor (NII) cascade using an entirely active NII [8] will produce a floating inductor from a grounded capacitor. This circuit employs two grounded amplifiers.

The advantage of these methods is the low number of amplifiers required in any circuit realization. For a low-pass filter, the number of amplifiers required by the above techniques is $2n$ (n being the number of inductive elements normally required), whereas the "two-gyrator method" [1] needs $4n$ amplifiers and the Deboo technique [3] needs $3n$ amplifiers or $2n$ amplifiers and associated floatation circuits [2]. The alternative circulator technique [4] requires $3n$ amplifiers when using third-order circulators or $5[(n+1)/2]$ amplifiers with fourth-order circulators. The multiterminal gyrator method [7] would need $2[(2n+1)/3]$ unity-gain-current and voltage amplifiers.

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On the Reflection Pattern Made by a Laser Beam on the Etched Surface of Germanium

Abstract—A laser beam is shot on the surface of single-crystal germanium, after etching. From the reflection pattern, the characteristics of etched pits and hillocks are examined and it is found that etched pits not only are simple holes but also are convex.

In addition, a new reflection pattern in the orientation of [110] is reported. These new data will be applied to decide the orientation of single-crystal growth and the effect of dislocation in crystal.

A determination of the orientation of semiconductor single crystals is needed for many purposes such as the use of seed in the growth of single crystals and the study of dislocation and isotropy of the crystal. Until now, two methods of measuring this have been known. One is an X-ray technique, the other involves using the reflection pattern of visible light. The former has accuracy, the latter has ease of measurement and the benefit of inexpensive machinery. When a high degree of accuracy is not required, it is more convenient to use the latter system.

The method of the reflection pattern of visible light is used in the following manner. A single crystal is first cut at an appropriate orientation and the surface is polished with emery paper. After that, the crystal is etched with a substance such as superoxol ($HF:H_2O_2:H_2O$) (ratio 1:1:4).

In the configuration outlined in Fig. 1, visible light (our experiment used a laser beam) is shot through a pinhole onto the pits and hillocks that have been etched into the surface of the crystal. From the reflected light pattern, the orientation of the axis and the degree of incline of the surface from the axis can be determined.

In our experiment, we tried to control the width of the laser beam by using slit diameters from 0.5 mm to 1.0 mm. The photographs obtained under such conditions are shown in Fig. 2; etched pits appear in the orientation of [111] and [100] and hillocks appear in the orientation of [110].

We concluded that the reflective surface was convex because the reflected light pattern was enlarged more than the diameter of the laser beam. Besides this, the size of the reflection pattern changed when the distance between sample and screen was changed. We can observe the effects of a convex mirror in the large etched pits of orientation [100] and [110], and the effects of a concave mirror in [111]. However, we were interested in why there were such special pits and hillocks corresponding to each orien-

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PAPER 10

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Synthesis of active devices†

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The paper considers the synthesis of active network devices from a mathematical point of view. It is demonstrated how various devices can be realized without any detailed prior knowledge of the circuit form. Commencing with a matrix which characterizes the device performance, an appropriate admittance matrix is produced and then expanded by node induction until a network consisting of amplifiers and resistances only can be recognized. The validity of the method is demonstrated by synthesis of some accepted practical device realizations.

1. Introduction

In recent years there has been considerable interest shown in the design and use of active network devices fabricated from operational amplifiers and resistors. Devices such as gyrators (Morse and Huelsman 1964, Antoniou 1967) negative impedance converters (Morse 1964, Antoniou 1965), active transformers (Holt and Stewart 1968, Keen and Glover 1968 b), circulators (Keen *et al.* 1968, Rollett and Greenaway 1968), and various others have been realized in this form. These devices are finding extensive use in active network theory.

Certain mathematical techniques have been employed in the design of these elements, such as the technique using a basic active form of network (Keen and Glover 1968 a) and then utilizing a matrix factorizing method. This method appears to be the sole attempt at approaching the whole problem mathematically, although even here some basic active form is assumed *a priori*. In the references cited, no rigorous mathematical techniques are employed in the circuit realization.

The method to be outlined does not assume any detailed initial active topology or rely upon any particular design skill. From the initial device specifications, the final circuit is derived by basic matrix operations. The technique of node introduction is employed; this mathematical method has been rigorously defined (Piercey 1962) and successfully applied to the synthesis of certain active networks employing operational amplifiers (Holt and Sewell 1969).

2. Synthesis of 2-port devices

A typical active 2-port device in current usage is the negative impedance converter (NIC). The synthesis of a current inversion negative impedance converter (INIC) will demonstrate the principles involved.

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† Communicated by the Author.

2.1. *Admittance matrix of an INIC*

The transmission matrix of an ideal INIC with unity conversion ratio is (Mitra 1969):

$$A = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}.$$

A non-ideal one has $a_{12}, a_{21} \neq 0$, let $a_{ij} = \delta_i \to 0$, $(i \neq j)$. Hence

$$A = \begin{bmatrix} 1 & \delta_1 \\ \delta_2 & -1 \end{bmatrix}.$$

Transforming to a Y matrix

$$Y = \begin{bmatrix} -\dfrac{1}{\delta_1} & \dfrac{1+\delta_1\delta_2}{\delta_1} \\ -\dfrac{1}{\delta_1} & \dfrac{1}{\delta_1} \end{bmatrix},$$

since $\delta_i \to 0$ any higher power or multiple δ_i terms can be neglected and for convenience define

$$\lim_{\delta_1 \to 0} \frac{1}{\delta_1} \to Kg,$$

where K is a real constant tending to infinity, g is some finite real constant. Thus

$$Y = \begin{bmatrix} -Kg & Kg \\ -Kg & Kg \end{bmatrix}. \tag{1}$$

2.2. *Method of synthesis*

The general technique employed here is that of node introduction. The general theory and application of this have been discussed elsewhere, but the basic idea is to commence with a 2×2 admittance matrix, which may consist of complex entries, and expand the matrix one node at a time until an $n \times n$ matrix is obtained, the elements of which can be directly recognized as the elements of an n node network. Most of the introductions are already known, but the additional ones required in this work and the method of deriving them are given in the Appendix.

It is not possible to commence synthesis immediately with eqn. (1) if it is required to have a network consisting of a voltage difference amplifier and resistors only. The compactness of such a network prevents the introduction of sufficient terms in the expanded matrix.

However, this problem is overcome by splitting the matrix Y into two matrices; performing node introductions on these, the resultant matrices represent two networks in parallel which realize the required device:

$$Y = Y_A + Y_B, \tag{2}$$

$$Y_A = \begin{bmatrix} -Kg & 0 \\ -Kg & 0 \end{bmatrix}, \quad Y_B = \begin{bmatrix} 0 & Kg \\ 0 & Kg \end{bmatrix}.$$

Consider Y_B and use an Active III b introduction with $\lambda_{33}=\frac{1}{2}$, $\lambda_{12}=0$. $\lambda_{21}=0$, $0<\lambda_{23}\ll 1$, $\lambda_{32}=K$.

$$Y_{B(3\cdot3)}=\begin{array}{|c|c|c|}\hline 0 & -\theta_{12} & \dfrac{-\frac{1}{2}(\theta_{12}+Y_{12})}{K} \\ \hline -\theta_{12} & Kg-2K\theta_{23} & -\theta_{23} \\ \hline \dfrac{\frac{1}{2}(\theta_{12}+Y_{21})}{\lambda_{23}} & -\theta_{23}+K^2 & Y_{33}+\frac{1}{2}K \\ \hline \end{array}$$

With $\theta_{12}=0$, $\theta_{23}=\frac{1}{2}g$ and $Y_{33}=g$ this becomes :

$$Y_{B(3\cdot3)}=\begin{bmatrix} 0 & 0 & \dfrac{-g}{2} \\ 0 & 0 & \dfrac{-g}{2} \\ 0 & \dfrac{-g}{2}+K^2 & g+\dfrac{K}{2} \end{bmatrix}.$$

In order to ensure realizability of the final network, terms which constitute the passive elements, i.e. any terms other than K, will have to produce a symmetric sub-matrix when $Y_{A(n.n)}$, $Y_{B(n.n)}$ are ultimately added. It is therefore necessary to perform a transformation of the type $T_{1B}YT_{2B}$; the response of the system is invariant under such a transformation.

For the above matrix $Y_{B(3\cdot3)}$, T_{1B} and T_{2B} have the form

$$T_1=\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & \dfrac{g}{K^2} \\ 0 & 0 & 1 \end{bmatrix}, \quad T_2=\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & \dfrac{-g}{K} & 1 \end{bmatrix}.$$

The transformed matrix becomes :

$$Y_{B(3\cdot3)}=\begin{bmatrix} 0 & 0 & \dfrac{-g}{2} \\ 0 & g & \dfrac{-g}{2} \\ 0 & -g+K^2 & g+\dfrac{K}{2} \end{bmatrix}. \tag{3}$$

Now consider Y_A and use an Active III a introduction with $\lambda_{33}=\frac{1}{2}$, $\lambda_{12}=\lambda_{21}=0$, $\theta_{12}=0$, $0<\lambda_{13}\ll 1$, $\lambda_{31}=-K$, $\theta_{13}=(g/2)$, $Y_{33}=g$.

$$Y_{A(3\cdot3)}=\begin{bmatrix} 0 & 0 & \frac{-g}{2} \\ 0 & 0 & \frac{-g}{2} \\ \frac{-g}{2}-K^2 & 0 & g+\frac{K}{2} \end{bmatrix}.$$

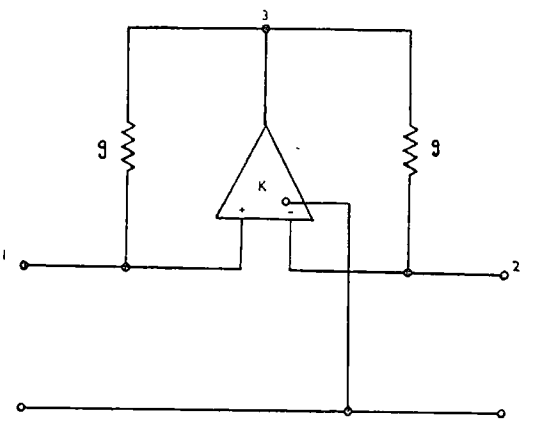
Again a transformation of the type $T_{1A}YT_{2A}$ is necessary to ensure ultimate realizability of the passive network. T_{1A}, T_{2A} have the form :

$$T_{1A}=\begin{bmatrix} 1 & 0 & \frac{-g}{K^2} \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}, \quad T_{2A}=\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ \frac{-g}{K} & 0 & 1 \end{bmatrix}.$$

Performing the transformation yields :

$$Y_{A(3\cdot3)}=\begin{bmatrix} g & 0 & \frac{-g}{2} \\ 0 & 0 & \frac{-g}{2} \\ -g-K^2 & 0 & g+\frac{K}{2} \end{bmatrix}. \tag{4}$$

Fig. 1



Current inverting negative impedance converter.

Because of the basic properties of node introduction, eqn. (2) will hold for these expanded matrices, hence the network matrix is obtained by adding eqns. (3), (4) :

$$Y=\begin{bmatrix} g & 0 & -g \\ 0 & g & -g \\ -g-K^2 & -g+K^2 & 2g \end{bmatrix},$$

which leads to a known INIC circuit shown in fig. 1 (Morse 1964).

2.3 *Synthesis of other 2-port devices*

It is possible to extend the method shown to include gyrators and other devices. But as a gyrator can be constructed from a cascade of circuits employing NIC's further elaboration is felt unnecessary.

3. Synthesis of multi-port devices

An interesting development arises in the synthesis of active circulators which belong to this class and have received some attention recently (Keen *et al.* 1968, Rollett and Greenaway 1968).

3.1. *N-port circulator transmission matrix*

The admittance matrix of an N-port circulator is skew symmetric and can be expressed as follows :

$$Y_{N,N}=KG_cK,$$

where G_c is the circulator matrix of the form :

$$G_c=g_c\begin{bmatrix} 0 & 1 & -1 & \dots & -1 \\ -1 & 0 & 1 & \dots & 1 \\ 1 & -1 & 0 & \dots & -1 \\ . & . & . & \dots & . \\ . & . & . & \dots & . \\ 1 & -1 & 1 & \dots & 0 \end{bmatrix},$$

the phase pattern of G_c is always that for N odd. The phase matrix K is used to produce the correct phase pattern, with particular reference to even order circulators where a phase reversal may be introduced between any two ports to ensure stability. K is a diagonal matrix containing elements ± 1, written as $\{1. -1 \dots 1\}$ and is of the same order as G_c.

Synthesis could commence by considering the matrix G_c and applying node introductions until a realizable network resulted. However, this would involve dealing with matrices of higher order and transformations of associated complexity. An alternative approach is suggested.

Most circulators consist of cascaded identical units enclosed within an overall feedback loop. If this loop is broken, it is then possible to derive a transmission matrix describing the path between the open ends of the feedback loop. The matrix for an Nth factor follows from easy factorization.

The overall transmission matrix has the form :

$$A_N = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}; \tag{5}$$

when N is even the matrix becomes :

$$A_N = \begin{bmatrix} -1 & 0 \\ 0 & 0 \end{bmatrix} \tag{6}$$

but the removal of a phase reversing stage will produce eqn. (5).

A_N can be split into N A matrices of the type

$$A_i = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}. \tag{7}$$

3.2. *Basic element admittance matrix*

For synthesis of an individual unit, by node introduction, it is necessary to commence with an admittance matrix. Immediate transformation of A_i would lead to a matrix with infinite entries, hence it is obligatory to consider the transmission matrix of a non-ideal unit :

$$A_i = \begin{bmatrix} a_{11} & \delta_1 \\ \delta_2 & \delta_2 \end{bmatrix}, \quad \text{where } \delta_i \to 0.$$

If $a_{11} = 1$ and δ_i is so small that only first-order terms are significant :

$$Y_i = \begin{bmatrix} \dfrac{\delta_3}{\delta_1} & \dfrac{-\delta_3}{\delta_1} \\ \dfrac{-1}{\delta_1} & \dfrac{1}{\delta_1} \end{bmatrix}.$$

Now investigate these terms in the limit

$$\lim_{\delta_i \to 0} \left(\frac{\delta_3}{\delta_1} \right) \to \frac{g}{\alpha}, \quad \text{where } g, \alpha \text{ are constants.}$$

$$\lim_{\delta_i \to 0} \left(\frac{1}{\delta_1} \right) \to \frac{K^2}{\alpha}, \quad \text{where } K \to \infty \text{ and is a real constant.}$$

Hence

$$Y_i = \frac{1}{\alpha} \begin{bmatrix} g & -g \\ -K^2 & K^2 \end{bmatrix}.$$

α is a constant introduced to aid synthesis, if $\alpha = 2$ synthesis proceeds in a convenient manner :

$$Y_i = \begin{bmatrix} \dfrac{g}{2} & \dfrac{-g}{2} \\ \dfrac{-K^2}{2} & \dfrac{K^2}{2} \end{bmatrix}. \tag{8}$$

This matrix is obviously not realizable by passive means.

3.3. *Method of synthesis*

The matrix of eqn. (8) is expanded by node introduction in the usual manner, commencing with an Active II b introduction with the following identities : $\lambda_{12}=0$, $\lambda_{21}=K/2$, $\lambda_{23}=-K$, $\theta_{23}=0$, $\lambda_{32}=-g_c/K^2$, $\theta_{12}=g/2$, $Y_{22}=g/2$:

$$Y_{i(3\cdot3)}=\begin{bmatrix} \frac{g}{2} & \frac{-g}{2} & 0 \\ \frac{-g}{2}+\frac{K^2}{2} & \frac{K^2}{2}+\frac{g}{2}+K & -K^2 \\ -g_c & 0 & g_c \end{bmatrix}.$$

The next step is to perform a passive II b introduction on the bottom right-hand 2×2 matrix with the conditions

$$(g_{21}-\theta_{12}-Y_{21})=(g_{22}+Y_{22})=(g_{23}-\theta_{23})\to0$$

and

$$\mathcal{L}\frac{(g_{21}-\theta_{12}-Y_{21})}{(g_{22}+Y_{22})}=-\tfrac{1}{2}. \quad \mathcal{L}\frac{(g_{23}-\theta_{23})}{(g_{22}+Y_{22})}=1,$$

$\theta_{12}=0$, $g_{21}=0$, $\theta_{23}=0$, $g_{12}=-g$.

$$Y_{i(4\cdot4)}=\begin{bmatrix} \frac{g}{2} & \frac{-g}{2} & 0 & 0 \\ \frac{-g}{2}+\frac{K^2}{2} & K+g & -g & -g+K^2 \\ -g_c & 0 & g_c & 0 \\ 0 & \frac{-g_{32}}{2} & g_{32} & g_{32} \end{bmatrix}.$$

Again it is necessary to perform an elementary transformation of the type $T_1 Y_i T_2$ with

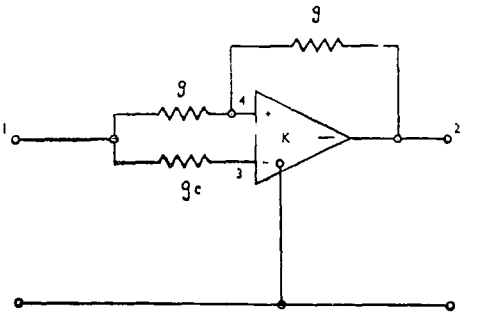
$$T_1=\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ -\frac{1}{2} & 0 & -1 & 1 \end{bmatrix}, \quad T_2=\begin{bmatrix} 1 & 0 & -1 & -\frac{1}{2} \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

and with $g_{32}=2g$ the following matrix results :

$$Y_{i(4\cdot4)}=\begin{bmatrix} g+g_c & 0 & -g_c & -g \\ 0 & K+g & -K^2 & -g+K^2 \\ -g_c & 0 & g_c & 0 \\ -g & -g & 0 & 2g \end{bmatrix}$$

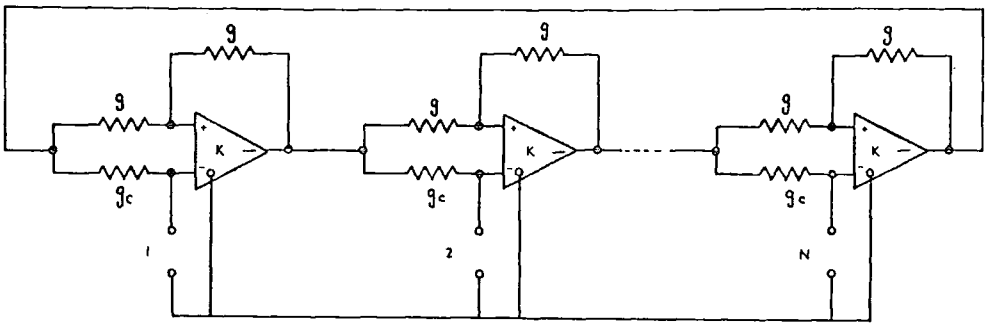
which can be recognized as the circuit shown in fig. 2. A cascade of these as shown in fig. 3 will realize an N-port circulator of the form reported by Rollett and Greenaway (1968).

Fig. 2



Circulator section.

Fig. 3



N-port circulator (N odd).

4. Transformation of amplifier type

If the amplifier used in a network has infinite gain, then it is immaterial which of the four types, voltage, current, transadmittance or transimpedance of the same configuration, are employed, as the system response is identical.

With finite gain devices it is possible to show a certain equivalence between amplifier types of different configurations. For instance, it has already been shown (Holt and Carey 1966) that a voltage amplifier can be transformed into a current one merely by taking the transpose of the amplifier matrix. Now for any matrix Y, $\det Y = \det Y^{T}$, and if the determinant is identical then the class of device remains unchanged, although there may be a change within the class, which is true in the case of negative impedance converters. The transpose transformation will convert a difference voltage amplifier into a current paraphase amplifier in a reverse direction. Similarly the transpose of a difference transimpedance amplifier is a paraphase transimpedance amplifier facing in the opposite direction. In the case of the NIC device both of these transformations have the effect of changing an INIC to a VNIC.

There is also an equivalence between a finite gain voltage difference amplifier and a finite gain transadmittance difference amplifier.

It is therefore possible to realize the devices synthesized earlier with different types of amplifier, provided that the forward gain is large compared to the other parameters of the amplifier admittance matrix. In the case of finite gain amplifiers some interchange of amplifiers is permitted by the transpose rule, although there may be some change within the class of device.

5. Conclusion

The mathematics of synthesizing active devices has been presented and demonstrated on two different types of devices. It is possible to realize all the devices in the 2-port group and the multi-port one using the techniques derived. The techniques could be modified to include amplifier non-idealities.

By employing the transformations indicated and others such as nullator-norator pairing (Antoniou 1968) a multitude of equivalent circuit realizations can be realized.

Appendix

Following Piercey (1962) and Holt and Sewell (1969) it is easy to derive the node introductions used in this work. For a matrix

$$Y_{2\cdot2}=\begin{bmatrix} Y_{011} & Y_{12} \\ Y_{21} & Y_{022} \end{bmatrix}$$

a 1-node introduction gives

$$Y_{3\cdot3}=\begin{bmatrix} Y_{011}+a_1A_1 & Y_{12}+a_2A_1 & a_3A_1 \\ Y_{21}+a_1A_2 & Y_{022}+a_2A_2 & a_3A_2 \\ a_1A_3 & a_2A_3 & a_3A_3 \end{bmatrix}.$$

For the Passive II b node introduction :

$$a_2A_2=g_{22}+Y_{22},$$
$$a_3A_2=g_{23}-\theta_{23},$$
$$a_2A_3=g_{32}-\theta_{23}.$$

On substitution the introduction becomes :

$Y_{011}+\dfrac{(g_{12}-\theta_{12}-Y_{12})(g_{21}-\theta_{12}-Y_{21})}{g_{22}+Y_{22}}$	$g_{12}-\theta_{12}$	$\dfrac{(g_{12}-\theta_{12}-Y_{12})(g_{23}-\theta_{23})}{g_{22}+Y_{22}}$
$g_{21}-\theta_{12}$	$Y_{022}+g_{22}+Y_{22}$	$g_{23}-\theta_{23}$
$\dfrac{(g_{21}-\theta_{12}-Y_{21})(g_{32}-\theta_{23})}{g_{22}+Y_{22}}$	$g_{32}-\theta_{23}$	$\dfrac{(g_{23}-\theta_{23})(g_{32}-\theta_{23})}{g_{22}+Y_{22}}$

The Active II b ($\lambda_{22}=1$) introduction has the following identities :

$$a_2 A_2 = K + Y_{22}.$$
$$a_2 A_3 = \lambda_{32} K - \theta_{23}. \quad K \to \infty.$$
$$a_3 A_2 = \lambda_{23} K - \theta_{23}.$$

Fig. 4

$Y_{011} - [(\theta_{12}+Y_{12})\lambda_{21} + (\theta_{12}+Y_{21})\lambda_{12}]$ $- Y_{22}\lambda_{21}\lambda_{12}$	$-\theta_{12}$	$-[(\theta_{12}+Y_{12})\lambda_{23} + \lambda_{12}\theta_{23}]$ $- Y_{22}\lambda_{12}\lambda_{23}$
$-\theta_{12}$	$Y_{022} + Y_{22}$	$-\theta_{23}$
$-[(\theta_{12}+Y_{21})\lambda_{32} + \lambda_{21}\theta_{23}] - Y_{22}\lambda_{21}\lambda_{32}$	$-\theta_{23}$	$-[\theta_{23}\lambda_{23} + \theta_{23}\lambda_{32}] - Y_{22}\lambda_{23}\lambda_{32}$

+

$K\,\lambda_{21}\lambda_{12}$	$K\,\lambda_{12}$	$K\,\lambda_{12}\lambda_{23}$
$K\,\lambda_{21}$	K	$K\,\lambda_{23}$
$K\,\lambda_{21}\lambda_{32}$	$K\,\lambda_{32}$	$K\,\lambda_{23}\lambda_{32}$

Active II b node introduction ($\lambda_{22}=1$).

Fig. 5

$Y_{011} - \frac{1}{\lambda_{33}}(\theta_{13}\lambda_{31} + \theta_{13}\lambda_{13}) - \frac{Y_{33}}{\lambda_{33}^2}\lambda_{31}\lambda_{13}$	$-\theta_{12}$	$-\theta_{13}$
$-\theta_{12}$	$Y_{022} + \frac{\lambda_{12}\lambda_{21}\lambda_{33}}{\lambda_{13}\lambda_{31}}\left(\frac{\theta_{13}}{\lambda_{31}} + \frac{\theta_{13}}{\lambda_{13}}\right)$ $+ \frac{\lambda_{33}}{\lambda_{13}\lambda_{31}}\left\{(\theta_{11}+Y_{11})\lambda_{21} + (\theta_{12}+Y_{21})\lambda_{12} - Y_{33}\lambda_{12}\lambda_{21}\right\}$	$\frac{\lambda_{21}Y_{33} - \lambda_{33}(\theta_{12}+Y_{21})}{\lambda_{31}}$ $+ \frac{\theta_{13}\lambda_{33}\lambda_{21}}{\lambda_{31}^2}$
$-\theta_{13}$	$\frac{\lambda_{12}Y_{33} - \lambda_{33}(\theta_{12}+Y_{12})}{\lambda_{13}} + \frac{\theta_{13}\lambda_{33}\lambda_{12}}{\lambda_{13}^2}$	Y_{33}

+

$K\,\frac{\lambda_{31}\lambda_{13}}{\lambda_{33}}$	$K\,\lambda_{12}$	$K\,\lambda_{13}$
$K\,\lambda_{21}$	$K\,\frac{\lambda_{12}\lambda_{21}\lambda_{33}}{\lambda_{13}\lambda_{31}}$	$\frac{K\,\lambda_{21}\lambda_{33}}{\lambda_{31}}$
$K\,\lambda_{31}$	$K\,\frac{\lambda_{12}\lambda_{33}}{\lambda_{13}}$	$K\,\lambda_{33}$

Active III a node introduction ($\lambda_{33}\neq 1$).

Fig. 6

$Y_{011} + \frac{Y_{33}\lambda_{12}\lambda_{21}}{\lambda_{23}\lambda_{32}} + \frac{\lambda_{12}\lambda_{21}\lambda_{33}}{\lambda_{23}\lambda_{32}}\left(\frac{\theta_{23}}{\lambda_{13}} + \frac{\theta_{23}}{\lambda_{32}}\right) - \frac{\lambda_{33}}{\lambda_{23}\lambda_{32}}\left(\lambda_{12}[\theta_{12}+Y_{21}] + \lambda_{21}[\theta_{12}+Y_{12}]\right)$	$-\theta_{12}$	$\frac{1}{\lambda_{32}}\left(\lambda_{12}Y_{33} - \lambda_{33}[\theta_{12}+Y_{12}]\right) + \frac{\theta_{23}\lambda_{12}\lambda_{33}}{\lambda_{32}^2}$
$-\theta_{12}$	$Y_{022} - \frac{1}{\lambda_{33}}\left(\lambda_{23}\theta_{23} + \lambda_{32}\theta_{23}\right) - \frac{Y_{33}\lambda_{32}\lambda_{23}}{\lambda_{33}^2}$	$-\theta_{23}$
$\frac{1}{\lambda_{23}}\left(\lambda_{21}Y_{33} - \lambda_{33}[\theta_{12}+Y_{21}]\right) + \frac{\theta_{23}\lambda_{21}\lambda_{33}}{\lambda_{23}^2}$	$-\theta_{23}$	Y_{33}

+

$K\frac{\lambda_{12}\lambda_{21}\lambda_{33}}{\lambda_{23}\lambda_{32}}$	$K\lambda_{12}$	$K\frac{\lambda_{12}\lambda_{33}}{\lambda_{32}}$
$K\lambda_{21}$	$K\frac{\lambda_{32}\lambda_{23}}{\lambda_{33}}$	$K\lambda_{23}$
$K\frac{\lambda_{21}\lambda_{33}}{\lambda_{23}}$	$K\lambda_{32}$	$K\lambda_{33}$

Active III b node introduction ($\lambda_{33} \neq 1$).

The Active III a ($\lambda_{33} \neq 1$) introduction has :

$$a_3 A_3 = \lambda_{33} K + Y_{33}.$$
$$a_1 A_3 = \lambda_{31} K - \theta_{13}.$$
$$a_3 A_1 = \lambda_{13} K - \theta_{13}.$$

and similarly for the Active III b ($\lambda_{33} \neq 1$) introduction :

$$a_3 A_3 = \lambda_{33} K + Y_{33}.$$
$$a_2 A_3 = \lambda_{32} K - \theta_{23}.$$
$$a_3 A_2 = \lambda_{23} K - \theta_{23}.$$

Substitution, expansion in a Taylor series, and neglecting any terms divided by K or higher powers of K will yield the introductions shown in figs. 4, 5, 6.

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PAPER 12

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The multiterminal active transformer†

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A method is presented for realizing an active multiterminal transformer which can then be used to produce a multiport transformer. This technique overcomes previously encountered restrictions and permits replacement of the floating transformer used in conventional network synthesis.

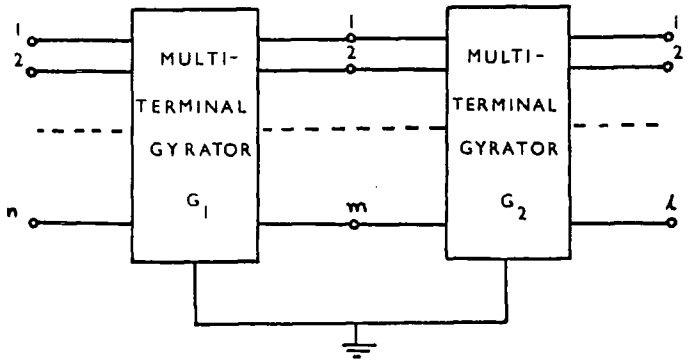
1. Introduction

Of the active realizations which have been produced for transformers (Weiss 1966, Su 1966, Brodie and Crocker 1966, Holt and Stewart 1968) only one does not have the restriction that one terminal on the input side and one on the output side form a common earth. This naturally prevents realizations of multiport transformers by these techniques. However the method developed by Weiss (1966) allows the realization of the multiport transformer, but unfortunately employs a considerable number of negative resistances and requires them to be floating. The method to be described overcomes the restrictions so far encountered.

2. Transformer realization

The basic procedure is to realize a multiterminal transformer, each terminal of which represents one end of a winding that has the other end grounded.

Fig. 1



Multiterminal active transformer.

† Communicated by the Author.

Suitable combinations of pairs of terminals will produce ports. The admittance matrix seen at the input of a multiterminal gyrator (Holt and Linggard 1968) is

$$Y = G Y_L^{-1} G^{\mathrm{T}},$$

where G is an $n \times m$ gyration matrix, and Y_L is an $m \times m$ load matrix. Consider two multiterminal gyrators in cascade as shown in fig. 1, the input matrix is then

$$Y = G_1(G_2 Y_L^{-1} G_2^{\mathrm{T}})^{-1} G_1^{\mathrm{T}}, \tag{1}$$

where G_1 is an $n \times m$ gyration matrix,
G_2 is an $m \times l$ gyration matrix,
and Y_L is an $l \times l$ load matrix.

2.1. *Realization with square G matrices*

In the case when the G matrices are square, straightforward manipulation of eqn. (1) yields :

$$Y = G_1(G_2^{\mathrm{T}})^{-1} Y_L G_2^{-1} G_1^{\mathrm{T}} \tag{2}$$

and a number of alternatives for the matrices G_1, G_2 are worthy of consideration.

2.1.1. *Unequal symmetric G matrices, G_2 non-singular*

This presents a valuable practical situation ; if $G_1 = g_1 A$ $G_2 = g_2 B$ where g_1, g_2 are constants and A, B are matrices, $A \neq B$, and $|B| \neq 0$ then eqn. (2) becomes

$$Y = \frac{g_1^2}{g_2^2} A B^{-1} Y_L B^{-1} A.$$

This equation represents transformer action on the load matrix, which may be readily observed by considering an example.

Let

$$Y_L = \begin{bmatrix} g_L & 0 \\ 0 & g_L \end{bmatrix}, \quad A = \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}, \quad B = \begin{bmatrix} b_1 & -b_2 \\ -b_2 & b_1 \end{bmatrix};$$

substitution gives

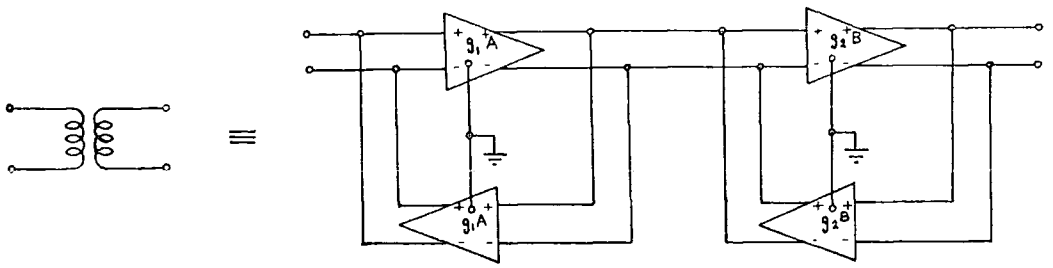
$$Y = 2c^2 \frac{g_1^2}{g_2^2} g_L \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix},$$

where

$$C = \frac{b_1 - b_2}{b_1^2 - b_2^2}.$$

In this case the constant $2c^2(g_1^2/g_2^2)$ can be considered to represent a turns ratio effect. The input matrix corresponds to the admittance matrix of a floating resistance and, as the load matrix describes two resistances which are grounded at one end, an isolation effect is apparent.

Fig. 2



Floating 2-port active transformer.

A simple realization of a two-port transformer as shown in fig. 2 follows, where the amplifiers are ideal transadmittance amplifiers (Sewell 1969) with appropriate transconductances. A unity turns ratio effect is available for $g_1 = g_2$ and $b_1 = 1 + \delta(\delta \ll 1)$, $b_2 = 1$.

2.1.2. *Unequal symmetric G matrices, both non-singular*

If $G_1 = g_1 B$, $G_2 = g_2 B$ and $|B| \neq 0$ then by eqn. (2)

$$Y = \frac{g_1^2}{g_2^2} BB^{-1} Y_L B^{-1} B = \frac{g_1^2}{g_2^2} Y_L.$$

The action of this circuit differs from the previous one in that although there is a turns ratio effect represented by $(g_1/g_2)^2$, the form of the input matrix is the same as the load one and hence does not reveal the same isolation effect.

2.1.3. *Unequal symmetric singular G matrices*

Let $G_1 = g_1 A$ and $G_2 = g_2 A$ where $|A| = 0$. Since this will give a singular matrix for G_2 the formulae derived cannot be applied and this situation does not represent a practical circuit. However, two comments are appropriate: first, in practice it would never be possible to ensure perfect equivalence between the two A matrices ; secondly, precise symmetry of A may be fairly difficult to ensure physically and thus there is a possibility of an inverse matrix existing. Hence a working circuit of this type is not too impractical, although the reasons for operation are more related to § 2.1.1 than to the properties of the matrices of this section.

2.1.4. *Unequal unsymmetric non-singular G matrices*

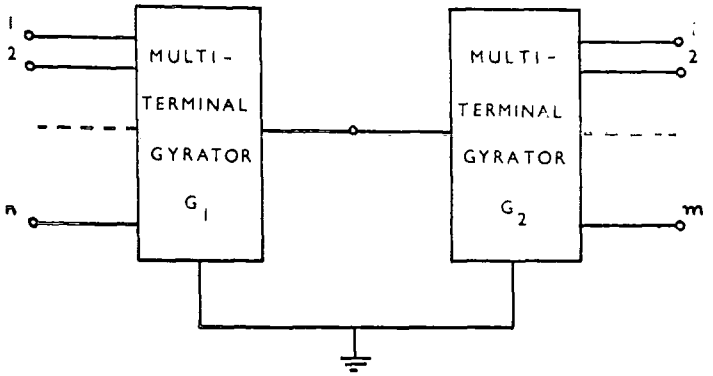
This choice of unsymmetric G matrices gives a type of transformer action, but the resultant input matrix demonstrates isolation properties which are a combination of those encountered in §§ 2.1.1 and 2.1.2.

2.2. *Realization with non-square G matrices*

A further significant step is obtained if fig. 3 is considered; the input matrix is again given by eqn. (1). As the G_2 matrix is not symmetrical it is not possible to utilize eqn. (2). However, it is obvious that $G_2 Y_L^{-1} G_2^{\mathrm{T}} = \text{constant}$ of the form $g_2^2 y_L$, where y_L is some complex admittance. Hence

$$Y = \frac{y_L}{g_2^2} G_1 G_1^{\mathrm{T}}$$

Fig. 3



Improved multiterminal transformer.

and if $G_1 = g_1 A$, where A is a connection matrix, then

$$Y = \frac{y_L}{g_2^2} g_1^2 A A^{\mathrm{T}}.$$

Again transformer action is recognizable, this can be illustrated by considering a simple example.

Let

$$G_2 = g_2[1 \quad -1] \quad \text{and} \quad G_1 = g_1 \begin{bmatrix} 1 \\ -1 \end{bmatrix},$$

i.e.

$$A = \begin{bmatrix} 1 \\ -1 \end{bmatrix}, \quad Y_L = \begin{bmatrix} g_L & 0 \\ 0 & g_L \end{bmatrix},$$

then

$$G_2 Y_L^{-1} G_2^{\mathrm{T}} = g_2^2 [1 \quad -1] \begin{bmatrix} \frac{1}{g_L} & 0 \\ 0 & \frac{1}{g_L} \end{bmatrix} \begin{bmatrix} 1 \\ -1 \end{bmatrix}$$

$$= \frac{2 g_2^2}{g_L}$$

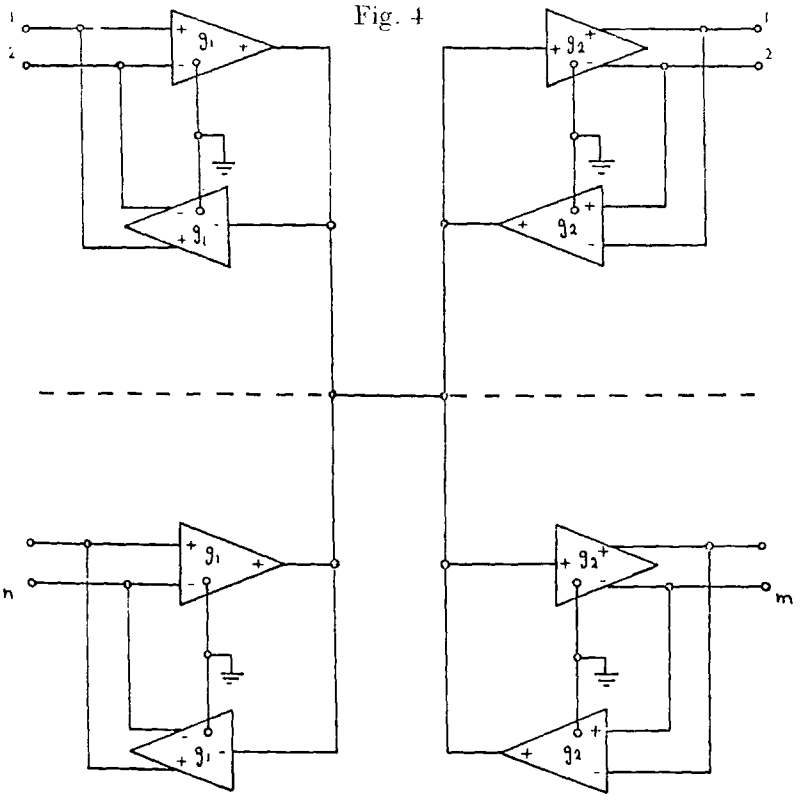
and hence

$$Y = \frac{g_L}{2 g_2^2} g_1^2 \begin{bmatrix} 1 \\ -1 \end{bmatrix} [1 \quad -1]$$

$$= g_L \frac{g_1^2}{2 g_2^2} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix},$$

which is a similar result to that of § 2.1.1.

Fig. 4



A realization of a multiterminal transformer.

A realization of such a transformer can be obtained directly by employing two multiterminal gyrators as shown, this would require $2(n+m+2)$ amplifiers of the unity gain current and voltage types. Another convenient realization is shown in fig. 4, this utilizes 4-terminal transadmittance amplifiers to produce the floating gyrators (Sewell 1969). The amplifier requirements are, for m, n both even, $m+n$; m or n odd, $m+n+1$; both m, n odd, $m+n+2$. An alternative circuit for a floating two-port transformer follows immediately.

3. Conclusions

The removal of the restriction of grounded terminals which the above technique has facilitated, means that active realizations of the ideal transformer can now be used to replace floating 2-port transformers in numerous synthesis techniques, although it may be necessary, for d.c. stability considerations, to ground one terminal of some of the structures presented. These techniques, together with inductor replacement by gyrators and capacitors will enable complete microminiaturization of the conventional circuits. It also provides a novel method for producing a multiport transformer by active means.

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PAPER 18

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A Theory of Equivalent Active Networks

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Abstract——**The effective application of equivalence transformations to active networks has been prevented by the difficulties produced by the nonsymmetric terms introduced by the active elements. These problems are overcome by constraint theory, and it is demonstrated how equivalent networks can be generated for active structures in which important parameters such as component spread and value, and sensitivity, can be optimized. Methods of controlling the number of elements in the equivalent networks are also given.**

I. Introduction

THE theory of equivalent networks as presented [1], [2], and with later elaborations [3], [5], has been effectively applied to passive networks. However the nonsymmetry of the nodal admittance matrix due to the presence of active devices renders the application of the theory to active networks difficult. On transformation, unsymmetric terms appear in the admittance matrix to such an extent that it is almost impossible to identify any conventional active devices. By constraining the nodal admittance matrix of the passive part of the circuit, it is shown that a general scaled Howitt transformation may be applied to circuits incorporating operational amplifiers. The optimization of network criteria may then be undertaken using a constrained nonlinear programming method. The type of active element remains unchanged and its position within the network is constant, but the passive elements may change in number, kind, and connection between the nodes of the initial structure.

II. Constraint Theory

The embedding of a differential input operational amplifier within a passive network may be considered as a constraint imposed upon the nodal admittance matrix of the passive part of the circuit [6], [7]. Consider a passive network $\mathfrak{N}$ with admittance matrix Y. Embed a differential amplifier gain A within $\mathfrak{N}$, positive input node i, negative input node j, and output node k. This introduces a constraint in the network forcing the potentials V_i, V_j, and V_k at node i, j, and k to obey the relation

$$A(V_i - V_j) = V_k. \tag{1}$$

As $A \to \infty$, (1) becomes

$$V_i - V_j = 0$$

so $V_i = V_j$; hence add column j to column i of Y and then delete column j. The current I_k at node k is arbitrary, being the output from a voltage source, so delete row k of Y, producing Y^r, the constrained admittance matrix of the active circuit. In the case of an embedded single input operational amplifier within $\mathfrak{N}$ between nodes i and k, the constraint imposed on Y consists of removing column i and row k. Also it is well known that in the limit of infinite gain the ideal current amplifier has exactly the same effect as the ideal voltage amplifier, hence the method may be generalized to include current amplifiers.

Keeping the numbering of the rows and columns of the constrained matrix Y^r unchanged, network functions may be calculated from Y^r in the usual manner. Y^r is a nonsymmetric matrix; however, due to the symmetry of Y certain pairs of elements are equal. It is postulated that matrix transformations can be applied to Y^r producing a scaled equivalent constrained matrix $Y^{r'}$, which has the necessary symmetry in the same places as Y^r. Then the matrix $Y^{r'}$ is rebuilt to produce a symmetric admittance matrix Y' of the passive part of a network $\mathfrak{N}'$ with voltage amplifiers embedded in the same positions as in the original passive network $\mathfrak{N}$. This rebuilt admittance matrix must obey the usual realizability constraints of a passive nodal admittance matrix

$$Y'_{ij} \leq 0 \quad \forall j \neq i \tag{2a}$$

$$Y'_{ii} - \sum_{j \neq i} Y'_{ij} \geq 0, \quad i = 1, \cdots, n. \tag{2b}$$

$$Y'_{ij} - Y'_{ji} = 0. \tag{2c}$$

III. Scaled Equivalence

Definition: Two networks $\mathfrak{N}, \mathfrak{N}'$ are scaled equivalent with respect to some voltage transfer function $T_v(s)$ if and only if $T'_v(s) = HT_v(s), H \in \boldsymbol{R}$. Note that $H = 1$ gives the usual definition of equivalence. Scaled equivalence will be considered with respect to the voltage transfer function

$$T_v(s) = \frac{\Delta_{ij}(s)}{\Delta_{ii}(s)}, \qquad \Delta_{ij}(s) = \det\left[Y(s)\right]_{ij}.$$

IV. Generalized Scaled Howitt Transformation

Consider two networks $\mathfrak{N}, \mathfrak{N}'$ with their admittance matrices Y, Y' (not necessarily symmetric) related by the

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equation

$$Y'(s)=\eta(s)Y(s)\xi(s) \tag{3}$$

where $\eta(s),\xi(s)$ are nonsingular.

Then for $\mathcal{N},\mathcal{N}'$ to be scaled equivalent networks with respect to the voltage transfer function $T_v(s)$,

$$\frac{\Delta'_{ij}(s)}{\Delta'_{ii}(s)}=H\frac{\Delta_{ij}(s)}{\Delta_{ii}(s)}. \tag{4}$$

It is required to determine the sufficient conditions on $\eta(s),\xi(s)$ for (4) to hoid. First we prove three lemmas.

Lemma 1:

$$\det[ABC\cdots Z]_{ij}=\sum_{abc}\sum\sum\cdots \sum_{z}(\det[A]_{ia}\det[B]_{ab}\det[C]_{bc}\cdots\det[Z]_{zj}).$$

Proof: We need only show

$$\det[AB]_{ij}=\sum_{s}\det[A]_{is}\det[B]_{sj}.$$

Let A',B' be the adjoint matrices of A,B, respectively. Then

$$A'_{pq}=\det[A]_{qp}\quad B'_{pq}=\det[B]_{qp}.$$

Now

$$B'A'_{ji}=\sum_{s}B'_{js}A'_{si}=\sum_{s}\det[B]_{sj}\det[A]_{is}. \tag{5}$$

Put

$$C=AB\Rightarrow C'=B'A'\Rightarrow B'A'_{ji}=\det[AB]_{ij}.$$

Hence from (5)

$$\det[AB]_{ij}=\sum_{s}\det[A]_{is}\det[B]_{sj}.$$

The lemma follows by obvious extension.

Lemma 2: If the ith row (column) of a matrix $A=m\boldsymbol{u}_i,\boldsymbol{u}_i$ the ith unit vector, then

$$\det[A]_{ii}=\frac{1}{m}\det[A].$$

Proof: The result is obtained by expanding $\det[A]$ along row (column) i.

Lemma 3: 1) If the ith column of a matrix $A=m\boldsymbol{u}_i,\boldsymbol{u}_i$ the ith unit vector, then

$$\det[A]_{ip}=0,\qquad \forall p\neq i.$$

2) If the jth row of a matrix $A=m\boldsymbol{u}_j^T,\boldsymbol{u}_j$ the jth unit vector, then

$$\det[A]_{pj}=0,\qquad \forall p\neq j.$$

Proof: For 1), removing any column $p\neq i$ from A makes column i of $[A]_{ip}$ all zeros. Hence $\det[A]_{ip}=0$ $\forall p\neq i$. The proof of 2) follows.

Theorem: Sufficient conditions on $\eta(s),\xi(s)$ to produce a scaled equivalent transformation are:

1) the ith column of $\eta(s)=m\boldsymbol{u}_i$;
2) the ith row of $\xi(s)=l\boldsymbol{u}_i^T$;
3) the jth row of $\xi(s)=k\boldsymbol{u}_j^T$; $\qquad m,l,k\in\boldsymbol{R}$

and the scaling factor $H=l/k$.

Proof:

$$\begin{aligned}\Delta'_{ij}(s)&=\det[Y'(s)]_{ij}\\&=\det[\eta(s)Y(s)\xi(s)]_{ij}\\&=\sum_{a}\sum_{b}\det[\eta(s)]_{ia}\det[Y(s)]_{ab}\det[\xi(s)]_{bj}\quad\text{(lemma 1)}\\&=\det[\eta(s)]_{ii}\det[Y(s)]_{ij}\det[\xi(s)]_{jj}\quad\text{(lemma 3)}\\&=\frac{1}{m}\det[\eta(s)]\det[Y(s)]_{ij}\frac{1}{k}\det[\xi(s)]\quad\text{(lemma 2).}\end{aligned}$$

Similarly,

$$\Delta'_{ii}(s)=\frac{1}{m}\det[\eta(s)]\det[Y(s)]_{ii}\frac{1}{l}\det[\xi(s)]$$

$$\Rightarrow\frac{\Delta'_{ij}(s)}{\Delta'_{ii}(s)}=\frac{l}{k}\frac{\det[Y(s)]_{ij}}{\det[Y(s)]_{ii}}=H\frac{\Delta_{ij}}{\Delta_{ii}}.$$

Thus the transformation $Y'(s)=\eta(s)Y(s)\xi(s)$ with the restrictions on $\eta(s),\xi(s)$ being $\det[\eta(s)]\neq 0$, $\det[\xi(s)]\neq 0$, and 1), 2), 3) of the theorem has been shown to be a scaled equivalent transformation. In the case $H=k=l=1$ the generalized Howitt transformation results.

No assumptions about the nature of $Y(s)$ were made in the proof of the theorem, hence this transformation may be applied to produce a scaled equivalent constrained matrix $Y'(s)$ from a constrained matrix $Y^r(s)$

$$Y'(s)=\eta(s)Y^r(s)\xi(s).$$

The elements of $Y'(s)$, and hence $Y'(s)$ are nonlinearly dependent on entries of $\eta(s)$ and $\xi(s)$

$$Y'_{ij}(s)=\sum_{p}\sum_{q}\eta_{ip}(s)Y^r_{pq}(s)\xi_{qj}(s).$$

Hence the elements of the passive part of the scaled equivalent network may be found after rebuilding $Y'(s)$ in symbolic form as quadratic equations in the entries of $\eta(s)$ and $\xi(s)$.

The scaling factor H will enable the generation of equivalent networks with different gain factors, which is of some significance in active RC network synthesis. Furthermore, the transformation matrices $\eta(s),\xi(s)$ can assume any type of entry, and hence it is easy to demonstrate the equivalence transformation of an RLC network into an active RC network containing $FDNR$ elements.

An important observation is that whereas in generation of passive equivalent networks the quadratic transformation is generally required to retain symmetry and hence realizability, no such limitations are imposed in the active

situation. As the constrained matrix is unsymmetric initially, a simple left-hand or right-hand transformation is usually quite sufficient. A sequence of these can, of course, be used.

V. Algorithm for Constraining and Rebuilding the Equivalent Admittance Matrices

Let N be the number of nodes in the network, 1 the input and 2 the output node, and $Y_{ij}(s)$ the value of admittance between nodes i and j of the passive part of the network.

If A is the number of single-input operational amplifiers embedded in the network, then let $I_1, I_2, \cdots, I_A$ = output nodes of single-input operational amplifiers $1 \cdots A$; $J_1, J_2, \cdots, J_A$ = input nodes of single-input operational amplifiers $1 \cdots A$.

If D is the number of differential-input operational amplifiers embedded in the network, then let $0_1, 0_2, \cdots, 0_D$ = output nodes of differential-input operational amplifiers $1 \cdots D$; $P_1, P_2, \cdots, P_D$ = positive input nodes of differential input operational amplifiers $1 \cdots D$; $M_1, M_2, \cdots, M_D$ = negative input nodes of differential input operational amplifiers $1 \cdots D$. k, m, l are scaling factors, $H = l/k$; δ_{ij} the Krönecker delta. The algorithm follows.

1) Construct component conductance and capacitance admittance matrices Y_G, Y_C from admittances $Y_{ij}(s)$.

2) Form the constrained component admittance matrices Y_G', Y_C' by the following operations on Y_G, Y_C:

a) remove rows $I_1, \cdots, I_A$;

b) remove columns $J_1, \cdots, J_A$;

c) remove rows $0_1, \cdots, 0_D$;

d) add columns P_1 and M_1, P_2 and $M_2, \cdots, P_D$ and M_D;

e) remove columns $M_1, \cdots, M_D$.

3) Form the symbolic transformation matrices η, ξ with dimensions $(N-A-D) \times (N-A-D)$ where

$$\eta_{ij} = \begin{cases} m\delta_{ij}, & j = 1 \\ X_t, & j > 1 \end{cases}$$

where X_t is a symbolic variable and $t = (N-A-D-1)(i-1)+j-1$ and

$$\xi_{ij} = \begin{cases} l\delta_{ij}, & i = 1 \\ k\delta_{ij}, & i = 2 \\ Y_t, & i > 2 \end{cases}$$

where Y_t is a symbolic variable and $t = (N-A-D-2)(j-1)+i-2$.

4) Transform the constrained component admittance matrices Y_G', Y_C' to the scaled equivalent constrained component admittance matrices Y_G'', Y_C''. Thus

$$Y_{G^{uv}}'' = \sum_p \sum_q \eta_{iu} Y_{G^{pq}}' \xi_{qj}$$

$$Y_{C^{uv}}'' = \sum_p \sum_q \eta_{iu} Y_{C^{pq}}' \xi_{qj}.$$

5) Form the scaled equivalent component admittance matrices of the passive part of the network, Y_G', Y_C' by the following operations on Y_G'', Y_C'':

a) Expand Y_G'', Y_C'' to dimension $N \times N$ by inserting rows of zeros in positions $I_1, \cdots, I_A, 0_1, \cdots, 0_D$, and columns of zeros in positions $J_1, \cdots, J_A, M_1, \cdots, M_D$.

b) Put

$$Y_{G^{ip}}' = Y_{G^{ip}}'' + Y_{G^{jp}}'', \quad \forall j \neq p \quad p = I_1, \cdots, I_A, 0_1, \cdots, 0_D$$

$$Y_{G^{ip}}' = \sum_{j \neq p} Y_{G^{jp}}'', \quad p = I_1, \cdots, I_A, 0_1, \cdots, 0_D.$$

c) Put

$$Y_{G^{pj}}' = Y_{G^{pj}}'' + Y_{G^{pi}}'', \quad \forall i \neq p \quad p = J_1, \cdots, J_A$$

$$Y_{G^{pi}}' = \sum_{i \neq p} Y_{G^{pi}}'', \quad p = J_1, \cdots, J_A.$$

d) Put

$$\left.\begin{aligned} Y_{G^{ip}}' &= Y_{G^{ip}}'' + Y_{G^{iM}}'' \\ Y_{G^{iM}}' &= 0 \end{aligned}\right\}, \quad \begin{aligned} &\text{for the pairs} \\ &p = M_1, q = P_1; \\ &p = M_2, q = P_2; \cdots \\ &p = M_D, q = D_D. \end{aligned}$$

e) Put

$$Y_{G^{pj}}' = Y_{G^{pj}}'' + Y_{G^{pM}}'', \quad \forall_i \neq p \quad p = M_1, \cdots, M_D.$$

f) Put

$$Y_{G^{ip}}' = Y_{G^{ip}}'' - Y_{G^{iq}}'', \quad \forall_i \neq I_1, \cdots, I_A; 0_1, \cdots, 0_D; M_1, \cdots, M_D; P_1, \cdots, P_D \text{ for the pairs } p = M_1, q = P_1; p = M_2, q = P_2; \cdots p = M_D, q = P_D.$$

g) Put the resulting matrices equal to Y_G', Y_C'.

6) We now have symbolic scaled equivalent passive part matrices Y_G', Y_C' which are symmetrical in all but

$$\frac{N^2 - (1+4(A+D))N}{2} + (A+D)(2+A+D)$$

pairs of entries.

VI. Optimization

In general, if a least squares error criterion is used to optimize some performance function of the scaled equivalent circuits, the resulting cost function is quartic in entries of $\eta(s)$ and $\xi(s)$, and the realizability constraints necessary to satisfy (2a)–(2c) are quadratic in the entries of $\eta(s)$ and $\xi(s)$.

The requirement that the equivalence transformations be executed in symbolic form so that the transformation algebra is needed only once introduces quite large storage requirements for the arrays involved. This is especially true with the quadratic transformation when quadratic terms of the transformation variables occur in the constraint arrays. With a one-sided transformation the con-

straint arrays contain linear combinations of the transformation variables, and hence storage requirements are less crucial. In consequence, the results obtained in the present implementation have been produced by application of a one-sided transformation with real entries.

The programming problem produced is

$$\min F(x), x=(x_1, x_2, \cdots, x_p)$$

$$\text{subject to } G_i(x) \geq 0, \quad i=1, \cdots, m$$

$$H_j(x)=0, \quad j=m+1, \cdots, m+q$$

where x is the vector of entries of $\eta(s)$ or $\xi(s)$ depending on whether a left- or right-hand transformation is used. F is the nonlinear cost function. The inequality constraints $G_i(x)$ derive from consideration of (2a) and (2b), and the equality constraints $H_j(x)$ follow from (2c).

The method used to solve this constrained nonlinear programming problem uses a modified SUMT [8], [9] program. The basis of the method is to determine a starting point x^0 such that $G_i(x^0)>0, i=1, \cdots, m$ and then solve a sequence of unconstrained minimizations of the sequence of functions

$$P(x, r_k) \equiv F(x) - r_k \sum_{i}^{m} {}_1 \log_e G_i(x) + \sum_{j}^{m+q} {}_{m+1} [H_j(x)]^2 / r_k + \lambda \sum_{l}^{p} {}_1 w_l x_l^n$$

where $\{r_k\}$ is a sequence that decreases strictly monotonically to zero, the conjecture being that the sequence of unconstrained minima $\{x(r_k)\}$ will approach the solution to the original programming problem as $r_k \to 0$.

In general, the inequality constraints $G_i(x)$ in this problem formulation will never be all satisfied strictly, and so a small boundary term $B_i \ll \min(G_i)$, where $G_i \neq 0$, was added to each inequality constraint, enabling an interior starting point x^0 to be found. B_i is somewhat dependent upon the computer word length, and the particular problem, for the examples included, $B_i = 10^{-8}$ proves satisfactory; if B_i is much larger, then an excessive number of nonzero elements is introduced in the solution. For a smaller value of B_i rounding errors prevent profitable solutions.

The method generally leads to solutions which have more elements than the original network; it is found useful to be able to control the number of new elements introduced using the final penalty term of the objective function $\lambda \sum_{l}^{p} {}_1 w_l x_l^n$. After an initial run with $\lambda = 0$ it is clear which x_l tend to zero in order to satisfy the constraints; grouping these x_l with the x_i which are zero in order to prevent elements being grown across certain branches forms the set $X = \{x_l : x_l \to 0\}$. Then by putting λ large and specifying nonzero values for the weights w_l corresponding to the $x_l \in X$, convergence to solutions yielding feasible networks with the desired restrictions upon topology is effected.

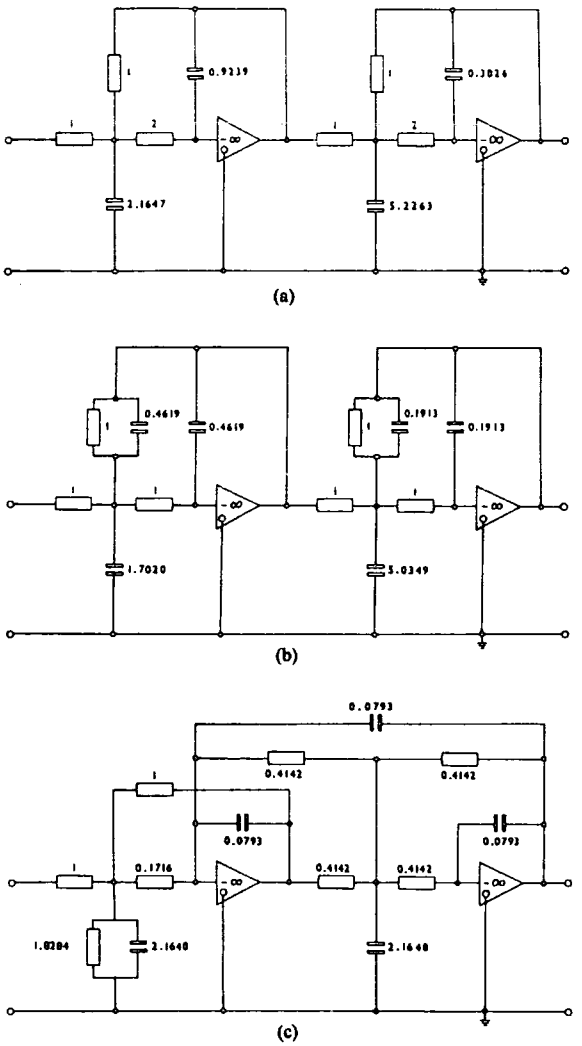

Fig. 1. (a)Original Rauch fourth order Butterworth realization. (Elements in siemens and farads). (b)Equal resistance realization. (c) Combined equal capacitance and resistance realization.

VII. Results and Conclusions

The computer implementation of the problem is in two parts. One program produces a symbolic transformation of the networks; this avoids the use of the optimizer and transformation simultaneously and the transformation is required only once. The two output files of the transformation program enable the information to be presented in a simple manner so that objective functions can be set up easily; at the same time the large arrays of constraints are available for input to the optimizer. The programs are run on an ICL 1906A, CDC 7600 computer configuration.

A typical objective function can be formulated from a least squares approach $\Sigma_i (G_i - G)^2$, which can be used to reduce resistance spread to center the values on some mean G. Similar objective functions are used for capaci-

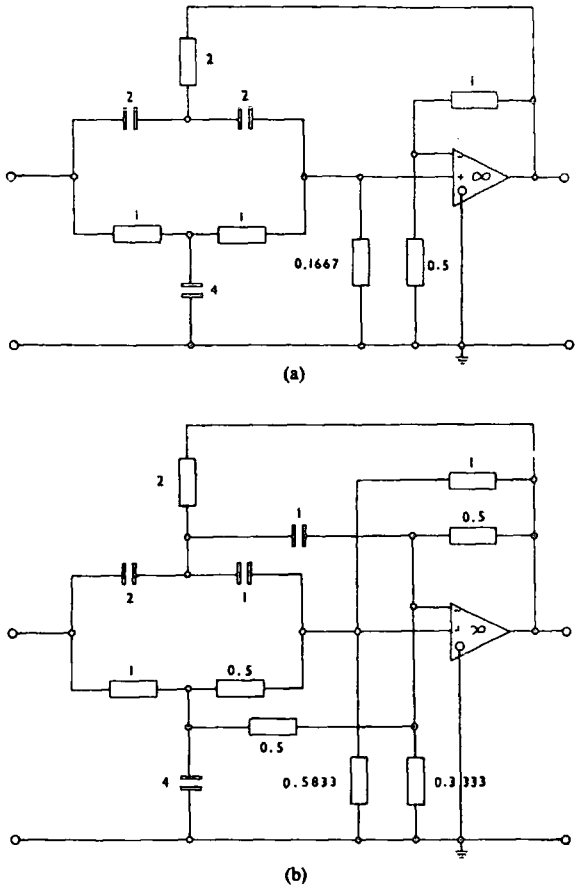

Fig. 2. (a)Original Sallen-Key elliptic realization. (b)Equivalent realization.

tance spread and size. At the present time the method using such objective functions has been applied successfully in circuits up to fourth order and containing a number of operational amplifiers. There is no limit to the number of amplifiers in a network; the main limit on the transformation program is dictated by the symbolic storage required. The optimizer, using the Newton-Raphson alternative in SUMT, has worked effectively on problems with 20 variables and 98 constraints.

The diagrams of Fig. 1 show alternative realizations for a fourth order Butterworth function, starting with the circuit of Fig. 1(a); an equal resistance solution with two pairs of equal capacitors was produced [Fig. 1(b)]. The circuit of Fig. 1(c) has a combination of as many equal capacitors as possible, together with numbers of equal resistances. The transformation program and file handling are executed by the ICL 1906A and only take a few seconds on all the problems tackled. The optimization step for these circuits required about 70 s on the CDC 7600. The circuits of Fig. 2 show similar results when a finite gain Sallen-Key circuit is transformed.

It has been demonstrated how equivalent active networks can be produced. Because active circuits have to satisfy more critical criteria than passive ones, more work is required in producing practical realizations. It is likely that parameters such as sensitivity, component spread, and size will produce conflicting demands under transformation, and further investigation is required in optimizing with compound objective functions.

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PAPER 21

Sensitivity minimisation and partitioned transformations in active equivalent networks

L.G. Grant and J.I. Sewell

Indexing terms: *Active networks, Minimisation, Sensitivity*

Abstract: Following the extension of equivalence transformations to a general class of electrical networks containing active devices such as operational amplifiers, the theory is developed to accommodate the minimisation of the sensitivity of the network response function to component variations. Theorems for passive-component sensitivity invariance and for updating routines applicable to the optimisation step are proved. Previous limitations imposed upon the optimisation routine by equality realisability constraints are completely eliminated by a partitioned approach. This leads to a new form of transformation. The partitioned transformation can be implemented in both discrete and continuous forms, and applied to the optimisation of component values and sensitivities in active networks.

1 Introduction

Equivalent-network theory is well established in the passive-filter field,[1,2] and the application to sensitivity studies and component value optimisation is well documented. For active networks it has been shown recently[3] that

$$Y_R' = \eta Y_R \xi \tag{1}$$

is a scaled equivalence transformation with respect to the voltage transfer function, where Y_R is the constrained admittance matrix of a passive network with embedded operational amplifiers and η, ξ are suitably constrained generalised Howitt transformation matrices. The solution of problems involving the minimisation of component spread and size has been successfully attempted using this transformation. The implications of this theory upon sensitivity minimisation of active *RC* networks obviously require investigation. The initial implementation of the transformation[3] resulted in large arrays of equality and inequality constraints that must be satisfied to maintain realisability. In particular, the equality constraints can prove to be quite a nuisance in the constrained optimisation routine. A new transformation is developed from a partitioned approach, and this completely eliminates all equality conditions.

2 Active-network sensitivities

Assuming that the active elements are ideal operational amplifiers, whose effects upon the network can be represented as ideal constraints, then only the sensitivities of the passive components need be considered.

The relative sensitivity $S_{pq}^{T_v}$ of the voltage transfer function T_v to some passive element e_{pq} between the nodes p and q is defined as

$$S_{pq}^{T_v} = \frac{e_{pq}}{T_v}\frac{\partial T_v}{\partial e_{pq}} = e_{pq} Q_{pq}^{T_v} \tag{2}$$

where

$$Q_{pq}^{T_v} = \frac{1}{T_v}\frac{\partial T_v}{\partial e_{pq}} \tag{3}$$

is termed the semi-relative sensitivity. Noting that

$$T_v = \frac{\det [Y_R]_{ij}}{\det [Y_R]_{ii}} = \frac{N(s)}{D(s)} \tag{4}$$

we define as follows the entry sensitivities E_{kl}^N, E_{kl}^D of the numerator and the denominator to the entry y_{kl} of Y_R:

$$E_{kl}^N = \frac{\partial N}{\partial y_{kl}} = \frac{\partial(\det [Y_R]_{ij})}{\partial y_{kl}} = \det [Y_R]_{ij,\ kl} \tag{5}$$

$$E_{kl}^D = \frac{\partial D}{\partial y_{kl}} = \frac{\partial(\det [Y_R]_{ii})}{\partial y_{kl}} = \det [Y_R]_{ii,\ kl} \tag{6}$$

Hence

$$Q_{pq}^{T_v} = \frac{1}{T_v}\sum_k\sum_l \frac{\partial T_v}{\partial y_{kl}}\frac{\partial y_{kl}}{\partial e_{pq}}$$

$$= \sum_k\sum_l \left\{\frac{E_{kl}^N}{N} - \frac{E_{kl}^D}{D}\right\}\frac{\partial y_{kl}}{\partial e_{pq}} \tag{7}$$

Sensitivity polynomials are considered, since this enables sensitivity optimisation over a range of frequencies to be undertaken without further development.

We define the variable

$$A_{pq}^{kl} = \delta_{kl}(\delta_{kp} + \delta_{kq} + \delta_{kp}\delta_{kq}) - (\delta_{kp}\delta_{lq} + \delta_{kq}\delta_{lp}) \tag{8}$$

$$\frac{\partial y_{kl}}{\partial e_{pq}} = \begin{cases} A_{pq}^{kl} \text{ if } e_{pq} \text{ is a conductance} \\ sA_{pq}^{kl} \text{ if } e_{pq} \text{ is a capacitor} \end{cases} \tag{9}$$

Therefore, once the matrix of entry sensitivities is obtained, the relative sensitivity of any element may be found using eqns. 9, 7 and 2.

During the generation of equivalent active networks, it is advantageous to be able to calculate the current-sensitivity values (in terms of the current transformation matrices) and the entry-sensitivity values of the original network without further sensitivity analyses. The following theorem demonstrates how the current entry sensitivity matrix may be evaluated at any point of the transformation:

Theorem 1

$$\left[\frac{E^{N'}}{N'}\right] = \left[\eta^T\right]^{-1}\left[\frac{E^N}{N}\right]\left[\xi^T\right]^{-1}$$

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where $E^{N'}$ is the current entry numerator sensitivity matrix, E^N the original entry numerator sensitivity matrix, and η, ξ the current transformation matrices.

Proof

$$\left[\frac{E^{N'}}{N'}\right]_{pq} = \frac{1}{N'}\frac{\partial N'}{\partial y'_{pq}} = \frac{1}{\det [Y'_R]_{ij}}\frac{\partial(\det [Y'_R]_{ij})}{\partial y'_{pq}}$$

$$= \frac{\det [Y'_R]_{ij,\,pq}}{\det [Y'_R]_{ij}}$$

Now

$$\det [Y'_R]_{ij} = \det [\eta Y_R \xi]_{ij}$$

$$= \det \eta \det [Y_R]_{ij} \det \xi$$

for a scaled equivalence transformation.[3] Form y such that

$$\det y = \det [Y_R]_{ij}$$

$$\Rightarrow \det [Y'_R]_{ij} = \det \eta \det y \det \xi$$

$$= \det [\eta y \xi]$$

$$\Rightarrow \det [Y'_R]_{ij,pq} = \det [\eta y \xi]_{pq}$$

$$= \sum_a \sum_b \det [\eta]_{pa} \det [y]_{ab} \det [\xi]_{bq}$$

therefore

$$\frac{1}{N'}\frac{\partial N'}{\partial y'_{pq}}$$

$$= \frac{1}{\det \eta \det [Y_R]_{ij} \det \xi}$$

$$\times \sum_a \sum_b \det [\eta]_{pa} \det [Y_R]_{ij,\,ab} \det [\xi]_{bq}$$

$$= \sum_a \sum_b \frac{1}{\det \eta}\frac{\partial(\det \eta)}{\partial \eta_{pa}}$$

$$\times \frac{1}{\det [Y_R]_{ij}}\frac{\partial(\det [Y_R]_{ij})}{\partial y_{ab}}\frac{1}{\det \xi}\frac{\partial(\det \xi)}{\partial \xi_{bq}}$$

$$= \sum_a \sum_b \left[\eta^T\right]^{-1}_{pa}\left[\frac{1}{N}\frac{\partial N}{\partial y_{ab}}\right]\left[\xi^T\right]^{-1}_{bq}$$

Hence the theorem is proved.

Using theorem 1 and its equivalent for the entry denominator sensitivity matrix, the current relative sensitivity of some element e'_{pq} during a generalised scaled equivalence transformation may be found in terms of the original entry sensitivities using the relation

$$S^{T'v}_{pq} =$$

$$\sum_k \sum_l \sum_a \sum_b \left\{\left[\left[\eta^T\right]^{-1}_{ka}\left[E^{ND}\right]_{ab}\left[\xi^T\right]^{-1}_{bl}\right\}\frac{\partial y'_{kl}}{\partial e'_{pq}} e'_{pq} \quad (10)$$

where

$$E^{ND} = \left[\frac{E^N}{N} - \frac{E^D}{D}\right] \quad (11)$$

Theorem 2

The sum of the relative sensitivities of all passive components of one type in an RC network with embedded operational amplifiers is invariant under a generalised scaled Howitt transformation.

Proof

Let Y_G be the conductance component of Y_R. Then, where 'sum of diagonal entries' is represented by s.d.e.,

$$\sum_{\substack{\text{all}\\ \text{conductances}}} S^{T_v} = \text{s.d.e. of } Y_G^T E^{ND}$$

Putting

$$S = Y_G^T E^{ND}, \quad \sum S^{T_v} = \sum_p [S]_{pp} \quad (12)$$

$$\Rightarrow \sum_{\substack{\text{all}\\ \text{conductances}}} S^{T'v} = \text{s.d.e. of } [Y'_G]^T E^{ND}$$

$$= \text{s.d.e. of } [\eta Y_G \xi]^T [(\eta^T)^{-1} E^{ND} (\xi^T)^{-1}]$$

$$= \text{s.d.e. of } \xi^T Y_G^T \eta^T (\eta^T)^{-1} E^{ND} (\xi^T)^{-1}$$

$$= \text{s.d.e. of } \xi^T Y_G^T E^{ND} (\xi^T)^{-1}$$

$$= \sum_p \sum_a \sum_b [\xi^T]_{pa} [S]_{ab} [\xi^T]^{-1}_{bp}$$

$$= \sum_a \sum_b \sum_p [S]_{ab} [\xi]_{ap} [\xi]^{-1}_{pb}$$

Now

$$\sum_p [\xi]_{ap} [\xi]^{-1}_{pb} = \delta_{ab}$$

$$\Rightarrow \sum_{\substack{\text{all}\\ \text{conductances}}} S^{T'v} = \sum_a \sum_b [S]_{ab} \delta_{ab}$$

$$= \sum_a [S]_{aa}$$

$$= \sum_{\substack{\text{all}\\ \text{conductances}}} S^{T_v} \qquad \text{from eqn. 12.}$$

Hence the theorem is proved, and an alternative proof is given of sensitivity invariance of active networks generated by the scaled equivalence transformation (eqn. 1).

The theory presented here has been used to formulate objective functions designed to minimise sum squared sensitivity, using the computer program described in Reference 3 and utilising a s.u.m.t. optimisation technique.[4]

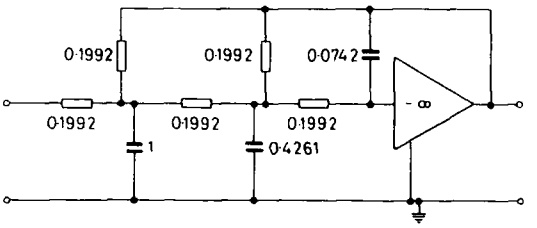

Fig. 1 *Initial realisation of a 3rd-order Butterworth function*
Conductances in siemens (S): capacitances in farads (F)

Fig. 1 shows an initial circuit for a 3rd-order Butterworth function; the value of sum squared sensitivity function at $s = j1$ is 7·7016. The circuit of Fig. 2 results from sensitivity minimisation and has a comparative sensitivity value of 6·8393. This solution is a local as opposed to a global minimum. The increase in number of elements is apparent, but this is not unexpected as the limiting solution to these problems is a fully connected network with equal element sensitivity values.

The results shown here were obtained using one-sided transformations only, because of the problems reported in Reference 3 and the difficulties arising from the nonlinear form of the equality constraints generated by the quadratic transform.

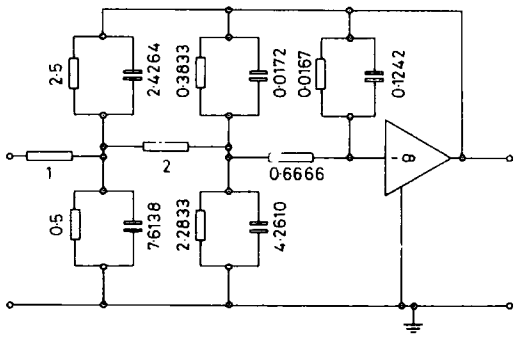

Fig. 2 *Reduced sensitivity realisation of a 3rd-order Butterworth function*

Conductances in siemens (S): capacitances in farads (F)

3 Partitioned transformation

The equality constraints, which are necessary to keep symmetric the passive part of the admittance matrix during optimisation, have prevented, up to now, the formulation of a continuous quadratic transformation for active *RC* networks like that proposed for passive networks.[5] Essentially, continuous techniques depend on the transformation being small and the ability to make linear approximations to quadratic constraints. If the constraints are inequalities, good linear approximations may be made; however, it is almost impossible to make efficient linear approximations to quadratic equality constraints. The elimination of equality constraints in the discrete transformation will reduce the complexity of the optimisation problem.

Here, a transformation is constructed which eliminates the equality constraints by means of topological transformations of the constrained nodal admittance matrix, and which utilises the redundancy of the row of the constrained nodal admittance matrix corresponding to the input node to simplify the application of the transformation.

Consider an n-node *RC* network N with m embedded operational amplifiers. The constrained admittance matrix Y_R, formed by deleting rows corresponding to amplifier output nodes and columns corresponding to amplifier input nodes, has dimensions $(n-m) \times (n-m)$ and is symmetrical in $(n-2m-1)(n-2m)/2$ pairs of entries. From eqn. 4,

$$T_v = \frac{\det [Y_R]_{ij}}{\det [Y_R]_{ii}} = \frac{\det [Y_r]_{.j}}{\det [Y_r]_{.i}} = \frac{N(s)}{D(s)} \tag{13}$$

where Y_r is formed by removing the ith row of Y_R. Inspection reveals that Y_r is symmetrical in $(n-2m-2)(n-2m-1)/2$ pairs of entries. Now consider Y_r re-ordered so as to place these symmetrical entries in an $(n-2m-1) \times (n-2m-1)$ symmetrical submatrix in the top right hand corner. That is, form

$$Y^* = \begin{bmatrix} Y_1 & \overbrace{\vdots}^{f} & Y_s \\ \cdots & & \cdots \\ Y_0 & \vdots & Y_2 \end{bmatrix} \Big\} f \tag{14}$$

$$f = n - 2m - 1$$

where Y_s is an $f \times f$ symmetric matrix.

The following well-known matrix properties are used:

(i) the interchange of columns i and j of a matrix A is obtained by forming the product $AT_{i \to j}$, and

(ii) the interchange of rows i and j of a matrix A is obtained by forming the product $T_{i \to j}A$

where the topological transformation matrix $T_{i \to j}$ is the unit matrix with its ith and jth rows interchanged.

Let the unloaded nodes (those not connected to an amplifier, and not the input node i) be $p_1, p_2, \ldots, p_f$; let the corresponding rows and columns be $r_1, r_2, \ldots, r_f$; $c_1, c_2, \ldots, c_f$. Then the topological transformations from $Y_r \to Y^*$ take the form

$$Y^* = T_{r_f \to f} \ldots T_{r_2 \to 2} T_{r_1 \to 1} Y_r T_{c_f \to n-m} T_{c_{f-1} \to n-m-1} \cdots \cdots T_{c_1 \to m+2} \tag{15}$$

where the $T_{r_i \to i}$ are $(n-m-1) \times (n-m-1)$ and the $T_{c_j \to k}$ are $(n-m) \times (n-m)$. Hence, taking inverse transformations, and noting $T_{i \to j}$ is self inverse,

$$Y_r = T_{r_1 \to 1} T_{r_2 \to 2} \ldots T_{r_f \to f} Y^* T_{c_1 \to m+2} \ldots T_{c_f \to n-m} \tag{16}$$

In practical terms, this amounts to simply re-ordering the nodes.

The following results emerge and are proved where necessary.

Theorem 3

$$\begin{aligned} \det [T_{p \to q}]_{ij} &= (-1)^{|p-q|-1}(1-\delta_{pq})(\delta_{iq}\delta_{jp} + \delta_{ip}\delta_{jq}) \\ &\quad - \delta_{ij}(1-\delta_{pq})(1-\delta_{ip})(1-\delta_{iq}) + \delta_{pq}\delta_{ij} \\ &= 0, \text{ or } -1, \text{ or } 1 \end{aligned}$$

Theorem 4

For fixed p, q, i there exists only one j such that $\det [T_{p \to q}]_{ij} \neq 0$

For fixed p, q, j there exists only one i such that $\det [T_{p \to q}]_{ij} \neq 0$

Theorem 5

$$\det [AB \ldots Z]_{ij} = \sum_a \sum_b \ldots \sum_z \det [A]_{ia} \det [B]_{ab} \ldots \det [Z]_{zj}$$

Proof

See Reference 3.

Theorem 6

If A is $(l-1)\times(l-1)$, Y is $(l-1)\times l$, B is $l\times l$, then

$$\det [AYB]_{.j} = \sum_{b=1}^{l} \det A \det [Y]_{.b} \det [B]_{bj}$$

Proof

Construct

$$A' = \begin{bmatrix} 1 & \vdots & a_1 \\ \cdots & \vdots & \cdots \\ 0 & \vdots & \\ 0 & \vdots & \\ 0 & \vdots & A \\ 0 & \vdots & \end{bmatrix} \Bigg\} l \qquad Y' = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots \\ & & & \\ & & Y & \\ & & & \end{bmatrix} \Bigg\} l$$

(the l columns of A' and the l columns of Y' are indicated)

then

$$A'Y'B = \begin{bmatrix} a_1 & Y & B \\ \cdots & \cdots & \cdots \\ & & \\ A & Y & B \end{bmatrix} \Bigg\} l-1$$

Hence, from theorem 5,

$$\det [A'Y'B]_{1j} = \sum \sum \det [A']_{1a} \det [Y']_{ab} \det [B]_{bj}$$

Now

$$\det [A']_{1a} = 0 \text{ for all } a \neq 1$$

$$\Rightarrow \det [A'Y'B]_{1j} = \sum_{b} \det [A']_{11} \det [Y']_{1b} \det [B]_{bj}$$

$$\Rightarrow \det [AYB]_{.j} = \sum_{b} \det A \det [Y]_{.b} \det [B]_{bj}$$

Theorem 7

If A is $(l-1)\times(l-1)$, Y is $(l-1)\times l$ and $B, C \ldots Z$ are $l\times l$, then

$$\det [AYBC \ldots Z]_{.j} = \sum_{b} \sum_{c} \cdots \sum_{z} \det A \det [Y]_{.b} \times \det [B]_{bc} \ldots \det [Z]_{zj}$$

Proof

By extension of theorems 5 and 6, writing

$$A = T_{r_1 \to 1} T_{r_2 \to 2} \cdots T_{r_f \to f}$$

using eqn. 16 and theorem 6, we get

$$\det [Y_r]_{.j} = \sum_{a} \sum_{b} \cdots \sum_{z} \det A \det [Y^*]_{.a} \det [T_{c_1 \to m+2}]_{ab} \cdots \ldots \det [T_{c_f \to n-m}]_{zj} \quad (17)$$

and

$$\det [Y_r]_{.i} = \sum_{\alpha} \sum_{b} \cdots \sum_{\omega} \det A \det [Y^*]_{.\alpha} \det [T_{c_1 \to m+2}]_{\alpha\beta} \cdots \ldots \det [T_{c_f \to n-m}]_{\omega i} \quad (18)$$

Hence, from theorems 3 and 4,

$$\det [Y_r]_{.j} = \pm \det [Y^*]_{.l} \quad (19)$$

$$\det [Y_r]_{.i} = \pm \det [Y^*]_{.t} \quad (20)$$

where l, t are the unique solutions of the equations. The signs are ignored, as inverse transforms are taken later. Then

$$\det [T_{c_1 \to m+2}]_{lb} \det [T_{c_2 \to m+3}]_{bc} \cdots \ldots \det [T_{c_f \to n-m}]_{zj} \neq 0 \quad (21)$$

$$\det [T_{c_1 \to m+2}]_{t\beta} \det [T_{c_2 \to m+3}]_{\beta\gamma} \cdots \ldots \det [T_{c_f \to n-m}]_{\omega i} \neq 0 \quad (22)$$

Eqns. 21 and 22 are solved easily by a computer algorithm using the result of theorem 3.

We observe from eqns. 19 and 20 that the problem of applying transformations to Y_r to retain invariant $[\det Y_r]_{.j}/\det [Y_r]_{.i}$ is equivalent to that of applying transformations to Y^* to retain invariant $\det [Y^*]_{.l}/\det [Y^*]_{.t}$.

We now wish to form $Y^{*\prime}$ by transformations upon Y^*, such that

$$\frac{\det [Y^{*\prime}]_{.l}}{\det [Y^{*\prime}]_{.t}} = \frac{H \det [Y^*]_{.l}}{\det [Y^*]_{.t}} \quad (23)$$

where $H \in \mathscr{R}$ ($\mathscr{R}$ denotes real space).

Put

$$Y^{*\prime} = \eta Y^* \xi \quad (24)$$

where η is $(n-m-1)\times(n-m-1)$ and ξ is $(n-m)\times(n-m)$, and where

$$\eta = \begin{matrix} \\ f \\ m \end{matrix} \begin{matrix} \overset{f}{\overset{\downarrow}{}} \quad \overset{m}{\overset{\downarrow}{}} \\ \begin{bmatrix} \eta' & \vdots & 0 \\ \cdots & \vdots & \cdots \\ \eta_1 & \vdots & \eta_0 \end{bmatrix} \end{matrix} \qquad \xi = \begin{matrix} \overset{m+1}{\overset{\downarrow}{}} \quad \overset{f}{\overset{\downarrow}{}} \\ \begin{bmatrix} \xi_0 & \vdots & 0 \\ \cdots & \vdots & \cdots \\ \xi_1 & \vdots & \xi' \end{bmatrix} \end{matrix} \quad (25)$$

Considering eqn. 14, eqn. 24 becomes

$$Y^{*\prime} = \overbrace{\begin{bmatrix} \eta' Y_1 \xi_0 + \eta' Y_s \xi_1 & \vdots & \eta' Y_s \xi' \\ \cdots & \vdots & \cdots \\ \eta_1 Y_1 \xi_0 + \eta_1 Y_s \xi_1 + & \vdots & \eta_1 Y_s \xi' + \\ + \eta_0 Y_0 \xi_0 + \eta_0 Y_2 \xi_1 & \vdots & \eta_0 Y_2 \xi' \end{bmatrix}}^{n-m} \Bigg\} \begin{matrix} f \\ n-m-1 \end{matrix} \quad (26)$$

$$= \begin{bmatrix} Y_1' & \vdots & Y_s' \\ \cdots & \vdots & \cdots \\ & \vdots & \\ Y_0' & \vdots & Y_2' \end{bmatrix} \quad (27)$$

where $Y_s' = \eta' Y_s \xi'$. Putting $\eta'^T = \xi'$ gives

$$Y_s' = \eta' Y_s \eta'^T, \quad (28)$$

a transformation which retains the symmetry of the $f\times f$ top-right-hand submatrix. Now

$$\det [Y^{*\prime}]_{.l} = \det [\eta Y^* \xi]_{.l} = \sum_{b} \det \eta \det [Y^*]_{.b} \det [\xi]_{bl} \quad (29)$$

from Theorem 6, and

$$\det [Y^{*\prime}]_{.t} = \sum_a \det \eta \det [Y^*]_{.a} \det [\xi]_{at} \quad (30)$$

Putting the lth row of $\xi = \phi\delta_{ij}$ and the tth row of $\xi = \omega\delta_{ij}$ ($\phi, \omega \in \mathscr{R}$), then from eqns. 29 and 30 we have

$$\frac{\det [Y^{*\prime}]_{.l}}{\det [Y^{*\prime}]_{.t}} = \frac{\det \eta \det [Y^*]_{.l}\, \phi^{-1} \det \xi}{\det \eta \det [Y^*]_{.t}\, \omega^{-1} \det \xi}$$

$$= H \frac{\det [Y^*]_{.l}}{\det [Y^*]_{.t}} \quad (32)$$

where $H = \omega/\phi$.
Hence we have the following theorem:

Theorem 8

Constraining η, ξ such that

(i) $\xi' = \eta'^T$ and ξ, η have the partitioned form of eqn. 25
(ii) ξ, η are nonsingular
(iii) the lth row of $\xi = \phi\delta_{ij}$
(iv) the tth row of $\xi = \omega\delta_{ij}$

then the transformation $Y^{*\prime} = \eta Y^* \xi$ is a scaled equivalence transformation with scaling factor ω/ϕ, and the necessary symmetry properties of Y^* are conserved under the transformation.

Once we have $Y^{*\prime}$ in symbolic form, inverse transformations are applied to produce Y'_r; thus

$$Y'_r = T_{r_1 \to 1} \ldots T_{r_f \to f} Y^{*\prime} T_{c_1 \to m+2} \ldots T_{c_f \to n-m} \quad (33)$$

The matrix Y' is then rebuilt from Y'_R by inserting suitable symbolic rows and columns corresponding to the constrained nodes, to form the symmetric nodal admittance matrix of the passive part of an equivalent active network. The symmetry of this matrix has been ensured entirely by the form of the transformation and not by equality constraints imposed on the optimiser in a previous implementation.[3]

4 The continuous partitioned transformation

The partitioned transformation may be implemented in a continuous form. Let

$$\hat{\eta} = I_{f+m} + \eta x \quad \hat{\xi} = I_{f+m+1} + \xi x \quad (34)$$

where I_{f+m}, I_{f+m+1} are identity matrices, η, ξ are of the form described in theorem 8 and x is a small real scalar. Then $\hat{\eta}$, $\hat{\xi}$ clearly obey the conditions of theorem 8 and

$$Y^{*\prime} = \hat{\eta} Y^* \hat{\xi} \quad (35)$$

is a generalised scaled equivalence transformation. Substituting eqn. 34 into eqn. 35 gives

$$Y^{*\prime}(x) = (I_{f+m} + \eta x) Y^* (I_{f+m+1} + \xi x)$$

$$= Y^* + (\eta Y^* + Y^* \xi)x + (\eta Y^* \xi)x^2 \quad (36)$$

If the transformation parameter x is small, a linear approximation can be made to eqn. 36:

$$Y^{*\prime} = Y^* + (\eta Y^* + Y^* \xi)x \quad (37)$$

The consequence of eqn. 37 is that, for a small x, a transformation may be applied producing an equivalent network which is close in some metric sense to the original. The realisability constraints obtained from eqn. 37 are linear, and if a linear approximation to the objective function is made then a linear programming problem may be solved for a sequence of step sizes. Using eqn. 36 as a check of realisability, and cutting the step size x if realisability is contravened, a series of networks which tend towards some optimum may be obtained.

From eqn. 10 it can be seen that the matrices of entry semirelative sensitivities for an active network under equivalence transformation are related as follows:

$$E^{ND\prime} = [\hat{\eta}^T]^{-1} E^{ND} [\hat{\xi}^T]^{-1} \quad (38)$$

but

$$\hat{\eta} = I_{f+m} + \eta x \Rightarrow \hat{\eta}^T = I_{f+m} + \eta^T x$$

$$\Rightarrow (\hat{\eta}^T)^{-1} = I_{f+m} - \eta^T x + \eta^T \eta^T x^2 + \ldots \quad (39)$$

and

$$(\hat{\xi}^T)^{-1} = I_{f+m+1} - \xi^T x + \xi^T \xi^T x^2 + \ldots \quad (40)$$

therefore

$$E^{ND\prime} = (I_{f+m} + \eta^T x)^{-1} E^{ND} (I_{f+m+1} + \xi^T x)^{-1}$$

$$= (I_{f+m} - \eta^T x + \eta^T \eta^T x^2 \ldots)$$

$$\times E^{ND} (I_{f+m+1} - \xi^T x + \xi^T \xi^T x^2 + \ldots)$$

$$= E^{ND} - (\eta^T E^{ND} + E^{ND} \xi^T) x + 0(x^2) \quad (41)$$

The sensitivity minimisation techniques of Section 1 can now be implemented using linear programming methods; this avoids matrix inversion each time the semirelative sensitivities are updated.

5 Conclusion

A method for the minimisation of the sensitivity of active networks using equivalent-network transformations has been produced, and appropriate sensitivity updating routines derived. A new transformation is given which eliminates equality constraints and enhances the application of the quadratic transformation, both in the minimisation of element spread and in the sensitivity of active networks. It also enables a continuous form of the transformation to be used. The choice between discrete and continuous forms is somewhat subjective, as some assessment of the effect of the truncation steps in the continuous form must be weighed against the avoidance of matrix inversion present in the discrete implementation. The equivalent networks produced by the two forms can differ quite considerably. Both methods will produce new networks containing more elements than the original, an effect observed particularly when the optimisation of total sum squared sensitivity is attempted.

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PAPER 22

Some further sensitivity theorems in active equivalent-network theory

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Indexing terms: Active networks, Sensitivity analysis

Abstract: The relevance of various sensitivity measures in the study of active equivalent networks is investigated. It is known that the summed differential sensitivity of the passive components in an active *RC* network is invariant under the transformation; it is now shown that the similar sums of large-change sensitivities and the large-change multiparameter sensitivity are both invariant for component changes within specified bounds. Even more practical sensitivity measures derive from integral definitions over a specified frequency interval. It is demonstrated that the sums of integral sensitivities are noninvariant under transformation but the integral of the multiparameter sensitivity function again remains invariant. These results are of significance in any attempted optimisation of the sensitivities of active-filter structures.

1 Introduction

The theory of equivalent networks[1,2] has been extended to the case of networks containing active devices such as operational amplifiers together with passive elements,[3] and some interesting results have followed. The active devices are regarded as constraints on the passive network N with a nodal admittance matrix Y from which a constrained matrix Y_R is obtained by deleting appropriate rows and columns. The characteristic network functions are available from Y_R by the usual ratio of cofactors and determinants. In particular, the voltage transfer function T_v, which is a function of the complex frequency s and the passive elements, is

$$\frac{\det [Y_R]_{ij}}{\det [Y_R]_{ii}} = \frac{N}{D} \tag{1}$$

Whole series of equivalent networks, maintaining this function constant, but which are optimised with respect to component size and spread,[3] and component differential sensitivity[4] have been generated. Some basic theorems on differential sensitivity have been noted.[4]

In this paper expressions are obtained for both the large-change and multiparameter large-change sensitivities, which obviously have considerable practical significance.[5] In each case it is shown that the summed sensitivity for component changes within certain practical bounds is invariant under a generalised scaled Howitt transformation. The next Section investigates the question of invariance of the integral definition of the differential, large-change, and multiparameter large-change sensitivities.

2 Large-change sensitivity

Two networks N, N', consisting of active devices (in the same positions in both networks) together with passive elements, are scaled equivalent[3] with respect to some voltage transfer function T_v iff, $T_v' = HT_v$; $H \in \mathscr{R}$. Defining the entry sensitivities E_{kl}^N and E_{kl}^D of the numerator and denominator of T_v (eqn. 1) with respect to the entry y_{kl} of Y_R as

$$E_{kl}^N = \frac{\partial N}{\partial y_{kl}}$$

$$E_{kl}^D = \frac{\partial D}{\partial y_{kl}}$$

the complete relationships between entry and element sensitivities are outlined elsewhere.[4]

Now $T_v = T_v(s, e)$ where e is the passive element of interest between nodes p, q and sensitivity calculations assume the bilinear properties of network functions.[5] Hence

$$\begin{aligned}\Delta T_v &= T_v(e + \Delta e) - T_v(e) \\ &= \frac{N(e + \Delta e)}{D(e + \Delta e)} - \frac{N(e)}{D(e)} \\ &= \frac{D(e)\left[N(e) + \Delta e \dfrac{\partial N(e)}{\partial e}\right] - N(e)\left[D(e) + \Delta e \dfrac{\partial D(e)}{\partial e}\right]}{D(e)\left[D(e) + \Delta e \dfrac{\partial D(e)}{\partial e}\right]}\end{aligned}$$

$$\Delta T_v = \frac{T_v(e)\,\Delta e \sum_k \sum_l E_{kl}^{ND} \dfrac{\partial y_{kl}}{\partial e}}{1 + \Delta e \sum_k \sum_l \dfrac{E_{kl}^D}{D} \dfrac{\partial y_{kl}}{\partial e}} \tag{2}$$

where

$$E_{kl}^{ND} = \frac{1}{N} \frac{\partial N(e)}{\partial y_{kl}} - \frac{1}{D} \frac{\partial D(e)}{\partial y_{kl}}$$

Now large-change sensitivity $S_{\Delta e}^{T_v}$ is defined to be

$$S_{\Delta e}^{T_v} = \frac{e}{T} \frac{\Delta T_v}{\Delta e}$$

From eqn. 2

$$S_{\Delta e}^{T_v} = \frac{e \sum_k \sum_l E_{kl}^{ND} \dfrac{\partial y_{kl}}{\partial e}}{1 + \Delta e \sum_k \sum_l \dfrac{E_{kl}^D}{D} \dfrac{\partial y_{kl}}{\partial e}} \tag{3}$$

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$$= \frac{e\left(\frac{\partial N/\partial e}{N} - \frac{\partial D/\partial e}{D}\right)}{1 + \Delta e \frac{\partial D/\partial e}{D}} \quad (4)$$

as $\Delta e \to 0, S^{T_v}_{\Delta e} \to S^{T_v}_{e}$ (differential sensitivity). Now

$$\left| \Delta e \sum_k \sum_l \frac{E^D_{kl}}{D} \frac{\partial y_{kl}}{\partial e} \right| < 1$$

and for changes in e of up to 10%, eqn. 3 can be expanded to give a bounded large-change sensitivity function

$$S^{T_v}_{\Delta e} = e \sum_k \sum_l E^{ND}_{kl} \frac{\partial y_{kl}}{\partial e} \left[1 - \Delta e \sum_k \sum_l \frac{E^D_{kl}}{D} \frac{\partial y_{kl}}{\partial e} + \left(\Delta e \sum_k \sum_l \frac{E^D_{kl}}{D} \frac{\partial y_{kl}}{\partial e} \right)^2 \right] \quad (5)$$

The computation of such a sensitivity measure during each cycle of optimisation would obviously be expensive. However it is possible to update eqn. 5 without further evaluation of the complete function. Direct application of the updating theorem[4] to eqn. 5 gives the current sensitivity function of some element e', during a generalised scaled equivalence transformation, in terms of the original entry sensitivities as

$$S^{T_v}_{\Delta e'} = e' \sum_k \sum_l \sum_a \sum_b \left([\eta^T]^{-1}_{ka} [E^{ND}]_{ab} [\xi^T]^{-1}_{bl} \right) \frac{\partial y'_{kl}}{\partial e'} \left[1 - \Delta e' \sum_k \sum_l \sum_a \sum_b \left([\eta^T]^{-1}_{ka} \frac{1}{D} [E^D]_{ab} [\xi^T]^{-1}_{bl} \frac{\partial y'_{kl}}{\partial e'} \right) + \{ \Delta e' \sum_k \sum_l \sum_a \sum_b \left([\eta^T]^{-1}_{ka} \frac{1}{D} [E^D]_{ab} [\xi^T]^{-1}_{bl} \frac{\partial y'_{kl}}{\partial e'} \right) \}^2 \right] \quad (6)$$

Theorem 1: The sum of the bounded large-change sensitivities of all passive components of one type in an *RC* network with embedded operational amplifiers is invariant under a generalised scaled Howitt transformation.

Proof: Consider all the conductances in the network. By induction (see Appendix 7) it may be shown that

$$\sum_{\substack{\text{all} \\ \text{conductances}}} S^{T_v}_{\Delta e} = \sum_{\text{diagonal}} Y^T_G E^{ND} - \frac{1}{D} \sum_{\text{diagonal}} Y^T_G E^{ND} (\Delta Y_G)^T E^D + \frac{1}{D^2} \sum_{\text{diagonal}} Y^T_G E^{ND} (\Delta Y_G)^T E^D (\Delta Y_G)^T E^D \quad (7)$$

where Y_G is the conductance component of Y_R the constrained admittance matrix.
Let $S = Y^T_G E^{ND}$ then

$$\sum_{\text{diagonal}} Y^T_G E^{ND} = \sum_p [S]_{pp}$$

and for a scaled equivalent network

$$\sum_{\text{diagonal}} Y^{T'}_G E^{ND'} = \sum_{\text{diagonal}} [\eta Y_G \xi]^T [(\eta^T)^{-1} E^{ND} (\xi^T)^{-1}]$$

$$= \sum_{\text{diagonal}} \xi^T Y^T_G \eta^T (\eta^T)^{-1} E^{ND} (\xi^T)^{-1}$$

$$= \sum_p \sum_a \sum_b [\xi^T]_{pa} [S]_{ab} [\xi^T]^{-1}_{bp}$$

$$= \sum_a \sum_b \sum_p [S]_{ab} [\xi]_{ap} [\xi]^{-1}_{pb}$$

$$= \sum_a \sum_b [S]_{ab} \delta_{ab} \quad (\delta = \text{the Kronecker delta})$$

$$= \sum_a [S]_{aa} = \sum_{\text{diagonal}} Y^T_G E^{ND} \quad (8)$$

Let $\mathscr{S} = Y^T_G E^{ND} (\Delta Y_G)^T \frac{E^D}{D}$ then

$$\sum_{\text{diagonal}} Y^T_G E^{ND} (\Delta Y_G)^T \frac{E^D}{D} = \sum_q [\mathscr{S}]_{qq}$$

Now

$$\sum_{\text{diagonal}} Y^{T'}_G E^{ND'} (\Delta Y_G)^{T'} \left(\frac{E^D}{D} \right)' = \sum_{\text{diagonal}} [\eta Y_G \xi]^T [(\eta^T)^{-1} E^{ND} (\xi^T)^{-1}] [\eta (\Delta Y_G) \xi]^T [(\eta^T)^{-1} \frac{E^D}{D} (\xi^T)^{-1}]$$

$$= \sum_{\text{diagonal}} \xi^T Y^T_G E^{ND} (\Delta Y_G)^T \frac{E^D}{D} (\xi^T)^{-1}$$

$$= \sum_q \sum_a \sum_b [\xi^T]_{qa} [\mathscr{S}]_{ab} [\xi^T]^{-1}_{bq}$$

$$= \sum_a [\mathscr{S}]_{aa} = \sum_{\text{diagonal}} Y^T_G E^{ND} (\Delta Y_G)^T \frac{E^D}{D} \quad (9)$$

Similarly, the third term gives

$$\sum_{\text{diagonal}} Y^{T'}_G E^{ND'} (\Delta Y_G)^{T'} \left(\frac{E^D}{D} \right)' (\Delta Y_G)^{T'} \left(\frac{E^D}{D} \right)' = \sum_{\text{diagonal}} Y^T_G E^{ND} (\Delta Y_G)^T \frac{E^D}{D} (\Delta Y_G)^T \frac{E^D}{D} \quad (10)$$

Hence

$$\sum_{\substack{\text{all} \\ \text{conductances}}} S^{T_v}_{\Delta e} = \sum_{\substack{\text{all} \\ \text{conductances}}} S^{T_v}_{\Delta e'} \quad (11)$$

The same proof will hold when considering capacitances.

Theorem 2: The bounded large-change multiparameter sensitivity of all the passive components of one type in an *RC* network with embedded operational amplifiers is invariant under a generalised scaled Howitt transformation.

Proof: In reality $T_v = T_v(s, e_1, \ldots, e_n)$ hence

$$\Delta T_v = \frac{N(e_1 + \Delta e_1, \ldots e_n + \Delta e_n)}{D(e_1 + \Delta e_1, \ldots e_n + \Delta e_n)} - \frac{N(e_1, \ldots e_n)}{D(e_1, \ldots e_n)}$$

$$= \frac{\left\{ D(e_1, \ldots e_n)[N(e_1, \ldots e_n) + \Delta e_1 \frac{\partial N}{\partial e_1}(e_1, \ldots e_n) + \ldots + \Delta e_n \frac{\partial N}{\partial e_n}(e_1, \ldots e_n)] - N(e_1, \ldots e_n)[D(e_1, \ldots e_n) + \Delta e_1 \frac{\partial D}{\partial e_1}(e_1, \ldots e_n) + \ldots + \Delta e_n \frac{\partial D}{\partial e_n}(e_1, \ldots e_n)] \right\}}{D(e_1, \ldots e_n)[D(e_1, \ldots e_n) + \Delta e_1 \frac{\partial D}{\partial e_1}(e_1, \ldots e_n) + \ldots + \Delta e_n \frac{\partial D}{\partial e_n}(e_1, \ldots e_n)]}$$

$$= \frac{T_v(e_1, \ldots e_n) \sum_i \Delta e_i \sum_k \sum_l E_{kl}^{ND} \frac{\partial y_{kl}}{\partial e_i}}{1 + \sum_i \Delta e_i \sum_k \sum_l \frac{E_{kl}^D}{D} \frac{\partial y_{kl}}{\partial e_i}} \qquad (12)$$

For convenience define the large-change multiparameter sensitivity as:

$$S_{\Delta e_i}^{T_v} = \frac{\Delta T_v}{T_v} \qquad (13)$$

$$= \left[\sum_i \Delta e_i \sum_k \sum_l E_{kl}^{ND} \frac{\partial y_{kl}}{\partial e_i} \right] \left[1 + \sum_i \Delta e_i \sum_k \sum_l \frac{E_{kl}^D}{D} \frac{\partial y_{kl}}{\partial e_i} \right]^{-1} \qquad (14)$$

For

$$\left| \sum_i \Delta e_i \sum_k \sum_l \frac{E_{kl}^D}{D} \frac{\partial y_{kl}}{\partial e_i} \right| < 1$$

$$S_{\Delta e_i}^{T_v} = \left[\sum_i \Delta e_i \sum_k \sum_l E_{kl}^{ND} \frac{\partial y_{kl}}{\partial e_i} \right] \left[1 - \sum_i \Delta e_i \sum_k \sum_l \frac{E_{kl}^D}{D} \frac{\partial y_{kl}}{\partial e_i} + \left(\sum_i \Delta e_i \sum_k \sum_l \frac{E_{kl}^D}{D} \frac{\partial y_{kl}}{\partial e_i} \right)^2 \right] \qquad (15)$$

which is a definition for bounded large-change multiparameter sensitivity.

Using an induction proof similar to that given in Appendix 7, it may be shown that

$$S_{\Delta e_i}^{T_v} = \sum_{\text{diagonal}} (\Delta Y_G)^T E^{ND} - \left(\sum_{\text{diagonal}} (\Delta Y_G)^T E^{ND} \right) \left(\sum_{\text{diagonal}} (\Delta Y_G)^T \frac{E^D}{D} \right) + \left(\sum_{\text{diagonal}} (\Delta Y_G)^T E^{ND} \right) \left(\sum_{\text{diagonal}} (\Delta Y_G)^T \frac{E^D}{D} \right) \left(\sum_{\text{diagonal}} (\Delta Y_G)^T \frac{E^D}{D} \right) \qquad (16)$$

Using the same methods of proof as for eqns. 8–10, it follows that

$$S_{\Delta e_i'}^{T_v'} = S_{\Delta e_i}^{T_v} \qquad (17)$$

Hence theorem 2, and of course this also implies the invariance of the differential multiparameter sensitivity of the same networks.

3 Integral sensitivity

The previous definitions of sensitivity and the resultant theorems do have both theoretical and practical implications and although proved in general, their meaningful interpretations are restricted to a point-by-point frequency basis. It has been rightly pointed out[6] that a more significant sensitivity measure over a relevant frequency band will involve the integral of the appropriate functions.

The relative sensitivity is commonly defined as

$$S_e^{T_v} = \frac{e}{T_v} \frac{\partial T_v}{\partial e} = e \left[\frac{\partial N/\partial e}{N} - \frac{\partial D/\partial e}{D} \right] \qquad (18)$$

Now $N = a_n s^n + a_{n-1} s^{n-1} + \ldots + a_0$ where $a_i = a_i(e_1, \ldots e_p)$ where p is the number of network elements. Hence

$$\frac{\partial N/\partial e}{N} = \frac{\partial a_n/\partial e}{a_n} \left[\frac{s^n + \frac{(\partial a_{n-1}/\partial e)}{(\partial a_n/\partial e)} s^{n-1} + \ldots + \frac{(\partial a_0/\partial e)}{(\partial a_n/\partial e)}}{s^n + \frac{a_{n-1}}{a_n} s^{n-1} + \ldots + \frac{a_0}{a_n}} \right]$$

Let N have n distinct roots $s_t = \alpha_t + j\beta_t$ $t = 1, \ldots n$ and $\partial a_i/\partial e = a_i'$. Then

$$\frac{N'}{N} = \frac{a_n'}{a_n} \left[1 + \frac{F(s_1)}{s - s_1} + \ldots + \frac{F(s_n)}{s - s_n} \right] \qquad (19)$$

where

$$F(s_i) = \frac{\left(\frac{a_{n-1}'}{a_n'} - \frac{a_{n-1}}{a_n} \right) s_i^{n-1} + \ldots + \left(\frac{a_0'}{a_n'} - \frac{a_0}{a_n} \right)}{(s_i - s_1)(s_i - s_2) \ldots (s_i - s_n)}$$

and similarly for

$$\frac{D'}{D} = \frac{b_m'}{b_m} \left[1 + \sum_{r=1}^{m} \frac{G(s_r)}{s - s_r} \right] \qquad (20)$$

where D has m distinct roots $s = \gamma_r + j\epsilon_r$, $r = 1, \ldots, m$. Substituting eqns. 19 and 20 into eqn. 18 yields

$$\left.\left(\frac{N'}{N} - \frac{D'}{D}\right)\right|_{s=jw} = \left[\frac{a_n'}{a_n} - \frac{b_m'}{b_m}\right] + \frac{a_n'}{a_n}\sum_{t=1}^{n} \frac{F(s_t)}{-\alpha_t + j(\omega - \beta_t)} + \frac{b_m'}{b_m}\sum_{r=1}^{m} \frac{G(s_r)}{\gamma_r + j(\epsilon_r - \omega)}$$

$$\left.S_{\bar{e}}^{T_v}\right|_{s=jw} = eU + eV\sum_{t=1}^{n} \frac{F(s_t)}{[-\alpha_t + j(\omega - \beta_t)]} + eW\sum_{r=1}^{m} \frac{G(s_r)}{[\gamma_r + j(\epsilon_r - \omega)]} \quad (21)$$

where

$$U = \frac{a_n'}{a_n} - \frac{b_m'}{b_m}, \quad V = \frac{a_n'}{a_n}, \quad W = \frac{b_m'}{b_m}$$

Hence, from eqn. 21,

$$|S_e^{T_v}|_{s=jw} \leqslant |eU| + |eV|\sum_{t=1}^{n} \frac{|F(s_t)|}{[\alpha_t^2 + (\omega - \beta_t)^2]^{1/2}} + |eW|\sum_{r=1}^{m} \frac{|G(s_r)|}{[\gamma_r^2 + (\epsilon_r - \omega)^2]^{1/2}}$$

and for the case of a lowpass filter the integral of sensitivity over the passband interval is

$$\int_0^1 |S_e^{T_v}(s, e)|_{s=jw}\, d\omega \leqslant \left[|eU|\omega + |eV|\sum_{t=1}^{n} |F(s_t)| \sinh^{-1}\frac{\omega - \beta_t}{\alpha_t} - |eW|\sum_{r=1}^{m} |G(s_r)| \sinh^{-1}\frac{\epsilon_r - \omega}{\gamma_r}\right]_{\omega=0}^{1} \quad (22)$$

Theorem 3: The sum of the integrals of the differential modulus sensitivities of all the passive components of one type in an *RC* network with embedded operational amplifiers is noninvariant under a generalised scaled Howitt transformation.

Proof: Since the summations concerned are finite

$$\sum_{i=1}^{p} \int_0^1 |S_{e_i}^{T_v}|\, d\omega = \int_0^1 \sum_{i=1}^{p} |S_{e_i}^{T_v}| d\omega \quad (23)$$

Under a generalised scaled Howitt transformation it has already been established that

$$\sum_i S_{e_i}^{T_v} = \sum_i (S_{e_i}^{T_v})', \quad \text{i.e. invariance.}$$

However

$$\sum_i |S_{e_i}^{T_v}| \neq \sum_i |(S_{e_i}^{T_v})'| \quad (24)$$

and so

$$\sum_i \int_0^1 |S_{e_i}^{T_v}|\, d\omega \neq \sum_i \int_0^1 |(S_{e_i}^{T_v})'|\, d\omega \quad (25)$$

Hence the theorem.

Corollary: The sum of the integrals of the bounded large-change modulus sensitivities of all the passive components of one type in an *RC* network with embedded operational amplifiers is noninvariant under a generalised scaled Howitt transformation.

Proof: From eqns. 4 and 5

$$S_{\Delta e}^{T_v} = e\left[\frac{N'}{N} - \frac{D'}{D}\right]\left[1 - \Delta e\frac{D'}{D} + \left(\Delta e\frac{D'}{D}\right)^2\right] \quad (26)$$

The first term corresponds with that of the differential sensitivity already studied. Now consider the second term

$$S_{2\Delta e} = -e\Delta eW\left[1 + \sum_r \frac{G(s_r)}{s - s_r}\right]\left[U + V\sum_t \frac{F(s_t)}{s - s_t} - W\sum_r \frac{G(s_r)}{s - s_r}\right]$$

Integration over the passband interval $\omega = [0, 1]$ gives

$$\int_0^1 |S_{2\Delta e}|_{s=jw}\, d\omega \leqslant |e\Delta eW|\left[|U|\omega - |V|\sum_t |F(s_t)| \sinh^{-1}\left(\frac{\beta_t - \omega}{\alpha_t}\right) - |U - W|\sum_r |G(s_r)| \sinh^{-1}\left(\frac{\gamma_r - \omega}{\epsilon_r}\right) - |V|\sum_r\sum_t \frac{|F(s_t)||G(s_r)|}{\sqrt{(\alpha_t - \epsilon_r)^2 + (\beta_t - \gamma_r)^2}}\left\{\sinh^{-1}\left(\frac{\beta_t - \omega}{\alpha_t}\right) + \sinh^{-1}\left(\frac{\gamma_r - \omega}{\epsilon_r}\right)\right\} - |W|\sum_{r_1 \neq r_2}\sum \frac{|G(s_{r_1})||G(s_{r_2})|}{\sqrt{(\epsilon_{r_1} - \epsilon_{r_2})^2 + (\gamma_{r_1} - \gamma_{r_2})^2}}\left\{\sinh^{-1}\left(\frac{\gamma_{r_1} - \omega}{\epsilon_{r_1}}\right) + \sinh^{-1}\left(\frac{\gamma_{r_2} - \omega}{\epsilon_{r_2}}\right)\right\} - |W|\sum_r \frac{|G^2(s_r)|}{\epsilon_r} \tan^{-1}\left(\frac{\gamma_r - \omega}{\epsilon_r}\right)\Bigg]_{\omega=0}^{1}$$

A similar expression may be obtained for the third term.

Direct application of theorem 3 establishes the noninvariance of the sum of the integrals of the moduli of expressions of the type given in eqn. 26. Hence the corollary.

Theorem 4: The integral of the modulus of the bounded large-change multiparameter sensitivity of the passive components of an *RC* network with embedded operational amplifiers is invariant under a generalised scaled Howitt transformation.

Proof: With reference to eqns. 15–17 the bounded large-change multiparameter sensitivity function is invariant under transformation, and hence the integral of the modulus is also.

4 Examples and conclusions

Fig. 1 shows an initial circuit for a 3rd-order Butterworth function and Fig. 2 an equivalent network produced by transformation but having a reduced value for the sum squared sensitivity function evaluated at a typical value of $s = j1$. For the first circuit this numerical value taken over all components is 7·7016 and for the second circuit 6·8393, a moderate reduction. Examining the summed sensitivities according to the definitions given, over all conductances say, yields for the differential case values of 2·9154 and 2·9008. For component changes of 10% the bounded large-change sensitivity sums are 2·9030 and 2·8795 and for the bounded large-change multiparameter

sensitivity 0·2416 and 0·2416 for the respective circuits at $s = j1$. So considering the limits of accuracy in the calculations, these results confirm the invariance theorems.

For the integral definitions the following values are obtained, over all conductances, for the first circuit:

$$\sum \int_0^1 |S_e^{T_v}| d\omega \leqslant -1{\cdot}9999$$

and for the transformed circuit

$$\sum \int_0^1 |S_e^{T_{v'}}| d\omega \leqslant -7{\cdot}3133$$

and bounded large change integral sensitivity evaluations give

$$\sum \int_0^1 |S_{\Delta e}^{T_v}| d\omega \leqslant -2{\cdot}7486$$

and

$$\sum \int_0^1 |S_{\Delta e}^{T_{v'}}| d\omega \leqslant -6{\cdot}7217$$

The results demonstrate again the care required in specifying sensitivity measures. The sums of the integrals of the moduli of differential and large-change sensitivities are noninvariant and can be grouped with the other noninvariant measures such as the sum of sensitivity squares or moduli.

The sensitivity measures having real practical significance, the bounded large-change multiparameter sensitivity and the integral of the modulus of this function exhibit a complete invariance, when the network is subject to a fairly general class of equivalence transformations, and this confirms an underlying practical feature.

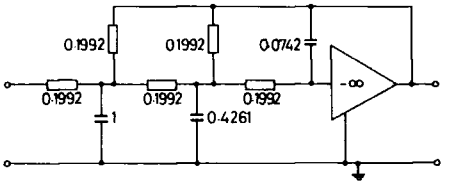

Fig. 1 *Initial realisation of a 3rd-order Butterworth function*
Elements in siemens and farads

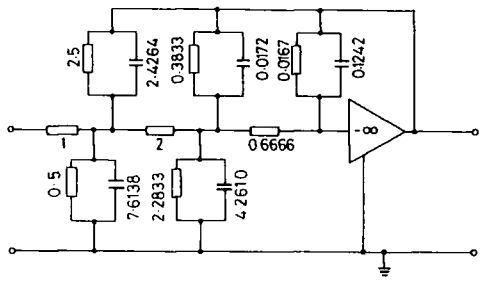

Fig. 2 *Reduced sum-squared-sensitivity realisation of a 3rd-order Butterworth function*

5 Acknowledgment

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7 Appendix

Consider the second terms in eqns. 5 and 6. It is necessary to show that

$$\sum_{\text{all conductances}} S''_{\Delta e} = -e \sum_k \sum_l E_{kl}^{ND} \frac{\partial y_{kl}}{\partial e} \Delta e \sum_k \sum_l \frac{E_{kl}^D}{D} \frac{\partial y_{kl}}{\partial e} \tag{27}$$

$$= -\frac{1}{D} \sum_{\text{diagonal}} Y^T E^{ND} (\Delta Y_G)^T E^D \tag{28}$$

where ΔY_G is the matrix of entry increments.

For a network with n nodes and m operational amplifiers, for simplicity consider single input/output type, where I_l is the input at the node l and O_l is the output at node l. Let $f = n - 2m$, the number of nodes not connected to an amplifier. Also $e_{ij} = e_{ji}$ and $e_{ij} \Delta e_{kl} = 0$, $\forall (i \neq k, j \neq l)$. Eqn. 27 gives:

$$\sum_{\text{all conductances}} S''_{\Delta e} = -\frac{1}{D} \sum_{a=1}^{f} \sum_{b=a+1}^{f} \sum_{l=1}^{m} \sum_{s=1}^{m}$$
$$[e_{aa} \Delta e_{aa} E_{aa}^{ND} E_{aa}^D + e_{ab} \Delta e_{ab} (E_{aa}^{ND} + E_{bb}^{ND} - E_{ab}^{ND}$$
$$- E_{ba}^{ND})(E_{aa}^D + E_{bb}^D - E_{ab}^D - E_{ba}^D) + e_{aO_l} \Delta e_{aO_l}$$
$$(E_{aa}^{ND} - E_{aO_l}^{ND})(E_{aa}^D - E_{aO_l}^D) + e_{aI_l} \Delta e_{aI_l} (E_{aa}^{ND} - E_{I_l a}^{ND})$$
$$(E_{aa}^D - E_{I_l a}^D) + e_{O_l I_s} \Delta e_{O_l I_s} (-E_{I_l O_s}^{ND})(-E_{I_l O_s}^D)]$$

Equating to eqn. 28

$$\Sigma S''_{\Delta e} = -\frac{1}{D} \sum_{\text{diagonal}} Y^T E^{ND} (\Delta Y)^T E^D = P_{n,m}$$

For a network of $n + 1$ nodes, m amplifiers and $f' = f + 1$ free nodes

$$\Sigma S''_e = P_{n,m} - \frac{1}{D} \Bigg[e_{f'f'} \Delta e_{f'f'} E_{f'f'}^{ND} E_{f'f'}^D$$
$$+ \sum_{a=1}^{f} e_{af'} \Delta e_{af'} (E_{aa}^{ND} + E_{f'f'}^{ND} - E_{af'}^{ND} - E_{f'a}^{ND})$$
$$(E_{aa}^D + E_{f'f'}^D - E_{af'}^D - E_{f'a}^D)$$
$$+ \sum_{l=1}^{m} e_{f'O_l} \Delta e_{f'O_l} (E_{f'f'}^{ND} - E_{f'O_l}^{ND})(E_{f'f'}^D - E_{f'O_l}^D)$$
$$+ \sum_{l=1}^{m} e_{f'I_l} \Delta e_{f'I_l} (E_{f'f'}^{ND} - E_{I_l f'}^{ND})(E_{f'f}^D - E_{I_l f'}^D) \Bigg]$$

$$= -\frac{1}{D}\left[\sum_{a=1}^{f'} e_{aa}\Delta e_{aa}E_{aa}^{ND}E_{aa}^{D} + \sum_{a=1}^{f'}\sum_{b=a+1}^{f'} e_{ab}\Delta e_{ab}(E_{aa}^{ND}+E_{bb}^{ND}-E_{ab}^{ND}-E_{ba}^{ND})(E_{aa}^{D}+E_{bb}^{D}-E_{ab}^{D}-E_{ba}^{D}) + \sum_{a=1}^{f'}\sum_{l=1}^{m} e_{aO_l}\Delta e_{aO_l}(E_{aa}^{ND}-E_{aO_l}^{ND})(E_{aa}^{D}-E_{aO_l}^{D}) + \sum_{a=1}^{f'}\sum_{l=1}^{m} e_{al_l}\Delta e_{al_l}(E_{aa}^{ND}-E_{l_la}^{ND})(E_{aa}^{D}-E_{l_la}^{D}) + \sum_{l=1}^{m}\sum_{s=1}^{m} e_{l_lO_s}\Delta e_{l_lO_s}(-E_{l_lO_s}^{ND})(-E_{l_lO_s}^{D})\right]$$

$$= P_{n+1,m}$$

Similarly for a network with n nodes, $m+1$ amplifiers, $f'=f-2$

$$\Sigma S_e'' = -\frac{1}{D}\left[\sum_{a=1}^{f'}\sum_{b=a+1}^{f'}\sum_{l=1}^{m+1}\sum_{s=1}^{m+1} e_{aa}\Delta e_{aa}E_{aa}^{ND}E_{aa}^{D} + e_{ab}\Delta e_{ab}(E_{aa}^{ND}+E_{bb}^{ND}-E_{ab}^{ND}-E_{ba}^{ND})(E_{aa}^{D}+E_{bb}^{D}-E_{ab}^{D}-E_{ba}^{D}) + e_{aO_l}\Delta e_{aO_l}(E_{aa}^{ND}-E_{aO_l}^{ND})(E_{aa}^{D}-E_{aO_l}^{D}) + e_{al_l}\Delta e_{al_l}(E_{aa}^{ND}-E_{l_la}^{ND})(E_{aa}^{D}-E_{l_la}^{D}) + e_{l_lO_s}\Delta e_{l_lO_s}(-E_{l_lO_s}^{ND})(-E_{l_lO_s}^{D})\right]$$

$$= P_{n,m+1}$$

Finally, for a network with $n+1$ nodes, $m+1$ amplifiers, $f'=f-1$

$$\Sigma S_e'' = -\frac{1}{D}\left[\sum_{a=1}^{f'}\sum_{b=a+1}^{f'}\sum_{l=1}^{m+1}\sum_{s=1}^{m+1} e_{aa}\Delta e_{aa}E_{aa}^{ND}E_{aa}^{D} + e_{ab}\Delta e_{ab}(E_{aa}^{ND}+E_{bb}^{ND}-E_{ab}^{ND}-E_{ba}^{ND})(E_{aa}^{D}+E_{bb}^{D}-E_{ab}^{D}-E_{ba}^{D}) + e_{aO_l}\Delta e_{aO_l}(E_{aa}^{ND}-E_{aO_l}^{ND})(E_{aa}^{D}-E_{aO_l}) + e_{al_l}\Delta e_{al_l}(E_{aa}^{ND}-E_{l_la}^{ND})(E_{aa}^{D}-E_{l_la}^{D}) + e_{l_lO_s}\Delta e_{l_lO_s}(-E_{l_lO_s}^{ND})(-E_{l_lO_s}^{D})\right]$$

$$= P_{n+1,m+1}$$

For a specific case of $n=3$, $m=1$ these expressions hold, hence the second term can be written

$$\sum_{\substack{\text{all}\\ \text{conductances}}} S'_{\Delta e} = -\frac{1}{D}\sum_{\text{diagonal}} Y^T E^{ND}(\Delta Y)^T E^D$$

The same process can be used to identify the other terms in eqn. 6.

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ON THE GENERATION OF EQUIVALENT SWITCHED CAPACITOR NETWORKS

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Abstract - By reformulating the fundamental describing matrices in a manner that permits access to basic theorems governing the existence and structure of relevant transformation matrices, this paper develops a general theory for the generation of equivalent switched capacitor (SC) networks. The method is pertinent to the common 2-phase SC networks and is easily demonstrated on a simple second order SC filter network. It also provides the foundation for a general transformation program SCNAPT.

1. INTRODUCTION

The generation of equivalent networks using matrix transformations was originated by Howitt[1]. The method was later adapted by Schoeffler and others to obtain passive networks with minimal sensitivities [2]. More recently, equivalent network theory has been extended to include active RC circuits [3], [4]. Some limited results for the SC case include a method for obtaining an equivalent strays free active circuit from a given strays sensitive circuit [5], an adaptation of Schoeffler's method using SC building blocks (SCB's) [6], and an application of state space methods to produce equivalent circuits with minimum capacitor ratio and total capacitance [7].

In this paper a systematic general theory is presented which enables modification to be made to circuit parameters and topology at component level, and applies equally to passive and active networks. Using z-domain formulation of the nodal charge equations, it is demonstrated both in theory and by example that a wide class of distinct but equivalent networks can be obtained using two sided scalar transformations of a reformulated MNA matrix (RMNA). For simplicity of presentation, only circuits with two non-overlapping clock phases will be considered; the corresponding time slots will be referred to as *odd* and *even* respectively.

2. EVALUATION OF TRANSFER FUNCTIONS USING MODIFIED NODAL ANALYSIS

A variety of equivalent presentations of the nodal equations of SC networks are in current use. The presentation described in this section combines nodal analysis in the z-domain [8] with the modified nodal approach (MNA) [9], to produce a matrix description which always includes the complete admittance matrix of the passive part of the network in symmetric form. Details of the matrix formulation are shown in (1); since the evaluation of solutions is not involved, arguments favouring a full clock cycle definition of z, as used in [10], do not apply. The scheme is based on the elemental switch time for the definition of z, and has the advantage of retaining the total system description within the matrix.

Suppose that the network under consideration has n nodes, and that of these the first p form an independent set of nodes after both *even* and *odd* switching has taken place. (This restriction is not essential to the subsequent analysis; however its simplifying effect enables the principle features of the argument to be presented more clearly). The 2p x 2p passive admittance matrix (PAM) Y is constructed from the capacitor matrix C and the *even* and *odd* switching matrices S_e and S_o using

$$M = \left[\begin{array}{c|c} S_e^{\,t} C S_e & -z^{-1} S_e^{\,t} C S_o \\ \hline -z^{-1} S_o^{\,t} C S_e & S_o^{\,t} C S_o \end{array}\right]$$

The switching matrices are in standard form [8]; note that separate current and voltage derivations of $S_e^{\,t}$, $S_o^{\,t}$ and S_e, S_o respectively, are unnecessary. Note also that all non-zero off diagonal terms in S_e and S_o occur in rows p+1, ...,n and columns 1, ...,p, and that Y is obtained from M by deletion of the zero rows and columns p+1, ...,n, n+p+1, ...,2n.

The submatrix R of T includes the constraints due to the active devices (assumed here to be VCVS's), the vector I represents the current variables introduced as a result of the MNA method, and S contains entries due to the resulting current balance equations. Note that input is at node 1, and that (1) represents the equations for *even* excitation. Since V_1^e has been normalised to 1, the transfer functions $H_{ee}(z)$, $H_{eo}(z)$ may be equated to V_2^e and V_2^o respectively, which are readily evaluated

$$\begin{bmatrix} Y_{ee} & -z^{-1}Y_{eo} & \begin{matrix}1&0\\0&\cdot\\\cdot&\cdot\\\cdot&\cdot\\0&0\end{matrix} & S \\ -z^{-1}Y_{oe} & Y_{oo} & \begin{matrix}0&0\\\cdot&\cdot\\\cdot&\cdot\\\cdot&\cdot\\0&1\end{matrix} & \\ \begin{matrix}1&0&\cdots&\cdots&0\\0&1&0&\cdots&0\end{matrix} & & & 0 \\ R & & & \end{bmatrix} \begin{bmatrix} V_1^e \\ \cdot \\ \cdot \\ V_p^e \\ V_1^o \\ \cdot \\ \cdot \\ V_p^o \\ I \end{bmatrix} = \begin{bmatrix} 0 \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ 0 \\ 1 \\ 0 \\ \cdot \\ \cdot \\ \cdot \\ 0 \end{bmatrix} \quad \ldots\ldots (1)$$

or, simply, $TX = U_{2p+1}$

using Cramer's Rule. To obtain $H_{oo}(z), H_{oe}(z)$, it is necessary to replace the unit vector U_{2p+1} by U_{2p+2}, then solve the resulting equations for V_2^o and V_2^e respectively.

Two circuits will be said to be equivalent (*resp.* scaled equivalent) with respect to a given transfer function if the transfer function of the second circuit is the same as (*resp. a scalar multiple of*) that of the first.

3. REFORMULATION OF THE MNA

Consider whether a class of two-sided transformations of T exists such that $T' = GTH$ is the matrix representation of a distinct SC network in modified nodal form. If G and H were to have scalar entries and a block diagonal form, then scalar and non-scalar entries in T' would automatically occur in the correct positions. If in addition, the submatrix of G consisting of elements in rows and columns $1,\ldots 2p$ were transpose of the corresponding submatrix P of H, then symmetry of the transformed PAM would be assured (see (2)).

$$\begin{bmatrix} P_1^t & 0 & \\ 0 & P_2^t & 0 \\ & A & \end{bmatrix} \begin{bmatrix} Y_{ee} & z^{-1}Y_{eo} & \\ -z^{-1}Y_{oe} & Y_{oo} & W \\ V & & 0 \end{bmatrix} \begin{bmatrix} P_1 & 0 & \\ 0 & P_2 & 0 \\ 0 & B & \end{bmatrix}$$

$$= \begin{bmatrix} P_1^t Y_{ee} P_1 & -z^{-1} P_1^t Y_{eo} P_2 & P^t W B \\ -z^{-1} P_2^t Y_{oe} P_1 & P_2^t Y_{oo} P_2 & \\ A\ V\ P & & 0 \end{bmatrix} \qquad \ldots (2)$$

or, simply, $GTH = T'$

Unfortunately, the following difficulty arises. If two distinct capacitor matrices C and C' with the same rank and dimension are given, and if Y and Y' are corresponding PAMs, then, in general, no block diagonal scalar matrix P exists for which $Y' = P^t Y P$. A primary reason is that the number of unknowns in P, $2p^2$, is smaller than the number of equations needing to be satisfied, which is, taking due account of symmetry, $2p^2+p$.

To overcome this difficulty, without sacrificing the advantages of transformations of the type shown in (2) we shall reformulate the matrix presentation (1). The key to the problem is the singularity of the switching matrices S_e and S_o.

Consider a modified switching matrix $\tilde{S}_e$ defined by:

$$(\tilde{S}_e)_{ij} = (S_e)_{ij} \quad \forall\ i, j \in \{1,\ldots,n\},\ i \neq j$$

$$(\tilde{S}_e)_{ii} = 1 \qquad \forall\ i \in \{1,\ldots,n\}$$

Thus $\tilde{S}_e$ is identical to S_e except that zeros on the diagonal have been replaced by 1's. Suppose $\tilde{S}_o$ is defined similarly. Then

Lemma 1: *$\tilde{S}_e$ and $\tilde{S}_o$ are non-singular.*

Proof: Let $I = \{1,\ldots, p\}$, $D = \{p+1,\ldots,n\}$ be the sets of independent and dependent nodes respectively. As noted earlier, the non-zero off diagonal terms in S_e occur only in rows $p+1,\ldots,n$ and columns $1,\ldots,p$.

Hence, if $\ell \in I$,

$$(\tilde{S}_e)_{\ell m} = \begin{cases} 0 & \forall\ m \in \{1, \ldots, n\} \setminus \ell \\ 1 & \text{if} \quad m = \ell \end{cases} \qquad \ldots (3)$$

and if $s,t \in D$,

$$(\tilde{S}_e)_{st} = \begin{cases} 0 & \text{if} \quad s \neq t \\ 1 & \text{if} \quad s = t \end{cases} \qquad \ldots (4)$$

Also,

$$\det \tilde{S}_e = \sum \pm (\tilde{S}_e)_{1j} (\tilde{S}_e)_{2k} \ldots\ldots\ldots\ldots (\tilde{S}_e)_{nr}$$

where $\{j, k, \ldots r\} = \{1,\ldots n\}$ and the sum is taken over all permutations of the second subscripts. From (3) every non-zero element in this sum has the form

$$\prod_{i=1}^{p} (\tilde{S}_e)_{ii} \prod_{s,t \in D} (\tilde{S}_e)_{st}$$

so that, from (4), the only non-zero element of the sum is

$$\prod_{i=1}^{n} (\tilde{S}_e)_{ii}$$

It follows that $\det \tilde{S}_e = 1$; similarly $\det \tilde{S}_o = 1$ so the lemma is proved.

Lemma 2: *If* $\tilde{M} = \begin{bmatrix} \tilde{S}_e^t C \tilde{S}_e & -z^{-1} \tilde{S}_e^t C \tilde{S}_o \\ -z^{-1} \tilde{S}_o^t C \tilde{S}_e & \tilde{S}_o^t C \tilde{S}_o \end{bmatrix}$ *and if $\tilde{Y}$ is obtained from $\tilde{M}$ by deleting rows and columns* $p+1,\ldots,n$ *then* $\tilde{Y} = Y$.

Proof: If I, D are as in Lemma 1, then if $\ell \in I$

$$(\tilde{S}_e^t)_{\ell q} = (S_e^t)_{\ell q} \qquad \forall\ q \in \{1,\ldots n\}$$

and if $m \in I$,

$$(\tilde{S}_e)_{rm} = (S_e)_{rm} \qquad \forall\ r \in \{1,\ldots n\}$$

Hence for each ℓ, m in I

$$(\tilde{S}_e^t C \tilde{S}_e)_{\ell m} = \sum_{q=1}^{n} \sum_{r=1}^{n} (\tilde{S}_e^t)_{\ell q} C_{qr} (\tilde{S}_e)_{rm}$$

$$= \sum_{q=1}^{n} \sum_{r=1}^{n} (S_e^t)_{\ell q} C_{qr} (S_e)_{rm}$$

$$= (S_e^t C S_e)_{\ell m}$$

and a similar relationship holds for $\tilde{S}_e^t C \tilde{S}_o$, $\tilde{S}_o^t C \tilde{S}_e$, $\tilde{S}_o^t C \tilde{S}_o$. The lemma now follows from the construction of Y.

From henceforth the matrix $\tilde{M}$ in Lemma 2 will be referred to as the extended passive admittance matrix (EPAM). The following corollary to Lemma 1 is immediate:

Corollary: *If $\tilde{M}$ and $\tilde{M}'$ are EPAMs corresponding to two distinct capacitor matrices* C *and* C' *which have the same dimension and full rank, then there exists a block diagonal scalar matrix* P *such that* $\tilde{M}' = P^t \tilde{M} P$.

Proof: Since C and C' are positive definite, there exists a non-singular matrix Q such that $C' = Q^t C Q$. By Lemma 1, $\tilde{S}_e$ and $\tilde{S}_o$ are non-singular so if,

$$P = \begin{bmatrix} P_1 & 0 \\ 0 & P_2 \end{bmatrix}$$

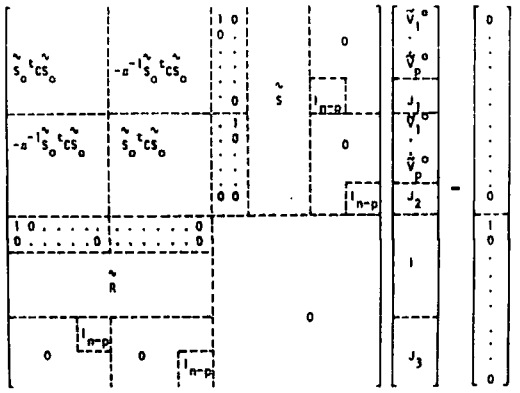
where P_1, P_2 are n x n matrices such that

$$P_1 = \tilde{S}_e^{-1} Q \tilde{S}_e \quad , \quad P_2 = \tilde{S}_o^{-1} Q \tilde{S}_o \qquad \ldots (5)$$

then P satisfies $\tilde{M}' = P^t \tilde{M} P$

Thus by Lemma 2, $\tilde{M}$ contains the PAM Y as a submatrix, and by Lemma 2 and the Corollary, one PAM can now be obtained from another by means of a very convenient type of congruence transformation. It would therefore seem desirable if $\tilde{M}$ rather than Y could be incorporated into the matrix formulation of the nodal equations in such a way that the existence of the extra rows and columns did not alter the solutions $V_1^e, \ldots, V_p^e, V_1^o, \ldots, V_p^o$.

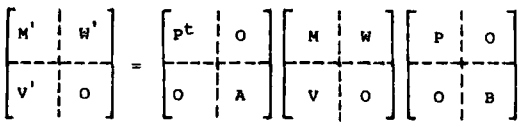
Consider the set of equations presented in matrix form in (6). The presence of the four submatrices I_{n-p} effectively removes rows and columns p+1,..., n,n+p+1, ..2n in the evaluation of the determinant of any submatrix of $\tilde{T}$ containing these four identity blocks. Therefore by Cramer's Rule and Lemma 2, $\tilde{V}_i^e = V_i^e$, $\tilde{V}_i^o = V_i^o$ $\forall$ i $\in$ {1,...,p}, where $\{V_i^e, V_i^o, i = 1, .., p\}$ are solutions of the original set of equations (1).



or simply, $\tilde{T}X_o = U_{2n+1}$ ... (6)

Comparing (1) with (6), it is seen that a number of new unknowns have been introduced into the second set of equations, in the vectors J_1, J_2, J_3. However, all solutions of interest are the same in both formulations, so the formulation (6) may be adopted instead of (1), as convenient. The advantages are clear in the context of two sided transformations of $\tilde{T}$.

Consider the transformation of $\tilde{T}$ shown in (7),where G and H are scalar matrices and P is as in the Corollary.



or, simply, $\tilde{T}' = G\,\tilde{T}\,H$ ... (7)

Not only is one PAM readily obtained from another on account of the Corollary, the remaining equations which need to be satisfied present no obstacle either. For, consider the equations AVP = V', $P^tWB = W'$, or equivalently, $AV = V'P^{-1}$, $WB = W'(P^t)^{-1}$,where A and B are k x k matrices; clearly for fixed V,V', W, W', the number of unknowns in B, A and P, $2(k^2+n^2)$, cannot be less than the number of linear equations to be satisfied in these unknowns, which is 4nk. Therefore, subject to the entries of P being such that $C' = Q^tCQ$ is realisable, there seems a good prospect that distinct networks can be obtained by transformations of the RMNA $\tilde{T}$ as shown in (7).

4. EQUIVALENCE TRANSFORMATIONS USING THE RMNA

Let us suppose that matrix transformations of the RMNA can yield realisable new SC networks and enquire whether it is possible to restrict the entries of such transformations so that equivalence of the new networks is assured.

The theorem presented below gives a set of sufficient conditions for the invariance of $H_{ee}(z)$ up to a scalar multiple under the type of transformation of the RMNA shown in (7). Only quite simple adjustments are required to obtain the analogous conditions for any or all of the other transfer functions. The approach is a natural extension of earlier methods [1], [4], and realisability constraints on C' do not occur as conditions in the theorem but must be separately considered.

Theorem: *Let the non-singular matrix* $\tilde{T}$ *be the RMNA of a SC networks with* n *nodes, input and output being at nodes* 1 *and* 2 *respectively. Let* G *and* H *be scalar block diagonal matrices as in* (7) *with the following properties:*

(i) G *is non-singular*
(ii) *the first row of* H *is* $\ell^{-1}U_1^t$
(iii) *the second row of* H *is* k U_2^t
(iv) *the* (2n+1)*th row of* G *is* ℓU_{2n+1}^t
(v) *the* (2n+1)*th column of* G *is* ℓU_{2n+1}

where U_i *denotes the ith unit vector.*
Then if $\tilde{G}\tilde{T}H$ *is the RMNA of a realisable network,*

$$H_{ee}'(z) = (\ell k)^{-1} H_{ee}(z)$$

where $H_{ee}(z)$ *and* $H_{ee}'(z)$ *are the even input/even output voltage transfer functions of the networks corresponding to* $\tilde{T}$ *and* $\tilde{T}' = \tilde{G}\tilde{T}H$ *respectively.*

Proof: It suffices to show that the first and second entries X_1 and X_2 of the solution vector X of

$$G\,\tilde{T}\,H\,X = U_{2n+1} \qquad \ldots(8)$$

are suitable scalar multiples of the first and second entries $(X_o)_1$ and $(X_o)_2$ of the solution vector X_o of

$$\tilde{T}\,X_o = U_{2n+1} \qquad \ldots(9)$$

Now by condition (v)

$$\ell^{-1}\,G\,U_{2n+1} = U_{2n+1}$$

so that from (8), condition (i) and (9)

$$\ell\,\tilde{T}\,H\,X = U_{2n+1} = \tilde{T}\,X_o$$

since T is non-singular, it follows that

$$\ell\,H\,X = X_o$$

so that $X_2 = (\ell k)^{-1}\,(X_o)_2$ by condition (ii). The structure of $\tilde{T}$ ensures that $(X_o)_1 = V_1^e = 1$ (see (6)), and conditions (ii) and (iv) ensure that the (2n+1)th row of $\tilde{G}\tilde{T}H$ is U_{2n+1}^t so that $X_1 = 1$. The theorem is now proved.

If $\tilde{T}$ is the RMNA of a realisable network, it seems reasonable to expect that, in general, $\tilde{T}'$ will be non-singular as in the hypothesis of the theorem. Note that conditions (i) - (v) ensure only that certain solutions are preserved after transformation of $\tilde{T}$, and that additional conditions are necessary to ensure that $\tilde{G}\tilde{T}H$ has the structure of an RMNA. For example, if the original amplifier and switching arrangements are to be retained, then conditions (ii) and (iv) would be replaced by AVP = V and $P^tWB = W$, in the notation of (6), and realisability constraints on $\tilde{M}'$ would also be necessary. Nevertheless, application of the theorem can produce equivalent SC networks in infinite variety, as will now be shown.

5. APPLICATION TO SECOND ORDER FILTER

Consider the second order active SC filter shown in Fig 1. Nodes 1 - 4 are independent, nodes 5 - 7 are dependent, and if C is the capacitor matrix of the filter then

$$C' = Q^tCQ \qquad \ldots(10)$$

where

$$Q = \begin{bmatrix} k & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & k & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & q & 0 & 0 & 0 & k-q \\ 0 & 0 & 0 & k & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & k & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & k & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & k \end{bmatrix} \qquad \ldots(11)$$

E7.1

$$k > 0 \quad , \quad \frac{(C_1 + C_3 + C_4)k}{C_1 + C_2 + C_3 + C_4} \leq q \leq k \quad \ldots(12)$$

is a realisable capacitor matrix. Moreover, if P is derived from Q using (5), and A and B from the relations AVP = V, $P^t WB = W$ (cf (7)), then $\tilde{GTH}$ is a transformation of the RMNA $\tilde{T}$ of the filter satisfying the conditions of the theorem, where G and H are in (7). Therefore, each SC network whose capacitor matrix C' satisfies (10), (11), (12) above and whose switching and amplifier arrangements are as in Fig 1 is equivalent to the filter in Fig 1. Two examples are shown in Figs 2 and 3; note that the original network corresponds to k = q = 1. Analysis of these three equivalent networks using the computer program SCNAP 2 shows good agreement of the transfer functions.

Note that, since k and q can take a continuous range of values, the same is true of the capacitance values of the networks in the equivalence class. Moreover, this class of equivalent networks is only a small subset of the class of all networks which are equivalent to the filter of Fig. 1 and can be obtained using the conditions of the theorem. Hence optimisation with respect to such parameters as component sum and spread, or sensitivity would seem to be one possible application of the theory.

A general transformation and optimisation program SCNAPT which is being developed will facilitate a comprehensive implementation of this theory.

6. CONCLUSIONS

A simplified theory has been developed to enable the generation of equivalent SC networks. Fundamental theorems relating to the existence of equivalence transformations have been proved and the application to one simple SC filter network is shown. Results from the application of the general transformation program SCNAPT to a variety of larger filter networks will follow.

ACKNOWLEDGEMENTS

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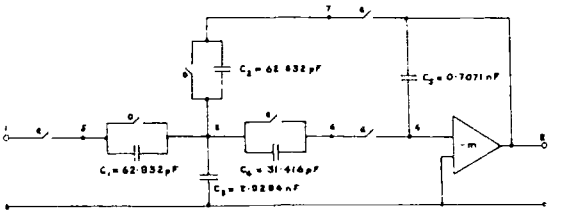

FIG. 1 : SECOND ORDER ACTIVE SC FILTER

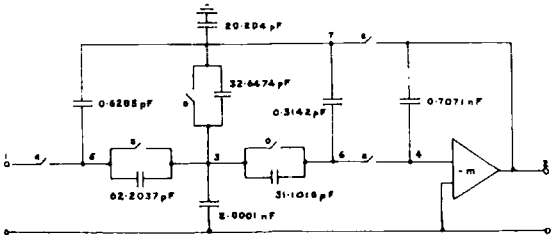

FIG. 2 : EQUIVALENT FILTER WITH k=1, q=0.99

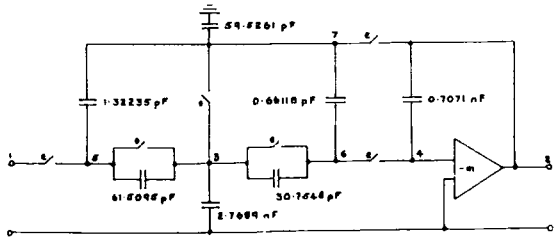

FIG. 3 : EQUIVALENT FILTER WITH k=1, q=0.978954

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OPTIMISATION OF SWITCHED CAPACITOR NETWORKS USING EQUIVALENCE TRANSFORMATIONS

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ABSTRACT

Provided a single network realisation of a desired transfer function is available, an infinite class of distinct but equivalent networks can be generated using special congruence transformations of the capacitor matrix. Continuity properties of these transformations enable improvements to network parameters, such as capacitor sum and spread, dynamic range or sensitivity, to be achieved while desired transfer functions are preserved. To implement the method, a program SCNAPT, incorporating a constrained optimisation subroutine, has been developed; as illustration, the application to a range of two-phase strays insensitive switched capacitor networks is discussed.

INTRODUCTION

The recent development of a theory of equivalence transformations for switched capacitor (SC) networks enables modifications to component values and network topology to be achieved while preserving one or more transfer functions. Starting from a single network realisation, an infinite class of equivalent networks can normally be generated using matrix transformations; possible modifications to network parameters which can be achieved include the growth and loss of capacitors, and alterations to capacitor values, amplifier gain or switching arrangements [1], [2], [3].

Owing to continuity properties of the transforming matrices, equivalence theory can be applied to network design using constrained non-linear optimisation techniques. It is normally possible to optimise a given network with respect to component sum, spread, dynamic range, sensitivity or indeed any other performance factors which can be formulated suitably in terms of a continuous objective function. Other features of interest, such as layout or number of components, can also be taken into account by appropriate adjustments to the constraints.

EQUIVALENCE TRANSFORMATIONS

To adapt the classical method of Howitt [4], the MNA representation of nodal charge equations in the z-domain is reformulated in terms of an enlarged RMNA system matrix T. This enables a class of transformation matrices {G,H} to be identified which have the property that relevant solutions, and hence transfer functions, of the matrix equation (1) representing the initial network

$$T\underline{X} = \underline{W} \qquad (1)$$

and of the transformed system

$$GTH\underline{X}' = \underline{W} \qquad (2)$$

are identical. Restrictions to the entries of G and H ensure not only the invariance of certain solutions, but also that T' = GTH has the structure of an RMNA matrix. The resulting networks may be exact or scaled equivalents with respect to any or all of the voltage transfer functions, as desired [1], [2].

Equivalence transformations can also be expressed as congruence transformations

$$C' = Q^{t}CQ \qquad (3)$$

of the nxn capacitor matrix C of the initial network, the entries of Q being suitably restricted; this formulation can be deduced from (2) and is more convenient from the point of view of computer implementation. The unrestricted entries of Q constitute an n^2- dimensional Euclidean space, and the restricted entries a constrained space ψ. Every point in ψ corresponds to a realisable network which is equivalent to the initial network, and may have the same, or different, amplifier and switching arrangements.

If equivalent networks are required which have the same amplifier and switching arrangements as the initial network, the corresponding subset of ψ will usually include a simply connected region κ which contains the point $Q = I_n$ corresponding to the initial network. Starting from $Q = I_n$, it is then normally possible to move around in κ in incremental steps until some desired optimal point is reached. For this reason equivalence transformations which preserve the switching and amplifier arrangements of an initial network may be applied to SC network design using standard optimisation techniques. The fundamental theorem governing equivalence transformations of this type may be stated for two phase networks as follows:

Theorem: *Let the* nxn *matrix* C *be the capacitor matrix of a given SC network* N *with* n *nodes. Let the scalar matrices* $\tilde{S}_e$, $\tilde{S}_o$ *and* K_e, K_o *denote the modified even and odd switching matrices and gain matrices respectively, suppose the RMNA matrix of* N *is non-singular, and that non-singular* nxn *matrices* P_e, P_o *and* Q *satisfy*

(i) $Q = \tilde{S}_e P_e \tilde{S}_e^{-1} = \tilde{S}_o P_o \tilde{S}_o^{-1}$

(ii) $R_e = [P_e]_{11} + K_e[P_e]_{21}$ *and* $R_o = [P_o]_{11} + K_o[P_o]_{21}$ *are non-singular,*

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(iii) $[P_e]_{12} = [P_o]_{12} = 0$

(iv) $R_e K_e = K_e [P_e]_{22}$, $R_o K_o = K_o [P_o]_{22}$

(v) *the 1st column of* R_e *is* $\underline{U}_1$

(vi) *the 2nd row of* P_e *is* $k^{-1} \underline{U}_2^t$, $k>0$,

(vii) $C' = Q^t C Q$ *is a realisable capacitor matrix,*

where $\underline{U}_i$ *denotes the* i*th unit vector.*

If $H_{ee}(z)$ *and* $H_{ee}'(z)$ *respectively denote the even input/even output voltage transfer function of* N *and of the network with capacitor matrix* C' *and the same switching and amplifier arrangements as* N, *then*

$$H_{ee}'(z) = k\, H_{ee}(z)$$

Further details and notation may be found in [2]. Since $P_e = \hat{S}_e^{-1} Q S_e$, $P_o = \hat{S}_o^{-1} Q \hat{S}_o$ and the entries of $\hat{S}_e, S_e, K_e$ and K_o are fixed real numbers determined by the initial network N, the conditions of the theorem constitute, in effect, a set of constraints on the entries of Q. Where the initial network is strays free, some slight adjustments are normally required to ensure that a satisfactory class of equivalent networks is generated; this aspect will now be considered.

STRAYS INSENSITIVE NETWORKS

In the practical implementation of SC filter structures using MOS technology it is important where possible to adopt topologies which ensure insensitivity to stray capacitances to ground. It is usual therefore to design such networks so that

(a) *the amplification of the op-amps is large*

(b) *in each switching phase, every node is either a low impedance node or a virtual ground*

(c) *a capacitor node is never switched from a low impedance node, other than ground, to a virtual ground.*

It has been shown that conditions (b) and (c) are sufficient to ensure complete insensitivity to strays under the assumption of ideal operational amplifiers [5]. From now on, "strays insensitive" will refer only to networks satisfying (a), (b) and (c), and for the purposes of equivalence transformations, such networks are assumed to have infinite amplifier gain.

If a given SC network N satisfies (a), (b) and (c), then the same is true of every network generated from N using the conditions of the theorem; this is because the only possible modifications to network topology are the growth and loss of capacitors which cannot affect the classification of nodes. In theory, therefore, the conditions of the theorem are sufficient not only to preserve the transfer function $H_{ee}(z)$ but also to preserve strays insensitivity whenever this is present in the initial network.

In practice, however, many of the potentially equivalent topologies cannot be generated from an initial network which is strays insensitive by straightforward application of the theorem. This is because congruence transformations preserve rank, and the typically low rank of the capacitor matrix in strays insensitive networks is likely to be affected by small changes in network topology. Fortunately, some slight adjustments to the usual procedure enable this problem to be overcome.

In strays insensitive networks, a significant proportion of possible capacitor connections never contribute to network functioning; in the case of 2-phase networks, for example, only those categories of connections listed in Table I can ever contribute. One method of overcoming the problem of low rank in the capacitor matrix, therefore, is to incorporate additional functionally redundant, or 'phantom', capacitor elements into the initial network date in order to increase the rank of the initial capacitor matrix C. After applying an equivalence transformation (3), any functionally redundant capacitors in the network with capacitor matrix C' are removed to yield the final equivalent network [3].

Type	Capacitor Plate 1		Capacitor Plate 2	
	connected to	switching phase	connected to	switching phase
I	i/p of network	e	virtual ground	e
II	virtual ground	e	op-amp o/p	e
III	i/p of network	e	virtual ground	o
IV	virtual ground	e	op-amp o/p	o
V	op amp o/p	o	virtual ground	o
VI	virtual ground	o	op-amp o/p	o

TABLE I: CATEGORIES OF CAPACITOR CONNECTIONS WHICH CONTRIBUTE TO $B_{ee}(z)$ IN 2-PHASE STRAYS INSENSITIVE NETWORKS

An alternative approach, which avoids the explicit introduction of phantom elements, is based on the removal of unnecessary realisability constraints from the transformed matrix C'. In this method, C is the capacitor matrix of the initial network, and the entries of Q and C' in (3) are restricted in accordance with the conditions of the theorem, except that now only those entries in C' which represent capacitor connections in categories I - VI in Table I need to satisfy the usual capacitor matrix realisability constraints; the remaining entries of C' may be positive, negative or zero. To obtain the capacitor matrix C" of the final equivalent network from C', all off diagonal terms which do not represent connections in any of the categories I-VI are equated to zero; then the on-diagonal terms are adjusted to yield

$$\sum_{j=1}^{n} C_{ij}'' = 0 \qquad \text{for each } i = 1,\ldots,n$$

These two methods for generating equivalent strays insensitive networks can be rigorously justified, and are, in fact, intimately related. The capacitor connections not listed in Table I are precisely those connections which can never contribute to network functioning, and hence may be used as phantom elements. Although the use of phantom elements is intuitively more appealing, the removal of constraints from the transformed capacitor matrix achieves the same goal more economically and more systematically. The result in either case is that strays insensitive networks whose capacitor matrices may have different ranks can now be related by equivalence transformations.

If an increase in the number of switches is acceptable, a far wider variety of equivalent strays insensitive networks can be generated by inserting redundant switch pairs at suitable nodes in the initial network. This technique enables networks whose capacitor matrices may have different dimensions to be related by equivalence transformations [3]. Sometimes the equivalence class can be still

further extended by using the fact that the inputs of operational amplifiers are virtual grounds to weaken condition (vi).

FORMULATING THE OPTIMISATION PROBLEM

The mathematical complexity of the optimisation problem means that a computational approach is essential in all but the simplest cases. A Fortran 77 program SCNAPT has therefore been developed which first determines equivalence and realisability conditions from the initial network data, and then optimises a chosen objective function subject to these constraints. It is necessary to specify at the outset whether the initial network is insensitive to strays, so that appropriate constraints and objective functions are utilised in the program.

It is evident from the theorem and from the discussion in the previous section that equivalence and realisability conditions can be expressed in terms of the entries of Q; the equivalence conditions are mostly linear equality constraints and the realisability conditions quadratic inequality constraints. Since the only variation in network components under the equivalence transformations is to capacitor elements, every objective function can be expressed as a function of the entries of C', and hence also, by (3), of the entries of Q; however, where the initial network is insensitive to strays, only those entries of C' should be involved which correspond to one or more of the types of capacitor connection listed in Table I.

Formulating the problem in terms of the entries of Q results in n^2 variables for a network with n nodes; this would be extravagant on computer time for even quite small networks, and for larger networks could jeopardise the optimisation process completely. The linear equality constraints, once these have been determined, are therefore used within the program to reduce the number of variables; the reduction achieved is normally around 75%. If there are still too many variables for optimisation to proceed efficiently, the user has the option of imposing additional constraints which will reduce both the number of variables and the constrained space over which the objective function is minimised.

Each point $\underline{x}$ in the constrained space corresponds to a specific network $N(\underline{x})$ which is equivalent to the initial network and has the same switching and amplifier arrangements. If $\underline{x}$ is an interior point, then $N(\underline{x})$ can be expected to have the most general equivalent topology, whereas, if $\underline{x}$ is a boundary point, $N(\underline{x})$ will have fewer capacitor elements, since at least one of the realisability constraints is active. The most general equivalent topology incorporates all the capacitor connections which occur in any of the other equivalent topologies; because of this property, an equivalent network N_G with the most general topology can be generated from the initial network by using individual capacitor elements (which are continuous on the whole constrained space) as objective functions and then maximising with SCNAPT. The remaining equivalent topologies can be obtained by successive minimisations of capacitor elements present in N_G.

Within each of the equivalent topologies, the capacitor elements normally take a continuous range of values; occasionally, however, the values are unique up to a scalar multiple in minimum element topologies. A sequential augmented Lagrangian technique is used in the optimisation subroutine in SCNAPT, the minimisation subproblems being solved by a quasi-Newton method; the objective functions should therefore be continuous, and preferably continuously differentiable, over a suitable constrained space. Many network parameters of interest, for example, normalised capacitor sum (total sum ÷ smallest capacitor) or spread (largest capacitor ÷ smallest capacitor) give rise to objective functions which are not continuous on all of the constrained space, but are continuous on regions corresponding to a fixed topology. Since regions corresponding to fixed topologies are usually simply connected, optimisation of such parameters can be carried out for each of the equivalent topologies in turn in order to obtain the global optimum.

Suppose a network N is given, and that, proceeding as above, equivalent networks $N_1, \ldots, N_\ell$ with distinct topologies $T_1, \ldots, T_\ell$ respectively have been obtained whose components are scaled so that no capacitor value is less than 1. For each $i = 1, \ldots, \ell$, let

$$C_1^i(\underline{q}), \ldots, C_{r_i}^i(\underline{q})$$

denote the capacitor elements present in T_i, where $\underline{q}$ is a vector in the space of reduced variables. To obtain an equivalent network with topology T_i and minimal spread $S_i(\underline{q}_i)$ using SCNAPT, it is required to

$$\text{minimise } \{F_i(\underline{q}) = \max\{C_1^i(\underline{q}), \ldots, C_{r_i}^i(\underline{q})\}\}$$

subject to equivalence and realisability constraints, and, additionally,

$$C_1^i(\underline{q}), \ldots, C_{r_i}^i(\underline{q}) \geq 1$$

all other possible capacitor connections being constrained to zero. Since the value of the smallest capacitor is forced down to 1 by the minimisation process,

$$S_i(\underline{q}_i) = \min_{\underline{q}} F_i(\underline{q})$$

subject to the above constraints, and the global minimum is

$$S_{min} = \min_i S_i(\underline{q}_i)$$

A similar approach is adopted to minimise normalised capacitor sum; note that this technique avoids the problem of identifying the smallest capacitors. Sometimes the number of equivalent topologies is so large that it is only practicable to consider a sample of the possibilities.

A number of objective functions have already been incorporated into SCNAPT, both for the purpsoe of identifying the equivalent topologies, and in order to improve specific performance factors such as capacitor sum and spread. There is no difficulty in principle in incorporating further objective functions, for example, weighted objective functions which reflect those parameters considered to be most important, provided they can be simply evaluated within the program, and are continuous on identifiable simply connected regions of the constrained space. Additional range constraints may be used to prevent improvements to some parameters from resulting in unacceptable deterioration in others.

APPLICATION TO PRACTICAL NETWORKS

Some results of applying equivalence transformations to 2-phase strays insensitive filter sections are shown in Figs. 1-3. In each case the governing equivalence equations are given, $\{C_i\}$ and $\{C'_i\}$ being the sets of capacitors in the initial and resulting equivalent networks respectively; note that connections not present in the initial networks are marked with a broken line.

The range and extent of improvements to network parameters which are possible in a given case depend both on the topological structure and on the component values of the initial network. In the first order section, no improvements to capacitor sum and spread are possible within the initial topology, unless a scaling factor is used; however, in second and higher order filters there are more degrees of freedom and significant reductions can usually be achieved both within the initial topology and in many of the more general equivalent topologies. If scaled equivalence is acceptable (this may be true where a filter is constructed from cascaded sections, for example), then there is an additional degree of freedom which can be used to optimise performance.

In some of the equivalent topologies, switches are effectively lost because they become redundant; this occurs in the first order section if $C'_3 = C'_5 = 0$, since no capacitors are connected to node 4, and in the low pass filter where many switches are shared in the equivalent networks in Fig.3b. This process can be reversed by the use of redundant switch pairs [3].

CONCLUSION

The formulation of equivalence transformations as congruence transformations of the capacitor matrix enables optimisation of SC network performance factors to be achieved using computational methods. In addition to the 2-phase strays insensitive networks considered in this paper, equivalence transformations may be applied to passive, strays sensitive and multiphase networks, and, indeed, the program SCNAPT has been designed to cope with all of these cases. Although in principle applicable to networks of arbitrary size, the practical implementation of the theory is dependent both on the existence of satisfactory optimisation algorithms and on the available hardware; however, reasonable results are certainly achievable with small and medium sized networks.

ACKNOWLEDGEMENT

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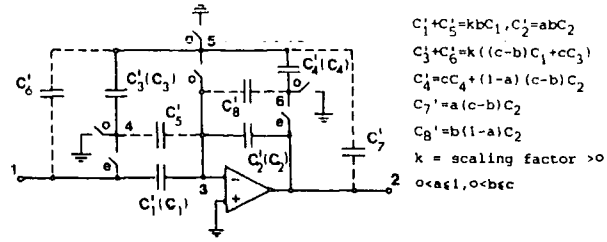
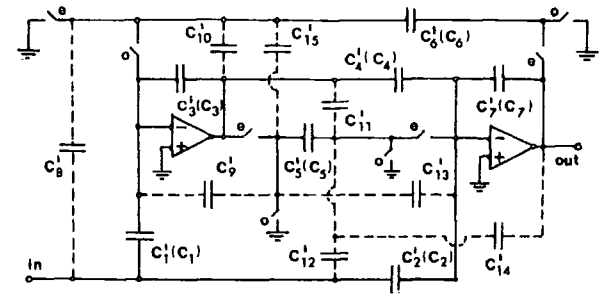
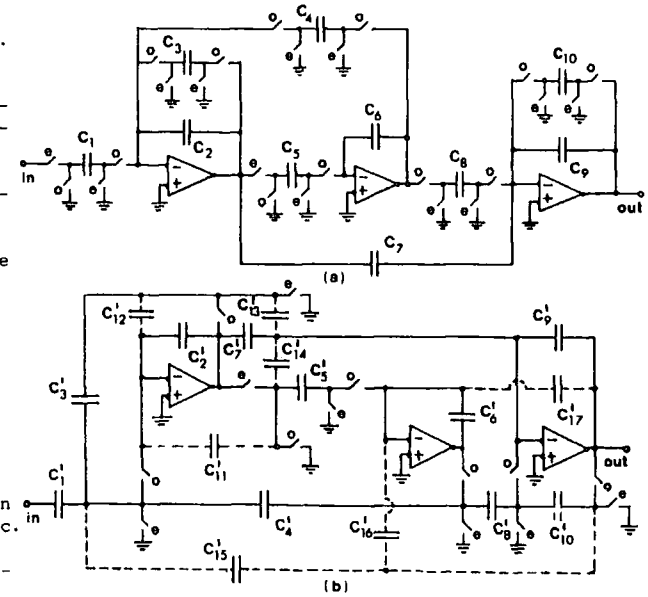


FIG.1: FIRST ORDER SECTION



$C'_1=kaC_1, C'_2=keC_2, C'_3=acC_3, C'_4=ceC_4, C'_5=fdC_5+ihC_4, C'_6=bC_6, C'_7=eC_7$
$C'_8=kgC_1, C'_9=ahC_3, C'_{10}=cgC_3, C'_{11}=ciC_4, C'_{12}=kiC_2, C'_{13}=ehC_4, C'_{14}=iC_7$
$C'_{15}=ghC_3$; $g=b-a, h=d-c, i=f-e, b\geq a>0, d\geq c>0, f\geq e>0$

FIG.2: SECOND ORDER BANDPASS FILTER



$C'_1=kaC_1, C'_2+C'_{11}=abC_2, C'_3=abC_3, C'_4=adC_4, C'_5=bcC_5, C'_6=cdC_6$
$C'_7+C'_{13}=beC_7, C'_8=deC_8, C'_9=eC_9, C'_{10}=eC_{10}, (f+g)C'_8, C'_{17}=C'_{12}$
$C'_{13}=C'_{14}=C'_{15}=(f+g)C'_4, C'_{16}=fC'_6, C'_{17}=gC'_6$; $a,b,c,d,e>0, f,g\geq0$

FIG.3: THIRD ORDER LOWPASS FILTER

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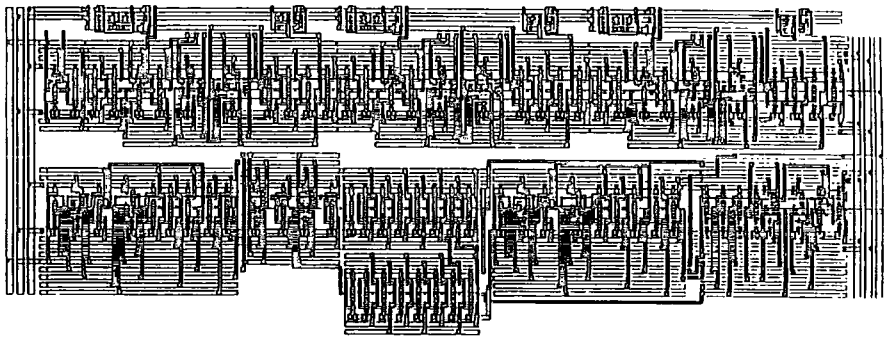

Fig. 4. Layout of a testable serial–parallel multiplier.

in the logic block, the output PZ should be low (connected to V_{ss}) in the case of n-logic and high (connected to V_{dd}) in the case of p-logic.

In the case of static CMOS, the presence of a stuck-on transistor may result in both p- and n-networks being conducting. The output voltage thus depends on the resistance of the p- and n-network and hence increases the complexity of fault detection. Such cases do not happen in NORA CMOS because the p- and the n-network cannot be both conducting at the same time even if stuck-on occurs in the logic block. This is because the clock (ϕ or $\bar{\phi}$) is applied to both the pMOS and the nMOS transistor that are in series with the logic block and thus prevent both transistors to be conducting at the same time. Hence the output voltage is not dependent on the resistance of the networks and, therefore, it is easier to detect stuck-on faults. The procedure for testing stuck-on is similar to those described for other faults. For the circuit with n-logic block shown in Fig. 2, TEST2 is charged high prior to the evaluation phase. A low TEST2 during the evaluation phase with appropriate test vector inputs TV1 applied prior to, and kept constant at the evaluation phase indicates a stuck-on condition. Similarly, for the circuit with p-logic block as shown in Fig. 3, a low TEST4 during the evaluation phase with appropriate test vector inputs TV2 indicates a stuck-on condition. It can again be seen that the test for stuck-on fault and the test for stuck-at fault are overlapped to some extent, because a device stuck-on could result in the output to be either stuck-at-one or stuck-at-zero.

V. Area and Time Considerations

The additional circuits (shown in Figs. 2 and 3) used to detect stuck-at, stuck-open, and stuck-on faults occupy only a small amount of area overhead and is independent of the complexity of the gate to be tested. The amount of contact cuts for the layout is also very small. This is favorable because contact cuts occupy large areas and degrate reliability of the circuit. However, by connecting many nMOS devices or pMOS devices in series may reduce the speed of operation for testing. This disadvantage is not so important because the clock can be slowed down for testing. Moreover, buffers can be inserted between the devices to reduce the delay.

VI. Applications and Conclusions

This testability enhancement technique is employed in implementing a testable serial-parallel multiplier. A prototype of multiplier with 4-bit multiplicand and 3-bit multiplier has been implemented using 4-μm CMOS (NORA) technology, Fig. 4, the total layout area is found to be 3.89 mm^2. The multiplier takes around 11 ns to produce the product and the error signal. The additional cost for the error detection circuitry is only in the range of 10 percent of the total area.

The testability enhancement technique is useful especially where the internal nodes of the system are difficult to test. It can also be used for probe testing of wafer. In conclusion, the proposed error detection circuit, based on the structure, properties, and operations of NORA CMOS, can detect stuck-at, stuck-open, and stuck-on faults. It occupies only a small amount of area overhead and is independent of the complexity of the cell to be tested.

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The LUD Approach to Switched-Capacitor Filter Design

LI PING AND J. I. SEWELL

***Abstract*—A new design method for switched-capacitor filters (SCF) is presented. It is based upon an LU matrix decomposition technique and has the distinct advantage of producing SC filter realizations containing no delay free loops. These are formed traditionally by capacitors and op-amps in leapfrog realizations. It is demonstrated that this feature should render reduced dependence of the filter response to nonideal effects such as finite amplifier GB and switch resistance. Results from realistic leapfrog and LUD SC filter realizations confirm this.**

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Introduction

Passive terminated LC ladder simulations are popular techniques in switched-capacitor filter (SCF) design, as they retain the low sensitivities of the prototype passive ladders. Among various simulation methods the leapfrog-type SCF has received most attention because of its strays insensitive property [1]–[3].

There are two kinds of transformations commonly adopted in designing leapfrog SCF's: LDI and bilinear transformations [1]. LDI SCF's have the problem of strictly unrealizable terminations. Some approximation must be made and this limits their applications. Bilinear leapfrog SCF's using LDI integrators are more favorable. However, there is a major drawback for the bilinear leapfrog SCF (and, also, for LDI leapfrog SCF when the transfer function has finite transmission zeros) that there always exist delay-free loops formed by capacitors and op-amps. This increases the op-amps settling times. As a result, some considerable distortion of the transfer function may be caused by the finite GB product of op-amps and on-resistance of switches [3], [4], [6]. Incidentally the existence of delay-free loops makes digital circuit realization difficult [7]–[9].

In this paper, the matrix form derivation of leapfrog SCF is viewed first. Then a new structure of SCF based on LU decomposition is presented and the corresponding digital circuit realization is briefly discussed. No delay-free loops exist in these circuits. Examples are given to show that the new approach produces circuits with better performances than leapfrog-type circuits when nonideal effects of op-amps and MOS switches are considered.

Derivation of Leapfrog SCF in Matrix Form

The first bilinear leapfrog SCF's were sensitive to stray capacitance. A further development [1] allowed application of the bilinear transformation whilst using modified LDI integrators which are completely strays insensitive. We shall derive this kind of SCF as the preliminary to the new approach.

Starting from a passive RLC prototype network which can be described by nodal equation:

$$\left(sC+\frac{1}{s}\Gamma+G\right)V=J \tag{1}$$

where C, Γ, and G stand for the contribution of capacitors, inductors, and conductors respectively. Performing the bilinear transformation on (1) we have (when $T=2$ for simplicity)

$$\left\{\frac{1-z^{-1}}{1+z^{-1}}C+\frac{1+z^{-1}}{1-z^{-1}}\Gamma+G\right\}V=J. \tag{2}$$

Equation (2) is equivalent to

$$AV=\left\{-\frac{4z^{-1}}{(1-z^{-1})^2}\Gamma-\frac{2z^{-1}}{1-z^{-1}}G\right\}V+\frac{1+z^{-1}}{1-z^{-1}}J \tag{3a}$$

with

$$A=C+\Gamma+G. \tag{3b}$$

The inverse inductance matrix Γ in (3) can be decomposed into

$$\Gamma=A_L D_L A_L^T \tag{4}$$

where A_L is the incidence matrix of the network obtained by removing all elements except inductors, and $D_L=\mathrm{diag}(1/L_i)$. Let

$$A=D_a+B \tag{5}$$

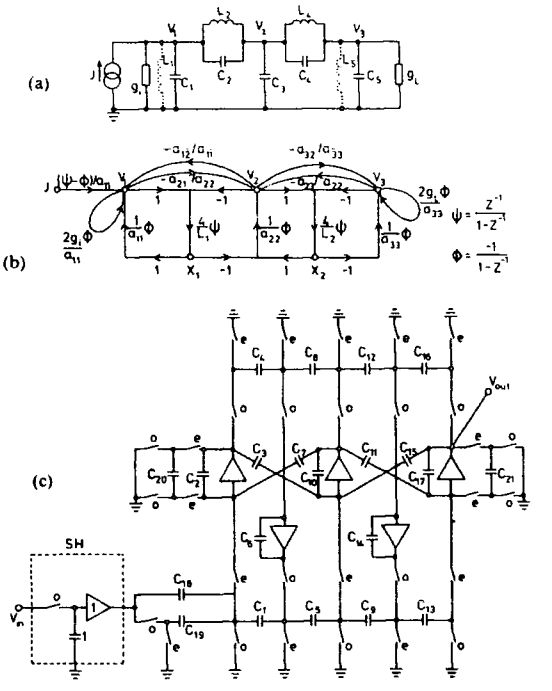


Fig. 1. (a) A terminated LC ladder passive prototype. (b) Leapfrog-type signal-flow-graph simulation of the circuit in (a). (c) Leapfrog SCF simulation of the circuit in (a).

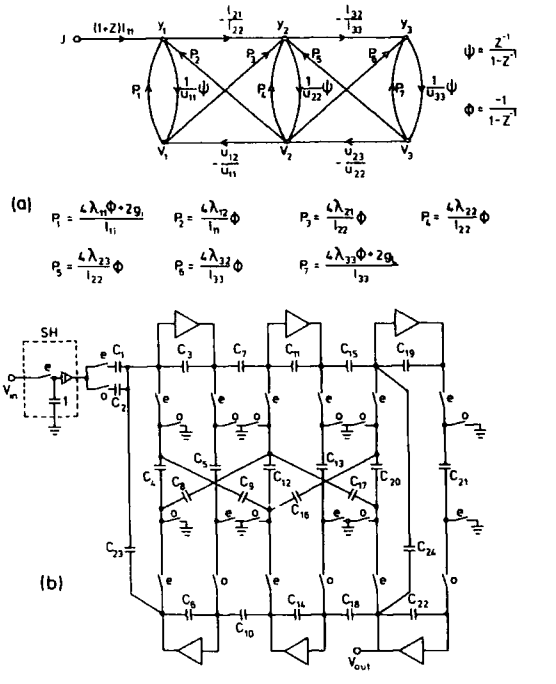


Fig. 2. (a) LUD type signal-flow-graph simulation of the circuit in Fig. 1(a). (b) LUD SCF simulation of the circuit in Fig. 1(a).

TABLE I
DESIGN DATA FOR THE SC FILTER EXAMPLES OF FIG. 1 AND FIG. 2

Normalized Data for the LC Ladder of Fig.(1a)

1) Fifth order Lowpass Elliptic Case

passband edge	1.			stopband edge	1.555723827				
passband ripple	0.0436 dB			stopband ripple	41.9 dB				
G1 = GL = 1	L1	0	C1	0.867058	L2	1.223976	C2	0.137493	
C3	1.511948	L4	0.940651	C4	0.406594	C5	0.669168	L5	0

2) Sixth order Bandpass Elliptic Case

upper passband edge	1.034			lower passbad edge	0.967				
upper stopband edge	1.173			lower stopband edge	0.895				
passband ripple	< 0.25 dB			stopband attenuation	> 34 dB				
G1 = G2 = 1	C3 = 0		C1	1.6310	L1	0.014807	C2	0.38030	
L2	0.088285	C3	0.27356	L3	0.063504	C4	1.6310	L4	0.014807

Component Values for the Leapfrog SCF of Fig.(1c)

passband edge	3.225 kHz		stopband edge	4.800 kHz			
C1	4.3117021	C2	3.8187507	C3	1.0000000	C4	1.1283536
C5	3.8212329	C6	2.7566618	C7	1.0000000	C8	1.0000000
C9	3.3194505	C10	8.8680304	C11	1.3122242	C12	1.6543911
C13	2.1279985	C14	3.0446682	C15	1.2372708	C16	1.0000000
C17	1.3110067	C18	1.7601345	C19	3.5202689	C20	3.2856668
C21	1.0000000						
number of capacitors	21		number of switches	30			
number of op amps	5		total capacitance	52.2778			
capacitance spread	8.8680		clock frequency	32 kHz			

Component Values for the LUD SCF of Fig.(2b)

1) Fifth order Lowpass Elliptic Case

passband edge	3.325 kHz		stopband edge	4.8 kHz			
C1	1.125332	C2	1.125332	C3	3.664828	C4	1.128354
C5	5.732167	C6	7.104417	C7	1.000000	C8	1.938541
C9	1.000000	C10	1.000000	C11	7.464650	C12	3.953523
C13	4.867762	C14	7.053555	C15	1.295663	C16	1.654369
C17	1.351268	C18	1.000000	C19	1.905143	C20	1.000000
C21	1.000000	C22	1.595858	C23	2.100672	C24	1.430766
number of capacitors	24		number of switches	26			
number of op amps	6		total capacitance	62.4922			
capacitance spread	7.4646		clock frequency	32 kHz			

2) Sixth order Bandpass Elliptic Case

upper passband edge	1 kHz		lower passband edge	0.9 kHz			
upper stopband edge	1.08 kHz		lower stopband edge	0.829 kHz			
C1	1.000000	C2	1.000000	C3	23.35666	C4	13.72274
C5	2.353740	C6	2.807107	C7	2.180592	C8	1.030186
C9	3.930910	C10	1.000000	C11	7.101668	C12	4.910849
C13	4.977363	C14	5.842078	C15	6.643089	C16	5.464835
C17	1.000000	C18	1.000000	C19	12.62665	C20	10.11870
C21	1.000000	C22	1.375713	C23	1.432187	C24	1.000000
number of capacitors	24		number of switches	26			
number of op amps	6		total capacitance	116.8751			
capacitance spread	23.3567		clock frequency	8 kHz			

where D_a is diagonal and all diagonal elements in B are zeros. Then (3) can be written as

$$D_a V = -BV - \frac{2z^{-1}}{1-z^{-1}} GV - \frac{1}{1-z^{-1}} A_L X + \frac{1+z^{-1}}{1-z^{-1}} J \quad (6a)$$

$$X = +\frac{4z^{-1}}{1-z^{-1}} D_L A_L^T V. \quad (6b)$$

These equations can be represented in signal-flow-graph form. Fig. 1 gives a terminated passive LC ladder with its corresponding signal-flow-graph in the discrete domain and the SCF implementation. Notice branches representing the term $-BV$ in (6a) form two delay-free loops.

LU DECOMPOSITION (LUD)-TYPE SCF

In the last section it was shown that a leapfrog-type signal-flow-graph is formed by decomposing matrix Γ and realizing all nondiagonal elements in A by feedthrough branches. If A is of upper triangle or lower triangle form then these branches will not form delay-free loops. Unfortunately, A is neither of these cases for a practical ladder prototype.

One way to solve this problem is to decompose A into LU form. Let

$$A = \mathrm{LU} \quad (7a)$$

$$Y = \frac{1-z^{-1}}{z^{-1}} UV. \quad (7b)$$

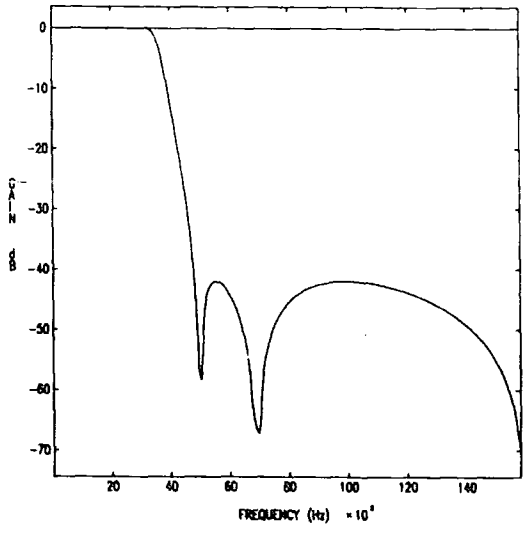
From (3) and (7) we have

$$LY = \left(-\frac{4}{1-z^{-1}} \Gamma - 2G \right) V + (1+z) J \quad (8a)$$

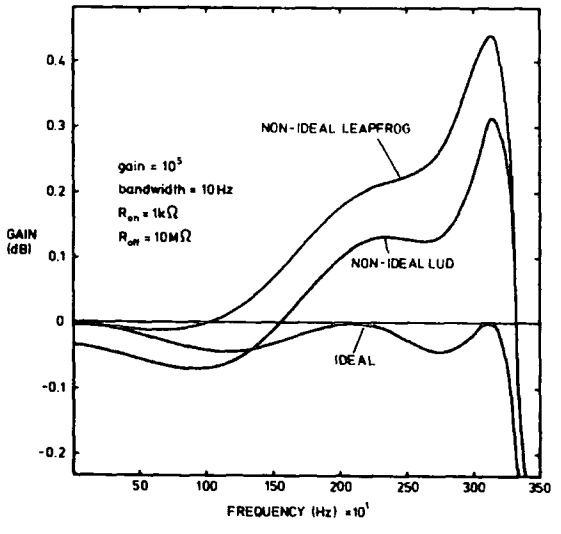
$$UV = +\frac{z^{-1}}{1-z^{-1}} Y. \quad (8b)$$

A signal-flow-graph can be drawn to represent (8); Fig. 2(a) shows one for the prototype given in Fig. 1(a).

The SCF implementation is shown in Fig. 2(b). Normally for a prototype network with n nodes, $2n$ op-amps are required. It seems that for a prototype having more loops than nodes, we can start from a loop equation instead of the nodal equation in (1). In more general cases, a hybrid description of the prototype network can be used.



(a)



(b)

Fig. 3. (a) Response of ideal fifth-order low-pass elliptic filter (LUD). (b) Comparison of filter passband characteristics with typical amplifier and switch parameters, (sinc not included).

Fig. 2(a) can be realized directly by digital circuits. In this case the number of multiplication operations must be taken into consideration. So we can decompose A into (note A is always symmetrical)

$$A = L_n D_n L_n^T \tag{9}$$

where diagonal entries of L_n are all 1 and D_n is a diagonal matrix. Thereby (8) can be rewritten as

$$L_n D_n Y = \left(-\frac{4}{1-z^{-1}} \Gamma - 2G \right) V + (1+z) J \tag{10a}$$

$$L_n^T V = + \frac{z^{-1}}{1-z^{-1}} Y. \tag{10b}$$

Approximately $3n$ (n is the number of the nodes) coefficients need to be stored and $4n$ multiplications performed in each period. It can be shown that this kind of digital filter is highly insensitive to finite length of coefficients.

Examples

A program named SCNDP (SC network design program) has been developed using LUD as well as leapfrog approaches. This is used in conjunction with analysis programs SCNAPIF and SCNAPNIF [5].

Some typical filter realizations are shown in Figs. 1 and 2. The extra components in the passive prototype are required for the bandpass realization. The calculated capacitance values are listed in Table I. In the LUD realization it can be seen that one extra amplifier is only required for low-pass filters, the bandpass case utilizes the same circuit topology with changed component values and is canonic in number of amplifiers. A leapfrog bandpass realization would require a changed topology and a simple comparison does not follow. The one extra amplifier in the low-pass case will require more chip area, but this difference reduces in significance as the filter order increases. The op-amp's outputs in all circuits are adjusted to give the same level as the input. No attention has been given to minimizing the capacitance spread.

Fig. 3(a) shows the ideal filter response. Fig. 3(b) gives a comparison between ideal performance and non-ideal responses in the passband for LUD and leapfrog realizations with typical amplifier and switch parameters. The LUD realization demonstrates some improvement in performance over the equivalent leapfrog circuit for typical parameter values.

Preliminary sensitivity studies indicate that the LUD realization possesses similar properties to the leapfrog structure, except at $\omega = 0$ in the low-pass case where a drop in magnitude response is observed. This is a subject of further work.

Conclusion

A new kind of structure for SC filters is presented. Results obtained show that the proposed circuits demonstrate better performance than leapfrog circuits in certain non-ideal cases. It can be observed also that the particular ranges of non-ideal parameters pose serious influence on both circuits. Work is being undertaken to formally eliminate these effects in the design procedure.

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PAPER 37

Filter realisation by passive network simulation

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Indexing terms: Filters and filtering, Simulation, Digital circuits

Abstract: General simulation methods of passive networks are investigated. A new simulation approach based on LU matrix decomposition is presented. This approach can be used to design active-*RC*, switched-capacitor and digital networks. The resulting system demonstrates very low sensitivities with respect to component values. New digital realisations, in particular, reveal structures of low complexity, high speed of operation and low cost of implementation.

1 Introduction

A wide variety of design methods are available for digital filter circuits. Direct methods, including cascade biquads and follow-the-leader (FL), have the advantage of simplicity but the penalty of high sensitivity [1]. The effort devoted to low-sensitivity structures has achieved notable success. In particular, wave and lattice approaches have developed into a distinguished family [2, 3]. Modification of the leapfrog method drawn from active-*RC* circuits has also attracted much attention [4–6]. An interesting recent development is the introduction of the lossless bounded real (LBR) concept with several promising structures emerging [7–9]. The remaining problem with these low-sensitivity circuit designs is that they are generally complicated, suffering from high hardware cost or limitation of operation speed, especially for high-order realisations.

This paper discusses a new approach based on passive ladder simulation in matrix form. The LU matrix decomposition is employed to derive new filter structures. Besides retaining the low-sensitivity of the prototype, the new method also has the important property of relatively low hardware cost and high operation speed. Some strategies are adopted to obtain structures most suitable for parallel processing. Because the design method is unified through matrix manipulations, the resulting circuit structures are regular, allowing easy programmable implementation.

This method has been previously proposed for switched-capacitor (SC) realisation [10, 11]. For simplicity of comprehension, the application to active *RC* circuit design is outlined first in this paper, and the development of the digital case is then discussed in detail. Examples are given comparing the performance of the new design with those of other methods.

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Discussions are restricted to the lowpass case. The principles are the same for other types of *RC* circuits and also for bandpass digital design [10, 11]. For the highpass digital case a well known transformation of $z^{-1} \rightarrow -z^{-1}$ can be used. For the bandstop digital case the technique adopted is somewhat different and will be presented elsewhere.

2 Matrix form simulation of passive ladders

Leapfrog structures have been very popular in active-*RC* and SC filter design and are conventionally explained as methods simulating the voltage/current relationships in *RLC* ladders [12–14]. The structure is derived according to these voltage/current relations, which can be a tedious procedure. A more systematic derivation is now presented as the preliminary to further developments in succeeding sections.

The procedure starts with a typical passive *RLC* prototype network, Fig. 1*a*, which can be described by the nodal equation

$$(sC + s^{-1}\Gamma + G)V = J \tag{1}$$

where C, Γ and G represent the contributions of capacitors, inductors and conductors, respectively. For convenience V is defined by $[v_1, -v_2, v_3, -v_4, \ldots]^T$ to make all the entries of C, Γ and G positive. Notice the inverse inductance matrix Γ in eqn. 1 can be decomposed according to network topology into

$$\Gamma = A_L D_L A_L^T \tag{2a}$$

where A_L is the incidence matrix of the inductor subnetwork and $D_L = \text{diag}\,(L_1^{-1}, L_2^{-1}, \ldots)$.

Define a new set of variables

$$X = s^{-1} D_L^T A_L V \tag{2b}$$

with

$$(sC + G)V = -A_L X + J \tag{2c}$$

For an allpole lowpass filter (Fig. 1*a*) C is diagonal and $(sC + G)^{-1} = \text{diag}\,[(sc_1 + g_{in})^{-1}, (sc_2)^{-1}, (sc_3)^{-1}, \ldots, (sc_n + g_L)^{-1}]$. X and V can be expressed in a recursive form

$$\begin{bmatrix} V \\ X \end{bmatrix} = \begin{bmatrix} 0 & -(sC + G)^{-1} A_L \\ s^{-1} D_L A_L^T & 0 \end{bmatrix} \begin{bmatrix} V \\ X \end{bmatrix} + \begin{bmatrix} (sc_1 + g_{in})^{-1} J \\ 0 \end{bmatrix} \tag{3}$$

A signal flow graph (SFG), Fig. 1*b* can be drawn to represent eqn. 3 and the corresponding active-*RC* implementation follows directly (Fig. 1*c*). The output of every op-amp represents a variable either in V or in X. For every nonzero entry in the coefficient matrix of eqn. 3 there is a corresponding connection between two op-

amps. For circuits with series capacitors (Fig. 2*a*) matrix C will have off-diagonal elements and this would appear

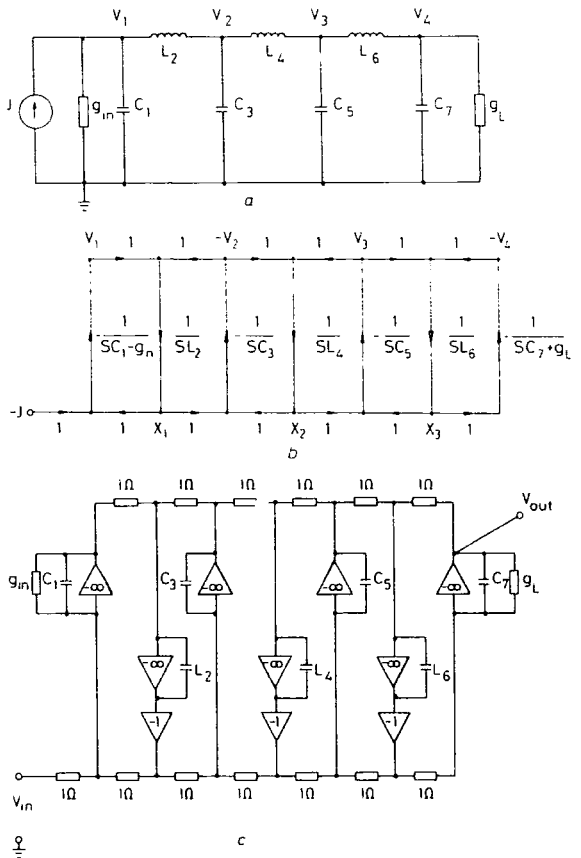


Fig. 1 *7th-order Chebyschev lowpass ladder*

a Circuit diagram
$g_{in} = 1S$ $g_L = 1S$
$c_1 = 3.585F$ $L_2 = 4.330H$
$c_3 = 6.370F$ $L_4 = 4.789H$
$c_5 = 6.370F$ $L_6 = 4.330H$
$c_7 = 3.585F$
b Leap-frog type SFG simulation of the passive circuit
c Corresponding active-*RC* realisation (normalised)

to make the matrix inversion $(sC + G)^{-1}$ in eqn. 3 somewhat more complicated. In this case eqn. 3 can be rewritten as

$$\begin{bmatrix} V \\ X \end{bmatrix} = \begin{bmatrix} -(sC_{diag} + G)^{-1}sC_{offd} & -(sC_{diag} + G)^{-1}A_L \\ s^{-1}D_L A_L^T & 0 \end{bmatrix} \times \begin{bmatrix} V \\ X \end{bmatrix} + \begin{bmatrix} (sc_{11} + g_{in})^{-1}J \\ 0 \end{bmatrix} \quad (4)$$

where $C = C_{diag} + C_{offd}$. $C_{diag} = \{c_{ii}\}$ and $C_{offd} = \{c_{ij} | i \neq j\}$ contain the diagonal and off-diagonal elements of C, respectively. Now the SFG and the corresponding circuit implementation can be obtained from eqn. 4 (see Figs. 2*b*, *c*). Branches representing the term $-(sC_{diag} + G)^{-1}sC_{offd}$ in eqn. 4 form three feed-through loops, shown in the upper part of Fig. 2*b*. These feed-through loops, which are realised by cross-coupled capacitors, increase the high-frequency noise levels; as can be seen from Fig. 2*c*, the high frequency noise created by each op-amp will be fed directly via the cross-coupled capacitors to the output. They also extend the settling time of op-amps in SC realisations and render digital realisation difficult. In the next Section, a new simulation structure is suggested to overcome this problem.

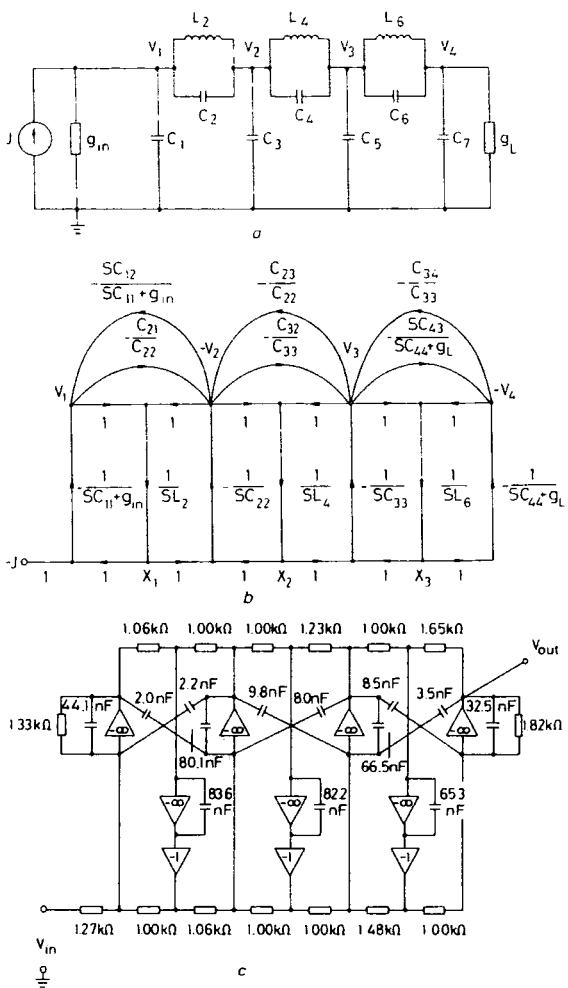


Fig. 2 *7th-order elliptic lowpass ladder*

a Circuit diagram
$g_{in} = 1S$ $g_L = 1S$
$c_1 = 3.450F$ $c_2 = 0.1717F$ $L_2 = 4.137H$
$c_3 = 5.601F$ $c_4 = 0.8016F$ $L_4 = 3.828H$
$c_5 = 5.328F$ $c_6 = 0.5722F$ $L_6 = 3.659H$
$c_7 = 3.082F$
b Leap-frog type SFG simulation of the passive circuit
c Corresponding active-*RC* realisation (scaled for maximum dynamic range and denormalised, 3.4 kHz)

3 The LU decomposition simulation method

The elimination of feed-through loops is possible. Let matrix C in eqn. 1 be decomposed into LU form [15]

$$C = LU \quad (5a)$$

As matrix C in the nodal equation (eqn. 1) is always symmetric for passive networks, eqn. 5*a* can be expressed in symmetric form with D being a diagonal matrix.

$$C = U^T DU \quad (5b)$$

Choose $L = U^T D$ and introduce a new set of variables

$$X = sDUV \quad (5c)$$

From eqns. 1 and 5

$$U^T X = -s^{-1}\Gamma V - GV + J \quad (6a)$$

$$DUV = s^{-1}X \tag{6b}$$

To show how the system of eqns. 6 can be represented by a SFG form, choose U with all the diagonal entries being 1 and separate U into diagonal and off-diagonal terms:

$$U = I + U_{offd} \tag{7}$$

From eqns. 6 and 7 a recursive representation of V and X is obtained:

$$\begin{bmatrix} X \\ V \end{bmatrix} = \begin{bmatrix} -U_{offd}^T & -(s^{-1}\Gamma + G) \\ s^{-1}D^{-1} & -U_{offd} \end{bmatrix} \begin{bmatrix} X \\ V \end{bmatrix} + \begin{bmatrix} J \\ 0 \end{bmatrix} \tag{8}$$

Then the so-called LUD-type SFG and corresponding active-RC implementation can be obtained according to eqn. 8 (see Fig. 3). This circuit configuration with altered component values can also realise an 8th order bandpass filter. No feed-through loop exists in the circuit. Only in the lowpass case is one extra op-amp required when compared with the leapfrog approach. In other cases the number of amplifiers can be made canonical.

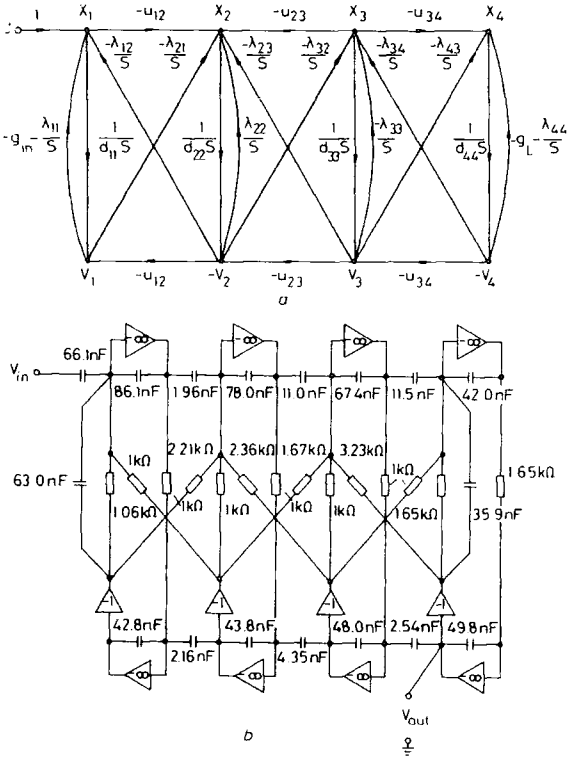


Fig. 3 *LUD type simulation of circuit in Fig. 2a*

a Diagram

b Corresponding active-RC realisation (scaled for maximum dynamic and denormalised, 3.4 kHz)

For a prototype with more loops than nodes, it is possible to start with a loop description of the network instead of eqn. 1. In more general cases, hybrid descriptions of the prototype can be used.

4 The LUD and leapfrog (LL) approach for discrete systems

It is now logical to examine the application of this theory to discrete implementations. To afford some means of comparison with existing approaches, Fig. 4 shows cascaded biquad and wave digital realisations of a standard elliptic filter (Fig. 2*a*). Both the biquad and wave filters are canonical in terms of the number of multipliers whereas the wave digital filter requires a higher number of additions and delays and offers a slower speed of operation because multiplications must be performed in some hierarchical sequence [1, 9]. This Section will develop new structures which offer some noteworthy improvements.

4.1 Standard LL discrete system

Perform the bilinear transform on eqn. 1 (let sampling period $T = 2$ s for simplicity)

$$\left(\frac{1 - z^{-1}}{1 + z^{-1}}C + \frac{1 + z^{-1}}{1 - z^{-1}}\Gamma + G\right)V = J \tag{9}$$

To produce a system without delay-free loops, the following manipulations are required. Eqn. 9 is equivalent to

$$\left(A + \frac{4z^{-1}}{(1 - z^{-1})^2}\Gamma + \frac{2z^{-1}}{1 - z^{-1}}G\right)V = \frac{1 + z^{-1}}{1 - z^{-1}}J \tag{10a}$$

with

$$A = C + \Gamma + G \tag{10b}$$

For simplicity rewrite eqn. 10*a* as

$$(A + \Psi\Phi 4\Gamma + \Psi 2G)V = \Psi(1 + z)J \tag{11}$$

with

$$\Psi = z^{-1}/(1 - z^{-1}) \tag{12a}$$

$$\Phi = 1/(1 - z^{-1}) \tag{12b}$$

It is interesting that Ψ and Φ constitute a pair of LDI integrators [4]. The relationship between bilinear and 'exact' LDI transformed systems is discussed elsewhere [11]. As matrix A is always symmetric, it can also be decomposed into the form

$$A = U^T D U \tag{13}$$

where D is used in the same way as in eqn. 5 and let $U = I + U_{offd}$. This leads to the discrete LUD system

$$\begin{bmatrix} X \\ V \end{bmatrix} = \begin{bmatrix} -U_{offd}^T & -(\Phi 4\Gamma + 2G) \\ \Psi D^{-1} & -U_{offd} \end{bmatrix} \begin{bmatrix} X \\ V \end{bmatrix} + \begin{bmatrix} (1 + z)J \\ 0 \end{bmatrix} \tag{14}$$

The corresponding SFG is shown in Fig. 5, and is suitable for SC realisation [10]. The realisation of input function $(1 + z)$ can be accomplished by multiplying by z^{-1} giving $(1 + z^{-1})$, but introducing a delay of one period.

For digital realisation Γ can be decomposed as in the leapfrog method, $\Gamma = A_L D_L A_L^T$, in this way the number of multiplications is reduced. The corresponding standard LL (LUD-leapfrog) can be realised directly by the circuit shown in Fig. 6*a*.

Now it is essential to take into consideration some factors related to the operation speed. Let

m = order of the filter (15*a*)

n = number of nodes of the prototype (15*b*)

T_s = sampling period (15*c*)

T_m = time for one multiplication operation (15*d*)

T_a = time for one addition operation (15*e*)

For an ordinary odd-order lowpass RLC ladder, $m = 2n - 1$. Examining eqns. 15 and Fig. 6*a* carefully, it

can be seen that when the transfer factors $\{c_i\}$ of the horizontal branches in Fig. 6*a* are general numbers, the operation speed is limited by

$$T_s \geqslant \frac{m+5}{2} \cdot T_a + \frac{m+1}{2} \cdot T_m \tag{16}$$

because in every period, additions and multiplications along horizontal branches must be performed serially, for the upper line from left to right and for the lower line from right to left. Since $T_m \gg T_a$, the limit is dominated by the multiplication time. In the following we shall show some strategies to improve this limitation on operation speed.

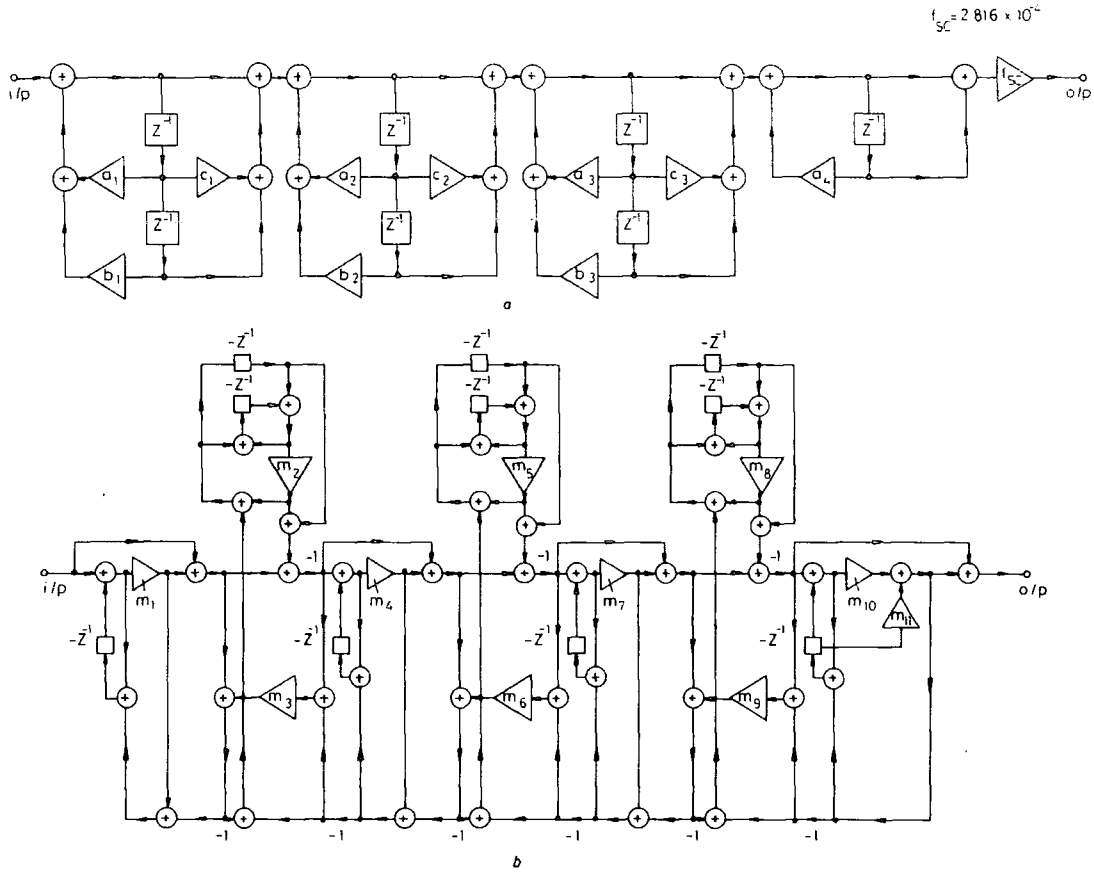


Fig. 4 *Realisations of the elliptic filter*

a Cascade biquadratic digital realisation

$a_1 = 1.498$ $b_1 = 0.6331$ $c_1 = 0.3442$
$a_2 = 1.488$ $b_2 = 0.7751$ $c_2 = -1.013$
$a_3 = 1.522$ $b_3 = 0.9252$ $c_3 = -0.7097$
$a_4 = 0.7541$

b Wave digital realisation

$m_1 = -0.7748$ $m_5 = -0.7532$ $m_9 = 0.1203$
$m_2 = -0.4140$ $m_6 = 0.1511$ $m_{10} = -0.6899$
$m_3 = 0.08522$ $m_7 = -0.8550$ $m_{11} = -0.5811$
$m_4 = -0.9366$ $m_8 = -0.6774$

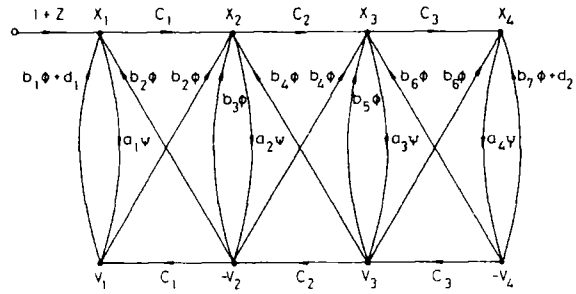


Fig. 5 *LUD-type SFG for the elliptic filter*

$a_1 = 0.2056$ $b_1 = -0.9668$ $c_1 = -0.0850$
$a_2 = 0.1420$ $b_2 = -0.9668$ $c_2 = -0.1509$
$a_3 = 0.1412$ $b_3 = -2.011$ $c_3 = -0.1201$
$a_4 = 0.2070$ $b_4 = -1.045$
$b_5 = -2.138$ $d_1 = -2$
$b_6 = -1.093$ $d_2 = -2$
$b_7 = -1.093$

4.2 Modified LL system

The limitation given by eqn. 16 can be reduced by scaling all nonzero elements in $\boldsymbol{U}$ to the nearest powers of 2, as the operation required to multiply a number by 2^{-k} is simply to shift it by k bits. It is also possible to scale all nonzero entries in $\boldsymbol{U}$ to ± 1s, but this results in a very large coefficient spread, which is undesirable. The scaling procedure can be performed in terms of matrix transformations. Let $\boldsymbol{S}$ be a diagonal constant matrix, pre- and post-multiply the matrices in eqn. 11 by $\boldsymbol{S}$. Let

$$\boldsymbol{A}_s = \boldsymbol{SAS} \qquad \boldsymbol{B}_s = \boldsymbol{SA}_L 4\boldsymbol{D}_L \boldsymbol{A}_L^T \boldsymbol{S} \qquad \boldsymbol{G}_s = \boldsymbol{S}2\boldsymbol{GS}$$
$$\boldsymbol{V}_s = \boldsymbol{S}^{-1}\boldsymbol{V} \qquad \boldsymbol{J}_s = \boldsymbol{SJ} \tag{17}$$

A new system is obtained with a transfer function differing from that of eqn. 11 only by a constant.

$$(\boldsymbol{A}_s + \Psi\Phi\boldsymbol{B}_s + \Psi\boldsymbol{G}_s)\boldsymbol{V}_s = \Psi(1+z)\boldsymbol{J}_s \tag{18}$$

Scaling is carried out so that $\boldsymbol{A}_s$ will decompose into

$$\boldsymbol{A}_s = \boldsymbol{U}_s^T \boldsymbol{D}_s \boldsymbol{U}_s \tag{19}$$

where every diagonal element of U_s is 1 and also the upper-diagonal elements are powers of 2. It can be verified that this procedure is possible provided A_s is tridiagonal, which is always the case for a ladder structure.

According to the decomposition of B_s, several systems can be obtained as listed in the following:

(i) *Type M1 (Fig. 6b)*

Use the straightforward decomposition of B_s according to eqn. 17:

$$B_s = SA_L 4D_L A_L^T S \tag{20}$$

In the lowpass case there are $(n-1)$ inductors in the prototype (Fig. 2*a*). D_L is $(n-1) \times (n-1)$ and A_L is $n \times (n-1)$. This also means that the rank of B_s is at most $n-1$, which is an important property related to the system behaviour at $\omega = 0$, as shown in the next Section.

(ii) *Type M2 (Fig. 6c)*

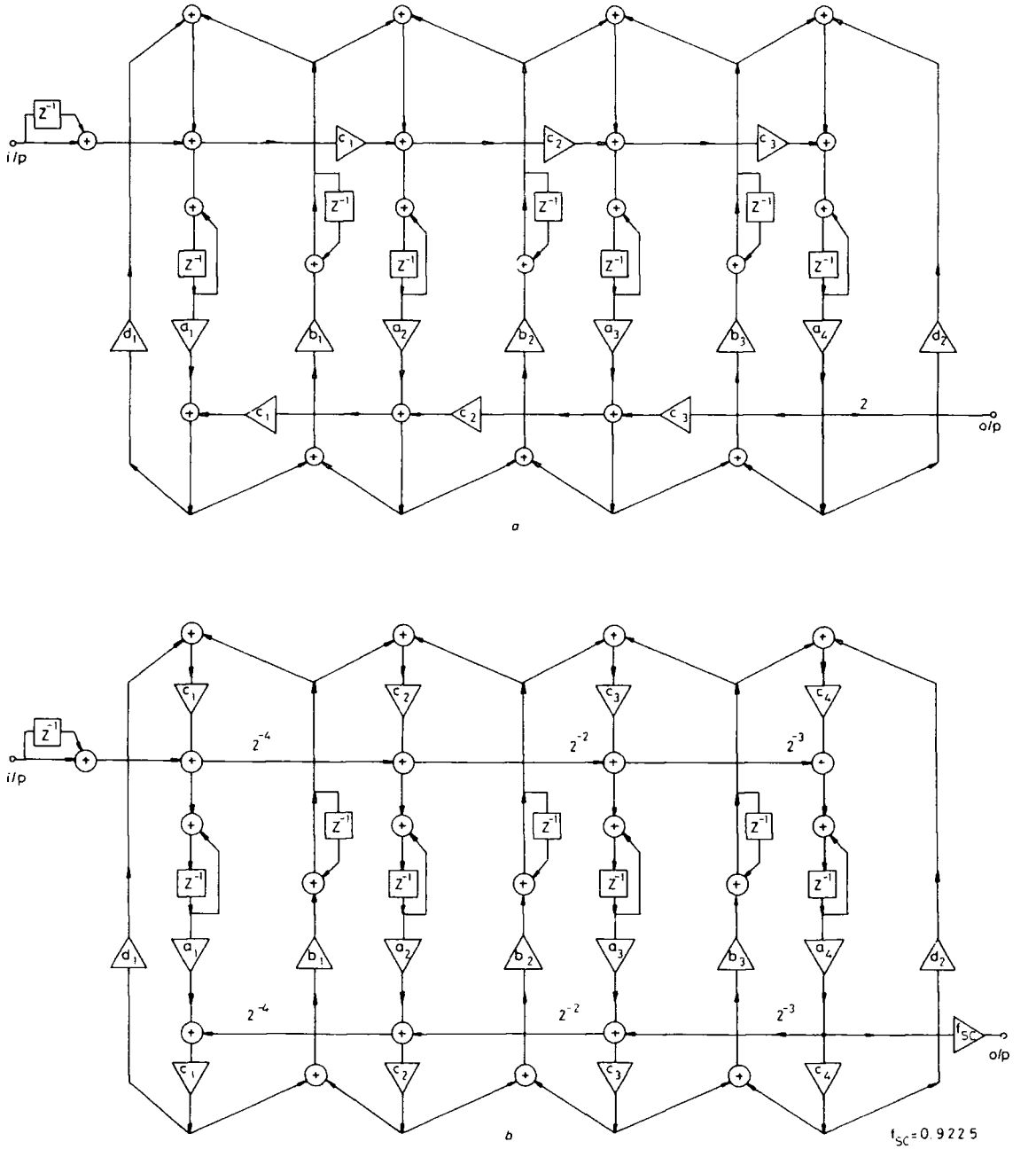
LU decomposition can also be performed on B_s

$$B_s = U_b^T D_b U_b \tag{21}$$

with diagonal entries of U_b being 1. As just mentioned, the rank of B_s is $n-1$, so that at the last step of LU decomposition the pivot is zero. In this case D_b and U_b can be expressed in $(n-1) \times (n-1)$ and $(n-1) \times n$ matrices, respectively.

(iii) *Type M3 (Fig. 6d)*

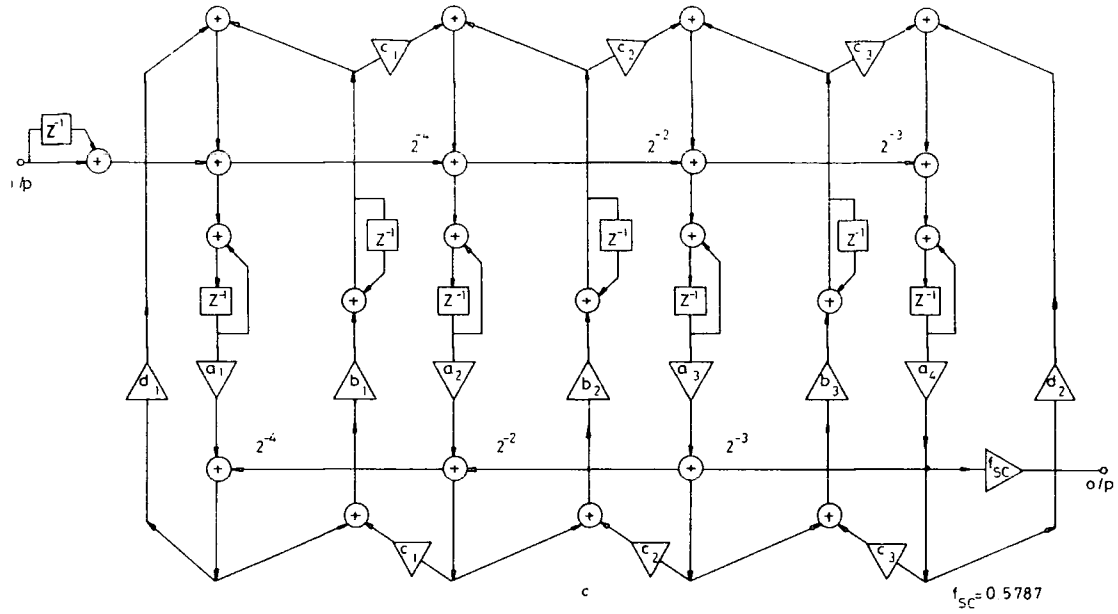
$$B_s = A_b D_b A_b^T + D_m \tag{22}$$



with all entries of A_h being either 1 or -1. It will be shown that although this type of circuit has an improved speed limitation, it has high sensitivity at $\omega = 0$.

4.3 Examples

The following example illustrates the design procedures for a Standard LL and a Type M1 circuit. For the



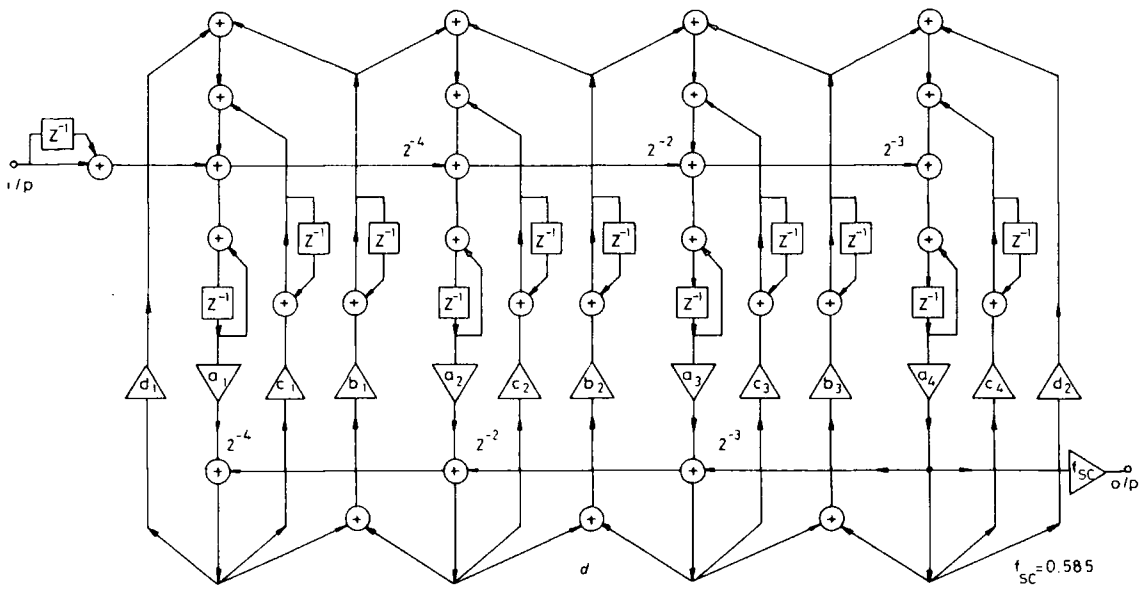


Fig. 6 *Digital realisations of the elliptic filter*

a Standard LL

$a_1 = 0.2056$ $b_1 = -0.9668$ $c_1 = -0.0850$
$a_2 = 0.1420$ $b_2 = -1.045$ $c_2 = -0.1509$
$a_3 = 0.1412$ $b_3 = -1.093$ $c_3 = -0.1201$
$a_4 = 0.2070$ $d_{1,2} = -2$

b Type M1

$a_1 = 0.5651$ $b_1 = -0.9668$ $c_1 = 0.6032$
$a_2 = 0.7219$ $b_2 = -1.045$ $c_2 = 0.4435$
$a_3 = 0.2616$ $b_3 = -1.093$ $c_3 = 0.7347$
$a_4 = 0.3541$ $c_4 = 0.7646$
$d_{1,2} = -2$

c Type M2

$a_1 = 0.8807$ $b_1 = -0.226$ $c_1 = 0.7352$
$a_2 = 1.125$ $b_2 = -0.131$ $c_2 = 1.657$
$a_3 = 0.4078$ $b_3 = -0.379$ $c_3 = 1.041$
$a_4 = 0.5519$ $d_1 = -0.4670$
$d_2 = -0.7502$

d Type M3

$a_1 = 0.8911$ $b_1 = -0.1640$ $c_1 = -0.5907$
$a_2 = 1.138$ $b_2 = -0.2159$ $c_2 = 0.1290$
$a_3 = 0.4126$ $b_3 = -0.3894$ $c_3 = -0.1265$
$a_4 = 0.5583$ $c_4 = -0.01587$
$d_1 = -0.4615$
$d_2 = -0.7416$

passive network, Fig. 2*a*, eqn. 1 becomes

$$\left\{ s \begin{bmatrix} 3.62 & 0.171 & & \\ 0.171 & 6.57 & 0.802 & \\ & 0.802 & 6.71 & 0.577 \\ & & 0.577 & 3.66 \end{bmatrix} + s^{-1} \begin{bmatrix} 0.242 & 0.242 & & \\ 0.242 & 0.503 & 0.261 & \\ & 0.261 & 0.535 & 0.273 \\ & & 0.273 & 0.273 \end{bmatrix} + \begin{bmatrix} 1 & & & \\ & 0 & & \\ & & 0 & \\ & & & 1 \end{bmatrix} \right\} V = \begin{bmatrix} J_{in} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (23)$$

where $V = [v_1, -v_2, v_3, -v_4]^T$. Let $s = (1 - z^{-1})/(1 + z^{-1})$ and follow the procedure eqns. 9–14. The relevant matrices are

$$A = \begin{bmatrix} 1 & & & \\ 0.085 & 1 & & \\ & 0.151 & 1 & \\ & & 0.121 & 1 \end{bmatrix} \begin{bmatrix} 4.86 & & & \\ & 7.04 & & \\ & & 7.08 & \\ & & & 4.83 \end{bmatrix} \times \begin{bmatrix} 1 & 0.085 & & \\ & 1 & 0.151 & \\ & & 1 & 0.121 \\ & & & 1 \end{bmatrix} \quad (24a)$$

$$4\Gamma = \begin{bmatrix} 1 & & & \\ 1 & 1 & & \\ & 1 & 1 & \\ & & 1 & \end{bmatrix} \begin{bmatrix} 0.968 & & & \\ & 1.06 & & \\ & & 1.09 & \end{bmatrix} \begin{bmatrix} 1 & 1 & & \\ & 1 & 1 & \\ & & 1 & 1 \end{bmatrix} \quad (24b)$$

$$2G = \begin{bmatrix} 2 & & & \\ & 0 & & \\ & & 0 & \\ & & & 2 \end{bmatrix} \quad (24c)$$

The standard LL realisation can now be drawn (Fig. 6*a*).

To produce a type M1 realisation, continue by choosing the scaling matrix S (from eqn. 17)

$$S = \text{diag}\,[0.603, 0.444, 0.735, 0.765] \quad (25)$$

Then for eqns. 17–20

$$A_s = SAS = U_s D_s U_s^T = \begin{bmatrix} 1 & & & \\ 2^{-4} & 1 & & \\ & 2^{-2} & 1 & \\ & & 2^{-3} & 1 \end{bmatrix} \times \begin{bmatrix} 1.77 & & & \\ & 1.39 & & \\ & & 3.82 & \\ & & & 2.82 \end{bmatrix} \begin{bmatrix} 1 & 2^{-4} & & \\ & 1 & 2^{-2} & \\ & & 1 & 2^{-3} \\ & & & 1 \end{bmatrix}$$

$$B_s = S4\Gamma S = \begin{bmatrix} 0.603 & & & \\ & 0.444 & & \\ & & 0.735 & \\ & & & 0.765 \end{bmatrix} \begin{bmatrix} 1 & & & \\ 1 & 1 & & \\ & 1 & 1 & \\ & & 1 & \end{bmatrix} \times \begin{bmatrix} 0.968 & & & \\ & 1.06 & & \\ & & 1.09 & \end{bmatrix} \begin{bmatrix} 1 & 1 & & \\ & 1 & 1 & \\ & & 1 & 1 \end{bmatrix} \begin{bmatrix} 0.603 & & & \\ & 0.444 & & \\ & & 0.735 & \\ & & & 0.765 \end{bmatrix}$$

$$G_s = S2GS = \begin{bmatrix} 0.603 & & & \\ & 0.444 & & \\ & & 0.735 & \\ & & & 0.765 \end{bmatrix} \begin{bmatrix} 2 & & & \\ & 0 & & \\ & & 0 & \\ & & & 2 \end{bmatrix} \times \begin{bmatrix} 0.603 & & & \\ & 0.444 & & \\ & & 0.735 & \\ & & & 0.765 \end{bmatrix} \quad (26)$$

The type M1 realisation shown in Fig. 6*b* follows immediately.

4.4 Comments

Since the transfer coefficients of the horizontal branches in Figs. 6*b–d* are all 2^k, and assuming shift and add has the same cost as addition, then for M1 and M2 the operation speed is limited by

$$T_s \geq \frac{m+5}{2} T_a + 3T_m \quad (27)$$

and for M3 the limit is given by

$$T_s \geq \frac{m+5}{2} T_a + 2T_m \quad (28)$$

All these new systems demonstrate a high degree of parallelism [1], and types M1 and M2 will show low sensitivity; thus a combination of the features of the biquad cascade and the wave filters is possible. As these new structures only use some simple matrix operations (see eqn. 14), they are particularly attractive in the case where an array processor is available.

It is important to distinguish between the number of multiplications and the number of multiplication coefficients to be stored in the new structure. Traditionally, in biquad and wave realisations these two processes are inextricably linked. In some of these new methods (standard LL, types M1 and M2), because of their symmetrical structures, two identical multiplications $\{c_i\}$ can be undertaken serially by one multiplier. For hardware implementation, therefore, the number of multipliers required is nearly cononical for these circuits. The adders can be shared in a similar way.

The methods introduced in this Section can be applied directly to bandpass but not to highpass and bandstop design. The difficulty is that for these latter cases the transfer function is not of zero value at $z = -1$ (corresponding to $s = \infty$ in continuous domain). However, the input function of eqn. 14, $(1 + z^{-1})|_{z=-1} = 0$. This implies that the transfer function from $(1 + z)J$ to the output must be infinite at $z = -1$ to facilitate cancellation, which inevitably results in an unstable system. For the highpass case this difficulty can be overcome by using a frequency transformation of $z^{-1} \rightarrow -z^{-1}$ to obtain the desired system from a lowpass

reference. For the bandstop case some different techniques are adopted which are beyond the scope of this paper.

5 Comparison of the various approaches

In the above Sections four types of digital filters simulating passive ladders have been proposed (standard LL and types M1–M3). Now they are compared with each other as well as with cascade biquad and wave realisations.

5.1 Sensitivity estimates

When the coefficient matrices in eqns. 11 and 18 are realised by digital circuits, they will deviate from their ideal values owing to finite wordlength. This also happens when they are realised by SC circuits, owing to element deviations. It is observed that the sensitivities of all four types of circuits differ most significantly at $\omega = 0$. This effect is now explained mathematically.

Making the standard substitution

$$j\Omega = j \tan(\omega T/2) = \left.\frac{1 - z^{-1}}{1 + z^{-1}}\right|_{z = e^{j\omega T}} \tag{29}$$

eqn. 9 becomes

$$[j(\Omega \boldsymbol{C} - \Omega^{-1}\boldsymbol{\Gamma}) + \boldsymbol{G}]\boldsymbol{V} = \boldsymbol{J} \tag{30}$$

Denote

$$\boldsymbol{Y} = j(\Omega \boldsymbol{C} - \Omega^{-1}\boldsymbol{\Gamma}) + \boldsymbol{G} \tag{31}$$

Use the following properties, which always hold true for a nodal description of a passive ladder (eqn. 1):

(*a*) $\boldsymbol{C}$, $\boldsymbol{\Gamma}$ and $\boldsymbol{G}$ are all tri-diagonal matrices; hence, $\boldsymbol{Y}$ is also tri-diagonal

(*b*) $\boldsymbol{J}$ has only one nonzero element, i.e. $\boldsymbol{J} = (J_{in}, 0, \ldots, 0)$

(*c*) $\boldsymbol{G}$ has only two nonzero elements $g_{11} = g_{in}$ and $g_{nn} = g_L$

(*d*) output is the nodal voltage v_n.

From these properties and Cramer's rule it can be found for output v_n

$$v_n = \frac{\prod_{i=1}^{n-1}[j\Omega c_{(i+1,i)} - (j\Omega)^{-1}\gamma_{(i+1,i)}]}{\det|\boldsymbol{Y}|} J_{in} \tag{32}$$

where $\boldsymbol{\Gamma} = \{\gamma_{(i,j)}\}$ and $\boldsymbol{C} = \{c_{(i,j)}\}$.

It can be shown that when $\Omega \to 0$,

$$\det|\boldsymbol{Y}| \to (j\Omega)^{-n} \det(\boldsymbol{\Gamma}) + (j\Omega)^{-(n-1)}[g_{11} \det(\boldsymbol{\Gamma})_{11} + g_{nn} \det(\boldsymbol{\Gamma})_{nn}] + (j\Omega)^{-(n-2)} \tag{33}$$

By comparing the power of $(j\Omega)^{-1}$ in the denominator and numerator it can be seen that in order to retain the output v_n nonzero, the coefficient of $(j\Omega)^{-n}$ in $\det|\boldsymbol{Y}|$ must be zero. This leads to the following:

Remark: The system given in eqn. 30 has nonzero response at $\Omega = 0$ only if $\boldsymbol{\Gamma}$ is singular. The response is given by

$$v_n = \frac{\prod_{i=1}^{n-1}\gamma_{(i+1,i)}}{g_{11} \det(\boldsymbol{\Gamma})_{11} + g_{nn} \det(\boldsymbol{\Gamma})_{nn}} J_{in} \quad \text{at} \quad \Omega = 0 \tag{34}$$

Otherwise, if $\boldsymbol{\Gamma}$ is nonsingular, then $v_n = 0$ at $\Omega = 0$.

Using this result for a lowpass filter, it would seem mandatory to ensure that $\boldsymbol{\Gamma}$ is singular. However, for LUD it is easily seen that deviation in the entries of $\boldsymbol{\Gamma}$ may cause it to become nonsingular; this is also true for type M3 from the relation that $\boldsymbol{\Gamma} = \boldsymbol{S}^{-1}(\boldsymbol{B}_s/4)\boldsymbol{S}^{-1}$. Only Standard LL, M1 and M2 will always guarantee singular $\boldsymbol{\Gamma}$ or $\boldsymbol{B}_s$ whatever the deviation in entries, since the decompositions of $\boldsymbol{\Gamma}$ or $\boldsymbol{B}_s$ in these three structures involve multiplications of matrices with only $(n-1)$ rows or columns. The resulting matrices can never have rank greater than $n-1$.

Incidentally, the extra zeros introduced at the origin can be viewed as an advantage or disadvantage according to the filter application; for instance, low-frequency noise suppression can be facilitated by these zeros.

5.2 Implementation cost

Table 1 gives a comparison of the implementation cost of the various types of digital filter proposed in this paper, as well as for the biquad and wave filters used for reference. It can be seen that type M3 is a special case. In the remaining five structures the numbers of multiplier coefficients to be stored are roughly equal. For the number of additions, delays and speed of operation, the biquad approach appears best, the wave filter is worst, with Standard LL, M1 and M2 being in between these extremes.

The lower limitation on T_s for the cascade biquad is achieved by assuming that a delay is inserted between every successive biquad block, so ensuring independent processing of the signal, but this increases the signal delay between input and output.

If adders are time-shared, then the numbers required for LL and its derived types can be much less than the numbers of additions listed in Table 1. For example, the minimum number of adders for type M1 is $(m+1)/2$, provided that other relevant figures in Table 1 are kept unchanged.

Table 1: Comparison of implementation cost and operation speed of various digital realisations for an odd-order lowpass elliptic function

Function	Cascade biquad	Wave	Standard LL	Type M1	Type M2	Type M3
Number of additions	$2m$	$6m-2$	$3m+1$	$3m+1$	$3m+1$	$\frac{7m+5}{2}$
Number of multiplier coefficients to be stored (scale factor f_{sc} not included)	$\frac{3m-1}{2}$	$\frac{3m+1}{2}$	$\frac{3}{2}(m+1)$	$\frac{3m+5}{2}$	$\frac{3}{2}(m+1)$	$\frac{3m-5}{2}$
Number of delays	m	$\frac{3m-1}{2}$	$m+1$	$m+1$	$m+1$	$\frac{3m+4}{2}$
Lower bound on T_s (T_m and T_a are multiplication and addition times, respectively)	$2T_a + T_m$	$3mT_a + mT_m$	$\frac{m+5}{2}T_a + \frac{m+1}{2}T_m$	$\frac{m+5}{2}T_a + 3T_m$	$\frac{m+5}{2}T_a + 3T_m$	$\frac{m+7}{2}T_a + 2T_m$

m = order of function

5.3 Design examples

In Fig. 7 the ideal response of a bilinear transformed digital elliptic lowpass response is given. Its prototype is simply the lowpass ladder in Fig. 2*a* (C-071536 Saal notation [16]). All six type digital structures are simulated using the same prototype. Sampling frequency is 32 000 Hz. It is assumed that floating-point storage of coefficients is used. All the coefficients are truncated to the nearest smaller number.

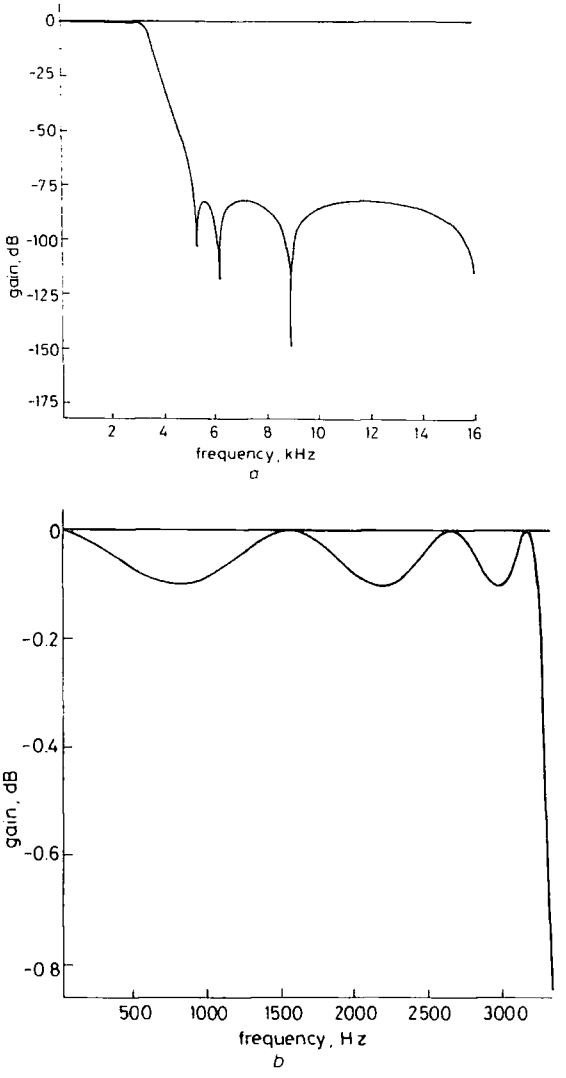


Fig. 7 *Ideal response of elliptic filter*
a Overall ideal response (wave digital with 16 bits)
b Ideal passband response of elliptic filter

The detailed passband responses for 8-bit implementation given in Fig. 8 show that a droop at zero-frequency occurs for type M3 and quite serious overall distortion for the biquad, whereas all other responses are almost ideal. When the wordlength is reduced to 4 bits, the overall filter response for wave and M1 is retained with reasonable accuracy while biquad response variation is dramatic, Fig. 9. The passband detail comparison of wave, M1, M2 and M3 realisation with 4 bits is also shown in Fig. 10. The zero-frequency droop exhibited by type M3 supports the mathematical prediction.

6 Conclusions

A new approach to the simulation of passive filter structures by active-*RC* and digital means has been developed. A detailed comparison of the various digital implementations has been undertaken and reveals that although the sensitivity of a wave digital filter is usually optimum, it can be approached by types standard LL, M1 and M2. However, in practical realisations types M1 and M2 will out-perform all others, apart from the biquad, in terms of speed of operation and number of additions and delays. For increased order, the wave filter shows linear increases in both multiplication and addition times, whereas the alternatives have a linear dependence only in addition time. So for sensitivity, speed of operation and cost of implementation, the new structures offer attractive possibilities, especially for high order realisations.

The scaling technique introduced in modified LL types in this paper may also find useful application in other digital filter implementations, and is worthy of further investigation.

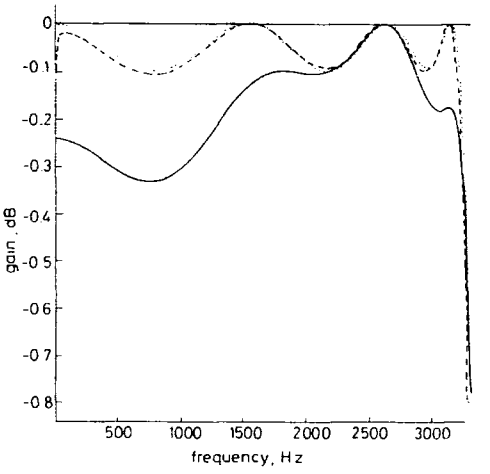


Fig. 8 *Filter passband responses with 8-bit digital realisation*
Biquad
M3
Wave, M1, M2

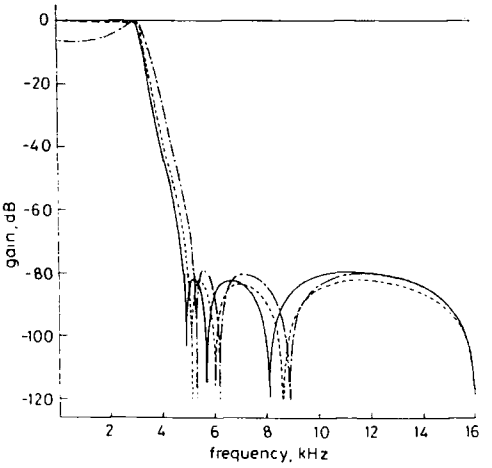


Fig. 9 *Overall frequency response of elliptic filter with 4-bit digital realisation*
M2
Wave
Biquad

The problem of truncation error analysis in these new structures is a more complex study and is the subject of future work.

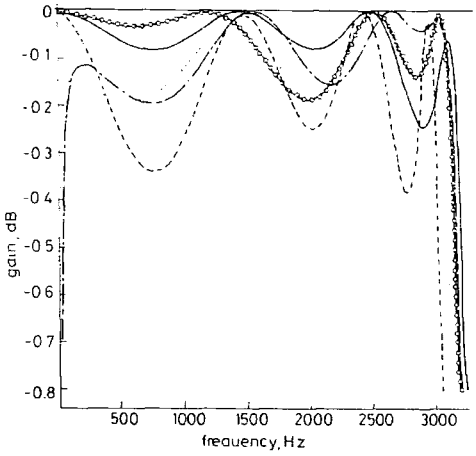


Fig. 10 *Filter passband responses with 4-bit digital realisation*

O—O Wave
——— Standard LL
- - - - Type M1
— — — Type M3
····· Type M2

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TABLE I
ELECTRONIC CHARACTERISTICS OF THE 8×8 NEURAL NET

	G_0	u_{thr}	ρ	γ	C_0
Mean Value	10S	- 70 mV	510 KΩ	4 ns	2 pF
Distribution	5%	10%	96%	5%	-

TABLE II
PERFORMANCE ESTIMATION OF THE 8×8 NEURAL NET CONTROLLER

Average rank	Average Throughput Efficiency	Analog Computation
8	98%	120ns
6	99.66%	120ns
4	100%	120ns
2	100%	120ns

totally optimal configuration matrices, the analog computation which results from the set of synaptic weights of (4) leads to very satisfactory throughput performance.

IV. Real-Time Simulation and Optimization of an 8×8 Neural Net Controller

Given an arbitrary input request matrix, the problem of maximizing the throughput of the crossbar reduces to finding numerical values for the set of synaptic weights defined in (4), and the characteristics of the amplifiers of an $N \times N$ neural net which would compute optimal configuration matrices in the least amount of time. It is clearly impossible to simulate the analog computation of a configuration matrix for each of the $2^{N^2} N \times N$ binary matrices. For $N = 8$, there are already of the order of 10^{19} possible input request matrices. In order to estimate the performance of the net, we have generated separate subsets of 500 input request matrices by choosing their matrix elements to be "1" with a probability χ and "0" with a probability $1 - \chi$, χ being a positive number between 0 and 1. Within each subset, the analog computation of a configuration matrix associated to each input request matrix has been real-time simulated by integrating on a VAX 8650 the set of coupled differential equations (1). The selected electronic characteristics of a VLSI implementation of the neural cells are reported in Table I for the 2-μm CMOS technology.

In Table I, G_0, u_{thr}, ρ and γ denote the average gain, offset, input resistance and propagation delay of the amplifiers respectively, and C_0 is the capacitance per connection. Such a distribution of the input resistances of the neurons is chosen in order to break the symmetry of the neuron time-constants so as to enhance the performance of the neural dynamics.

For $N = 8$, the resistances between neurons of the same row and the same column have been randomly chosen distributed around 4 kΩ within 1 percent. The initial voltages of the "free" neurons have been randomly distributed in the interval [−2.5 mV, +2.5 mV] around the ground potential. The stability of the analog computation with respect to noise has been tested by simulating, at the input of each inverter, a white noise gaussianly distributed around 0 V with a standard deviation of 10 μV. With this set of parameters and initial conditions, the time-evolution of the 8×8 neural net controller has been simulated for a period of 120 ns. The results of the simulation are reported in Table II for subsets of input request matrices having an average rank of 2, 4, 6, and 8 respectively. (The rank of an input request matrix being interpreted here as the maximum total number of packets that can be transmitted through the crossbar switch without destructive interference.)

The statistical estimations reported in Table II indicate that an 8×8 neural net controller which has the above characteristics is expected to compute configuration matrices within a period of 120 ns, and with at least 98 percent of average throughput efficiency.

V. Conclusions

This letter has demonstrated the efficiency of neural networks to arbitrate the packets at the input of an 8×8 crossbar switch with nearly optimal throughput performance. The proposed architecture computes configuration matrices in a lapse of time of approximately 100 ns, with an average throughput efficiency of at least 98 percent.

The number of neural interconnections of this architecture is of the order of N^3 (instead of N^4 for a fully connected neural net), N being the dimension of the crossbar. This reduction in the number of neural interconnections will facilitate hardware implementation of the proposed neural net arbitrator with VLSI technology, and perhaps of larger size controllers, e.g., 16×16. As for the 8×8, the resistance of the larger neural nets can be optimized through computer simulations of the real-time evolution of their neurons for various samplings of the input request matrices.

Finally, in view of the simplicity of this architecture, i.e., synaptic weights having the same sign and absence of external input currents, an implementation based on opto-electronic or photonic technologies would probably be more suitable for the larger size and faster switch controllers.

Acknowledgment

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The TWINTOR in Bandstop Switched-Capacitor Ladder Filter Realization

LI PING AND J. I. SEWELL

Abstract **— A new design for strays-insensitive bandstop switched-capacitor (SC) ladder filter structures is introduced. A two channel scheme obviates the need for term cancellation in realizing bandstop-type operators and is less demanding on opamp settling time.**

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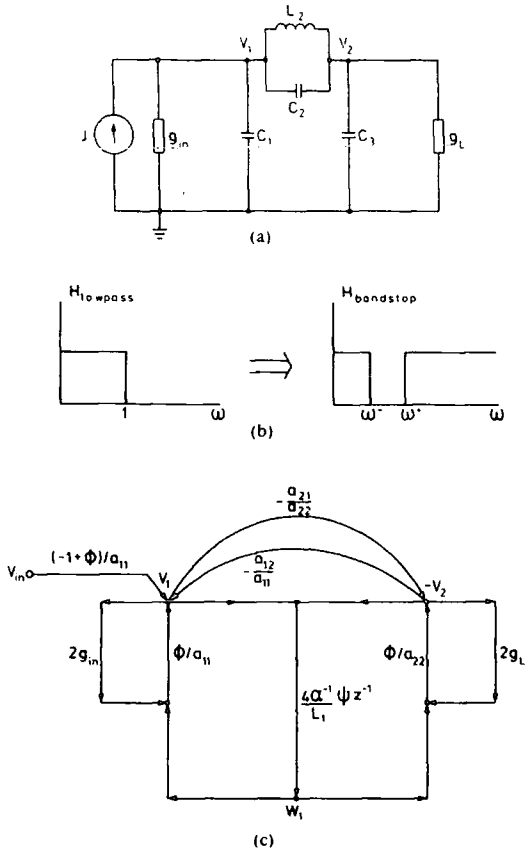

Fig. 1. (a) A third-order normalized low-pass ladder. (b) Low-pass to bandstop transformation. (c) The signal flowgraph of leapfrog-type simulation.

I. Introduction

Switched-capacitor (SC) filter structures based on passive ladder simulations have attracted much attention because of their low sensitivity properties. However, an instability problem exists in the design of bandstop SC ladders by stray-insensitive LDI integrators [1]. A second-order building block technique has been proposed in [2] to overcome this difficulty.

In this paper a new type of second-order building-block called a TWINTOR (TWinned INTegraOR) is introduced for bandstop SC ladder design. The circuit uses two signal channels to directly realize the basic bandstop operators without term cancellations [2], and also reduces the required opamp operation speed by a factor of two. Either single-input or differential-input integrators are allowed, giving flexibility for fabrication.

II. The TWINTOR Circuit

Following a matrix leapfrog method [3], [4] a passive low-pass reference *RLC* ladder, Fig. 1(a), is described by the nodal admittance matrix equation

$$\left(sC + \frac{1}{s}\Gamma + G\right) = V = J \tag{1}$$

where C, Γ, and G are admittance matrices formed by the contributions of capacitors, inductors, and resistors, respectively. The voltage vector $V = [v_1, -v_2, v_3, -v_4, \cdots]$ to ensure all the entries of the matrices non-negative. It is well known that in the continuous-time domain a symmetric bandstop function can be derived from a normalized low-pass one by transformation [5], (see Fig. 1(b)):

$$s \rightarrow a^{-1}\left(\frac{s}{\omega_m} + \frac{\omega_m}{s}\right)^{-1} \tag{2}$$

with

$$a = \frac{\omega_m}{\omega^+ - \omega^-}, \qquad \omega_m = \sqrt{\omega^+ \omega^-}.$$

Substitute (2) into (1) and perform the bilinear transformation $s = 2(1 - z^{-1})/T(1 + z^{-1})$,

$$\left\{a^{-1}\left(\frac{2}{\omega_m T}\frac{1-z^{-1}}{1+z^{-1}} + \frac{\omega_m T}{2}\frac{1+z^{-1}}{1-z^{-1}}\right)^{-1} C + a\left(\frac{2}{\omega_m T}\frac{1-z^{-1}}{1+z^{-1}} + \frac{\omega_m T}{2}\frac{1+z^{-1}}{1-z^{-1}}\right)\Gamma + G\right\} V = J. \tag{3}$$

Multiply through (3) by the coefficient of Γ and rearrange to give

$$(A - 4\alpha z^{-1}\Psi\Phi\Gamma - \Phi 2G) = (-1 + \Phi)J \tag{4}$$

where

$$\Phi = (\beta z^{-1} - 1)/(1 - z^{-2})$$
$$\Psi = (z^{-1} - \beta)/(1 - z^{-2})$$
$$A = \alpha^{-1}C + \alpha\Gamma - \Gamma - G$$

with

$$\mu = \omega_m T/2$$
$$\alpha = a(\mu^{-1} + \mu)$$
$$\beta = (\mu^{-1} - \mu)/(\mu^{-1} + \mu).$$

Topologically, decompose Γ into

$$\Gamma = A_L D_L A_L^T \tag{5}$$

where A_L is an incidence matrix of the inductors in the ladder, D_L is a diagonal matrix of reciprocal inductance values. With this (4) can be rewritten in the form

$$\begin{cases} AV = \Phi(A_L W + 2GV) + (-1 + \Phi)J & \text{(6a)} \\ W = 4\alpha^{-1}z^{-1}\Psi D_L A_L^T V & \text{(6b)} \end{cases}$$

A signal flowgraph can be drawn to represent (6), Fig. 1(c) which can be replaced by a SC circuit. The frequency-dependent operators Ψ and Φ given by (4) are realized with a new TWINTOR second-order strays-insensitive biquad scheme, Fig. 2(a). In a TWINTOR each opamp is operated only in every other period, T. The charge relations for the circuit of Fig. 2(a) are

$$C_e[y^e(n) - y^e(n-2)] = -C_1 x^e(n) + C_2 x^0(n-1)$$
when n even (7a)

$$C_3[y^0(n) - y^0(n-2)] = -C_1 x^0(n) + C_2 x^e(n-1)$$
when n odd. (7b)

Therefore, the overall transfer function is given by

$$Y(z) = \frac{1}{C_3}\frac{C_2 z^{-1} - C_1}{1 - z^{-2}} X(z). \tag{8}$$

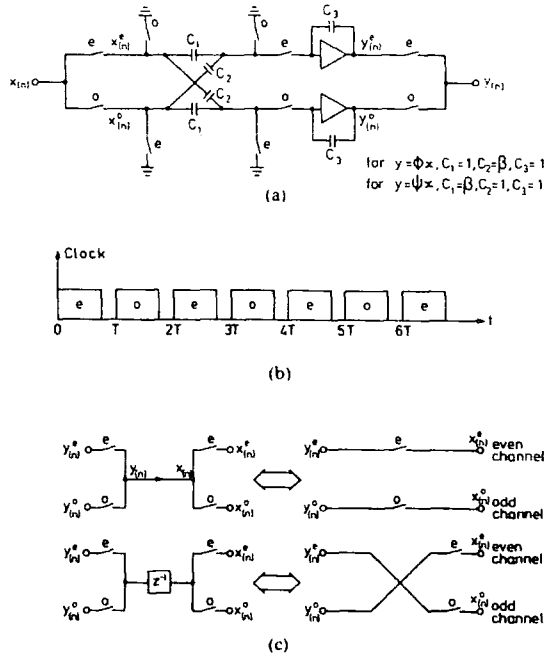

Fig. 2. (a) A TWINTOR circuit. (b) The clock waveform. (c) Two channel equivalent connectors of TWINTOR's.

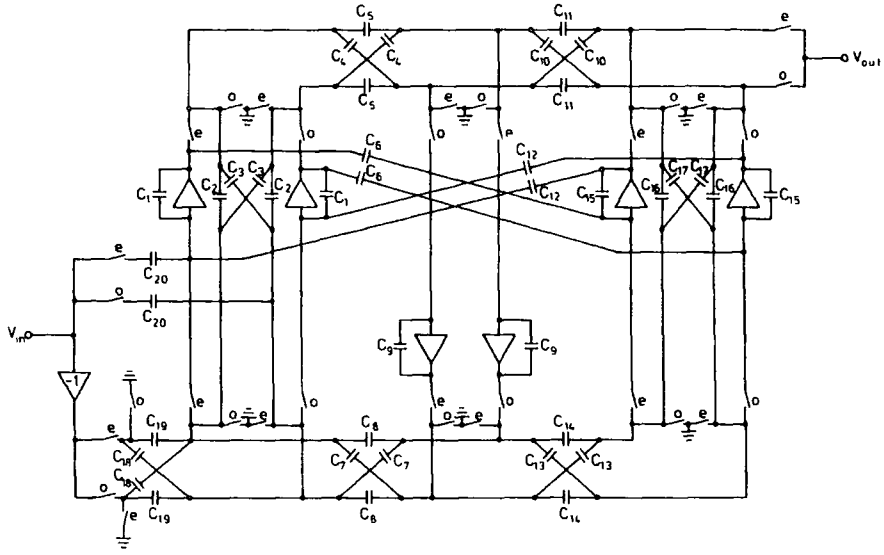

Fig. 3. A sixth-order bandstop SC bichannel filter realization.

Notice that the denominator $(1 - z^{-2})$ is exactly realized without term cancellation.

It can be seen from Fig. 2(b) that now the clock period is $2T$ compared to T in a conventional LDI integrator SC circuit. This means that the operation speed for the whole circuit, determined by sampling frequency, can be doubled without requiring an increase in opamp speed.

By selecting suitable capacitance values Φ and Ψ can be easily implemented. When TWINTORS are connected together to form a ladder structure, some simplifications are possible by separating signals into two channels, Fig. 2(c). The first equivalence in Fig. 2(c) is obvious. For the second equivalence, notice that a sampling signal of an even (odd) channel opamp output in a odd (even) period is actually the signal held from the previous period, therefore a delay factor, z^{-1}, is realized. A number of switches are saved by this two channel technique.

An overall sixth-order bichannel bandstop SC ladder is shown in Fig. 3 with the low-pass *RLC* ladder of Fig. (1a) as reference

TABLE I
DESIGN DATA FOR THE SIXTH-ORDER SC BANDSTOP FILTER

Specifications for the Bandstop SC Filter

lower passband edge	4.5 kHz	upper passband edge	5.5 kHz
lower stopband edge	3.5 kHz	upper stopband edge	6.5 kHz
passband ripple	< 0.1 dB	stopband attenuation	> 26 dB
sampling frequency	100 kHz		

Normalized Data for the Lowpass SC Ladder Reference Filter

G1 = GL = 1 C1 0.91646 L2 0.96995 C2 0.17046 C3 0.91646

Component Values for the Bandstop SC Filter

C1	14.79097	C2	1.414525	C3	1.398662	C4	1.614900	C5	1.633215
C6	15.64070	C7	37.44417	C8	37.86882	C9	1.000000	C10	1.141830
C11	1.154780	C12	10.93656	C13	37.86304	C14	38.29245	C15	10.57509
C16	1.011341	C17	1.000000	C18	1.977572	C19	2.000000	C20	1.000000

number of capacitors	40	number of switches	30
number of op amps	6	total capacitance	439.51
capacitance spread	38.29		

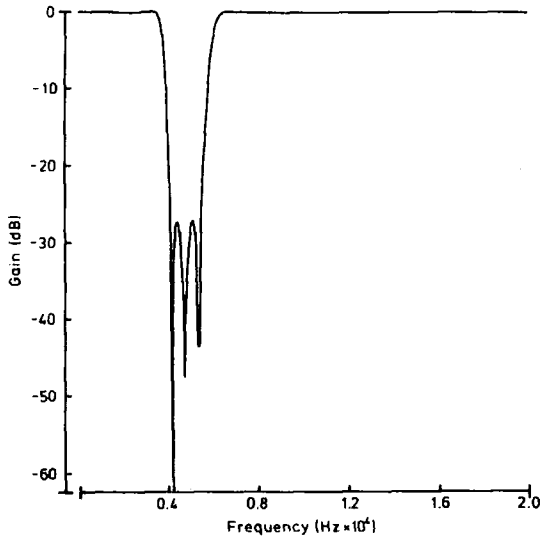

Fig. 4. Computed response of the SC bandstop filter.

prototype. The specifications and the component values are listed in Table I. The simulated response of the SC bandstop ladder is shown in Fig. 4. A negative input is required to realize the constant term in (6a), which may be avoided by the technique of [6].

III. CONCLUSIONS

A new strays-free SC circuit scheme has been proposed for bandstop SC ladder design. A major feature of the new circuit is that the clock period required is $2T$ so that the circuit can operate at a higher speed without extra demands on opamp performance.

ACKNOWLEDGMENT

The authors are grateful for the valuable help from R. K. Henderson.

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An Improved Search Algorithm for the Design of Multiplierless FIR Filters with Powers-of-Two Coefficients

HENRY SAMUELI

Abstract **— An improved algorithm is presented for the discrete optimization of FIR digital filter coefficients which are represented by a canonic signed-digit (CSD) code, i.e., numbers representable as sums or differences of powers-of-two. The proposed search algorithm allocates an extra nonzero digit in the CSD code to the larger coefficients to compensate for the very nonuniform nature of the CSD coefficient distribution. This results in a small increase in the filter complexity however the improvement in the frequency response is substantial. The coefficient optimization is performed in two stages. The first stage searches for an optimum scale factor and the second stage consists of a local bivariate search in the neighborhood of the scaled and rounded coefficients.**

I. INTRODUCTION

High-speed digital filtering applications (sample rates in excess of 10 MHz) generally require the use of custom application specific integrated circuits (ASIC's). Programmable signal processors cannot accommodate such high sample rates without an

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PAPER 39

High-performance filter networks and symmetric matrix systems

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Indexing terms: Filters and filtering, Matrix algebra

Abstract: A unified investigation is presented for low-sensitivity and limit-cycle-free filter structures. It is shown that important properties like boundedness and pseudopassivity are closely related to the symmetry of the system matrix description. Negative elements can be incorporated in certain prototypes leading to real advantages in switched-capacitor (*SC*) realisations. Stability and noise problems are also discussed. According to the realisation, component variations can result in matrix symmetry being maintained, or more generally, in the introduction of assymmetry. Sensitivity considerations are outlined for both situations. Implementation by passive *RLC*, SC and digital circuits are considered.

1 Introduction

There are a number of attractive features about filter structures derived from passive *RLC* network simulations: they show very low sensitivity in the passband, which is an important factor for active-*RC* and switched-capacitor (*SC*) filter fabrications [1–7]. They can be made limit-cycle free for digital-filter implementation, as shown for wave structures [8–10], and they usually have better dynamic range compared with cascade biquads or other direct-form structures, which can be observed from many practical designs. Limit-cycle suppression and better dynamic range can improve the noise behaviour of the circuits.

Theories have been proposed to analyse and generalise the properties of passive ladders and their simulations [10, 14]. A unified investigation has been proposed in References 17 and 18 for digital circuits. It was shown that general low-sensitivity filters can be constructed by properly connecting LBR (lossless-bounded-real) sections, which include adaptors for wave digital circuits as specific examples. In general, this approach is mainly concerned with the topological point of view.

This paper investigates the problem of high-quality network design based on matrix principles. Attention is given to the properties of the system descriptions of the circuits. It is shown that matrix symmetry is a crucial factor to ensure optimal performance of the systems. Two concepts considered by many other authors, boundedness and pseudopassivity, are proved to be closely related to the matrix symmetry.

A difference between the topological [8–18] and matrix approaches is that the former analyses the behaviour of local building blocks, whereas the latter examines the overall system. The two approaches complement each other to provide insight into the filter design problem.

The matrix system discussed in this paper can be used to produce prototypes for various implementations. Detailed realisation methods are discussed elsewhere [20–22]. It is also shown that the symmetric matrix system is a generalised concept of a passive network, allowing negative elements. Examples will be given to show that advantages can be gained for *SC* and digital simulations.

The problem of sensitivity behaviour for asymmetric deviations is also investigated. In active-*RC* or *SC* implementations the component deviations may destroy the symmetry of the system description. From practical observations the sensitivities of active-*RC* and *SC* ladder simulations are nevertheless very good; this is attributed to their multifeedback nature. Sensitivity formulas are presented which clearly indicate that better performance is assured by more complete symmetry.

2 Basic concepts

The concept of boundedness can be traced back to an observation by Orchard about the low-sensitivity properties of doubly terminated ladders [1].

Definition 1. Boundedness: The transfer function $H(\boldsymbol{P})$ of a system is said to be bounded with respect to the change of a set of parameters, $\boldsymbol{P} = \{p_i\}$, if there is a positive number M and

$$|H(\boldsymbol{P})| \leqslant M \tag{1}$$

is always satisfied when $\boldsymbol{P}$ varies within the allowed range.

When a bounded system is properly designed to make $|H(\boldsymbol{P})|$ attain M at a frequency point in the passband $j\omega_m$, then the deviation of $\boldsymbol{P}$ can only cause $|H(\boldsymbol{P})|$ to decrease. This means that $|H(\boldsymbol{P})|$ must have zero derivative with respect to any parameter p_i at $j\omega_m$, and consequently the sensitivity is also zero, i.e.

$$S_{p_i}^{|H|} = \frac{p_i}{|H(\boldsymbol{P})|} \frac{\partial |H(\boldsymbol{P})|}{\partial p_i} = 0 \quad \text{at } s = j\omega_m \tag{2}$$

and it may be reasonably expected that over the whole passband the sensitivity will remain small, a reassuring argument used by many other authors for ladders as well as various simulation methods [23–25].

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The generalised concept of pseudopassivity has been employed in discussion for wave digital filters [10], which is, in fact, based on the principle of the Lyapunov function. Consider a standard state-space system in the continuous domain

$$sX = AX + BJ \tag{3}$$

or in the discrete domain

$$X = z^{-1}AX + BJ \tag{4}$$

Definition 2: Pseudopassivity: A state-space system eqn. 3 or 4 is said to be pseudopassive if

$$e(t) = x^T(t)x(t) \tag{5}$$

is a monotonically decreasing function for any initial value $x(0) = X_0$ with $J = 0$. (For a discrete system $x(t)$ is examined at a discrete instance, i.e. $t = nT$).

$e(t)$ can be seen as an energy function and it is always decreasing for a pseudopassive system without excitation. The pseudopassive property in a discrete system is important for the suppression of parasitic oscillations. If the input $J = 0$, the state-space variables $x(nT)$, and so all the variables, in a stable digital system (eqn. 4) will approach zero regardless of the initial state in the ideal linear case. However, when the necessary quantisations are adopted in a digital filter, $x(nT)$ may oscillate and take nonzero values due to nonlinear effects, which may even cover the entire number range in the filter when overflow occurs. These parasitic oscillations, so-called limit cycles, can be avoided if the discrete system is pseudopassive and magnitude rounding for quantisation of $x(nT)$ is adopted. In magnitude rounding, a number a is truncated to a finite number of bits $Q[a]$, with $|Q[a]| \leqslant |a|$. Let $Q[x]$ denote the vector of x after magnitude rounding, and suppose in a pseudopassive system (eqn. 4) that these are the only quantisation operations, then according to eqn. 5

$$Q^T[x(nT)]Q[x(nT)] \leqslant x^T(nT)x(nT) \leqslant Q^T[x((n-1)T)] \times Q[x((n-1)T)] \leqslant x((n-1)T)x((n-1)T) \leqslant \cdots \tag{6}$$

Therefore, if $x(nT) \to 0$ in the ideal case, then in the non-ideal case it will still approach zero. This will completely suppress limit cycles [10, 18].

The second norm of a matrix A is given by [27]

$$\|A\| = \max_{x \neq 0} \frac{x^T A^T A x}{x^T x} \tag{7}$$

The time-domain equation (eqn. 4) gives (when $J = 0$)

$$x(n) = Ax(n-1) \tag{8}$$

Hence, from eqns. 7 and 8 a necessary and sufficient condition for pseudopassivity is

$$\|A\| \leqslant 1 \tag{9}$$

In this case

$$x^T(n+k)x(n+k) \leqslant \cdots \leqslant x^T(n)x(n) = x^T(n-1)A^T A x(n-1) \leqslant x^T(n-1)x(n-1) \tag{10}$$

It has been proved on a topological basis that the condition in eqn. 9 is met by wave, normalised-lattice and LBR structures [18], and the same concept has been used in the design of second-order 'minimum norm' building blocks [19]. In Section 4 it will be shown that higher order networks, based on a symmetric matrix decomposition approach, can also be designed to meet this condition.

3 Continuous symmetric matrix systems

Consider the matrix system of the following form:

$$YV = J \tag{11a}$$

with

$$Y = sC + s^{-1}\Gamma + G \tag{11b}$$

Output functions may be added in the form

$$y = DV + EJ \tag{12}$$

but only the system in eqn. 11 will be considered, since sensitivity and noise problems arise mainly from the feedback loops in eqn. 11.

Eqn. 11 is a generalised form of the standard state-space equation (eqn. 3). Indeed, eqn. 11 is reduced to eqn. 3 when $\Gamma = 0$. Alternatively, eqn. 11 can always be rearranged into the form of eqn. 3 by introducing some intermediate variables. However, the advantage of using the system description of eqn. 11 is that optimal performance can be achieved by imposing some simple conditions (notably symmetry) on the matrix. If the matrices in eqn. 3 are constrained to be symmetric, then the system can only have real poles, which is too restrictive for most applications.

The most convenient way to set up the system in eqn. 11 is the formulation of the network equations (nodal, loop or hybrid) of a general passive *RLC* ladder, designed either by a synthesis process or with the help of tables. It can be easily shown that in this case all the matrices of eqn. 11*b* can be made non-negative if nodal or loop formulations are used. For more general cases, an optimisation procedure can be used to adjust the entries of the matrices of eqn. 11 to make the transfer function fit the prescribed specifications. In this case conditions are required for testing the stability of the resulting system.

3.1 Critical stability

It can be shown that the system in eqn. 11 is critically stable if C, Γ and G are all symmetric non-negative. Let $\{s_m = \sigma_m + j\omega_m\}$ be the set of roots of det $Y(s)$ of eqn. 11

$$\det(s_m^2 C + s_m G + \Gamma) = 0 \tag{13}$$

So there is a non-zero vector X which satisfies [27] the equation

$$X^*(s_m^2 C + s_m G + \Gamma)X = 0 \tag{14}$$

(X^* denotes the transposed conjugate of X) or

$$as_m^2 + bs_m + c = 0 \tag{15}$$

with

$$a = X^*CX \quad b = X^*GX \quad c = X^*\Gamma X \tag{16}$$

As C, G and Γ are all definite non-negative, a, b and c are all non-negative numbers [27]. But in this case, eqn. 15 has no roots with

$$\mathrm{Re}(s_m) = \sigma_m > 0 \tag{17}$$

That is, the system in eqn. 11 has no poles in the right-half plane if C, Γ and G are all symmetric non-negative.

3.2 Absolute stability

The absolute stability condition for the system in eqn. 11 is that $\sigma_m < 0$ for all m. Therefore, some extra constraints should be added to ensure that no roots lie on the imaginary axis. This can be checked by evaluating det $|Y(j\omega)|$. In most cases the system in eqn. 11 is designed to realise a transfer function $H(s)$ which has no

poles on the imaginary axis. If the system is properly designed without redundancy so that the order of the system is equal to the order of $H(s)$, or in other words it is observable from the output, then it will have no poles on the imaginary axis either, as in this case $H(s)$ and the system have the same set of poles.

The non-negative property of the symmetric matrices C, Γ and G can be easily tested. For instance, decompose C into symmetric LU form [28]

$$C = L_c D_c L_c^T \tag{18}$$

where D_c is a diagonal matrix. C is non-negative if, and only if, all the entries of D_c are non-negative. The computational requirement for this test is nearly equal to performing Gaussian elimination.

3.3 Boundedness

From network topology it is known that the output power of a doubly terminated ladder is bounded by maximum input power, a reasonable fact since a passive ladder cannot create power within itself. This result can also apply to the system in eqn. 11 in a more abstract sense. Let eqn. 11 be evaluated on the imaginary axis $s = j\omega$ and denote

$$Q = \omega C - \omega^{-1}\Gamma \tag{19}$$

The system can be written as

$$YV = (jQ + G)V = J \tag{20}$$

Suppose matrix G in eqn. 11 can be separated according to input and output parts, respectively,

$$G = G_{in} + G_{out} \tag{21}$$

Then eqn. 20 can be written as

$$jQV + G_{out}V + G_{in}V = J \tag{22}$$

We first prove a general relation.

Theorem 1: Assume that in eqn. 11

(i) $G_{in}X = J$ has at least one solution

(ii) all matrices are symmetric non-negative.

Then the following inequality holds:

$$V^*G_{out}V \leqslant \tfrac{1}{4}J^*R_{in}J \tag{23}$$

where R_{in} is the Moore-Penrose inverse of G_{in}.

Proof: According to Moore-Penrose's theories [28, 29], R_{in} is defined by

$$\begin{aligned} G_{in}R_{in}G_{in} &= G_{in} \qquad R_{in}G_{in}R_{in} = R_{in} \\ (G_{in}R_{in})^T &= G_{in}R_{in} \quad (R_{in}G_{in})^T = R_{in}G_{in} \end{aligned} \tag{24}$$

and $X_s = R_{in}J$ is a solution of $G_{in}X = J$, if it has a solution at all, which means

$$G_{in}R_{in}J = J \tag{25}$$

Now multiply eqn. 11 by V^*

$$jV^*QV + V^*G_{out}V + V^*G_{in}V = V^*J \tag{26}$$

Take the real part of eqn. 26

$$V^*G_{out}V = \mathrm{Re}\,\{V^*J\} - V^*G_{in}V \tag{27}$$

Notice from eqns. 24 and 25

$$\begin{aligned} &[J^*R_{in}J - (J^* - 2V^*G_{in})R_{in}(J - 2G_{in}V)]/4 \\ &= [2J^*R_{in}G_{in}V - 2V^*G_{in}R_{in}J - 4V^*G_{in}R_{in}G_{in}V]/4 \\ &= \mathrm{Re}\,\{V^*J\} - V^*G_{in}V \end{aligned} \tag{28}$$

From eqns. 27 and 28

$$\begin{aligned} V^*G_{out}V = [&J^*R_{in}J \\ &- (J^* - 2V^*G_{in})R_{in}(J - 2G_{in}V)]/4 \end{aligned} \tag{29}$$

If G_{in} is non-negative, then from eqn. 24 R_{in} is also non-negative, which means that $(J^* - 2Y^*G_{in})R_{in}(J - 2G_{in}V)$ is a non-negative number. Theorem 1 follows from eqn. 29 immediately.

3.4 Boundedness for terminated reactance network

Eqn. 23 is a general expression which can be applied to multi-input/output systems. To provide some insight of its physical meaning, consider the special case of a single-input/output system. Suppose eqn. 11 has only one input $J = [J_1, 0, \ldots, 0]$ and one output v_n. G_{in} and G_{out} have only one non-zero diagonal entry, respectively, corresponding to the input and output, i.e.

$$G_{in} = \mathrm{diag}\,(g_{11}, 0, 0, \ldots, 0) \tag{30a}$$

$$G_{out} = \mathrm{diag}\,(0, 0, \ldots, 0, g_{nn}) \tag{30b}$$

Then R_{in} can be generated by

$$R_{in} = \mathrm{diag}\,(g_{11}^{-1}, 0, 0, \ldots, 0) \tag{31}$$

Therefore, in this case eqn. 29 is reduced to

$$g_{nn}|v_n|^2 = [1 - |1 - 2g_{11}v_1/J_1|^2]\frac{1}{4g_{11}}|J_1|^2 \tag{32}$$

so

$$g_{nn}|v_n|^2 \leqslant \frac{1}{4g_{11}}|J_1|^2 \tag{33}$$

or

$$|v_n| \leqslant \frac{1}{2(g_{11}g_{nn})^{1/2}}|J_1| \tag{34}$$

A typical example of the system constrained by the conditions of eqn. 30 is a doubly terminated ladder (Fig. 1),

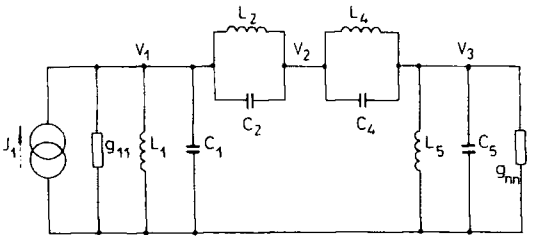


Fig. 1 *Terminated LC ladder passive prototype*

in which case (eqn. 11) are its nodal equations with input and output nodes labelled 1 and n, respectively. The physical meaning of eqn. 32 can be seen by rewriting it as

$$g_{nn}|v_n|^2 = [1 - |\rho|^2]g_{11}^{-1}|J_1|^2/4 \tag{35}$$

with ρ defined by

$$\rho = 1 - 2g_{11}v_1/J_1 \tag{36}$$

Consider a passive ladder with the source resistor being $r_{11} = g_{11}^{-1}$ and input impedance of the two-port ladder including the load is $z_{in} = y_{in}^{-1}$

$$\begin{aligned} \rho = 1 - 2g_{11}v_1/J_1 &= 1 - \frac{2g_{11}}{y_{in} + g_{11}} \\ &= \frac{y_{in} - g_{11}}{y_{in} + g_{11}} = \frac{r_{11} - z_{in}}{r_{11} + z_{in}} \end{aligned} \tag{37}$$

So ρ is just the reflection function and the upper bound of $|v_n|$ is attained at $\rho = 0$. This result is well known in network theory.

In the proof of the boundedness, no condition has been imposed on C and Γ except that they must be symmetric and non-negative. Accordingly, zero-sensitivity with respect to symmetric deviation can be achieved at the frequency points where the transfer function attains its upperbound.

4 Sensitivity formulas

The above result provides only an estimation of sensitivity for symmetric deviations. More general sensitivity formulas are now derived. To simplify the problem, only single-input/output system will be considered.

Suppose a single-input/output system meets the conditions of theorem 1 and eqn. 30. Let the system in eqn. 11*a* be excited by another arbitrary input K instead of J and let the response be U. The system can be written as

$$YU = K \tag{38}$$

then the output of the new system is related to the old system by

$$u_n = (2g_{nn}\bar{v}_n)^{-1}(\bar{\rho}V^T - V^*)K \tag{39}$$

($^-$ indicates conjugate). The derivation of eqn. 39 is given in Appendix 10.1.

4.1 Sensitivity formulas

Differentiate eqn. 11*a* w.r.t. some network element ξ to get

$$Y\,dV/d\xi + V\,dY/d\xi = 0 \tag{40}$$

Here the second term can be viewed as the new input vector for eqn. 38 and we have

Theorem 2:

$$dv_n/d\xi = (2g_{nn}\bar{v}_n)^{-1}(-\bar{\rho}V^T + V^*)\,dY/d\xi\,V \tag{41a}$$

and

$$\begin{aligned} d|v_n|/d\xi &= \mathrm{Re}\,[\bar{v}_n\,dv_n/d\xi]/|v_n| \\ &= (2g_{nn}|v_n|)^{-1}\,\mathrm{Re}\,[(-\bar{\rho}V^T + V^*)\,dY/d\xi\,V] \end{aligned} \tag{41b}$$

In particular, if the deviation of ξ only perturbs the imaginary part of Y, jX say, and $dY/d\xi = j\,dX/d\xi$ is symmetric, then

$$\begin{aligned} d|v_n|/d\xi &= (2g_{nn}|v_n|)^{-1}\,\mathrm{Re}\,[-j\bar{\rho}V^T\,dX/d\xi\,V \\ &\quad + j|V^*\,dX/d\xi\,V|] \\ &= (2g_{nn}|v_n|)^{-1}\,\mathrm{Re}\,[-j\bar{\rho}V^T\,dX/d\xi\,V] \\ &= -(2g_{nn}|v_n|)^{-1}\,\mathrm{Im}\,[\rho V^T\,dX/d\xi\,V] \end{aligned} \tag{42}$$

So $d|v_n|/d\xi = 0$ when $\rho = 0$. This again confirms the conclusion for single-input/output system, that $|v_n|$ attains its upper bound and has zero-sensitivity at $\rho = 0$, if the deviation is symmetric.

4.2 Application to passive networks

When the system in eqn. 11 is implemented by a real passive RLC network, $\xi \in \{R_i, L_i, C_i\}$ and $dY/d\xi$ is always symmetric. Then a very simple alternative to the topological derivation of sensitivity follows: let the contribution to Y of a branch admittance jq_k between nodes a, b be $jq_k M_{ab}$, where

$$M_{ab} = \begin{bmatrix} 0 & \vdots & \vdots & 0 \\ \cdots & 1 & -1 & \cdots \\ \cdots & -1 & 1 & \cdots \\ 0 & \vdots & \vdots & 0 \end{bmatrix} \begin{matrix} \\ a \\ b \\ \\ \end{matrix} \qquad \begin{matrix} \\ \\ \\ a \quad b \end{matrix} \tag{43}$$

So

$$dY/dq_k = jM_{ab} \tag{44}$$

It is easily seen that

$$V^T M_{ab} V = v_k^2 \quad \text{and} \quad V^* M_{ab} V = |v_k|^2 \tag{45}$$

where v_k is the voltage across jq_k. Then eqns. 41*a* and *b* are reduced to

$$dv_n/dq_k = (2g_{nn}|v_n|)^{-1}(-j\bar{\rho}v_k^2 + |v_k|^2) \tag{46a}$$

and

$$d|v_n|/dq_k = (2g_{nn}|v_n|)^{-1}\,\mathrm{Im}\,[\bar{\rho}v_k^2] \tag{46b}$$

Eqn. 46*b* is zero at the frequency points where $\rho = 0$ or equivalently $|v_n|$ attains maximum bound. This is just the well known zero-sensitivity property for doubly terminated ladders. An alternative derivation of eqn. 46 based on a topological approach is given elsewhere [31].

4.3 Application to digital and active networks

In the following Sections it will be shown that the system in eqn. 11 can be simulated by digital or active networks. For digital simulations, even in non-ideal cases, it is still possible to keep deviations in Y symmetric by carefully selecting the coefficient quantisations, so the zero-sensitivity property can be preserved. For active-RC and SC simulations, it is difficult to keep deviations of Y symmetric, since the element value drift is a random phenomenon. The component drift may cause the equivalent system description (eqn. 11) to become nonsymmetric, so that the output may exceed the bound given by eqn. 23 or 34. However, in practical active-RC or SC implementations, low sensitivity is still observed, a property due to the multifeedback nature of the structures. Eqns. 41*a* and *b* are valid for these general cases.

5 Discrete symmetric matrix systems

The results in the previous Section can be readily extended to the discrete domain if a bilinear transformation is applied to the system in eqn. 11

$$YV = J \tag{47a}$$

with

$$Y = \Psi C + \Psi^{-1}\Gamma + G \tag{47b}$$

where

$$\Psi = \frac{2}{T}\frac{1 - z^{-1}}{1 + z^{-1}} \tag{47c}$$

Eqn. 47 can be rearranged as

$$(P + z^{-1}Q + z^{-2}R)V = (1 - z^{-2})J \tag{48a}$$

with

$$P = \left(\frac{2}{T}C + \frac{T}{2}\Gamma + G\right)$$

$$Q = -2\left(\frac{2}{T}C - \frac{T}{2}\Gamma\right) \tag{48b}$$

$$R = \left(\frac{2}{T}C + \frac{T}{2}\Gamma - G\right)$$

which can be seen as a generalised form of the standard state-space equation (eqn. 4), by introducing a second-order term.

As bilinear transformation will keep the stability property and map the imaginary axis in the s domain to the unit circle in the z domain, it is easy to show:

Remark: The system in eqn. 47 has no poles outside the unit circle $z = e^{j\omega T}$ if C, Γ and G are all symmetric non-negative and has the same boundedness and sensitivity properties as indicated by theorems 1 and 2, except that eqn. 47 is evaluated on the unit circle $z = e^{j\omega T}$.

As indicated in Section 2, the pseudopassive property is of particular interest for discrete systems in order to suppress parasitic oscillations. Consider the problem of constructing a pseudopassive state-space system from eqn. 47, which can be written in an equivalent form

$$\left(\frac{2}{T}C + \frac{T}{2}\Gamma + G\right)V + \left(\frac{2}{T}\frac{-2z^{-1}}{1+z^{-1}}C + \frac{T}{2}\frac{2z^{-1}}{1-z^{-1}}\Gamma\right)V = J \tag{49}$$

Let C and Γ be decomposed into symmetric forms.

$$\frac{2}{T}C = L_C L_C^T \quad \frac{T}{2}\Gamma = L_\Gamma L_\Gamma^T \tag{50a}$$

Define

$$X = \begin{bmatrix} X_C \\ X_\Gamma \end{bmatrix} = \begin{bmatrix} \frac{2z^{-1}}{1+z^{-1}}L_C \\ \frac{-2z^{-1}}{1-z^{-1}}L_\Gamma \end{bmatrix} V \tag{50b}$$

From eqns. 49 and 50

$$V = \left(\frac{2}{T}C + \frac{T}{2}\Gamma + G\right)^{-1}\left\{[L_C\, L_\Gamma]\begin{bmatrix} X_C \\ X_\Gamma \end{bmatrix} + J\right\} \tag{51}$$

Substituting eqn. 51 into eqn. 50 we get a state-space description

$$X = z^{-1}AX + z^{-1}BU \tag{52}$$

with

$$A = 2\begin{bmatrix} L_C^T \\ -L_\Gamma^T \end{bmatrix}\left(\frac{2}{T}C + \frac{T}{2}\Gamma + G\right)^{-1}[L_C\, L_\Gamma] + \begin{bmatrix} -I & \\ & I \end{bmatrix} \tag{53a}$$

$$B = \begin{bmatrix} L_\Gamma^T \\ -L_\Gamma^T \end{bmatrix}\left(\frac{2}{T}C + \frac{T}{2}\Gamma + G\right)^{-1} \tag{53b}$$

Theorem 3: $\|A\| \leqslant 1$ if C, Γ and G are non-negative.

Proof: First, only if C and Γ are both non-netative can the decompositions of eqn. 5 be carried out. Substantial manipulation of eqns. 50 and 53a gives

$$A^TA = \begin{bmatrix} I & \\ & I \end{bmatrix} - 4\begin{bmatrix} L_C^T \\ L_\Gamma^T \end{bmatrix}\left(\frac{2}{T}C + \frac{T}{2}\Gamma + G\right)^{-T} G \times \left(\frac{2}{T}C + \frac{T}{2}\Gamma + G\right)^{-1}[L_C\, L_\Gamma] \tag{54}$$

From eqns. 51 and 54 it can be seen that the following relationships hold when $J = [0]$:

$$x^T(n)A^TAx(n) = x^T(n)x(n) - v^T(n)Gv(n) \tag{55a}$$

If G is non-negative, then $v^T(n)Gv(n)$ is a non-negative number, and therefore

$$x^T(n)A^TAx(n) \leqslant x^T(n)x(n) \tag{55b}$$

no matter what the value of $x(n)$. The theorem follows from eqns. 7 and 9. Incidentally, from eqn. 54 it can be seen that matrix A is orthogonal if $G = [0]$.

Conditions for the continuous time-domain systems have no direct practical applications; however, for completeness a derivation is given in 10.2 Appendix.

6 Circuit implementations

In the previous Sections effort has been given to the investigation of the theoretical properties of symmetric matrix systems (eqn. 11) and their discrete form (eqn. 47). Now the circuit implementations of these systems by various techniques, general *RLC* networks, active-*RC*, *SC* and digital networks, are considered. The discussion is brief as *RLC* and wave circuit designs are well known and matrix methods for circuit design have presented in other recent publications.

6.1 General passive RLC implementations

Eqn. 11 can always be derived from a nodal-voltage or loop-current formulation of a passive *RLC* network. In a nodal-voltage approach the contribution of every component is indicated by eqn. 43. The reverse procedure, from an equation with symmetric non-negative matrices to a network, is not always possible unless negative element values are allowed. Advantage can be gained by permitting negative elements [7], as regular structures easier for fabrication may result. According to the last Section, negative elements would not appear to cause any special sensitivity problems.

6.2 Active-RC circuit implementations

Let matrices C and Γ in eqn. 11 be decomposed into the form, $C = L_C L_C^T$, $\Gamma = L_\Gamma L_\Gamma^T$. Then eqn. 11 can be written as the left-LUD form

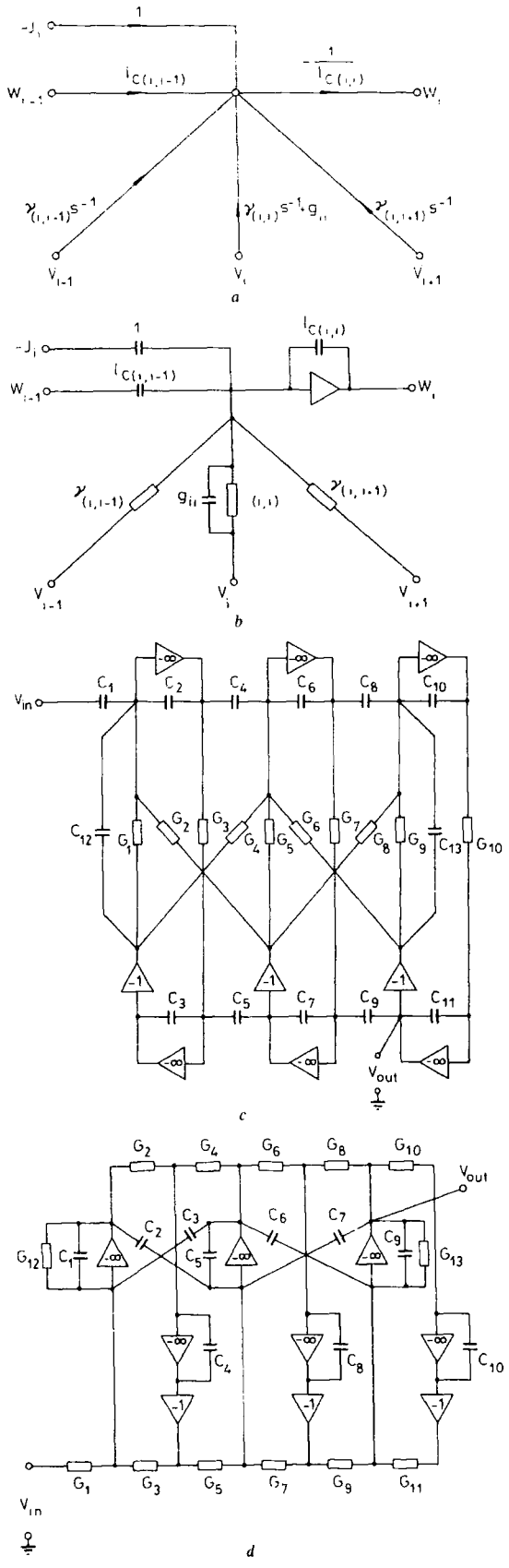
$$\begin{cases} L_C W = -(s^{-1}\Gamma + G)V + J & (56a) \\ L_C^T V = s^{-1}W & (56b) \end{cases}$$

or the right-LUD form

$$\begin{cases} (sC + G)V = -L_\Gamma U + J & (57a) \\ U = s^{-1}L_\Gamma^T V & (57b) \end{cases}$$

Both eqns. 56 and 57 can be realised directly by active-*RC* circuits. Every non-zero entry is realised by a corresponding element. To illustrate the implementation technique, consider a typical row equation in eqn. 56a

$$(l_{c(i,\,i-1)} + l_{c(i,\,i)})w_i = -s^{-1}[\gamma_{(i,\,i-1)}v_{i-1} + \gamma_{(i,\,i)}v_i + \gamma_{(i,\,i+1)}v_{i+1}] + g_{ii}v_i + J_i \tag{58}$$



This can be represented by a signal-flow graph (SFG) (Fig. 2*a*) and the corresponding active circuit, (Fig. 2*b*). The overall active-*RC* simulations of the passive prototype (Fig. 1) are shown in Figs. 2*c* and *d*.

In an example of sensitivity analysis for a right-LUD form (eqn. 57), ξ corresponds to a single entry c_{ij} in $\boldsymbol{C}$. then from eqn. 41*a*

$$dv_n/dc_{ij} = (2g_{nn}\bar{v}_n)^{-1}(-\bar{\rho}\boldsymbol{V}^T + \boldsymbol{V}^*)j\omega\, d\boldsymbol{C}/d\xi\, \boldsymbol{V}$$
$$= (2g_{nn}\bar{v}_n)^{-1} j\omega(-\bar{\rho}v_i v_j + \bar{v}_i v_j) \quad (59)$$

Similar formulas can be derived in the same way for other elements.

For the lowpass case, the right-LUD system (eqn. 57) results in identical circuit structures to those derived from a leapfrog approach. The left-LUD simulation (eqn. 56) has a significant advantage for elliptic transfer functions in that there are no capacitor-coupled op amp loops in the circuit implementation. The right-LUD simulation may produce such loops, and high-frequency oscillations may exist in these loops, resulting in undesirable noise problems.

6.3 Switched capacitor circuit implementations

Eqn. 47 is equivalent to

$$\left(\boldsymbol{P} + 4\frac{-1}{(1-z^{-1})}\frac{z^{-1}}{(1-z^{-1})}\frac{T}{2}\,\boldsymbol{\Gamma} + 2\frac{z^{-1}}{1-z^{-1}}\boldsymbol{G}\right)\boldsymbol{V} = \frac{1+z^{-1}}{1-z^{-1}}\boldsymbol{J} \quad (60)$$

As matrix $\boldsymbol{P}$ is always symmetric, it can be decomposed into the form

$$\boldsymbol{P} = \boldsymbol{L}_p\boldsymbol{L}_p^T \quad (61)$$

Similar to active-*RC* design, eqn. 60 can be written in the left-LUD form

$$\begin{cases} \boldsymbol{L}_p\boldsymbol{W} = -\left(\dfrac{2}{1-z^{-1}}\dfrac{T}{2}\boldsymbol{\Gamma} + 2\boldsymbol{G}\right)\boldsymbol{V} + (1+z)\boldsymbol{J} & (62a) \\ \boldsymbol{L}_p^T\boldsymbol{V} = \dfrac{2z^{-1}}{1-z^{-1}}\boldsymbol{W} & (62b) \end{cases}$$

or the right-LUD form (with $\boldsymbol{L}_\Gamma\boldsymbol{L}_\Gamma^T = T/2\,\boldsymbol{\Gamma}$)

$$\begin{cases} \boldsymbol{P}\boldsymbol{V} = -\dfrac{2}{1-z^{-1}}(\boldsymbol{L}_\Gamma\boldsymbol{U} + \boldsymbol{G}\boldsymbol{V}) + \dfrac{1+z^{-1}}{1-z^{-1}}\boldsymbol{J} & (63a) \\ \boldsymbol{U} = \dfrac{2z^{-1}}{1-z^{-1}}\boldsymbol{L}_\Gamma^T\boldsymbol{V} & (63b) \end{cases}$$

A number of new realisations have been derived in References 20–21. Here only an application of adopting negative elements in the prototype design is discussed. When the prototype relation (eqn. 11) is produced by nodal-

Fig. 2

a SFG representation of a continuous domain equation
b Corresponding active-RC realisation
c Left-LUD type active-RC realisation
d Right-LUD type active-RC realisation

voltage simulation of a passive ladder, matrix P, given by eqn. 48, is generally not diagonal. The design procedures according to eqn. 62 or 63 require cross-coupling capacitors to realise the non-zero off-diagonal entries of P. However, in an all-pole case, negative elements can be introduced to simplify the circuit structure. If every series-inductor branch L_i in a Chebyshev ladder has a parallel negative capacitor, C_i, added according to the relation

$$\frac{2}{T} C_i = -\frac{T}{2} \frac{1}{L_i} \tag{64}$$

This is shown by dotted lines in Fig. 3*a*. Then, from eqn. 48*b*, it can be verified that the off-diagonal entries of C

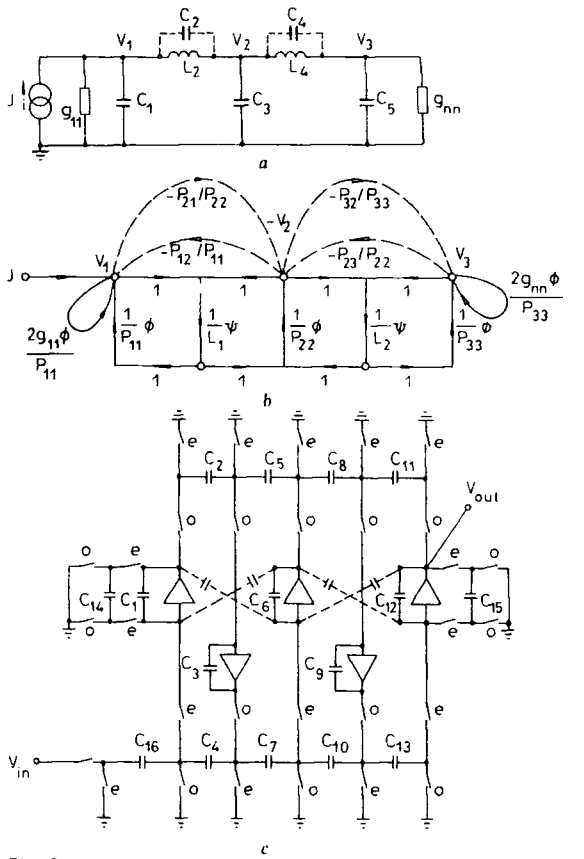


Fig. 3

a Terminated all-pole LC ladder prototype
Component values for normalised ladder
$C_1 = 0.93106$ $C_2 = -0.073694$ $L_2 = 1.4326$
$C_3 = 1.9453$ $C_4 = -0.071313$ $L_4 = 1.4804$
$C_5 = 1.5760$ $g_{11} = g_{nn} = 1$
b Leapfrog (or right-LUD) simulation

$$\psi = \frac{z^{-1}}{1 - z^{-1}}$$

$$\phi = \frac{-2T}{1 - z^{-1}}$$

c Leapfrog SCF simulation of the circuit in Fig. 3A
Capacitance values for the SC ladder
$C_1 = C_2 = C_{10} = C_{11} = C_{15} = 1$
$C_3 = 3.410$ $C_4 = 1.658$ $C_5 = 1.352$
$C_6 = 3.125$ $C_7 = 1.194$ $C_8 = 1.846$
$C_9 = 4.029$ $C_{12} = 1.925$ $C_{13} = 1.769$
$C_{14} = 1.072$ $C_{16} = 1.547$

and Γ will cancel each other and make P diagonal. This will remove the coupling capacitor in the simulation and save on the fabrication cost. However, zeros are introduced by these series branches and are given by

$$s^2 = \frac{-1}{L_i C_i} = \frac{4}{T^2} \tag{65}$$

A response error is thereby incurred, but this can be eliminated in the approximation procedure, by placing transmission zeros on the real axis. Examples of a right-LUD SFG and *SC* circuit are shown in Fig. 3*b* and *c*. The input stage is modified to realise $z^{-1}/(1 - z^{-1})$. The resulting distortion is compensated, together with that caused by real zeros. The response is shown in Fig. 4. If

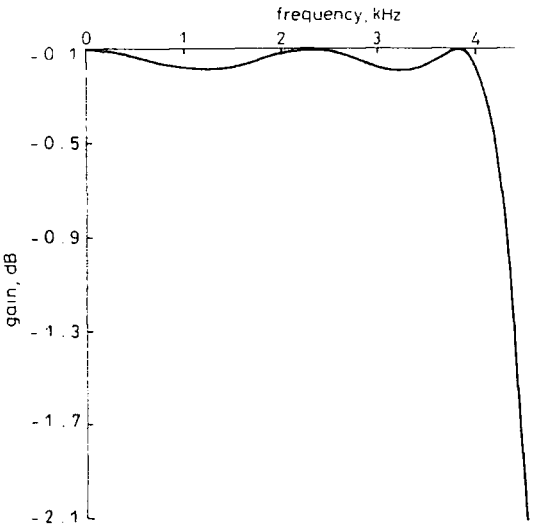


Fig. 4 *Simulated response of the circuit in Fig. 3C*

the off-diagonal entries of P are not zero, then the dotted branches in the SFG and the *SC* circuit would be required. Notice that in this lowpass case the right-LUD structure corresponds with that produced by a leapfrog approach.

6.4 Digital implementations

6.4.1 Matrix method: Eqn. 52 has already given one realisation of the system (eqn. 47). Direct implementation of the multiplication of X and U by A and B can require a high number of multiplications and additions, as usually A and B are full matrices. If A and B are decomposed according to eqn. 53, the multiplications of A and B are then carried out by a sequence of multiplications by factors. Efficiency is achieved by taking into consideration matrix sparsity. Numerical methods, such as LU factorisation, can be employed in the multiplications by $(2/T\,C + T/2\,\Gamma + G)^{-1}$ (Fig. 5*a*). This method could have advantages for implementation on concurrent array processors. However, for conventional single-processor implementation an excessive number of multiplications are required.

Digital structures can also be derived from eqn. 62, since there are no delay-free loops in the corresponding signal-flow graph (Fig. 5*b*). This approach has advantages concerning the properties of sensitivity behaviour, parallelism and the ability to be pipelined [22]. However, no efficient way to suppress parasitic oscillation for this type of structure has yet been found. As pseudopassivity is only a sufficient condition for limit-cycle suppression, a possible solution should not be ruled out.

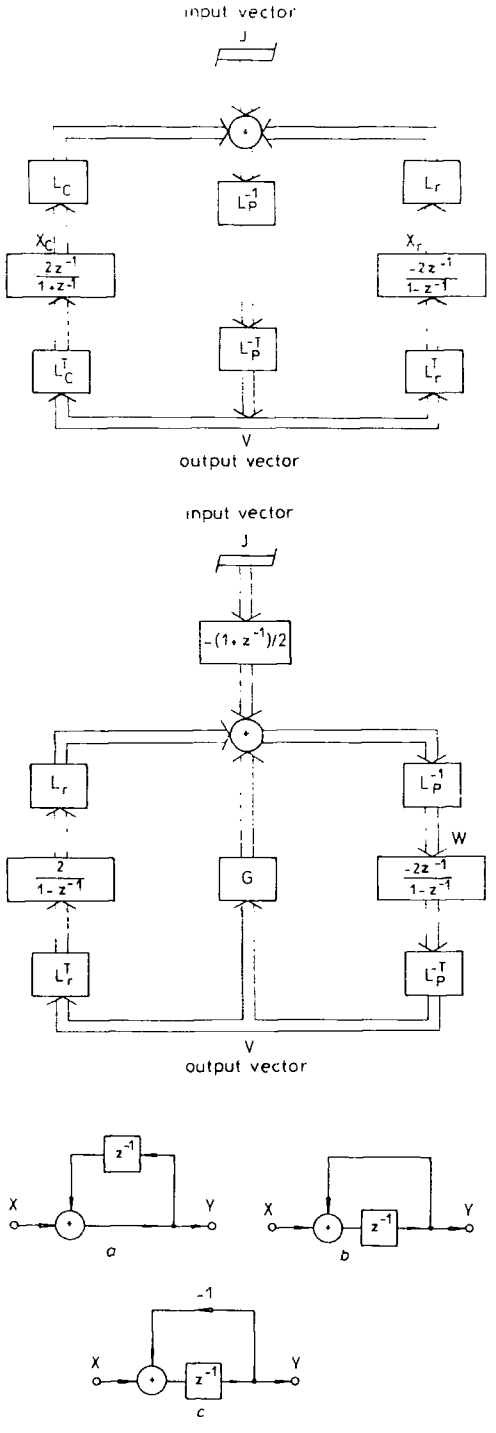


Fig. 5

a Block realisation of wave-related structure
b Block realisation of LDI-related structure
c Realisation of frequency-dependent factors

$a\ Y = \frac{1}{1 - z^{-1}} X$

$b\ Y = \frac{z^{-1}}{1 - z^{-1}} X$

$c\ Y = \frac{z^{-1}}{1 + z^{-1}} X$

6.4.2 Topological method: As indicated above, the prototype system (eqn. 11) can always be realised by a general passive *RLC* ladder. Consequently, a indirect realisation of system (eqn. 47) can be

(i) determine eqn 11 from eqn. 47 according to the bilinear transformation relationship

(ii) construct a general passive circuit from eqn. 11

(iii) design a wave digital circuit from the general passive circuit.

In Appendix 10.3 it is shown that the rounding of wave variables is equivalent to the rounding of the state variables given by eqn. 50 to keep the pseudopassivity property of the system. This agrees with the early theories of wave circuits using the property of adaptors. It can also be shown that the wave approach represents a special decomposition of matrices A, B in a topological way.

The results of this paper can also be applied to the circuits containing not only adaptors. For example, a standard wave circuit may require a excessive number of delays [25]. Techniques have been proposed for the design of wave filters with a canonical number of delays [9], resulting in a circuit structure which does not follow the rules of the connection of adaptors [25]. But, according to the discussion of Section 5 and Appendix 10.3, provided rounding is carried out at the points where wave variables can be accessed, limit cycles can still be suppressed.

It is interesting to point out that the discrete system (eqn. 47) can be rearranged into two equivalent forms, that of eqn. 49 and that of eqn. 60. Using these two different forms as the basis of derivation produces two major families of circuits, wave [8] and LDI [11]. In wave approaches the basic frequency-dependent factors are $-z^{-1}/(1 - z^{-1})$ and $z^{-1}/(1 + z^{-1})$ (Appendix 10.3). On the other hand, in LDI approaches the basic frequency-dependent factors are $-1/(1 - z^{-1})$ and $z^{-1}/(1 - z^{-1})$, as shown in eqn. 60 which can be seen as a stable and exact LDI-type realisation. The system expression of eqn. 49 involves matrices P, C and Γ, whereas that of eqn. 60 involves matrices P, Γ and G. Usually, matrix C is more complicated than G. Therefore, implementation based on eqn. 60 may result in simpler structures. However, no simple method for oscillation suppression has been found for standard LDI-type [11–12] digital structures nor for the exact structures based on eqn. 60. Therefore, structures based on eqn. 49 are suitable for digital design, if both sensitivity and noise due to number-truncation-induced oscillations are considered. Realisations based on eqn. 60 are interesting for other discrete systems, in particular for SC filter design, due to the fact that the two LDI factors coincide with the transfer functions of a pair of stray-insensitive integrators, resulting in efficient fabrications [6].

7 Conclusions

A family of low-sensitivity/noise systems have been studied for both continuous and discrete filter design. It is shown that symmetric matrix systems can be designed with optimal performance. Sensitivity can be minimised if the deviation of component values is kept symmetric, which is possible for a digital-filter design by carefully selecting the coefficient truncations. In fact, it can be proved that for some structures like wave circuits the coefficient truncations will always result in symmetric deviations.

For active-*RC* and *SC* circuits, asymmetric deviations may occur. Efficient sensitivity analysis and optimisation can thus be carried out utilising theorem 2.

The matrix decomposition method for filter design is the subject of continuing research and other articles will describe the application of these theoretical studies to the practical synthesis of traditional and novel circuit structures.

8 Acknowledgments

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10 Appendix

10.1 Derivation of the perturbed system output equation

Commence with

$$\boldsymbol{YU} = \boldsymbol{K} \tag{66}$$

Left multiply by $\boldsymbol{V}^*$ gives

$$\boldsymbol{V}^*\boldsymbol{YU} = \boldsymbol{V}^*\boldsymbol{K} \tag{67}$$

Note that when $\boldsymbol{J}$ is a real vector

$$\begin{aligned}(\boldsymbol{V}^*\boldsymbol{Y})^T &= \boldsymbol{Y}\bar{\boldsymbol{V}} = (j\boldsymbol{Q} + \boldsymbol{G})\bar{\boldsymbol{V}} \\ &= -(-j\boldsymbol{Q} + \boldsymbol{G})\bar{\boldsymbol{V}} + 2\boldsymbol{G}\bar{\boldsymbol{V}} \\ &= 2\boldsymbol{G}\bar{\boldsymbol{V}} - \boldsymbol{J} \\ &= (2g_{11}\bar{v}_1 - J_1, 0, \ldots, 0, 2g_{nn}\bar{v}_n)^T \\ &= (\bar{\rho}J_1, 0, \ldots, 0, 2g_{nn}\bar{v}_n)^T\end{aligned} \tag{68}$$

Substitute eqn. 68 into eqn. 67 and make some rearrangement to get

$$2g_{nn}\bar{v}_n u_n - \bar{\rho}J_1 u_1 + \boldsymbol{V}^*\boldsymbol{K} = 0 \tag{69}$$

Again left multiplying eqn. 66 by $\boldsymbol{V}^T$ and noticing that $\boldsymbol{V}^T\boldsymbol{Y} = \boldsymbol{J}^T = [J_1, 0, \ldots, 0]$ we have

$$\boldsymbol{V}^T\boldsymbol{K} = \boldsymbol{V}^T\boldsymbol{YU} = \boldsymbol{J}^T\boldsymbol{U} = J_1 u_1 \tag{70}$$

Eqn. 39 follows by substituting eqn. 70 into eqn. 69.

10.2 Continuous time-domain pseudopassive systems

We first show that a continuous time system (eqn. 3) is pseudopassive if $-(\boldsymbol{A} + \boldsymbol{A}^T)$ is non-negative. Set $\boldsymbol{J} = \boldsymbol{0}$ in eqn. 11. Then the time-domain solution is given by

$$\boldsymbol{x}(t) = \exp(\boldsymbol{A}t)\boldsymbol{x}_0 \tag{71}$$

where $\boldsymbol{x}_0$ is the initial value vector. Take the derivative of $e(t) = \boldsymbol{x}^T(t)\boldsymbol{x}(t)$

$$de/dt = \boldsymbol{x}_0^T \exp(\boldsymbol{A}t)^T(\boldsymbol{A} + \boldsymbol{A}^T)t \exp(\boldsymbol{A}^T t)\boldsymbol{x}_0 \tag{72}$$

$e(\boldsymbol{x}(t))$ is monotonically decreasing if $de/dt \leqslant 0$, or equivalently, the system in eqn. 11 is pseudopassive if $-(\boldsymbol{A} + \boldsymbol{A}^T)$ is non-negative.

Let a state space system $\boldsymbol{X} = s^{-1}\boldsymbol{AX} + \boldsymbol{L}_C^{-1}\boldsymbol{J}$ be constructed from eqn. 11 by

$$\boldsymbol{X} = \begin{pmatrix}\boldsymbol{X}_C \\ \boldsymbol{X}_L\end{pmatrix} = \begin{pmatrix}\boldsymbol{L}_C^T \\ \boldsymbol{L}_\Gamma^T\end{pmatrix}\boldsymbol{V} \tag{73}$$

with

$$\boldsymbol{C} = \boldsymbol{L}_C\boldsymbol{L}_C^T \quad \boldsymbol{\Gamma} = \boldsymbol{L}_\Gamma\boldsymbol{L}_\Gamma^T \tag{74a}$$

and

$$\boldsymbol{A} = \begin{bmatrix}-\boldsymbol{L}_C^{-1}\boldsymbol{G}\boldsymbol{L}_C^{-T} & -\boldsymbol{L}_C^{-1}\boldsymbol{L}_\Gamma \\ \boldsymbol{L}_\Gamma^T\boldsymbol{L}_C^{-T} & \boldsymbol{0}\end{bmatrix} \tag{74b}$$

It is easily seen that

$$-(\boldsymbol{A}+\boldsymbol{A}^T)=2\begin{bmatrix}\boldsymbol{L}_C^{-1}\boldsymbol{G}\boldsymbol{L}_C^{-T} & \boldsymbol{0}\\ \boldsymbol{0} & \boldsymbol{0}\end{bmatrix} \tag{75}$$

is non-negative. The pseudopassivity of eqn. 73 follows immediately.

10.3 Wave variables

When eqn. 11 is derived from a passive ladder by nodal formulation, the matrices can be generated by topological means [26]

$$\boldsymbol{C}=\boldsymbol{A}_C\boldsymbol{D}_C\boldsymbol{A}_C^T \tag{76a}$$

$$\boldsymbol{\Gamma}=\boldsymbol{A}_\Gamma\boldsymbol{D}_\Gamma\boldsymbol{A}_\Gamma^T \tag{76b}$$

where $\boldsymbol{D}_C$ and $\boldsymbol{D}_\Gamma$ are diagonal branch-admittance matrices with entries consisting of the corresponding capacitance or inverse inductance values. $\boldsymbol{A}_C$ and $\boldsymbol{A}_\Gamma$ are the corresponding incidence matrices. Let $\boldsymbol{V}_C$, $\boldsymbol{I}_C$, $\boldsymbol{V}_\Gamma$ and $\boldsymbol{I}_\Gamma$ be vectors of the voltages and currents of the capacitance and inductance branches, respectively, then the voltage vectors are related to the nodal-voltage vector $\boldsymbol{V}$ by

$$\boldsymbol{V}_C=\boldsymbol{A}_C^T\boldsymbol{V} \tag{77a}$$

$$\boldsymbol{V}_\Gamma=\boldsymbol{A}_\Gamma^T\boldsymbol{V} \tag{77b}$$

The current vectors are related to the nodal-voltage vector by

$$\boldsymbol{I}_C=\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}\boldsymbol{D}_C\boldsymbol{A}_C^T\boldsymbol{V} \tag{78a}$$

$$\boldsymbol{I}_\Gamma=\frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}}\boldsymbol{D}_\Gamma\boldsymbol{A}_\Gamma^T\boldsymbol{V} \tag{78b}$$

According to the definition of wave variables: incident wave vectors are

$$\boldsymbol{W}_{CI}=\boldsymbol{V}_C+\left(\frac{2}{T}\boldsymbol{D}_C\right)^{-1}\boldsymbol{I}_C=\frac{2}{1+z^{-1}}\boldsymbol{A}_C^T\boldsymbol{V} \tag{79a}$$

$$\boldsymbol{W}_{\Gamma I}=\boldsymbol{V}_\Gamma+\left(\frac{T}{2}\boldsymbol{D}_\Gamma\right)^{-1}\boldsymbol{I}_\Gamma=\frac{2}{1-z^{-1}}\boldsymbol{A}_\Gamma^T\boldsymbol{V} \tag{79b}$$

and reflected wave vectors are

$$\begin{aligned}\boldsymbol{W}_{CR}&=\boldsymbol{V}_C-\left(\frac{2}{T}\boldsymbol{D}_C\right)^{-1}\boldsymbol{I}_C\\&=\frac{2z^{-1}}{1+z^{-1}}\boldsymbol{A}_C^T\boldsymbol{V}=z^{-1}\boldsymbol{W}_{CI}\end{aligned} \tag{80a}$$

$$\begin{aligned}\boldsymbol{W}_{\Gamma R}&=\boldsymbol{V}_\Gamma-\left(\frac{T}{2}\boldsymbol{D}_\Gamma\right)^{-1}\boldsymbol{I}_\Gamma\\&=\frac{-2z^{-1}}{1-z^{-1}}\boldsymbol{A}_\Gamma^T\boldsymbol{V}=-z^{-1}\boldsymbol{W}_{\Gamma I}\end{aligned} \tag{80b}$$

By comparing eqns. 50, 76 and 80 it can be found that

$$\begin{aligned}\boldsymbol{x}^T(n)\boldsymbol{x}(n)=&\boldsymbol{w}_{CR}^T(n)\frac{2}{T}\boldsymbol{D}_C\boldsymbol{w}_{CR}(n)\\&+\boldsymbol{w}_{\Gamma R}^T(n)\frac{T}{2}\boldsymbol{D}_\Gamma\boldsymbol{w}_{\Gamma R}(n)\end{aligned} \tag{81}$$

When the branch admittance matrices $\boldsymbol{D}_C$ and $\boldsymbol{D}_\Gamma$ are diagonal with positive element values, the magnitude rounding of $\boldsymbol{w}_{CR}$ and $\boldsymbol{w}_{\Gamma R}$ will have the same effect as magnitude rounding on $\boldsymbol{x}(n)$ to cause a reduction of $\boldsymbol{x}^T(n)\boldsymbol{x}(n)$.

PAPER 40

400 MHz SWITCHING RATE GaAs SWITCHED CAPACITOR FILTER

Indexing terms: Filters, Gallium arsenide, Integrated circuits

The letter presents experimental results for a second order switched capacitor bandpass filter designed to operate with a 250 MHz switching frequency and implemented using gallium arsenide (GaAs) technology. Measurements on a chip fabricated in a 0·5 μm GaAs process confirm that the filter design, amplifier and switching components meet the desired performance specifications. The filter operates with high precision at 300 MHz and bandpass filtering at a switching frequency of 400 MHz is demonstrated.

Introduction: Gallium arsenide (GaAs) technology has an important rôle in the realisation of high speed analogue sampled data systems.[1] Reference 2 describes the design and optimisation of a second order switched capacitor (SC) bandpass filter for implementation using GaAs technology and with a maximum design switching frequency of 250 MHz. Since Reference 2 was published, the filter chip described has been fabricated and very encouraging experimental results obtained. The objective of this paper is to report these results.

Switched capacitor filter design: The second order switched capacitor bandpass filter was designed to realise a Q-factor of 16, midband gain of unity and midband frequency of 1/25th of the switching frequency for a maximum switching frequency of 250 MHz.[2] The circuit used the single-stage, double-cascode, double-level-shifting operational amplifier design of Reference 3, which had a simulated gain of 60 dB, typical gain-bandwidth product of 3·5 GHz and a minimum settling time of 630 ps. The switch control circuit used is that of Reference 4, which features low power consumption and low signal dependence of clock feedthrough. The switch capacitor circuit was optimised for high frequency operation using the technique of References 2 and 5, whereby amplifier load capacitances are introduced to maintain acceptable settling behaviour and stability in all switching states. The filter architecture is shown in Fig. 1, where capacitors C_a, C_b and C_c have been introduced as a result of the optimisation procedure.

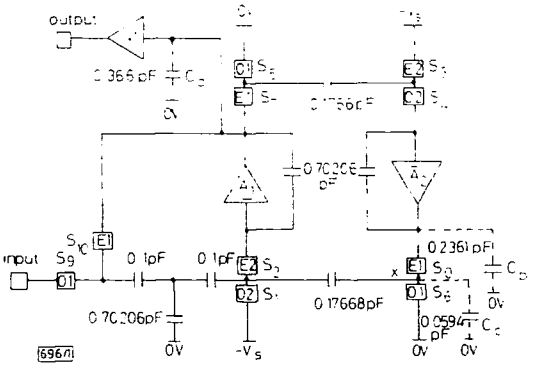

Fig. 1 *Second order SC filter for implementation*

The circuit was layed out using MAGIC with a specially written technology file for the Anadigics 0·5 μm GaAs process and a layout plot is shown in Fig. 2. The size of the chip, which was fabricated by Anadigics, is 3·3 × 2·6 mm and the power consumption is 440 mW.

Testing and experimental results: The chip was bonded within a dual-in-line package, which was mounted in a dual-in-line socket on a circuit board. The input signal level for all tests was +7 dBm, or 0·5 V RMS.

The filter was found to operate very accurately up to and beyond its design maximum switching frequency of 250 MHz. The amplitude/frequency response was measured for switching frequencies of 300 MHz, 350 MHz and 400 MHz. The responses for 300 MHz and 400 MHz are shown in Figs. 3*a* and *b*, respectively. Expanded passband plots for the above switching frequencies are shown in Figs. 4*a* and *b*. Peak gains,

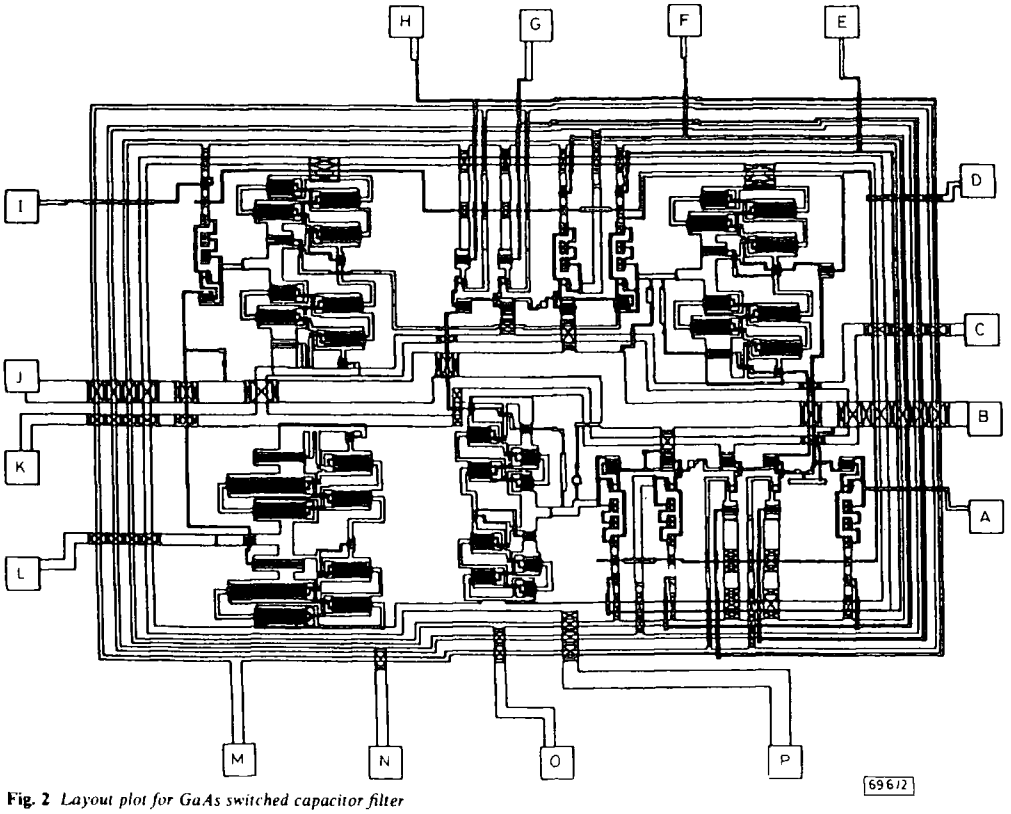

Fig. 2 *Layout plot for GaAs switched capacitor filter*
Total size = 3·3 × 2·6 mm

−3 dB frequencies and calculated midband frequencies and Q-values are tabulated in Table 1. Midband frequency accuracies range from less than 1% to about 2% and represent a considerable improvement over the previous results presented in Reference 6. The Q-factor accuracy is reasonable for a 300 MHz switching frequency, but the Q-factor is reduced for the higher switching frequencies. The noise at the output of the filter was measured for a measuring bandwidth of 10 kHz. The peak noise is at −75 dB relative to the maximum signal level. Observation of the filter output signal at the resonant frequency indicated a DC offset voltage of less than 50 mV and reasonably low levels of clock feedthrough. Future testing on an improved jig could improve these results.

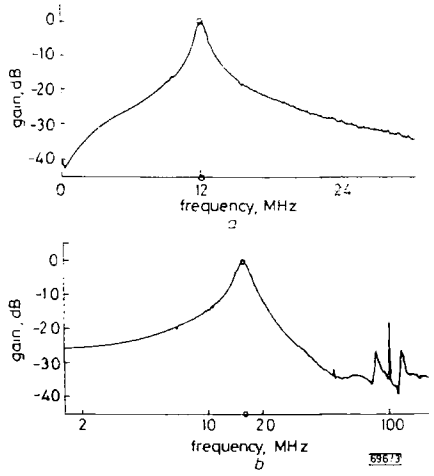

Fig. 3 *Measured amplitude/frequency response of filter*
a 300 MHz switching frequency
b 400 MHz switching frequency

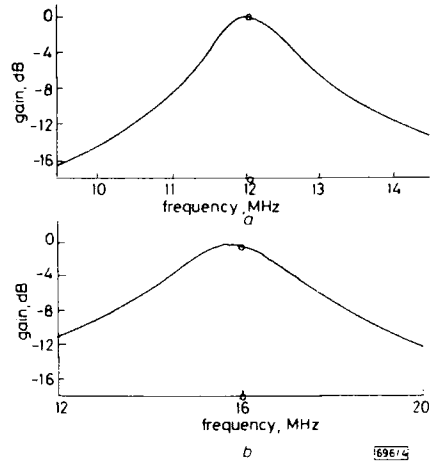

Fig. 4 *Measured expanded passband response*
a 300 MHz switching frequency
b 400 MHz switching frequency

Table 1 MEASURED FILTER PERFORMANCE DATA

Switching frequency	Peak gain	−3 dB frequencies		F_0	Q-factor
		F_1	F_2	$\sqrt{(F_1F_2)}$	$\frac{F_0}{F_2-F_1}$
MHz	dB	MHz	MHz	MHz	
300	−0·15	11·7	12·5	12·1	15
350	−0·20	13·5	14·7	14·1	12
400	−0·15	14·6	16·9	15·7	7

Conclusions: A significant increase in the maximum switching frequency for switched capacitor filters has been demonstrated. In spite of the results achieved, the operational amplifier used in the design is relatively slow compared with more recent designs[7] and advanced designs implemented using state-of-the-art technology.[8] This opens up future opportunities for SC systems operating with gigahertz clock rates.

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ON THE RELEVANCE OF THE STRICT AVALANCE CRITERION

Indexing terms: Codes, Boolean functions

Some recent work concerning the strict avalanche criterion for a Boolean function has been motivated by the claim that a certain cryptographically useful property will be true of any function satisfying the criterion. In the letter it is observed that not only is this claim untrue, but that possession of the property in question is in fact precluded by satisfaction of the strict avalanche criterion.

Definitions and motivation: Webster and Tavares[1] introduced the strict avalanche criterion (SAC) for a Boolean function to combine the concepts of completeness and the avalanche

PAPER 41

Active and digital ladder-based allpass filters

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Indexing terms: Filters and filtering, Circuit theory and designs

Abstract: Ladder-based allpass filters are extended for active *RLC*, active *RC*, SC and digital realisations. The resulting circuits have the attractive properties of parallel structure and very low amplitude sensitivity to component changes. The analogue implementations are canonical with respect to the number of op amps and the digital ones are multiplier canonic. Detailed examples are given for SC designs and these are critically assessed for capacitance spread and sensitivity.

1 Introduction

Allpass filters are primarily designed to provide phase characteristics and any interference with an existing magnitude response should be avoided. However, in practical realisations, the amplitude response will inevitably be influenced by component variations. It is important therefore to use circuits with low amplitude sensitivity characteristics. Because allpass functions are non-minimum phase by definition, low-sensitivity ladder-based design remains an open problem. Instead, cascaded biquad sections are typical in active and digital realisations, and such topologies are highly sensitive to component deviations, especially in high-Q cases [1–3].

A novel method for allpass digital filter design has recently been proposed [4, 6]. The allpass transfer function is decomposed into two terms: a constant and a function realisable as the driving point impedance of a passive network, which is, in turn, simulated by a digital circuit. The resulting system is structurally allpass, that is, wordlength truncation will not introduce any distortion into the amplitude response. Switched capacitor (SC) simulations of the Foster II structure used in Reference 4 are also known [5].

In this paper, a ladder-based approach is presented for the design of prototypes. The op amps can be made canonical in number for SC implementations, if the allpass equaliser and amplitude filter are considered together (this can also be insured in fully differential active-*RC* circuits). The new configurations are also very suitable for parallel digital circuit implementations and lead to circuits canonical in the number of delays.

Major emphasis will be placed on SC circuit realisations. Design examples are given and comparisons made between the different ladder-based structures and with cascade biquads. It will be demonstrated that the sensitivities of the amplitude responses of ladder systems are much lower than those of cascade biquad structures and that the sensitivities of the delay responses are similar for all realisations. Low capacitance spreads are also observed for ladder-based methods.

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2 Continuous domain allpass ladders

It can be shown [6] that an allpass function in the s-domain

$$H_a(s) = \pm \frac{P(-s)}{P(s)} \tag{1}$$

can be rearranged as

$$H_a(s) = \frac{1 - Y(s)}{1 + Y(s)} = 1 - \frac{2}{1 + Y(s)} \tag{2}$$

where

$$Y(s) = \begin{cases} \dfrac{\mathrm{Ev}P(s)}{\mathrm{Od}P(s)} & \text{if } n \text{ is even} \quad (3) \\ \dfrac{\mathrm{Od}P(s)}{\mathrm{Ev}P(s)} & \text{if } n \text{ is odd} \quad (4) \end{cases}$$

for the Hurwitz polynomial

$$P(s) = \mathrm{Ev}P(s) + \mathrm{Od}P(s) \tag{5}$$

A signal flow graph (SFG) is given in Fig. 1 for the realisation of eqn. 2, where the transfer function $1 + Y(s)$ can be synthetised by a singly terminated LC ladder. It is well-known that, if $P(s)$ is Hurwitz, then $Y(s) = \mathrm{Ev}P(s)/\mathrm{Od}P(s)$ can be expanded in continued fraction form and realised according to the ladder circuit of Fig. 2.

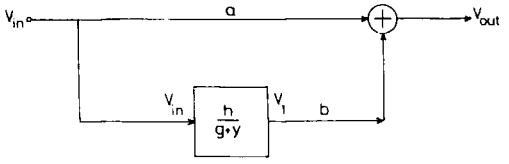

Fig. 1 *Realisation of allpass function*
For s-domain, $a = b = g = 1$, $h = -2$
For z-domain, $a = b = g = 1$, $h = -(1 + z)$

Traditionally, passive allpass filters are realised as cascaded lattice-derived bridged-T structures. Two major disadvantages are associated with this method. First, the amplitude response is sensitive to all components, and, secondly, the circuits are not canonical, requiring approximately $2.5n$ reactance elements in their implementation. For the scheme shown in Fig. 2, the amplitude response is completely insensitive to the deviation in the reactance elements (Section 4) and only n reactance elements are

required. The summing amplifier and several resistors are an extra cost.

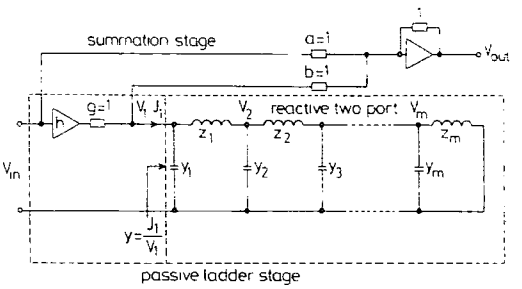

Fig. 2 *Active-RLC allpass circuit*

$z_i = \Phi^{-1}L_i$, $y_i = \Psi^{-1}C_i$
For s-domain, $\psi = s^{-1}$, $\Phi = s^{-1}$, $h = -2$
For z-domain, $\psi = z^{-1}/(1 - z^{-1})$, $\Phi = 1/(1 - z^{-1})$, $h = -(1 + z)$

2.1 Active RC ladder design

The passive ladder network part of the circuit of Fig. 2 can be simulated by active RC circuits. The nodal admittance matrix equation for the passive ladder subnetwork is

$$\left(sC + \frac{1}{s}\Gamma + G\right)V = J \tag{6}$$

where $J = [-ghv_{in}, 0, \ldots, 0]$ and C, Γ and G are admittance matrices formed by the contributions of capacitors, inductors and resistors, respectively. V is defined as $V = [v_1, -v_2, v_3, -v_4, \ldots]$, where alternate signs are introduced to insure that all entries in eqn. 6 are positive.

The matrix decomposition method for active RC network design described in References 9–11 can be readily applied here. Eqn. 6 can be written in the LUD form, (because all of the capacitors in Fig. 2 are connected to earth, C is simply diagonal and no real decomposition of C is necessary)

$$\begin{cases} W = -(s^{-1}\Gamma + G)V + J & (7a) \\ V = s^{-1}C^{-1}W & (7b) \end{cases}$$

or, from the topological decomposition of $\Gamma = A_L D_L A_L^T$, the leapfrog form results:

$$\begin{cases} (C + s^{-1}G)V = s^{-1}(-A_L W + J) & (8a) \\ W = s^{-1}D_L A_L^T V & (8b) \end{cases}$$

Both eqns. 7 and 8 are linearised with respect to s^{-1} so that they can be realised directly with active-RC circuits. For a sixth order circuit, the signal flow graphs (SFGs) of Figs. 3*a* and *b* (case A) and the simulation circuits of Figs. 4*a* and *b* (incorporating the summation stages) can be obtained. Inversion in the output stage is incorporated in the simulation part. Notice the different termination stages in LUD and leapfrog realisations.

The summing amplifier employed in the output stage in Fig. 4 need not be realised explicitly in delay equalised filter systems. Provided the allpass filter is succeeded by an amplitude filter stage, the virtual earth of the input integrator of the amplitude stage can be directly connected to P_v to realise the summation function. In a fully differential implementation, separate inverters are not required and thus realisations with a canonical number of op amps are possible.

3 Discrete domain allpass ladders

There are several approaches to the derivation of allpass ladders in the z-domain. In particular, it has been found

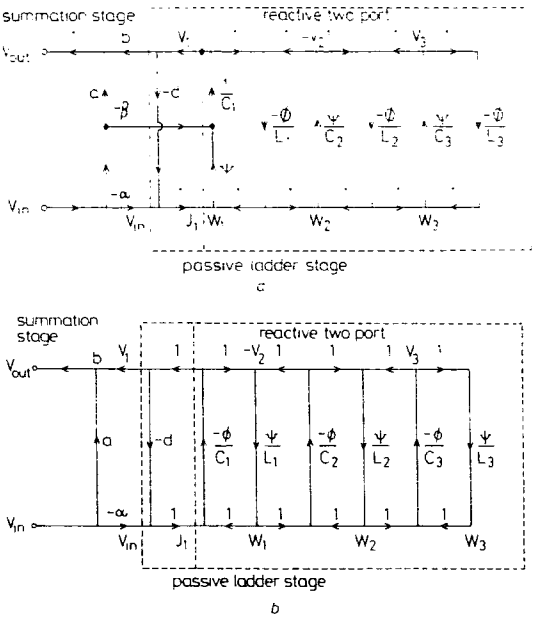

Fig. 3 *SFGs for allpass realisation*

a LUD type
Case A: s-domain
$\Phi = \psi = s^{-1}$, $a = b = d = g = 1$, $\alpha = 2$, $\beta = 0$
Case B: z-domain
$\Phi = 1/(1 - z)^{-1}$, $\psi = z^{-1}/(1 - z^{-1})$, $a = b = d = g = 1$, $\alpha = 2$, $\beta = 1$
Case C: z-domain
$\Phi = 1/(1 - z)^{-1}$, $\psi = z^{-1}/(1 - z^{-1})$, $a = \alpha = d = g = 1$, $b = 1 + z$, $\beta = 0$
b Leapfrog type
Case A: s-domain
$\Phi = \psi = s^{-1}$, $a = b = d = g = 1$, $\alpha = 2$
Case B: z-domain
$\Phi = 1/(1 - z^{-1})$, $\psi = z^{-1}/(1 - z^{-1})$, $b = 1 + z^{-1}$, $a = \alpha = d = g = 1$

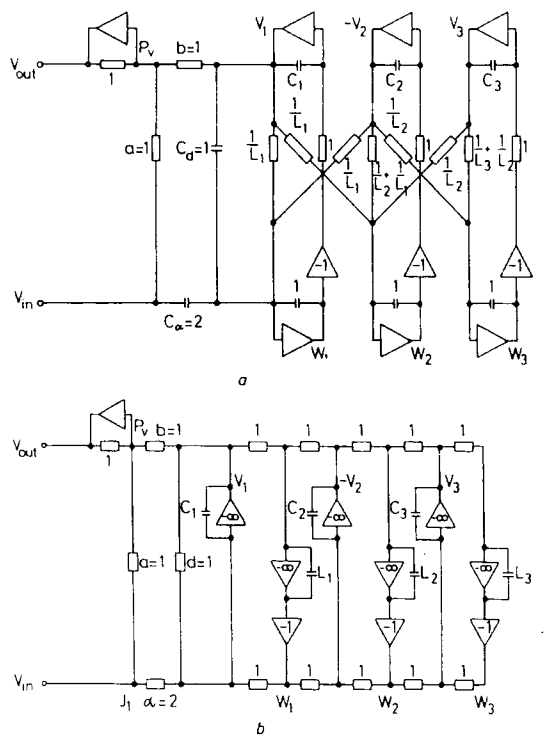

Fig. 4 *Active-RLC allpass filters (elements in μF and μS)*

a LUD type
b Leapfrog type

most efficient to use the so-called bilinear-LDI method, as it is both exact in frequency response and efficient in terms of implementation cost. Such a structure could be derived by the technique of Reference 11, which places real zeros in the ladder prototype to introduce the cancellation of capacitors after bilinear transformation. However, a more straightforward derivation is presented here, which uses a continued fraction expansion for z-domain transfer functions [6–8, 12].

3.1 LUD method for SC and digital ladder design

For an allpass function in z-domain

$$H_a(z) = \mp \frac{z^n P(z^{-1})}{P(z)} = 1 - \frac{1+z}{1 + \dfrac{zP(z) \pm z^n P(z^{-1})}{P(z) \mp z^n P(z^{-1})}}$$

$$= 1 - \frac{1+z}{1+Y(z)} \tag{9}$$

($-$sign for $n = 2m$, $+$sign for $n = 2m + 1$)

To avoid the noncausal term z in eqn. 9, the transfer function is modified to

$$z^{-1}H_a(z) = z^{-1} - \frac{1+z^{-1}}{1+Y(z)} \tag{10}$$

which introduces only a single extra delay. Define

$$\Phi = \frac{1}{1-z^{-1}} \qquad \Psi = \frac{z^{-1}}{1-z^{-1}} \tag{11}$$

The digital realisations of Ψ and Φ are shown in Fig. 5. The continued fraction expansion of $Y(z)$ can be achieved in terms of Ψ^{-1} and Φ^{-1} alternately [12]:

$$Y(z) = \Psi^{-1}C_1 + \cfrac{1}{\Phi^{-1}L_1 + \cfrac{1}{\Psi^{-1}C_2 + \cfrac{1}{\Phi^{-1}L_2 + \ddots \; \Psi^{-1}C_m + \cfrac{1}{\Phi^{-1}L_m}}}} \tag{12}$$

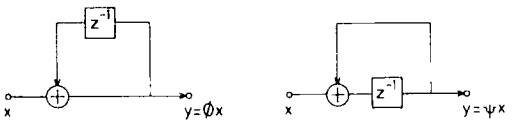

Fig. 5 *Digital realisations of Φ and Ψ*

For n odd, eqn. 12 will terminate with a $\Psi^{-1}C_{m+1}$ term. Positive values of $\{C_i\}$ and $\{L_i\}$ are guaranteed [12]. By analogy with eqn. 2, it can be seen that a ladder simulation is appropriate. The passive ladder part in Fig. 2 can again be used to realise eqn. 12 by means of a 'passive network', with admittance $y_i = \Psi^{-1}C_1$ and impedance $z_i = \Phi^{-1}L_i$. Although physically unrealisable, it can be used as prototype for SC and digital simulations. A nodal description can be set up for the ladder section of Fig. 2 in terms of Ψ and Φ:

$$\left(\frac{1}{\Psi}\boldsymbol{C} + \Phi\boldsymbol{\Gamma} + \boldsymbol{G}\right)\boldsymbol{V} = (1+z)\boldsymbol{J} \tag{13}$$

LUD SC and digital circuits can be obtained [9–11] by rewriting eqn. 13:

$$\begin{cases} \boldsymbol{W} = -(\Phi\boldsymbol{\Gamma} + \boldsymbol{G})\boldsymbol{V} + \alpha\boldsymbol{J} & (14a) \\ \boldsymbol{V} = \boldsymbol{C}^{-1}(\Psi\boldsymbol{W} + \beta\boldsymbol{J}) & (14b) \end{cases}$$

where $\alpha = 2$, $\beta = 1$. This can be again represented by an SFG, Fig. 3*a* (case B), including the output stage. Notice that the corresponding digital implementation is canonical with respect to both multiplier coefficients and delays. The SC realisation is straightforward, but this method results in a large capacitance spread. There is another realisation of eqn. 13, by choosing $\alpha = 1 + z$ and $\beta = 0$, Fig. 3*a* (case C) results. Note that α and b can be exchanged without affecting the overall transfer function. The corresponding SC circuit can be obtained by replacing the branches in the SFG by SC elements, see Fig. 6*a*. The single z^{-1} of eqn. 10 is realised by a rearrangement of switching in the sample-and-hold and other input/output circuitry. The sampled input from an even phase is transferred to the output summing amplifier during the subsequent odd phase. The unit delay is realised when the output is sampled in the even phase of the next clock period. This scheme usually results in a lower capacitance spread than for case B.

LUD type SC circuits will always require an even number of op amps, which is canonical for even order cases, but not for odd cases.

3.2 Leapfrog method for SC and digital ladder design

Use of 13 to derive directly the leapfrog type circuit causes difficulty in realisation of the termination terms. Instead, it is easy to verify the equivalence between eqn. 13 and the following system:

$$\left(\frac{1}{\Phi}\boldsymbol{C} + \Psi\boldsymbol{\Gamma} + \boldsymbol{G}\right)\boldsymbol{V} = z^{-1}\boldsymbol{J} \tag{15}$$

where

$$\boldsymbol{C}' = \boldsymbol{C} - \boldsymbol{G} \tag{16}$$

The right matrix decomposition structure can be derived [9–11] by rewriting eqn. 15. as

$$\begin{cases} (\boldsymbol{C}' + \Phi\boldsymbol{G})\boldsymbol{V} = \Phi(-\boldsymbol{A}_L\boldsymbol{W} + z^{-1}\boldsymbol{J}) & (17a) \\ \boldsymbol{W} = \Psi\boldsymbol{D}_L\boldsymbol{A}_L^T\boldsymbol{V} & (17b) \end{cases}$$

The SFG of Fig. 3*b* (case B) can be used to represent eqn. 17 and an illustration of SC replacement is given in Fig. 6*b*, which is comparable to an independently reported realisation [7]. Notice that the z^{-1} factor in eqn. 17*a* cancels the noncausal factor of $1 + z$ in eqn. 10.

Leapfrog SC simulation can always realise a circuit with a canonical number of op amps, provided the amplitude and allpass stages are considered together. However, for narrow band SC design, it will result in a larger total capacitance than the LUD method.

From Fig. 3*b* (case B), it is seen that there is a delay-free loop at the termination stage: $v_1 \rightarrow -g \rightarrow J_1 \rightarrow \Phi/c_1 \rightarrow v_1$. For a digital realisation this can be eliminated by the equivalent circuit transformation shown in Fig. 7. The resulting circuit is highly parallel

and requires only a canonical number of multipliers for digital implementation. The number of additions required is also relatively small (roughly $2n$). The digital leapfrog realisation requires one more delay than the equivalent canonical LUD realisation (case B).

racies in the values of $\{C_i\}$, $\{L_i\}$ and all unity-valued elements of Figs. 4 and 6 would affect the sensitivity.

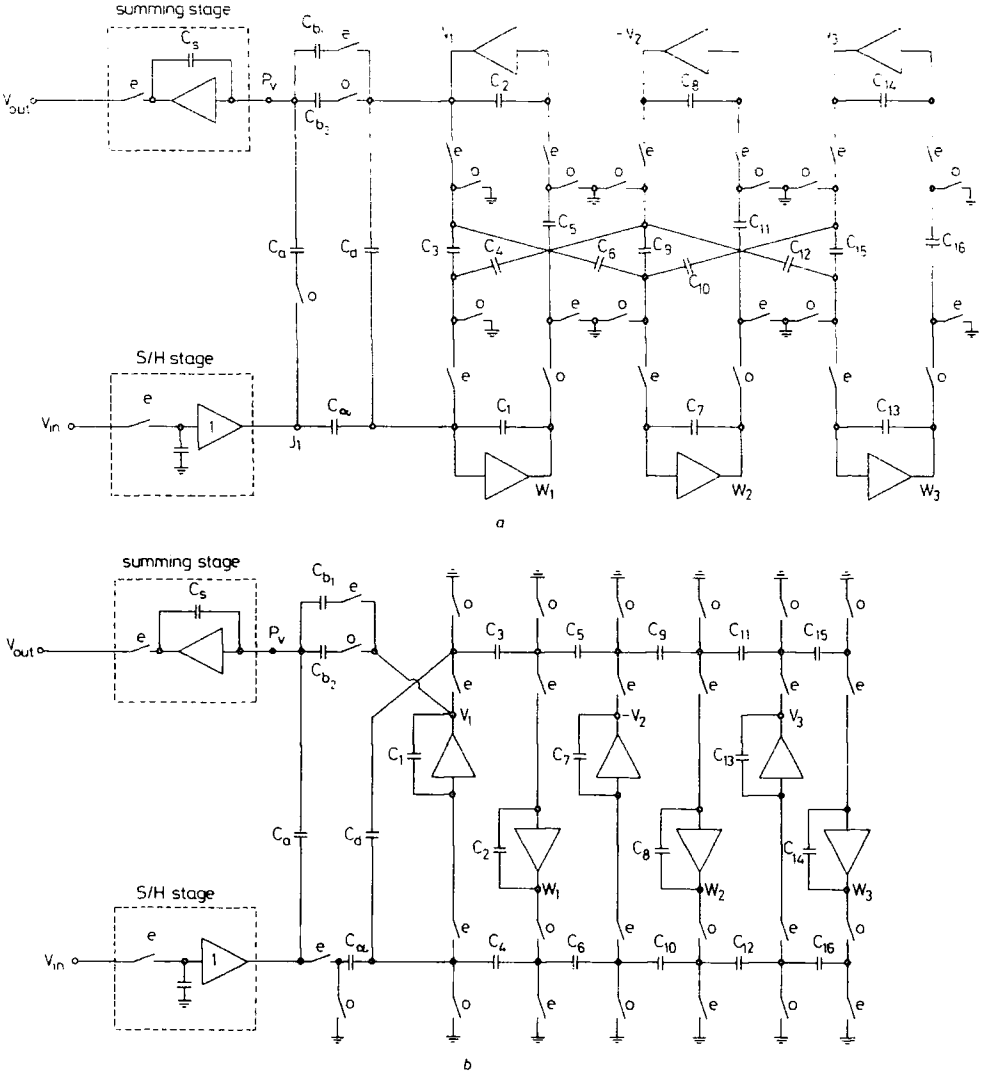

Fig. 6 *SC allpass filters*
a LUD type *b* Leapfrog type

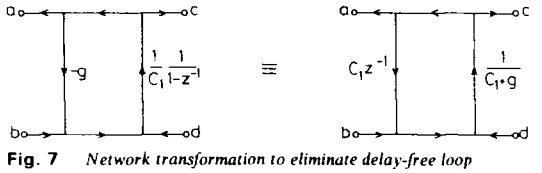

Fig. 7 *Network transformation to eliminate delay-free loop*

4 Sensitivity estimations

In the fabrication process, nonideal factors will inevitably lead to deviation in the system parameters. In the digital case, the nonideal factor would be the truncation of multiplier coefficients to finite wordlength, which will affect only $\{C_i\}$ and $\{L_i\}$. For analogue cases, inaccu-

It will be proved that the amplitude response of the structures introduced in this paper, unlike their biquad counterparts, are completely insensitive with respect to deviation of most of the element values and are bounded for a few terminating elements. The transfer functions of Figs. 2, 4 and 6 have the form

$$\frac{v_{out}}{v_{in}} = H_a = \pm\left(a - \frac{b\alpha v_1/J_1}{1 + dv_1/J_1}\right) \tag{18}$$

For Figs. 2 and 4, $a = b = d = g = 1$, and $\alpha = 2$, and, for Fig. 6, $b = b_1 + b_2 z^{-1}$ and $a = b_1 = b_2 = \alpha = d = g = 1$.

Remark: For the circuits in Figs. 2, 4, and 6, if a, b (or b_1, b_2) and α are fixed, then $|H_a| = 1$, regardless of all other parameters, even the unity valued elements.

Proof: In the s-domain (Figs. 2 and 4), eqn. 18 becomes

$$|H_a| = \left|\frac{1 - v_1/J_1}{1 + v_1/J_1}\right| \tag{19}$$

It is easily seen that $|H_a| = 1$ if v_1/J_1 is imaginary.

For the circuit in Fig. 2, v_1/J_1 is certainly imaginary, being the admittance of a reactive network.

For the circuit in Fig. 4*a*, we can apply the Mason formula [13] to derive v_1/J_1:

$$\frac{v_1}{J_1} = \frac{1}{\Delta} \sum_{\substack{\text{all forward} \\ \text{paths}}} (g_k \Delta_k) \tag{20}$$

with

$$\Delta = 1 - \sum_m P_{m1} + \sum_m P_{m2} - \sum_m P_{m3} + \cdots \tag{21}$$

where g_k is the product of edge weights for kth forward path, P_{mr} is the product of loop transmissions for the mth set of vertex-disjoint feedback loops and Δ_k is the value of Δ for the part of the graph with no vertices in common with the kth forward path.

Every loop in the subnetwork of the reactive two port in Fig. 3*a* (case A) involves exactly one Ψ term and one Φ term. In the s-domain, $\Psi\Phi = (j\omega)^{-2} = -\omega^{-2}$ and, therefore, $P_{mr} = \Pi(\Psi/C_i)(-\Phi/L_j)$ will be real, and so will all Δ and $\{\Delta_k\}$. There is only one forward path from J_1 to v_1, $g_1 = \Psi/C_1 = j\omega/C_1$, hence, from eqn. 20, v_1/J_1 is imaginary and $|H_a| = 1$. A similar proof can be applied to Fig. 4*b*.

For the z-domain circuit of Fig. 6*a*, note that all Δ and $\{\Delta_k\}$ are, again, real. Referring to Fig. 3*a* (case C),

$$\Psi\Phi = \frac{z^{-1}}{(1 - z^{-1})^2} = -\sin^{-2}\left(\frac{\omega T}{2}\right) \quad \text{for } z = e^{j\omega T} \tag{22}$$

Since the only forward path is $g_1 = \Psi/C_1$, from eqn. 20, v_1/J_1 will have the form $v_1/J_1 = \varepsilon\Psi$, with ε real. Hence, the following identities are derived:

$$|H_a| = \left|1 - \frac{1 + z}{1 + J_1/v_1}\right|$$

$$= \left|\frac{-1 + \dfrac{1 - z}{1 + z} + 2\dfrac{J_1/v_1}{1 + z}}{1 + \dfrac{1 - z}{1 + z} + 2\dfrac{J_1/v_1}{1 + z}}\right| = \left|\frac{-1 + \left(1 + \dfrac{2}{\varepsilon}\right)\dfrac{1 - z}{1 + z}}{1 + \left(1 + \dfrac{2}{\varepsilon}\right)\dfrac{1 - z}{1 + z}}\right| \tag{23}$$

As $(1 - z)/(1 + z) = j \tan(\omega T/2)$ is imaginary for $z = e^{j\omega T}$, one can see that $|H_a| = 1$. A similar result can be proved for the circuit in Fig. 6*b*.

The sensitivity formulas for the remaining elements in the circuits of Fig. 4 can be derived (since $Y(j\omega) = J_1/v_1$ is a pure imaginary number) as

$$-1 \leqslant \frac{a}{|H_a|}\frac{\partial|H_a|}{\partial a} = \pm\frac{1 - |Y(j\omega)|^2}{1 + |Y(j\omega)|^2} \leqslant 1 \tag{24a}$$

$$-2 \leqslant \frac{b}{|H_a|}\frac{\partial|H_a|}{\partial b} = \frac{x}{|H_a|}\frac{\partial|H_a|}{\partial x} = \frac{\pm 2}{1 + |Y(j\omega)|^2} \leqslant 2 \tag{24b}$$

$$-2 \leqslant \frac{d}{|H_a|}\frac{\partial|H_a|}{\partial d} = \frac{\pm 2}{1 + |Y(j\omega)|^2} \leqslant 2 \tag{24c}$$

Similar formulas can be derived for the circuits of Fig. 6.

5 Examples and Comparisons

The design procedure presented above has been incorporated into the filter design software package PANDDA, where cascade biquad structures are also available [14]. As an example, a sixth order allpass SC filter (case C) is designed to achieve an equiripple correction of the delay distortion caused by a sixth order SC bandpass filter, see Table 1. The design data given in Table 2 relate to the two ladder-based equaliser structures, LUD and leapfrog of Fig. 6. Each of these circuits can be followed by the amplitude stage in Fig. 8, designed as a sixth order elliptic LUD-type SC circuit, see Table 1. All of the circuits have been scaled for maximum dynamic range. The P_v point of either circuit of Fig. 6 can be directly connected to the input of the circuit of Fig. 8. The amplitude and delay responses are shown in Figs. 9*a* and *b*.

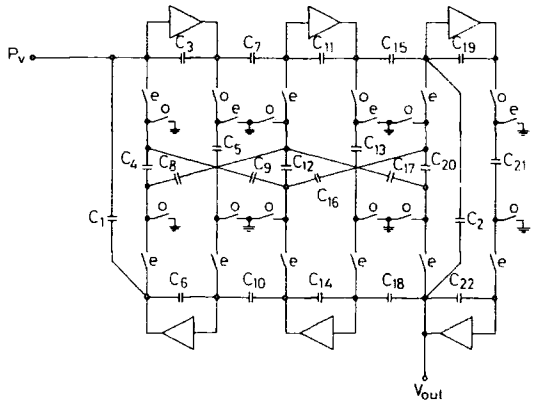

Fig. 8 *Sixth order bandpass SC elliptic LUD filter*

The following formula is used to measure the overall system sensitivity:

$$S = \left\{\sum_i \left(\frac{c_i}{|H_{ci}|}\frac{\partial|H_{ci}|}{\partial c_i}\right)^2\right\}^{1/2} \tag{26}$$

Table 1: Design data for sixth order bandpass SC elliptic filter

Specification for amplitude filter			
Lower passband edge	8000 Hz	Upper passband edge	10000 Hz
Lower stopband edge	7200 Hz	Upper stopband edge	10800 Hz
Passband ripple	<0.3 dB	Stopband attenuation	>25 dB
Approximation type	elliptic	Filter order	6
Sampling frequency	150000	Hz	

Component values for LUD SC ladder					
C_1 1.000	C_2 1.000	C_3 10.83	C_4 2.769	C_5 1.000	C_6 2.182
C_7 5.041	C_8 1.000	C_9 1.335	C_{10} 1.356	C_{11} 10.76	C_{12} 4.055
C_{13} 1.794	C_{14} 3.733	C_{15} 5.873	C_{16} 2.573	C_{17} 1.263	C_{18} 1.000
C_{19} 7.265	C_{20} 3.285	C_{21} 1.000	C_{22} 2.430		

Total capacitance	74 units	Capacitance spread	10 units
Number of switches	25	Number of capacitors	22
Number of op amps	6		

The system delay sensitivity can be defined in the same way. For comparison, two cascade biquad SC circuits are designed for the delay equalisation stage, using biquad topologies 1 and 2 of Reference 3. The resulting design parameters are listed in Table 3. As in Reference 3, topology 1 has quite a small spread, but very high sensitivity, whereas topology 2 has an improved sensitivity at the cost of high spread, see Fig. 10. Other biquad topologies

Table 2: Design data for SC delay equalisers

Specification for delay equaliser					
Lower equalisation edge 8000 Hz			Upper equalisation edge 10000 Hz		
Approximation type equiripple			In-band ripple <0.00014 s		
Filter order 6			Sample frequency 150000 Hz		
Poles of normalised allpass transfer function in s-domain					
$-0.0518242 + j1.01293$			$-0.0518242 - j1.01293$		
$-0.0482866 + j1.08983$			$-0.0482866 - j1.08983$		
$-0.0458278 + j0.93370$			$-0.0458278 - j0.93370$		
Component values for the LUD SC ladder					
C_a 1.000	C_{b1} 1.023	C_{b2} 1.023	C_c 2.333	C_d 2.386	
C_1 9.903	C_2 2.380	C_3 3.273	C_4 1.000	C_5 1.000	C_6 1.011
C_7 24.22	C_8 2.478	C_9 8.660	C_{10} 1.000	C_{11} 1.000	C_{12} 1.000
C_{13} 29.29	C_{14} 2.651	C_{15} 10.99			
Total capacitance		109 units	Capacitance spread		29 units
Number of switches		27	Number of capacitors		21
Number of op amps		6			
Component values for the leapfrog SC ladder					
C_a 1.015	C_{b1} 1.000	C_{b2} 1.000	C_c 1.015	C_d 1.000	
C_1 8.878	C_2 9.546	C_3 3.289	C_4 3.982	C_5 1.000	C_6 1.000
C_7 20.34	C_8 22.19	C_9 8.305	C_{10} 7.565	C_{11} 1.000	C_{12} 1.000
C_{13} 29.21	C_{14} 2.660	C_{15} 1.000			
Total capacitance		138 units	Capacitance spread		29 units
Number of switches		28	Number of capacitors		21
Number of op amps		6			

Table 3: Comparison of various SC delay equalisers

	LUD	Leapfrog	Biquad topology 1	Biquad topology 2
Total capacitance	109 units	138 units	102 units	311 units
Capacitance spread	29 units	29 units	26 units	62 units
Number of op amps	6	6	6	6
Number of switches	27	28	32	32
Number of capacitors	21	21	24	24
S/H and summation stages excluded				

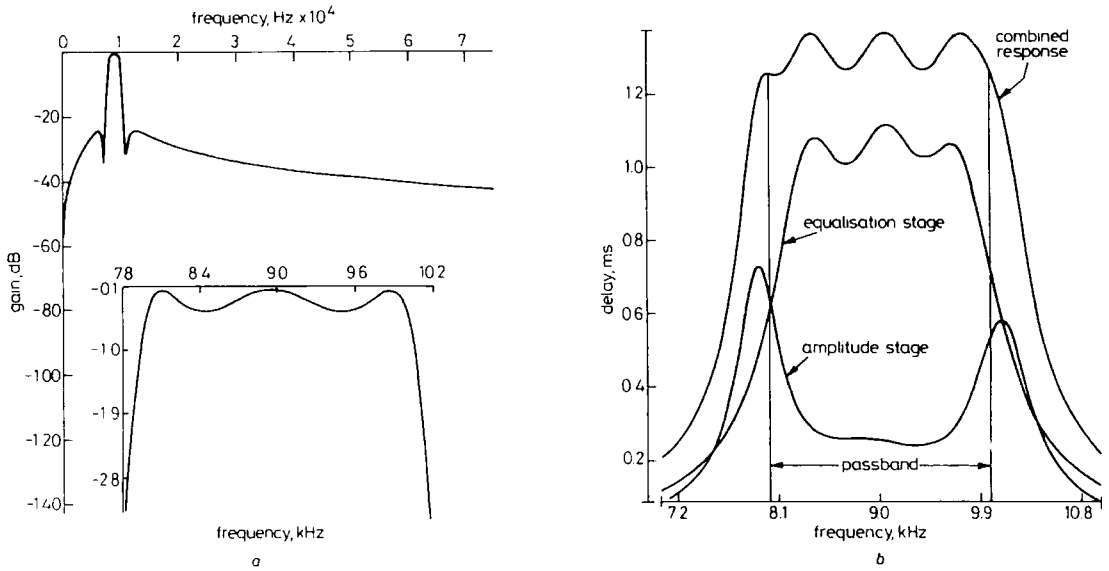

Fig. 9 *SC circuit responses*

a Amplitude response of sixth order SC LUD filter

b Delay response of equalised SC filter system

[3] show some tradeoff of sensitivity and spread between these two extremes. However, it is seen that ladder-based structures demonstrate the significant advantage of both low sensitivity and low capacitance spread.

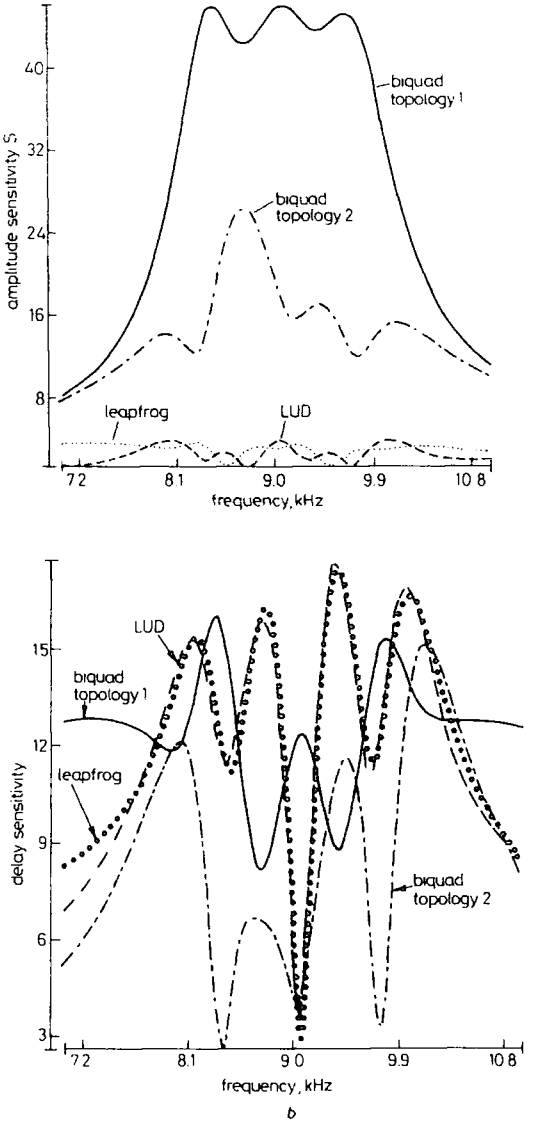

Fig. 10 *Equaliser sensitivities*
a Amplitude *b* Delay

The amplitude sensitivities for ladder-based circuits, of the type shown in Fig. 6, are mainly determined by five parameters, i.e. $a = C_a/C_s$, $b_1 = C_{b1}/C_s$, $b_2 = C_{b2}/C_s$, $\alpha = C_c/C_1$ and $d = C_d/C_1$. Provided these ratios are carefully controlled, good allpass properties can be expected.

6 Conclusions

A systematic approach has been proposed for active and digital allpass ladder-based design and novel LUD structures have been developed that demonstrate very low amplitude sensitivity, as well as other advantages, such as high parallelism for digital realisation and low total capacitance for SC realisation. It is shown that LUD ladder-based structures can be implemented with a canonical number of multipliers and delays for digital circuits or with a canonical number of op amps for analogue circuits.

A formal sensitivity analysis of the ladder-based all pass structures has indicated that amplitude sensitivities are strictly bounded, and this is confirmed by detailed examination of example circuits.

The allpass ladder-based networks have direct application in delay equalisation and also in the realisation of general amplitude functions by a sum of allpass functions [15] to achieve low-sensitivity and low-noise properties.

7 Acknowledgements

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PAPER 42

Extended Remez algorithms for filter amplitude and group delay approximation

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Indexing terms: Mathematical techniques, Filter amplitude, Group delay functions

Abstract: Various Remez-type algorithms for the computation of rational filter functions of a general form are proposed. They allow filter amplitude and group delay functions to be arbitrarily shaped and tapered. Such functions can be applied to predistort for undesirable effects in communication systems such as sinc (x), transmission line weighting or distortion due to nonideal components. High-order touch points are introduced as a generalisation of the concept of maximum flatness. They are used to trade off between the amplitude, group delay and passive sensitivity properties of a filter. The high-order touch points can be used directly to design a passive ladder prototype by an iterative algorithm.

1 Introduction

The paper is concerned with computational methods for the design of rational filter functions. Classical functions which approximate ideal filter amplitude specifications are commonly known. These functions have special properties of symmetry and constant equiripple attenuation in passband or stopband. Their coefficients can be conveniently calculated by explicit formulas or simple iterations [1, 2]. However, classical approximations are not suitable for highly asymmetric specifications or amplitude equalisation tasks which are often encountered in modern communications systems [3]. Approximation methods for such specifications are not well developed. They are usually highly specific to a given filtering task and are not flexible enough for a general, easy-to-use software package [3–7]. Although general multiple-criterion optimisation techniques can certainly be applied, they tend to involve a large amount of computation and do not always guarantee convergence [8–10]. This is frequently because they do not make enough use of the special properties of filter functions, which are particular cases of rational functions with well-confined root locations. Moreover, the approximation problem is often not expressed conveniently for a filter designer without detailed knowledge of optimisation theory.

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Methods for the approximation of polynomial filter functions within arbitrarily weighted amplitude specifications are considered. Several new algorithms are proposed, which bear interesting relationships to the Remez minimax approximation technique [11, 12]. The concept of maximum flatness is generalised to allow compromises between equiripple and flatband properties. The computational aspects of the algorithms are discussed. As accuracy is particularly critical in the approximation of filter functions in finite word length computer arithmetic, methods to preserve accuracy without recourse to the complications of transformed variables are given [1, 2].

The design of minimum phase rational functions with arbitrary passband and stopband tolerance schemes is investigated. These functions are of particular importance because they can be efficiently realised as the transfer functions of linear analogue networks, including switched-capacitor filters (SCFs). Numerator and denominator polynomials have special properties which are best designed by a combination of two different methods.

The approximation discussion so far has considered only filter amplitude functions and has ignored their associated group delay. Modern digital communications and signal-processing systems often require filters which satisfy simultaneous specifications on amplitude *and* group delay. A common practical design approach is to separate the two approximation problems by employing an all-pass function to equalise the group delay of a minimum phase amplitude function. The latter function should first be optimised to reduce the peaking of the delay towards the passband edges, either by smoothing the passband amplitude function (e.g. Butterworth) or reducing the rolloff into the stopband. The general amplitude approximation methods offer various ways to trade off between the amplitude and group delay characteristics. High-order touch points can be introduced into the passband and notches can be placed to tailor the stopband rolloff. Although the demands on the group delay correction can be reduced in these ways, it is still costly to use allpass functions. They are known to offer a non-canonic solution to the combined amplitude and group delay approximation problem. Greater efficiency can be achieved by employing a general nonminimum phase function [13, 14]. However, these functions cannot be simulated by low-sensitivity SCFs at present. The argument for all-pass equalisation is strengthened by the recent development of low-sensitivity all-pass SC ladder structures [15].

A method is presented whereby the techniques developed to approximate the amplitude of a transfer function can also be applied to the group delay of an allpass func-

tion. Unfortunately, when this group delay function is interpolated, a system of ill-conditioned nonlinear equations arises which becomes very difficult to solve with increasing order [16]. Since Newton- and Remez-type approximation methods depend on an efficient interpolation step, they are difficult to apply with efficiency or reliability [17]. Alternative methods based on optimisation techniques have therefore been studied [18, 19].

A new algorithm is proposed which permits direct application of Remez-type approximation methods to the problem [20]. By observing the similarity between the group delay function and a filter amplitude function, the techniques and theorems for amplitude approximation are still valid. A stable, accurate algorithm is then developed for arbitrary group delay correction.

2 Filter amplitude approximation

A transmission function is designed by working with a magnitude squared function. It has the following property:

$$T(s)T(-s)\Big|_{s=j\omega} = T(x)\Big|_{x=\omega^2} \tag{1}$$

The phase information has been removed and the function has been linearised in terms of a single real variable, avoiding the use of complex arithmetic in later computations.

2.1 Curve-fitting problem

Consider the problem of fitting a polynomial $p(x) = a_n x^n + \cdots + a_0$ in a minimax sense to some prescribed function $m(x)$ on the interval $[a, b]$ such that the maximum error $\max|p(x) - m(x)|$ is minimised. A variant of this problem is of interest to filter designers (Fig. 1). Two

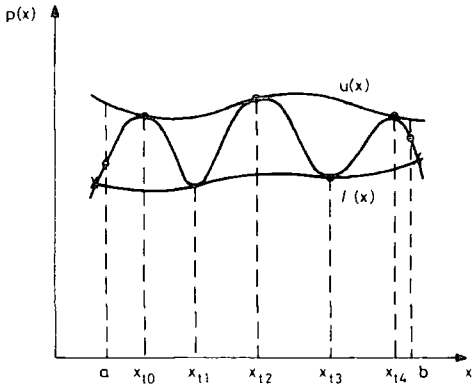

Fig. 1 *Solution of minimum curve-fitting problem by polynomial p(x)*

curves, $u(x) = m(x) + \delta$ and $l(x) = m(x) - \delta$, can be seen as boundary functions and $p(x)$ is sought to fit between them. At a series of points, the so-called *touch points*, $p(x)$ will touch $u(x)$ and $l(x)$ alternately, which implies that $p(x)$ will have the same zero- and first-order derivative values of $u(x)$ or $l(x)$. In a general sense, $u(x)$ and $l(x)$ can be any functions satisfying $u(x) > l(x)$ on $[a, b]$ and the order of tangency at the touch points can be greater than one. At M points (the touch points) on the upper and the lower function, $\{x_{ti} : a < x_{ti} < x_{ti+1} < b\}$

$$p^{(r)}(x_{ti}) = u^{(r)}(x_{ti}) \quad \text{or} \quad l^{(r)}(x_{ti}) \quad r = 0, 1, 2, \ldots, \mu_i \tag{2}$$

where $i = 1, 2, 3, \ldots, M$ and the superscript (r) signifies the rth derivative with respect to x. The exact locations of $\{x_{ti}\}$ are unknown but the sequence $\{\mu_i\}$ is specified (Fig. 2). For convenience we fix the two endpoints by

$$p(a) = \mathrm{A} \quad l(a) \leqslant A \leqslant u(a)$$

$$p(b) = \mathrm{B} \quad l(b) \leqslant B \leqslant u(b) \tag{3}$$

where A and B are usually fixed to the upper and lower boundaries, but could be assigned to some arbitrary values in between. In total there are N_c specifications on the values and the derivatives of $p(x)$ where

$$N_c = 2 + \sum_{i=1}^{M} (\mu_i + 1) \tag{4}$$

The aim of the curve-fitting problem is to find the lowest order approximating polynomial which fits the specifications in eqns. 2 and 3.

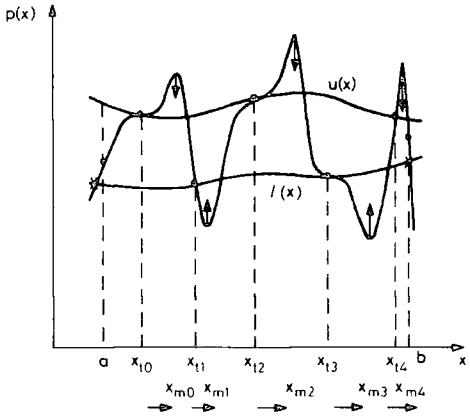

Fig. 2 *Bilateral approximation*

2.2 Interpolation

The unknown positions of $\{x_{ti}\}$ provide M degrees of freedom, which can be used to reduce the order of the polynomial from the nominal problem order N_c. Thus $N_c - M$ of the specifications can be chosen as constraints to form a polynomial of order N, where

$$N + 1 = N_c - M \tag{5}$$

The remaining M specifications must be met by adjusting the M positions of the touch points.

The relation between the behaviour and the order of a polynomial is a complicated issue. To decide the minimum order is a difficult problem and some theoretical discussion can be found in Reference 21; however, in most cases the order determined by eqn. 5 is satisfactory. A Nth order polynomial can always be interpolated by $N + 1$ constraints. Osculatory Newton interpolation [22] can be used to interpolate a number of derivatives with certain computational advantages over other interpolation methods [23].

2.3 Bilateral method

Assume that, for the specifications

(i) all μ_i are odd

(ii) the touch points are assigned alternately to $u(x)$ and $l(x)$, i.e. $\{x_{ti} | i = 1, 3, \ldots, M_u\}$ and $\{x_{ti} | i = 2, 4, \ldots, M_l\}$ are the set of touch points on $u(x)$ and $l(x)$, respectively (where $M_u = M$ and $M_l = M - 1$ if M is odd and $M_u = M - 1$ and $M_l = M$ if M is even).

These assumptions are true for a Chebyshev function where all μ_i are equal to 1 (osculatory points) and are valid for most filter functions. The Weierstrass polynomial approximation theorem guarantees that, if the filter order is high enough, a solution lying between the two boundary functions will exist [21].

Interpolate $p(x)$ such that

$$p^{(r)}(x_{ti}) = u^{(r)}(x_{ti}) \quad r = 0, 1, \ldots, \mu_i - 1 \quad i = 1, 3, 5, \ldots, M_u \tag{6a}$$

$$p^{(r)}(x_{ti}) = l^{(r)}(x_{ti}) \quad r = 0, 1, \ldots, \mu_i - 1 \quad i = 2, 4, 6, \ldots, M_l \tag{6b}$$

and

$$p(a) = A \quad p(b) = B \tag{6c}$$

Thus, exactly $N_c - M$ specifications are met by interpolation. It now remains to adjust $\{x_{ti}\}$ to make $\{p^{(\mu_i)}(x_{ti})\}$ satisfy the other M specifications.

Definitions

upper error function $e_u(x) = p(x) - u(x)$

lower error function $e_l(x) = l(x) - p(x)$

mid-function $m(x) = (l(x) + u(x))/2$

search function $s(x) = \max [e_u(x), e_l(x)]$

combined error function

$$e(x) = \begin{cases} -e_u(x) & \text{if } p(x) > m(x) \\ e_l(x) & \text{if } p(x) \leqslant m(x) \end{cases}$$

From assumption (i) above, $\{\mu_i - 1\}$ are restricted to be even, so, in general, the touch points are now points of inflection (Fig. 2) and $s(x)$ will change sign in the neighbourhood of each touch point $\{x_{ti}\}$. If the polynomial is manipulated such that $p(x)$ does not cross $u(x)$ or $l(x)$ at these points, $p(x)$ must possess an extra order of tangency to $u(x)$ or $l(x)$, having then up to the μ_ith order tangency at $\{x_{ti}\}$ required for $p(x)$ to be a solution. At this stage, $\max [s(x)] = 0$ in the neighbourhood of $\{x_{ti}\}$. Notice that from assumption (ii) there must be at least one minimum of $e(x)$, denoted as x_{mi}, on $[x_{ti-1}, x_{ti+1}]$. Therefore, if

$$x_{mi} = x_{ti} \quad i = 1, 2, 3, \ldots, M \tag{7}$$

is achieved, $p(x)$ is a solution. An approximation scheme can be adopted to generate an adjustment $\{\Delta x_{ti}\}$

$$\{x_{ti}\} \leftarrow \{x_{ti} + \Delta x_{ti}\} \quad i = 1, 2, 3, \ldots, M \tag{8}$$

to reduce $\{e(x_{mi})\}$.

2.4 Newton's method

Obviously, $\{\Delta x_{ti}\}$ can be generated by a technique based on Newton's method which is found by solving a Jacobian system [22]

$$\begin{bmatrix} g_1(x_{m1}) & g_2(x_{m1}) & \cdots & g_M(x_{m1}) \\ g_1(x_{m2}) & \vdots & \cdots & \vdots \\ \vdots & \vdots & & \vdots \\ g_1(x_{mM}) & g_2(x_{mM}) & \cdots & g_M(x_{mM}) \end{bmatrix} \begin{bmatrix} \Delta x_{t1} \\ \Delta x_{t2} \\ \vdots \\ \Delta x_{tM} \end{bmatrix} = \begin{bmatrix} e(x_{m1}) & & & \\ & e(x_{m2}) & & \\ & & \ddots & \\ & & & e(x_{mM}) \end{bmatrix} \tag{9}$$

where

$$g_i(x) = \frac{\partial p(x)}{\partial x_{ti}} \tag{10}$$

The computational cost of setting up the Jacobian matrix $\boldsymbol{J}$ and solving the Newton system is usually large ($O(n^3)$). Efficient methods to obtain the derivatives $g_i(x_{mj})$ and to solve for the touch point increments $\{\Delta x_{ti}\}$ are now presented.

Theorem 1: Define a Nth order polynomial $q(x)$ subject to the following $N + 1$ interpolation conditions

$$q(x_{mi}) = e(x_{mi}) \quad i = 1, 2, \ldots, M \tag{11a}$$

$$q^{(r)}(x_{ti}) = 0 \quad r = 0, 1, \ldots, \mu_i - 2, i = 1, 2, \ldots, M \tag{11b}$$

and

$$\delta_i(x) = \frac{(x - x_{ti})q(x)}{\mu_i e(x)} \quad i = 1, 2, \ldots, M \tag{11c}$$

then the Newton system (eqn. 9) can be solved for the touch point increments $\{\Delta x_{ti}\}$ by

$$\Delta x_{ti} = \lim_{x \to x_{ti}} \delta_i(x) \tag{12}$$

Proof of theorem 1: Consider the solution of the Newton system for touch point movements Δx_{ti} by interpolation of $q(x)$. Two remarks are necessary for the proof.

Remark 1: Suppose $u(x)$ or $l(x)$ (and so $e(x)$) are differentiable up to μ_ith order at all the touch points. The function $g_i(x)$, formed by differentiating the interpolated polynomial $p(x)$ with respect to a touch point x_{ti}, is therefore itself an Nth order polynomial of x. It can be calculated by interpolation subject to the following constraints:

$$g_i^{(r)}(x_{tj}) = 0 \quad r = 0, 1, \ldots, \mu_j - 1 \quad j = 1, 2, \ldots, M \quad j \neq i \tag{13a}$$

$$g_i^{(\mu_i - 1)}(x_{ti}) = e^{(\mu_i)}(x_{ti}) \quad r = 0, 1, \ldots, \mu_i - 1 \tag{13b}$$

Proof: Eqn. 13*a* is evident as the μ_j interpolated derivatives of $p(x_{tj})$ are fixed with respect to another touch point x_{ti}, $i \neq j$. The proof of eqn. 13*b* follows. Suppose that one of the touch points on $u(x)$, x_{ti}, changes to $x'_{ti} = x_{ti} + h$ and the ordinate from $u(x_{ti})$ to $u(x_{ti} + h)$. Define the new polynomial interpolated from $\{x_{t1}, x_{t2}, \ldots, x'_{ti}, \ldots, x_{tM}\}$ by $p_h(x)$. As the polynomial is interpolated up to $\mu_i - 1$th tangency to $u(x)$ at this touch point,

$$p_h^{(r)}(x_{ti} + h) = u^{(r)}(x_{ti} + h) \quad r = 0, 1, 2, \ldots, \mu_i - 1 \tag{14}$$

Expand $p_h(x)$ at x'_{ti} by a Taylor series and evaluate $p_h^{(r)}(x)$ at $x = x_{ti}$ and notice (eqn. 14)

$$p_h^{(r)}(x_{ti}) = \left\{ \sum_{k=0}^{\infty} \frac{p_h^{(k)}(x_{ti} + h)}{k!} (-h)^k \right\}^{(r)} = u^{(r)}(x_{ti} + h) - p_h^{(r+1)}(x_{ti} + h)h + O(h^2) \tag{15}$$

for $r = 0, 1, 2, \ldots, \mu_i - 1$.

$$g_i^{(r)}(x_{ti}) = \left. \frac{\partial p^{(r)}(x)}{\partial x_{ti}} \right|_{x = x_{ti}} = \lim_{h \to 0} \frac{p_h^{(r)}(x_{ti}) - p^{(r)}(x_{ti})}{h} \tag{16}$$

$$= \lim_{h \to 0} \frac{[u^{(r)}(x_{ti} + h) - p_h^{(r+1)}(x_{ti} + h)h] - u^{(r)}(x_{ti}) + O(h^2)}{h} \tag{17}$$

$$= u^{(r+1)}(x_{ti}) - p_h^{(r+1)}(x_{ti}) \tag{18}$$

Eqn. 13*b* follows by noting that $\lim p_h^{(r+1)}(x_{ti} + h) = p^{(r+1)}(x_{ti})$ as $h \to 0$ and the definition of $e(x)$ for $r = 0, 1, 2, \ldots, \mu_i - 1$. In general, the above proof can be applied to all $\{x_{ti}\}$, which may be touch points on either $u(x)$ or $l(x)$.

Remark 2: The Newton system can be solved for the touch point increments $\{\Delta x_{ti}\}$ by

$$\Delta x_{ti} = \frac{q^{(\mu_i-1)}(x_{ti})}{g_i^{(\mu_i-1)}(x_{ti})} = \frac{q^{(\mu_i-1)}(x_{ti})}{e_i^{(\mu_i)}(x_{ti})} \quad i = 1, 2, \ldots, M \tag{19}$$

Proof: A single row of the Jacobian system (eqn. 9) is

$$\sum_{i=1}^{M} g_i(x_{mj})\,\Delta x_{ti} = e(x_{mj}) \quad j = 1, 2, \ldots, M \tag{20}$$

and define

$$q(x) = \sum_{i=1}^{M} g_i(x)\Delta x_{ti} \tag{21}$$

From theorem 1, $q(x)$ is also a polynomial and meets the constraints of eqn. 11. Substitute $x = x_{tj}$ into eqn. 21 and

$$q_j^{(\mu_j-1)}(x_{tj}) = \sum_{i=1}^{M} g_i^{(\mu_j-1)}(x_{tj})\,\Delta x_{ti} = g_j^{(\mu_j)}(x_{tj})\,\Delta x_{tj} \tag{22}$$

Eqn. 19 follows.

From eqns. 11*b* and 6*a*, x_{ti} is a $(\mu_i - 2)$th order zero of $q(x)$ and $(\mu_i - 1)$th order zero of $e(x)$. They can be expanded by a Taylor expansion at x_{ti} as

$$q(x) = A_q(x - x_{ti})^{\mu_i-1} + O[(x - x_{ti})^{\mu_i}] \tag{23}$$

$$e(x) = A_e(x - x_{ti})^{\mu_i} + O[(x - x_{ti})^{\mu_i+1}] \tag{24}$$

From eqns. 19, 23 and 24,

$$\Delta x_{ti} = \frac{q^{(\mu_i-1)}(x_{ti})}{e^{(\mu_i)}(x_{ti})} \cong \frac{(\mu_i - 1)!\,A_q}{\mu_i!\,A_e} = \frac{A_q}{\mu_i A_e} \tag{25}$$

From eqns. 23, 24 and 25, it is easily seen that eqn. 12 is true.

As both numerator and denominator of eqn. 19 tend to zero at x_{ti}, each touch point increment Δx_{ti} can only be calculated from the limiting values of the increment polynomial $q(x)$ and error function $e(x)$ in the proximity of the touch point, $x_{ti} + h$. The distance h must be chosen suitably according to word length and order of touch point. A suggested rule is $\mu_i \times 10^{-6}/N$ for double precision arithmetic.

The computational cost of the whole procedure is very small as it involves only repeated interpolation. The $O(n^3)$ step of solving the Newton system has been reduced to an $O(n^2)$ interpolation. Each evaluation of the interpolated polynomial costs $O(n)$ multiplications.

2.5 Generalised Remez methods

As has been shown, Δx_{ti} can be approximately evaluated by $\delta_i(x)$ at a point close to x_{ti}. If this point is selected as $x = x_{mi}$, a very simple adjustment to the touch point positions is revealed (notice eqn. 11*a*)

$$\Delta x_{ti} = \delta_i(x_{mi}) = \frac{(x_{mi} - x_{ti})q(x_{mi})}{\mu_i e(x_{mi})} = \frac{x_{mi} - x_{ti}}{\mu_i} \tag{26}$$

In the special case of the curve-fitting problem with all $\mu_i = 1$, eqn. 26 results in the well-known Remez method which updates the variable vector by

$$\{x_{ti}\} \leftarrow \{x_{mi}\} \quad i = 1, 2, \ldots, M \tag{27}$$

This indicates that the interpolation ordinates are simply exchanged with the locations of the extrema and reinterpolated (Fig. 2). It may be expected that ordinates separated by an excessively large ripple will be brought together and those separated by an insufficiently large ripple will be moved apart. When the $\{x_{ti}\}$ are close to the solution, the $\{x_{mi}\}$ are also close to $\{x_{ti}\}$, and the adjustment given by eqn. 26 becomes similar to that given by a Newton method. This confirms that the Remez method achieves the good convergency of Newton iteration on approach to the solution. Convergency of this algorithm is guaranteed [21] for sufficiently large N, and it has been widely adopted in FIR and IIR digital filter design [24–26]. For the case of $\mu_i > 1$, the simple exchange process of eqn. 27 is unsuitable. Instead, the adjustment given by eqn. 26 is applicable

$$\{x_{ti}\} \leftarrow \{x_{ti} + (x_{mi} - x_{ti})/\mu_i\} \quad i = 1, 2, \ldots, M \tag{28}$$

This can be seen as a generalisation of the Remez method of eqn. 27 in which, instead of moving the abscissa all the way to the extremum, it is moved by a fraction of the distance dependent on the order of the touch point.

2.6 Unilateral method

In most filter applications, emphasis is given to one of the bounding functions. For example, in the passband region of a filter, $u(x)$ is most important as it determines the points of maximum transmission. All the high-order touch points (with $\mu_i > 1$) could be assigned to $u(x)$ for greatest effect. In a unilateral method the $N_c - M$ specifications can be met by directly interpolating $p(x)$ to μ_ith order tangency at all the touch points on $u(x)$. The lower curve $l(x)$ is used only as a bound for the ripple, so that all touch points on $l(x)$ should be adjusted to $\mu_i = 1$ (Fig. 3). The difference between $p(x)$ and $l(x)$ is used as the objective function. Only half of the touch points are kept as variables compared with the bilateral method.

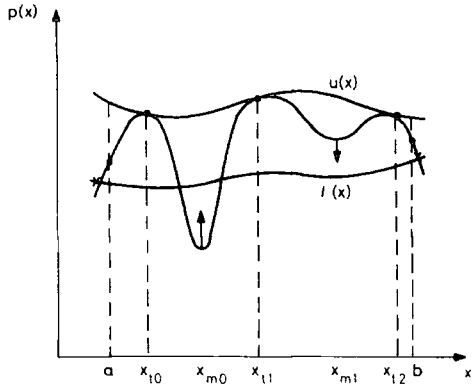

Fig. 3 *Unilateral approximation*

2.7 Computer algorithm

The approximation methods proposed in Section 2.6 can be implemented on a computer by the following algorithm:

Step 1: Read the boundary functions $u(x)$ and $l(x)$ as piecewise linear functions on range $[a, b]$. Read the number of touch points and specified orders μ_i.

Step 2: Distribute $\{x_{ti}\}$ uniformly over $[a, b]$ assigning $x_{t0} = a$ and $x_{tn} = b$.

Step 3: Interpolate $\{x_{ti}\}$ alternately to boundaries $u(x)$ and $l(x)$.

Step 4: Set $x_{m0} = a$

$i = 0, 2, 4, \ldots, n$; choose x_{mi} to maximise

$$\{p(x) - u(x),\ x_{mi-1} \leqslant x \leqslant x_{ti+1}\}$$

$i = 1, 3, 5, \ldots, n-1$; choose x_{mi} to maximise

$$\{l(x) - p(x),\ x_{mi-1} \leqslant x \leqslant x_{ti+1}\}$$

Step 5: Compute improved touch point estimates by one of the methods in Section 2.3. The extended Remez method indicates that

$$x_{ti} = x_{ti} + ((x_{mi} - x_{ti})/\mu_i)$$

Step 6: Compute convergence estimate for kth iteration as

$$\varepsilon_k = \frac{\sum_{i=1}^{n} e(x_{mi})}{\sum_{i=1}^{n} |u(x_{mi}) - l(x_{mi})|}$$

Terminate if $\varepsilon_k <$ tolerance or $\varepsilon_k > \varepsilon_{k+1}$ (divergent)

2.8 Software considerations

2.8.1 Interpolation: The interpolation of the polynomial at Step 3 can be done by *osculatory* Newton interpolation. This is an extended form of the well known Newton interpolation, whereby a number of derivatives can be matched to the specified function.

It is particularly important in a filter problem to take care with the accuracy of construction and representation of the polynomials within finite word length arithmetic. Cancellation errors are particularly severe as the touch points of a filter function become closely spaced near a band edge. A typical calculation would be

$$f[x_{t0}, x_{t1}] = \frac{f(x_{t0}) - f(x_{t1})}{x_{t0} - x_{t1}} \tag{29}$$

where cancellation errors occur in numerator and denominator as x_{t0} approaches x_{t1}.

The effects of these cancellation errors can be minimised by calculating interpolated values by the zig-zag path method [22]. The principle is that a path is taken through the Newton table, such that the coefficients with the largest errors are multiplied by abscissae with the smallest differences. By using this accurate interpolation and representation of polynomials, high-order functions can be obtained (up to length 110 FIR designs). This avoids the complications of transformed variable methods [1, 2].

2.8.2 Searching: At Step 4 a search must be made for the touch point extrema. For reliability, the best method is found to be a single linear search over a uniform grid of points. Normally only 10–20 points are required per touch point for a terminating accuracy better than 1%. The linear search requires a fairly large number of function evaluations for higher order approximation. Faster searching is available by applying cubic, quadratic or golden section search methods which require only five or six steps per touch point for very high accuracy (10^{-8}%). However, when the attenuation boundaries are specified in piecewise linear form and not by a smooth function with continuous derivatives, these search methods can mislead and may determine the extrema erroneously. A combination of the reliability of the linear search with the speed of gradient search methods is discussed by Antoniou [27].

2.8.3 Cluster method: In most cases, the boundary functions are only given by values and the derivatives are not available. Although the derivatives can be calculated by numerical differentiation, this is notoriously inaccurate for high orders. The polynomial obtained by a Newton interpolation may become totally unreliable in the neighbourhood of a high-order touch point. A better conditioned method is to interpolate the polynomial at a *cluster* of points with first-order tangency to the boundary function. A μ_ith-order touch point with μ_i odd requires $(\mu_i + 1)/2$ first-order touch points distributed in the neighbourhood of x_{ti}. In practice, it is found that a spacing of 10^{-6} (with normalised passband width of 1) can be chosen. The error caused by this approximate method can be controlled and made much smaller than the allowed ripple [the separation of $u(x)$ and $l(x)$].

2.8.4 Damping: The term damping is used for the process whereby the step sizes determined by Newton's method may be reduced to avoid divergence. A form of damping can be useful where Newton's method is used to predict adjustments Δx_{ti}, and the touch points would cross one another or move entirely outside the approximating region $[a, b]$. In these cases (usually far from solution), it is found useful to limit the movement of the touch points to half the distance in the direction of their closest neighbour. In this way, no touch point may cross or escape the region $[a, b]$, and yet the direction required to reduce the extrema is observed.

2.8.5 Convergency, accuracy and storage: Computation costs are $O(n^2)$ for passband approximation. Stopband approximation requires solution of a matrix system with $O(n^3)$ efficiency. Convergence is quadratic near solution, a property of algorithms based on Newton's method. Divergence occurs only in those cases where the boundary functions are too severe for the selected order of the function. The accuracy of the algorithm is limited solely by the fineness of the search grid used to determine the positions of the extrema. Storage is dominated by the matrix system and Newton interpolation tables and is of $O(n^2)$ size.

3 Rational approximation

3.1 Approximation method for rational functions

In this section, a design technique for rational filter transfer functions will be considered. The filter amplitude specifications need not be ideal and can have arbitrary weightings in both passband and stopband. The approximating function can be designed in a minimax fashion, with high-order touch points assigned to certain positions in each band. Classical functions result as special cases from a general algorithm.

For simplicity, a lowpass filter specification will be considered first. The filter specification is defined as a piecewise template of attenuation in dB against frequency in Hz. The following parameters must be specified by a designer:

f_{plo}, f_{phi}: passband edge frequencies (Hz)
f_{slo}, f_{shi}: stopband edge frequencies (Hz)
NN, ND: numerator and denominator orders

The transfer function to be designed is

$$T(x) = \frac{N(x)}{D(x)} \quad x = \omega^2 \tag{30}$$

The zeros of $T(x)$ are contained in the numerator polynomial. In a filter transfer function they are most effectively assigned to the imaginary axis of the s-plane (real x-plane locations) and placed in the stopband region for maximum attenuation. By making this restriction, the rational function becomes a minimum phase function. The denominator polynomial contains the complex pole locations which must be positioned to control the passband transmission characteristics.

The following procedure is used to design a rational filter approximation.

Step 1: Read ND, NN, f_{plo}, f_{phi}, f_{slo}, f_{shi}, touch point orders $\{\mu_{tsi}\}$, $\{\mu_{tpi}\}$ and piecewise linear descriptions of $L(\omega)$ and $U(\omega)$.

Step 2: Initialise $\{x_{tpi}\}$ in the passband region $[x_{plo}, x_{phi}]$ and $\{x_{tsi}\}$ in the stopband region $[x_{slo}, x_{shi}]$, equidistantly spaced. Set $N(x)$ to 1.

Step 3: Solve the passband approximation problem on $[x_{plo}, x_{phi}]$ using $D(x)$ such that

$$u(x) = N(x)/L(x)$$

$$l(x) = N(x)/U(x)$$

and compute initial convergence estimate ε_p.

Step 4: Solve stopband approximation problem on $[x_{slo}, x_{shi}]$ using $N(x)$ such that

$$u(x) = \beta U(x)/D(x)$$

$$l(x) = \beta L(x)/D(x)$$

and compute initial convergence estimate ε_s.

Step 5: Terminate if ε_p and $\varepsilon_s <$ tolerance *or* $k >$ maxiter.

Owing to the special properties of the numerator and denominator polynomials, two different approaches are appropriate for solving steps 3 and 4. Note that a multiplying factor β is introduced in step 4 so that the stopband attenuation will only be met to a constant dB error. In general, it is not possible to meet the stopband and passband specifications exactly and some error margin must be allowed in either passband or stopband, or both. In this approach, the passband specifications will be met as closely as possible, and the stopband attenuation characteristics will have some error above or below the specified attenuation. This expression of the filtering problem is useful in practice, as good control of the passband characteristics is usually of greater importance than the stopband. Note that if the factor β is less than 1, then the specifications have been exceeded and it may be possible to reduce the order of the function or the number of zeros. Conversely, if $\beta > 1$ the order must be increased or more zeros should be introduced.

3.1.1 Passband design: Any of the methods of Sections 2.3–4 are suitable for the design of the passband function $D(x)$. It is found that the bilateral method has very good global convergence. The unilateral method is then useful to ensure that the function does not exceed maximum transmission (i.e. $0 < T(x) < 1$) for passive filter realisation. The touch points are all fixed to the upper boundary.

3.1.2 Stopband design: The numerator polynomial is of the following particular form:

$$N(x) = Kx^{n_0} \prod_{i=1}^{nf} (x - x_{tsi})^{\mu_{tsi}} \tag{31}$$

This corresponds to a special case of the unilateral method where all touch points are tangential to the lower boundary which is zero. It remains to compute the attenuation margin β (Fig. 4). Two methods can be

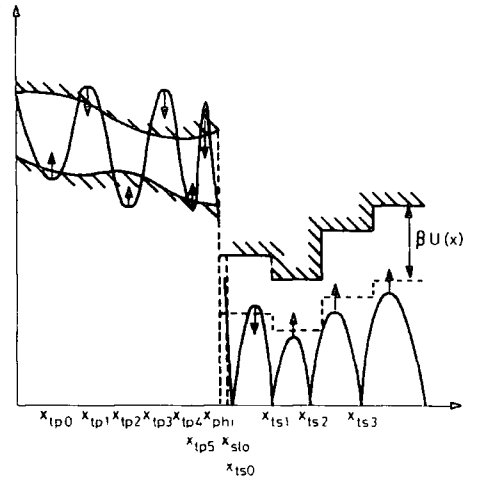

Fig. 4 *Scheme for approximation of an arbitrary lowpass filter specification by a rational function*

applied: the heuristic method [26] permits the approximation methods of this section to be used. However, a variant of the method of Temes and Smith [1] has proved to be more stable and more easily extended to multiband approximations. A Jacobian matrix of the peak positions with respect to the touch points must be set up and solved.

$$\left[\begin{array}{ccc|c} \frac{\partial T(x_{ms0})}{\partial x_{ts0}} & \cdots & \frac{\partial T(x_{ms0})}{\partial x_{tsn}} & -U(x_{ms0}) \\ \vdots & & \vdots & \vdots \\ \frac{\partial T(x_{msn})}{\partial x_{ts0}} & \cdots & \frac{\partial T(x_{msn})}{\partial x_{tsn}} & -U(x_{msn}) \end{array}\right] \left[\begin{array}{c} \Delta x_{ts0} \\ \vdots \\ \frac{\Delta x_{tsn}}{\beta} \end{array}\right] = \left[\begin{array}{c} -T(x_{ms0}) \\ \vdots \\ -T(x_{msn}) \end{array}\right] \tag{32}$$

and because

$$\frac{\partial T(x)}{\partial x_{tsi}} = \frac{-\mu_i}{(x - x_{tsi})} T(x) \tag{33}$$

Eqn. 32 can be rearranged and evaluated as

$$\left[\begin{array}{ccc|c} \frac{\mu_0}{(x_{ms0} - x_{ts0})} & \cdots & \frac{\mu_n}{(x_{ms0} - x_{tsn})} & \frac{U(x_{ms0})}{T(x_{ms0})} \\ \vdots & & \vdots & \vdots \\ \frac{\mu_0}{(x_{msn} - x_{ts0})} & \cdots & \frac{\mu_n}{(x_{msn} - x_{tsn})} & \frac{U(x_{msn})}{T(x_{msn})} \end{array}\right] \times \left[\begin{array}{c} \Delta x_{ts0} \\ \vdots \\ \Delta x_{tsn} \\ \beta \end{array}\right] = \left[\begin{array}{c} 1 \\ \vdots \\ 1 \end{array}\right] \tag{34}$$

The touch points are updated as

$$x_{tsi} = x_{tsi} + \Delta x_{tsi} \tag{35}$$

and some damping may be necessary. Note that the constant K must also be determined. A good method of assigning a value to K is to fix the passband edge position between passband and stopband iterations.

$$K = L(x_{phi})/T(x_{phi}) \tag{36}$$

3.2 Passive ladder design

Often the transfer function designed by the methods of previous sections will be decomposed into a passive ladder prototype for later simulation by active circuits. This is an error-prone numerical procedure. In this section, it will be demonstrated that the ladder can be designed directly from the touch points to provide high accuracy at the ripples that characterise the filter response.

Orchard has proposed a very simple but efficient algorithm to design an RLC ladder from a given reflection function $\rho(\omega)$ [28]. The structure of the ladder is prescribed and only the component values remain to be determined. A set of real and imaginary parts $\{\mathrm{Re}\,[\rho(\omega_{ti})], \mathrm{Im}\,[\rho(\omega_{ti})]\}$ are used to set up the objective function vector $\boldsymbol{F}$ for Newton-type iteration, and component values $\{y_k\}$ form a vector of variables $\boldsymbol{Y}$ [22]. The core of Orchard's algorithm is an elegant, well conditioned method to compute $\boldsymbol{F}$ and the Jacobian matrix of derivatives

$$\mathrm{Re}\left[\frac{\partial \rho(j\omega_{tk})}{\partial y_i}\right] \quad \text{and} \quad \mathrm{Im}\left[\frac{\partial \rho(j\omega_{tk})}{\partial y_i}\right]$$

by chain matrix calculations.

In the case of certain classical approximations, where the points of maximum or minimum transmission ($\rho(j\omega) = 0$ or $\rho(j\omega) = 1$) are known, the explicit calculation of $\rho(j\omega)$ is not necessary for Orchard's algorithm. However, in general, Orchard's method requires the formation of $\rho(j\omega)$ by Hurwitz factorisation of $|\rho|^2$ as in classical synthesis, which is an ill-conditioned procedure [1]. An extension of Orchard's method is described below which works with more general forms of $|\rho|^2$ but eliminates any root-finding requirement.

The value of $|\rho|^2$ and its deriatives at the touch points $\{x_{ti}\}$ can be chosen as the objective function for the Newton scheme. The derivatives of $|\rho|^2$ with respect to the element values $\{y_k\}$ are required for the construction of the Jacobian matrix and are given by (let $x_{ti} = \omega_{ti}^2$)

$$\frac{\partial}{\partial y_k}\left(\frac{d^r |\rho(\omega_{ti})|^2}{dx^r}\right) = 2\frac{d^r}{d\omega^r}\left\{\mathrm{Re}\left[\bar{\rho}(j\omega_{ti})\frac{\partial \rho(j\omega_{ti})}{\partial y_k}\right]\right\} \tag{37}$$

for $r = 0, \ldots, \mu_i$ and $i = 1, 2, \ldots, M$.

Notice that here $\bar{\rho}$ (the conjugate of ρ) and $\partial\rho/\partial y_k$ are obtained from the approximate network with guessed component values, which can be generated by Orchard's algorithm and then the remaining part of eqn. 37 can be calculated by a numerical differentiation. Here it is also found to be efficient to use the 'cluster' method mentioned in Section 2.8.3. The objective function $|\rho(\omega_{ti})|^2$ and derivatives are obtainable from a unilateral passband approximation of Section 2.6. This provides a direct link between approximation and ladder design procedures, bypassing the traditional Hurwitz factorisation step.

3.3 Computed examples

A series of computed approximation examples is now given to illustrate the power and flexibility of the above methods. Fig. 5 shows a polynomial (FIR) approximation to arbitrarily shaped boundaries. A touch point of fifth-order tangency is seen at the centre of the function. FIR approximations up to length 110 ($N = 55$) have been obtained using double precision arithmetic.

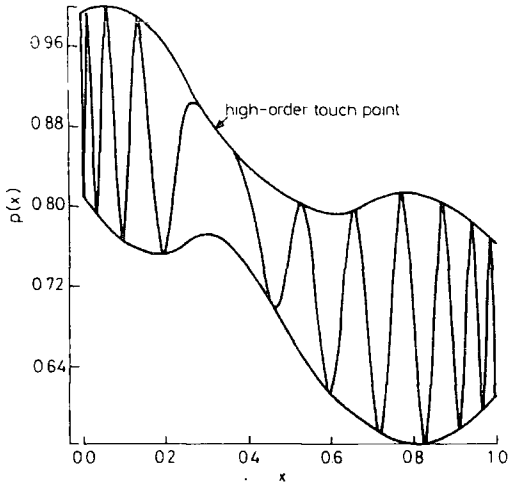

Fig. 5 *Length 51 FIR approximation to arbitrary boundaries*

Arbitrary rational function (IIR) filter responses are shown in Figs. 6–7. An 11th-order function is fitted touching the passband boundaries and meeting the stopband boundary to within some constant dB error (Fig. 6). A bandpass approximation with asymmetric stopband and sagging passband is shown in Fig. 7. High-order touch points can be placed in the passband to trade off between group delay, stopband attenuation and passive sensitivity properties. A series of such passbands is shown in Fig. 8, including inverse Chebyshev and elliptic forms as special cases. The effects on stopband attenuation and group delay is shown in Table 1. As high-order touch points are introduced into the response, there is a significant reduction in the peaks of the group delay, which follows from the progressive smoothing of the amplitude characteristic. There is also an accompanying improvement in sensitivity behaviour of the resulting passive filter realisation, as would be expected from Orchard's criterion [29], since the higher order touch points ensure adherence to maximum transmission over a wider interval. This property is inherited by active simulations, where sensitivity considerations are of major concern. There is some attendant cost, with a corresponding loss in stopband attenuation. Trade-off between these factors must be considered in design. It is obviously not possible to dictate the location, sequence and order of the touch points in a general manner, but it is recommended that they are deployed in regions where the filter characteristic is most critical.

Practical examples of the use of amplitude-shaping capabilities are given in Figs. 9–10. In Fig. 9 a length 69 differentiator is designed with a high-order touch point at 0 Hz for increased DC linearity [4]. A 14th-order wideband SC filter with 200 kHz clock frequency shows a 1 dB passband droop due to sinc (x) weighting. The original 0.1 dB flat equiripple passband behaviour can be

restored by prewarping the filter response upwards. Attenuation line-weighting and LDI ladder termination distortion can be treated in a similar manner. This technique is used in a more general sense (Fig. 11) to compensate for distortion caused by switch and amplifier

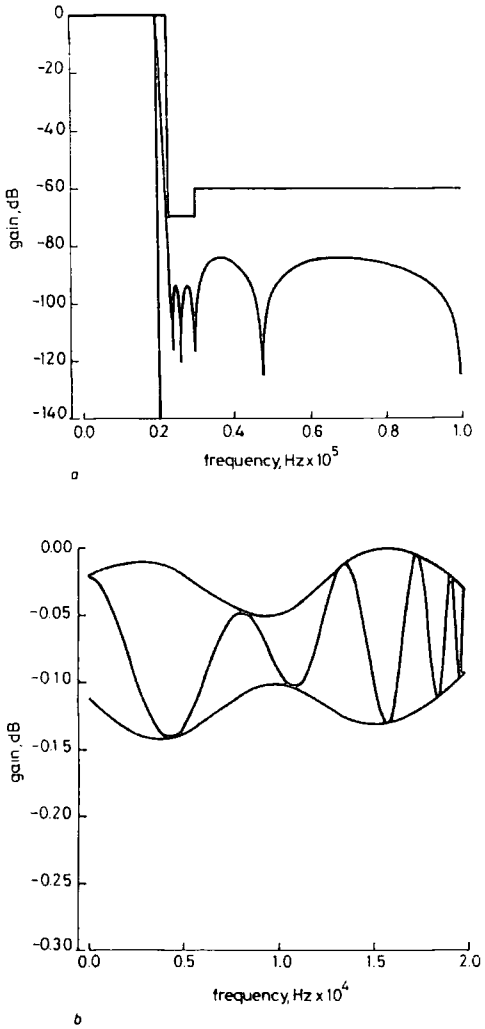

Fig. 6

a 11th-order lowpass filter with arbitrary passband and stopband specifications
b Passband detail

nonidealities in a 10th-order SC left-LUD ladder filter [30]. In fact, the optimisation process involves a few iterations of circuit analysis and redesign to inverse weighted specifications. However, it is significantly more efficient

Table 1: Comparison of group delay and stopband attenuation of filters in Fig. 8

Filter number	Name	Group delay variation, ms	Stopband rejection, dB
1	inverse Chebyshev	0.7	22
2	2-10-2	1.35	43
3	4-6-4	1.4	47
4	2-2-6-2-2	1.9	53
5	6-2-6	1.3	48
6	4-2-2-2-4	1.6	55
7	elliptic	2.2	58

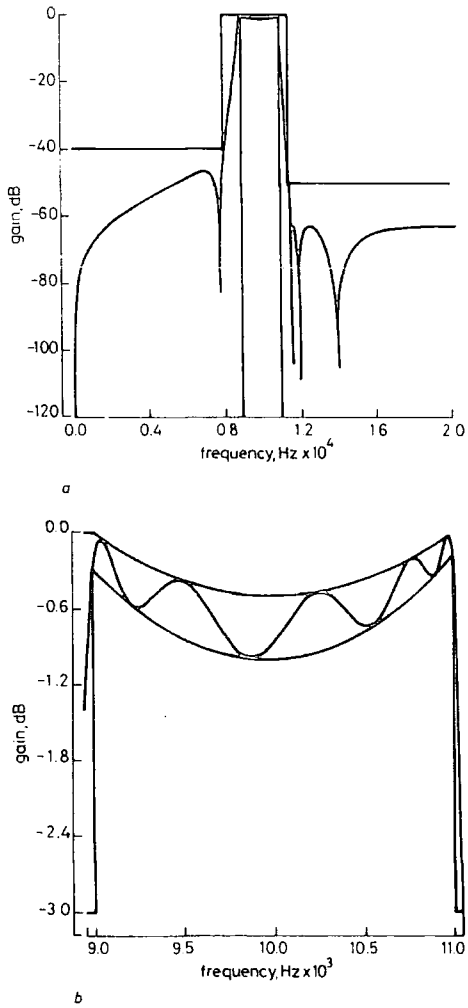

Fig. 7

a 10th-order asymmetric bandpass filter with sagging passband
b Passband detail

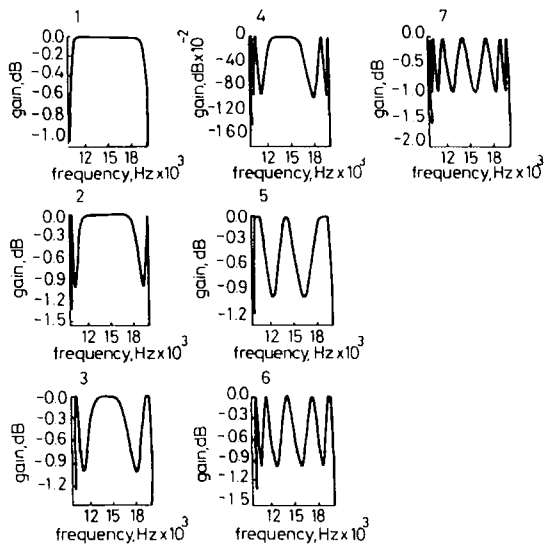

Fig. 8 *Sequence of 14th-order filter passbands employing high-order touch points*

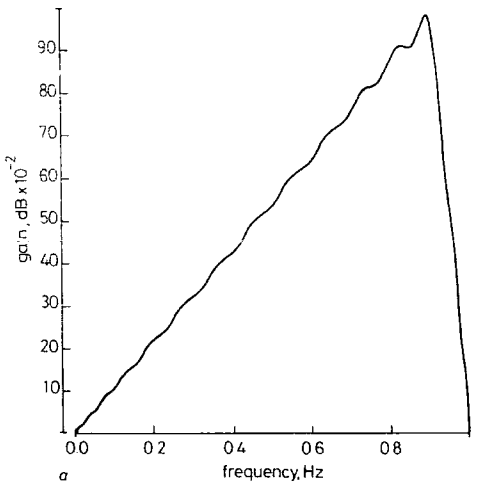

Fig. 9A *Length 69 FIR differentiator*

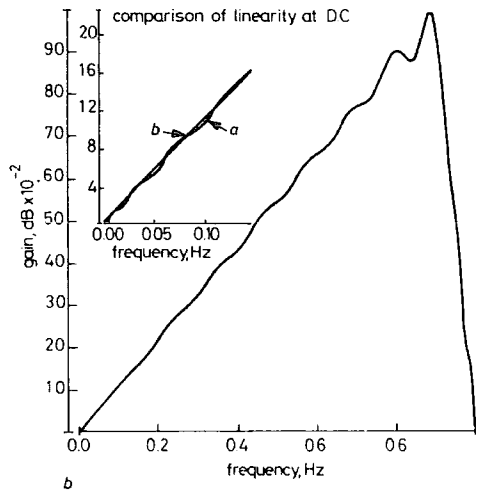

Fig. 9B *Length 69 FIR differentiator with 13th-order touch point at 0 Hz (linearity comparison shown as inset)*

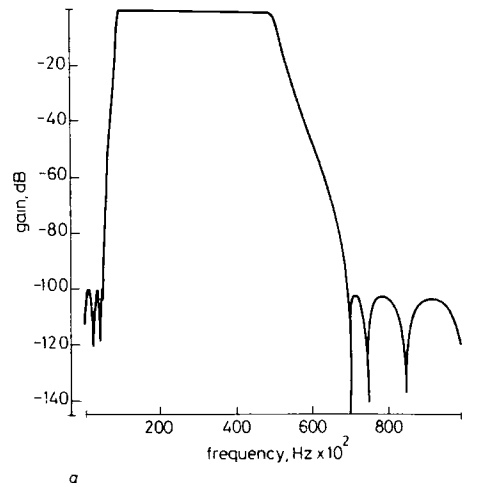

Fig. 10A *Wideband bandpass SC filter with sinc (x) distortion*

than a full circuit optimisation as the computation is dependent on the order of the filter rather than the number of components in the circuit (e.g. a 10th-order filter will be realised as a circuit with 40 components).

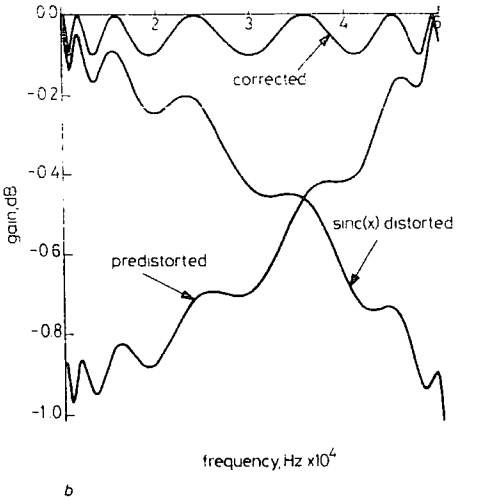

Fig. 10B *Sinc (x) correction*

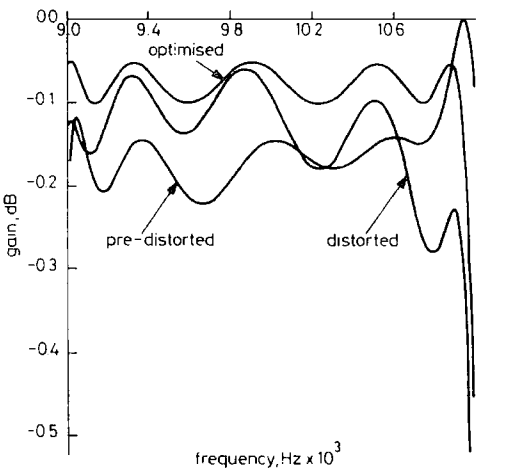

Fig. 11 *Optimisation of distortion in left-LUD SC filter due to op-amp and switch nonidealities*

4 Group delay approximation by allpass functions

The allpass function in the continuous time s-domain is

$$T(s) = \frac{X(-s)}{X(s)} \tag{38}$$

and the group delay function can be expressed as

$$\tau(\omega) = \frac{2\,\mathrm{Re}\left\{X(s)\dfrac{dX(-s)}{ds}\right\}\Big|_{s=j\omega}}{X(s)X(-s)} = \frac{N(\omega)}{D(\omega)} \tag{39}$$

As the denominator of eqn. 39 is a magnitude-squared function, it can be designed by standard Remez-type methods. The numerator function is an even function of s which can be formed by Hurwitz factorisation of the denominator polynomial.

4.1 New Remez-type algorithm

Consider now the problem of fitting the delay function to lower and upper boundaries $L(\omega)$ and $U(\omega)$ in a minimax sense over a frequency interval ω_{lo} to ω_{hi} (Fig. 12). It is required that

$$L(\omega) + C \leqslant \frac{N(\omega)}{X(j\omega)X(-j\omega)} \leqslant U(\omega) + C \tag{40}$$

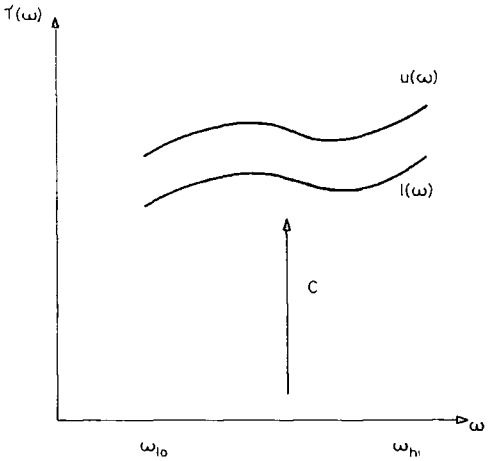

Fig. 12 *Approximation scheme for allpass group delay*

where the unknown constant delay offset C is necessary to ensure that

$$\int_0^\infty \tau(\omega)\, d\omega = n\pi \tag{41}$$

The constant C can be added without affecting the relative delay variation over the approximating region.

The allpass approximation method may be summarised by the following steps:

Step 1: Read lower and upper delay boundaries as piecewise boundaries $L(\omega)$ and $U(\omega)$ and equaliser order n.

Step 2: Set numerator function $N(\omega) = 1$ and guess constant $C = n\pi/(\omega_{hi} - \omega_{lo})$

Step 3: Apply Remez approximation techniques to solve

$$\begin{aligned} u(\omega) &= N(\omega)/(L(\omega) + C) \\ l(\omega) &= N(\omega)/(U(\omega) + C) \end{aligned} \tag{42}$$

over the range ω_{lo}–ω_{hi} using $D(x)$.

Step 4: Recalculate C as average delay constant between specified and approximated $\tau(\omega)$ over ω_{lo} to ω_{hi}.

Step 5: Form numerator function by Hurwitz factorisation of $D(\omega)$. Let the roots be $s_i = -a_i + jb_i$, then the delay function is

$$\tau(\omega) = 2\sum_{i=1}^{n/2} \left\{ \frac{a_i}{a_i^2 + (\omega + b_i)^2} + \frac{a_i}{a_i^2 + (\omega - b_i)^2} \right\} \tag{43}$$

The numerator function can be calculated from eqns. 43 and 44

$$N(\omega) = D(\omega) \times \tau(\omega) \tag{44}$$

Step 6: Repeat from step 2 until converged.

4.2 Computer implementation

The factorisation at step 5 can be made very efficient by utilising root positions from the previous factorisation as good initial guesses of roots for the present factorisation. Using Muller's quadratic interpolation method, this typically only requires two to three iterations per root [31].

Accuracy is preserved in the algorithm by avoiding representation of polynomials in coefficient form. Instead, Newton interpolated form is used at step 3 and factored form at step 4. Both forms are well conditioned on the approximation region, allowing high-order functions and narrow band allpass functions to be designed.

No theoretical proof has been obtained of convergence. However, experience has shown that convergence is good and that five or six cycles will generally suffice. The mechanism of the algorithm is dependent on the similarity between the group delay function $\tau(\omega)$ and the denominator magnitude function $D(\omega)$ in eqn. 39. The numerator is observed to be a smooth function over the approximating region, which warps the delay function of the denominator. Further theoretical investigation is being undertaken.

Digital allpass functions can be obtained by bilinear transformation. The delay specifications must be prewarped by a factor of $\cos(\omega T/2)^2$.

Group delay equalisation can be performed by combining $L(\omega)$ and $U(\omega)$ with the additive inverse of the group delay function of the amplitude filter. In this case, the total group delay of the allpass and amplitude filter stages will meet the desired specifications.

4.3 Computed examples

High-order touch points can be introduced into the delay function by the approximation methods of Section 2. Fig. 13 shows a 12th-order maximally flat group delay response (11th-order touch point). Fig. 14 shows a stepped form of group delay. Fig. 15 shows a 28th-order stepped group delay response with a 5th-order touch point at the lower band edge. Finally, a 28th-order allpass function is employed to equalise the delay of a 10th-order elliptic amplitude filter to a variation of ± 50 μs over the passband (Fig. 16).

4.4 Advantages

An iterative design procedure which works on the group delay function and employs Remez-type approximation has been proposed. Advantages of this algorithm are as follows:

(1) Good initial guesses of parameters are not required for convergence. As with the Remez approximation the

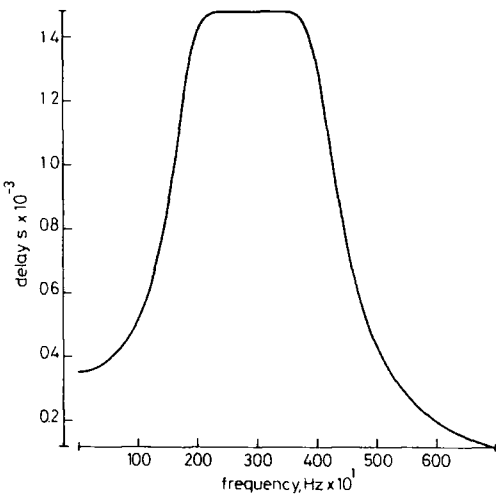

Fig. 13 *12th-order maximally flat allpass group delay approximation*

interpolation abscissae can be arbitrarily spaced on the approximation region (normally equidistantly).

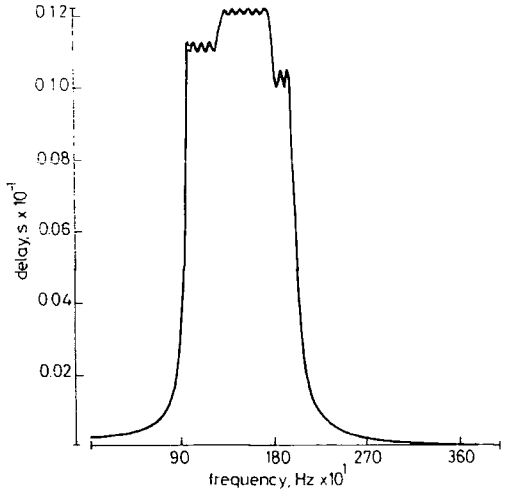

Fig. 14 *28th-order stepped allpass group delay approximation*

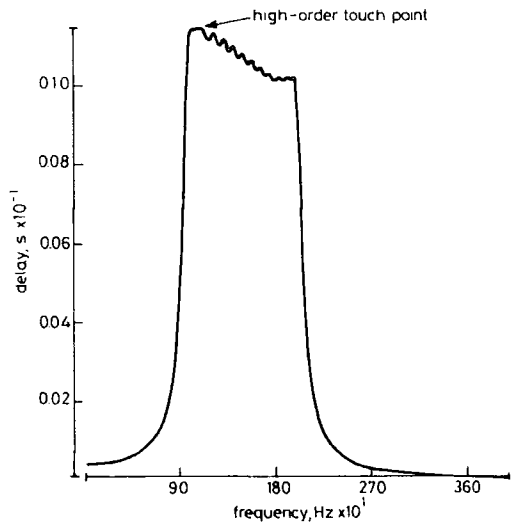

Fig. 15 *28th-order allpass group delay approximation with high-order touch point*

(2) The algorithm is well conditioned. Accuracy is maintained by representing the design polynomials in either Newton or factored form, instead of the ill conditioned coefficient form. High orders (>40) and narrow band design can be obtained. High-order designs are of some interest for digital filters where a very selective linear phase filter is required, which would be too expensive in nonrecursive form.

(3) Stability of the solution is guaranteed at all stages of the algorithm. The roots of the denominator of the allpass function must lie in the left-half plane because of the Hurwitz factorisation step.

(4) Computational requirements are light. The process only involves the fast Remez exchange and a factorisation step.

(5) The convergence of the algorithm is good.

In computer terms, this algorithm can be conveniently combined with amplitude approximation software, since it draws on the same numerical methods of interpolation and factorisation.

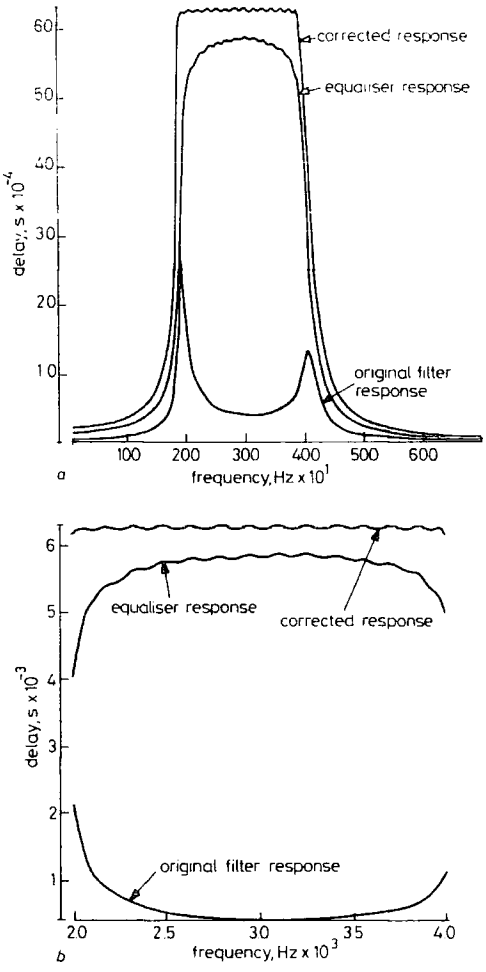

Fig. 16

a Equalisation of 10th-order elliptic filter delay response by 28th-order allpass function
b Passband detail

5 Conclusions

The amplitude and group delay response of filters can be designed with great flexibility by a series of extended Remez exchange algorithms. The amplitude response can be weighted arbitrarily in passband and stopband. High-order touch points have been introduced as a generalisation of the idea of maximum flatness. They are shown to offer the designer freedom to influence the filter characteristic in critical regions, when trade-off in the properties of group delay, passive sensitivity and stopband attenuation can be effected. Similar manipulations are possible in the group delay of an allpass function. The new algorithms are fast and efficient and have found successful application in the PANDDA filter compiler [30].

6 Acknowledgments

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PAPER 43

Canonical design of integrated ladder filters

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Indexing terms: Active filters, Ladder filters, Simulation

Abstract: Necessary conditions are given for the existence of a one-opamp-per-pole (canonical) realisation of a transfer function by an active ladder filter designed by operational simulation methods. The parity of the transfer function is shown to be critical. Some new design methods are applied to guarantee canonical low-sensitivity realisation of hitherto problematic filter types. These ensure a uniform progression of circuit structures with filter order. Hybrid matrix methods are shown to be useful to minimise the use of opamps in the simulation of arbitrary prototype ladder topologies.

1 Introduction

Low-sensitivity integrated active *RC* or switched-capacitor (SC) filter structures based on passive ladder simulation have been widely used for more than three decades [1, 2]. Among many alternatives, the most popular are the leapfrog and coupled-biquad circuits by virtue of their stray insensitivity [3, 4]. However, the advantages of these circuits have always been compromised by their relatively complicated design procedures, requiring different design techniques to meet different filter specifications. For this reason, matrix methods have been introduced to regularise the design procedures, ensuring that the steps involved do not change significantly according to the form of prototype and system order [5, 6]. Some inconsistencies still remain, and it is the purpose of this paper to address these.

An efficient integrated filter design will normally minimise the use of opamps, since these consume power and are sources of noise. Realisations with less than one opamp per pole are normally sensitive to component deviations and, in particular for SC circuits, to top and bottom plate stray capacitance. Therefore, it is generally accepted that one-opamp-per-pole realisations are canonical for low-sensitivity ladder circuits. However, this is not always achievable. For example, a 'pure' even-order lowpass elliptic function cannot be realised by a prototype passive ladder, unless the function is modified at the cost of poorer attenuation in the stopband [7]. Another problem exists for bandstop or highpass functions where, although a prototype can be synthesised, its straightforward active simulation would be unstable [2]. Hence it is of both theoretical and practical interest to develop a procedure for canonical ladder design for general forms of transfer function.

A necessary condition is derived to assess whether a given transfer function possesses a canonical ladder realisation. The outcome is shown to be dependent on the parity of the numerator. This condition is also believed to be sufficient, although a rigorous proof has not been obtained. For transfer functions with the wrong parity, a novel method is introduced to realise canonical ladder circuits by changing the parity of the numerator and compensating for the distortion in the simulation procedure. Thus a wide family of hitherto problematic transfer functions can be realised by canonic active circuits. A regular progression of circuits with increasing order is now possible, in the same way as for biquadratic cascade realisations. The simulation of arbitrary forms of ladder prototype which do not belong to the minimum node type is considered. Hybrid matrix methods are shown to be useful to ensure canonical realisations in these cases.

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2 Standard ladder simulation methods

A passive ladder can be described by the nodal equation

$$\boldsymbol{Y}\boldsymbol{V} = \boldsymbol{J} \tag{1}$$

where

$$\boldsymbol{Y}(s) = (s\boldsymbol{C} + s^{-1}\boldsymbol{\Gamma} + \boldsymbol{G}) \tag{2}$$

and where $\boldsymbol{C}$, $\boldsymbol{\Gamma}$ and $\boldsymbol{G}$ are matrices formed from the contributions of capacitors, inductors and resistors respectively, $\boldsymbol{V}$ is the vector of node voltages and $\boldsymbol{J}$ is the input vector. A design procedure has been developed to realise eqn. 1 by active *RC* and SC circuits [8]. This is done by creating a set of intermediate variables and decomposing the system eqn. 1 into two interrelated systems. For example, in active *RC* circuits this decomposition can be performed in the following ways.

2.1 Left matrix decomposition

Factorise the matrix $\boldsymbol{C}$ into

$$\boldsymbol{C} = \boldsymbol{C}_l\boldsymbol{C}_r \tag{3}$$

The following pair of equations is equivalent to eqn. 1:

$$\boldsymbol{C}_l\boldsymbol{W} = (-s^{-1}\boldsymbol{\Gamma} - \boldsymbol{G})\boldsymbol{V} - (-\boldsymbol{J}) \tag{4a}$$

$$\boldsymbol{C}_r\boldsymbol{V} = s^{-1}\boldsymbol{W} \tag{4b}$$

where $\boldsymbol{W}$ is the vector of intermediate variables.

2.2 Right matrix decomposition

$\boldsymbol{\Gamma}$ can also be factorised as

$$\boldsymbol{\Gamma} = \boldsymbol{\Gamma}_l\boldsymbol{\Gamma}_r \tag{5}$$

The following pair of equations is equivalent to eqn. 1:

$$\boldsymbol{C}\boldsymbol{V} = -s^{-1}[\boldsymbol{\Gamma}_1\boldsymbol{W} + \boldsymbol{G}\boldsymbol{V} + (-\boldsymbol{J})] \tag{6a}$$

$$\boldsymbol{I}\boldsymbol{W} = s^{-1}\boldsymbol{\Gamma}_r\boldsymbol{V} \tag{6b}$$

The details of the design procedure can be found in [5, 6, 8, 9], covering the well known leapfrog and coupled-biquad methods together with some new ones, notably those obtained by adopting LU decompositions [10]. As system eqn. 1 with size n can at most realise a $2n$th-order or a $(2n-1)$th-order transfer function for an even-order or an odd-order system respectively, then:

Definition 1: System eqn. 1 with size n is said to represent a canonical ladder prototype if it realises a $2n$th-order or a $(2n-1)$th-order transfer function.

In [10] it has been shown that system eqn. 1 can always be simulated by an active RC or SC ladder with $2n$ opamps; alternatively, if the transfer function is of order $2n-1$ a simulation with $2n-1$ opamps is possible. Therefore the problem of finding a canonical standard ladder simulation becomes that of finding a canonical ladder prototype.

3 Canonical ladder prototypes

In the following, conditions will be derived for a ladder prototype eqn. 1 to be canonical. First some properties of the prototype eqn. 1 are stated as follows:

Remark 1: The nodal description of a doubly-terminated ladder synthesised from the minimum node two-port sections in Fig. 1 has the following properties:

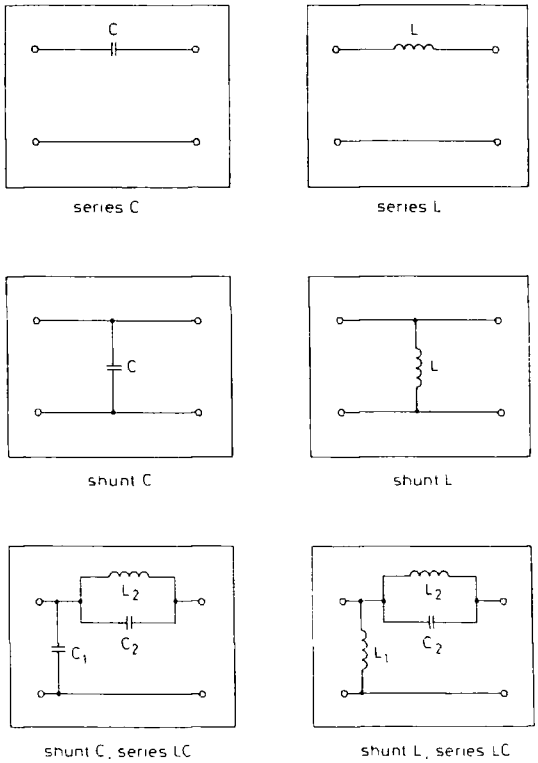

Fig. 1 *Minimum node two-port sections*

(*a*) $\boldsymbol{C}$, $\boldsymbol{\Gamma}$ and $\boldsymbol{G}$ are all tridiagonal matrices. So $\boldsymbol{Y}$ is also tridiagonal.

(*b*) $\boldsymbol{J}$ has only one nonzero element, i.e. $\boldsymbol{J} = [J_1, 0, \ldots, 0]^T$.

(*c*) $\boldsymbol{G}$ has only two nonzero elements $g_{11} = g_{in}$ and $g_{nn} = g_L$, so that in general

$$y_{i+1,i} = sc_{i+1,i} - s^{-1}\gamma_{i+1,i} \tag{7}$$

(*d*) The output is the nodal voltage v_n.

The constraints for a transfer function to be realisable by a canonical doubly-terminated ladder are as follows:

Theorem 1:

(*a*) The numerator of the transfer function v_n/J_1 of a canonical even-order doubly-terminated ladder is an odd polynomial.

(*b*) The numerator of the transfer function v_n/J_1 of an odd-order doubly-terminated ladder is an odd polynomial if $|\boldsymbol{C}|$ is nonsingular or an even polynomial if $|\boldsymbol{\Gamma}|$ is nonsingular.

Proof: From remark 1 the nodal admittance matrix of a doubly-terminated ladder is tridiagonal. By Cramer's rule [12] it can be found for the output v_n that

$$\frac{v_n}{J_1} = \frac{\pm\Delta_{1n}}{\Delta(s)} \tag{8}$$

where $\Delta(s)$ is the determinant of $\boldsymbol{Y}$ and Δ_{1n} is the appropriate cofactor. It can be shown that

$$\frac{v_n}{J_1} = \frac{\prod_{i=1}^{n-1}[sc_{i+1,i} - s^{-1}\gamma_{i+1,i}]}{\Delta(s)} \tag{9}$$

where $\boldsymbol{\Gamma} = \{\gamma_{i,j}\}$ and $\boldsymbol{C} = \{c_{i,j}\}$. Let v_n/J_1 be expressed in the form of a rational function

$$\frac{v_n}{J_1} = \frac{N(s)}{D(s)} \tag{10}$$

$D(s)$ and $N(s)$ are the denominator and numerator polynomials respectively, and they contain only non-negative powers of s. Consider first the case of an even canonical realisation. Notice that by using the Laplace expansion [12] repeatedly the determinant of $\Delta(s)$ can be expanded as follows, where n is the size of the coefficient matrices:

$$\Delta(s) = |\boldsymbol{C}|s^n + a_{n-1}s^{n-1} + \cdots + a_{-(n-1)}s^{-(n-1)} + |\boldsymbol{\Gamma}|s^{-n} \tag{11}$$

A ladder realising a $2n$th-order function must have a nonsingular $\boldsymbol{\Gamma}$, and so the denominator can be rearranged to be a $2n$th-order polynomial as

$$D(s) = s^n\Delta(s) \tag{12a}$$

and the numerator becomes

$$N(s) = s^n\prod_{i=1}^{n-1}[sc_{i+1,i} - s^{-1}\gamma_{i+1,i}] \tag{12b}$$

Here $c_{i+1,i}$ and $\gamma_{i+1,i}$ (for all i) cannot both be zero, otherwise the transfer function would be zero. Suppose $c_{i+1,i}$ are nonzero for all i; then it can be seen that $N(s)$ is a $(2n-1)$th-order polynomial with only odd terms. If

any $c_{i+1,i}$ is zero then $N(s)$ will reduce to a $(2n-3)$th-order polynomial (since in this case $\gamma_{i+1,1}$ must be nonzero) and $N(s)$ will stay odd. It is easy to deduce that $N(s)$ will remain odd for cases of more zero $\{c_{i+1,i}\}$. The same reasoning can be applied to the cases that some $\{\gamma_{i,i+1}\}$ are zero.

Now consider the case of odd-order design, where either C or Γ must be singular to make $D(s)$ in eqn. 12*a* odd. If Γ is nonsingular, exactly the same reasoning as for the even case can be used to show that $N(s)$ must be odd. If C is nonsingular then

$$D(s) = s^{n-1}\Delta(s) \tag{13a}$$

$$N(s) = s^{n-1}\prod_{i=1}^{n-1}[sc_{i+1,i} - s^{-1}\gamma_{i+1,i}] \tag{13b}$$

and it is easily shown that $N(s)$ must be an even polynomial.

Theorem 1 establishes some necessary conditions for a transfer function to have a canonical realisation. It appears that these conditions are also sufficient for realisability provided that the transfer function is stable.

It is seen from theorem 1 that the constraint on the parity of the numerator is related to the singularity of the matrices C and Γ. The singularities, however, cannot be arbitrarily chosen.

Theorem 2: A doubly-terminated ladder has a nonzero response at $\omega = \infty$ only if C is singular and has a nonzero response at $\omega = 0$ only if Γ is singular.

Proof: Let $s = j\omega$. From eqn. 12 it can be seen that when $\omega \to \infty$,

$$\Delta(s) \to |C| s^n + a_{n-1}s^{n-1} \tag{14}$$

and from eqn. 9 the numerator is at most to the power of s^{n-1}. Therefore if $|C|$ is not zero then eqn. 9 must be zero. Similar reasoning can be used at $\omega \to 0$.

It is mandatory that lowpass transfer functions have nonzero values at $\omega = 0$ and highpass and bandstop functions at $\omega = \infty$. This indicates that the singularity of the matrices is predetermined by the filtering types, and therefore the parity of the numerators of odd-order cases is also constrained.

Since the singularities of C and Γ mean that their rank can at most be $n-1$, according to eqn. 14 a list of the upper bounds for various filtering types by a ladder with order n is obtained in Table 1.

Table 1: Upper bounds on system order for various classes of ladder filter with *n* nodes

Classes	Constraint	Upper bound of system order
Lowpass	$H(0) \neq 0$ Γ singular	$2n-1$
Bandpass		$2n$
Highpass	$H(\infty) \neq 0$ C singular	$2n-1$
Bandstop	$H(0) \neq 0$ $H(\infty) \neq 0$ both C and Γ singular	$2n-2$

It is easily seen that canonical designs can be achieved only by bandpass, odd-order lowpass and odd-order highpass. For other cases, constraints given in theorem 2 make a canonical realisation impossible. In the succeeding sections it will be seen that a noncanonical ladder prototype will lead to an integrated circuit simulation of excessive size, unless some complicated procedure is adopted. It will also be shown that the wrong parity of numerator can be easily corrected, and a simple technique is introduced to eliminate the error caused by this modification. This results in a unified procedure, with very regular structures, to realise a wide family of transfer functions. There is a uniform progression in the form of the circuit structures regardless of the type of specification or order.

4 Canonical ladder simulation by modified prototype

The numerators of the transfer functions considered in this paper are restricted to be polynomials with purely even or odd terms. This means their zeros are restricted to lie on or have quadrantal symmetry about the imaginary axis. Such a constraint is valid for most filter design problems. With this constraint and from theorem 1 the problem concerned in this paper has been greatly simplified: whether a given transfer function can be realised by a canonical standard ladder depends solely on the numerator parity.

The most common example of a transfer function with the wrong parity is an even-order 'pure' elliptic function with an even-order numerator. It is well known that this kind of function cannot be realised by a doubly-terminated ladder [13]. Traditionally the solution to this problem is to modify the numerator by moving a pair of finite zeros to infinity [7], which incurs the penalty of a loss of stopband attenuation (Fig. 2).

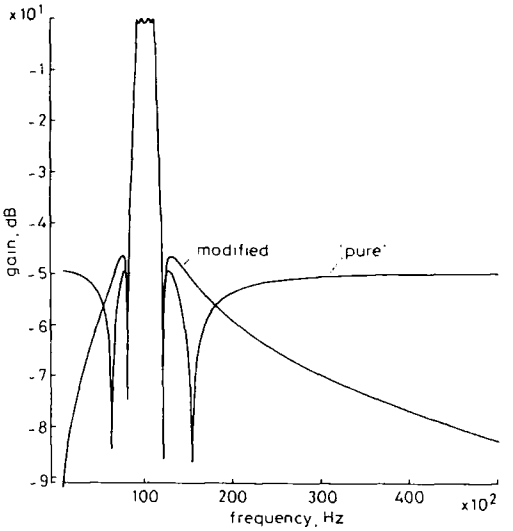

Fig. 2 *Modified and 'pure' eighth-order bandpass elliptic functions*

A new scheme is introduced here to realise the transfer function exactly without any sacrifice of filtering quality. Let $H(s)$ be a transfer function with all its zeros on the imaginary axis or at infinity. If the constraints of theorem 1 are not met, or more precisely if $N(s)$ has the wrong parity, some simple manipulation of the transfer

function can be made to cope with the problem. Consider three possibilities:

(*a*) The numerator of H is a constant.

(*b*) The numerator of H has a single root at $\omega_i = 0$.

(*c*) The numerator of H has a pair of imaginary roots at $\pm\omega_i$ (ω_i can be zero).

To change the parity, manipulate as follows:

$$\left.\begin{array}{l}(a)\ \text{Let } H'(s) = H(s)s.\\ (b)\ \text{Let } H'(s) = H(s)s \quad \text{or} \quad H'(s) = H(s)/s.\\ (c)\ \text{Let } H'(s) = H(s)s/(s^2 + \omega_i^2).\end{array}\right\} \tag{15}$$

Then the parity of H' is opposite to that of H, and $H'(s)$ can now be realised by a canonical prototype ladder described by the nodal equation

$$(sC + s^{-1}\Gamma + G)V = J \tag{16}$$

4.1 Canonical ladder simulation by active RC circuits

A system realising the original transfer function $H(s)$ can be obtained by multiplying the input vector J by the inverse of the modification function. For case (*c*) we have

$$(sC + s^{-1}\Gamma + G)V = (s + \omega_i^2 s^{-1})J \tag{17}$$

This system can now be expressed in realisable form by matrix methods [5, 6].

4.1.1 Left matrix decomposition form: Let $C = C_l C_r$. Then the system can be written as

$$C_l W = -s^{-1}[\Gamma V + GV + \omega_i^2(-J)] \tag{18a}$$

$$C_r V = s^{-1}W - C_l^{-1}(-J) \tag{18b}$$

4.1.2 Right matrix decomposition form: Let $\Gamma = \Gamma_l \Gamma_r$. Then the system can be written as

$$CV = -s^{-1}(\Gamma_l W + GV) - (-J) \tag{19a}$$

$$W = s^{-1}[\Gamma_r V + \omega_i^2 \Gamma_l^{-1}(-J)] \tag{19b}$$

Active RC networks can be obtained directly from these two equations. It is found that the most efficient method in either case is to use UL factorisation, which minimises the required number of input branches (only two).

The prototype in Fig. 3 is simulated by the two canonical eighth-order left-ULD and right-ULD active RC circuits shown in Fig. 4. These canonical designs differ from standard ones in the position of the input stage branches.

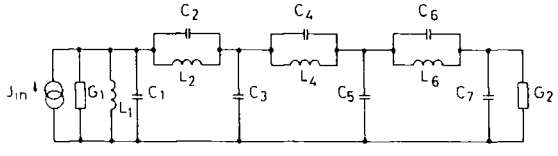

Fig. 3 *Eighth-order prototype ladder designed from partitioned transfer function*

4.2 Canonical discrete ladder simulations

The design of a discrete ladder simulation starts from the modified prototype system eqn. 17, which after bilinear transformation becomes

$$\left(\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}C + \frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}}\Gamma + G\right)V = \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}J + \frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}}\omega_i^2 J \tag{20}$$

The system can be rearranged as

$$\left(\frac{1}{\Psi}A + \Phi B + D\right)V = \left[(\omega_i^2 + 1)\frac{1}{\Psi} + 4\Phi\omega_i^2\right]J \tag{21a}$$

$$A = 2/TC + T/2\Gamma + G \qquad B = 2T\Gamma$$

$$D = 2G \qquad \Psi = z^{-1}/(1 - z^{-1}) \tag{21b}$$

$$\Phi = 1/(1/z^{-1})$$

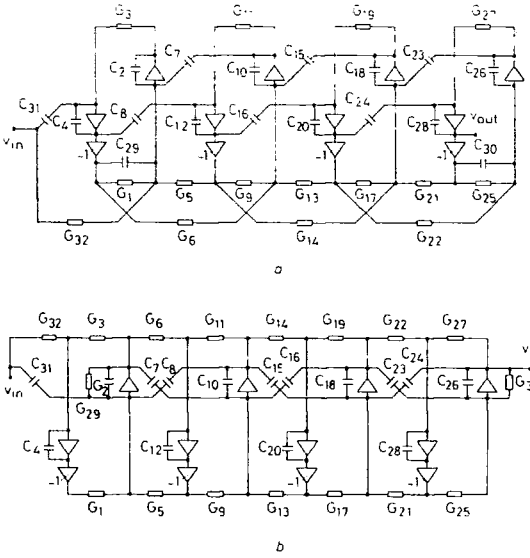

Fig. 4 *Canonic eighth-order active RC ladder filters*

a Left-ULD active *RC* circuit

b Right-ULD active *RC* circuit

or

$$\left(\frac{1}{\Psi}A + \Phi B + D\right)V = \left[(\omega_i^2 + 1)\frac{1}{\Phi} + 4\Psi\omega_i^2\right]J \tag{21c}$$

$$A = 2/TC + T/2\Gamma - G \qquad B = 2T\Gamma$$

$$D = 2G \qquad \Psi = z^{-1}/(1 - z^{-1}) \tag{21d}$$

$$\Phi = 1/(1 - z^{-1})$$

The above equations can be linearised respectively as follows.

4.2.1 Left matrix Decomposition

$$A_l W = -(\Phi B + G)V - \Phi 4\omega_i 2(-J) \tag{22a}$$

$$A_r V = \Psi W - A_l^{-1}(\omega_i^2 + 1)(-J) \tag{22b}$$

4.2.2 Right matrix decomposition

$$AV = -\Phi(B_l W + GV) - (\omega_i^2 + 1)(-J) \tag{23a}$$

$$W = \Psi(B_r V + 4\omega_i^2 B_l^{-1})(-J) \tag{23b}$$

The prototype in Fig. 3 is simulated by the two canonic eighth-order left-ULD and right-ULD SC circuits shown in Fig. 5. The sensitivity behaviour of the new structures must be examined, as they are no longer strictly ladder simulations and would seem to depart from Orchard's low-sensitivity criterion [1]. From the following examples, and many others studied by computer simulation, the sensitivity for the new structures has been confirmed to be much better than their biquad counterparts, and very close to traditional ladder simulations.

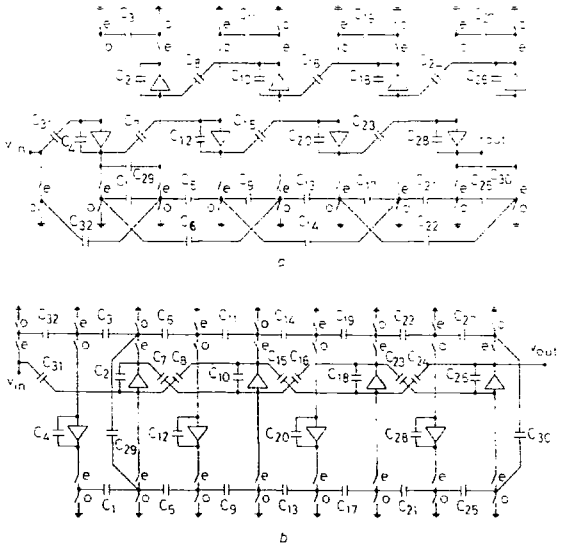

Fig. 5 *Canonic eighth-order SC ladder filters*
a Left-ULD SC circuit
b Right-ULD SC circuit

5 Circuit design examples

The circuits of Fig. 5 are generated by the PANDDA filter compiler [14] to realise the 'pure' eighth-order elliptic bandpass function of Fig. 2. The design data are given in Table 2. A passband sensitivity comparison is shown in Fig. 6 with a corresponding cascade biquad design. A left-ULD realisation proves preferable in all respects, having lower sensitivity and total capacitance.

Table 2: Design data for eighth-order bandpass filter realisations

Comparison of canonical left-ULD ladder and biquad SC filters		
	ULD	Biquad
Total capacitance	188.03	193.91
Capacitance spread	57.38	41.54
Average capacitor	5.88	6.46
Number of capacitors	32	30
Number of switches	34	36
Number of opamps	8	8

Capacitor values of left-ULD SC ladder filter in Fig. 5*a*

$C_1 = 18.20$	$C_2 = 57.38$	$C_3 = 2.28$	$C_4 = 7.69$	$C_5 = 3.82$
$C_6 = 1.05$	$C_7 = 1.00$	$C_8 = 4.80$	$C_9 = 5.25$	$C_{10} = 14.09$
$C_{11} = 3.12$	$C_{12} = 10.72$	$C_{13} = 1.00$	$C_{14} = 1.12$	$C_{15} = 1.36$
$C_{16} = 5.36$	$C_{17} = 3.96$	$C_{18} = 12.66$	$C_{19} = 1.00$	$C_{20} = 2.87$
$C_{21} = 1.00$	$C_{22} = 2.01$	$C_{23} = 1.26$	$C_{24} = 3.21$	$C_{25} = 2.57$
$C_{26} = 11.05$	$C_{27} = 1.00$	$C_{28} = 2.16$	$C_{29} = 2.05$	$C_{30} = 1.00$
$C_{31} = 1.00$	$C_{32} = 1.00$			

Clock frequency = 200 kHz; Passband ripple < 1 dB; Stopband attenuation > 50 dB; Lower passband edge = 9 kHz; Upper passband edge = 11 kHz

The passive ladder of Fig. 3 can also be used to realise the partitioned transfer function of an eighth-order lowpass function in Fig. 7. The circuits of Fig. 5 are once again employed. The design data for a right-ULD SC realisation are given in Table 3. A sensitivity comparison is shown in Fig. 8. The left-ULD has a serious peak towards low frequency, a known problem for lowpass design, and would not normally be considered. The right-ULD design has very low sensitivity, well below the cascade biquad realisation. In this case, the ladder has a larger total capacitance.

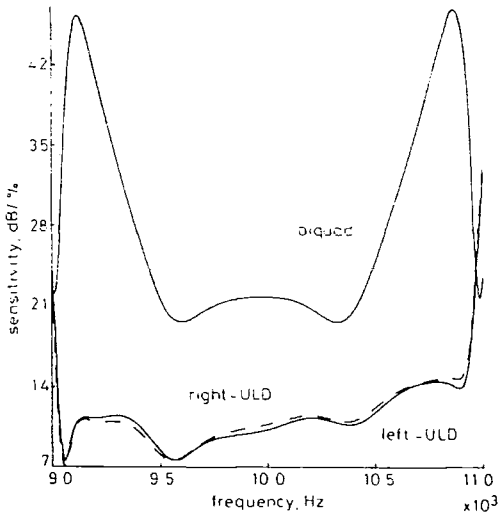

Fig. 6 *Passband sensitivity comparison for canonic eighth-order bandpass filters*

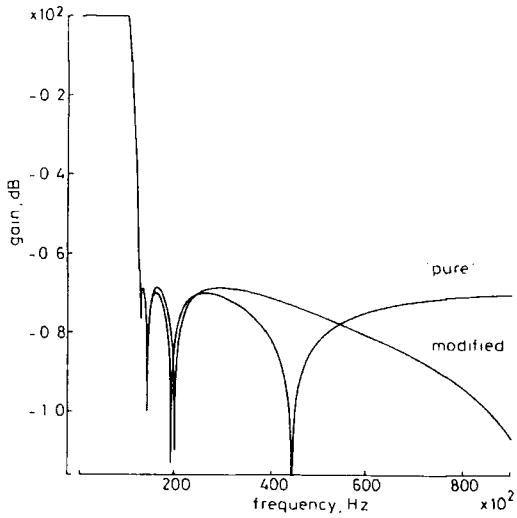

Fig. 7 *Modified and 'pure' eighth-order lowpass elliptic functions*

Table 3: Design data for eighth-order lowpass filter realisations

Comparison of canonical right-ULD ladder and biquad SC filters		
	ULD	Biquad
Total capacitance	189.43	107.83
Capacitance spread	75.16	14.08
Average capacitor	5.92	3.59
Number of capacitors	32	30
Number of switches	34	36
Number of opamps	8	8

Capacitor values of right-ULD SC ladder filter in Fig. 5*b*

$C_1 = 13.15$	$C_2 = 75.16$	$C_3 = 2.21$	$C_4 = 7.96$	$C_5 = 13.99$
$C_6 = 1.04$	$C_7 = 1.00$	$C_8 = 6.15$	$C_9 = 2.19$	$C_{10} = 11.61$
$C_{11} = 1.00$	$C_{12} = 6.33$	$C_{13} = 2.30$	$C_{14} = 1.27$	$C_{15} = 1.04$
$C_{16} = 1.72$	$C_{17} = 1.10$	$C_{18} = 5.86$	$C_{19} = 1.00$	$C_{20} = 6.72$
$C_{21} = 1.00$	$C_{22} = 1.66$	$C_{23} = 6.01$	$C_{24} = 1.45$	$C_{25} = 2.49$
$C_{26} = 3.11$	$C_{27} = 1.00$	$C_{28} = 4.27$	$C_{29} = 2.61$	$C_{30} = 1.00$
$C_{31} = 1.00$	$C_{32} = 1.00$			

Clock frequency = 200 kHz; Passband edge = 10 kHz; Passband ripple < 0.1 dB, Stopband attenuation > 70 dB.

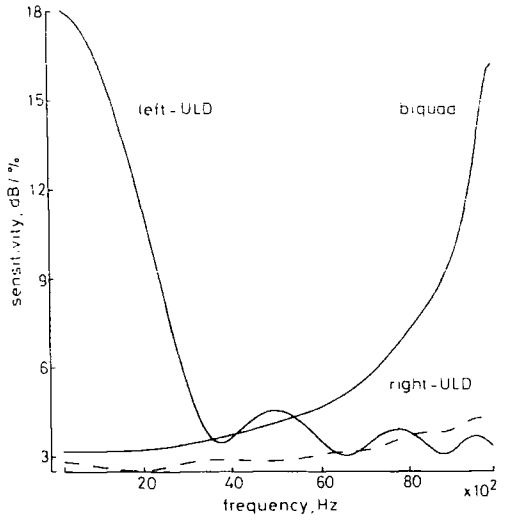

Fig. 8 *Passband sensitivity comparison for canonic eighth-order lowpass filters*

6 Hybrid matrix approaches

The above techniques, which guarantee the existence of a canonic ladder simulation, require restrictions to be made on the structure of the passive prototype. Given a prototype which does not have this structure, how can a canonic simulation be obtained? The restrictions were made in order to provide an efficient matrix nodal description. For arbitrary prototypes, more general hybrid matrix descriptions can be adopted to minimise the size of the matrix systems and their resulting simulated circuits. The drawback of the hybrid method is that there is no unified rule. The exact design method depends on the individual prototype structures and the selection of the internal variables, which can be seen from the following examples.

An even-order lowpass circuit shown in Fig. 9*a* has $n + 1$ nodes but the filter order is $2n$. The rank of $\boldsymbol{\Gamma}$ is n as there are n inductors in the circuit, making the total number of opamps required $2n + 1$; so even a leapfrog design cannot directly provide a canonical circuit. However, if a single mesh current i_n is selected as a variable to replace v_{n-1}, the last two row equations will have the following form:

$$\left\{ s \begin{bmatrix} \cdots & & \\ \cdots & c_{m-2} & c_{m-1} + c_{m-2} & 0 \\ & & \cdots & L_m \end{bmatrix} + s^{-1} \begin{bmatrix} \cdots & & \\ \cdots & L_{m-1}^{-1} & L_{m-1}^{-1} & 0 \\ & & \cdots & 0 & 0 \end{bmatrix} + \begin{bmatrix} \cdots & & \\ \cdots & 0 & 1 \\ \cdots & -1 & 1/g_L \end{bmatrix} \right\} \begin{bmatrix} -v_{n-1} \\ v_n \\ i_n \end{bmatrix} = \boldsymbol{J} \quad (24)$$

The output is now i_n, which differs from v_{n+1} by only a constant g_L. The rank of matrix $\boldsymbol{\Gamma}$ will be $n - 1$ since the contribution of the mth inductor is now moved to the first matrix. If a right-LUD decomposition method $\boldsymbol{\Gamma} = \boldsymbol{LU}$ is used, two zero rows will appear in matrix $\boldsymbol{U}$. According to eqn. 6*b* the intermediate variable vector $\boldsymbol{W} = s^{-1}\boldsymbol{UV}$ contains two variables which can be deleted. This means that the total number of variables is $2n$ and only n opamps are necessary, providing a canonical solution.

The same technique can be applied to the left decomposition designs for a $2n$-order bandpass prototype (Fig. 9*b*) derived from an nth-order lowpass reference with n even. There are $n + 1$ nodes in the ladder, so a nodal description is not efficient. If a single mesh current i_n is selected as a variable to replace v_n and v_{n+1}, the last two row equations can be arranged into the following form, providing a canonical solution:

$$\left\{ s \begin{bmatrix} \cdots & & \\ \cdots & c_{m-2} & c_{m-1} + c_{m-2} & 0 \\ & & \cdots & L_m \end{bmatrix} + s^{-1} \begin{bmatrix} \cdots & & \\ \cdots & L_{m-1}^{-1} & L_{m-1}^{-1} & 0 \\ & & \cdots & c_m^{-1} \end{bmatrix} + \begin{bmatrix} \cdots & & \\ \cdots & 0 & 1 \\ \cdots & -1 & 1/g_L \end{bmatrix} \right\} \begin{bmatrix} -v_{n-2} \\ v_{n-1} \\ i_n \end{bmatrix} = \boldsymbol{J} \quad (25)$$

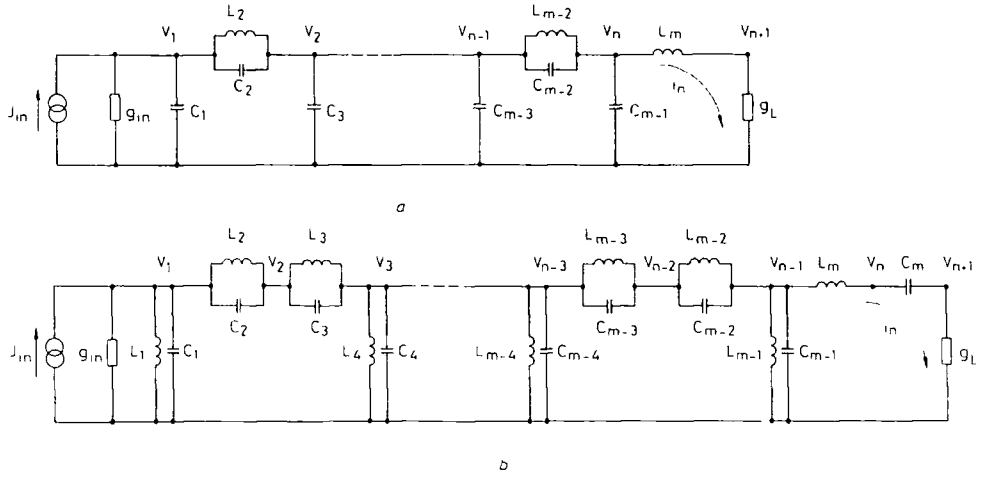

Fig. 9 *Canonical simulation scheme*

a Even-order lowpass prototype
b 2nth-order bandpass prototype

7 Conclusion

An objection to the use of active ladder simulation filters is the difficulty of guaranteeing a canonic filter circuit. By standard methods, a passive ladder realisation may not exist or the simulation of the ladder would yield non-canonic circuits. This paper has presented a set of conditions on the transfer function and prototype structure whereby a canonic simulation is obtainable. For the exceptions, a new design method and new canonic ladder structures are proposed. These circuits are applicable to all active technologies and are stray insensitive in switched-capacitor implementation. Despite departing from the strict conditions for low-sensitivity passive ladder simulation, the circuits are shown to have very good sensitivity properties. Although competitive with biquad cascade realisations for certain types of transfer function, there is some cost in component spread for others. The design is formulated in a very regular manner in terms of matrix equations, making it highly suited to computer implementation. The problem of obtaining a canonic simulation of an arbitrary ladder sturcture is demonstrated to be one of properly choosing the system variables to ensure a sparse matrix description. Some example techniques are illustrated for symmetric bandpass elliptic ladder filters.

8 Acknowledgment

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Design Optimization and Testing of a GaAs Switched-Capacitor Filter

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Abstract—**This paper is concerned with the design of high frequency switched-capacitor filters implemented using GaAs MESFET technology. The design techniques developed are illustrated by means of a 2nd-order switched-capacitor bandpass filter designed to operate at a switching frequency of 500 MHz. The design incorporates a recently proposed operational amplifier architecture with a simulated gain of 60 dB and a recently proposed switch driver circuit. Amplifiers are characterized in terms of settling time performance and a general procedure is presented for optimization of the switched-capacitor circuit to maximize switching frequency. Measurements on a fabricated chip confirm the design of the filter and its components.**

I. Introduction

HIGH-precision tunable sampled-data analog filters can be integrated using the switched-capacitor (SC) circuit approach. Using presently available CMOS technology, switching frequencies up to 30 MHz have been achieved [1] and an absolute maximum frequency limit of 130 MHz has been predicted [2]. The higher peak electron velocity and resulting higher lowfield electron mobility of GaAs have been exploited for high-speed analog sampled-data signal processing applications [3]. In [4] and [5], a switching frequency of 250 MHz has been achieved for a GaAs 2nd-order bandpass filter with midband frequency of 10 MHz and Q-factor of 16. The accuracy of the midband frequency was only a few percent, which is inadequate for precision applications. The errors were attributed to low amplifier gains of 40 dB; low capacitor Q-factors were due to the use of polyimide dielectric and suspected back-gating effects [7].

Larson *et al.* [6] have accepted a low value for amplifier gain and have proposed the use of finite gain insensitive SC circuits. A more suitable capacitor dielectric, namely silicon nitride, was used, and novel switching circuits with the introduction of diodes to reduce the signal dependence of clock feedthrough were explored. Excellent filter results for switching frequencies up to 100 MHz were obtained.

This paper is concerned with the design, optimization, and testing of a GaAs 2nd-order bandpass filter using a recently proposed high-gain operational amplifier [8], which can have a low frequency gain of over 60 dB, and a recently proposed switch control circuit [9]. The amplifier is characterized in terms of its minimum settling time and the SC circuit is optimized for maximum possible clock frequency. The design procedure is evaluated by measurements on a fabricated chip. Some of the work described in this paper has been reported in [10], [11], and [12].

II. Filter Architecture

A well-demonstrated approach for the realization of high-order SC filters is to interconnect a number of parasitic insensitive integrators according to a leapfrog configuration that simulates a low sensitivity LCR filter [13]. For the evaluation of SC filters realized in GaAs technology, a 2nd-order bandpass filter consisting of two such integrators was chosen as shown in Fig. 1 [5]. The circuit requires a nonoverlapping clock as shown in Fig. 2 with two phases (E and O) and guard intervals (INT) where all switches are open. The capacitor values shown provide a Q-factor of 16, a midband gain of unity, and a midband frequency equal to 1/25th of the switching frequency, which is a typically chosen value taking into account the problems of aliasing and imaging [13].

III. Switch Driver Circuits

When SC circuits are implemented in CMOS technology, the switches can be realized by MOSFET's, the gates of which may be driven from the negative to the positive power supply rails to open and close the switches. This is possible because in CMOS technology the gate is separated from the channel by an insulating layer (oxide). The situation in GaAs technology is quite different in that the gate forms a Schottky diode with the channel, and therefore, large gate currents will flow if the gate voltage exceeds the voltage at the source or drain by more than about 0.5 V, resulting in a failure of normal FET opera-

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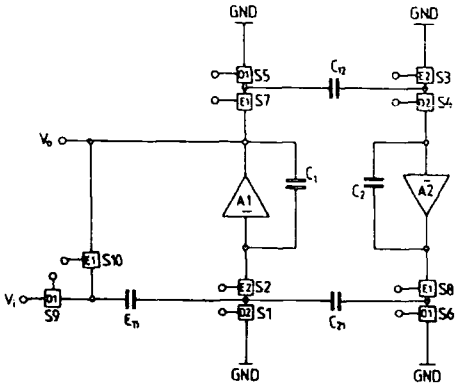

Fig. 1. 2nd-order SC filter circuit ($C_{11} = 1$, $C_{12} = C_{21} = 15.937$, $C_1 = C_2 = 63.330$).

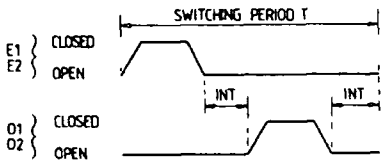

Fig. 2. 2-phase clock waveforms.

tion. Thus we cannot apply the simple switching arrangement used in CMOS SC circuits.

The switches in Fig. 1 may be divided into two categories. The switches adjacent to the amplifier inputs (e.g. S1–S4) are switching signals close to ground and they may be realized as a MESFET with gate voltage switched between 0 V (on-state) and $V1$, where $V1 < VT$ (off-state). The remaining switches in Fig. 2 (S5–S10) are associated with the integrator input terminals. Four of these switches (S7–S10) are switching large analog signals, and it is necessary to introduce a switch control circuit (SCC) for them in order to limit the high-level voltage on the switching MESFET gate to track the analog voltage so that the switching MESFET's gate Schottky diode is not forward biased [5]. The remaining two switches (S5 and S6) are switching signals at around 0 V and, therefore, do not strictly need the introduction of SCC's; they were, however, included in order to obtain balanced drive signals for each pair of switches.

A number of SCC circuits have been previously employed [4]–[6], [9], [12], all of which can be derived from the general architecture shown in Fig. 3(a). The digital input is fed to an inverter, the output of which drives the gate of the switch MESFET M1. The output of the inverter switches between the inverter negative supply voltage $-V_s$, which opens the switch, and the inverter positive supply voltage. The inverter positive supply is derived from the output of a unity-gain voltage buffer, the input voltage of which is the voltage on one of the switch terminals X. As a result, the voltage on the gate of M1 is equal to the voltage at node X, as required, when the

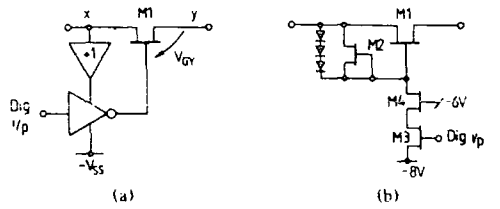

Fig. 3. Switch control circuits for GaAs technology. (a) Basic architecture. (b) Circuit adopted (Gatewidths: M1—50 μm; M2—15 μm; M3, M4—24 μm).

switch is in the closed state. It may appear that the gate diode of M1 might become forward biased if the voltage at Y is significantly less than that at X at the start of a closing transition. In fact, this does not occur because, well before the voltage V_{GY} reaches the critical 0.5 V, the switch would start to go into its closed state, tending to make the voltage of Y change towards that at X. Although several SCC circuits have been proposed, they have several deficiencies including voltage buffer gain errors, large chip area, high power consumption, and high levels of signal-dependent clock feedthrough. Thus the design of SCC's remains a critical step in the realization of sampled data systems in GaAs.

Some of the problems associated with the voltage buffer in Fig. 3(a) can be avoided by replacing it with a short circuit with the consequence that the circuit now draws a finite dc current at switch node X, when the switch is in the open state [6]. This can be accepted when the operational amplifier driving this node can supply the current. In any case, the voltage at this node when the switch is in the open state is not sampled. The circuit to be used in this work is an example of this approach and is shown in Fig. 3(b) [9]. MESFET's M2 and M3 constitute the inverter; diodes, as in [6], make clock-feedthrough signal independent, and signal dependence is further reduced by the use of inverter cascode device M4 [9]. Having considered the realization of the switches in the SC circuit, we now turn our attention to the operational amplifiers.

IV. Transconductance Amplifier Settling Behavior

Amplifier settling time is the most important dynamic performance parameter for sampled data circuit design because it determines the maximum frequency limit and affects response accuracy [14]. Suitable amplifiers are generally of the single-stage, transconductance type, for which settling time is critically dependent on load capacitance [13]. Since, in general, the amplifiers in an SC filter experience different capacitative loads, the settling time of each amplifier has to be assessed separately. Most SC circuits, like that in Fig. 1, operate with a 2-phase switching scheme. Thus, as shown in Fig. 2, there are three distinct states ("E," "O," and "INT") for which an amplifier's settling characteristics have to be considered.

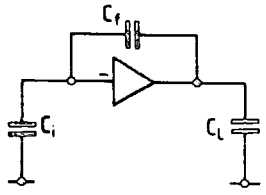

Fig. 4. General amplifier embedding.

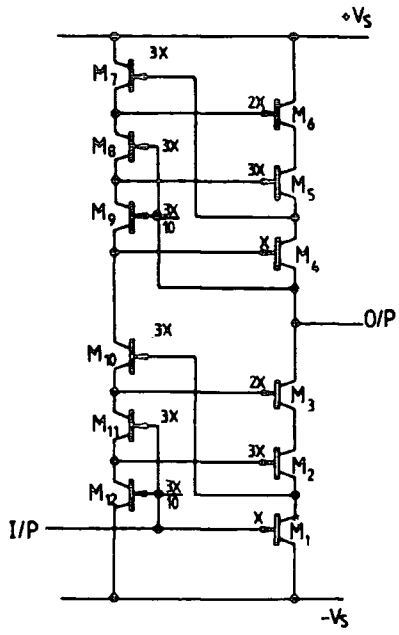

Fig. 5. High gain double cascode amplifier (V_s = 5 V).

In order to investigate the effect of switching state on settling time, we initially make two simplifications. Firstly, we begin by assuming that the switches are ideal, i.e., open or short circuit, depending on switching state. Secondly, whereas in certain switching states some of the amplifiers are coupled together, as for example in Fig. 1 in the "E" phase, we investigate the settling characteristics of each amplifier in turn under the assumption that the remaining amplifiers are ideal. The validity of these simplifications will be confirmed by simulation in Section VIII.

Under the above assumptions, each amplifier in an SC filter may be considered to have an embedding of the general form shown in Fig. 4 for each switching state. If the amplifier is modeled as an ideal transconductance *gm*, the system in Fig. 4 is first order and has a settling time given by

$$t_s = T \ln(1/d) \tag{1}$$

where T is a time constant and d is the settling value tolerance. Matsui *et al.* [15] have shown that the time

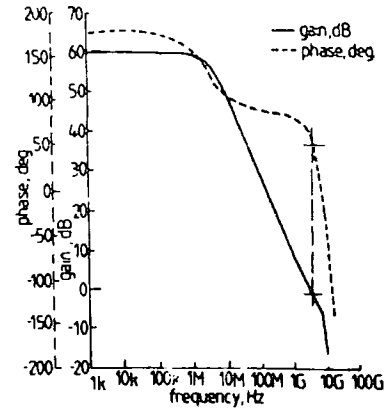

Fig. 6. Simulated amplifier frequency response.

TABLE I
KEY PARAMETERS FOR JFET MODEL OF GaAs MESFET

Parameter Name	Value	Units
VT0	−1	V
BETA	0.067E-3	mAV^{-2}
LAMBDA (LF)	0.06	V^{-1}
LAMBDA (HF)	0.3	V^{-1}
RD	2920	Ohms
RS	2920	Ohms
CGS	0.39E-15	F
CGD	0.39E-15	F
PB	0.79	V
IS	0.075E-15	A

constant T is given by

$$T = [Ci + CL + Ci \cdot CL / Cf] / gm. \tag{2}$$

Thus amplifier settling time (to within 0.5% settling value tolerance) may be expressed as

$$t_s = 5.3\ CL\,\mathrm{eff}/gm \tag{3}$$

where

$$CL\,\mathrm{eff} = Ci + CL + Ci \cdot CL / Cf. \tag{4}$$

As well as describing the dependence of settling time on an amplifier's external embedding, (3) also describes the dependence of settling time on the amplifier circuit itself via the transconductance *gm*. In this paper, the required transconductance values are obtained by uniform scaling of the gatewidths of all the MESFET devices in the amplifier. Thus we may write

$$gm = Kgx \tag{5}$$

where x (in μm) is a reference gatewidth factor that scales the gatewidths of all the devices in the amplifier, and K_g is a constant. Thus we have

$$t_s = \frac{5.3}{Kg} \frac{CL\,\mathrm{eff}}{x}. \tag{6}$$

The term $CL\,\mathrm{eff}/x$ is referred to as the amplifier "loading factor."

V. Amplifier Circuit and Characterization

GaAs MESFET's have a number of disadvantages for the design of high gain operational amplifiers, including the lack of a suitable *P*-channel device, the general lack of enhancement mode devices (depletion mode devices are easier to manufacture), and a low value for the open-circuit voltage gain (transconductance/output conductance) of the device, typically only 20. The requirement for high bandwidth and voltage gains of the order of 60 dB has led to the development of a range of circuit techniques [16]. High voltage gain is achieved by introducing double cascode techniques and biasing the MESFET's using a "double level-shifting" approach. Performance is optimized for a given power consumption and chip area by using a single-stage push–pull architecture based on a high performance GaAs current mirror [17].

The amplifier circuit to be used is shown in Fig. 5. [8]. It is a single-stage double cascode push–pull transconductance amplifier design using double level-shift biasing. The gatewidths of the MESFET's in Fig. 5 are specified in terms of the reference gate width factor x. Amplifier performance is simulated using SPICE via a MINNIE graphics interface [18] with a JFET model for the GaAs MESFET's. For the filter to be designed, the model parameters shown in Table I [8] were assumed. For an amplifier gate width factor x of 100 μ and a load capacitance of 0.8 pF, the simulated gain and phase frequency responses are shown in Fig. 6. Key performance parameters, taken from these curves, are given in Table II. Unlike previous amplifiers [4]–[6] used in SC filters, the amplifier in Fig. 5 has a single-ended input (rather than a differential-input) and the quiescent input voltage is equal to the negative power supply voltage. These features lead to minimum circuit complexity, since internal differential and level-shifting circuitry is avoided, and hence provide optimum high-frequency performance. The use of a single-ended input amplifier will result in a nonoptimum power supply rejection ratio and, therefore, a well-regulated power supply is required. Differential input amplifiers, if required, can be realized using differential to-single-ended converters in conjunction with single-ended input designs, but settling time is increased [16]. We have already seen in (3) and (4) that for the ideal single-stage transconductance type of amplifier, settling time is proportional to effective load capacitance value CL eff. For real amplifier implementations this linear relationship is not strictly observed [20], [21]. Our approach is to characterize the settling time of the particular amplifier design by simulation in a test circuit such that the embedding (see Fig. 4) satisfies both

$$Ci \ll CL \tag{7}$$

$$Ci \ll Cf \tag{8}$$

in which case we have from (4) that CL eff $= CL$. Settling time may be simulated for a range of load capacitance values CL, which may be interpreted as CL eff values, and hence used via (4) to predict settling behavior within the SC filter for the capacitative embedding corresponding to a particular switching state.

TABLE II
Operational Amplifier Performance Parameters
(Gatewidth Factor $x = 100\ \mu$)

Parameter	Value	Units
dc Gain	63	dB
GB Product	3.1	GHz
Phase Margin	64	deg
Load Capacitance	0.8	pF

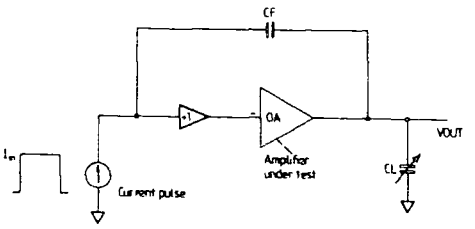

Fig. 7. Test setup for amplifier characterization.

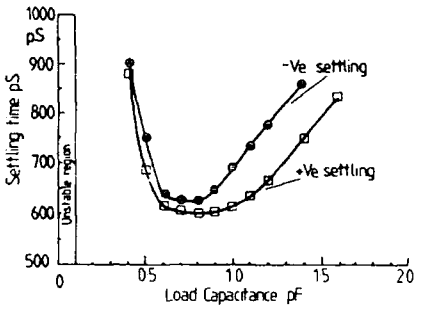

Fig. 8. Settling time characterization curves for amplifier in Fig. 5.

The characterization test circuit is shown in Fig. 7. The ideal unity gain buffer amplifier is included if required in order to establish inequalities (7) and (8), depending on the amplifier input capacitance [22]. The excitation is a finite charge ΔQ applied to the inverting amplifier input using a pulsed current source to give a required output voltage step $\Delta V = \Delta Q / Cf$. The voltage step ΔV is normally chosen to be the maximum voltage step the amplifier is to experience in a particular sampled data application. Settling time is determined using SPICE with the GaAs MESFET parameters of Table I. For characterization of the amplifier in Fig. 5, the value of Cf was 0.7 pF and the buffer amplifier in Fig. 7 was omitted. The input current pulse was of amplitude 1.36 mA and duration 200 ps giving an output voltage step for $Cf = 0.7$ pF of 0.37 V.

The settling time versus load capacitance for the amplifier of Fig. 5 with gatewidth factor x of 100 μ is shown in Fig. 8. It can be seen from Fig. 8 that, for CL greater than about 1 pF, settling time increases linearly with CL as expected from (3) and (4) with inequalities (7) and (8)

satisfied. However, for CL of about 1 pF, there is a turning point, and settling time increases for smaller loading leading to instability for very small loading. This is due to high-frequency poles in the amplifier transfer function, which represent a deviation from ideal transconductance behavior and reduce phase margin for light loading [20], [21]. The minimum, or fastest, settling time of about 630 ps is obtained for a load capacitance of 0.8 pF.

Since for an ideal transconductance amplifier settling time is proportional to loading factor (effective load capacitance divided by gate width factor—see (6)) we divide the load capacitance scale in Fig. 8 by gatewidth factor x (in this case, 100 μ) to obtain a graph of settling time versus loading factor, which forms the starting point for optimization of the SC filter circuit.

VI. High-Frequency Circuit Optimization

Switching states may be divided into critical and noncritical switching states. Critical switching states are those in which the amplifier is receiving charge at its input or conveying charge to a subsequent integrator. It is desirable that in a critical switching state, the operating point on the amplifier characterization curve should be close to that for minimum settling time. Other switching states are denoted noncritical and usually include the guard INT state. Effective load capacitance CL eff, as defined in (4), is frequently close to zero in noncritical switching states since Ci and CL are usually very small in practice. It can be seen from the characterization curves in Fig. 8 that this leads to possible unstable oscillation. We now present a technique for avoiding such instability and maintaining control of amplifier settling behavior by specifying the amplifier operating point in all switching states. This control is achieved by the introduction of grounded capacitance at the amplifier output terminals.

For each switching state, denoted i, let the values of CL eff and Ci/Cf before addition of load capacitance be denoted $CL\,\mathrm{eff}_i$ and a_i, respectively, and let the value of added load capacitance be ΔCLi. From (4), the augmented effective load capacitance for the ith switching state may be written

$$CL\,\mathrm{eff}_i' = CL\,\mathrm{eff}_i + \Delta CL_i(1 + a_i). \tag{9}$$

Denoting the loading factor required in this switching state as f_i and the amplifier gate width factor x, we may write

$$CL\,\mathrm{eff}_i' = xf_i. \tag{10}$$

Thus combining (9) and (10), we have

$$xf_i = CL\,\mathrm{eff}_i + \Delta CL_i(1 + a_i). \tag{11}$$

This equation may be written for each switching state. We require to solve this set of equations for the amplifier gate width factor x and for the added load capacitances ΔCL_i for $i = 1, 2 \cdots n$. Since the number of variables $n + 1$ exceeds the number of equations n by one, we may constrain the added load capacitances to be equal in two switching states, which we denote j and k. Equation (11) for these two switching states allows us to solve for $\Delta CL_j = \Delta CL_k$ and x. ΔCL for the remaining switching states may then be determined from (11) for these remaining states. The expressions obtained for x and the ΔCL_i are given in Table III. It can be seen that if $f_j = f_k$ and either $CL\,\mathrm{eff}_j = CL\,\mathrm{eff}_k$ or $a_j = a_k$, then the values of x or $\Delta CL_j = \Delta CL_k$ will become indeterminate. Thus it is important to choose carefully the two switching states for which ΔCL is the same.

TABLE III
Expressions for Circuit Optimization

$x = \dfrac{CL\,\mathrm{eff}_j(1 + a_k) - CL\,\mathrm{eff}_k(1 + a_j)}{f_j(1 + a_k) - f_k(1 + a_j)}$
$\Delta CL_j = \Delta CL_k = \dfrac{CL\,\mathrm{eff}_j f_k - CL\,\mathrm{eff}_k f_j}{f_j(1 + a_k) - f_k(1 + a_j)}$
$\Delta CL_i = \dfrac{xf_i - CL\,\mathrm{eff}_i}{1 + a_i}$

The addition of amplifier load capacitance will not increase minimum settling time because the amplifier gatewidth factors are adjusted to remain at prescribed operating points on amplifier characterization curves. This will, however, increase chip area and power consumption and therefore, the values of added load capacitance must be carefully optimized. The application of the expressions in Table III to optimize an SC circuit will be illustrated in Section VIII.

VII. Effect of Amplifier Parasitic Capacitances

Amplifier input and output capacitances can each be considered as the sum of two contributions. One, which is primarily due to interconnections, is independent of amplifier gatewidth factor and can be included in the capacitances Ci and CL of the embedding circuit in Fig. 4, and hence allowed for in the circuit optimization. The other contribution derives from MESFET model capacitances, which are proportional to gatewidth factor x. Amplifier input capacitance is related to MESFET gate-source capacitance, which is typically much larger than the gate-drain capacitance, which determines amplifier output capacitance. We therefore now extend the above circuit optimization procedure to allow for amplifier input capacitance, which scales with the gatewidth factor of the amplifier. A method for determining amplifier input capacitance by computer simulation is presented in [23].

We denote the amplifier input capacitance as $x\ kc$, where kc is a constant and x is the amplifier gatewidth factor. It may be shown that the augmented effective load capacitance for the ith switching state, previously given by (9), becomes

$$CL\,\mathrm{eff}_i' = CL\,\mathrm{eff}_i + \Delta CL_i(1 + a_i + xb_i) \tag{12}$$

TABLE IV
EXPRESSIONS FOR CIRCUIT OPTIMIZATION INCLUDING AMPLIFIER INPUT CAPACITANCE

$$Ax^2 + Bx + C = 0$$

where $A = f_j b_k - f_k b_j$

$B = f_j(1 + a_k) - f_k(1 + a_j) + b_j CL\,\mathrm{eff}_k - b_k CL\,\mathrm{eff}_j$

$C = CL\,\mathrm{eff}_k(1 + a_j) - CL\,\mathrm{eff}_j(1 + a_k)$

$$\Delta CL_j = \Delta CL_k = \frac{xf_j - CL\,\mathrm{eff}_j}{1 + a_j + xb_j}$$

$$\Delta CL_i = \frac{xf_i - CL\,\mathrm{eff}_i}{1 + a_i + xb_i}$$

where b_i denotes kc/Cf_i. From (10) and (12), we have

$$xf_i = CL\,\mathrm{eff}_i + \Delta CL_i(1 + a_i + xb_i) \qquad (13)$$

which may be written for each switching state. Constraining, as before, the added load capacitances to be equal in two switching states, j and k, we again solve for $\Delta CL_j = \Delta CL_k$ and x. In this case, x is given by the solution to a quadratic equation, which is given in Table IV. Having obtained the value of x, the added load capacitance in the j and k switching states $\Delta CL_j = \Delta CL_k$ is given by the expression given in Table IV. Finally, (13) for the remaining switching states gives the added load capacitances ΔCL_i for these states according to the expression in Table IV.

VIII. Optimization of an SC Filter

A. General Considerations

We now describe the optimization of the GaAs 2nd-order bandpass filter in Fig. 1. The circuit is shown again in Fig. 9 with some modifications; capacitor C11 has been replaced by an equivalent capacitor "T" network in order to reduce capacitor spread; we have added a buffer amplifier for driving off-chip loads; capacitors Ca, Cb, and Cc will be discussed later. The circuit uses the high-gain push–pull amplifier of Fig. 5. The switch control circuit to be used is that shown in Fig. 3(b).

Since the amplifier in Fig. 5 has the property that the quiescent input voltage is equal to the negative power supply voltage, the ground connections for switches S1 and S3 in the filter of Fig. 9 have to be connected to the negative power supply. The settling time characterization curve for the amplifier has already been shown in Fig. 8 and it is shown again in Fig. 10(a) with the addition of chosen operating points (note that the horizontal scale is now loading factor as mentioned in Section V). Since points to the left of the minimum settling time point correspond to underdamped behavior it was considered safer, in view of process tolerances, to select the optimum operating point for the critical switch phases to the right of the minimum corresponding to a loading factor of 0.012 pF/μm, indicated "Opt" in Fig. 10(a). For noncritical switching states, we shall adopt operating points corresponding to loading factors of 0.004 and 0.006 pF per μm, indicated "P1" and "P2" in Fig. 10(a). Points "P1" and "P2" are strictly outside the range of loading factor for

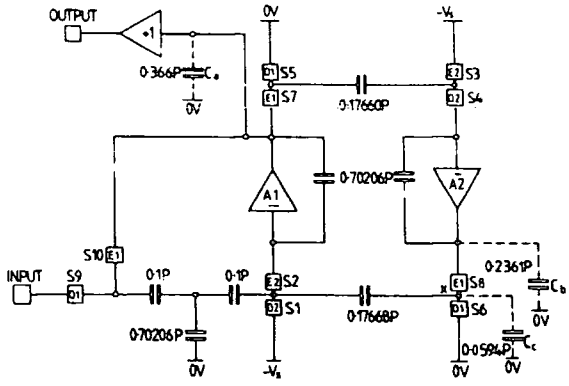

Fig. 9. 2nd-order SC filter for implementation.

which the amplifier behaves like an ideal transconductance, but the computer simulations to be given in Section IX confirm that reasonably accurate prediction of settling time is obtained using the transconductance approximation for these operating points. The settling curves for the three operating points to be used are shown in Fig. 10(b), illustrating the different degrees of damping. The settling times for a 0.5% settling value tolerance are given in Table V. We now apply the optimization method of Section VI.[1]

B. Amplifier 1

The values of Ci, CL, and Cf (as defined in Fig. 4) for amplifier 1 in the three switching states are given in Table VI. The values of CL eff (as defined in (4)) and $a = Ci/Cf$ are also given. In the case of amplifier 1, the "E" phase is the critical phase, and its loading factor f_e is to correspond to the optimum operating point on the characterization curve. We assume that the operating points in the noncritical "O" and "INT" switching states are identical and we denote the corresponding loading factor f_o. This makes all parameters in the "O" and "INT" switching states identical (see Table VI) and therefore, they may be treated for optimization as a single switching state. Application of the equations in Table III (with $j = e$ and $k = o$) to the data in Table VI yields added load capacitor value and amplifier gatewidth factor given by

$$\Delta CL_e = \Delta CL_o = \frac{f_o CL\,\mathrm{eff}_e}{f_e - f_o(1 + a_e)} \qquad (14)$$

$$x = \frac{CL\,\mathrm{eff}_e}{f_e - f_o(1 + a_e)}. \qquad (15)$$

Table VII shows values of ΔCL and x for a range of "O"

[1]The optimization technique (including scaled amplifier input capacitances) had not been developed at the time the integrated filter was designed.

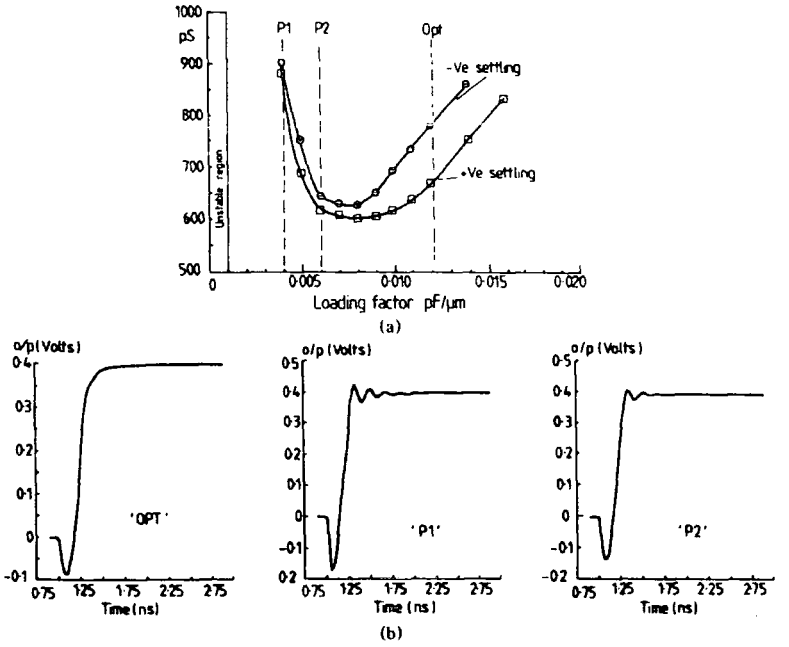

Fig. 10. Amplifier settling characteristics. (a) Characterization curve with operating points. (b) Transient settling curves for "OPT," "P1," and "P2" operating points.

TABLE V
AMPLIFIER SETTLING TIMES

Operating Point	Positive Settling Time (ps)	Negative Settling Time (ps)
Opt	670	778
P1	881	910
P2	615	643

TABLE VI
SC FILTER LOADING FOR AMPLIFIER 1 IN FIG. 9

Phase	Ci (pF)	Cf (pF)	CL (pF)	CL eff (pF)	$a\ (= Ci/Cf)$
E	0.2545	0.7131	0.2545	0.5998	0.3569
O	0	0.7021	0	0	0
Int	0	0.7021	0	0	0

TABLE VII
EFFECT OF "O" PHASE LOADING FACTOR FOR AMPLIFIER 1 ($f_e = 0.012$ pF/μm)

f_o (pF/μm)	ΔCL (pF)	x (μm)	Ts (ps)
0	0	50	oo
0.002	0.129	65	5000
0.004	0.366	90	900
0.006	0.930	155	700
0.008	4.190	524	600

TABLE VIII
SC FILTER LOADING FOR AMPLIFIER 2 IN FIG. 9

Phase	Ci (pF)	Cf (pF)	CL (pF)	CL eff (pF)	$a\ (= Ci/Cf)$
E	0	0.7021	0.1767	0.1767	0
O	0.1767	0.7021	0	0.1767	0.2517
Int	0	0.7021	0	0	0

phase loading factors f_o for the optimum f_e of 0.012 pf per micron. From Table VII, a value of f_o of 0.004 pF per μm, corresponding to operating point "P1" in Fig. 10(a), provides a reasonable amplifier device width factor x of 90 μ and a ΔCL value of 0.366 pF, which is indicated as Ca in Fig. 9.

C. Amplifier 2

The relevant parameters for amplifier 2 in the three switching states are given in Table VIII. In this case, phases "E" and "O" are both critical phases, and the required loading factor should be the same and correspond to the optimum operating point (we denote the loading factor f_e). Table VIII indicates that for these two phases, the values of CL eff are also the same and therefore, as discussed in Section VI, the added load capacitances in these switching states cannot be made equal. Selecting the "O" and "INT" phases as the phases for which the load capacitances are equal and denoting the loading factor in the noncritical "INT" phase by f_{int}, the equations in Table III yield:

$$\Delta CL_o = \Delta CL_{\text{int}} = \frac{CL\,\text{eff}_o\, f_{\text{int}}}{f_e - f_{\text{int}}(1 + a_o)} \tag{16}$$

$$x = \frac{CL\,\text{eff}_o}{f_e - f_{\text{int}}(1 + a_o)} \tag{17}$$

TABLE IX
SIMULATED AND DESIGN FILTER SETTLING TIMES (ps)

Amp	Sign		Int-phase	O-phase	E-phase Isolated	E-phase Coupled
A1	+	Simulated	778	778	689	935
		Design	881	881	670	-
A1	-	Simulated	797	797	739	894
		Design	910	910	778	-
A2	+	Simulated	605	658	652	811
		Design	615	670	670	-
A2	-	Simulated	507	747	772	865
		Design	643	778	778	-

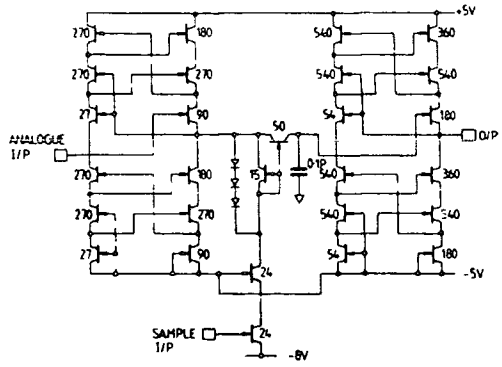

Fig. 11. Output buffer circuit.

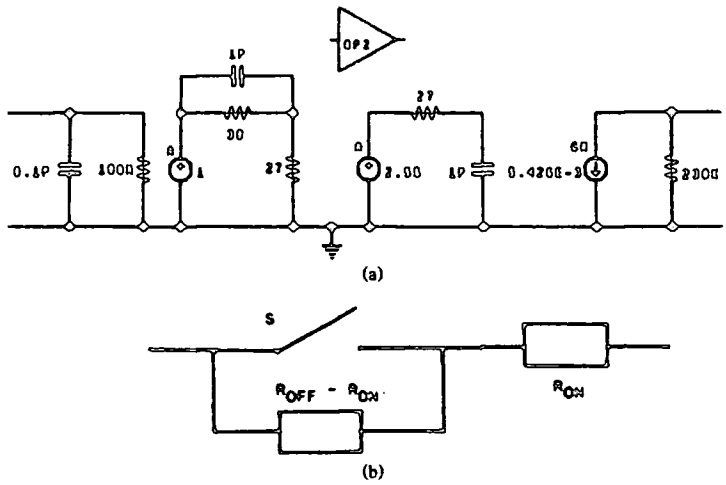

Fig. 12. Macromodels for SC filter. (a) Amplifier macromodel. (b) Switch macromodel.

$$\Delta CL_e = \frac{CL\,\mathrm{eff}_o\, f_e}{f_e - f_{\mathrm{int}}(1+a_o)} - CL\,\mathrm{eff}_e. \qquad (18)$$

A value for f_{int} of 0.006 pF per μm (operating point "P2" in Fig. 10(a)) gave an amplifier gatewidth factor x of 40 μm and values for ΔCL_o and ΔCL_e of 0.2361 pF and 0.2955 pF, respectively. These load capacitor requirements are met by adding the 0.2361-pF capacitor Cb directly to the output of amplifier 2, as shown in Fig. 9, and a 0.0594-pF capacitor Cc to the node "x." If the load capacitances had been made equal in the "E" and "INT" switching states, then the equations would still have been soluble, but then ΔCL_{int} would have been greater than ΔCL_o; this would have made implementation difficult as no switches are closed in the "INT" switching state.

IX. Simulation of Settling Behavior

Having optimized the SC filter for prescribed settling behavior of the two amplifiers in each time slot, we now verify the settling behavior of the circuit as a whole by computer simulation. At this stage, we still assume that the switches in the filter of Fig. 9 are ideal; the effect of nonideal switches will be considered in Section XI. Whereas up to now we have considered amplifiers settling in isolation, we now consider the settling behavior of the whole filter. We thus consider the filter in each of the three switching states "E," "O" and "Int." For each switching state, the filter degenerates to an amplifier-capacitor subcircuit. For these subcircuits, SPICE was used to simulate the settling times of the transient output voltages of the two amplifiers for positive and negative output voltage steps [24]. The excitation, consisting of current pulses applied to the amplifier virtual ground nodes, and the initial conditions were chosen to give realistic amplifier output voltage steps of 0.37 V. The results of the simulation are shown as "Simulated" in Table IX. The settling times denoted "Design" are the design settling times of Table V for the chosen operating points. In the "E" phase, the two amplifiers in Fig. 9 are coupled by a capacitor; thus in reality there is interaction between the amplifiers during settling, which was not

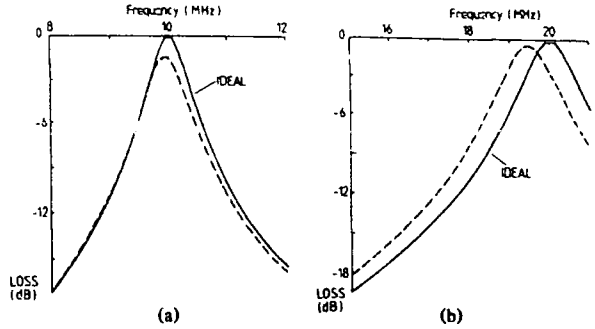

Fig. 13. Simulated amplitude response of integrated filter with ideal curve. (a) 250-MHz switching frequency. (b) 500-MHz switching frequency.

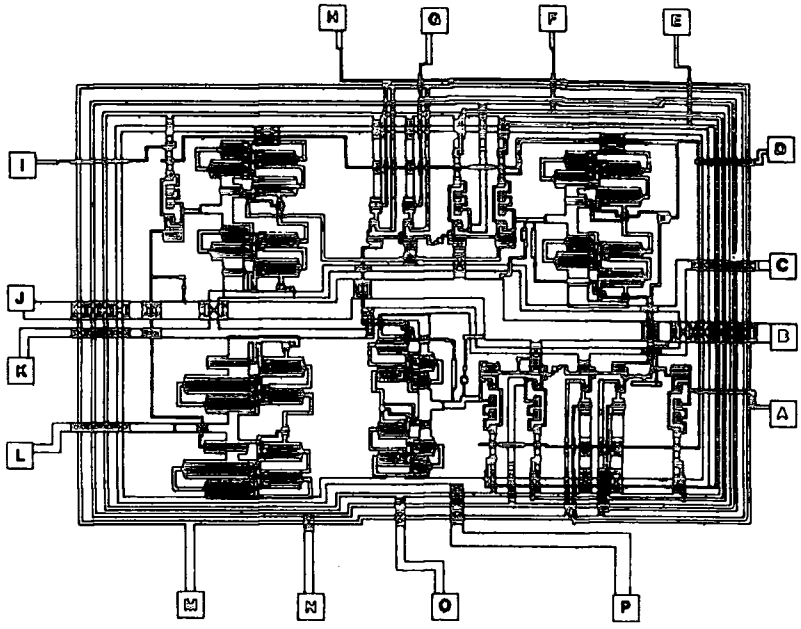

Fig. 14. Layout plot for GaAs SC filter; total size 3.3 mm×2.6 mm.

allowed for in the above design procedure. For the results denoted "Isolated" in Table IX, the interaction was broken by replacing the other amplifier by an ideal voltage source. The results denoted "Coupled" include the interaction. It can be seen that the interaction between amplifiers increases settling times by about 30%. For the "O," "Int," and noncoupled "E" cases, there is reasonable agreement between design settling times and those obtained by simulating the filter.

X. Output Buffer

The design for the output buffer of Fig. 9 is shown in Fig. 11. It consists of two unity gain sections separated by a switching circuit and hold capacitor. The unity gain sections are very high-quality modified source followers derived from the operational amplifier of Fig. 5. The switching circuit is similar to that in Fig. 3(b). By feeding an appropriate clock signal to the digital input, the buffer acts as a sample and hold circuit where the sampling instant may be freely chosen. Alternatively, with a dc digital input, the circuit acts as a nonsampling buffer. SPICE simulation of the circuit in switched and nonswitched modes showed that in both cases there is negligible performance deterioration over the required frequency band.

XI. System Verification

The frequency response of the final SC filter system is simulated using a sophisticated SC system analysis package, which can simulate resistive effects, thus allowing for nonideal switch resistance to be included. The package used is the University of Glasgow SCNAP software suite [25]. The analysis is based on the use of small signal macromodels for the amplifiers and the switches.

The gain and phase responses of the amplifier are analyzed using the stead-state analysis facility of SPICE to give results of the kind already shown in Fig. 6. Examination of these curves indicates that they can be approximated to a sufficient accuracy over the frequency range of interest by a linear macromodel possessing two poles and a single zero. The circuit diagram of the macromodel chosen is shown in Fig. 12(a). The component values are adjusted by trial and error to give the best fit to the gain and phase characteristics and to give correct input and output impedances. For the switches, SPICE transient analysis of the step response of a single switch device connected to a capacitor allows the determination of on-resistance and off-resistance, leading to a switch macromodel of the form shown in Fig. 12(b). The SC filter system of Fig. 9, with its amplifiers and switches replaced by macromodels consisting of capacitors, ideal switches, resistors, and controlled sources, is analyzed using the SC system simulator SCNAP. The amplitude response curves are shown in Fig. 13 for switching frequencies of 250 MHz and 500 MHz.

XII. Layout and Fabrication

The 2nd-order SC filter based on Fig. 9 was laid out using MAGIC with a specially written technology file for the Anadigics GaAs process, which provides 0.5-μm gate-length MESFET's and silicon nitride metal–insulator–metal (MIM) capacitors. Separate lines and pads were used for the analog and digital grounds and power supplies. Reasonable precautions were taken to avoid back-gating effects. A plot of the circuit layout is shown in Fig. 14. The size of the chip is 3.3×2.6 mm and the power consumption is 440 mW. From the simulation results in the previous section, it was expected that the circuit would operate with high precision at a switching frequency of 250 MHz and that operation would still be possible up to 500 MHz. The filter had been designed to realize a Q-factor of 16, a midband gain of unity (0 dB), and a switching frequency to midband frequency ratio of 25.

XIII. Testing and Experimental Results

For testing, the chip was thermo-compression gold-wire bonded within an 18-pin ceramic dual-in-line package. For measurements at a 250-MHz switching rate, the package was mounted in a dual-in-line socket, which was placed on an insulating circuit board. For measurements at a 500-MHz switching rate, the package was mounted directly on a copper-clad board, which formed a ground plane. BNC sockets were provided for the two switching signals and the input and output signals. The signal input and the switching inputs were terminated in 51-Ω resistors as close to the chip as possible. For the tests to be described here, the output buffer amplifier was operated in continuous, nonsampling mode with a dc sample voltage of −10 V. The input signal level for all tests was +7 dBm, or 0.5 Vrms.

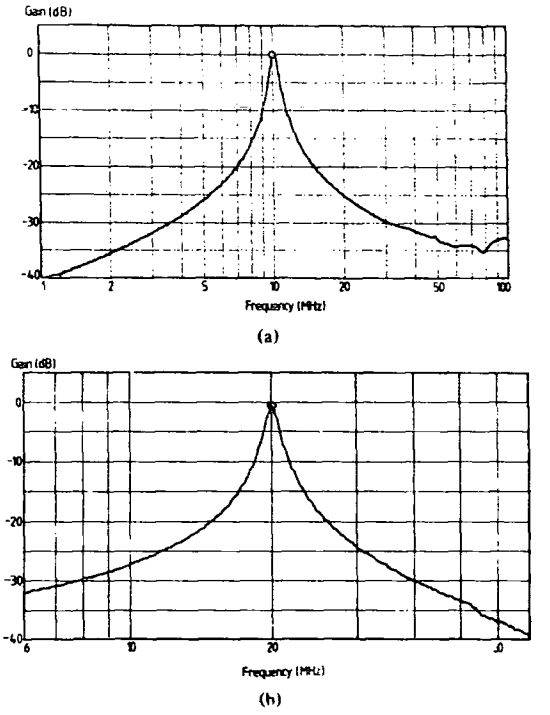

Fig. 15. Measured amplitude response of filter. (a) 250-MHz switching frequency. (b) 500-MHz switching frequency.

The measured amplitude/frequency response of the filter for switching frequencies of 250 MHz and 500 MHz are shown in Fig. 15(a) and (b), respectively. These responses are insensitive to power supply voltage variations. Expanded passband plots for the above switching frequencies are shown in Fig. 16(a) and (b). The peak gains, midband frequencies, and Q-factors for 250 MHz and 500 MHz switching frequencies are +0.2 dB and −0.4 dB, 10.02 MHz and 20.01 MHz, and 15.1 and 16.7, respectively. These frequency response accuracies represent a considerable improvement over the previous results of [4]. The zero-input noise measured at the output of the filter is shown in Fig. 17 for a measuring bandwidth of 100 kHz compared with the response for an input signal level of +7 dBm; the average noise at the midband frequency is about −70 dB relative to the signal level used giving a dynamic range of about 76 dB. Observation of the filter output signal at the resonant frequency indicated a dc offset voltage of less than 100 mV and reasonably low levels of clock feedthrough.

XIV. Conclusions

A significant increase in the maximum switching frequency for SC filters has been achieved and good response precision demonstrated at these frequencies. This work has contributed towards demonstrating the engineering feasibility of GaAs technology for sophisticated

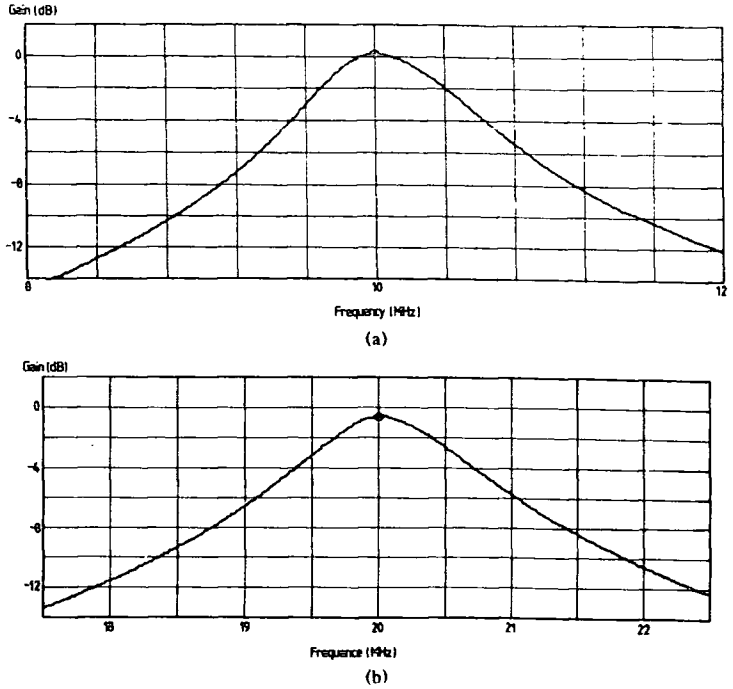

Fig. 16. Measured expanded passband response. (a) 250 MHz switching frequency. (b) 500 MHz switching frequency.

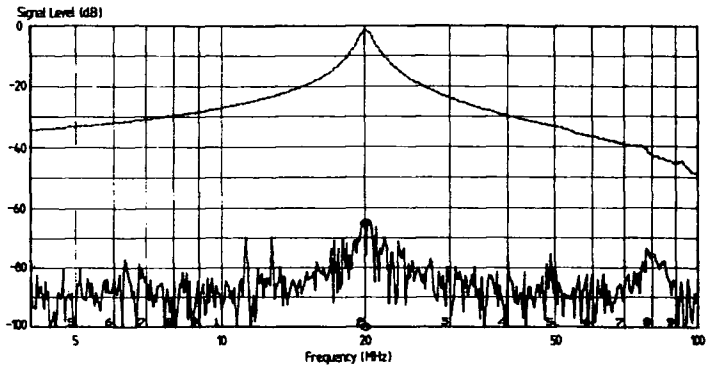

Fig. 17. Measured noise of filter.

analog applications. Comparison of the computed and measured response curves indicates a need for more realistic computer simulation of the integrated system, perhaps along the lines proposed in [24]. In spite of the results achieved, the operational amplifier used in the design is significantly less fast than more recent designs [26] and advanced designs implemented using state-of-the-art technology [27]. Thus future opportunities are opened up for SC systems operating with gigahertz clock rates. It is thought that the techniques for amplifier characterization and optimization of an SC circuit for maximum switching frequency that have been presented are also applicable to other technologies, including CMOS.

Acknowledgment

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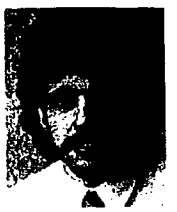

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PAPER 45

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A Methodology for Integrated Ladder Filter Design

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Abstract—**The design procedures for integrated ladder filter design by operational simulation are regularized in terms of matrix operations. This provides a systematic framework for the derivation of standard circuits, such as leapfrog and coupled-biquad, as well as several novel structures. Each circuit is now seen to belong to a certain family, dependent on the type of matrix factorization employed. A detailed comparison of the properties of the different structures is undertaken for a range of filter specifications, demonstrating that ladder filters offer good solutions to several hitherto difficult filtering problems. The methods are applicable to all active filter technologies including active-*RC* and switched capacitor (SC).**

I. Introduction

Integrated active filters designed by passive ladder simulation have long been known to have the property of low sensitivity to fabrication errors [1]–[3]. Among various design approaches the leapfrog ladder and coupled biquad methods are the most popular [4], [5]. A recent alternative is the LUD ladder simulation technique, which has the notable feature of being free from capacitor-coupled op-amp loops [6]. However, the advantages of adopting ladder simulation methods have always been compromised by their complicated design procedures and overheads such as chip area, which are highly dependent on proper selection of the prototype and simulation technique.

This paper provides a comprehensive study of integrated ladder filter design by operational simulation methods. A unified matrix form is introduced, which permits the design procedures to be expressed in terms of a series of matrix operations. This provides a systematic basis for design of filters with different prototype structures and response specifications. Most existing operational ladder simulation and cascade biquad approaches are described, as well as several novel strategies.

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Some constraints will first be stated to define a class of matrix equations that are directly realizable. These equations are linear in s^{-1} so that op-amp circuits can be used to perform additions, multiplications, and integrations. Techniques are then introduced to render the matrix description of the ladder prototype realizable, by decomposing it into several linear subequations. A large family of circuit structures is revealed depending on the choice of matrix decomposition, including the existing leapfrog, coupled biquad, and LUD ones as specific cases. All circuits are insensitive to parasitic capacitance in SC implementation.

LDI-transformed SC ladders are discussed initially [3] and it is shown that the design procedure for the active-*RC* ladders is nearly the same. However, since LDI design requires a complicated procedure to eliminate the distortion caused by improperly realized terminations [7], so-called bilinear-LDI methods will be adopted to develop exact z-domain SC circuits. In many cases, the LDI and bilinear-LDI structures are identical except for different input stages. However, for prototypes with purely inductive branches (without a parallel capacitor) the LDI structure is simpler than the corresponding bilinear-LDI one. A technique is introduced in this paper to cancel excess components in the bilinear-LDI structures, hence combining the advantages of simplicity of the LDI structure and exact frequency response of bilinear transformations.

Finally, a detailed comparison of various circuit structures is presented for different applications. With the help of a filter compiler, PANDDA [8], some studies of the various structures over a range of relative bandwidths (for bandpass designs) and transition bandwidths (for low-pass designs) are undertaken. This provides guidelines as to the suitability of each structure to a given filter specification.

II. Directly Realizable Matrix Systems

The basic building blocks for active-*RC* and SC networks are shown in Fig. 1, realizing the elementary transfer functions of feedthrough, inverting, and noninverting integration.

Directly Realizable Matrix Systems

Matrix methods are known to be an efficient means of representing large interconnected networks. The inverse

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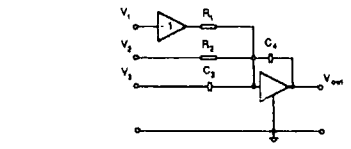
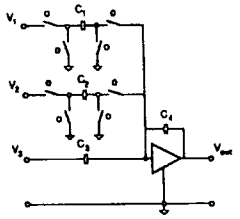


$$V_{out}(s) = \frac{1}{sR_1C_4}V_1(s) - \frac{1}{sR_2C_4}V_2(s) - \frac{C_3}{C_4}V_3(s)$$

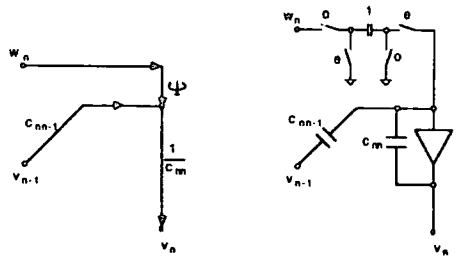
(a)



$$V_{out}(z) = \frac{-1}{1-z^{-1}}\frac{C_1}{C_2}V_1(z) + \frac{z^{-1}}{1-z^{-1}}\frac{C_2}{C_4}V_2(z) - \frac{C_3}{C_4}V_3(z)$$

(b)

Fig. 1. First-order building blocks. (a) Active-*RC* building block. (b) SC building block.



(a) (b)

Fig. 2. Representations of a linear systems. (a) Signal flow graph. (b) SC circuit realization.

procedure is how to construct an active-*RC* or SC circuit from a set of predetermined matrix equations. If the equations are linear with respect to the transfer functions of the basic building blocks, then the problem becomes most simple. For example, consider the following single algebraic equation:

$$c_{nn}v_n + c_{nn-1}v_{n-1} = \frac{z^{-1}}{1-z^{-1}}w_n. \tag{1}$$

This equation can be directly represented by the SFG in Fig. 2(a). Let the variables $\{v_i\}$ and $\{w_i\}$ be the voltages of op-amp outputs, then the SFG can be replaced by the SC network shown in Fig. 2(b).

This simple example can be generalized to the case of constructing an SFG and an SC circuit from a set of algebraic equations in matrix form. A matrix equation is considered to be *directly realizable* if it meets the following assumptions.

i) *The matrix equation is linear with respect to the transfer function of the basic building blocks.*

ii) *In each matrix equation only one variable vector and associated coefficient matrix will be written on the left-hand side.*

iii) *The coefficient matrix on the left-hand side is square and nonsingular with all the diagonal elements nonzero.*

With the above assumptions a *directly realizable* matrix equation will have the following form:

$$A_{ii}X_i = \sum_k \zeta_{ik}A_{ik}X_k + \zeta_k J_k \tag{2}$$

where $\{X_k\}$ are vectors of variables, $\{J_k\}$ are input vectors, $\{A_{ik}\}$ are connection matrices, and $\{\zeta_{ik}\}$ and $\{\zeta_k\}$ are the transfer functions of the building blocks.

The following rules are used to derive SFG's and circuits directly from matrix equations throughout this paper.

1) *Every entry in the variable vectors is represented by a nodal variable in the SFG and by an output of an op-amp in the circuit. The input variables are represented by independent voltage sources.*

2) *The ith row equation represents the linear relationship at the node corresponding to x_i, or, for the circuit, the input–output voltage relationship of the op-amp corresponding to x_i.*

3) *Each diagonal entry a_{ii} is realized by an integrating element. Every other nonzero entry in a matrix represents the connection of a circuit element between op-amps.*

Notice that Assumptions i)–iii) are only sufficient conditions for realizability. If a matrix system meets these assumptions, then using the above rules its realization becomes straightforward and unique. The major task of this research is to develop systematic procedures to realize matrix systems which initially fail to meet these assumptions.

III. Continuous-Time and LDI Transformed Discrete Ladder Systems

A passive ladder can be described by the nodal equation [9]

$$(sC + s^{-1}\Gamma + G)V = J. \tag{3}$$

To ensure that all the entries in C, Γ, and G are positive, we introduce alternating signs in V, i.e., let $V = [v_1, -v_2, v_3, -v_4, \cdots]$.

A. LDI Transformed Systems

The LDI transformation is defined as $s \rightarrow (2/T)[(1-z^{-1})/z^{-1/2}]$ (T is the sampling period) and a pair of LDI

integration operators are

$$\Phi = 1/(1 - z^{-1}) \tag{4a}$$

$$\Psi = z^{-1}/(1 - z^{-1}). \tag{4b}$$

Applying the LDI transformation to (3) and introducing an extra half-period delay at the terminations for stability [10], (3) becomes

$$\boldsymbol{Y}(z)\boldsymbol{V} = \boldsymbol{J} \tag{5a}$$

$$\boldsymbol{Y}(z) = \left[\frac{2}{T}\frac{1 - z^{-1}}{z^{-1/2}}\boldsymbol{C} + \frac{T}{2}\frac{z^{-1/2}}{1 - z^{-1}}\boldsymbol{\Gamma} + z^{\pm 1/2}\boldsymbol{G}\right] \tag{5b}$$

multiplying equation (5a) through by $z^{1/2}$ gives

$$\left(\frac{1}{\Psi}\boldsymbol{A} + \Phi\boldsymbol{B} + \boldsymbol{G}\right)\boldsymbol{V} = \boldsymbol{J}' \tag{6a}$$

$$\boldsymbol{A} = (2/T)\boldsymbol{C},$$

$$\boldsymbol{B} = (T/2)\boldsymbol{\Gamma},$$

$$\boldsymbol{J}' = z^{1/2}\boldsymbol{J}. \tag{6b}$$

Multiply (5a) through by $z^{-1/2}$ to get

$$\left(\frac{1}{\Phi}\boldsymbol{A} + \Psi\boldsymbol{B} + \boldsymbol{G}\right)\boldsymbol{V} = \boldsymbol{J}' \tag{6c}$$

$$\boldsymbol{A} = (2/T)\boldsymbol{C},$$

$$\boldsymbol{B} = (T/2)\boldsymbol{\Gamma},$$

$$\boldsymbol{J}' = z^{-1/2}\boldsymbol{J}. \tag{6d}$$

Since the transfer functions from $\boldsymbol{J}$ and $\boldsymbol{J}'$ to the output differ only by a delay of a half period, we will not distinguish between them in the following discussion.

As system (6) can be made identical to (3) by replacing $\Psi = \Phi = s^{-1}$, there is virtually no difference between active-*RC* and LDI transformed ladder design, apart from replacing a pair of LDI integrators by a pair of inverting and noninverting continuous domain integrators. For this reason, only LDI SC ladder design will be detailed, assuming that all the techniques can be used directly for active-*RC* design.

B. System Linearization by Matrix Decompositions

Equation (3) contains nonlinear combinations of the basic functions Ψ and Φ; therefore, it does not meet Assumption i). It is more convenient to linearize the system into the form of (2). This can be done by creating a set of intermediate variables and decomposing the system of (3) into two inter-related systems. This decomposition can be performed in various ways.

C. Left Matrix Decomposition

Factorize the left hand matrix $\boldsymbol{A}$ into

$$\boldsymbol{A} = \boldsymbol{A}_l\boldsymbol{A}_r. \tag{7a}$$

The following pair of equations is equivalent to (6a):

$$\begin{cases} \boldsymbol{A}_l\boldsymbol{W} = (-\Phi\boldsymbol{B} - \boldsymbol{G})\boldsymbol{V} - (-\boldsymbol{J}) & (7b) \\ \boldsymbol{A}_r\boldsymbol{V} = \Psi\boldsymbol{W} & (7c) \end{cases}$$

where $\boldsymbol{W}$ is the vector of intermediate variables.

TABLE I
VARIOUS MATRIX DECOMPOSITIONS

Category	Name	Matrix Decompositions		
Left Decompositions	Left-LUD	$A = L_a U_a$	$A_l = L_a$	$A_r = U_a$
	Left-direct (IA)	$A = \mathrm{IA}$	$A_l = \mathrm{I}$	$A_r = A$
Right Decompositions	Right-LUD	$B = L_b U_b$	$B_l = \mathrm{L_b}$	$B_r = U_b$
	Right-direct (BI)	$B = \mathrm{BI}$	$B_l = \mathrm{B}$	$B_r = I$
	Leapfrog	$B = 4A_\Gamma D_\Gamma A_\Gamma^T$	$B_l = 4A_\Gamma$	$B_r = D_\Gamma A_\Gamma^T$

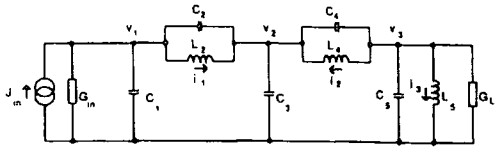


Fig. 3. 6th-order bandpass ladder prototype.

D. Right Matrix Decomposition

$\boldsymbol{B}$ can also be factorized as

$$\boldsymbol{B} = \boldsymbol{B}_l\boldsymbol{B}_r. \tag{8a}$$

The following pair of equations to (6c):

$$\begin{cases} \boldsymbol{A}\boldsymbol{V} = -\Phi[\boldsymbol{B}_l\boldsymbol{W} + \boldsymbol{G}\boldsymbol{V} + (-\boldsymbol{J})] & (8b) \\ \boldsymbol{I}\boldsymbol{W} = \Psi\boldsymbol{B}_R\boldsymbol{V}. & (8c) \end{cases}$$

From the rules given in Section II, (7) and (8) can be realized by SC circuits, provided that the relevant matrices are obtained by certain decompositions. The one-to-one correspondence between the circuit elements and the matrix entries indicates that the efficiency of the SC implementation in terms of numbers of capacitors is related to the sparsity of the system matrices. Consequently, a good simulation of a prototype by matrix methods will attempt to maintain the sparsity property of (3).

E. Further Matrix Decompositions

The following methods are commonly known to preserve the sparsity of the matrices to be decomposed: the LUD method [6], the topological method [11], and, simplest of all, the direct methods that decompose matrix $\boldsymbol{A}$ into $\boldsymbol{AI}$ or $\boldsymbol{IA}$; see Table I. There are also some dual systems, which can be obtained by replacing LU decomposition by UL decompositions, or by replacing $\boldsymbol{A} = \boldsymbol{IA}$ and $\boldsymbol{B} = \boldsymbol{BI}$ by $\boldsymbol{A} = \boldsymbol{AI}$ and $\boldsymbol{B} = \boldsymbol{IB}$, respectively. The dual methods are useful in realizing a family of canonical structures [12].

From network topology it is known that $\boldsymbol{D}_\Gamma\boldsymbol{A}_\Gamma^T\boldsymbol{V} = \boldsymbol{I}_L$ is the current vector of the inductance branches. This confirms that topological decomposition of $\boldsymbol{B}$, derived as shown at the bottom of Table I, yields the same structures as those by a conventional leapfrog method. In general, if

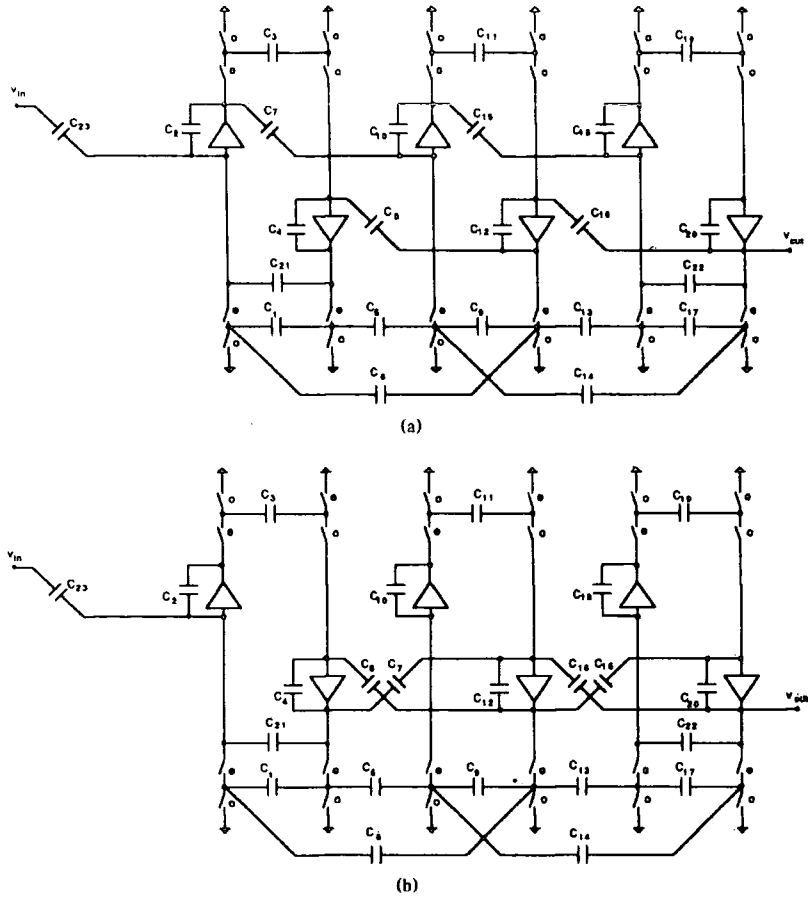


Fig. 4. Various SC filter realizations. (a) Left-LUD type SC circuit. (b) Left-direct (IA) type SC circuit. (c) Right-LUD type SC circuit. (d) Right-direct (BI) type SC circuit.

topological decomposition is applied to the left-hand matrix A, it cannot be assured that the resulting A_l and A_r will be square. Consequently, the resulting system (6) may violate Assumption (iii) in Section II. If A_l and A_r, obtained from a topological decomposition, are square, then in most cases they are identical to those derived by LU decomposition. Therefore, the topological decomposition will not be considered for left-hand matrices.

F. Examples of Various Circuit Structures

The passive ladder prototype of Fig. 3 is simulated by left-LUD, left-direct, right-LUD, and right-direct SFG's and circuits of Fig. 4.

Interestingly, it is found that the circuits in Fig. 4(b) and 4(d) resulting from direct decompositions can be identified as a coupled type-E and type-F biquad circuit, respectively [5]. By comparing the intermediate variables introduced in the two approaches it can be shown that they differ only by voltage scaling factors.

IV. Other System Linearization Approaches

A. Inverse Matrix Approaches

If a left-direct decomposition is used, i.e., $A_l = I$, $A_r = A$, then (7) is equivalent to

$$\begin{cases} IW = (-\Phi B - G)V - (-J) & \text{(9a)} \\ IV = \Psi A^{-1} W. & \text{(9b)} \end{cases}$$

Similarly, if a right-direct decomposition $B = IB$ is used, then an alternative realization of (8), by inverting B, results

$$\begin{cases} AV = -\Phi[IW + GV + (-J)] & \text{(10a)} \\ B^{-1}W = \Psi IV. & \text{(10b)} \end{cases}$$

The significant properties of these inverse matrix methods occur in the continuous-time domain, when $\Psi = \Phi = s^{-1}$, $A = C$ and $B = \Gamma$, (9) is a minimum capacitor realization while (10) is a minimum resistor realization. This is because the nonzero entries of the matrices in the left-hand side require only capacitors for realization while those of

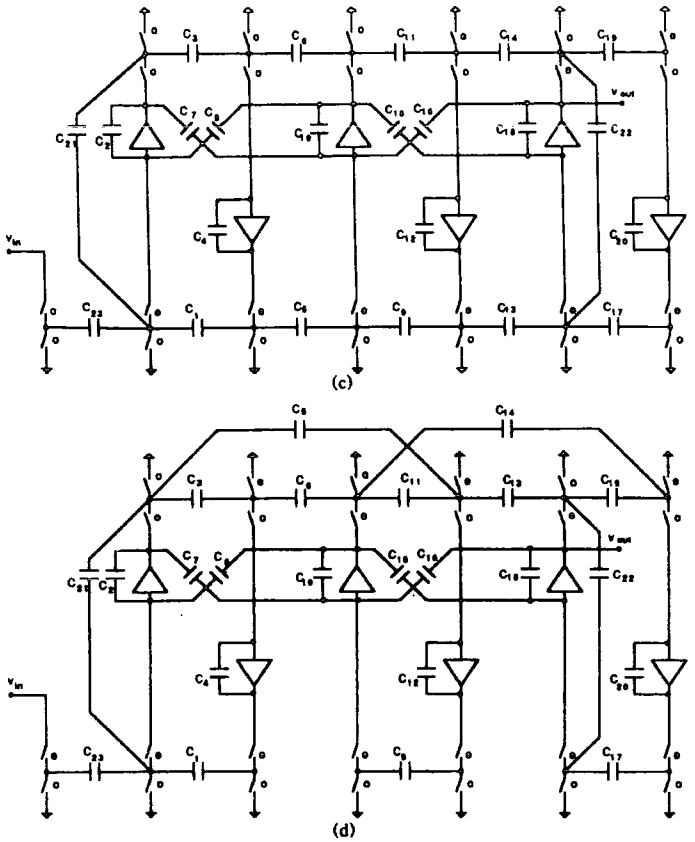


Fig. 4. (*Continued*)

the right-hand side with coefficient $\Psi = \Phi = s^{-1}$ require resistors. The identity matrix I on the right-hand side has the fewest nonzero entries and hence requires a minimum number of resistors. Minimum capacitor or resistor properties are useful for certain fabrication technologies such as continuous-time transconductance-C [13].

The disadvantage of this method is that even when C or Γ is tridiagonal, C^{-1} or Γ^{-1} is usually a full matrix, representing a fully interconnected system. This will cost extra elements, the number increasing with the square of the matrix order. For high-order filters with multiple zeros at infinity, C or Γ can be made a block diagonal matrix with 2×2 blocks and the realization will not incur any extra cost. A block diagonal C (Γ) means that there must be pure series inductor (capacitor) branches in the prototype which realize transmission zeros at infinite (zero) frequency. Another restriction of the inverse method is that C^{-1} or Γ^{-1} may contain negative entries whose realization is efficient only if differential signals are available.

B. UL – LU Approaches

UL and LU factorizations can be applied to both the left- and right-hand matrices of (3). Restricted by the requirements of preserving matrix sparsity and maintaining a canonical number of variables, derivations for such structures are not straightforward and are explored in this section. Rearrange (3) as

$$\left(\frac{1}{\Psi}A + \Phi B + zD_1 + D_n\right)V = (1+z)J' \tag{11a}$$

$$A = 2/TC + T/2\Gamma - G_1 + G_n$$
$$B = 2T\Gamma$$
$$D_1 = 2G_1$$
$$D_n = 2G_n \tag{11b}$$

and let

$$A = U_a L_a \tag{12a}$$
$$B = L_b U_b. \tag{12b}$$

Define

$$W_a = \Psi^{-1}\left(L_a V + U_a^{-1} J\right) \tag{13a}$$
$$W_b = U_b V \tag{13b}$$
$$G_1 = \text{diag}[g_{11}, 0, \cdots, 0] \tag{13c}$$
$$G_n = \text{diag}[0, \cdots, 0, g_{nn}] \tag{13d}$$
$$D_{1s} = 2G_1 L_a^{-1} \tag{13e}$$
$$D_{ns} = 2G_n U_b^{-1}. \tag{13f}$$

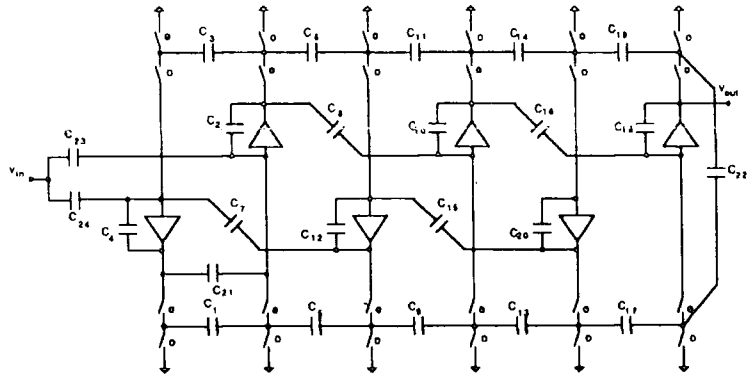


Fig. 5. UL–LU type SC circuit.

The upper triangular matrix U_{as} and lower triangular matrix L_{bs} are defined (Appendix) to satisfy the identity

$$U_{as}L_c = L_{bs}U_b. \tag{13g}$$

Also let

$$J' = -(1 + D_{1s}A^{-1})J \tag{13h}$$

Then (11a) can be linearized as

$$\begin{cases} U_aW_a = -[(\Phi L_b + D_{ns})W_b + \Phi D_{1s}W_a] \\ \qquad\quad -(2 + D_{1s}U_a^{-1})J & \text{(14a)} \\ L_{bs}W_b = \Psi U_{as}W_a - U_{as}U_a^{-1}J. & \text{(14b)} \end{cases}$$

Notice now that the output is w_{bn}. As U_b is upper triangular, w_{bn} differs from the original output v_n by only a constant factor. An example of a UL–LU circuit is shown in Fig. 5. Such circuits are found to be useful for special wide-band filtering problems [14].

V. Bilinear-LDI Ladder Design

In LDI transformed ladders, a $z^{\pm 1/2}$ factor is introduced to represent the improperly realized terminations and to ensure stability, causing a distortion of the designed frequency response. The bilinear transformation, on the other hand, has the advantage of both stability and exactness. Unfortunately, bilinear integrators are sensitive to the stray capacitance and are not practically useful. Instead, an equivalent SC ladder utilizing LDI integrators can be formed.

After bilinear transformation $s \to (2/T)(1 - z^{-1})/(1 + z^{-1})$, (3) becomes

$$\left[\frac{2}{T}\frac{1 - z^{-1}}{1 + z^{-1}}C + \frac{T}{2}\frac{1 + z^{-1}}{1 - z^{-1}}\Gamma + G\right]V = J. \tag{15}$$

and multiplying the system through by $(1 + z^{-1})/(1 - z^{-1})$ gives

$$\left[\frac{2}{T}C + \frac{T}{2}\left[\frac{1 + z^{-1}}{1 - z^{-1}}\right]^2\Gamma + \frac{1 + z^{-1}}{1 - z^{-1}}G\right]V = -\frac{1 + z^{-1}}{1 - z^{-1}}J. \tag{16}$$

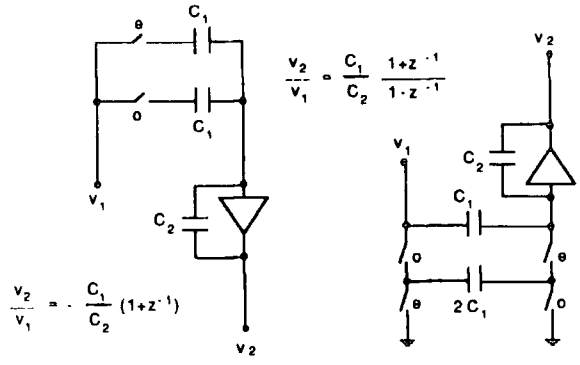


Fig. 6. SC realization of bilinear input functions.

Equation (16) can be rearranged as

$$\left(\frac{1}{\Psi}A + \Phi B + D\right)V = J'' \tag{17a}$$

$$A = 2/TC + T/2\Gamma + G$$
$$B = 2T\Gamma$$
$$D = 2G$$
$$J'' = (1 + z)J \tag{17b}$$

or

$$\left(\frac{1}{\Psi}A + \Phi B + D\right)V = J'' \tag{17c}$$

$$A = 2/TC + T/2\Gamma - G$$
$$B = 2T\Gamma$$
$$D = 2G$$
$$J'' = (1 + z^{-1})J. \tag{17d}$$

A. Termination Problem

Although system (6) is derived by LDI transformation while system (17) arises from the bilinear transformation, they both have the same appearance apart from the input terms. This equivalence makes it possible to design bilinear ladders using LDI integrators, a fact indicated first by

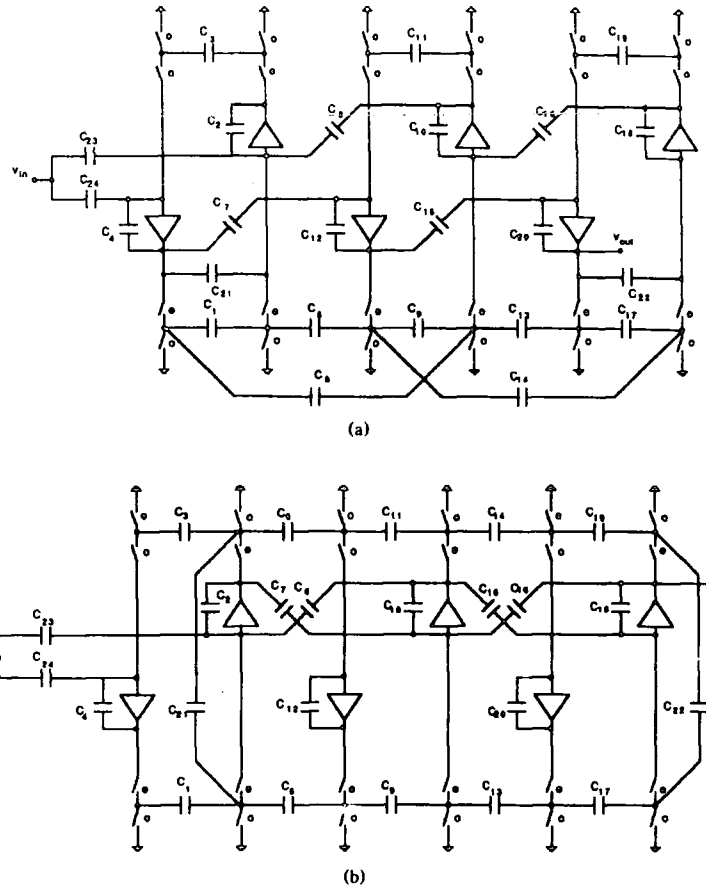


Fig. 7. Exact bilinear-LDI SC filters. (a) Left-ULD type SC circuit. (b) Right-ULD type SC circuit.

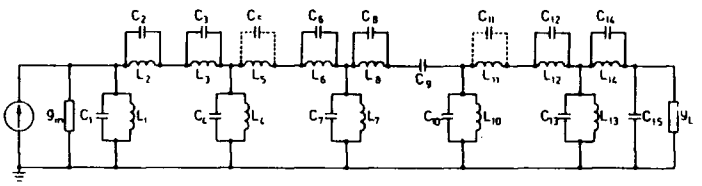


Fig. 8. A 20th-order bandpass ladder prototype.

Lee and Chang [4] from a topological basis for SC circuits. Application of the methods of Section II to (17) results in a similar range of circuit structures.

The input of (17a) has a $(1+z)$ or $(1+z^{-1})$ multiplier. The realization of the noncausal factor $(1+z)$ can be accomplished by multiplying by z^{-1} giving $(1+z^{-1})$, and introducing a delay of one period. Several realizations are possible.

Direct realizations of $(1+z^{-1})$ for left-decomposition designs and $(1+z^{-1})/(1-z^{-1})$ for right-decomposition designs can be achieved by using some special circuit arrangements [15], Fig. 6.

Alternatively, the following systems can be used for left and right decompositions:

$$\begin{cases} \boldsymbol{A}_l\boldsymbol{W} = -(\Phi\boldsymbol{B}+\boldsymbol{D})\boldsymbol{V} - 2(-\boldsymbol{J}) & \text{(18a)} \\ \boldsymbol{A}_r\boldsymbol{V} = \Psi\boldsymbol{W} - \boldsymbol{A}_l^{-1}(-\boldsymbol{J}) & \text{(18b)} \end{cases}$$

$$\begin{cases} \boldsymbol{A}\boldsymbol{V} = -\Phi(\boldsymbol{B}_l\boldsymbol{W}+\boldsymbol{D}\boldsymbol{V}) - \boldsymbol{J} & \text{(19a)} \\ \boldsymbol{W} = \Psi\boldsymbol{B}_r\boldsymbol{V} - 2\boldsymbol{B}_l^{-1}\boldsymbol{J}. & \text{(19b)} \end{cases}$$

It can be verified that (18) and (19) are equivalent to the original system (16), respectively. They can be directly simulated by SC circuits with LDI type integrators. Notice

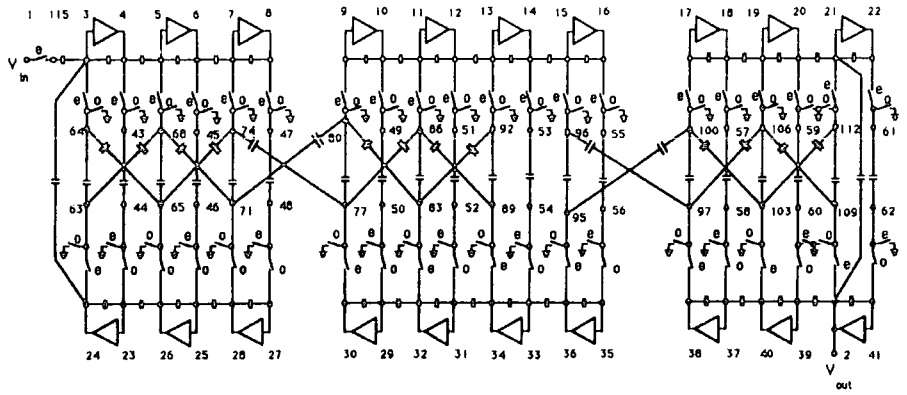


Fig. 9. Left-LUD SC ladder simulation with broken loops.

if J has only one nonzero input, i.e., $J=[J_1,0,\cdots 0]$, it is preferable to have the first column of A_l^{-1} and B_l^{-1} with as few nonzero entries as possible. This number is minimized to one when A_l^{-1} and B_l^{-1} are upper triangular matrices, which occurs when UL or IA or IB decompositions are selected. Fig. 7 shows examples of exact left-and right-ULD circuits.

Both the above methods require some extra components that may introduce a significant layout overhead for low-order filters. They may be simply dispensed with by replacing the $(1+z^{-1})$ factor in the numerator function by 1 or z^{-1}, resulting in the same circuit structures as LDI ones. However, this incurs a penalty warping function of $(1+z)^{-1}$ or $z^{-1/2}\cos^{-1}(\omega T/2)$, and a zero at half the sampling frequency is lost. The distortion introduced in the passband by $\cos(\omega T/2)$ can be corrected by prewarping the original prototype ladder. This can also be conveniently combined with $\sin(x)/x$ correction resulting in a $x/\tan(x)$ function, which can then be superimposed on the frequency response specifications [16]. If the sampling frequency is very high compared with the center frequency, as is often the case in practice, $x/\tan(x)=1$ and no real compensation is necessary.

B. Modification of Bilinear Discrete Ladders

In some cases matrix A in (17) has more nonzero entries than its counterpart matrix in (6), costing more circuit elements in realization. This happens when there are inductance branches without corresponding parallel capacitance branches in the prototype, and consequently A is less sparse than C after adding the nonzero entries of $(T/2)\Gamma$ to the zero entries of $(2/T)C$. The pure inductance branches are normally used to realize poles at infinity. Since the entries in $(T/2)\Gamma$ are usually much smaller than those in $(2/T)C$, addition of $(T/2)\Gamma$ to $(2/T)C$ also causes an uneven distribution of values in A and results in a large capacitance spread in the SC implementation.

The difficulty can be overcome by placing a negative capacitor, C_i, in parallel with the purely inductive branch,

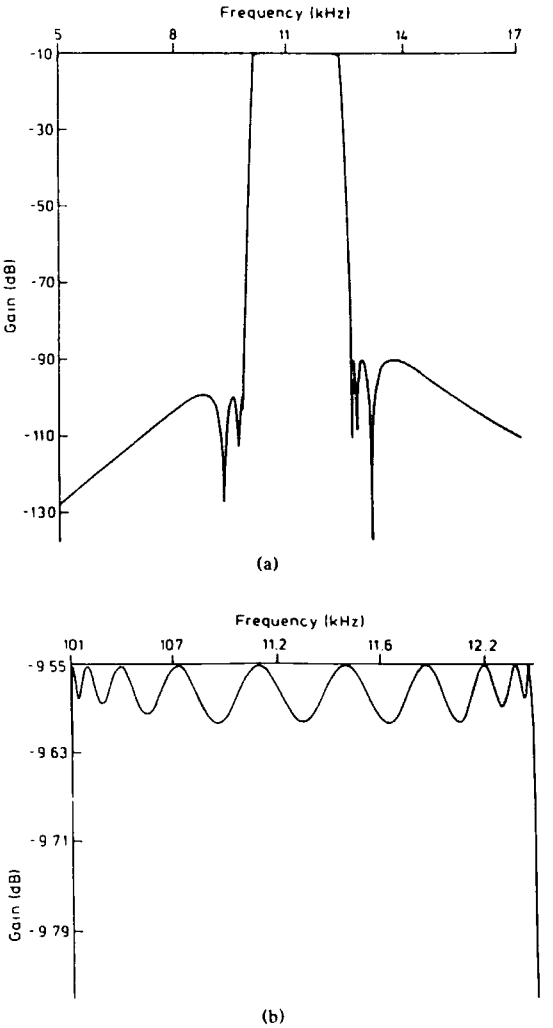


Fig. 10. A 20th-order bandpass filter. (a) Overall response. (b) Passband response.

TABLE II
DESIGN DATA FOR A 20TH-ORDER SC LADDER FILTER

Normalized Data for the *RLC* Ladder

g_{in}	1.0	G_L	0.51020				
C_1	2.4200	L_1	0.39346	C_2	9.1911	L_2	0.084942
C_3	7.9789	L_3	0.16361	C_4	8.5633	L_4	0.11936
C_5	−0.001237	L_5	2.5595	C_6	1.4699	L_6	0.99020
C_7	10.453	L_7	0.09341	C_8	3.2603	L_8	0.23531
C_9	0.59787			C_{10}	10.308	L_{10}	0.095873
C_{11}	−0.0016599	L_{11}	1.9075	C_{12}	3.1240	L_{12}	0.42852
C_{13}	7.6061	L_{13}	0.14009	C_{14}	3.04204	L_{14}	0.23821
C_{15}	0.51578						
lower passband edge			0.9075	upper passband edge			1.1065
lower stopband edge			0.877	upper stopband edge			1.132
passband ripple			< 0.03 dB				
lower stopband atten.			> 95 dB	upper stopband atten.			> 85 dB

Component Values for the SC Ladder

NODE1	NODE2	VALUE	NODE1	NODE2	VALUE	NODE1	NODE2	VALUE	NODE1	NODE2	VALUE
4	3	24.38	4	5	10.37	6	5	9.095	6	7	40.92
8	7	39.09	10	9	47.51	10	11	6.576	12	11	25.31
12	13	4.401	14	13	5.049	14	15	4.493	16	15	43.78
18	17	46.54	18	19	7.795	20	19	14.39	20	21	4.113
22	21	2.712	24	23	16.32	26	23	18.05	26	25	28.15
28	25	18.62	28	27	30.77	30	29	28.71	32	29	9.335
32	31	22.63	34	31	9.969	34	33	34.52	36	33	3.243
36	35	31.09	38	37	32.58	40	37	15.40	40	39	28.45
2	39	6.541	2	41	30.91	43	44	1.000	45	46	1.000
47	48	1.000	49	50	1.000	51	52	1.000	53	54	1.000
55	56	1.000	57	58	1.000	59	60	1.000	61	62	1.000
63	64	3.764	65	64	4.341	63	68	1.670	65	68	3.558
71	68	1.000	65	74	6.805	71	74	13.62	77	74	1.000
71	80	1.000	77	80	10.02	83	80	2.349	77	86	1.000
83	86	5.139	89	86	2.533	83	92	1.000	89	92	1.852
95	96	10.65	97	96	1.000	95	100	1.000	97	100	10.70
103	100	4.128	97	106	1.463	103	106	4.049	109	106	1.000
103	112	1.243	109	112	1.000	24	3	2.993	2	21	1.383
115	3	1.000									
total capacitance				814 units			capacitance spread			47.5 units	
capacitance unit				1 pF			clock frequency			800 kHz	
number of capacitors				73			number of switches			81	
number of op-amps				20							
lower passband edge				10.1 kHz			upper passband edge			12.45 kHz	
lower stopband edge				9.18 kHz			upper stopband edge			13.00 kHz	

L_i, of value

$$C_i = -\frac{T^2}{4}\frac{1}{L_i}. \tag{20}$$

Then from (17) the contributions of C_i and L_i will cancel each other. This reduces both the number of capacitors and spread of capacitance values. The resonant frequency of the pole due to C_i and L_i is given by

$$s_r^2 = \frac{-1}{L_i C_i} = \frac{4}{T^2} = (\pm 2f_s)^2 \tag{21}$$

where f_s is the sampling frequency. If L_i is a series inductance branch in a ladder, s_r will become a zero of the transfer function. The response error thus caused can be eliminated in the approximation procedure, by replacing poles at infinity by ones at $-2f_s$ on the real axis. The negative capacitance required can then be incorporated in the synthesis of the passive ladder prototype [16]. The low-sensitivity properties are not influenced by the introduction of negative elements [17].

For high-order SC filters, these inductor and negative capacitor pairs can be used to cancel the off-diagonal nonzero entries in A, and therefore, break the unfavorable unswitched capacitor op-amp chains that influence op-amp settling times. A 20th-order bandpass ladder (Fig. 8) is simulated by the left-LUD circuit (Fig. 9). The structure is very regular and the long unswitched capacitor op-amp chains have been broken by introducing two negative elements into the prototype. The response of the circuit is shown in Fig. 10; note that special approximation techniques have been used to taper the ripple at the band edges and hence improve sensitivity in these regions. The component values for the circuit are listed in Table II.

VI. COMPARISONS AND APPLICATIONS

Two notable novel categories of ladder simulations presented in Table I are left-LUD and right-LUD (and their duals by UL decompositions) circuits. Both have some characteristic features.

In the left-LUD method the below-diagonal and above-diagonal elements of A are separated to matrices L_a and L_a^T, respectively, effectively removing all capacitor-coupled op-amp loops. They also demonstrate excel-

lent properties regarding component spread and dynamic range for bandpass design. However, since L_a and L_a^T must be square, the dimension of the intermediate variable vector W is n (the number of nodes), and so altogether W and V contain $2n$ variables. Sometimes this is more than necessary. For instance, the left-LUD simulation of Fig. 4(a) could also be used to realize a fifth-order low-pass function. Alternatively, right-LUD methods would use only $2n-1$ variables, a canonical number for an odd order prototype.

For right matrix decompositions, B_l and B_r can be made rectangular and the dimensions of V and W are not necessarily equal. Consequently, the dimension of W can be smaller than that of V. In the case of a low-pass filter simulated by LUD methods, it is mandatory that Γ be singular [17] so that a zero column in L_Γ will appear after LU decomposition. It can be then deleted, making L_Γ an $n \times (n-1)$ matrix. Thus one variable is saved in forming W.

There are also sensitivity problems in lowpass design for all the methods mentioned above except right-LUD. Deviation in the entries of B, caused by the inaccuracy of the element values associated with these entries, may cause B to become nonsingular, introducing a zero at $\omega = 0$. Extra zeros introduced at the origin can be viewed either as an advantage or disadvantage; for instance, low-frequency noise suppression can be facilitated by these zeros. The right-LUD method does not have this problem as it involves multiplication of matrices with only $(n-1)$ rows or columns. The resulting matrices can never have a full rank n.

The right-LUD method, however, does have the drawback of possessing capacitor-coupled op-amp loops. Undesirable large component spread and poor dynamic range are also observed for certain bandstop designs.

These arguments indicate that right-LUD is a good candidate for low-pass design. It is more complicated to reach any conclusion about bandpass designs as the performances the circuits vary dramatically according to the relative bandwidth. This can be seen from some comparative studies.

A. Comparison of Bandpass SC Ladder Designs

The following indices are used as global measures of system sensitivity and dynamic range, respectively:

$$s(\omega) = \left\{ \sum_i \left[\frac{c_i}{|H(\omega)|} \frac{\partial |H(\omega)|}{\partial c_i} \right]^2 \right\}^{1/2} \tag{22a}$$

$$d(\omega) = \left\{ \prod_m |H_m(j\omega)| \right\}^{1/M} \tag{22b}$$

where $\{c_i\}$ and $\{H_m\}$ are the sets of capacitances and op-amp output voltages, respectively, and M is the number of op-amps.

As the passband behavior is of most interest to filter designers, define two indices for system sensitivity and dynamic range, which are the average measures of $s(\omega)$ and $d(\omega)$ over the passband

$$S = \frac{1}{\text{width of passband}} \int_{\text{passband}} s(\omega)\, d\omega \tag{23a}$$

$$D = \frac{1}{\text{width of passband}} \int_{\text{passband}} d(\omega)\, d\omega. \tag{23b}$$

Normally the chip area required for fabrication of an SC filter is measured by

$$T_c = \sum_{\text{all capacitors}} c_i \tag{23c}$$

but to reflect the influence of capacitance spread the following index will also be used

$$C = \left[\sum_{\text{all capacitors}} c_i^2 \right]^{1/2}. \tag{23d}$$

An overall performance index of an SC filter can be defined by

$$P = \frac{CS}{D}. \tag{23e}$$

For these indices, it is desirable to have lower S, T_c, C, and P (the lower limit is 0). The maximum op-amp output will always be assumed to have been scaled to 1, so that D will always be a positive number less than 1. It is desirable to have D close to 1, which means that all the op-amps have equal output swing in the passband.

For a bandpass filter, the relative bandwidth is defined by

$$\text{RBW} = (\omega^+ - \omega^-)/\omega_m, \quad \omega_m = (\omega^+ \omega^-)^{1/2} \tag{24}$$

where ω^+ and ω^- are the upper and lower band-edge frequencies, respectively. It is known that RBW has a great influence on the system performance. For sixth-order elliptic designs, let the passband ripple be fixed as 0.1 dB, stopband attenuation 50 dB and f_s/f_m ratio 25 ($2\pi f_m = \omega_m$, f_s is the sampling frequency). Computations of S, T_c, D, and P are displayed against relative bandwidth (Fig. 11). The same analysis has been performed for higher order elliptic type designs and similar trends are observed.

B. Narrow Bandpass Filter Design

From Fig. 11 it can be seen that the left-decomposition designs have very good total capacitance over the narrow-band range, but the biquad method is better around RBW = 1. Regarding the sensitivity index S, all the ladder designs are much better than the biquad method over the whole range as expected [1]. The plots for cascade biquads are occasionally discontinuous; this is due to the fact that E-type and F-type biquads are selected according to Q-factor required, and discontinuity of internal nodal voltages may take place when the design is switched from E-type to F-type or vice versa affecting the dynamic range index. Another reason is that the pairing of biquadratic sections is carried out to achieve minimum total capacitance, which does not take into consideration voltage levels.

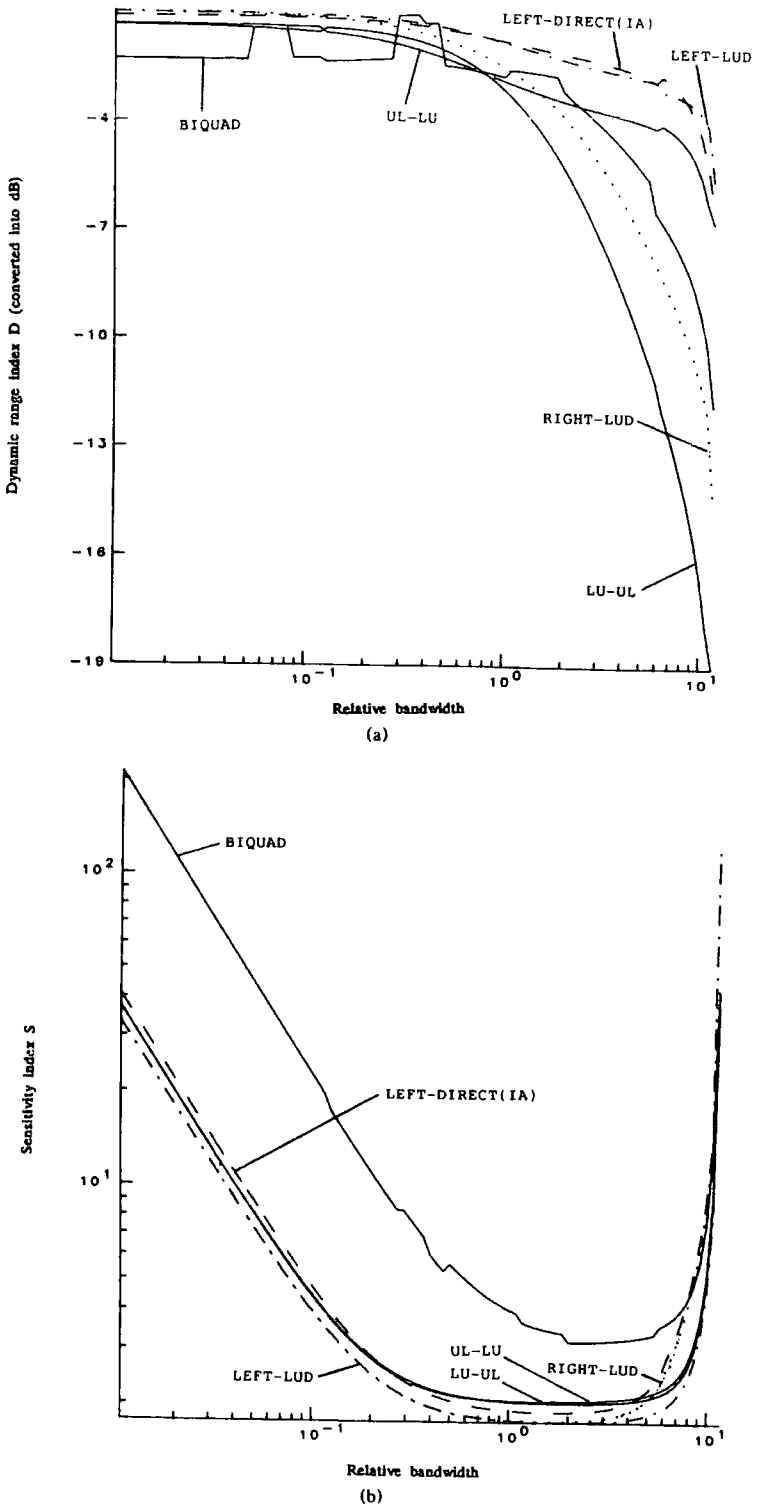
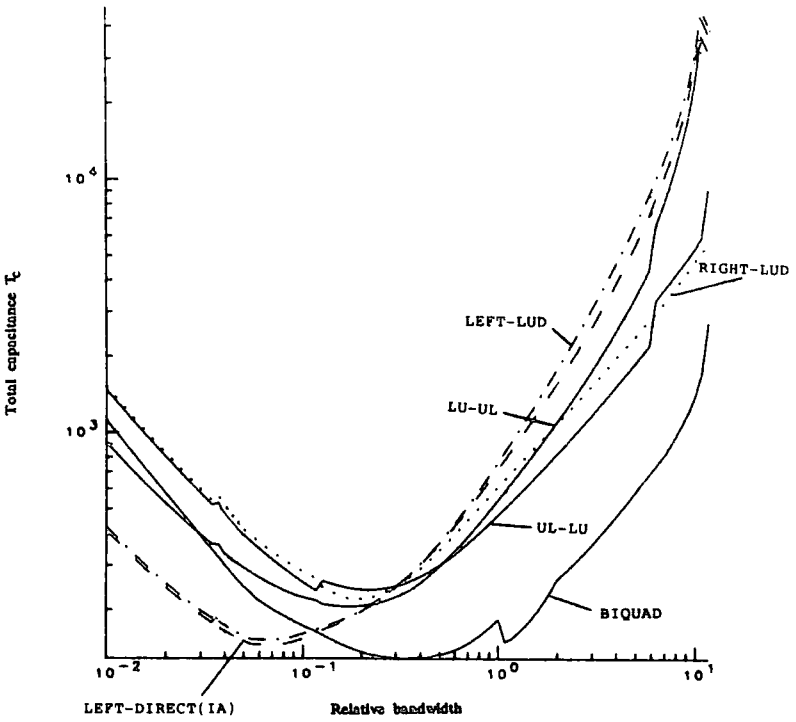
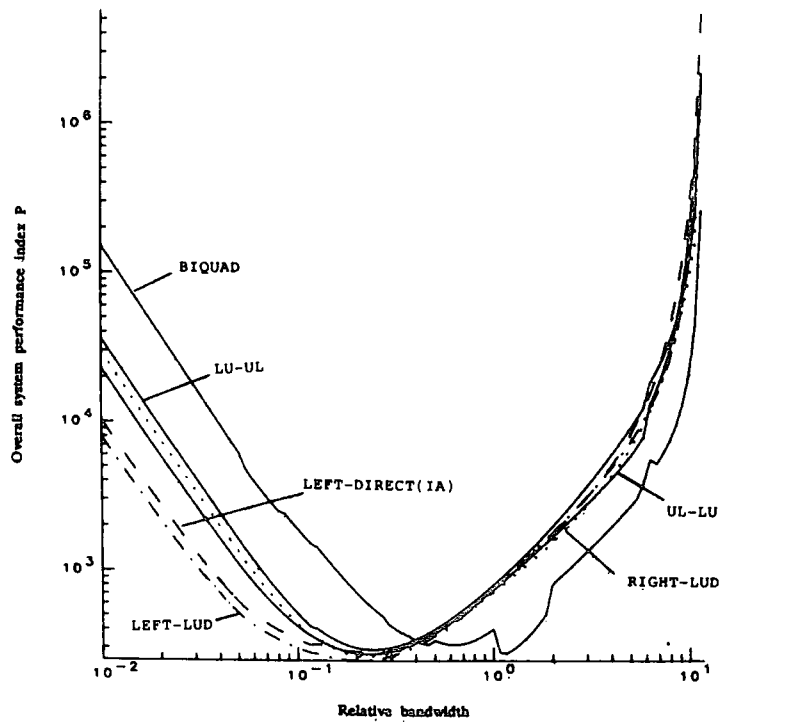


Fig. 11. Performance comparison of 6th-order bandpass filter realizations. (a) Dynamic range. (b) Sensitivity. (c) Total capacitance. (d) Performance index.



(c)



(d)

Fig. 11. (*Continued*)

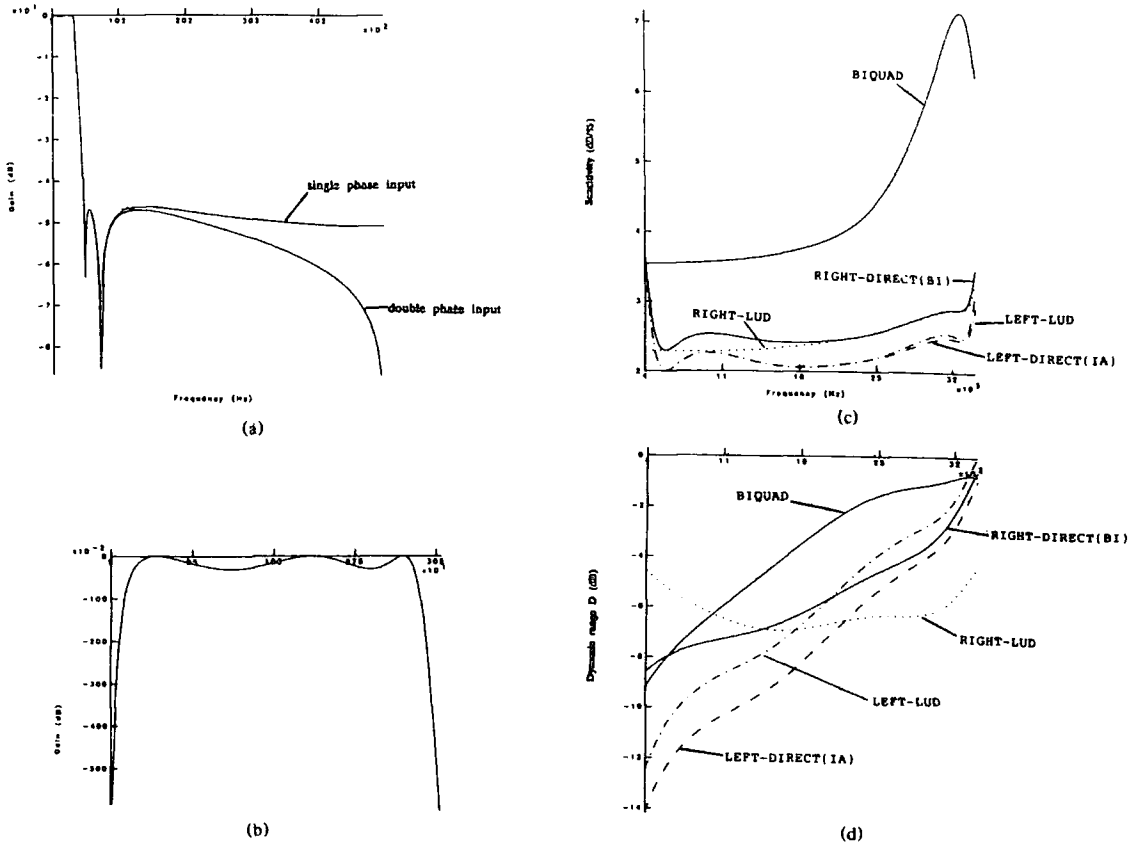


Fig. 12. 6th-order asymmetric bandpass filter realization. (a) Overall response. (b) Passband response. (c) Sensitivity. (d) Dynamic range.

TABLE III
DESIGN DATA FOR A WIDE-BAND PROTOTYPE LADDER OF FIG. 3

C_1	0.3465	C_2	0.1580	L_2	0.2484
C_3	0.6119	C_4	0.0596	L_4	0.3006
C_5	0.4836			L_5	4.0362
G_{in}	1.0000	G_L	0.8802		
Sampling frequency			100 kHz		
Lower passband edge			300 Hz		
Upper passband edge			3400 Hz		
Passband ripple			< 0.2 dB		
Lower stopband edge			10 Hz		
Lower stopband att.			> 30 dB		
Upper stopband edge			5000 Hz		
Upper stopband att.			> 45 dB		

A comparison of the overall performance indices indicates that the left-LUD method is the best candidate for narrow-band design RBW < 1 and the biquad method is best for bandpass design with RBW around 1.

C. Wide Bandpass Filter Design

From Fig. 11 it is seen that both ladders and biquads are far from ideal for a very important area of filtering

TABLE IV
DESIGN DATA FOR WIDE-BAND SC LADDER SIMULATIONS

	Left-LUD	Left-Direct (IA)	Right-LUD	Right-Direct (BI)
C_1	1.000	1.000	3.147	3.147
C_2	9.174	9.174	9.392	9.392
C_3	1.000	1.000	1.000	1.000
C_4	3.620	3.620	9.821	9.821
C_5	1.615	1.615	3.387	1.615
C_6	1.266	1.266	1.266	1.266
C_7	4.445	3.435	3.435	3.435
C_8	1.375	1.375	4.044	4.044
C_9	3.736	3.736	2.391	5.433
C_{10}	21.697	25.451	22.474	22.474
C_{11}	4.632	5.433	1.690	3.736
C_{12}	21.169	22.474	11.201	25.451
C_{13}	1.573	1.573	2.935	1.600
C_{14}	1.000	1.000	1.000	1.573
C_{15}	1.612	1.000	2.074	1.473
C_{16}	1.000	1.000	1.000	1.000
C_{17}	1.000	1.000	1.000	2.137
C_{18}	8.326	9.325	9.953	7.070
C_{19}	1.000	1.265	1.000	1.000
C_{20}	4.804	5.475	51.232	10.686
C_{21}	3.907	3.907	1.252	1.252
C_{22}	4.999	4.999	1.407	1.000
C_{23}	3.120	3.120	1.000	1.000
total	111.199	117.373	150.109	123.014
spread	21.697	25.451	51.232	25.451

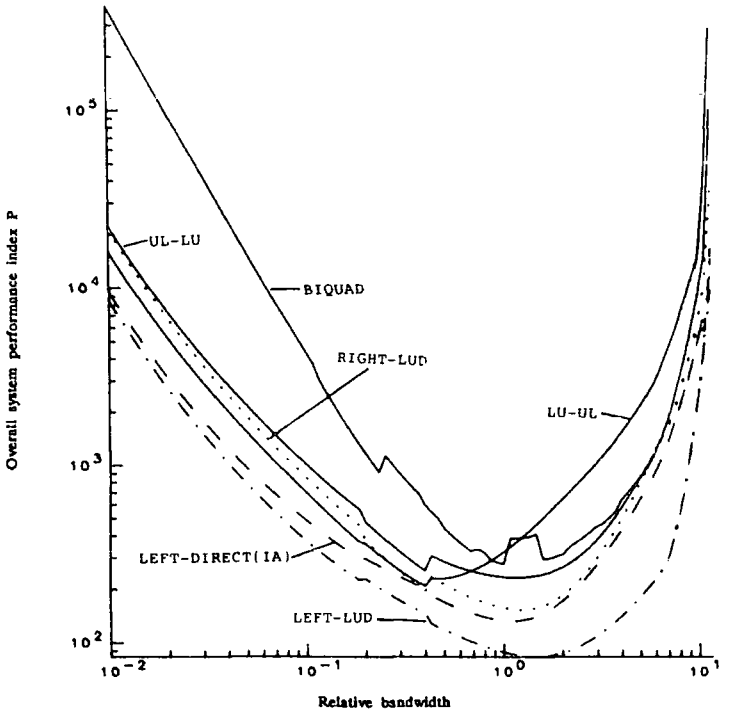


Fig. 13. Performance comparison of 8th-order asymmetric bandpass filter realizations.

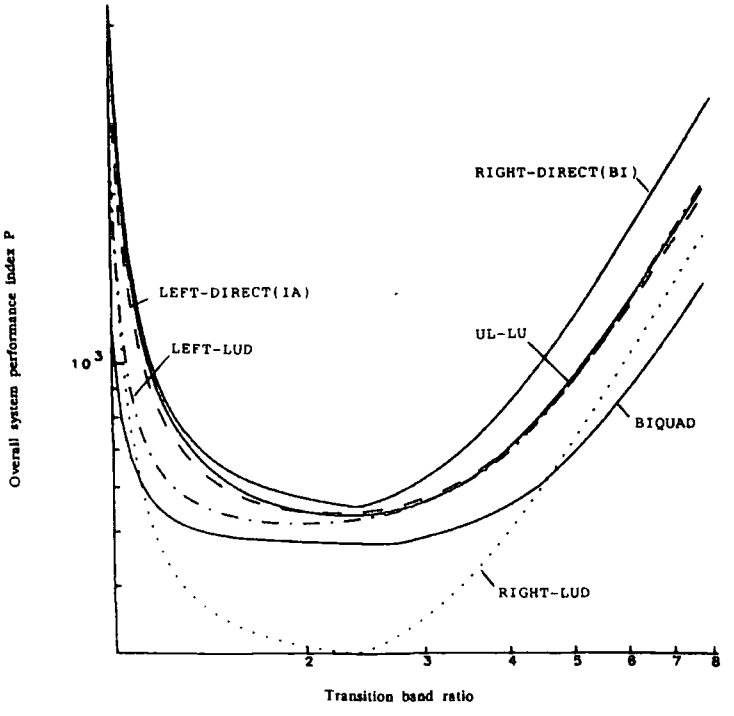


Fig. 14. Performance comparison of 5th-order low-pass filter realizations.

applications, that is, for the voice band application with passband from 300 Hz to 3400 Hz whose RBW > 3. It is found that for this type of wide-band design the most significant factor causing the deterioration of all designs is the location of lower band finite zeros, which approach zero as the RBW increases. Realization of these zeros requires large capacitance spread. The deterioration process can be reduced if the lower band finite zeros are replaced at the origin. Since the zeros in the lower stopband are very close to origin anyway, this shifting will have only a slightly deleterious effect on the characteristic. The performance of a 6th-order design of this type is shown in Fig. 12. The design data of four SC circuits are given in Tables III and Table IV. The left-LUD has the lowest capacitance spread and best dynamic range.

A sweep of an 8th-order design is done over a range of relative bandwidths comparing the performance with four alternative ladder circuits with cascade biquads (Fig. 13). This result echoes the conclusions for the previous specific example—that left-LUD design is still the best choice for this family of filtering applications, exceeding all others over the whole bandwidth range.

D. Low-Pass Design

Fig. 14 shows a sweep of performance index P against transition bandwidth ratio (passband edge/stopband edge) for various 5th-order elliptic low-pass filters. The passband ripple is fixed at 0.1 dB; the passband edge is 1 kHz and the sampling frequency is 200 kHz. Note that only cascade biquad and right-LUD circuits provide one-op-amp-per-pole realizations; the others require six op-amps. Overall, the right-LUD is the best choice followed by biquad. The low sensitivity and good dynamic range of the right-LUD are its main advantages despite the lower total capacitance of the biquad. A sensitivity peak at the origin mitigates against the left-decomposition circuits for low-pass design.

E. Software Development

The matrix scheme discussed in this paper is also highly suitable for software development. A wide range of circuit structures, including both ladders and cascade biquads, can be represented in a unified format. The PANDDA software package [8] has been developed employing this scheme together with many other sophisticated approximation, ladder synthesis, and optimization algorithms.

VII. Conclusions

A methodology has been developed for the design of active-*RC* and SC ladder simulation filters. A wide range of circuits can be derived by adopting different matrix factorizations, notably LU and UL decompositions, including both existing and novel structures. A detailed comparison of various SC circuit structures has been undertaken and some notable conclusions are: the left-LUD method is the best choice for filters with very narrow and very wide passbands; the leapfrog method is the best choice for sharp transition low-pass filter design; and cascade biquads are the best choice for moderately selective low-pass and bandpass filter design. Some special design techniques can be applied to produce efficient circuits in other technologies such as continuous-time transconductance-capacitor filters.

Appendix

When A and B are tridiagonal, L_a and U_b are also tridiagonal as well as triangular. Separate the diagonal and off-diagonal parts of the matrices

$$L_a = L_{ad} + L_{ao} \tag{25a}$$

$$U_b = U_{bd} + U_{bo} \tag{25b}$$

where L_{ad} and L_{bd} are diagonal matrices, L_{ao} has nonzero entries only on the first lower off diagonal, and U_{bo} has nonzero entries only on the first upper off-diagonal,

$$L_{ao} = \begin{bmatrix} & 0 & & & \\ * & & 0 & & \\ & \ddots & & \ddots & \\ & & * & & 0 \end{bmatrix}$$

$$U_{bo} = \begin{bmatrix} 0 & * & & & \\ & 0 & * & & \\ & & \ddots & \ddots & \\ & & & * & \\ & & & & 0 \end{bmatrix} \tag{26}$$

where $*$ stands for the nonzero entries.

In (13) assume that U_{as} and L_{bs} are also tridiagonal and triangular matrices. Separate U_{as} and L_{bs} as

$$U_{as} = U_{asd} + U_{aso} \tag{27a}$$

$$L_{bs} = L_{bsd} + L_{bso}. \tag{27b}$$

Equate the different parts of (13) according to the position of the nonzero entries:

$$U_{asd} L_{ao} = L_{bso} U_{bo} \tag{28a}$$

$$U_{aso} L_{ad} = L_{bsd} U_{bo} \tag{28b}$$

$$U_{asd} L_{ad} + U_{aso} L_{ao} = L_{bsd} U_{bd} + L_{bso} U_{bo}. \tag{28c}$$

Since in (28a–c) the number of constraints is less than the number of variables, we can assign

$$L_{bsd} = I \tag{29}$$

which guarantees the realizability of system (14). From (28) and (29) we have

$$U_{asd} = \left(L_{ad} - L_{ao} U_{bd}^{-1} U_{bo}\right)^{-1} \times \left(U_{bd} - U_{bo} L_{ad}^{-1} L_{ao}\right) \tag{30}$$

and remaining variables can be solved from (28):

$$L_{bso} = U_{asd} L_{ao} U_{bd}^{-1} \tag{31a}$$

$$U_{aso} = U_{bo} L_{ad}^{-1}. \tag{31b}$$

The matrices in (30) and (31) may be singular and the

normal inverses do not exist. In these circumstances, Moore–Penrose's generalized inverse can be used [18]. As the matrices in (30) and (31) are all diagonal, the procedure to obtain their Moore–Penrose inverse is very simple. The Moore–Penrose inverse of a diagonal matrix $D = \text{diag}[d_{11}, \cdots, d_{nn}]$ is also a diagonal matrix given by $M = \text{diag}[m_{11}, \cdots, m_{nn}]$ with

$$m_{ii} = \begin{cases} 1/d_{ii}, & \text{if } d_{ii} \neq 0 \quad (32a) \\ 0, & \text{if } d_{ii} = 0. \quad (32b) \end{cases}$$

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PAPER 47

1294 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 27, NO. 9, SEPTEMBER 1992

Design of a Switched-Capacitor Filter for a Mobile Telephone Receiver

Li Ping, R. C. J. Taylor, R. K. Henderson, and J. I. Sewell

Abstract—**Conventional SC realizations of wide-band filters demand large capacitance spread and exhibit serious sensitivity problems. The UL-LU structure is a ladder type simulation which demonstrates superior sensitivity performance and maintains low capacitance spread. The design illustrates how the facilities of a modern filter compiler can be utilized to solve some quite difficult practical problems in a real application. Results from fabricated devices confirm the predicted properties.**

I. Introduction

THE voice-band frequency range normally extends from 300 Hz to 4 kHz. The difficulty of designing filters in this range is that the relative bandwidth, defined by

$$\text{RBW} = (\omega^+ - \omega^-)/\omega_m, \quad \omega_m = (\omega^+ \times \omega^-)^{1/2}$$

has a typical value of 3.5, which is quite high. Switched-capacitor (SC) realizations of such wide-band filters will have a large capacitance spread and serious sensitivity problems. In general, ladder-based realizations are known to produce low sensitivity solutions [1], though computer simulations [2] have shown that capacitance spread is particularly serious for bandpass leapfrog circuits [3] that use F-type damping. The sensitivity problem for cascade biquads is well known. It is also observed that coupled biquads [4] and LUD methods [5] suffer from high sensitivity at very low frequencies; in the case of low-pass filter filter designs, it has been proven [6] that this property will always result when the so-called right-hand matrix is not decomposed. Similar reasoning can be extended to the bandpass case.

In this paper, a practical voice-band filter design for a mobile telephone application is presented. A novel variant of the LUD method is utilized. It combines a low capacitance spread with low sensitivity, which are important in reducing silicon area and easing the design requirements of the amplifiers and switches compared to other solutions [7]. The strategy is to retain E-type damping (low capacitance spread) simultaneously with right-hand matrix decomposition (low sensitivity), which is not readily available with existing approaches. A modern filter compiler [9] has been used and exercised considerably to provide an optimum solution.

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II. Wide-Band Filter Design

An audio receiving filter for mobile telephony applications typically has a wide passband extending from 300 Hz to 3 kHz and exhibiting a −20-dB/decade slope for frequency de-emphasis. A notch is included to remove unwanted mixed down frequencies which are close to the upper passband edge. The template can be seen in Fig. 1.

If the specification is met by a function with an elliptic-type zero distribution, a very large capacitance spread will be incurred. The finite zeros in the lower stopband create very large time constants that require large capacitors. Alternatively, if these zeros are avoided by choosing an all-pole approximation with zeros at zero and infinite frequency, the required order will be very high. A compromise is to use a function with all lower band zeros at zero frequency and elliptic-type zeros in the upper stopband. Since the lower band edge of the filter is at low frequency, the movement of the lower band zeros to the origin has only a slightly deleterious effect on the filter characteristic [2]. Such a transfer function which meets the required template is shown in Fig. 1. It is a tenth-order function with a third-order zero at the origin, a zero at infinity, a pair of imaginary axis zeros, and two pairs of mirror image real axis zeros. The latter zeros are specially placed to cause negative element values in the passive prototype which cancel components in the SC simulation [2]. The number of capacitors required to realize a pair of mirror image real axis zeros at $\pm 2f_s$ (f_s is the sampling frequency) is less than that to realize a pair of zeros on the imaginary axis. The capacitance spread can also be greatly reduced this way. Since f_s is much higher than the passband frequency, a pair of zeros at $\pm 2f_s$ has the same function as those at infinity. The approximator tidies up after these forcing modifications and ensures that the original specifications are still satisfied.

A comparison of sensitivities is available from the filter compiler PANDDA [9]. This has been made for a number a different realizations [3]–[6] and the results are shown

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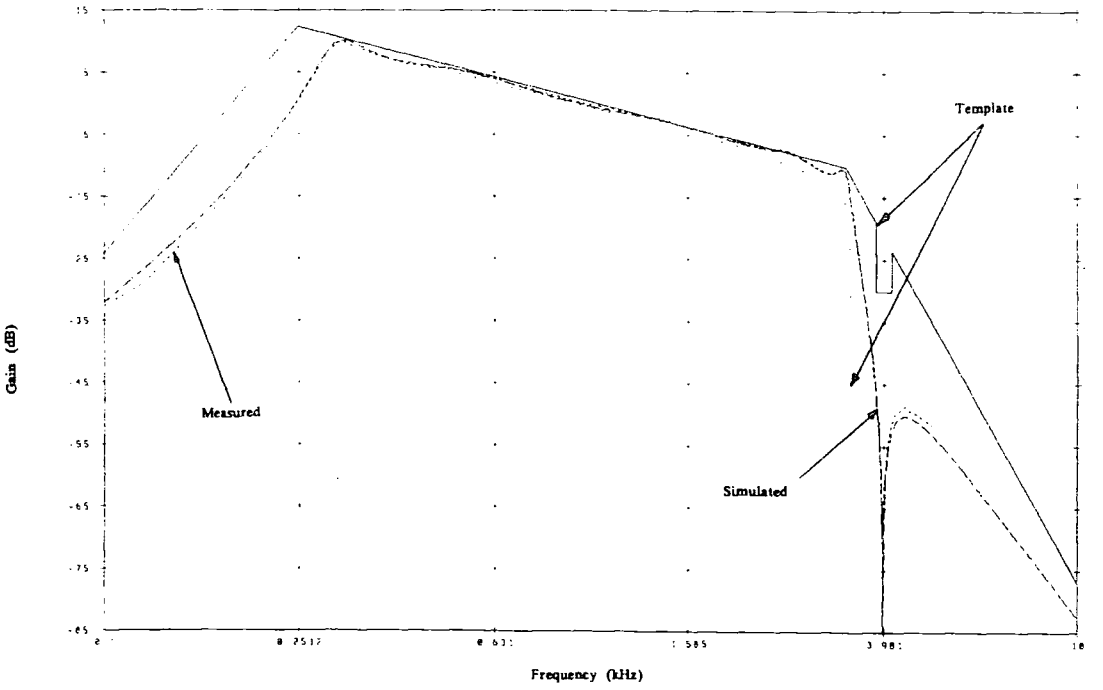

Fig. 1. Template and frequency responses of tenth-order filter.

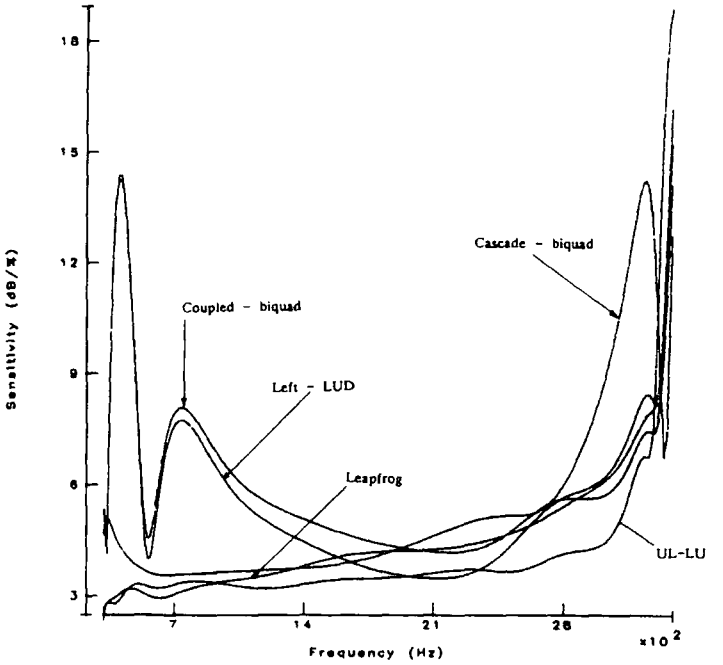

Fig. 2. Passband sensitivity comparison for tenth-order filter realizations.

in Fig. 2. The sensitivity measure being used is

$$s(\omega) = \left\{ \sum_i \left| \frac{c_i}{|H(\omega)|} \frac{\partial |H(\omega)|}{\partial c_i} \right|^2 \right\}^{1/2}.$$

It can be seen that both left-LUD and coupled-biquad circuits suffer from a low-frequency sensitivity peak, whereas the leapfrog and cascade-biquad circuits exhibit poorer sensitivity performance at the higher band edge.

TABLE I
COMPARISON OF CAPACITANCE COSTS FOR FILTER REALIZATION

Structure	Total Capacitance	Capacitance Spread
UL-LU	746.4	113.1
LUD	703.3	112.5
Coupled-E-Biquad	756.4	112.5
Leapfrog	1734.7	957.8
Biquad	728.8	122.5

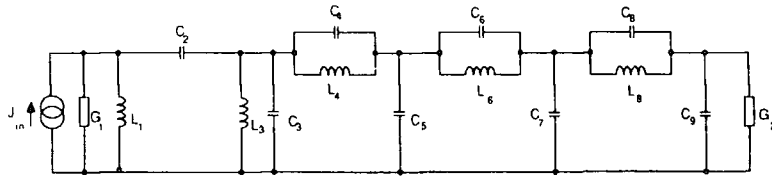

Fig. 3. Tenth-order passive prototype.

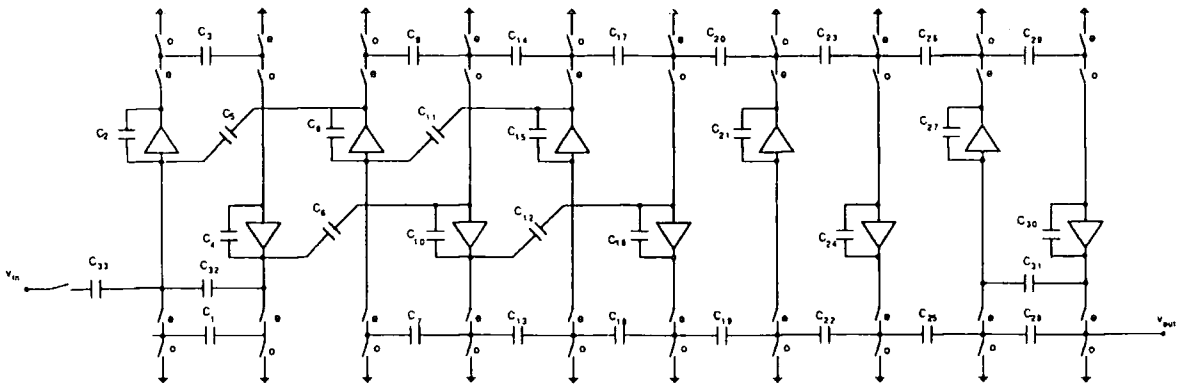

Fig. 4. UL-LU SC circuit realization.

The new UL-LU structure (detailed in the next section) maintains a low sensitivity over the whole passband. Table I gives a comparison of capacitance cost and highlights the penalty of choosing a leapfrog realization. The conclusion of these studies is that the UL-LU structure offers the best solution to this filtering problem. Fig. 3 shows the structure of a passive prototype synthesized from this transfer function. Note that the position of a series capacitor between the first and second nodes is required to ensure E-type terminations [7] in the SC circuit realization shown in Fig. 4. The simpler structure of the filter towards the output is due to the cancellation of feedthrough capacitors by the specially positioned real axis zeros (capacitors C_6 and C_8 in Fig. 3 therefore have negative values).

The circuit uses a clock frequency of 128 kHz and has been fabricated onto silicon using a 3-μm single-metal, double-poly, 5-V process. The amplifiers used are single-stage folded cascode without compensation capacitors, stability being ensured by the capacitors in the filter; the input devices are laid out as cross-coupled common centroid to help with matching and to reduce offsets. The area-to-perimeter ratio of unit to nonunit capacitors is kept constant so that parasitic peripheral capacitance effects are cancelled. The size of the filter is 3027 μm $\times$ 894 μm, which is relatively small considering the complexity of the response. Passband details of the measured frequency response can be seen in Fig. 5. The response meets the template very well and over a number of devices there was hardly any deviation. This illustrates the low sensitivity of the filter to process variations and hence the robust nature of the design. For commercial production this is an important factor in ensuring an increased yield and reliability of the devices. The noise floor at 1 kHz was -60 dB and was approximately level at this value over the entire passband; no harmonic level could be detected above the noise floor.

III. Derivation of the UL-LU Structure

The derivation utilizes a UL-LU decomposition together with a bilinear-LDI ladder design [2]. Starting from

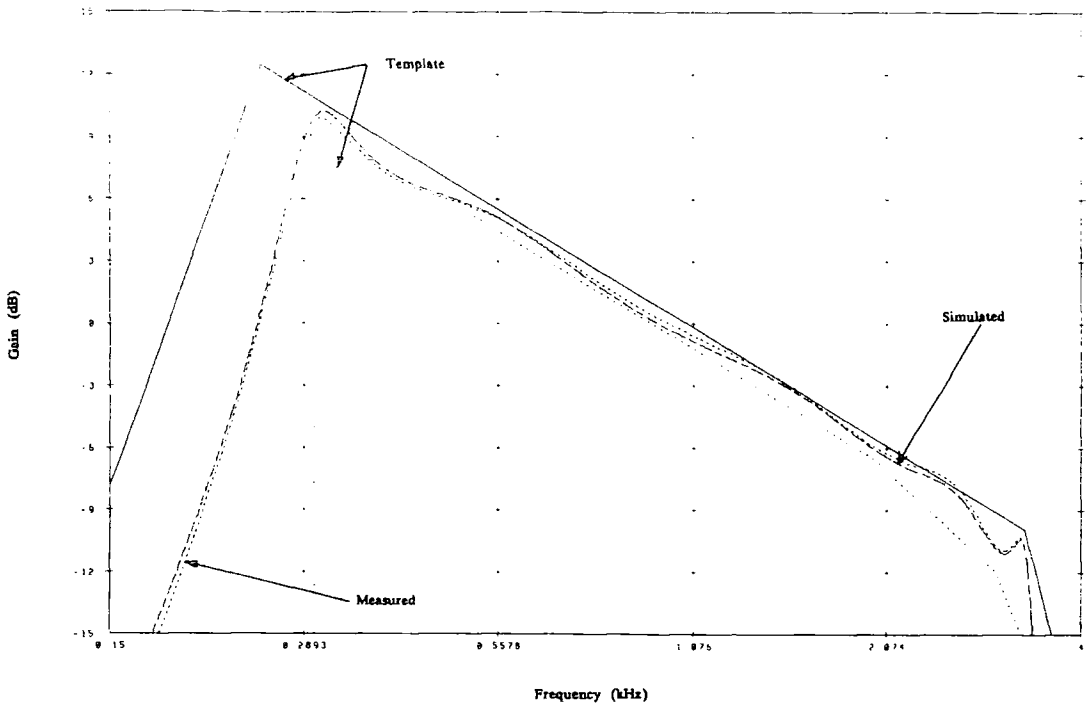

Fig. 5. Passband detail of tenth-order filter.

the nodal equation of a passive prototype ladder

$$(sC + s^{-1}\Gamma + G)V = J, \tag{1}$$

applying a bilinear transformation, and separating out a pair of LDI integration operators $\Phi = 1/(1 - z^{-1})$ and $\Psi = z^{-1}/(1 - z^{-1})$, equation (1) becomes

$$\left(\frac{1}{\Psi}A + \Phi B + D\right)V = (1 + z)J \tag{2}$$

where $A = 2/TC + T/2\Gamma + G$, $B = 4T\Gamma$, and $D = 2G$.

A simplified UL-LU form has $A = U_a L_a$, $B = L_b U_b$, $W_a = \Psi^{-1} L_a V$, $W_b = U_b V$, and $D_s = D U_b^{-1}$. Again the upper triangular matrix U_{as} and lower triangular matrix L_{bs} are defined to satisfy the identity $U_{as} L_a = L_{bs} U_b$. Then (2) can be linearized in terms of the LDI operators as

$$U_a W_a = -(\Phi L_b + D_s)W_b - (1 + z^{-1})J \tag{3a}$$

$$L_{bs} W_b = \Psi U_{as} W_a. \tag{3b}$$

The scheme described by (3) is a variation on those derived in [2]. In general D_s is less sparse than D, as the entry D_{11} when multiplying the first row of U_b^{-1}, which is the upper triangle, would produce a full nonzero row. However, in this design, the first row of U_b^{-1} has only one nonzero entry, resulting from the fact that the first inductance L_1 in the prototype is separated from the other inductors. The beneficial effect of this is to ensure E-type damping at the input of the SC realization and this is consistent with E-type damping already implicit at the output. The virtue of E-type damping is to reduce capacitance spread in the termination sections of the SC realization. Notice now that the output is w_{bn}; as U_b is the upper triangular, w_{bn} differs from the output by only a constant. The realization procedure for (3) by an SC circuit follows matrix methods [2], [9] and yields the circuit shown in Fig. 4. A further point of interest is to note that the input factor $1 + z^{-1}$ in (3a) has been implemented implicitly by prewarping the original specification by a $1 + z^{-1}$ function. This is conveniently combined with the $\sin(x)/x$ correction, resulting in $\tan(x)/x$ prewarping.

IV. Conclusions

In this paper we have examined the problem of designing voice-band SC filters with wide-band specifications. Such filters do not have satisfactory realizations by conventional design techniques due to excessive area requirements or sensitivity to component value deviations. Low-frequency notches, which cause the large component spread, are eliminated by designing a transfer function with lower band zeros at the origin. A new ladder simulation structure has been proposed to overcome the sensitivity and capacitance spread problems of other realizations. A tenth-order filter with sloping passband response has been fabricated and the measured results verify that difficult audio frequency responses can be met practically using a relatively small area of silicon. This

particular design illustrates the potential of modern filter compilers and their application to difficult practical design problems.

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Analog Integrated Filter Compilation

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Abstract. A review of the progress in automated design of analog integrated filters is presented. Such tools are ahead of other analog circuit automation in terms of the acceptance by designers and practical applicability. A survey of the present-day commercial and academic systems is made and the range of facilities available is compared. The problems faced in the design of this type of software are typical of the problems of analog design systems in general; lack of openness for introduction of new design knowledge, difficulties of dealing simultaneously with expert and novice users, poor integration in design environments, and user-interface problems. The structure of a typical system is studied and the computer methods used within are discussed with regard to such issues as speed, flexibility, and ease-of-use. Some future directions for analog filter compilers are proposed.

1. Introduction

Synthesis and compilation tools for analog circuits have been slow to develop compared to their digital counterparts. This has been in part due to the greater difficulty in identifying the rules involved in analog design and a certain reluctance on the part of the designer to accept automation of his or her highly knowledge-intensive skill. Tools that do exist fall mainly into the categories of design capture, analysis and verification. Filter design is an exception; a set of clearly defined hierarchical steps backed up by a large body of well-established mathematical theory renders the discipline amenable to automation. The earliest design programs were developed in the 1950s and 1960s for passive *RLC* filters and demonstrated the feasibility of automatic circuit synthesis [1]. The domain witnessed the earliest application of several computer techniques to circuit design problems (notably optimization). When the modern integrated filter technologies such as active-*RC*, switched-capacitor (SC), and continuous-time arrived in the 1970s and 1980s they were followed up quickly by computer automation [2]. Moreover, these tools were successful in gaining acceptance by designers. There are two main reasons for this confidence. Unlike other analog blocks, high order filter circuits are a common requirement, demanding a considerable number of trade-offs and tedious numerical design steps. These increase greatly with order, quickly exceeding the scope of manual design but ideally suited to the capabilities of the computer. Second, the filter technologies (for mainstream applications) are now very well mastered, allowing a sufficient degree of assurance in "what you design is what you get" to permit computer aids to take over.

What are the main aims in the development of CAD tools for filters?

1. *To reduce design time and cost.* Filter design turnaround is reduced from months to a matter of days. Quick estimates of silicon area and power allow designers to make important trade-offs at system level. Filters synthesized by compilers come with a "correct-by-construction" guarantee (meaning that if there are no errors in the CAD software then the network connectivity and component values must be correct!). No errors means no costly redesign.
2. *To provide optimal designs.* Filter attributes can be tailored to specifications reducing wasted area and power. Computer assistance is essential in this computationally expensive task.
3. *To adapt quickly to changes in the technology.* Now that filter design tools are accepted the challenge is to make them more capable to absorb new technological developments, new circuit topologies and

design methods. This need has been made particularly evident by the continual emergence of new technologies, recently switched-current and MOSFET-C circuits [3–5].

Several filter compilers are now offered commercially and many more reside in academia. Filter design aids are also increasingly found as extensions to digital signal processing packages, standard circuit analyzers, and mathematics and systems simulation languages. This article will look at some of the issues faced in the design of this kind of software as a small illustration of the problems facing the current generation of analog CAD tools. One particularly significant issue, in view of the rapid technological developments over the past 30 years, is the extent to which "technology independent" filter design can be achieved. This means the degree to which the shared design methodology of filter in various technologies can be exploited to provide reusable programs (a major goal of present-day computer science). Good design software must not only be flexible enough to adapt easily to the changing possibilities offered by the technology but must also be able to incorporate the increasing base of knowledge of circuit structures. Versatile databases and algorithms are essential to provide this flexibility and some important contributions to this are reviewed. CAD, in general, is encountering increasingly the problem of tool integration; tools which were developed as stand-alone entities are being asked to work together to build larger systems. Filter compilers are no exception and their lack of integration is hindering the development of mixed analog/digital filter systems. Another theme will be the extent to which automation techniques can hide complexity from the user to provide simpler design decisions. There is always a tension between offering an excessive number of options to a designer and hiding too much ("push-button design"). The former risks bewildering the newcomer and the latter risks losing the confidence of the expert. A continuum between these two extremes needs to be offered by well-designed software with a sufficiently uniform view of the design process. These themes will be illustrated by developments and examples drawn from the XFILT filter compiler [6].

2. Background

Integrated filter compilation is the translation of a filter from a high level design description into layout [7]. There is a hierarchy of levels of description, involving more and more detail as we approach layout. Moving between levels is accomplished by a synthesis step which converts a design from a *behavioral* to a *structural* description. For example, *filter synthesis* commences with the description of the design in terms of a frequency response and terminates with a netlist of parameterized building blocks, e.g., op amps, transconductors, capacitors, resistors, and switches. Several synthesis steps follow before we finally arrive at silicon; for example an analog cell generator will translate from building block to sized device schematic and a layout tool from sized device to layout geometry. A typical organization of such a system is shown in figure 1 and the "state-of-the-art" is summarized in table 1 which compares some of the most reputed systems (this list is by no means exhaustive).

Some pertinent comments follow:

1. There is a very dominant forward path in the compilation process. Most compilers adopt the principle of making fast synthesis modules and placing the designer in control of a "weak" optimization (manual

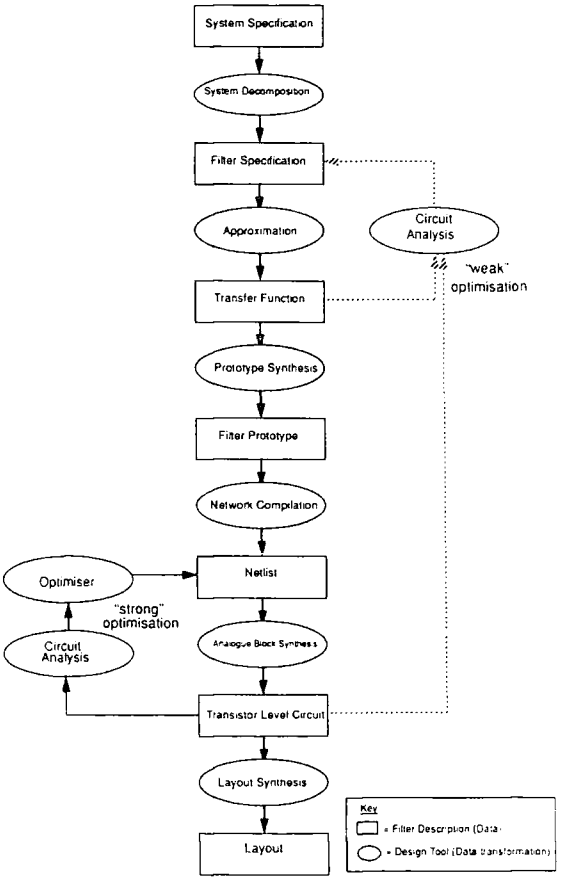

Fig. 1. Design flow in automated filter synthesis.

Table 1. Comparison of integrated filter design software.

Name	Classical approximations	Extended approximation	Allpass Equalisation	Ladder synthesis	Cascade biquad	Layout synthesis	Passive RLC	Switched-capacitor	Continuous-time/ Active-RC	Commercially available	Special features/ comments
S/FILSYN	●	●	●	●	●		●	●	●	●	The original passive filter synthesis program. Now extended to various filter implementations and design methods [8].
filtorX	●	●	●	●	●	●	●	●			A compendium of programs written by graduate students at the University of Toronto.[9-12]
VITOLD	●		●		●	●		●		●	Fairly complete commercial package. Z-domain approximation and synthesis. Sensitivity and THD optimisation.[13]
AutoFilter	●	●			●	●		●		●	Commercial package from Mentor Graphics [14].
PANDDA	●	●	●	●	●		●	●	●		High order touch point approximations.Wide variety of filter structures including new topologies. Non-ideal optimisation.[17]
IMSYS	●			●		●		●		●	Exact z-domain ladder synthesis. Leapfrog simulation ANACAD product. Good practical design options.[15].
FIESTA	●	●			●	●			●		First OTA-C filter synthesiser [16].
SCSYN				●	●	●		●			Gate-array SC filter synthesiser. Unified design of biquad and ladder structures. Noise and capacitance optimisation.[18]
AROMA	●		●		●			●			One of the earliest SC filter compilers. Cascade biquad trade-offs. [2]
MASFIL		●	●		●			●			Simulated annealing design algorithm. Anti-alias filter design. [19]
CAST/ALEX						●		●			Dedicated SC filter layout synthesis tool. Amplifier and switch sizing.[20]
SCULPTOR	●	●			●	●		●			Japanese contribution to filter automation. [21]
PSpice	●	●	●		●			●	●	●	Promising PC synthesis tool in popular environment of SPICE analysis tools .
SCDS	●	●	●		●	●		●		●	Bell Northern Research SC synthesis tool plus University of Waterloo analysis software marketed by Cadence [22]

iteration round the tools, viewing circuit simulation results and altering specifications). The alternative "strong" optimization approach consists of a core circuit simulator, a multivariable optimization package, and a graphical user's interface for viewing simulation results. In this case, an ideal design is taken as a starting point and circuit element values are manipulated by the optimizer to improve the circuit response in the presence of nonidealities such as switch resistance or amplifier bandwidth. However the "weak" approach is more efficient since there are generally many fewer filter specifications than circuit element values, but it relies on designer expertise to interpret simulation results and modify specifications accordingly. The "strong" approach trades speed for generality and ease-of-use tending toward the "push-button" end of design automation. Both (and a range of possibilities in between) are necessary for a complete system.

2. Very few existing compilers offer the complete cycle as depicted in figure 1. In particular, the system decomposition is rarely automated leaving this step to be performed by rule-of-thumb and system designer's expertise. This is a prospective area for future automation. The aim would be to help system designers to set-up realistic specifications and to obtain quickly a feel for the trade-offs involved between blocks and the possibilities offered by the technology.

3. At each of the filter description levels there is a potential to save the state of the design in some data format. There is very little standardization of these formats (except at netlist or layout level) leading to a difficulty in porting information between systems. For example, a standard frequency domain specification format or transfer function description format would allow much more shareable and extendable use of approximation software. At present however, advanced approximation techniques become an inaccessible part of a single system and there is very poor reuse of even standard software. Standard simulator formats for analog and switched-capacitor circuits are emerging by

default as SPICE and SWITCAP. Layout descriptions have already the GDSII and EDIF formats available. In certain cases this is the domain of analog behavioral modeling languages such as the projected analog extension to VHDL.

4. Compilers are normally devoted to only one design strategy and technology. Commercial compilers in particular restrict themselves to the mainstream design flow of cascade biquad designs in switched-capacitor technology derived from classical approximations (Butterworth, Chebyshev, etc.). This limits the designers ability to combine and compare technologies (e.g., active-*RC* and SC) and the benefits of different topologies (e.g., biquad and ladder). Not enough work has been put into an open framework of description for the design methods and the networks.

5. The importance of having more powerful approximation software is emerging [23]. As the design steps close to the fabrication technology are optimized the "room for improvement" shifts toward the higher levels of design (see also point 2) such as approximation. For example, traditional approximations based on classical functions (Butterworth, etc.) yield fu:..ctions with *flat* passbands which are suitable for frequency division multiplexing applications. However, filters with *shaped* frequency response can also compensate for signal distortions from other parts of a communications system (typically antialiasing and transmission line losses). Compared to a standard equalizer/filter solution the incorporation of an equalizing capability in the filter results in smaller circuits and better overall performance. Approximation for such designs is increasingly being recognized as a necessary utility in a compiler and several packages offer some facility to optimize a frequency response to an arbitrarily shaped template [17, 19, 22].

Instrumentation and data communications require approximations based on phase and time domain requirements. There is very little software available for such tasks and mostly designs are either "handcrafted" or cast in terms of problem to be solved by an optimization package.

6. The majority of compilers originate from universities. As with all analog CAD software it covers a very narrow and highly specialized group of users. The ratio of difficulty of development of the software to potential market is high, making it commercially unattractive. One solution to this problem is to place the software under the "umbrella" of digital CAD tools (i.e., make use of the schematic capture, layout, database, and user-interface standards). Closer integration would allow the digital tool to claim "full mixed analog/digital synthesis capability" while protecting the analog tool's interests.

3. Computer Methods for Analog Filter Compilation

The previous section has taken an external view of the existing filter compilers and the trends in their development. The present section will take an internal view and will examine some of the computer techniques being used inside such systems.

3.1. Approximation

In filter approximation a realizable transfer function must be computed to meet specifications of amplitude and delay in time or frequency domains. Obtaining a good approximation is a struggle between conflicting demands of filter selectivity, group delay variation, time domain response, and transfer function order. Approximation software can either help or hinder this process depending on its flexibility, speed and ability to satisfy both advanced and beginner users.

Table 2 shows a survey of the most successful algorithms for filter approximation. From a software perspective, a major remaining issue is simply the degree of accessibility to the user. Entering the specs and viewing the responses of classical filters such as Butterworth or elliptic is a fairly simple matter of entering fixed parameters and viewing the approximated solution. The order of the response can be determined from passband, stopband ripple, and frequency edge specifications (in fact any one of these can be left open, to be determined automatically from the specs on the other three). There is usually very little exploration of responses to be done (often the specification will even define the order and

Table 2. Comparison of different filter approximation algorithms.

User	Speed	Flexibility	Approximation Method	Properties	Ref
NOVICE	FAST	LESS FLEXIBLE	CLASSICAL	Butterworth Chebyshev etc. flat pass and stopband frequency domain amplitude specs.	[24]
			REMEZ	"Pole placer" algorithm family, allows weighted frequency domain passband and stopband specs	[24]
			ALLPASS GROUP DELAY EQUALISATION	Equiripple group delay specifications Remez-type algorithms applicable Less efficient than joint amplitude/ group delay optimisation.	[25]
			LEAST p^{th} OPTIMISATION	Simultaneous specs on amplitude, group delay and time domain response.	[26]
			QUADRATIC PROGRAMMING	As above but slow with convergence problems	
EXPERT	SLOW	MORE FLEXIBLE	SIMULATED ANNEALING	Slowest but avoids local minima problems and is very flexible	[19]

type of approximation to choose) and menu-driven input is quite satisfactory.

Design of more complex responses is quite another matter, the designer has great freedom to vary the characteristics of the filter in the passband(s) and stopband(s) by exploring different pole and zero placements. Here, graphical specification aids are important for the designer to visualize the response in the different domains of interest (frequency, time, and group delay). Often a problem is to view superimposed filter response plus a distortion function from another part of the system or from another cascaded filter. Easy manipulation of the plots and feedback into the pole placer algorithm is needed (e.g., the ability to select and place zeros or to interactively edit the shape of the template). Usually, a graphical input needs to go hand in hand with textual specification for detailed manipulation.

3.2. Prototype Synthesis

Prototype synthesis is the process of decomposition of the transfer function into simple terms corresponding to a realizable circuit building block. It is here that the basic topology of the filter begins to be seen. The algorithms are essentially numerical and are divided into the two principal categories of cascade biquad design and passive ladder synthesis (see table 3). The algorithms themselves are now well known. The problem is now largely how to present the bewildering (combinatorial) number of possible deompositions to the designer. Each decomposition of the transfer function will result in a circuit with different noise, dynamic range, area, and sensitivity.

Ladder synthesis is particularly difficult to automate satisfactorily because it requires an understanding of a number of theoretical conditions on the types of decomposition allowable, yet is worth the bother because of the higher quality circuits it generally provides. For the "push-button" user a default ladder structure can normally be proposed using inbuilt knowledge of the allowable synthesis steps. For the expert who wants to improve on the silicon area, or who needs a special structure of prototype the ladder synthesizer can propose a prioritized choice of structures.

Cascade biquad design requires a choice of a pole sequence and corresponding zero sequence ("pole-zero pairing") of which there are a factorial number. It is feasible up to around 14th order filters to investigate

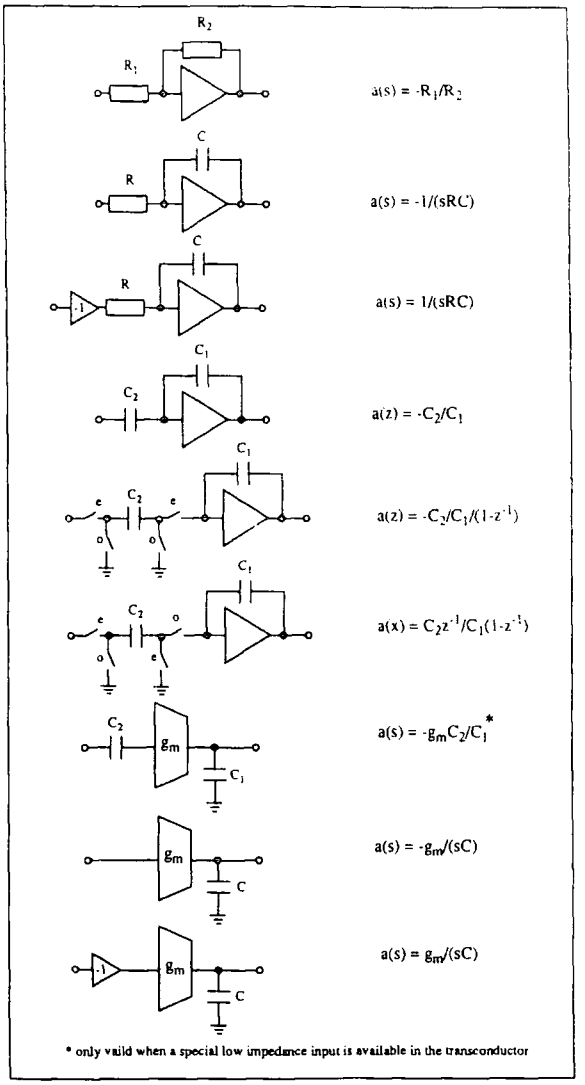

Fig. 2. Filter building-block library in different technologies.

Table 3. Comparison of different filter prototype design methods.

Ease-of-use	Algorithm	Quality of Circuit	Prototype Design Method	Properties	Ref
NOVICE	SIMPLE	LOW	RULE-OF-THUMB POLE-ZERO PAIRING	Cascade biquad circuits. Choose a fixed sequence of poles and zeros according to pre-defined rule	[27]
			COMBINATORIAL POLE-ZERO PAIRING	Cascade biquad circuits. Test all possible pole-zero pairings to find one giving best circuit performance (below 14th order)	[27]
			ITERATIVE LADDER DESIGN	Design a fixed structure of ladder by matching its transfer function iteratively with desired one	[28]
EXPERT	COMPLICATED	HIGH	PASSIVE LADDER SYNTHESIS	Synthesise a ladder by decomposing its transfer function using polynomial manipulation. Accuracy problems. Often needs expert but very general	[29]

all possible combinations. However the assessment needs to be based on some performance measure of the filter, e.g., area and sensitivity. A compiler can have a built-in performance measure or can allow a user to supply his own based on access to analysis results. The expert should also be permitted to enter a user-defined pairing while the "push-button" user can be offered default pairings based on reasonable rule-of-thumb choices, e.g. increasing Q factor for lowest noise transmission.

3.3. Network Compilation

Network compilation is the stage at which a filter prototype is decomposed into a netlist of ideal linear network blocks (capacitors, transconductance amplifiers, switches, op amps, etc.). There is very little standardization here, and the algorithms used are often rewritten for each different structure of filter. Yet a certain degree of technology independence can be maintained at this level so that the designs do not need to be recoded when the implementation of the building blocks change. The main task at this stage is the construction of a linearized flow graph of the circuit in terms of the building blocks. *The flow graph structure itself stays essentially constant between implementations. The basic integrator or resonator building blocks do change in implementation (switched-capacitor, switched-current, transconductor-D, active-RC).*

A convenient and portable representation of a flow graph is a matrix system. Several authors make use of such a system but no convention has emerged [30–32]. One possible form is a pseudostate space description

$$X = AX + BY \tag{1}$$

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} a_{11}(p) & a_{12}(p) & a_{13}(p) \\ a_{21}(p) & a_{22}(p) & a_{23}(p) \\ a_{31}(p) & a_{32}(p) & a_{33}(p) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} b_{11}(p) & b_{12}(p) & b_{13}(p) \\ b_{21}(p) & b_{22}(p) & b_{23}(p) \\ b_{31}(p) & b_{32}(p) & b_{33}(p) \end{bmatrix} \begin{bmatrix} y_1 \\ y_2 \\ y_3 \end{bmatrix} \tag{2}$$

where p can be either s or z and where the functions $a_{ij}(p)$ and $b_{ij}(p)$ represent the transfer function of the building block (typically but not necessarily integrator or resonator transfer functions). Figure 2 shows examples of possible block functions plus their realizations. Note that such a scheme has several advantages for computer implementation:

1. The netlist can be generated directly from the matrix form by representing each x variable by an active device (op amp, transconductor, etc.) output and linking the appropriate block as represented by an a_{ij} from output i to input j. The y vector represents an input signal (normally only one), and they should be linked to the corresponding x input via the blocks indicated by the b terms.
2. A library of the standard cells and their block transfer functions can be set up and modified according to changes in the technology or development of new cell topologies, e.g., low offset integrator structures.
3. Being based on a matrix representation the scheme is ideal for computer implementation and storage. A library of matrix manipulation routines can be made available to allow quick coding of new designs.
4. The matrix can be analyzed directly by substituting the numerical values of the block transfer functions and solving by conventional LU decomposition methods. This provides a quick first check before an external circuit simulator is called and can supply estimates of sensitivity and dynamic range. Note that since the matrix rank is normally dependent on the order of the filter rather than the number of components in the eventual circuit that the analysis is very efficient. The matrix is built up from the transfer functions of the building blocks rather than those of the individual components inside them (as it would in a standard MNA scheme). This avoids reanalyzing each occurrence of a building block in the circuit to determine its transfer function.
5. The matrix allows scaling for minimum area and maximum dynamic range to be performed with ease. Simple row and column multiplications are required.

Both cascade biquad and ladder structures in a variety of technologies can be represented by the above scheme. The designer is then faced with problem of choosing an appropriate topology of cascade biquad or ladder. There are many possibilities such as single op amp biquads, E or F-type biquads, low C-spread biquads as well as leapfrog, coupled-biquad, LU, gyrator-based ladder simulations [29–30]. Each structure has its own characteristic properties of noise, dynamic range, sensitivity and area requirement. The choice is strongly dependent on

1. The class of filtering (bandpass, low-pass, all-pass, etc.)
2. The bandwidth or Q-factor of the filter (narrow-band, wide-band)

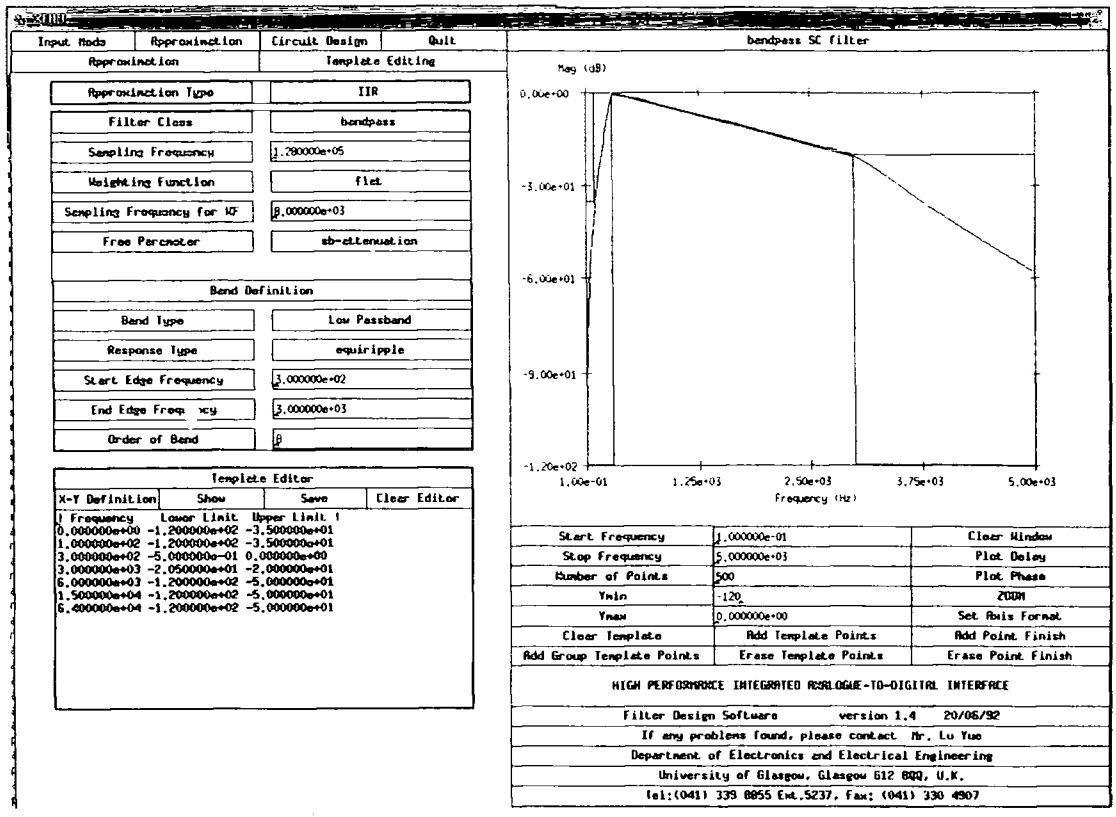

Fig. 3. Screen shot of XFILT showing template specification of lower passband and approximation of eighth order filter.

3. The order of the transfer function (particularly for ladders)

It is difficult to make general rules but usually some helpful defaults can be proposed, e.g., leapfrog structures are good for low-pass odd order designs, coupled-biquad, and LUD are best for bandpass, whereas cascade biquads excel at bandstop designs. Based on experimental running of a compiler over a range of specs a rule base can be established to make a reasonable suggestion of a structure. It is as important to preserve knowledge of successful as well as unsuccessful trial designs to avoid repreating the same mistakes. Otherwise this involves the "weak" optimization of a designer comparing possibilities by repreatedly running the compiler. This is not necessarily a bad thing in terms of designer "psychology" as it keeps him or her as a valuable part of the design process.

3.4. Module Synthesis and Layout

The interface between the block-level network description and silicon is filled by analog cell generators and layout tools. These have been the slowest parts of the design cycle to automate because they deal with difficult nonlinear design problems and are near the fast-changing demands of the technology. Nevertheless, several systems have been presented dedicated to switched-capacitor filters [33]. These programs interpret the loading demands and required charging times from the netlist as specifications on amplifier and switch designs. They then dimension the devices in order to minimize the power and area of the circuit either by an optimizer or by using rearranged device equations. This is normally the least accessible part of the process. Analog block generators are making efforts to become more open to the designer but are still evolving [34–35]. Often the solution is just to use a handcrafted standard amplifier cell and to accept the overspecification of the design.

Analog routers capable of taking into account special requirements of sensitive and noisy nets, power supplies and variable analog transistor sizes and styles have been developed [36]. The inherent regularity of the filter topologies makes this a more amenable task than for more general classes of analog network. Several

dedicated layout strategies for switched-capacitor networks have been reported [18–21]. Normally a fixed topology is adopted (as in random logic layout), row of op amps, row of capacitors, row of switches. The routing problems are greatly simplified and dedicated algorithms can be used. Sensitive nets such as the connections to the virtual ground of the op amp are known in advance and crosstalk can be avoided. Capacitors are designed in units with constant area-perimeter ratios for high-accuracy matching. The user can often control the relative positions of switches, op amps, and capacitors.

4. Automated Filter Synthesis Example

In this section an example of a complete synthesis of a nonstandard filter will be illustrated from the XFILT compiler. Figure 3 shows a screenshot of a filter frequency response being defined to the filter compiler. The response characteristics are defined in stopband and passband by a piecewise template of lower and upper bounds on amplitude and delay. The order and form of the transfer function are specified band by band (in this case the passband). Passbands can be assigned forms anywhere between equiripple and maximally flat and stopbands can have user-defined zero distributions. Of particular note is the 20 dB/decade slope in the passband for preemphasis. Three zeros have been placed at the origin to reduce capacitance spread over an elliptic-style zero distribution. Two notches are placed in the upper stopband but are not seen because of the frequency range of the plot. Figure 4 shows the designer evaluating different realizations of the filter. Depending on the designer's level of expertise so-called automatic, interactive or expert modes of design offer progressively more possibility for user intervention and customization of the circuit design. For example, capacitance spread can be reduced by different pole-zero pairing algorithms. In automatic mode, all possible combinations are tried, in interactive mode the designer chooses from among certain simple preprogrammed pairing rules aimed at making certain specific trade-offs while in expert mode he chooses the sequence by hand. The designer will normally also try a number of different

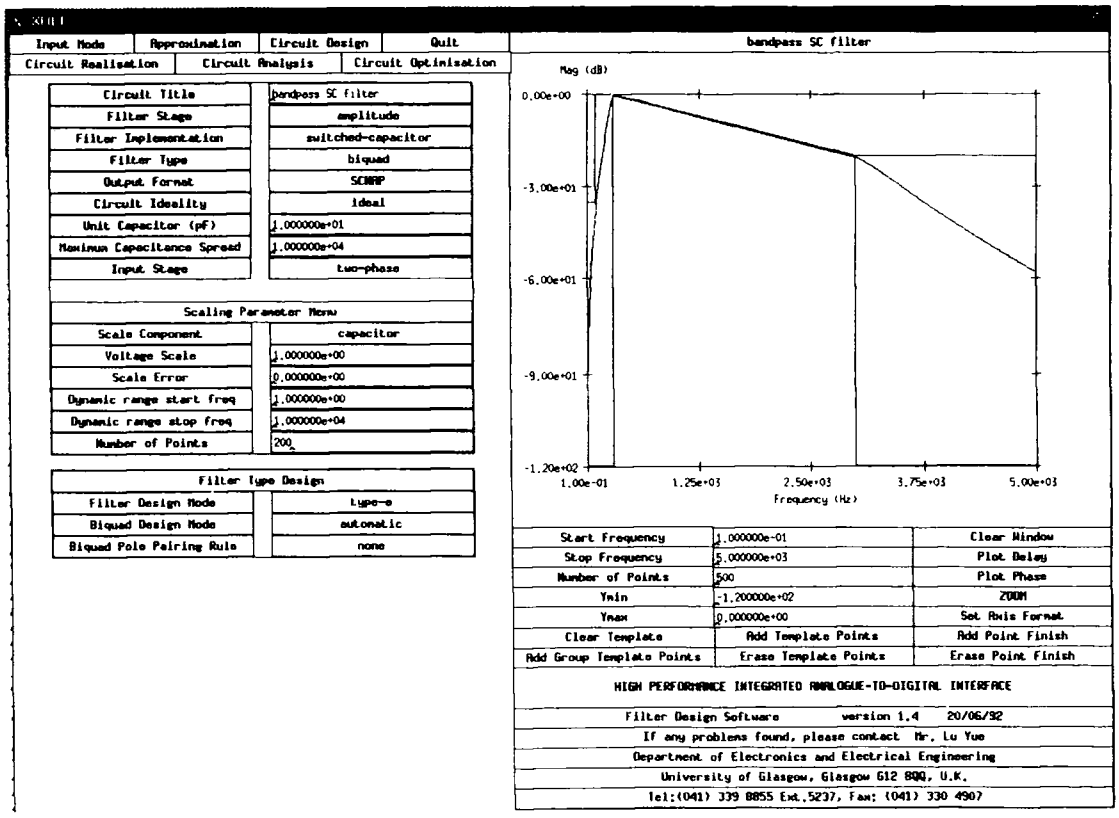

Fig. 4. Screen shot of XFILT showing circuit design of eighth order SC biquad.

circuit structures, comparing component area, power, dynamic range, noise, and sensitivity before arriving at a final choice. A selection of ladder simulation and cascade biquad structures are available. For this filtering problem, an eighth order cascade biquad circuit provides the best compromise between area and sensitivity considerations. Normally the final structure will have been selected after a number of iterations between approximation and circuit realization stages. The measured results of the filter (figures 5 and 6) show excellent agreement with the original template and ideal response. Finally a filter layout is shown in figure 7. The op amps and capacitors are standard cells taken from a library.

5. Conclusions

As regards the basic algorithms for filter design the field is now fairly mature. Moreover, the reliability with which filter compilers can produce good quality designs has been established. More work is now necessary on unifying the framework and offering better access to the design facilities. Integration with digital tool environments and more standardization of data formats is to be hoped for in this direction. Greater gains in terms of design efficiency should now become available at a system level. For example, by allowing the designer to more easily observe trade-offs between different blocks in his filter system design and offering more guidance in the setup of reasonable specifications. This means using the compiler in fast first-cut design mode and by storing informaton about already explored design space. Filter compilers should lead the way toward more integrated analog system design exploration tools.

Acknowledgments

The assistance of Wolfson Microelectronics Ltd. and Lu Yue at the University of Glasgow in producing screen shots of XFILT is gratefully acknowledged.

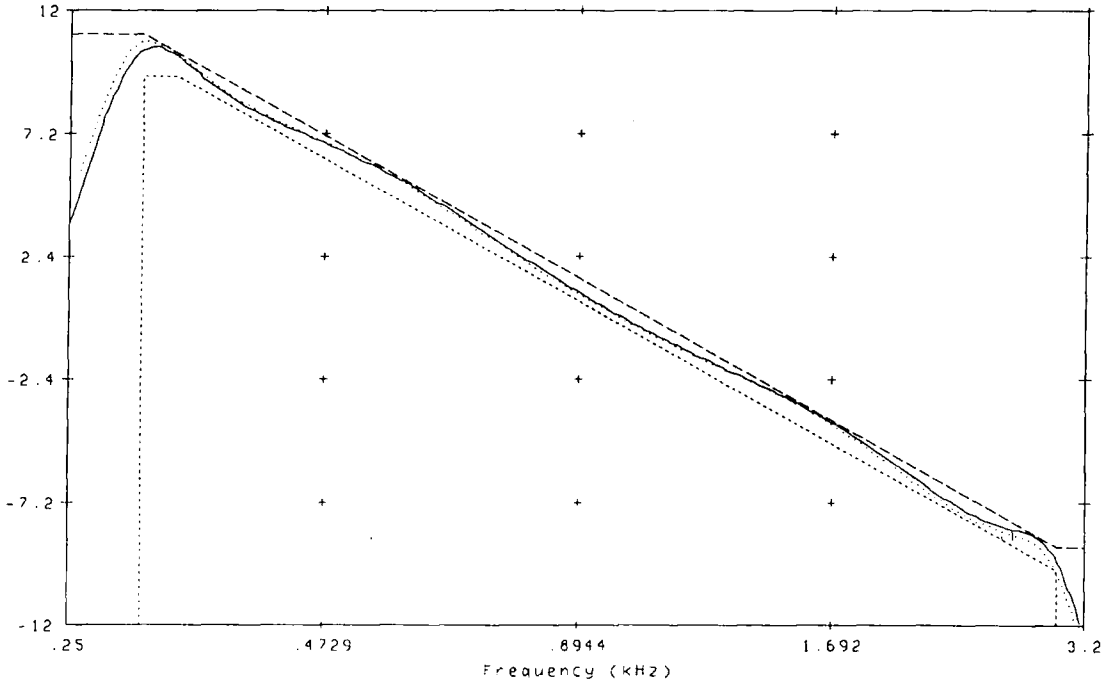

Fig. 5. Ideal passband response (solid) amd measured passband response (dotted) of eighth order SC filter.

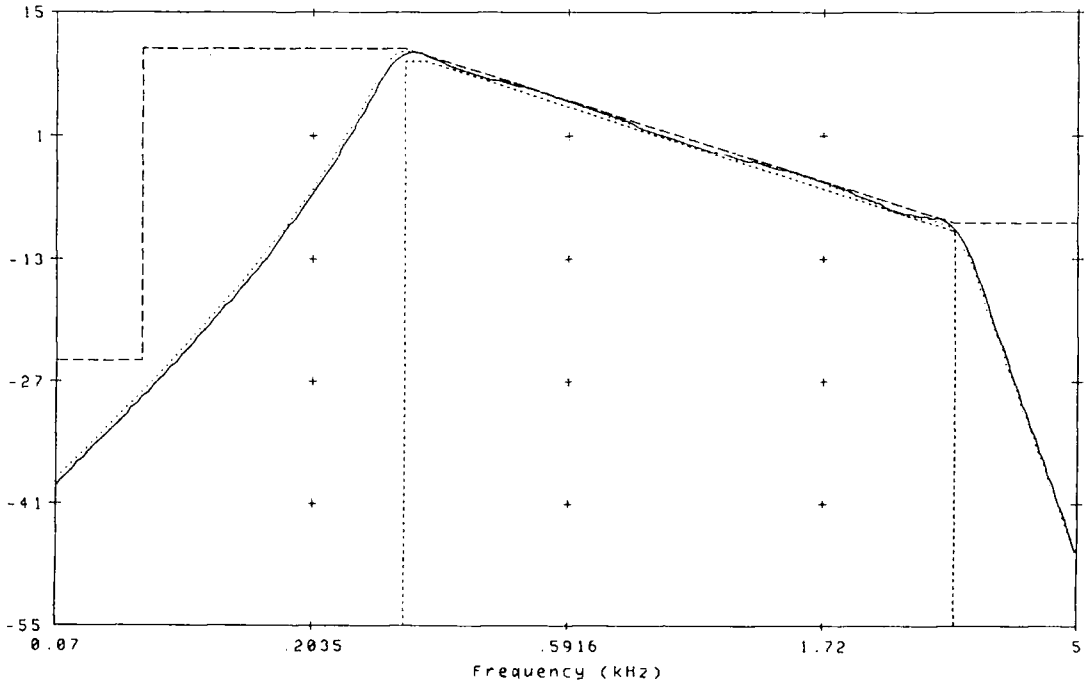

Fig. 6. Overall ideal response (solid) and measured reponse (dotted) of eighth order SC filter.

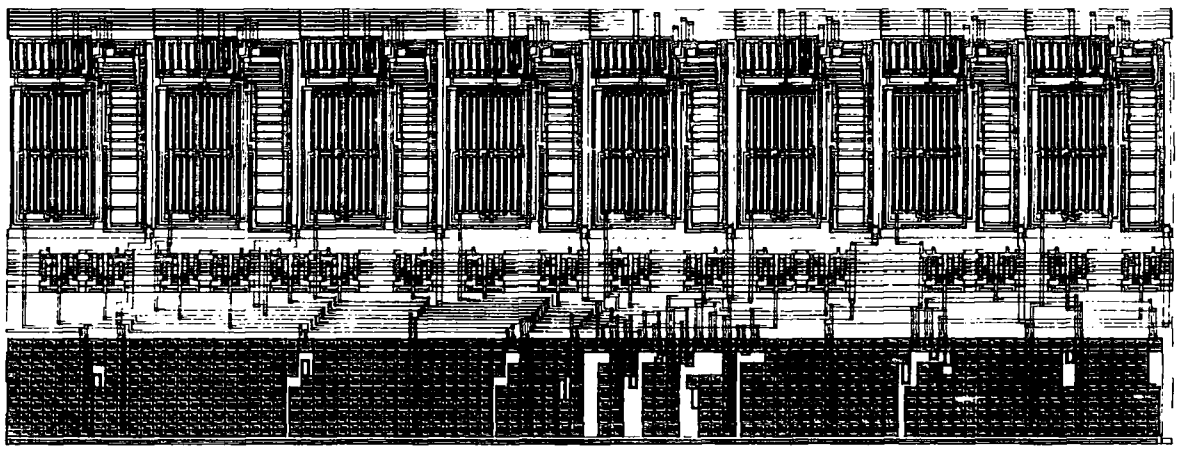

Fig. 7. Circuit layout of eighth order SC biquad filter.

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PAPER 52

Matrix methods for the design of transconductor ladder filters

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Indexing terms: Filters, Transconductor ladder

Abstract: Matrix-based methods for the design of transconductor ladder filters are presented. These allow the realisation of any bandpass or lowpass prototype using only one or two values of transconductance. The new methods are illustrated by experimental results from a 1 MHz elliptic lowpass filter, a 400 kHz elliptic bandpass filter, a 400 kHz Chebyshev bandpass filter, and a PLL frequency-control loop, all fabricated in a 1 μm CMOS process.

1 Introduction

In recent years, much research has been directed towards the development of continuous-time transconductor filters [1–7] as an alternative to switched-capacitor (SC) filters [8], particularly in the frequency range 100 kHz to 10 MHz. Although many linear transconductor circuits have been presented in the literature [9–12], less progress has been evident in the development of filter structures that are well suited to transconductor realisation.

A significant problem has been how to design ladder filters without recourse to ratioed transconductances. Ratioed transconductors are undesirable because the transistors which determine the value of a particular transconductor can vary in size within only a small range without suffering from poor matching in one extreme or producing significant parasitic capacitance and high power consumption in the other. Moreover, it is inconvenient for a designer to have to produce a different set of ratioed transconductors for each new filter design. This problem is specific to transconductor filters as the corresponding variables in RC and SC filters (resistors and sampling capacitors, respectively) can be scaled relatively freely.

Most methods used to derive active RC and SC filters from passive prototypes have been based, explicitly or otherwise, on the simulation of nodal voltages and inductor currents [13, 14]. Examples of such filters are leapfrog and coupled-biquad ladders, as well as circuits obtained by simulating inductors using gyrators [15]. These methods have been applied successfully to the design of lowpass transconductor ladders but they cannot generally be applied to bandpass ladders without the use of ratioed transconductor inputs. This is because, when the voltages of a coupled-biquad bandpass filter are scaled for dynamic range, the summing coefficients between biquads take values which are lower than the coefficients within each biquad by a factor typically close to the fractional bandwidth of the filter. The conventional coupled-biquad bandpass structure can only be used for transconductor ladders having an all-pole response of moderate selectivity [16]. The problem described above is compounded for highly selective filters which require large transconductance ratios, and for prototypes containing inductor loops as these lead to noninteger ratios that cannot be implemented by combinations of a unit transconductance [8].

In this paper, we present matrix-based methods for the design of transconductor ladder filters [17, 18], which can be applied to many more response types than conventional techniques. Ladder filters are considered to be preferable to those formed from cascaded biquad stages, the latter typically having much greater passband sensitivity. The objective of this work is to be able to realise any passive ladder as a canonical transconductor filter using only a single value of transconductance, or a small number of values in simple integer ratios.

Similar matrix methods have already been developed for the design of switched capacitor and active RC filters [19, 20]. As well as formalising the design procedure and providing a framework for computer-aided design tools, the use of matrices has facilitated the discovery of superior active filter structures which are not intuitively obvious. The same advantages are found for transconductor filters.

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The design procedure can be summarised as follows:

(i) A set of equations (derived by Kirchhoff's laws) which describe the passive prototype are combined to form a matrix equation

$$\boldsymbol{J} = (\boldsymbol{G} + s\boldsymbol{C} + s^{-1}\boldsymbol{\Gamma})\boldsymbol{V} \tag{1}$$

where $\boldsymbol{V}$ is a vector representing the nodal voltages (and/or branch currents), $\boldsymbol{J}$ is a vector representing the input current source and $\boldsymbol{G}$, $\boldsymbol{C}$, and $\boldsymbol{\Gamma}$ are matrices whose elements are simple algebraic combinations of the passive component values.

(ii) The nodal voltages and branch currents of the prototype can be scaled if required by performing simple multiplication operations upon eqn. 1.

(iii) The second-order matrix equation is decomposed into two first-order design equations by the introduction of a vector of auxiliary variables, $\boldsymbol{X}$. A large number of decompositions are possible, of which we present those most useful for transconductor filters. The choice of decomposition for a particular filter design is dictated by the type of building block available and the nature of the desired response.

(iv) To form the active filter, each row of each design equation is implemented by a first-order transconductor/capacitor section.

(v) Finally, the filter is scaled in frequency by the appropriate choice of transconductor and capacitor unit values.

2 Matrix representation of the passive prototype ladder

For a given passive prototype ladder, various forms of the second-order matrix equation (eqn. 1) can be constructed, depending on the choice of variables used to form the vector $\boldsymbol{V}$. We use the terms V-representation, I-representation and VI-representation to refer to the use of nodal voltages, branch currents and mixed variables, respectively, in $\boldsymbol{V}$. The choice of representation is governed mainly by two factors. First, the order of the matrices (which equals the number of variables in $\boldsymbol{V}$) should be kept to a minimum so that the resulting active circuit is canonical, i.e. has one integrator per pole of the desired transfer function. Secondly, a representation should be chosen which leads to the matrices $\boldsymbol{G}$, $\boldsymbol{C}$ and $\boldsymbol{\Gamma}$ being as sparse as possible, as the sparsity of these matrices is reflected in the complexity of interconnect in the resulting active circuit.

Each RLC ladder has a 'minimum inductance' and a 'minimum capacitance' version. Identical matrices are obtained if the V-representation is used for the former and the I-representation for the latter. However, the correct representation must be used for a particular prototype to ensure canonicity. Fig. 1 shows the minimum inductance version of a fifth-order elliptic lowpass prototype with 0.28 dB passband ripple and 60.5 dB stopband attenuation. In the V-representation, this ladder is described by the matrices

$$\boldsymbol{J} = \begin{pmatrix} V_{in}/R \\ 0 \\ 0 \end{pmatrix}, \quad \boldsymbol{V} = \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix}, \quad \boldsymbol{G} = \frac{1}{R}\begin{pmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{pmatrix},$$

$$\boldsymbol{C} = \begin{pmatrix} C_1 + C_2 & -C_2 & 0 \\ -C_2 & C_2 + C_3 + C_4 & -C_4 \\ 0 & -C_4 & C_4 + C_5 \end{pmatrix}$$

and

$$\boldsymbol{\Gamma} = \begin{pmatrix} \frac{1}{L_2} & \frac{-1}{L_2} & 0 \\ \frac{-1}{L_2} & \frac{1}{L_2} + \frac{1}{L_4} & \frac{-1}{L_4} \\ 0 & \frac{-1}{L_4} & \frac{1}{L_4} \end{pmatrix} \tag{2a–e}$$

In general, where the LC pairs in a ladder are parallel, it is best to use the V-representation. As an example, Fig. 2

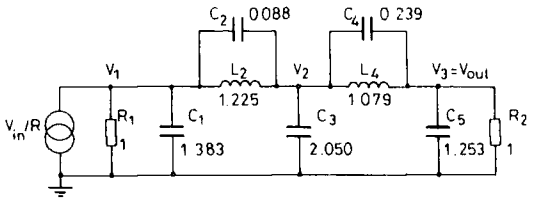

Fig. 1 *Fifth-order elliptic lowpass RLC ladder*

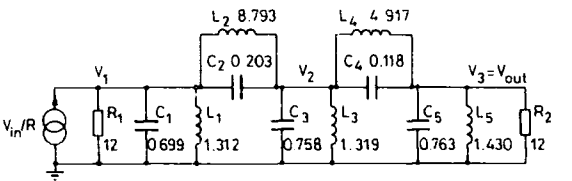

Fig. 2 *Sixth-order elliptic bandpass RLC ladder*

shows a sixth-order elliptic bandpass prototype with 0.1 dB passband ripple and 50 dB stopband attenuation. In the V-representation this is described by the matrices

$$\boldsymbol{J} = \begin{pmatrix} V_{in}/R \\ 0 \\ 0 \end{pmatrix}, \quad \boldsymbol{V} = \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix}, \quad \boldsymbol{G} = \frac{1}{R}\begin{pmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{pmatrix},$$

$$\boldsymbol{C} = \begin{pmatrix} C_1 + C_2 & -C_2 & 0 \\ -C_2 & C_2 + C_3 + C_4 & -C_4 \\ 0 & -C_4 & C_4 + C_5 \end{pmatrix}$$

and

$$\boldsymbol{\Gamma} = \begin{pmatrix} \frac{1}{L_1} + \frac{1}{L_2} & \frac{-1}{L_2} & 0 \\ \frac{-1}{L_2} & \frac{1}{L_2} + \frac{1}{L_3} + \frac{1}{L_4} & \frac{-1}{L_4} \\ 0 & \frac{-1}{L_4} & \frac{1}{L_4} + \frac{1}{L_5} \end{pmatrix} \tag{3a–e}$$

Another example is the asymmetric Chebyshev bandpass ladder shown in Fig. 3.

It will be demonstrated in Section 4 that the complexity of a symmetric bandpass transconductor ladder can be reduced if the condition $\boldsymbol{C} = \boldsymbol{\Gamma}$ is satisfied. This is the

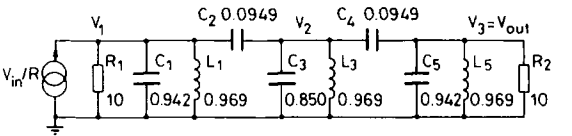

Fig. 3 *Sixth-order asymmetric Chebyshev bandpass RLC ladder*

case if the bandpass prototype is obtained by transformation of each component of a lowpass ladder individually [13, 14] and if the VI-representation is used. For example, the sixth-order elliptic ladder shown in Fig. 4 is

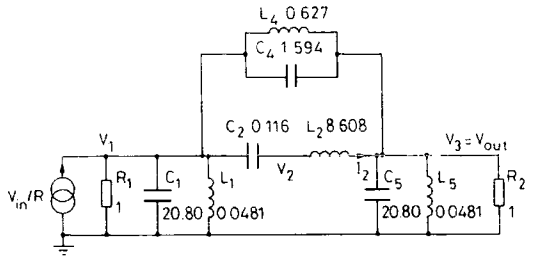

Fig. 4 *Another sixth-order elliptic bandpass RLC ladder*

obtained by transforming each component of a third-order elliptic prototype. In the VI-representation, this ladder is described by

$$\boldsymbol{J} = \begin{pmatrix} V_{in}/R \\ 0 \\ 0 \end{pmatrix}, \quad \boldsymbol{V} = \begin{pmatrix} V_1 \\ V_{I2} \\ V_3 \end{pmatrix}, \quad \boldsymbol{G} = \frac{1}{R}\begin{pmatrix} 1 & 1 & 0 \\ 1 & 0 & -1 \\ 0 & -1 & 1 \end{pmatrix},$$

$$\boldsymbol{C} = \begin{pmatrix} C_1 + C_4 & 0 & -C_4 \\ 0 & \dfrac{-L_2}{R^2} & 0 \\ -C_4 & 0 & C_4 + C_5 \end{pmatrix}$$

and

$$\boldsymbol{\Gamma} = \begin{pmatrix} \dfrac{1}{L_1} + \dfrac{1}{L_4} & 0 & \dfrac{-1}{L_4} \\ 0 & \dfrac{-1}{C_2 R^2} & 0 \\ \dfrac{-1}{L_4} & 0 & \dfrac{1}{L_4} + \dfrac{1}{L_5} \end{pmatrix} \qquad (4a\text{–}e)$$

To maintain dimensional consistency, the current I_2 is represented by the voltage variable V_{I2}, the multiplying factor being the termination resistance R. In this VI-representation, the $\boldsymbol{C}$ and $\boldsymbol{\Gamma}$ matrices are identical because by definition $L_i = 1/C_i$.

3 Transconductor–capacitor building blocks

The general first-order transconductor–capacitor building block has the transfer function

$$V_{out} = \left[\sum_i g_i V_i + s \sum_j C_j V_j\right] \Big/ sC \qquad (5)$$

It is desirable that only one value of g_i be used in a particular filter, but where more than one value is used, they should be in low-integer ratios. Using a conventional transconductor only, eqn. 5 is implemented by the circuit shown in Fig. 5. In this case, the capacitors C_j represent bidirectional coupling paths [21] when driven by internal nodes, as these nodes are all high-impedance. This can be a serious restriction, as many of the techniques available to maintain low-integer capacitor ratios in a filter (Section 4) rely on the use of unidirectional capacitive paths.

To obtain unidirectional capacitive coupling paths, a first-order stage with a low-impedance input and/or output is required. The most obvious realisation of this requires the addition of an opamp to create a virtual earth (Fig. 6). This is expensive in silicon area and current consumption, particularly as the opamp will need a very high bandwidth for video frequency operation. However,

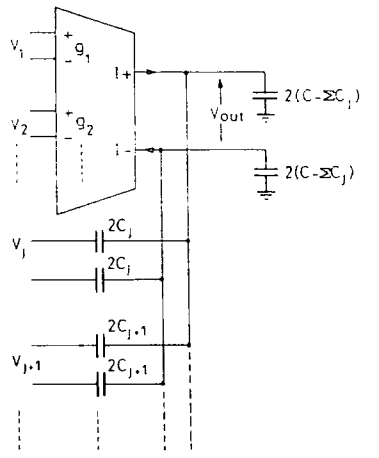

Fig. 5 *First-order section using conventional transconductor*

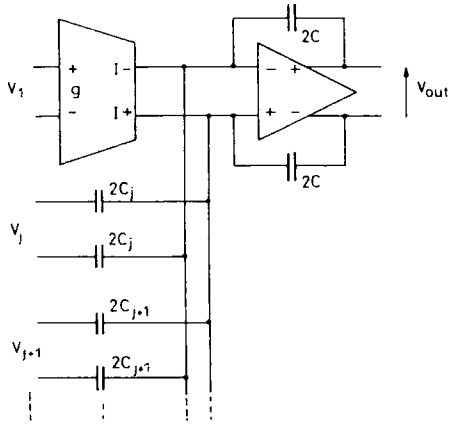

Fig. 6 *First-order section with transconductor and opamp*

these problems are offset by the fact that the design of the transconductor itself can be somewhat simplified because it is only driving into the virtual earth and does not need a very high output impedance. In the extreme, the transconductor can be reduced to a pair of MOSFETs operating in triode mode, giving a so-called 'MOSFET-C' circuit [22].

An alternative solution is to use a recently reported transconductor with low-impedance inputs [23]. The first-order section using this circuit is shown in Fig. 7.

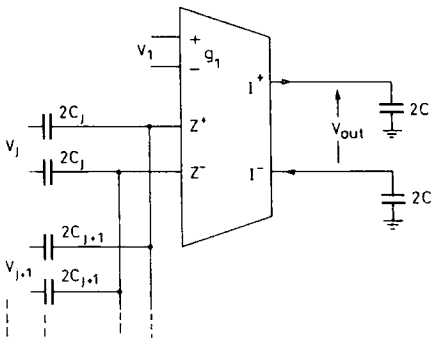

Fig. 7 *First-order section using transconductor with low-impedance inputs*

The output current of the transconductor is the sum of the transconductance multiplied by the voltage at high-impedance input ($V+$, $V-$), and the current entering the low impedance input ($Z+$, $Z-$). The circuit diagram of a transconductor with low-impedance inputs is given in Fig. 8.

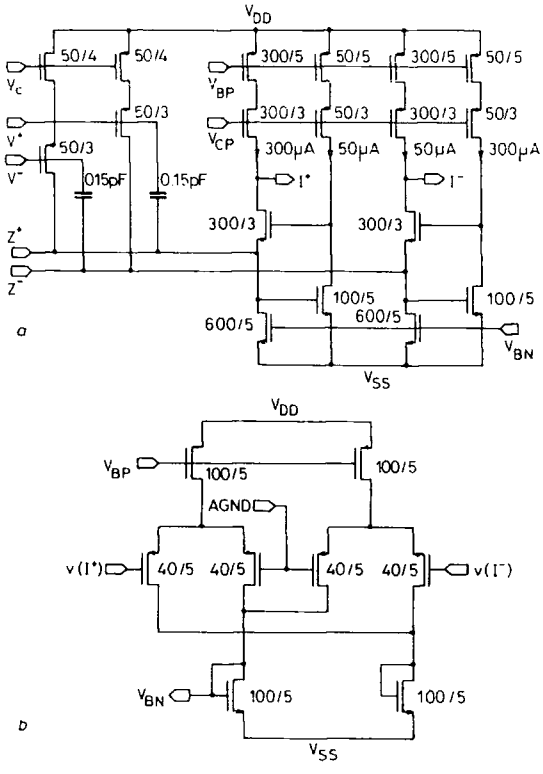

Fig. 8 *Folded cascode transconductor with low-impedance inputs (a) and common-mode feedback circuit (b)*

4 Matrix decompositions

Five ways of obtaining an active ladder from the general second-order equation (eqn. 1) are now given, together with design examples. The first is recommended for lowpass and the remaining four for bandpass responses. For clarity, single-ended ladders are shown. However, practical transconductor circuits (including those presented in Section 5) are normally fully differential, for several reasons: to obtain linear transconductance functions, to allow the realisation of negative floating capacitors, and to maximise power supply rejection.

In each decomposition, a scaling factor (g or ω_o) is introduced in the definition of the vector X. This factor may be used to perform nodal voltage scaling between the X and V voltages in the transconductor ladder. The scaling of the voltages within each of X and V is determined by the design of the passive prototype. This may also be optimised by matrix techniques, as shown on pages 127–128 of Reference 18.

4.1 Topological decomposition

The Γ matrix is factorised as

$$\Gamma = ADA^T \tag{6}$$

where D is a diagonal matrix whose elements are the reciprocals of the inductances in the prototype (assuming a V-representation), and A is a conventional incidence matrix. The auxiliary variables are defined by

$$X = (sg)^{-1}DA^TV \tag{7}$$

where g is a scaling factor with the dimensions of conductance, Eqns. 6 and 7 are substituted into eqn. 1 to obtain

$$CV = s^{-1}[J - GV - gAX] \tag{8}$$

Substituting the matrices (eqn. 2*a–e*) into the design eqns. 7 and 8, and implementing each row with a conventional transconductor stage (Fig. 5) gives the active filter shown in Fig. 9, which is equivalent to a standard leapfrog

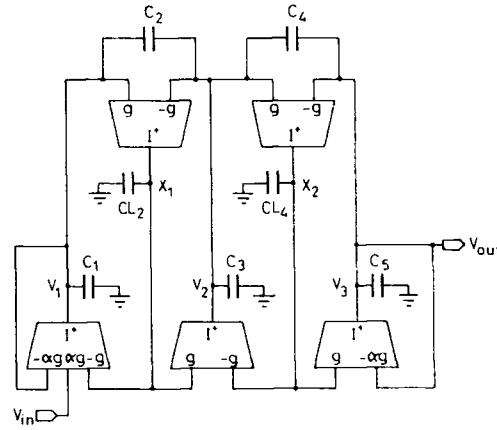

Fig. 9 *Lowpass elliptic ladder using conventional transconductor*

ladder. Using transconductors with low-impedance inputs instead, we obtain the circuit shown in Fig. 10. The advantage of the first realisation is that there are fewer capacitors and the transconductors are simpler. The advantage of the second is that bottom plates of the floating capacitors can be connected to the low-impedance inputs, so the associated parasitic capacitances do not need to be estimated and subtracted from the grounded capacitors [4].

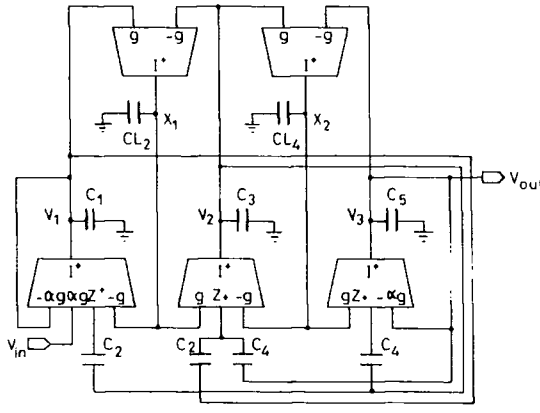

Fig. 10 *Lowpass elliptic ladder using transconductor with low-impedance inputs*

This topological decomposition is most applicable to lowpass ladders. It is less satisfactory for highly selective bandpass filters, in which case nodal voltage scaling forces high-transconductance ratios, and it cannot be applied to prototypes containing inductor loops as the resulting active circuits are unstable. For bandpass ladders, the following four decompositions are proposed.

4.2 Left-inverse decomposition type 1 (LID1)

The auxiliary variables are defined by

$$gX = sCV \tag{9}$$

where g is again a scaling factor with the dimensions of conductance, and eqn. 9 is substituted into eqn. 1, giving

$$gX = J - GV - s^{-1}\Gamma V \tag{10}$$

The LID1 design equations are obtained by rearranging eqn. 9 and multiplying eqn. 10 by the inverse of Γ:

$$g^{-1}CV = s^{-1}X \tag{11}$$

$$g\Gamma^{-1}X = -s^{-1}V + \Gamma^{-1}[J - GV] \tag{12}$$

From eqns. 11 and 12, the main features of LID1 can be deduced. First, both integrated terms (i.e. those containing the factor s^{-1}) are vectors, so only a single value of transconductance is required in the active ladder. Secondly, both nonintegrated terms on the right-hand side of eqn. 12 are generally asymmetric, so they must be realised using unidirectional capacitive coupling paths. In other words, the dependence of V upon X is not the same as the dependence of X upon V in these terms, so each branch must be realised by a separate capacitor, rather than symmetric branches being realised by a single capacitor connected between the nodes concerned. A single capacitor can be used for symmetric nonintegrated branches arising from off-diagonal terms on the left-hand sides of eqns. 11 and 12, as long as first-order sections with high-impedance outputs are used.

Fig. 11 shows the LID1 realisation of the sixth-order elliptic prototype of Fig. 2. This was obtained by substituting the V-representation matrices, (eqn. 3*a–e*), into eqns. 11 and 12 and translating each row of each equation into a first-order section of the type shown in Fig. 7.

A general feature of inverse matrix decompositions is that the number of components and the density of interconnect may be high in the transconductor ladder if the sparsity of Γ (or C) is lost upon inversion. This is not a serious problem for the sixth-order elliptic ladder of Fig. 11, but for higher-order filters care should be taken with the choice of prototype. Essentially this means placing capacitors such that long chains of directly connected inductors are avoided. Some passive prototypes also exist whose Γ matrix may not be inverted at all, due to the determinant being zero. The only examples of such filters known to the authors are bandstop. A question yet to be investigated is to what extent an inverse matrix filter preserves the low-passband sensitivity properties of its passive ladder prototype.

4.3 Left-inverse decomposition type 2 (LID2)

The auxiliary variables are defined by

$$\omega_0 X = sV \tag{13}$$

where ω_0 is a scaling factor with the dimensions of angular frequency, and eqn. 13 is substituted into eqn. 1, giving

$$\omega_0 CX = J - GV - s^{-1}\Gamma V \tag{14}$$

Rearranging eqn. 13 and multiplying eqn. 14 by Γ^{-1} gives the LID2 design equations

$$\omega_0\Gamma^{-1}CX = \Gamma^{-1}J - \Gamma^{-1}GV - s^{-1}V \tag{15}$$

and

$$V = \omega_0 s^{-1}X \tag{16}$$

As in the other left-inverse decomposition, only one value of transconductance is required, together with unidirectional nonintegrated paths. The distinguishing feature of LID2 is the term $\Gamma^{-1}C$, which gives the opportunity to obtain a relatively sparse transconductor ladder is a prototype can be used for which $\Gamma = C$. As shown in Section 2, this condition is satisfied for a symmetric bandpass filter derived by the transformation of each component of a lowpass ladder individually. Fig. 12 shows the sixth-order bandpass elliptic transconductor ladder obtained by substituting eqns. 4*a–e* into eqns. 15

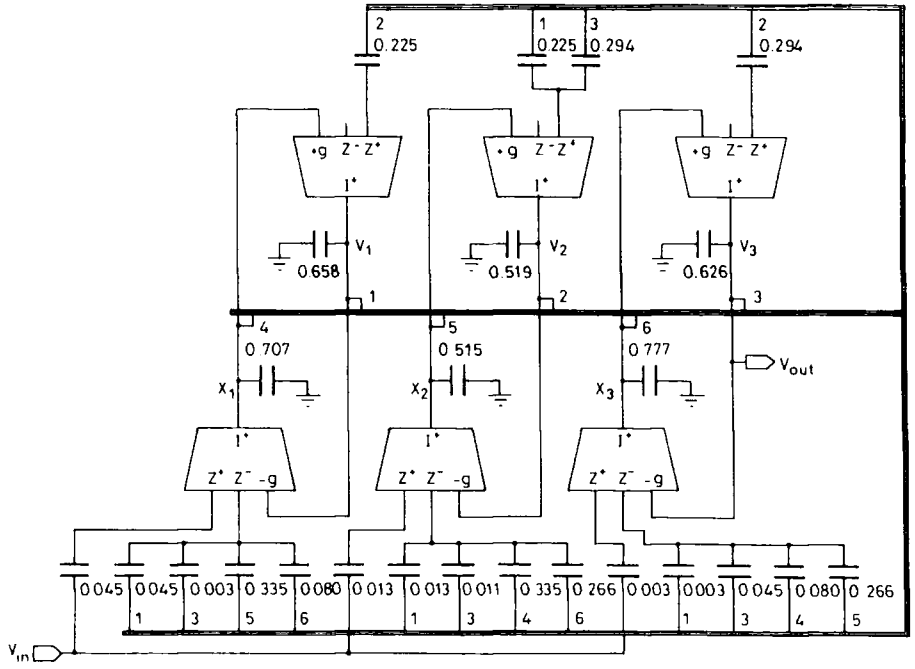

Fig. 11 *Elliptic bandpass ladder obtained by LI decomposition type 1*

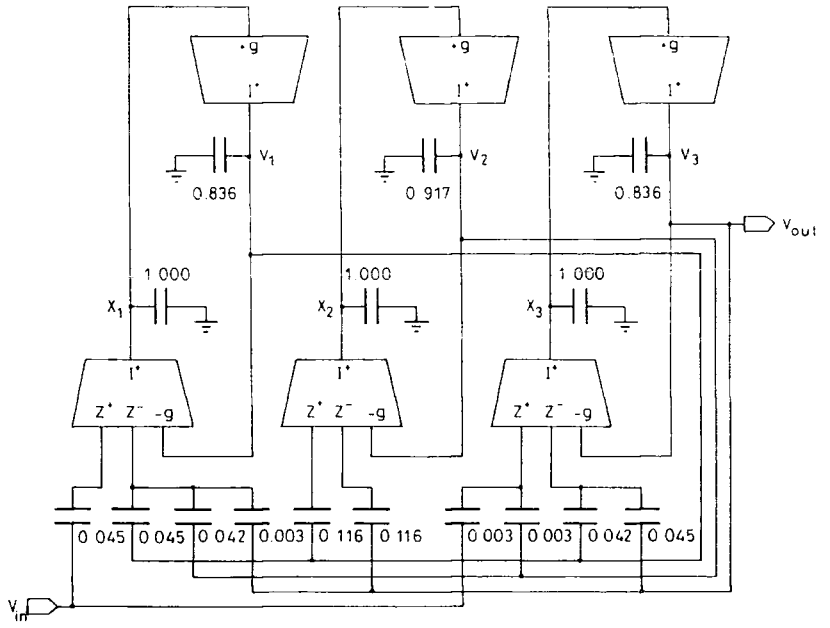

Fig. 12 *Elliptic bandpass ladder obtained by LI decomposition type 2*

and 16 and implementing each row of each design equation with the first-order section of Fig. 7.

4.4 Right-inverse decomposition (RID)

For the RID, X is defined by

$$gX = s^{-1}\Gamma V \tag{17}$$

This is substituted into eqn. 1 to give

$$J = (G + sC)V + gX \tag{18}$$

The design equations are obtained by multiplying eqn. 17 by Γ^{-1} and rearranging eqn. 18:

$$g\Gamma^{-1}X = s^{-1}V \tag{19}$$

$$g^{-1}CV = s^{-1}[g^{-1}(J - GV) - X] \tag{20}$$

Conventional transconductors can be used to implement eqns. 19 and 20 because the only nonintegrated terms are those arising from the offdiagonal elements of Γ^{-1} and C, which represent bidirectional coupling paths. Neither V nor X is premultiplied before integration, so no unrealisable summing coefficients are introduced. To scale the filter correctly for dynamic range, a second (smaller) value of transconductance is usually required to realise the input branch and filter terminations. This use of a second transconductance value is acceptable because it can be chosen to be in integer ratio to the first and it is used only to represent the termination resistors which are the least sensitive components of the prototype. Such a realisation compares favourably with a coupled-biquad ladder in which high and/or noninteger transconductor ratios can occur throughout the filter.

Fig. 13 shows the RID transconductor ladder obtained from the sixth-order elliptic prototype of Fig. 2, using the V-representation.

4.5 Left-direct decomposition (LD)

The vector of auxiliary variables X is defined by

$$gX = sCV \tag{21}$$

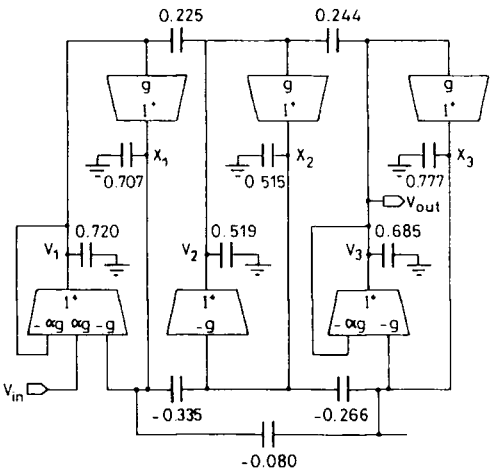

Fig. 13 *Elliptic bandpass ladder obtained by RI decomposition*

Eqn. 21 is substituted into eqn. 1 to give

$$J = GV + gX + s^{-1}\Gamma V \tag{22}$$

and the design equations are obtained by rearranging eqns. 21 and 22:

$$CV = s^{-1}gX \tag{23}$$

$$X = -(sg)^{-1}\Gamma V - g^{-1}GV + g^{-1}J \tag{24}$$

The principal features of the LD decomposition are as follows. First, the matrix Γ should be diagonal to avoid the requirement for summing integrators which would imply the use of randomly ratioed transconductor values. Secondly, the damping and coupling branches (as represented by the term $g^{-1}GV$) are nonintegrated. These branches are unidirectional, as they describe a dependence of X upon V which is not matched by an identical dependence on V upon X. Therefore, transconductors with low-impedance inputs (Fig. 7) or opamp-based integrators (Fig. 6) must be used in a left-direct filter.

Fig. 14 shows the LD ladder obtained from the sixth-order asymmetric Chebyshev prototype of Fig. 3, using the V-representation. Transconductors with low-impedance inputs are used only for the termination capacitors.

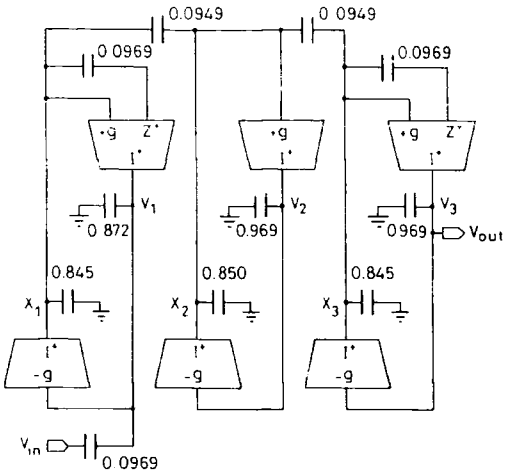

Fig. 14 *Chebyshev bandpass ladder obtained by LD decomposition*

Left- and right-decomposition filters employ capacitive and resistive damping, respectively, hence we can refer to them as 'E-type' and 'F-type' circuits by analogy with the terminations and terminology used for SC biquads [24].

5 Experimental results

To verify the methods described above, a set of high-frequency transconductor ladder filters has been designed and fabricated on a 1 μm double-poly double-metal CMOS process. In this Section, results are given from three filters: one lowpass elliptic, one bandpass elliptic, and one bandpass Chebyshev. Each of the bandpass filters includes a phase-lock frequency-control loop, a description of which is also given here. The operating frequencies and selectivities of these filters are not high enough for amplitude-control loops [3] to be required.

5.1 Elliptic lowpass filter

Fig. 15 shows the schematic of the experimental lowpass filter, which is a fully differential version of the filter shown in Fig. 9, scaled to a cutoff frequency of 1 MHz. Table 1 summarises the specification and measured performance. Fig. 16 shows the measured amplitude response.

The circuit diagram and a photomicrograph of the double-input transconductor used are shown in Figs. 17 and 18. The compact layout is achieved by dividing the larger transistors into units 100 μm wide so that the transistors of each polarity can be assembled in rectangular areas, supplied by the respective power lines. Between the two sets of transistors lies a routing bus, which occupies area that would have to be used anyway due to the relatively large 'p-well to n+ diffusion' design rule. The input and output ports run over the VDD line (to the right in the photograph). Including the bias lines in the central bus enables the transconductors to be butted directly. A photomicrograph of the complete lowpass filter is given in Fig. 19. The transconductors are laid out in a single row, and the capacitor bank (with units of 0.5 pF) is shaped to have approximately the same length. Another bus is used to provide efficient routing between the transconductors and capacitors.

Table 1: Specification and measured performance of lowpass filter

Parameter	Designed	Measured
Order	5	
Cutoff frequency	1 MHz	
Tuning range of cutoff freq.		250 kHz–1.2 MHz
Passband ripple	0.28 dB	0.4 dB
Stopband attenuation	60 dB	61.5 dB
Noise density in passband		97 nV/$\sqrt{}$Hz
THD (200 mV rms input)		−67.7 dB
Common mode rejection		71 dB
Power supply rejection		43 dB
Current consumption		10 mA

5.2 Elliptic bandpass filter

Fig. 20 shows the schematic of the experimental elliptic bandpass filter, which is a fully differential version of the filter shown in Fig. 13, scaled to a centre frequency of 400 kHz. Table 2 summarises the specification and measured performance. Fig. 21 shows the measured amplitude response. A photomicrograph is given in Fig. 22. The noise spike in the stopband at 1.9 MHz is breakthrough from the control loop used to set the centre frequency automatically with respect to a reference clock (see below).

Table 2: Specification and measured performance of elliptic bandpass filter

Parameter	Designed	Measured
Order	6	
Centre frequency	400 kHz	
Tuning range of centre freq.		100 kHz–525 kHz
Bandwidth	10%	10%
Stopband attenuation	50 dB	49.5 dB
Noise density in passband		920 nV/$\sqrt{}$Hz
Intermodulation distortion		−43.8 dB
Common mode rejection		72 dB
Power supply rejection		40 dB
Current consumption		11.3 mA

5.3 Chebyshev bandpass filter

Fig. 23 shows the schematic of the experimental Chebyshev bandpass filter. This is a fully differential version of the left-direct filter shown in Fig. 14, scaled to a centre frequency of 400 kHz. To the knowledge of the authors, it is the first example of a transconductor ladder filter that is capacitively terminated and has only a single value of transconductance (100 μS). Table 3 summarises the specification and measured performance. Fig. 24 shows the measured amplitude response. A photomicrograph is given in Fig. 25.

Table 3: Specification and measured performance of Chebyshev bandpass filter

Parameter	Designed	Measured
Order	6	
Centre frequency	400 kHz	
Tuning range of centre freq.		100 kHz–550 kHz
Bandwidth	10%	10%
Noise density in passband		920 nV/$\sqrt{}$Hz
Ref. signal breakthrough		200 μV
Intermodulation distortion		−48.7 dB
Common mode rejection		72 dB
Power supply rejection		46 dB
Current consumption		11.6 mA

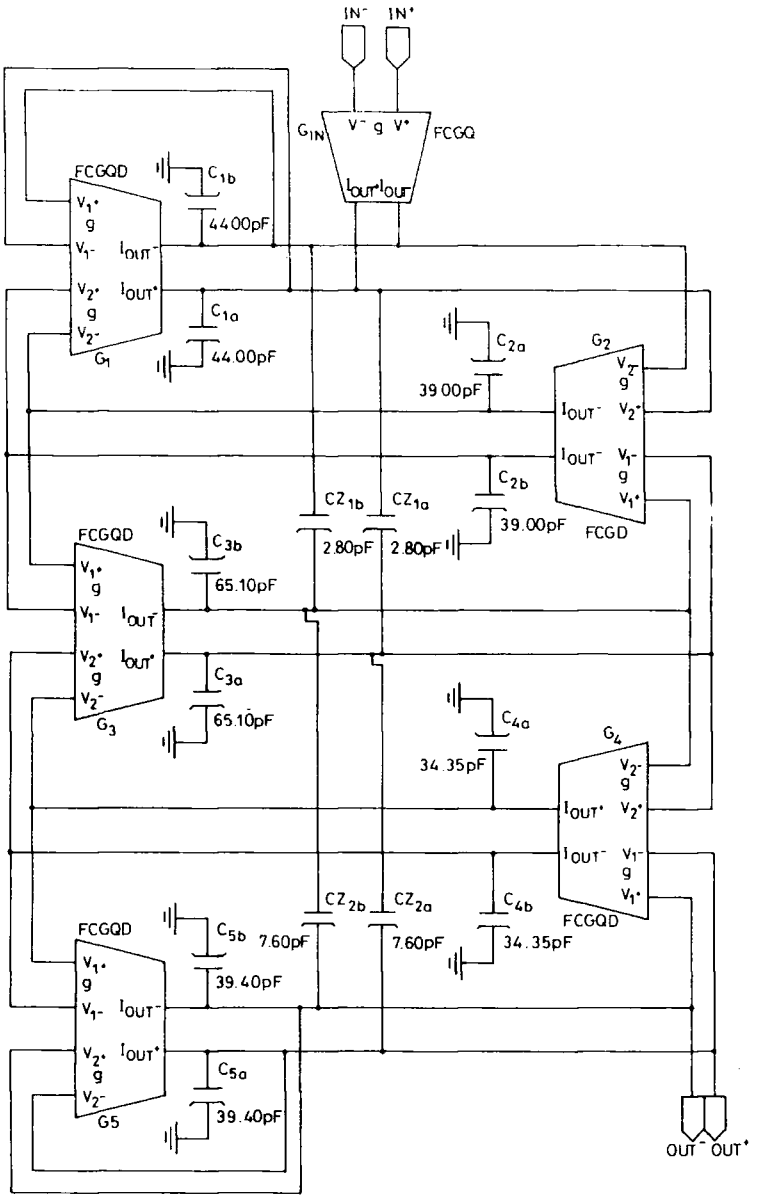

Fig. 15 *Fully differential lowpass transconductor ladder filter (bias lines omitted)*

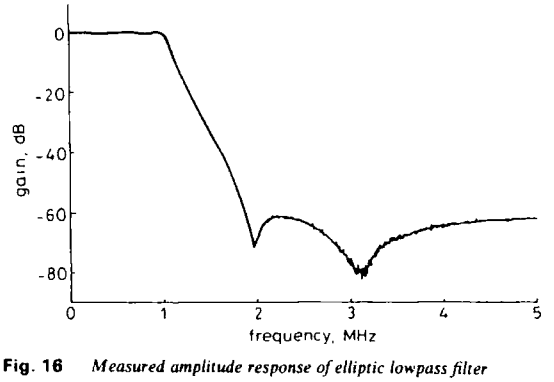

Fig. 16 *Measured amplitude response of elliptic lowpass filter*

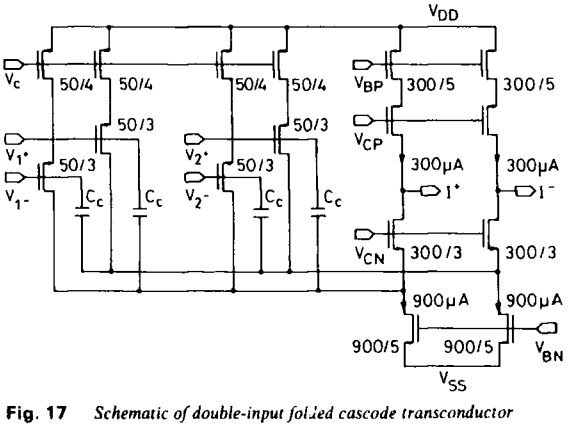

Fig. 17 *Schematic of double-input folded cascode transconductor*

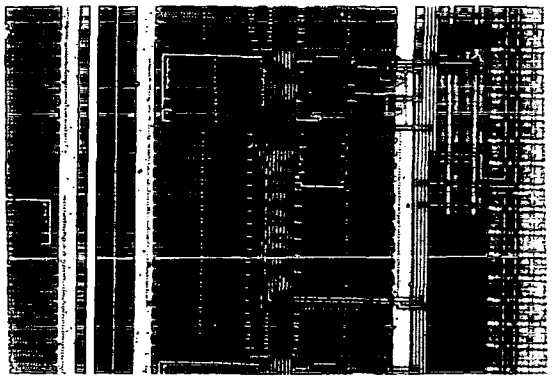

Fig. 18 *Photomicrograph of double-input folded cascode transconductor*

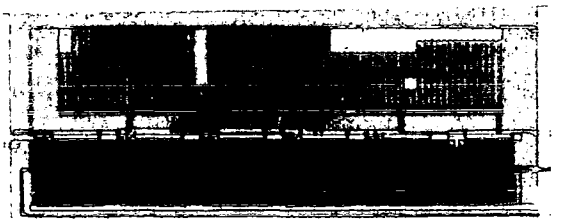

Fig. 19 *Photomicrograph of elliptic lowpass filter*

5.4 Frequency-control loop

The frequency-control loop fabricated with the test filters is a phase-lock loop (Fig. 26). Based on a voltage-controlled oscillator. This is similar in principle to those described in References 9 and 22, the main difference being that here a triangle-wave oscillator is used instead of a harmonic oscillator.

The triangle-wave oscillator is illustrated in Fig. 27. An analogue switch selects either $+\Delta V$ or $-\Delta V$ as the input to the transconductor and, respectively, $+\Delta V/2$ or $-\Delta V/2$ as one of the inputs of the comparator. If $+\Delta V$ is selected, the voltage across the capacitor will slew up linearly at a rate $(\Delta V g/C)$. When this voltage exceeds $\Delta V/2$, the comparator changes state so that the output of the analogue switch changes to $-\Delta V$. Then the output of the transconductor slews down until its value reaches $-\Delta V/2$ and the comparator changes state again. In each

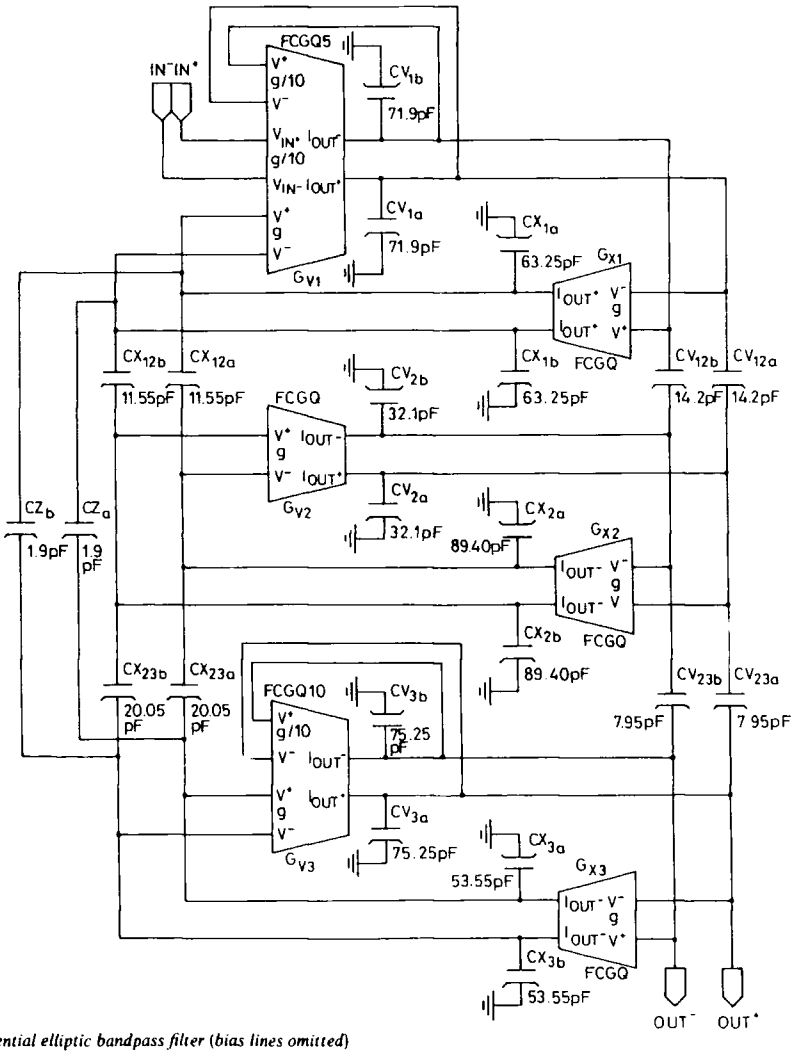

Fig. 20 *Fully differential elliptic bandpass filter (bias lines omitted)*

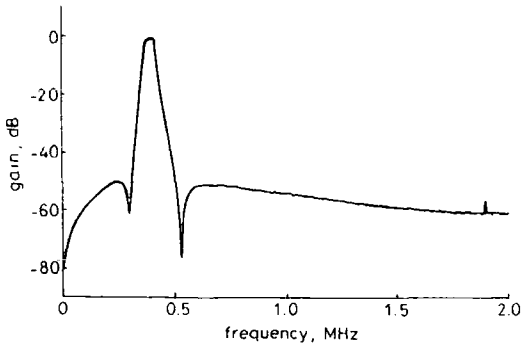

Fig. 21 *Measured amplitude response of elliptic bandpass filter*

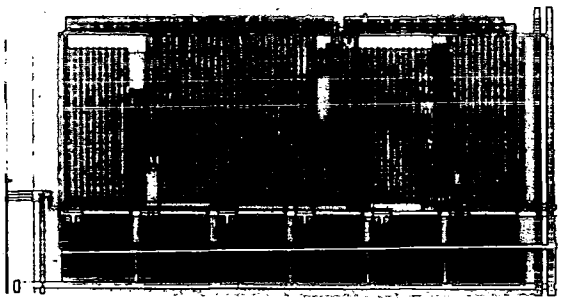

Fig. 22 *Photomicrograph of elliptic bandpass filter*

period, the transconductor output has to slew twice through a range of magnitude ΔV, so the frequency of oscillation is

$$f_{osc} = \frac{\Delta V g/C}{2\Delta V} = \frac{g}{2C} \tag{25}$$

The output of the comparator is, of course, a square wave at the same frequency.

The phase of the VCO output is compared to that of a reference square-wave clock by an XOR gate followed by a single-order lowpass filter. The result of the phase comparison is used as the control voltage for the transconductor in the VCO. When the PLL reaches lock, the

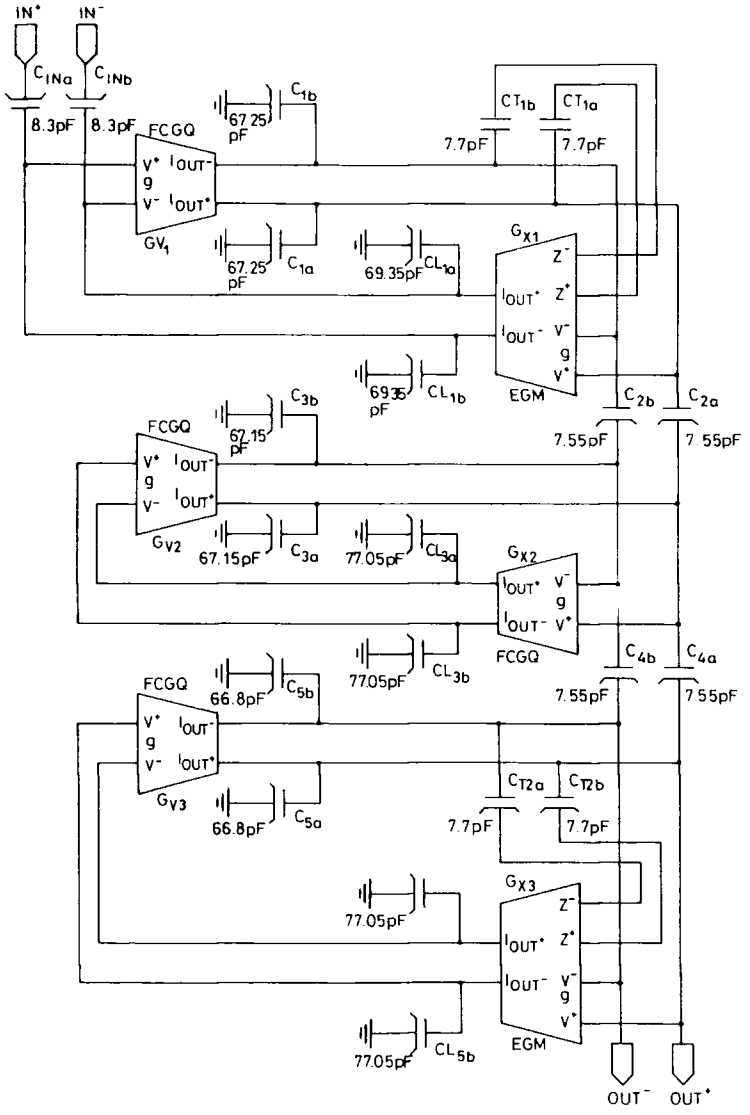

Fig. 23 *Fully differential Chebyshev bandpass filter (bias lines omitted)*

reference and VCO frequencies are identical, and so according to eqn. 25 the time constant of the transconductor and capacitor in the VCO are set. The same control voltage is used for each transconductor in the 'slave' filter. Therefore, within the accuracy of transconductor and capacitor matching, the frequency response of the filter is scaled with respect to the reference clock.

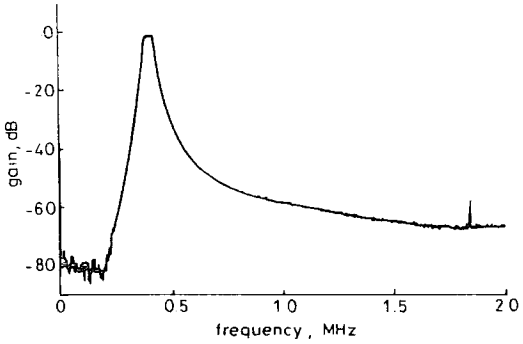

Fig. 24 *Measured amplitude response of Chebyshev bandpass filter*

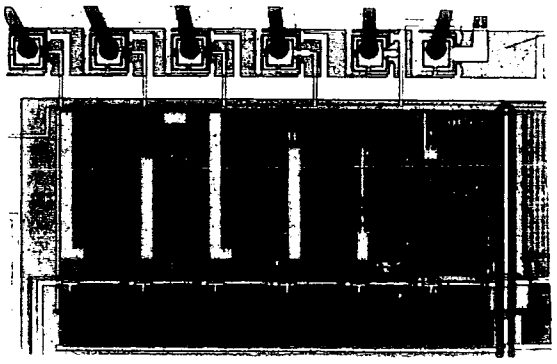

Fig. 25 *Photomicrograph of Chebyshev bandpass filter*

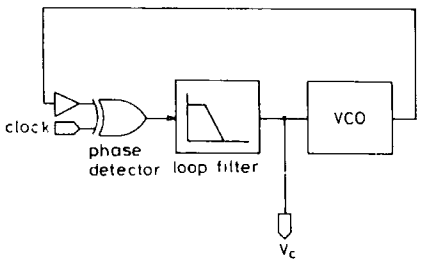

Fig. 26 *PLL control loop*

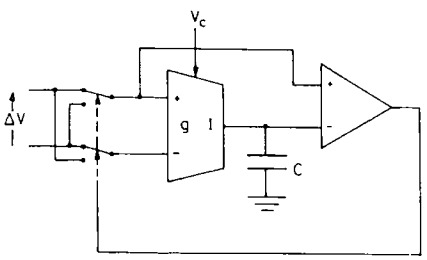

Fig. 27 *Triangle-wave voltage-controlled oscillator*

The operation of the control loop is illustrated in Fig. 28 which shows the measured amplitude response of the elliptic bandpass filter for three different values of clock frequency (865 kHz, 965 kHz and 1.065 MHz).

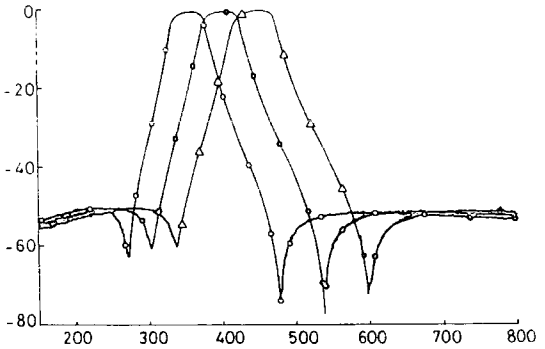

Fig. 28 *Measured elliptic bandpass filter response for three values of reference clock frequency*

□ 865 kHz
⊟ 965 kHz
◇ 1.065 MHz

6 Conclusions

A matrix-based methodology for the design of transconductor ladder filters has been presented. Many alternative design routes are possible, depending upon: how

Table 4: Comparison of different representations of RLC prototype

Name	Variables of prototype used	Comments
V	voltages	Best for a 'minimum inductance' prototype containing only parallel LC pairs
VI	voltages and currents	Best when prototype contains both parallel and series LC pairs
I	currents	Best for a 'minimum capacitance' prototype containing only series LC pairs

Table 5: Comparison of different decompositions of second-order matrix equation

Name (acronym)	Defining equations	Comments
Topological (TD)	7, 8	Most applicable to lowpass filters. When conventional transconductors are used, gives standard leapfrog filters
Left-inverse type 1 (LID1)	11, 12	Applicable to any bandpass filter. Only one value of transconductance needed per filter. Requires transconductor stages with unidirectional nonintegrating paths
Left-inverse type 2 (LID2)	15, 16	Similar to LID1, but gives sparser active circuit if a prototype is used, for which the condition $\Gamma = C$ is satisfied
Right-inverse (RID)	19, 20	Applicable to any bandpass filter. Conventional transconductors may be used, with up to two values required
Left-direct (LD)	23, 24	Applicable to all-pole bandpass filters. Only one value of transconductance needed per filter. Requires transconductor stages with unidirectional nonintegrating paths

Table 6: Comparison of different first-order transconductor stages

Active circuit used	Comments
Conventional transconductor (Fig. 5)	Best for VHF, due to simplicity. Unidirectional nonintegrating paths are not available. Parasitic input and output capacitance must be compensated for.
Opamp plus conventional transconductor or MOSFET 'resistor' (Fig. 6)	Parasitic capacitance does not affect filter, to first order. Presence of low-impedance nodes makes unidirectional paths available. Opamp dominant pole must be much higher in frequency than filter poles
Transconductor with low-impedance inputs (Fig. 7)	Combines good high-frequency performance of conventional transconductor with usefulness of unidirectional paths. But parasitic capacitances have first-order effect

the prototype ladder is represented by a second-order matrix equation, the way this equation may be decomposed into first-order equations, and the type of transconductor stage that is used to realise the first-order equation. The choices available and their relative merits are summarised in Tables 4 to 6. The utility of the techniques described is demonstrated by results from three high-frequency CMOS transconductor ladder filters.

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A COMPARISON STUDY OF SC BIQUADS IN THE REALISATION OF SC FILTERS

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ABSTRACT

A comparison for SC filter realisation based on different biquads is given. The total capacitance, capacitance spread, sensitivity, non-idealities and dynamic range of the designed filters are presented. Some conclusions are obtained as very useful guidelines for the choice of a suitable biquad structure according to the nature of the filter problem.

1. INTRODUCTION

During the past decade several SC biquads have been reported and used in practical applications. Most of the biquads proposed have been analysed individually and the investigations have been based on the characteristics of the biquad itself. However the various filters proposed are intended for different applications, frequency ranges, sensitivity requirements, dynamic range etc., therefore it is difficult to judge the suitability of the biquads. By using XFILT filter compiler[1], a systematic comparison for the realisation of SC filters using most popular SC biquads is given in this paper based on filter system realisation. Although the software has the facility to design a SC system with combined biquads, we restrict our comparison here to systems only composed of one kind of SC biquad, in order to simplify the question and make the guidelines of selecting SC biquads more practical for the SC filter designer who does not have an SC filter compiler or only a compiler with limited biquad structures.

2. BIQUAD CONFIGURATIONS

The biquads that we adopt here are:
Type-E:Fleischer and Laker's E-type biquad in [2].
Type-F:Fleischer and Laker's F-type biquad in [2].
FGL Type: Modified Fleischer and Laker's biquads[3].
G-T Type: Gregorian and Temes's biquad presented in [4].
M-S Type: Martin and Sedra's biquad in [5].
SSGI Type and SSGII Type: Sanchez-Sinencio, Silva-Martinez and Geiger's type-I and type-II biquads in [6].
Nagaraj type: Nagaraj's biquad proposed in [7].

3. FILTER REALISATION COMPARISON

a) Lowpass Filter : A 6th-order elliptic filter response is shown in Fig.1(a). The Table 1 shows the realisation statistics of different biquad cascades.

	No. C	Total C	C Spread
Type E	22	144.27	45.85
Type F	22	130.49	44.58
LGF	21	181.10	43.91
SSGI	27	170.87	21.96
SSGII	27	170.87	21.96
G-T	21	145.09	43.91
M-S	21	151.39	43.91
Nagaraj	27	199.25	43.91

Table 1. 6th-order lowpass filter realisation

b) Wide bandpass filter: The filter frequency response is given in Fig.1(b). The design results are given in Table 2.

	No. C	Total C	C Spread
Type E	22	315.90	78.49
Type F	22	706.13	191.48
LGF Type	21	329.02	95.09
SSGI	27	351.27	94.78
SSGII	27	351.27	94.78
G-T	21	329.02	95.09
M-S	21	328.95	95.16
Nagaraj	27	213.24	47.11

Table 2. Bandpass filter design results

c) Narrow bandpass filter: The filter response is given in Fig.1(c) and Table 3 shows design results.

	No. C	Total C	C Spread
Type E	20	1150.40	333.81
Type F	20	1112.97	332.04
LGF Type	20	1126.48	337.18
SSGI	25	1235.07	168.60
SSGII	25	1152.21	168.59
G-T	20	1126.48	337.18
M-S	20	1126.40	337.20
Nagaraj	27	5795.65	1050.51

Table 3. Narrow band bandpass filter design results

d) Highpass Filter: The highpass filter frequency response is given in Fig.1(d) and Table 4 gives the design results..

	No. C	Total C	C Spread
Type E	18	538.77	156.35
Type F	18	318.89	62.88
LGF Type	18	484.69	137.61
SSGI	23	366.23	66.53
SSGII	23	366.23	66.53
G-T	17	522.23	123.55
M-S	17	458.29	135.93
Nagaraj	21	158.32	27.58

Table 4. 4th-order highpass filter realisation

e) Bandstop Filter: The bandstop filter response is shown in Fig.1(e) and the design results are given in Table 5.

	No. C	Total C	C Spread
Type E	29	220.97	29.24
Type F	29	1309.69	361.34
LGF Type	28	219.72	33.18
SSGI	36	259.41	25.45
SSGII	36	259.41	25.45
G-T	28	555.12	107.12
M-S	28	213.04	22.88
Nagaraj	36	142.55	22.66

Table 5. 8th-order Elliptic bandstop filter realisation

4. SENSITIVITY AND DYNAMIC RANGE COMPARISON

The following indices are used as global measures of system sensitivity $S(\omega)$ and dynamic range $D(\omega)$, respectively

$$S(\omega) = 8.686\left\{\sum_i\left[\frac{c_i}{|H(\omega)|}\frac{\partial|H(\omega)|}{c_i}\right]^2\right\}^{1/2} /100.0$$

$$D(\omega) = \frac{1}{M}\sum_M 20\log|H_M(\omega)|$$

where C_i and $|H_m(\omega)|$ are the sets of capacitances and opamp output voltages, respectively, and M is the number of opamps. $S(\omega)$ should be as small as possible. $D(\omega)$ is related to SC filter dynamic range. It is hoped that the dynamic index curve $D(\omega)$ is as flat as possible and as close to zero or a fixed gain as possible in passband. Because of the similarity of some biquads, the total sensitivity index curves are sometimes very close to each other. Fig.2(a)-(e) gives the comparison of sensitivities of the five designs and the comparisons of the dynamic index curves are given in Fig.3(a)-(e).

5. FINITE GB AND SWITCH RESISTANCE EFFECT COMPARISON

The non-idealities of SC circuits is simulated by non-ideal SC analysis software SCNAP4[8]. For the comparison, we choose the opamp with 2MHz GB, switch on resistance of $1k\Omega$, and switch off resistance of $1M\Omega$. Fig.4(a)-(e) show the non-ideal circuit response of the designed circuits.

6. CONCLUSION

Nagaraj's biquad has significant advantages for wide bandpass, bandstop, and highpass filter designs in total capacitance and capacitance spread. It also has very good dynamic range performance, but with comparatively large non-ideality effect and slightly high sensitivity compared to other biquad realisations. Therefore the compensated structure is critical in cascading Nagaraj biquad realisation[9].

SSGI and SSGII biquads have very good dynamic range performance and they are best candidates for narrow band filters in total capacitance and capacitance spread. They also give best capacitance spreads in lowpass filter realisations. However, SSGI and SSGII structures usually have slightly high sensitivity to component change.

G-T biquad has lowest sensitivity and small non-ideal effect in the filter realisation.

Generally, type-E, LGF, M-S, and G-T structures have similar total capacitance and capacitance spread, except in bandstop, where G-T biquad needs large total capacitance and capacitance spread. They also have lower sensitivity and good dynamic range, and small non-ideal effect.

Type-F biquad is good in total capacitance and capacitance spread in highpass case, but poor in wide bandpass, and bandstop cases. It has fairly good sensitivity performance and dynamic range, and small non-ideal effect.

ACKNOWLEDGEMENT

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Fig.1(a) Lowpass Filter Response

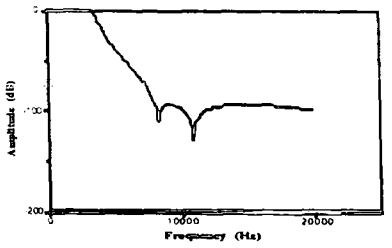


Fig.1(b) Wide Bandpass Filter Response

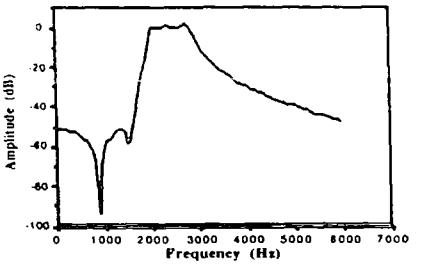


Fig.1(c) Narrow Bandpass Filter Response

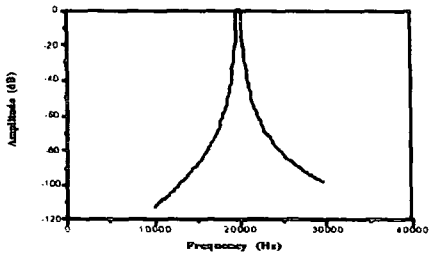


Fig.1(d) Highpass Filter Response

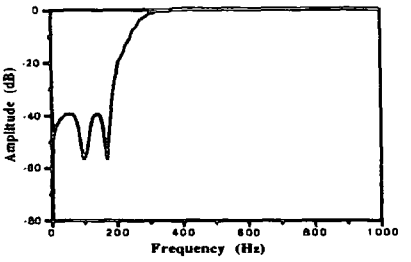


Fig.1(e) Bandstop Filter Response

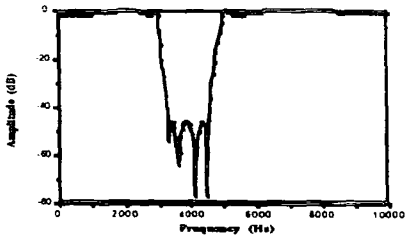


Fig.2(a) Comparison of Lowpass Filter Sensitivities

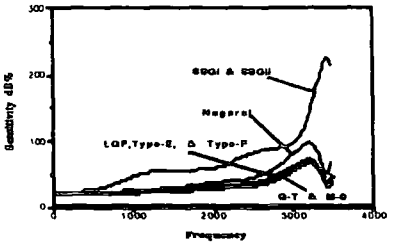


Fig.2(b)Comparison of Wide Bandpass Filter Sensitivities

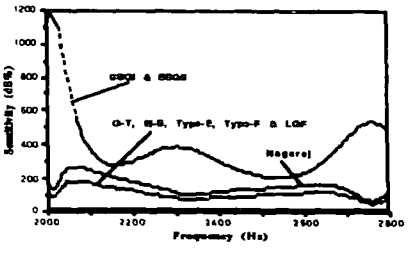


Fig.2(c) Comparison of Narrow Bandpass Filter Sensitivities

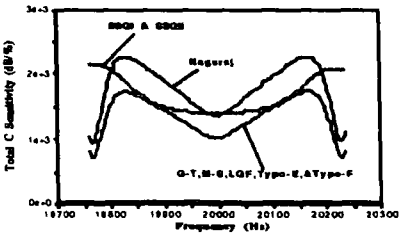


Fig.2(d) Comparison of Highpass Filter Sensitivities

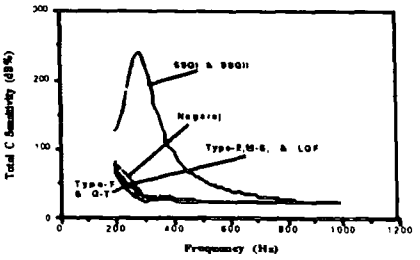


Fig.2(e) Comparison of Bandstop Filter Sensitivities

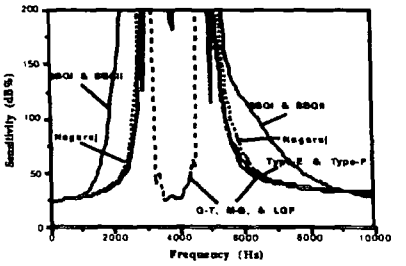


Fig.3(a) Dynamic Range Index of Lowpass Filter

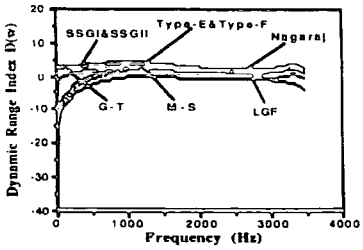


Fig.3(b) Dynamic Range Index of Wide Bandpass Filter

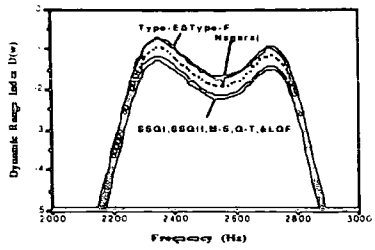


Fig.3(c) Dynamic Range Index of Narrow Bandpass

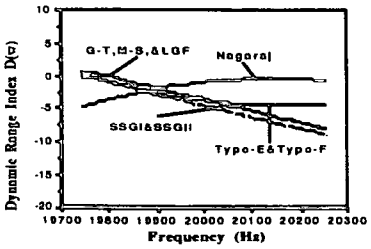


Fig.3(d) Dynamic Range Index of Highpass Filter

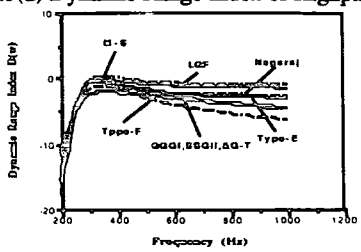


Fig.3(e) Dynamic Range Index of Bandstop Filter

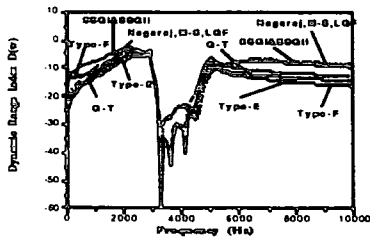


Fig.4(a) Non-ideal Response of Lowpass Filter

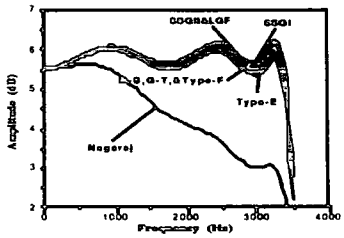


Fig.4(b)Non-ideal Response of Wide Bandpass Filter

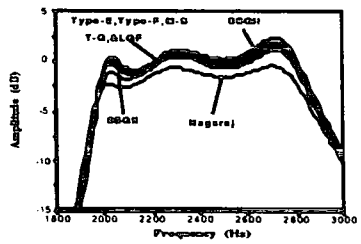


Fig.4(c) Non-ideal Response of Narrow Bandpass Filter

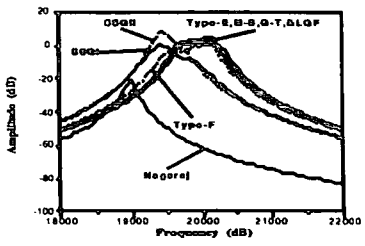


Fig.4(d) Non-ideal Response of Highpass Filter

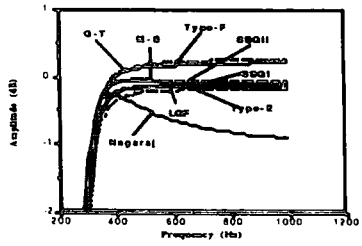
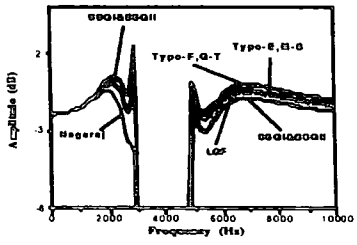


Fig.4(e) Non-ideal Response of Bandstop Filter



5. Network Analysis and CAD

PAPER 1

Table 1

APPROXIMATE GAIN-PRODUCT SENSITIVITIES

I.N.I.C.	S_K
I.0	$-\frac{4}{K}$

E.N.I.C.	S_K
E.0	$-\frac{2}{K}$

I.N.I.C.	S_{a1}	S_{a2}
I.1	$-\frac{4(1-a_2)}{a_1a_2}$	$-\frac{2}{a_1a_2}$
I.2	$\frac{4(1-a_2)}{a_1}$	$\frac{2a_2}{a_1}$
I.3	-2	$-\frac{2}{a_1}$

E.N.I.C.	S_{a1}	S_{a2}
E.1	$\frac{2(1-a_2)}{a_1}$	$\frac{1}{a_1}$
E.2	$-\frac{2(1-a_2)}{a_1a_2}$	$-\frac{1}{a_1}$
E.3	$-\frac{1}{a_2}$	$-\frac{1}{a_1}$

The approximate gain-product sensitivities of all four e.n.i.c. circuits are listed in Table 1, alongside those for the respective dual i.n.i.c. circuits. The factor-of-two enhancement in sensitivities of the circuits in the e.n.i.c. subclass compared with those in the i.n.i.c. subclass prevails throughout.

Finally, it might be noted from Table 1 that, if stabilisation and improvement in sensitivity performance is to be effected by use of Darlington-compounded transistors (as in Fig. 3*c*), it suffices to do this only for transistor T_2 in each circuit, whether i.n.i.c. or e.n.i.c., because the factor $1 - a_2$ appears in four cases, whereas the factor $1 - a_1$ does not appear at all, these being the significant factors.[1]

'Breadboard' models of each e.n.i.c. (Fig. 4) have been built and tested in the laboratory, and found to convert satisfactorily. They have not yet been tested exhaustively for stability and drift under variable operating conditions and environment.

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21st April 1965

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1 LARKY, A. I.: 'Negative impedance converters', *IRE Trans.*, 1957, **CT-4**, p. 124
2 HAKIM, S. S.: 'Some new negative-impedance convertors', *Electronics Letters*, 1965, **1**, p. 9

TABLE FOR THE VOLTAGE TRANSFER FUNCTIONS OF SINGLE-AMPLIFIER DOUBLE-LADDER FEEDBACK SYSTEMS

This letter presents a Z/Y table from which the voltage transfer functions for multiple-loop feedback systems using one operational amplifier may be written down. The table is given, together with a recurrence formula for the voltage transfer function. Expressions are also given for the product terms arising from the table.

It is well known that the burden of tedious calculations required to find the voltage transfer functions of networks having certain regular forms may be much eased or eliminated by the use of tabular forms in which the elements are set out in a systematic array of rows and columns. One such array for the analysis of a single-ladder feedback network has been given by Aggarwal.[1]

In practice, it is often necessary to determine the voltage transfer ratio for multiple-loop feedback systems, which may be represented by the double-ladder network and single amplifier shown in Fig. 1. This problem arises frequently in the study of *RC* active filter networks.

This paper presents a Z/Y table from which the voltage transfer ratio E_2/E_1 for networks of the form of Fig. 1 may be written down on inspection.

In this letter it will be assumed that the gain M of the amplifier and its input impedance are infinite, while its output impedance is zero. Further, it is assumed that a virtual earth exists at the amplifier input (point A).

It is, of course, possible in principle to find the voltage transfer ratio by direct analysis, but this is tedious unless the value of n is small. The analysis reveals, however, that it is possible to recognise the existence of a symmetrical pattern for the network elements in the voltage transfer functions. The essence of the method resides in the recognition of this pattern and the arrangement of the elements in a suitable table, which can be interpreted in a manner to be described.

Element numbering

The series input elements are all defined as impedances and have odd suffixes; i.e. Z_i, where i is an odd integer. The feedback elements in the upper ladder are defined as admittances and have even suffixes. The elements in the lower ladder, which are connected to earth, are defined as admittances with double-suffix notation. Thus the element from point B to earth is written Y_{23}, since point B is positioned between the Y_2 admittance and the Z_3 impedance. The circuit in Fig. 1 lacks symmetry, in that the upper and lower ladders contain different numbers and arrangements of elements.

When writing the suffixes to the elements, the following procedure is suggested. Begin with the feedback elements in the upper ladder and denote these as Y_2, Y_4, Y_{2n}, where n is the order of the network. The Z elements should then be given the suffixes 1, 3, $(2n-1)$, and finally the elements connected to earth in the lower ladder should be numbered as previously explained from Y_{23} to $Y_{(2n-2)(2n-1)}$. In a particular feedback network, some of the elements shown in Fig. 1 may not be present. The general procedure should nonetheless be adopted and the missing

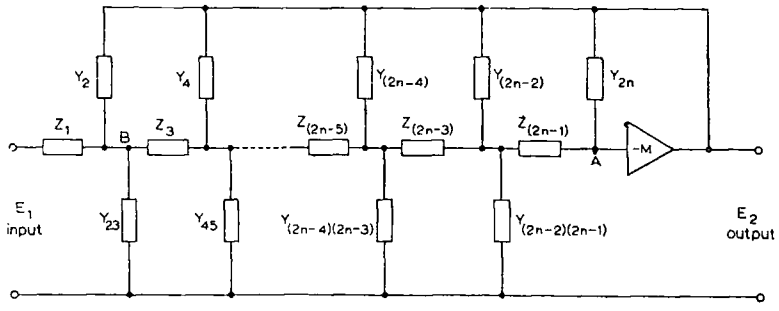

Fig. 1 *General double-ladder feedback network*

elements subsequently omitted.

Derivation of table

It is possible to derive a recurrence formula to give the voltage transfer function from which the pattern for the table can be observed.

For a complete network with the first series element denoted as Z_1 and the last feedback element as Y_f, let the transfer ratio $-E_f/E_2$ be denoted as $G(i, f)$ [i odd, f even, $i < f$; if $i > f$, $G(i, f) = 0$]. Initially assume a simple feedback system with one series input element and one feedback element. Then, extending the network towards the input three elements at a time (i.e. not disturbing the virtual earth), the expression for the current at node B (Fig. 1) is given by the following recurrence relation:

$$Z_1^{-1}[G(1, 2n) - G(3, 2n)] = Y_2 + (Y_2 + Y_{23})\,G(3, 2n) + Z_3^{-1}[G(3, 2n) - G(5, 2n)] \quad . \quad (1)$$

in which, for example, $G(5, 2n)$ is the same as $G(1, 2n-4)$ with all the suffixes increased by 4. Continuing the above expression, it becomes

$$G(1, 2n) = Z_1(Y_2 + Y_4 + \ldots + Y_{2n}) + [1 + Z_1(Y_2 + Y_{23})]\,G(3, 2n) + [Z_1(Y_4 + Y_{45})]\,G(5, 2n) + [Z_1(Y_6 + Y_{67})]\,G(7, 2n) + \ldots + [Z_1(Y_{(2n-2)} + Y_{(2n-2)(2n-1)}]\,G(2n-1, 2n) \quad . \quad (2)$$

The transfer function can now be written down by inspection.

$$G(1, 2) = Z_1 Y_2$$

$$G(1, 4) = Z_1(Y_2 + Y_4) + [1 + Z_1(Y_2 + Y_{23})]\,G(3, 4) = Z_1(Y_2 + Y_4) + [1 + Z_1(Y_2 + Y_{23})]\,Z_3 Y_4$$

$$G(1, 6) = Z_1(Y_2 + Y_4 + Y_6) + [1 + Z_1(Y_2 + Y_{23})]\,G(3, 6) + Z_1(Y_4 + Y_{45})\,G(5, 6)$$

$$= Z_1(Y_2 + Y_4 + Y_6) + [1 + Z_1(Y_2 + Y_{23})]\,\{Z_3(Y_4 + Y_6) + [1 + Z_3(Y_4 + Y_{45})] + Z_5 Y_6\} + Z_1(Y_4 + Y_{45})\,Z_5 Y_6 \quad . \quad . \quad (3)$$

The following pattern emerges for higher values of n:

There is a set of double product terms of the type ZY and a set of four component products with two factors in Z and two factors in Y etc. The last term has n factors in Z and n in Y. In Table 1 the Zs and Ys are so arranged that the voltage ratio $-(E_f/E_2)$ can very easily be obtained. The forward transfer ratio E_2/E_1 can, of course, be written down when $-(E_f/E_2)$ is known.

Use of the Table

The procedure for obtaining terms from the Table is as follows:

(a) Sets of double product terms of type ZY

Each Z_i is multiplied by the sum of the elements in the Y_f row, beginning with $Y_{(i+1)}$ up to Y_{2n}. The values of i are all odd, going from 1 to $2n-1$; i.e.

$$\sum_{i=1}^{2n-1} (Z_i \sum_{j=i+1}^{2n} Y_j) \quad . \quad . \quad . \quad . \quad . \quad (4)$$

where i is odd.

(b) Sets of four-component products in two Zs and two Ys

All Z_k and Z_l are multiplied by the sum of all the Ys between k and l and by the sum of the elements in the Y_f row between $l+1$ and $2n$; i.e.

$$\sum_{l=3}^{2n-1} \sum_{k=1}^{2n-3} \left[Z_k Z_l \sum_{j=k+1}^{l-1} (Y_j + Y_{j(j-1)}) \sum_{q=l+1}^{2n} Y_q \right] . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (5)$$

where k and l are odd.

(c) Sets of terms in three Zs and three Ys

All $Z_k Z_l Z_m$ are multiplied by (i) the sum of all Ys with suffixes between k and l, (ii) the sum of all Ys with suffixes between l and m, and (iii) the sum of Y_fs, starting at $m+1$, to $2n$. Here $k < l < m$, and all k, l and m are odd, beginning with 1, 3, 5, respectively; i.e.

$$\sum_{m=5}^{2n-1} \sum_{l=3}^{2n-3} \sum_{k=1}^{2n-5} \left[Z_k Z_l Z_m \sum_{j=k+1}^{l-1} (Y_j + Y_{j(j+1)}) \sum_{q=l+1}^{m-1} (Y_q + Y_{q(q-1)}) \sum_{r=m+1}^{2n} Y_r \right] . \quad . \quad . \quad (6)$$

(d) Sets of terms in four Zs and four Ys

Multiply $Z_k Z_l Z_m Z_p$ by (i) the sum of all Ys with suffixes between k and l, (ii) the sum of all Ys with suffixes between l and m, (iii) the sum of all Ys with suffixes between m and p, and (iv) the sum of Y_fs, starting with $p+1$, up to $2n$. Here $k < l < m < p$; all are odd.

$$\sum_{p=7}^{2n-1} \sum_{m=5}^{2n-3} \sum_{l=3}^{2n-5} \sum_{k=1}^{2n-7} \left[Z_k Z_l Z_m Z_p \sum_{j=k+1}^{l-1} (Y_j + Y_{j(j+1)}) \sum_{q=l+1}^{m-1} (Y_q + Y_{q(q+1)}) \sum_{r=m+1}^{p-1} (Y_r + Y_{r(r+1)}) \sum_{t=p+1}^{2n} Y_t \right] \quad . \quad . \quad . \quad . \quad (7)$$

The procedure is carried out until the last set for a particular value of n is reached, this having n factors in Zs and n factors in Ys. The last term has only one factor.

Concluding remarks

A general pattern has been derived for the terms which appear in the voltage transfer functions of single-amplifier multiple-loop feedback systems. The ZY table presented has been found exceedingly convenient and labour-saving when applied to feedback networks intended for use as RC active filters.

The authors have pleasure in acknowledging the interest of Prof. R. L. Russell, Professor of Electrical Engineering in the University of Newcastle upon Tyne. It is also a pleasure to acknowledge the suggestion by an IEE referee of the particular recurrence relations in eqns. 1 and 2. The financial support of the Department of Scientific and Industrial Research is also acknowledged.

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Reference

1 AGGARWAL, G. K.: 'ZY table for analysing a ladder network', *Proc. IEE*, 1964, **111**, p. 758

Table 1

ZY TABLE

	n	1	2	3	4		
Series element	Z_1	Z_1	Z_3	Z_5	Z_7		Z_{2n-1}
Upper ladder	Y_1	Y_2	Y_4	Y_6	Y_8		Y_{2n}
Lower ladder	Y_{01}	Y_{23}	Y_{45}	Y_{67}	Y_{89}	$Y_{(2n-2)(2n-1)}$	

PAPER 3

Finally, each of the following procedures may be used to generate from S other structures that also exhibit the phenomenon (2).

Procedure 1: Split any node of S in any way and insert a resistor and an inductor in parallel combination between the two halves of the node. Repeat this procedure as many times as desired on the resulting structure.

Procedure 2: Replace any resistor (inductor) of S by two resistors (inductors) in series. Connect an inductor (resistor) between the node joining the two resistors (inductors) and any other node of the structure. Repeat the procedure as many times as desired.

That Procedure 1 produces structures which exhibit phenomenon (2) follows from Theorem 7 of Lee[1]. That Procedure 2 also produces such structures follows from the observations that

1) Inequalities analogous to (7a) and (8a) can be written for the new structure.
2) The following selection for the column matrices B and C,

$$B = \begin{bmatrix} x_1 \\ -x_2 \\ x_1 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \quad \text{and} \quad C = \begin{bmatrix} x_1' \\ x_2 \\ x_1 \\ 0 \\ \vdots \\ 0 \end{bmatrix},$$

and subsequent division of (7a) by (8b), leads to a lower bound on $|s_{max}/s_{min}|$ similar to (9), the only difference being that l_1, l_2, and l_3 (r_1, r_2, and r_3) are replaced by sums of inductances (resistances) of the new structure.
3) Maximization of the bound with respect to x_1 and x_2, and subsequent minimization with respect to the l_i, again leads to (2).

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Table for the Voltage Transfer Functions of Single Amplifier Double Ladder Parallel Feedback Systems

This correspondence presents a method whereby the voltage transfer functions of single amplifier multiple ladder feedback systems may be obtained from a suitable ZY table with a minimum of calculation. It extends an earlier result for single amplifier double ladder systems [1] and includes what is believed to be the general case for this particular type of feedback system.

The circuit of order n and rank 2 is shown in Fig. 1. the term order referring to the highest order polynomial appearing in the transfer function, assuming all passive elements are resistors or capacitors. The term rank refers to the number of parallel double ladders in the system, in general denoted by m.

The basic assumptions made are that the gain and input impedance of the amplifier are infinite, its output impedance is zero, and a virtual earth point exists at the point A.

The element numbering is carried out as shown in Fig. 1, where the last subscript of each element denotes the double ladder to which it belongs.

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Derivation of Table

A recurrence formula for this system may be derived to give the voltage transfer function, and the application of this to various orders systems leads to the pattern from which the table may be derived.

Using a notation similar to that previously employed, let the first series element be denoted as Z_{ia}, where a is the respective double ladder suffix, and the last feedback element as Y_{fl}; the latter suffix is always unity, since the system is arranged to have the final feedback component in ladder 1. The transfer ratio $-E_1/E_i$ is denoted as $G(i, f)$ [i odd, f even, $i<f$; if $i>f$, $G(i, f) = 0$]. From inspection of the system it can be seen that for both parallel branches the network increases symmetrically three elements per node per branch until the node $(2n - 1)$ in each ladder is reached. The final section can be regarded as the common adding circuit well known in analog computation.

Considering a node such as B, but treating the elements for a general node in the symmetrical pattern, i.e., node $2r + 1$, the equation for continuity of current is

$$(e_{2r-1} - e_{2r+1})Z_{2r-1}^{-1} = (e_{2r+1} + e_{2n})Y_{2r} + e_{2r+1}Y_{2r,2r+1} + (e_{2r+1} - e_{2r+3})Z_{2r+1}^{-1}; \quad (1)$$

dividing by e_{2n} and rearranging gives

$$\frac{G(2r+1, 2n)_1}{Z_{2r-1_1}} - G(2r+1, 2n)_1\left[Y_{2r} + Y_{2r,2r+1} + \frac{1}{Z_{2r+1}} + \frac{1}{Z_{2r-1}}\right]_1 + \frac{G(2r+3, 2n)_1}{Z_{2r+1_1}} = Y_{2r_1} \quad (2)$$

for $r = 1,2,3 \ldots n - 1$. These equations are repeated for lower ladder with suffix 2.

The boundary conditions are as follows:

1) $G(1, 2n)_1 = G(1, 2n)_2 = G(1. 2n)$ say, [i.e. $e_{11} = e_{12}$] (3)

2) $$\frac{G(2n-1, 2n)_1}{Z_{2n-1_1}} + \frac{G(2n-1, 2n)_2}{Z_{2n-1_2}} = Y_{2n_1} \quad (4)$$

3) $G(2n + 1, 2n)_1 = G(2n + 1, 2n)_2 = 0$,

i.e., virtual earth assumed. (5)

Using the recurrence relationships on the appropriate successive nodes and substituting the boundary conditions, the transfer function can easily be obtained, since from the above it can be seen that there are $2n + 2$ equations and $2n + 2$ unknowns which will result in a soluble set of equations.

The transfer function can be written down easily on the solution of these equations and a pattern of terms in Z and Y emerges which is as follows.

Numerator

There is a set of three component products with two factors in Z and one in Y, a set of five component products with three factors in Z and two in Y, etc. The last term has $2n$ factors in Z and $2n-1$ factors in Y.

Denominator

There is a set of terms which are a function of Z only, a set in one Y and two Z's, etc. The last term has n factors in Z and $n - 1$ factors in Y.

The components are arranged as shown in Table I and the transfer voltage ratio $-E_1/E_2$ can be read off immediately.

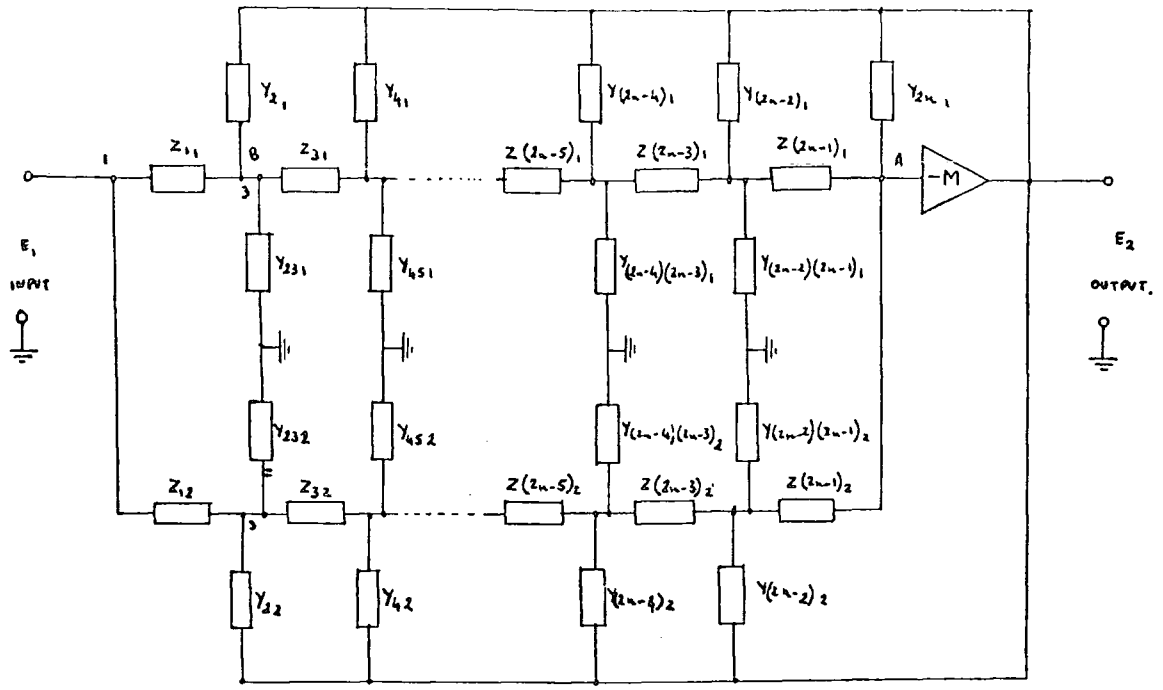

Fig. 1. General double-ladder feedback network of rank two.

TABLE I
ZY TABLE

	n	1	2	3	4		
Series Element 1	Z_{i1}	Z_{11}	Z_{21}	Z_{31}	Z_{41}		$Z_{(2n-1)1}$
Upper Ladder 1	Y_{f1}	Y_{21}	Y_{41}	Y_{61}	Y_{81}		Y_{2n1}
Lower Ladder 1	$Y_{p/1}$	Y_{231}	Y_{451}	Y_{671}	Y_{891}	$Y_{(2n-2)(2n-1)1}$	
Series Element 2	Z_{i2}	Z_{12}	Z_{22}	Z_{32}	Z_{42}		$Z_{(2n-1)2}$
Upper Ladder 2	Y_{f2}	Y_{22}	Y_{42}	Y_{62}	Y_{82}		Y_{2n2}
Lower Ladder 2	$Y_{p/2}$	Y_{232}	Y_{452}	Y_{672}	Y_{892}	$Y_{(2n-2)(2n-1)2}$	

Use of Table

Following a procedure similar to that outlined in Holt and Sewell [1], the terms may be obtained from the table as follows.

Numerator

Sets of Terms in Two Z's and One Y: All Z_{i1} and Z_{j2} are multiplied by the sum of the Y_{f1}'s and Y_{f2}'s beginning with $Y_{(i+1)1}$ up to Y_{2n} and $Y_{(j+1)2}$ up to Y_{2n}, respectively, where i, j are odd.

Sets of Terms in Three Z's and Two Y's: All $Z_{q1}\,Z_{i1}$ are multiplied by

1) all Z_{p2} and by
2) the sum of all Y_1's with suffixes lying between q and v
3) the sum of Y_{f1}'s starting at $v + 1$ to $2n$ plus the sum of Y_{f1}'s starting at $p + 1$ up to $2n$; p,q,v are odd and $q < v$.

This is repeated again with the branch subscripts interchanged.

Sets of Terms in Four Z's and Three Y's: All $Z_{q1}\,Z_{v1}\,Z_{w1}$ are multiplied by

1) all Z_{p2}
2) the sum of all Y_1's with suffixes between q and v
3) the sum of all Y_1's with suffixes between v and w
4) the sum of Y_{f1}'s starting with $w + 1$ to $2n$ plus the sum of Y_{f2}'s starting at $p + 1$ up to $2n$; p,q,v,w are odd and $q < v < w$.

This is repeated with branch subscripts interchanged, and there is a final set of terms in this group given as follows.
All $Z_{p1}\,Z_{q1}$ are multiplied by

1) all $Z_{r2}\,Z_{w2}$
2) the sum of all Y_1's with suffixes between p and q
3) the sum of all Y_2's with suffixes between v and w
4) the sum of Y_{f1}'s starting with $q + 1$ to $2n$ plus the sum of Y_{f2}'s starting with $w + 1$ to $2n$; p,q,v,w are odd and $p < q$, $v < w$.

This procedure is continued until the last term having $2n$ factors in Z and $2n-1$ in Y is reached.

Denominator

Sets of Terms in Zs: This is just the sum of all Z_{i1} and Z_{i2}, where i is odd.

Sets of Terms in Two Z's and One Y: All $Z_{p1}\,Z_{q1}$ are multiplied by the sum of all the Y's lying between suffixes p and q; this is also repeated for branch two; p,q are odd and $p < q$.

Sets of Terms in Three Z's and Two Y's: All $Z_{p1}\,Z_{q1}\,Z_{v1}$ are multiplied by

1) the sum of all Y's with suffixes between p and q
2) the sum of all Y_1's with suffixes between q and v.

This is repeated for branch two; p,q,v are odd and $p < q < v$. This procedure is continued until the last term which has n factors in Z and 2 in Y is reached.

General Systems

It is now possible to consider the general case which is of order n and rank m. The recurrence relations are derived in a similar manner, the boundary conditions now being

$$1) \qquad G(1,2n)_m = G(1,2n) \quad \text{for all} \quad m \tag{6}$$

$$2) \qquad \sum_{a=1}^{m} \frac{G(2n-1,2n)_a}{Z_{2n-1_a}} = Y_{2n_1}; \tag{7}$$

i.e., assume that branch 1 is the highest order ladder.

$$3) \qquad G(2n+1,2n)_m = 0 \quad \text{for all} \quad m. \tag{8}$$

Using these and the recurrence formula of (2) applied to the appropriate nodes, the transfer function may be derived.

The table is merely extended downwards by an appropriate amount and the transfer function read off by the pattern developed. The general expressions for each group of terms are given below.

Numerator

Terms in One Y

$$\sum_{\substack{k_j=1\\ k_j \text{ odd}\\ (j=1,2\cdots m)}}^{2n-1} \left[\left(\prod_{a=1}^{m} Z_{k_{a0}}\right) \sum_{h=1}^{m} \sum_{2l=k_h+1}^{2n_h} Y_{2l_h}\right] \tag{9}$$

n_i = order of i^{th} double ladder.

Terms in Two Y's

$$\sum_{b=1}^{m} \sum_{\substack{p=1\\ p \text{ odd}\\ k_b>p}}^{2n-1} \sum_{\substack{k_j=1\\ k_j \text{ odd}\\ (j=1\cdots m)}}^{2n-1} \left[Z_{pb}\left(\prod_{a=1}^{m} Z_{k_{a0}}\right)\left\{\sum_{2l=p+1}^{k_b-1} (Y_{2l_b} + Y_{2l(2l+1)_b})\right\} \cdot\left\{\sum_{2l=k_b+1}^{2n_b} Y_{2l_b} + \sum_{2s_c=k_c+1}^{2n_c} \sum_{\substack{c=1\\ c\neq b}}^{m} Y_{2s_{cc}}\right\}\right] \tag{10}$$

Terms in Three Y's

$$\sum_{\substack{b=1\\ c=1\\ \text{when } b=c\\ k_b>q>p}}^{m} \sum_{\substack{p=1\\ q=1\\ p,q \text{ odd}}}^{2n-1} \sum_{\substack{k_j=1\\ k_j \text{ odd}\\ (j=1\cdots m)\\ k_b>p\\ k_c>q}}^{2n-1} \left[Z_{pb}Z_{qc}\left(\prod_{a=1}^{m} Z_{k_{a0}}\right) \cdot\left\{\sum_{2l=p+1}^{k_b-1} (Y_{2l_b} + Y_{2l(2l+1)_b})\right\}\left\{\sum_{2l=q+1}^{k_c-1} (Y_{2l_c} + Y_{2l(2l+1)_c})\right\} \cdot\left\{\sum_{2l=k_b+1}^{2n_b} KY_{2l_b} + \sum_{2l=k_c+1}^{2n_c} Y_{2l_c} + \sum_{2s_d=k_d+1}^{2n_d} \sum_{\substack{d=1\\ d\neq b,c}}^{m} Y_{2s_{dd}}\right\}\right] \tag{11}$$

$$\text{when} \quad b=c \quad K=0$$
$$b\neq c \quad K=1$$

From the above it can be seen that for each increase in rank of the network another Z multiplier appears. The above expressions are continued until the last term is reached; in general there are $mn-(m-1)$ terms in the numerator.

Denominator

Terms in Z:

$$\sum_{\substack{q_j=1\\ (j=1\cdots m-1)\\ a_1>a_2\cdots>a_{m-1}}}^{m} \sum_{\substack{k_j=1\\ k_j \text{ odd}\\ (j=1\cdots m-1)}}^{2n-1} \left(\prod_{i=1}^{m-1} Z_{k_{iq_i}}\right) \tag{12}$$

Terms in Y:

$$\sum_{\substack{b=1\\ a_j=1\\ (j=1\cdots m-2)\\ a_j\neq b\\ a_1>a_2\cdots>a_{m-1}}}^{m} \sum_{\substack{q=3\\ q \text{ odd}}}^{2n-1} \sum_{\substack{p=1\\ p \text{ odd}}}^{q-2} \left[Z_{pb}Z_{qb}\left(\prod_{i=1}^{m-2} Z_{k_{ia_i}}\right) \cdot\left\{\sum_{2l=p+1}^{q-1} (Y_{2l_b} + Y_{2l(2l+1)_b})\right\}\right]$$

$$k_j = q,p \qquad (j=1\cdots m-2) \tag{13}$$

Terms in 2Ys:

$$\sum_{c=2}^{m} \sum_{b=1}^{c-1} \sum_{\substack{a_j=1\\ (j=1\cdots m-3)\\ a_j\neq b,c\\ a_1>a_2\cdots>a_{m-1}}}^{m} \sum_{\substack{q=3\\ q \text{ odd}}}^{2n-1} \sum_{\substack{p=1\\ p \text{ odd}}}^{q-2} \sum_{\substack{r=1\\ r \text{ odd}}}^{s-2} \left[Z_{pb}Z_{qb}Z_{rc}Z_{sc}\left(\prod_{i=1}^{m-3} Z_{k_{ia_i}}\right) \cdot\left\{\sum_{2l=p+1}^{q-1} (Y_{2l_b} + Y_{2l(2l+1)_b})\right\}\left\{\sum_{2l=r+1}^{s-1} (Y_{2l_c} + Y_{2l(2l+1)_c})\right\}\right]$$

$$k_j = q,p,r,s \qquad (j=1\cdots m-3) \tag{14}$$

These terms continue to follow the general pattern, there being $m+n-2$ of these.

Conclusion

It is possible to write down simply the voltage transfer ratios for extremely complex feedback systems of the type considered, by inspection of a table; this greatly reduces the arduous task of conventional analysis. It is also possible to carry out this analysis in general terms using a digital computer, since a program would involve only the arithmetic of the subscripts, and reduces error by limiting the operations involved to multiplication and summation, avoiding any redundant procedures.

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PAPER 4

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CORRECTION FUNCTION TECHNIQUES

J.I. Sewell and C. Nightingale

1. Introduction

It is well known [1,2] that the greatest source of error in analysis by the nodal admittance matrix approach occurs in the evaluation of the necessary cofactors and determinants. In particular, if numbers of large magnitude are multiplied and round-off occurs in the computer; then when these numbers, especially if they are nearly equal, are subsequently subtracted from each other, an error of gross magnitude can result. One brute force method of reducing this error is to resort to multiple length arithmetic on the computer, this unfortunately can involve complex machine code programming and a large machine to execute the resulting program.

Also if the nodal admittance matrix is used it is not possible to take full advantage of the network topology during analysis. It is again a known fact that for certain network topologies it is possible to derive recurrence relationships [3, 6] to give fast and accurate analysis methods. This is of particular relevance in iterative synthesis where the analysis time tends to be one of the limiting factors at the present [7].

If an examination of linear passive and active systems is made, one arrives at the following conjecture.

1.1 Conjecture

Any characteristic function (be it a transfer ratio, driving point or transfer immittance) describing a linear passive system with no r.h. plane zeros or an ideal feedback system* in which there is no positive feedback will consist of a ratio of polynomials, in the frequency variable, with positive coefficients only. As these coefficients are positive any subtractive step in the derivation of these is both redundant and error introducing, not only is the step of subtraction redundant but it implies redundancy of previous multiplication and addition steps. Hence, for the systems under consideration, it should be possible to derive analysis techniques which eliminate these redundant steps, thus improving both accuracy and speed of computation.

/1.2

* An ideal feedback system is one in which the active devices can be represented as a simple constraint. One example of this is the ideal voltage operational amplifier, which can be represented as a voltage constraint.

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1.2 Implementation of the Conjecture

For passive ladders, techniques which utilise the above principle have been in existence for some considerable time [3] and variants on the method are well known [4]. However, for many active networks, little work along these lines has been done, probably the main reason being due to added complexity which the active device introduces. Some work has been completed assuming the devices are ideal [5,6] and yield encouraging results.

Unfortunately if the active device cannot be assumed ideal and be represented by some simple constraint, these ideas cannot be used and some general method of analysis has been used. Thus all the disadvantages of a general method return. If, on the other hand, the system can be divided into two sub-systems, one of which represents the system when all devices are assumed ideal, and the other representing the correction required to produce the actual system, then a possible solution is obtained.

Suppose the system is represented by

$$Y = Y_I \oplus Y_c \qquad \text{.....(1)}$$

where Y is the actual system matrix
Y_I is the ideal system matrix
Y_c is the correction matrix.

The "ring sum" is used to indicate that simple addition of Y_I and Y_c is not implied as they are not of the same order as Y.

The required response, could in general be found from evaluating appropriate cofactors of Y. The response when the devices are assumed ideal can be determined from Y_I by one of the techniques referred to already. The actual response can be found by determining the effect which Y_c produces on the system and then combining this with the response due to Y_I.

It is therefore possible to observe the significance of the device non-idealities and parasitics, and at the same time utilise a high-speed, highly accurate procedure for the main task of analysis.

Because of the way in which the effect of Y_c is evaluated it is not possible to ensure comparable speed and accuracy in this section of the procedure.

In the majority of practical situations it is of great advantage if Y_c becomes the null matrix i.e.

$$Y = Y_I$$

Thus it is possible to include the minimisation of Y_c or some related function, in the general minimisation procedure required in the synthesis.

A secondary feature of the method, is concerned with the analysis of structures which depart from normal topologies, without recourse to general methods. For instance, in the case of bridging elements in passive ladder analysis it would be necessary to resort to some general technique and forfeit the benefits of continuant or cumulant methods. With this

technique the bridging elements could be associated with the correction matrix and the remainder of the circuit analysed by recurrence methods. It is also possible to analyse multiterminal amplifier structures by this technique, the positive feedback being assumed as a correction term.

2. The Determination of the Correction Matrix

In the case of a device which can be reduced to some simple constraint it is possible to eliminate a column or row from the admittance matrix, for one variable is a direct function of another. The terms produced in the elimination of the initial row or column can be separated into Y_c as correction elements. These are termed correction elements since if ideal operational amplifiers were being used they would be zero.

Unfortunately it is not always possible to reduce a device to simple current or voltage constraints without considerable difficulty (i.e. it is necessary to produce an equivalent circuit). Even in the case of a transistor, very complex equivalent circuits are proposed which require a computer program of fair complexity to determine them.

As it is possible to produce a Y matrix for any linear device which is non-ideal, either by measurement or by mathematical means via the manufacturers data, it will be assumed that this representation is sufficient. The terms of such an admittance matrix will in general be rational functions. It is thus necessary to assume that admittance matrices to be considered have rational functions as their elements. Obviously the passive elements will never contribute any term larger than a 2nd order polynomial over a 1st order one.

When the device is linear but not ideal some method of simulating the ideal constraint is required. This is accomplished by pivotal condensation. If a pivot or a number of pivots is chosen such that the device is effectively removed from the matrix, the extra terms produced by condensation are separated into Y_C and the original passive terms are retained in Y_I. When the network contains a number of devices the condensation step is repeated until they are all removed. Thus the system matrix has been partitioned into two new matrices Y_I, Y_C of order $n = N - na$ where na is the number of pivots required to remove the devices, and N is the number of nodes in the network.

i.e. $$Y = \left[\begin{array}{c|c} Y_I & 0 \\ \hline 0 & Y_C \end{array}\right] \qquad \text{.....(2)}$$

The method is not restricted to amplifiers, but may be used for systems containing N.I.Cs., gyrators or any linear network device. However, as most devices are fabricated from operational amplifiers its major use will be concerned with such active elements.

3. The Development of the Correction Function Matrix

It is now necessary to determine the effect of the terms of the correction matrix Y_c on the system, response function, or characteristic immittances. There are a number of possible ways of doing this, and these are outlined as follows.

/3.1

3.1 Bond Back-Substitution Method

Consider

$$|Y| = |Y_I \ominus Y_c| \qquad \ldots\ldots\ldots(3)$$

this gives $f_y = f_I + f_c$ $\qquad \ldots\ldots\ldots(4)$

where f_y is some response function

f_I is the ideal response function

f_c is the correction function

The determination of f_I and f_c is easily demonstrated by considering the method of evaluating equation 3, which is a general statement of a specific problem for which the solution is known [8]. A simple proof of the general technique follows.

Theorem

The determinant $|X^1 + X^2 + \ldots . X^n|$ where the 1,2, ...n are suffices not powers, can be calculated by summing individual determinants which themselves consist of all possible combinations of columns of the X^i matrices.

More explicitly let $(\underline{x}^p)_1$, $(\underline{x}^q)_2$ $(\underline{x}^r)_3$ be the first, second and third columns of any of the n matrices X^1, ...X^n, where p may or may not equal q and/or r.

Then let the matrix formed by assembling the three vectors be called x^{pqr}

Then the theorem states.

$$\left| \sum_{r=1}^{n} X^r \right| = \sum |x^{pqr}| \qquad \ldots\ldots\ldots(5)$$

(all possible p, q, r for p, q, r = 1, ...n)

The result is easily seen using the tensor notation. Let ε_{ijk} be the function of ijk such that for $i \neq j = k$ $\varepsilon_{ikj} = \pm 1$ according to whether i,k,j is an even or odd permutation of 1,2,3, (Otherwise $\varepsilon_{ijk} = 0$).

Then by a well known formula

$$|X| = \varepsilon_{ijk}\, x_{1i}\, x_{2j}\, x_{3k}$$

Thus $\left| \sum_{r=1}^{n} X^r \right|$

becomes $$\varepsilon_{ijk} \left(\sum_{r=1}^{n} x_{1i}^{r} \sum_{s=1}^{n} x_{2j}^{s} \sum_{t=1}^{n} x_{3k}^{t} \right)$$

$$= \varepsilon_{ijk} \sum_{r}^{n} \sum_{s}^{n} \sum_{t}^{n} x_{1i}^{r}\, x_{2j}^{s}\, x_{3k}^{t} = \sum_{r}^{n} \sum_{s}^{n} \sum_{t}^{n} \varepsilon_{ijk}\, x_{1i}^{r}\, x_{2j}^{s}\, x_{3k}^{t} \quad \ldots(6)$$

Examination of the equation (6) for r,s,t = 1, ...n shows it to be equivalent to the right hand side of (5) which proves the theorem.

If the terms produced by this method are inspected it will be seen that f_I corresponds to the evaluation of Y_I. Hence if the case of zero back-substitution is omitted, the summation of terms will yield Hf_0, where H is some constant.

It is possible to evaluate the determinant after each back-substitution but this will involve an excessive amount of computation. An alternative technique is to sum all the determinants or matrices after one step of pivotal condensation and then to continue reduction of the resulting matrix or determinant. (The technique of pivotal condensation is used in preference to any other because in the case when a correction function matrix is required, this is the superior method, since if cofactors are evaluated, four are required in the general case, thus the amount of computation is multiplied).

The general pivotal condensation formula for a determinant is

$$|Y|_{n-1,n-1} = (-1)^{pi+pj} (y_{pi,pj})^{-(n-2)} |X|_{n-1,n-1}$$

where X is a determinant formed from terms of the type

$$y_{ij}\ y_{pi,pj} - y_{pi,j}\ y_{i,pj}.$$

For a matrix the formula is

$$Y_{n-1,n-1} = (-1)^{pi+pj} (y_{pi,pj})^{-1} X_{n-1,n-1}$$

the terms of the matrix X are formed as above.

When Y = A + B say, these formulae now become:

$$|A+B|_{n-1,n-1} = \frac{(-1)^{pi+pj}(a_{pi,pj} + b_{pi,pj})^{-(n-2)} |C_{AB}|_{n-1,n-1}}{\sum_{r=0}^{n-2} {}^{n-2}C_r} \qquad \ldots(7)$$

$$[A+B]_{n-1,n-1} = \frac{(-1)^{pi+pj}(a_{pi,pj} + b_{pi,pj})^{-1} [C_{AB}]_{n-1,n-1}}{\sum_{r=0}^{n-2} {}^{n-2}C_r} \qquad \ldots(8)$$

C_{AB} is an n-1 x n-1 matrix formed by taking all the possible combinations of rows or columns from B, back-substituting these in A and developing new terms of the form

$$y_{ij}\ y_{pi,pj} - y_{pi,j}\ y_{j,pj}.$$

i.e. $C_{AB} = \sum_{s=1}^{p} C_{ab,s}$ where $p = \sum_{r=0}^{n} {}^{n}C_r$

Where $\sum_{r=0}^{n-2} {}^{n-2}C_r$ is the number of times any particular term appears in the expansion.

In the case of the ideal and correction matrices, the zero back-substitution step is omitted to produce a correction function matrix. The

formulae remain unchanged.

As will be appreciated from (8) it is necessary to consider a total of $\sum_{r=0}^{n-1} {}^{n}C_{r}$ combinations of back-substitution evaluations in general and $\sum_{r=0}^{n} {}^{n}C_{r} - 1$ in the correction function case. This is a prohibitively large number as n becomes large, and is the major disadvantage of this particular method.

3.2 Reduction of computation on Total Back-Substitution

In most networks it is highly unlikely that every node will be connected to an active device, thus it is most probable that there will be a number of rows and columns of Y_c which only contain zero. As the present policy is to back substitute columns, it ought to be possible to reduce the number of combinations considered by eliminating the zero columns from Y_c, this also reduces storage space. The original column numbering has of course to be retained in a counter.

Because the number of combinations is reduced a different divisor is required than that in equation (8). Obviously no term in a zero column can be used as a pivot. If nc is the number of non-zero columns, back substitution of a reduced Y_c matrix will yield

$\sum_{r=0}^{nc-1} {}^{nc}C_{r}$ combinations. Thus the number of excess combinations produced when zero columns are back-substituted is

$$\sum_{r=0}^{n-1} {}^{n}C_{r} - \sum_{r=0}^{nc-1} {}^{nc}C_{r}$$

The number of excess terms involving an $a_{pi,pj}$ or a $b_{pi,pj}$ term is

$$\frac{\sum_{r=0}^{n-1} {}^{n}C_{r} - \sum_{r=0}^{nc-1} {}^{nc}C_{r}}{2}$$

Thus if only columns which are not zero are back-substituted then the matrix (8) becomes

$$[A + B]_{n-1,n-1} = (-1)^{pi+pj}(a_{pi,pj} + b_{pi,pj})^{-1}\mathcal{E}C_{AB}$$

$$\mathcal{E} = \frac{\sum_{r=0}^{n-1} {}^{n}C_{r} - \sum_{r=0}^{nc-1} {}^{nc}C_{r} + 2\delta_{nc}^{n}}{2\sum_{r=0}^{n-2} {}^{n-2}C_{r}}$$

Applying these formulae considerable reduction in computation will result.

However there will be still a good number of back-substitutions and with increase in n the increase in these follows an exponential curve.

Further investigation reveals another method of evaluating the correction function matrix.

5.3 The Minimal Back-Substitution Method

Consider $Y = X_1 + X_2 + \ldots + X_m$

Where Y and X's are n x n matrices.

A new matrix Y' (n - 1) x (n - 1) may be formed according to the rule

$$Y'_{(n-1)(n-1)} = (-1)^{pi + pj} \left\{ \sum_{k=1}^{m}{}' (x_{pi,pj})_k \right\}^{-1} \cdot$$

$$X \left\{ \sum_{j=i+1}^{m} \sum_{i=1}^{m-1}{}' \left[W_i A_i + W_{ij} A_{ij} + W_{ji} B_{ji} + W_j B_j \right] \right\}$$

W's are weights calculated as shown later.
A_i is any matrix X_i reduced by one order.
A_{ij} is any matrix X_i with a pivot column or row from X_j substituted and reduced by one order.
B_j is any matrix X_j reduced by one order.
B_{ji} is any matrix X_j with a pivot column or row from X_i substituted and reduced by one order.

The validity of this rule may be established in the following way, take the case of m = 2, if the elements of the Y' matrix are examined it is found that they can be written down as the series:

$$Y'_{ii\ jj} = \sum_{r=0}^{q}{}' (x_1(pi,pj)\ x_2(i,j) - x_1(i,pj)\ x_2(pi,j))r$$

$$+ \sum_{r=0}^{q}{}' (x_1(pi,pj)\ x_1(i,j) - x_1(i,pj)\ x_1(pi,j))r$$

$$+ \sum_{r=0}^{q}{}' (x_2(pi,pj)\ x_1(i,j) - x_2(i,pj)\ x_1(pi,j))r$$

$$+ \sum_{r=0}^{q}{}' (x_2(pi,pj)\ x_2(i,j) - x_2(i,pj)\ x_2(pi,j))r$$

$$q = \sum_{r=0}^{n-2}{}' {}^{n-2}C_r \cdot$$

If the terms are collected, the expression can then be simply written in terms of the A and B matrices above. For m > 2 the procedure is repeated over all pairs of matrices.

It is therefore possible to synthesise the elements of C_{ij} from four combinations, and this is true for all n, hence it is not necessary to consider the large number of combinations normally required.

For the general problem of reducing A + B, the weights W_i assume the value of unity. In a case when omission of certain back-substitutions are required, it is necessary to determine relevant weighting functions.

$$\left[A + B\right]_{n-1,n-1} = (-1)^{pi+pj}(a_{pi,pj} + b_{pi,pj})^{-1}$$

$$\cdot \left\{ W_1 A_1 + W_2 A_{12} + W_3 B_{21} + W_4 B_2 \right\}$$

If the zero back substitution is omitted, one set of terms of the type A_1 will be missing; now in general there are

$$\frac{\sum_{r=0}^{n-1} {}^{n-1}C_r}{2} \quad \text{of these terms.}$$

Hence:

$$W_1 = 1 - \frac{2}{\sum_{r=0}^{n-1} {}^{n-1}C_r}$$

Once the matrix $\left[A + B\right]_{n-1,n-1}$ has been synthesised, further reduction is achieved by standard pivotal condensation on the single matrix.

4. Storage Requirements and Program Limitations

For the two main methods considered it is necessary to determine the storage requirements for each method.

4.1 Total Back-Substitution

In all calculations it is assumed that:

Y - N x N x (np + 2 + nd). Array Y = network matrix
(np = max. order of numerator Y)
(nd = max. order of denominator Y)
C - (N - na) x (N - na) x (npc + 2 + ndc). Array C = correction matrix. .....(9)

npc = max. order of numerator C
ndc = max. order of denominator C

Y1 - (N - na) x (N - na) x (npn + 2 + ndn). Array Y1 = ideal system matrix. .....(10)

npn = max. order of numerator Y1
ndn = max. order of denominator Y1

The working array YW has to contain the terms produced by substitution,

YW - (N - na) x (N - na) x (npw + 2 + ndw)

where npw and ndw are computed as follows:

$npw_i = 2(npw_{i-1} + ndw_{i-1})$

$ndw_i = 4\, ndw_{i-1}$

$i = 1, 2, \ldots (N - na - 2)$ $\quad npw_0 = npc \quad ndw_0 = ndc$

where npc and ndc are similarly calculated

$npc_i = 2npci_{i-1} + ndc_{i-1} + nd$

$ndc_i = 2(ndc_{i-1} + nd) + npci_{i-1}$

and $npci_{i-1} = \max.(np + ndc_{i-1},\ nd + npc_{i-1})$

$i = 1,2...na.$ $\quad npc_o = 0 \quad ndc_o = 0.$

Array YC, the correction function matrix requires:

$$YC = 2 \times 2\,(2 + [npw_{N-na-2} + npi_{N-na-3} + ndi_{N-na-3}] + [ndw_{N-na-2}]\,[2TNC\,(N-na) - 3])$$

$$TNC(N-na) = \sum_{r=0}^{N-na} {}^{N-na}C_r$$

$$ndi_o = \max.\,(npn + ndc,\ npc + ndn) \qquad npi_i = npi_{i-1} + ndw_{i-1}$$

$$npi_o = ndn + nic \qquad ndi_i = ndi_{i-1} + npw_{i-1}$$

$$i = 1,2,....(N - na - 3)$$

4.2 Minimal Back-Substitution

The two arrays C, Y1 are as in equations (9), (10).

Y1 - working array for the 1 node reduction.
Y1 - (N-na) x (N-na) x (2 [npc + ndc] + 4 ndc + 2)
YW - (N-na) x (N-na) x (npw + 2 + ndw)

where npw and ndw are computed as follows:

$$npa_i = \max.\,\{npa_{i-1} + 4ndc;\ 2(npc + ndc) + nda_{i-1}\}$$

$$nda_i = nda_{i-1} + 4\,ndc$$

$$i = 1,2,3$$

$$npa_o = 2(npn + ndn) \qquad nda_o = 4\,ndn$$

$$npw_i = 2(npw_{i-1} + ndw_{i-1})$$

$$ndw_i = 4\,ndw_{i-1}$$

$$i = 1,2...(N - na - 3)$$

where $npw_o = npa_3$, $ndw_o = nda_3$

$$YC = 4(2 + npi_{N-na-4} + npw_{N-na-3} + ndi_{N-na-4} + ndw_{N-na-3})$$

4.3 Comparison of Storage Requirements

	Total Back-Substitution	Minimal Back-Substitution
N = 4, np = 1, npn = 1 na = 1, nd = 0, ndn = 0	1,190	1,182
N = 5, np = 1, npn = 1 na = 1, nd = 0, ndn = 0	9,108	6,536
N = 6, np = 1, npn = 1 na = 1, nd = 0, ndn = 0	61,800	33,866

Extra storage will be necessary in both methods, for working areas and polynomial handling.

It can be seen that as the number of nodes increase the demand on storage space becomes severe. This is particularly evident in the total back-substitution method.

5. Correction Function and Correction Function Matrix

5.1 Correction Function Matrix

In most circumstances it is usually advisable to derive correction

parameters for all four admittance parameters of the network.

One method of reducing the storage required is by using the pivotal technique outlined in section 3. The common factor is retained outside the main array, thus the order of the individual elements is less than in the normal method. When the matrix has finally reached 2 x 2 dimensions the accumulated factor is then multiplied into the array. Hence only a 2 x 2 array has its 3rd dimension equal to the sum of the maximum orders of the polynomials involved. This is to be contrasted with the alternative situation where the first two dimensions of the array would be n.

5.2 Correction Function

In some cases it is not possible to derive a correction function matrix with finite parameters. This can occur, for example, in a network where the active element has a connection to the output node, e.g., a multi-loop feedback network with a voltage operational amplifier. In such circumstances it may be required to derive a correction for the voltage transfer ratio; this is achieved by reducing the matrix to 3 x 3, and then evaluating the appropriate cofactors and employing Cramers Rule.

6. Analysis of the Ideal System

The method employed here depends largely upon the system under investigation, the requirements for such a method have been cited earlier.

A system which has been of considerable interest recently is the multi-loop feedback one [7], the ZY methods [5,6] are applicable to this class of networks. A program ALA utilising these techniques has been written in Algol and is suitable for inclusion in a correction function analysis.

The development of other analysis procedures applicable in a correction function approach is the subject of further work.

7. Use of program

As the major limitation is due to storage space available on the computer, a block structure is employed to minimise the storage demanded at any one time by the program. Even so, a KDF9 with 16K store will only permit this computation on circuits with a maximum of 5 nodes. It may be possible to improve the storage demands by employing magnetic tape storage and segmentation, this unfortunately will tend to slow down the computation.

Of the two programs used, it is obvious that the one using the Minimal Back-Substitution Method is superior both in time taken for execution and for storage requirements. All examples have therefore been computed with this program.

An example of a 2nd order multi-loop Butterworth circuit (Fig. 1) was examined when the active device (ideally an infinite gain voltage amplifier) departs from ideal. The ideal analysis using program ALA took 4 secs. of computing time and the correction function approx. 2 mins. using the Algol compiler. The graphs, Figure 2, show the ideal response and two corrected responses for different amplifiers.

8. Conclusions

A general technique for taking account of non-idealities of active devices in network analysis has been presented. This enables the use of fast and accurate recursive procedures in the evaluation of an ideal response and correction terms are supplied subsequently. This technique provides a useful analysis method for iterative synthesis where speed is vital. For the correction terms, which are essentially numerical and require a longer time for evaluation, it may be possible to compute these,

say every ten cycles of iteration, and introduce them to the error function being minimised.

A corollary of this which is perhaps more important, is that using this technique the effects of the active devices are isolated and therefore can be minimised directly. As it is not easy to determine partial derivatives of these functions, probably a minimisation procedure such as Simplex could be employed. While using an ideal analysis technique one of the more powerful optimisation methods may be used since partial derivatives are readily available in explicit form and the correction terms can be treated as constraints.

It is difficult to give an appraisal of the accuracy of the method. Certainly the evaluation of the ideal response function is very accurate as no redundant algebraic steps are performed. There will be round-off error due to multiplication but this is not accentuated by subsequent subtractions. It is never possible to completely eliminate computational errors. The evaluation of the correction terms is subject to the conventional sources of error, but as these terms are usually of small magnitude and minimisation of them is usually intended, any errors here are of secondary importance.

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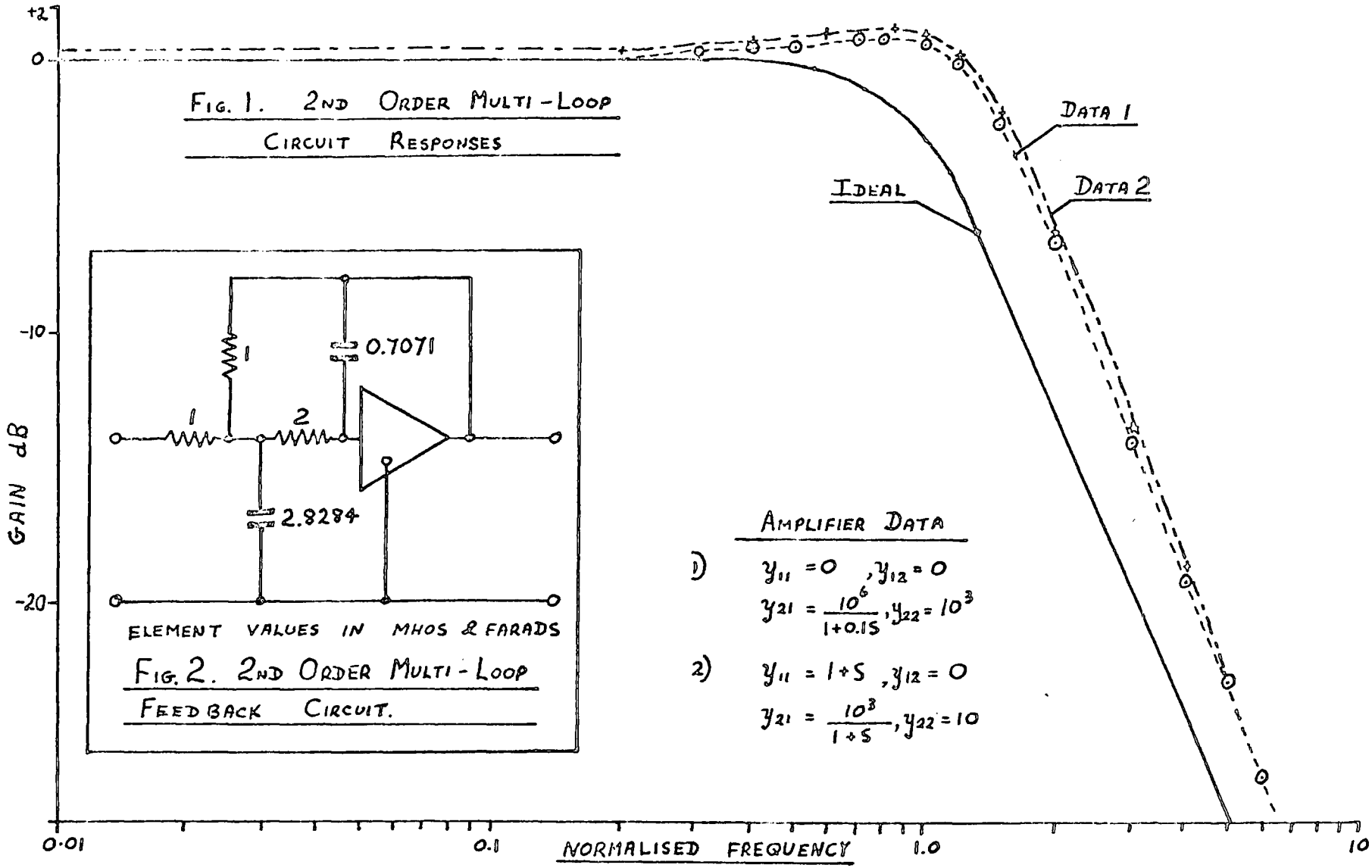

FIG. 1. 2ND ORDER MULTI-LOOP CIRCUIT RESPONSES

ELEMENT VALUES IN MHOS & FARADS

FIG. 2. 2ND ORDER MULTI-LOOP FEEDBACK CIRCUIT.

AMPLIFIER DATA

1) $y_{11} = 0$, $y_{12} = 0$

$y_{21} = \frac{10^6}{1+0.1S}$, $y_{22} = 10^3$

2) $y_{11} = 1+S$, $y_{12} = 0$

$y_{21} = \frac{10^3}{1+S}$, $y_{22} = 10$

PAPER 5

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Matrix Tables for the Generalized 5-Terminal Amplifier

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Summary: The paper considers the admittance matrices of the generalized 5-terminal amplifier and shows that the more commonly used amplifiers are special cases of the model. It is noted that the single operational amplifiers are equivalent when included in a network.

The admittance matrices of a number of familiar amplifier networks are listed in the tables.

1. Introduction

Voltage operational amplifiers are familiar active elements in electronics. Their characteristics have been relatively simple to attain using valves and, latterly, transistors.

The present design practice allows the engineer to produce other forms of operational amplifiers such as the transimpedance, transadmittance and current types.

The paper considers these different configurations from a matrix standpoint. The admittance matrices of the various amplifiers are listed and their properties are discussed. It is noted that networks made up from operational amplifiers have transfer characteristics which do not depend upon the particular type of amplifier used.

In the final Section of the paper, the admittance matrices for a number of familiar feedback sections are presented.

2. The 5-terminal Active Device

For the device shown in Fig. 1, it is assumed that the internal feedback terms are zero over the range of frequencies of interest. The definite admittance matrix can be written down immediately. It is logical to use the definite admittance matrix as in the majority of practical cases node 5 is grounded, hence this may be treated as the reference node. The matrix is shown in Fig. 2.

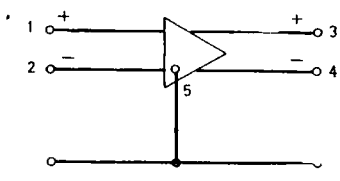

Fig. 1. 5-terminal active device.

In the majority of cases it is reasonable to assume that the common-mode input admittance $y_{12} = y_{21} \to 0$. Similarly, the common-mode output admittance $y_{34} = y_{43} \to 0$. Hence, in the tables developed, these terms are assumed to be zero. If in a particular case this is not true then the appropriate terms should be included.

3. Amplifier Admittance Matrices

3.1. *The Amplifier ABCD Parameters*

Using the amplifier driving point admittances it is of value to derive the remaining admittance entries in terms of certain parameters and these admittances. It is found that only four extra parameters are needed: open-circuit voltage gain A, short-circuit current gain B, transfer admittance C, transfer impedance D.

Thus, in the case of a voltage amplifier the forward transfer admittance $y_{n1} = -Ay_{nn}$ or, for a current amplifier, $y_{n1} = -By_{11}$. For the transadmittance amplifier the only parameter which appears is the transfer admittance C. The forward transfer admittance of a transimpedance amplifier whose transfer impedance is D, is $y_{n1} = -Dy_{11}y_{nn}$, since the amplifier is assumed to be completely non-reciprocal.

3.2. *The Matrix Tables*

These tables are derived from the matrix of Fig. 2 by assuming the arbitrarily assigned voltage polarities as shown in Fig. 1. Tables 1 to 4 give the matrices

	1	2	3	4
1	y_{11}	$-y_{12}$	0	0
2	$-y_{21}$	y_{22}	0	0
3	$-y_{31}$	$-y_{32}$	y_{33}	$-y_{34}$
4	$-y_{41}$	$-y_{42}$	$-y_{43}$	y_{44}

Fig. 2. Admittance matrix for the 5-terminal active device shown in Fig. 1.

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for practical and operational cases, the parameter K is a constant which tends to infinity.

Included in these tables are the matrices for the common amplifier configurations, which are obtained by eliminating certain nodes.

An interesting point to note is that the single operational amplifiers are equivalent when included in a network. This can be shown by simple transformation.[1]

The hybrid amplifiers are given in Tables 5 to 7. If there is 1 : 1 conversion from voltage to current, then $A = C$.

3.3. *A Comparison of the Different Types of Amplifiers*

In the physical realization of the various operational types it is obvious that some will be easier to construct than others. With modern techniques using f.e.t.s it is possible to obtain extremely high input resistances (10^{11} Ω) and, for a limited frequency range, $y_{11} \to 0$. The realization of very low output impedances (< 100 Ω) is common practice and application of suitable feedback can produce very low values indeed. Thus $y_{22} \to \infty$, at least in comparison with surrounding network elements, provided denormalization is suitably performed. The voltage operational amplifier is therefore a practical proposition and in fact is the most common type at the present time.

The realization of extremely high input admittances is not particularly difficult with a common-base circuit or with suitable feedback. But zero output admittances present a somewhat more difficult problem, although circuits approaching this (output resistances of the order of 50 MΩ or even 1000 MΩ) are not unknown.[2] This makes the current operational amplifier quite feasible, although, perhaps, rather more complex than the above.

The transimpedance operational type is probably the most suitable of all, i.e. zero input impedance and zero output impedance, both of which can be realized fairly accurately and simply.

The amplifier which presents the most practical problems in construction is the transadmittance one, which requires high input resistance and high output resistance. Although realization of this type is not at all beyond present techniques.

With regard to usage, if the forward gain parameter (voltage, current, impedance, admittance) of an

Table 1 Admittance matrices for the voltage type amplifier

Configuration		General amplifier				Operational amplifier			
		1	2	3	4	1	2	3	4
General	1	0	0	0	0	0	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-Ay_{33}$	Ay_{33}	y_{33}	0	K^2	$-K^2$	K	0
	4	Ay_{44}	$-Ay_{44}$	0	y_{44}	K^2	$-K^2$	0	K
Difference	1	0	0	×	0	0	0	×	0
	2	0	0	×	0	0	0	×	0
	3	×	×	×	×	×	×	×	×
	4	Ay_{44}	$-Ay_{44}$	×	y_{44}	K^2	$-K^2$	×	K
Paraphase	1	0	×	0	0	0	×	0	0
	2	×	×	×	×	×	×	×	×
	3	$-Ay_{33}$	×	y_{33}	0	$-K^2$	×	K	0
	4	Ay_{44}	×	0	y_{44}	K^2	×	0	K
Single in/out	1	0	×	×	0	0	×	×	0
	2	×	×	×	×	×	×	×	×
	3	×	×	×	×	×	×	×	×
	4	Ay_{44}	×	×	y_{44}	K^2	×	×	K

Table 2 Admittance matrices for the current type amplifier

Configuration		General amplifier				Operational amplifier			
		1	2	3	4	1	2	3	4
General	1	y_{11}	0	0	0	K	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-By_{11}$	By_{22}	0	0	$-K^2$	K^2	0	0
	4	By_{11}	$-By_{22}$	0	0	K^2	$-K^2$	0	0
Difference	1	y_{11}	0	×	0	K	0	×	0
	2	0	y_{22}	×	0	0	K	×	0
	3	×	×	×	×	×	×	×	×
	4	By_{11}	$-By_{22}$	×	0	K^2	$-K^2$	×	0
Paraphase	1	y_{11}	×	0	0	K	×	0	0
	2	×	×	×	×	×	×	×	×
	3	$-By_{11}$	×	0	0	$-K^2$	×	0	0
	4	By_{11}	×	0	0	K^2	×	0	0
Single in/out	1	y_{11}	×	×	0	K	×	×	0
	2	×	×	×	×	×	×	×	×
	3	×	×	×	×	×	×	×	×
	4	By_{11}	×	×	0	K^2	×	×	0

Table 3 Admittance matrices for the transadmittance type amplifier

Configuration		General amplifier				Operational amplifier			
		1	2	3	4	1	2	3	4
General	1	0	0	0	0	0	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-C$	C	0	0	$-K$	K	0	0
	4	C	$-C$	0	0	K	$-K$	0	0
Difference	1	0	0	×	0	0	0	×	0
	2	0	0	×	0	0	0	×	0
	3	×	×	×	×	×	×	×	×
	4	C	$-C$	×	0	K	$-K$	×	0
Paraphase	1	0	×	0	0	0	×	0	0
	2	×	×	×	×	×	×	×	×
	3	$-C$	×	0	0	$-K$	×	0	0
	4	C	×	0	0	K	×	0	0
Single in/out	1	0	×	×	0	0	×	×	0
	2	×	×	×	×	×	×	×	×
	3	×	×	×	×	×	×	×	×
	4	C	×	×	0	K	×	×	0

Table 4 Admittance matrices for the transimpedance type amplifier

Configuration		General amplifier				Operational amplifier			
		1	2	3	4	1	2	3	4
General	1	y_{11}	0	0	0	K	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-Dy_{11}y_{33}$	$Dy_{22}y_{33}$	y_{33}	0	$-K^3$	K^3	K	0
	4	$Dy_{11}y_{44}$	$-Dy_{22}y_{44}$	0	y_{44}	K^3	$-K^3$	0	K
Difference	1	y_{11}	0	×	0	K	0	×	0
	2	0	y_{22}	×	0	0	K	×	0
	3	×	×	×	×	×	×	×	×
	4	$Dy_{11}y_{44}$	$-Dy_{22}y_{44}$	×	y_{44}	K^3	$-K^3$	×	K
Paraphase	1	y_{11}	×	0	0	K	×	0	0
	2	×	×	×	×	×	×	×	×
	3	$-Dy_{11}y_{33}$	×	y_{33}	0	$-K^3$	×	K	0
	4	$Dy_{11}y_{44}$	×	0	y_{44}	K^3	×	0	K
Single in/out	1	y_{11}	×	×	0	K	×	×	0
	2	×	×	×	×	×	×	×	×
	3	×	×	×	×	×	×	×	×
	4	$Dy_{11}y_{44}$	×	×	y_{44}	K^3	×	×	K

Table 5 Admittance matrices for an amplifier with hybrid input admittances

Type		General amplifier				Operational amplifier			
		1	2	3	4	1	2	3	4
Voltage output	1	y_{11}	0	0	0	K	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-Dy_{11}y_{33}$	Ay_{33}	y_{33}	0	$-K^3$	K^2	K	0
	4	$Dy_{11}y_{44}$	$-Ay_{44}$	0	y_{44}	K^3	$-K^2$	0	K
Voltage output	1	0	0	0	0	0	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-Ay_{33}$	$Dy_{22}y_{33}$	y_{33}	0	$-K^2$	K^3	K	0
	4	Ay_{44}	$-Dy_{22}y_{44}$	0	y_{44}	K^2	$-K^3$	0	K
Current output	1	y_{11}	0	0	0	K	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-By_{11}$	C	0	0	$-K^2$	K	0	0
	4	By_{11}	$-C$	0	0	K^2	$-K$	0	0
Current output	1	0	0	0	0	0	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-C$	By_{22}	0	0	$-K$	K^2	0	0
	4	C	$-By_{22}$	0	0	K	$-K^2$	0	0

Table 6 Admittance matrices for an amplifier with hybrid output admittances

Type		General amplifier				Operational amplifier			
		1	2	3	4	1	2	3	4
Voltage input	1	0	0	0	0	0	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-C$	C	0	0	$-K$	K	0	0
	4	Ay_{44}	$-Ay_{44}$	0	y_{44}	K^2	$-K^2$	0	K
Voltage input	1	0	0	0	0	0	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-Ay_{33}$	Ay_{33}	0	y_{33}	$-K^2$	K^2	0	K
	4	C	$-C$	0	0	K	$-K$	0	0
Current input	1	y_{11}	0	0	0	K	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-Dy_{11}y_{33}$	$Dy_{22}y_{33}$	y_{33}	0	$-K^3$	K^3	K	0
	4	By_{11}	$-By_{22}$	0	0	K^2	$-K^2$	0	0
Current input	1	y_{11}	0	0	0	K	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-By_{11}$	By_{22}	0	0	$-K^2$	K^2	0	0
	4	$Dy_{11}y_{44}$	$-Dy_{22}y_{44}$	0	y_{44}	K^3	$-K^3$	0	K

Table 7 Admittance matrices for a complete hybrid amplifier

Type		General amplifier				Operational amplifier			
		1	2	3	4	1	2	3	4
Complete hybrid	1	0	0	0	0	0	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-C$	By_{22}	0	0	$-K$	K^2	0	0
	4	Ay_{44}	$-Dy_{22}y_{44}$	0	y_{44}	K^2	$-K^3$	0	K
Complete hybrid	1	y_{11}	0	0	0	K	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-By_{33}$	C	0	0	$-K^2$	K	0	0
	4	$Dy_{11}y_{44}$	$-Ay_{44}$	0	y_{44}	K^3	$-K^2$	0	K
Complete hybrid	1	0	0	0	0	0	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-Ay_{33}$	$Dy_{22}y_{33}$	y_{33}	0	$-K^2$	K^3	K	0
	4	C	$-By_{22}$	0	0	K	$-K^2$	0	0
Complete hybrid	1	y_{11}	0	0	0	K	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-Dy_{11}y_{33}$	Ay_{33}	y_{33}	0	$-K^3$	K^2	K	0
	4	By_{11}	$-C$	0	0	K^2	$-K$	0	0

amplifier is extremely large and approaching infinity then the values of the input and output admittances are immaterial.

4. Network Matrices

In this Section a number of familiar amplifier configurations are considered, together with their respective matrices.

4.1. *Basic Feedback Network*

The circuit shown in Fig. 3 has the definite admittance matrix shown in Table 8. For a conventional voltage operational amplifier

$$\frac{e_4}{e_s} = \frac{-y_{4s}}{y_{44}} = \frac{Y_1(Ay_{44}-Y_2)}{(y_{44}+Y_2)(y_{11}+Y_1+Y_2)+Y_2(Ay_{44}-Y_2)} \quad \ldots\ldots(1)$$

This expression reduces to the more familiar one:

$$\frac{e_4}{e_s} = -\frac{Y_1}{Y_2} \quad \ldots\ldots(2)$$

if y_{11}, $1/A \to 0$, where A denotes the amplifier gain.

4.2. *Non-inverting Amplifier I*

Figure 4 and Table 9 show the circuit and definite admittance matrix respectively.

In the derivation of the matrix it was assumed that

$$A_{14} = -A_{24} = -A \quad \text{and} \quad y_{12} = y_{21}$$

If we further assume that

$$y_{44} \to \infty \quad \text{and} \quad y_{11}, y_{12} \to 0$$

then

$$\frac{e_4}{e_s} = \frac{(Y_1+Y_2)A}{Y_1+Y_2(1+A)} = \left(1+\frac{Y_1}{Y_2}\right) \quad \ldots\ldots(3)$$

if $A \gg 1$.

4.3. *Non-inverting Amplifier II*

The network shown in Fig. 5 illustrates a further method of obtaining a non-inverted relationship between input and output voltages. From Table 10, if we let

$$y_{11}, y_{12} \to 0$$

and

$$Y_1 = Y_2 = Y_3 = Y_4 = Y$$

then

$$\frac{e_4}{e_s} = \frac{Y(Y+y_{44}A)}{[(2Y+Y_5)\left\{2Y+y_{44}+\frac{Y(y_{44}A-Y)}{2Y}\right\}-Y(y_{44}A+Y)]} \quad \ldots\ldots(4)$$

Now, if y_{44} and $A \to \infty$, then

$$\frac{e_4}{e_s} = \frac{2Y}{Y_5} \quad \ldots\ldots(5)$$

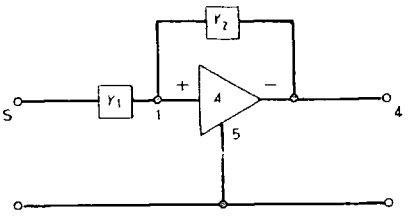

Fig. 3. Basic feedback network.

Table 8

Admittance matrix for a basic feedback network

$Y_1 - \frac{Y_1^2}{y_{11}+Y_1+Y_2}$	$\frac{-Y_1Y_2}{y_{11}+Y_1+Y_2}$
$\frac{Y_1(Ay_{44}-Y_2)}{y_{11}+Y_1+Y_2}$	$(y_{44}+Y_2) + \frac{Y_2(Ay_{44}-Y_2)}{y_{11}+Y_1+Y_2}$

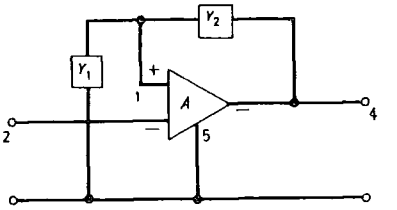

Fig. 4. Non-inverting amplifier (I).

Table 9 Admittance matrix for the non-inverting amplifier (I) (Fig. 4)

$(y_{22}+y_{12}) - \frac{y_{12}^2}{y_{11}+y_{12}+Y_1+Y_2}$	$-\frac{y_{12}Y_2}{y_{11}+y_{12}+Y_1+Y_2}$
$-y_{44}A + \frac{y_{12}(y_{44}A-Y_2)}{y_{11}+y_{12}+Y_1+Y_2}$	$(y_{44}+Y_2) + \frac{Y_2(y_{44}A-Y_2)}{y_{11}+y_{12}+Y_1+Y_2}$

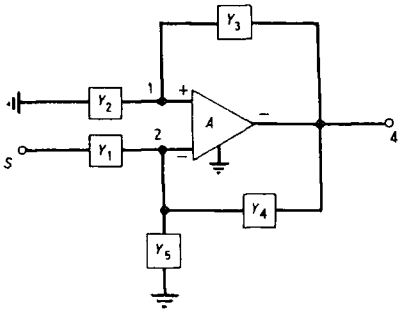

Fig. 5. Non-inverting amplifier (II).

Table 10 Admittance matrix for the non-inverting amplifier (II) (Fig. 5)

S	$Y_1 - \dfrac{Y_1^2}{\left\{\begin{matrix} y_{22}+y_{12}+Y_1+Y_4+Y_5 \\ -\dfrac{y_{12}^2}{y_{11}+y_{12}+Y_2+Y_3}\end{matrix}\right\}}$	$\dfrac{-Y_1\left\{Y_4+\dfrac{Y_3 y_{12}}{y_{11}+y_{12}+Y_2+Y_3}\right\}}{\left\{\begin{matrix} y_{22}+y_{12}+Y_1+Y_4+Y_5 \\ -\dfrac{y_{12}^2}{y_{11}+y_{12}+Y_2+Y_3}\end{matrix}\right\}}$
4	$\dfrac{Y_1\left\{\begin{matrix} -(Y_4+y_{44}A) \\ +\dfrac{Y_{12}(y_{44}A-Y_3)}{y_{11}+y_{12}+Y_2+Y_3}\end{matrix}\right\}}{\left\{\begin{matrix} y_{22}+y_{12}+Y_1+Y_4+Y_5 \\ -\dfrac{y_{12}^2}{y_{11}+y_{12}+Y_2+Y_3}\end{matrix}\right\}}$	$\left(y_{44}+Y_4+Y_3+\dfrac{Y_3(y_{44}A-Y_3)}{y_{11}+y_{12}+Y_2+Y_3}\right) - \left\{Y_4+\dfrac{Y_3 y_{12}}{y_{11}+y_{12}+Y_2+Y_3}\right\}\dfrac{\left\{\begin{matrix} -(y_{44}A+Y_4) \\ +y_{12}(y_{44}A-Y_3)\end{matrix}\right\}}{y_{11}+y_{12}+Y_2+Y_3}}{\left\{\begin{matrix} y_{22}+y_{12}+Y_1+Y_4+Y_5 \\ -\dfrac{y_{12}^2}{y_{11}+y_{12}+Y_2+Y_3}\end{matrix}\right\}}$

Table 11

Admittance matrix for the voltage follower (Fig. 6)

y_{12}	$-y_{12}$
$-(y_{44}A+y_{12})$	$y_{44}(1+A)+y_{12}$

This network can be used as a positive integrator.[3] If

$$Y_1 = 1/2R \quad \text{and} \quad Y_5 = \rho C$$

then

$$\frac{e_4}{e_s} = \frac{1}{\rho CR} \qquad \text{.....(6)}$$

4.4. *Voltage Follower*

The circuit and its matrix are shown in Fig. 6 and Table 11 respectively.

4.5. *Summing Network*

The familiar summing network is shown in Fig. 7 and its admittance matrix is shown in Table 12. In general, the matrix elements may be calculated from the following expressions:

(i) Diagonal elements (except y_{44}):

$$Y_{S_n,S_n} = Y_n - \frac{Y_n^2}{y_{11}+\sum_{i=1}^{n} Y_i} \qquad \text{.....(7)}$$

(ii) Off-diagonal elements (except those including node 4):

$$Y_{S_j,S_k} = \frac{-Y_j Y_k}{y_{11}+\sum_{i=1}^{n} Y_i} \quad j,k = 1 \rightarrow n \qquad \text{.....(8)}$$

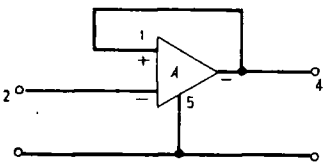

Fig. 6. Voltage follower.

(iii) Node 4 off-diagonal elements:

$$Y_{S_j,4} = \frac{-Y_j Y_f}{y_{11}+\sum_{i=1}^{n} Y_i} \quad = 1 \rightarrow n \qquad \text{.....(9)}$$

$$Y_{4,S_k} = \frac{Y_k(Ay_{44}-Y_f)}{y_{11}+\sum_{i=1}^{n} Y_i} \quad k = 1 \rightarrow n \qquad \text{.....(10)}$$

Y_{44} is listed in Table 12.

4.5. *Differential Output Network*

A configuration suitable for, say, a dual integrator is shown in Fig. 8 and its matrix is given in Table 13.

As $y_{11} \rightarrow 0$ and $y_{44} \rightarrow \infty$

$$\frac{e_4}{e_s} = \frac{-Y_1 A_{14}}{Y_1 + Y_2(1+A_{14})} \qquad \text{.....(11)}$$

If $A_{14} \gg 1$, then

$$\frac{e_4}{e_s} = \frac{-Y_1}{Y_2} \qquad \text{.....(12)}$$

Also, if $y_{33} \rightarrow \infty$

$$\frac{e_3}{e_s} = \frac{Y_1 A_{13}}{Y_2(1+A_{13})+Y_1} \qquad \text{.....(13)}$$

Table 12 Admittance matrix for the summing amplifier network (Fig. 7)

	S_1	S_2	S_n	4
S_1	$Y_1 - \dfrac{Y_1^2}{y_{11}+\sum Y_i}$	$\dfrac{-Y_1 Y_2}{y_{11}+\sum Y_i}$	$\dfrac{-Y_1 Y_n}{y_{11}+\sum Y_i}$	$\dfrac{-Y_1 Y_f}{y_{11}+\sum Y_i}$
S_2	$\dfrac{-Y_1 Y_2}{y_{11}+\sum Y_i}$	$Y_2 - \dfrac{Y_2^2}{y_{11}+\sum Y_i}$	$\dfrac{-Y_2 Y_n}{y_{11}+\sum Y_i}$	$\dfrac{-Y_2 Y_f}{y_{11}+\sum Y_i}$
S_n	$\dfrac{-Y_1 Y_n}{y_{11}+\sum Y_i}$	$\dfrac{-Y_2 Y_n}{y_{11}+\sum Y_i}$	$Y_n - \dfrac{Y_n^2}{y_{11}+\sum Y_i}$	$\dfrac{-Y_n Y_f}{y_{11}+\sum Y_i}$
4	$\dfrac{Y_1(Ay_{44}-Y_f)}{y_{11}+\sum Y_i}$	$\dfrac{Y_2(Ay_{44}-Y_f)}{y_{11}+\sum Y_i}$	$\dfrac{Y_n(Ay_{44}-Y_f)}{y_{11}+\sum Y_i}$	$\dfrac{(y_{44}+Y_f)+Y_f(Ay_{44}-Y_f)}{y_{11}+\sum Y_i}$

Table 13 Differential output network

	S	3	4
S	$Y_1 - \dfrac{Y_1^2}{Y_1+Y_2+y_{11}}$	0	$\dfrac{-Y_1 Y_2}{Y_1+Y_2+y_{11}}$
3	$\dfrac{-Y_1 y_{33} A_{13}}{Y_1+Y_2+y_{11}}$	y_{33}	$\dfrac{-Y_2 y_{33} A_{13}}{Y_1+Y_2+y_{11}}$
4	$\dfrac{Y_1(y_{44}A_{14}-Y_2)}{Y_1+Y_2+y_{11}}$	0	$Y_2+y_{44}+\dfrac{Y_2(y_{44}A_{14}-Y_2)}{Y_1+Y_2+y_{11}}$

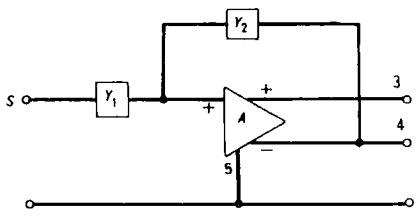

Fig. 8. Differential output network.

If $A_{13} \gg 1$, then

$$\frac{e_3}{e_s} = \frac{Y_1}{Y_2} \qquad \text{.....(14)}$$

If $Y_2 = \rho C$ and $Y_1 = 1/R$, then the network can be used as a dual integrator giving positive and negative integrals of the input signal.

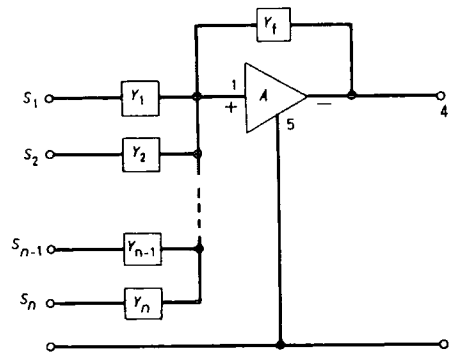

Fig. 7. Summing network.

5. Acknowledgments

The authors have pleasure in acknowledging financial support from the Ministry of Technology.

6. References

1. Sewell, J. I., 'The Application of Analogue Computing Techniques to the Design of Active Filters', Ph.D. Thesis, University of Newcastle-upon-Tyne, 1966.
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7. Appendix

The equivalent circuits and admittance matrices for the various amplifiers used in Section 4 are listed in Tables 14 and 15.

Table 14
Amplifier equivalent circuits

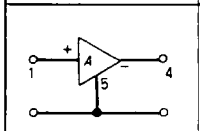
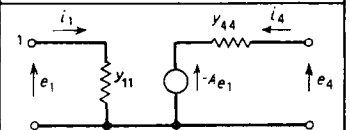
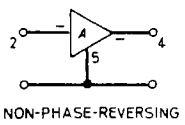
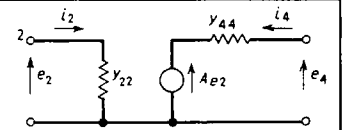
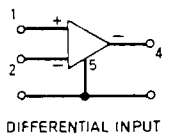
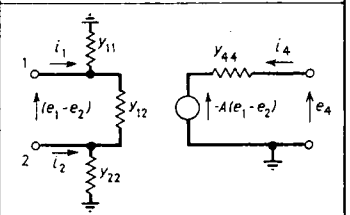
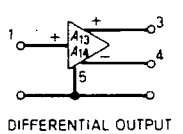
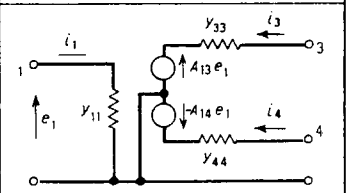
AMPLIFIER	EQUIVALENT CIRCUIT
 PHASE REVERSING	
 NON-PHASE-REVERSING	
 DIFFERENTIAL INPUT	
 DIFFERENTIAL OUTPUT	

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Table 15
Amplifier matrices

Amplifier		Admittance matrix		
Phase reversing		1		4
	1	y_{11}		0
	4	Ay_{44}		y_{44}
Non-phase reversing		2		4
	2	y_{22}		0
	4	$-Ay_{44}$		y_{44}
Differential input $\left\{\begin{matrix} y_{12}=y_{21} \\ A_{14}=A_{24}=A \end{matrix}\right\}$		1	2	4
	1	$y_{11}+y_{12}$	$-y_{12}$	0
	2	$-y_{12}$	$y_{22}+y_{12}$	0
	4	$y_{44}A$	$-y_{44}A$	y_{44}
Differential output		1	3	4
	1	y_{11}	0	0
	3	$-y_{33}A_{13}$	y_{33}	0
	4	$y_{44}A_{14}$	0	y_{44}

PAPER 9

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Accumulant theory and applications

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The increase in demand for synthesis of active networks by digital computer has accentuated the problem of producing fast and accurate analysis procedures. The accumulant method is one technique which is applicable to multiple-loop feedback systems and meets the time and accuracy requirements.

Modern optimization techniques used in iterative synthesis often require the computation of partial derivatives; the accumulant method permits these to be calculated analytically with great ease. The derivatives also find application in sensitivity studies.

Using accumulant techniques it is possible to divide a large analysis problem into smaller ones, thus reducing the store required at any one instant in the computer.

Various algebraic properties of accumulants are examined and appropriate proofs furnished.

1. Introduction

In recent years there has been an increasing interest in the derivation of algorithmic methods of analysis for various networks. This has been brought about by the demand for faster and more accurate analysis techniques for use on computers. General analysis methods are either not sufficiently accurate (Skwirzynski 1965) or occupy so much computer store to make them impracticable. These difficulties are accentuated when iterative synthesis is considered, and a third factor, the time occupied by the analysis step, becomes a major concern.

Many optimization procedures used in automatic synthesis require the computation of the partial derivatives of the error function each cycle of iteration. With many methods this is not particularly easy to accomplish, and if numerical differentiation is being used inaccuracies are inevitably present.

Analysis methods which will meet the above demands are quite well established for passive networks (Bartlett 1930, Herrero and Willoner 1966). But active networks have not received as much attention, although some progress has been made in the case of multi-loop feedback networks (Holt and Sewell 1966). These techniques do satisfy the accuracy, time and storage demands cited above but the computation of partial derivatives, though possible, is not straightforward and requires extra programming of the computer.

The accumulant method enables the accurate and speedy analysis of a multi-loop structure and permits an analytic assembly of the derivatives.

2. Formulation of the H matrix

For passive ladder networks, it has been shown (Herrero and Willoner 1966) that if a hybrid matrix is considered, instead of an admittance or impedance matrix, then a simple method of evaluation of the characteristic functions results. A similar method is applicable to multi-loop feedback systems of the single and double ladder type.

Consider fig. 1 and using the variables shown, it is possible to assemble equations for voltages and currents as the matrix eqn. (1):

$$\begin{bmatrix} e_0 \\ 0 \\ . \\ . \\ . \\ . \\ . \\ . \\ . \\ 0 \end{bmatrix} = \begin{bmatrix} Z_1 & 1 & 0 & 0 & . & . & . & . & . & 0 \\ -1 & Y_2 & 1 & 0 & . & . & . & . & . & Y_2 \\ 0 & -1 & Z_3 & 1 & 0 & . & . & . & . & 0 \\ . & 0 & -1 & Y_4 & 1 & 0 & . & . & . & Y_4 \\ . & . & . & . & . & . & . & . & . & . \\ . & . & . & . & . & . & . & . & . & . \\ . & . & . & . & . & . & -1 & Y_{2N-4} & 1 & Y_{2N-4} \\ . & . & . & . & . & . & 0 & -1 & Z_{2N-3} & 0 \\ . & . & . & . & . & . & 0 & 0 & -1 & Y_{2N-2} \end{bmatrix} \begin{bmatrix} i_1 \\ e_2 \\ i_3 \\ e_4 \\ . \\ . \\ e_{2N-4} \\ i_{2N-3} \\ e_{2N} \end{bmatrix} \tag{1}$$

N is the number of nodes in the network.

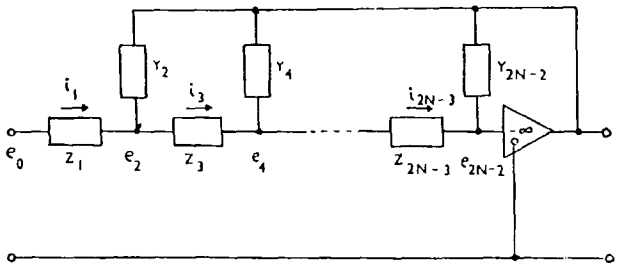
It is easily shown that various characteristic functions can be obtained, giving:

$$\text{voltage gain } G_{21} = \frac{1}{(Z_1 \text{——} Y_{2N-2})};$$

$$\text{input impedance } Z_{11} = \frac{(Z_1 \text{——} Y_{2N-2})}{(Y_2 \text{——} Y_{2N-2})}; \tag{2}$$

$$\text{forward transfer impedance } Z_{12} = \frac{1}{(Y_2 \text{——} Y_{2N-2})}.$$

Fig. 1



Single ladder multiple-loop feedback system.

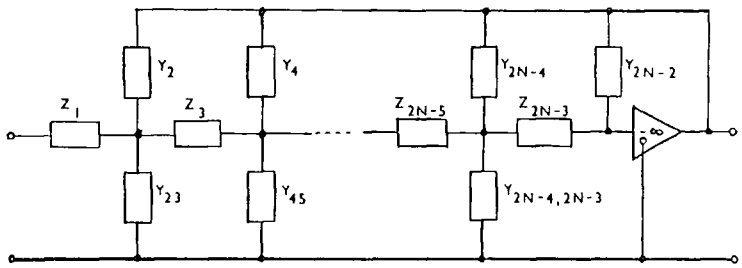
The terms in brackets are called accumulants, in this case they are referred to as single accumulants. They are similar to cumulants (Herrero and Willoner 1966) but because the form of the H matrix is slightly modified, different properties result.

If the double ladder feedback network of fig. 2 is considered, the hybrid matrix takes the form:

$$H = \begin{bmatrix}
Z_1 & 1 & 0 & . & . & . & . & . & . & 0 \\
-1 & Y_2+Y_{23} & 1 & 0 & . & . & . & . & . & Y_2 \\
0 & -1 & Z_3 & 1 & 0 & . & . & . & . & 0 \\
0 & 0 & -1 & Y_4+Y_{45} & 1 & 0 & . & . & . & Y_4 \\
. & . & . & . & . & . & . & . & . & . \\
. & . & . & . & . & . & . & . & . & . \\
. & . & . & . & . & . & -1 & Y_{2N-4}+Y_{2N-4,2N-3} & 1 & Y_{2N-4} \\
. & . & . & . & . & . & 0 & -1 & Z_{2N-3} & 0 \\
. & . & . & . & . & . & 0 & 0 & -1 & Y_{2N-2}
\end{bmatrix}$$

This matrix leads to double accumulants.

Fig. 2



Double ladder multiple-loop feedback system.

3. The relationship between single accumulants and the Euler form

It is well known that the determinants of the matrices which lead to simple continuants and cumulants are simply evaluated by a method due to Euler (Bartlett 1930). Single accumulants can be evaluated by a similar technique, which is now outlined.

Consider the hybrid matrix of a single ladder feedback system:

$$H = \begin{bmatrix}
a_1 & 1 & 0 & . & . & . & . & . & . & 0 \\
-1 & a_2 & 1 & 0 & . & . & . & . & . & a_2 \\
0 & -1 & a_3 & 1 & 0 & . & . & . & . & 0 \\
. & 0 & -1 & a_4 & 1 & 0 & . & . & . & a_4 \\
. & . & . & . & . & . & . & . & . & . \\
. & . & . & . & . & . & . & . & . & . \\
. & . & . & . & . & . & -1 & a_{n-2} & 1 & a_{n-2} \\
. & . & . & . & . & . & 0 & -1 & a_{n-1} & 0 \\
. & . & . & . & . & . & 0 & 0 & -1 & a_n
\end{bmatrix}$$

where a_i is an admittance or impedance.

This can be separated into the sum of two matrices:

$$H = H_1 + H_2$$

$$H = \begin{bmatrix} a_1 & 1 & 0 & . & . & . & . & . & 0 \\ -1 & a_2 & 1 & 0 & . & . & . & . & 0 \\ 0 & -1 & a_3 & 1 & 0 & . & . & . & 0 \\ . & 0 & -1 & a_4 & 1 & 0 & . & . & 0 \\ . & . & . & . & . & . & . & . & . \\ . & . & . & . & . & . & . & . & . \\ . & . & . & . & . & -1 & a_{n-2} & 1 & 0 \\ . & . & . & . & . & 0 & -1 & a_{n-1} & 1 \\ . & . & . & . & . & . & 0 & -1 & a_n \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & . & . & . & 0 \\ 0 & 0 & 0 & . & . & . & a_2 \\ 0 & 0 & 0 & . & . & . & 0 \\ 0 & 0 & 0 & . & . & . & a_4 \\ . & . & . & . & . & . & . \\ . & . & . & . & . & . & . \\ . & . & . & . & . & . & a_{n-2} \\ . & . & . & . & . & . & -1 \\ . & . & . & . & . & . & 0 \end{bmatrix}$$

Now $|H| = |H_1 + H_2|$ can be evaluated by a back-substitution method (Sewell and Nightingale 1969). As every column of H_2 is zero, apart from the final one:

$$|H| = |H_1| + \begin{vmatrix} a_1 & 1 & 0 & . & . & . & . & . & . & 0 \\ -1 & a_2 & 1 & 0 & . & . & . & . & . & a_2 \\ 0 & -1 & a_3 & 1 & 0 & . & . & . & . & 0 \\ 0 & 0 & -1 & a_4 & 1 & 0 & . & . & . & a_4 \\ . & . & . & . & . & . & . & . & . & . \\ . & . & . & . & . & . & . & . & . & . \\ . & . & . & . & . & . & -1 & a_{n-2} & 1 & a_{n-2} \\ . & . & . & . & . & . & 0 & -1 & a_{n-1} & -1 \\ . & . & . & . & . & . & . & 0 & -1 & 0 \end{vmatrix}$$

When n is even:

$$|H| = |H_1| - 1,$$

n odd:

$$|H| = |H_1|$$

H_1 is of the correct form for evaluation by the Euler method. The case when n is odd corresponds precisely to that of odd cumulants. When n is even -1 is present, this cancels the $+1$ which appears in the evaluation of even-order cumulants. Accumulants are normally of even order.

It must be noted that this is only true for complete accumulants, if, as is shown later, even-order split accumulants or partial accumulants occur, these must be treated as normal cumulants. The exception to this being the split or partial accumulant which contains the final element, this comes from a matrix which can be split into the form of $H_1 + H_2$ and is evaluated as above.

The algebraic properties of single accumulants are the same as those of cumulants (Herrero and Willoner 1966).

4. The algebra of double accumulants

The algebra of double accumulants is somewhat more complex than that of the single accumulants, the most important properties are now investigated.

4.1. *Rule for expansion*

Let

$$(a_1 \text{——} a_n) \oplus (b_1 \text{——} b_{n-2}) = \begin{vmatrix} a_1 & 1 & 0 & . & . & . & . & 0 \\ -1 & a_2+b_2 & 1 & 0 & . & . & . & a_2 \\ 0 & -1 & a_3 & 1 & 0 & . & . & 0 \\ 0 & 0 & -1 & a_4+b_4 & 1 & 0 & . & a_4 \\ . & . & . & . & . & . & . & . \\ . & . & . & . & . & . & . & . \\ . & . & . & . & . & a_{n-2}+b_{n-2} & 1 & a_{n-2} \\ . & . & . & . & . & -1 & a_{n-1} & 0 \\ . & . & . & . & . & 0 & -1 & a_n \end{vmatrix},$$

where a_i (i odd) are series impedances,

a_i (i even) are feedback admittances,

b_i (i even) are shunt admittances to earth,

$$(a_1 \text{——} a_n) \oplus (b_1 \text{——} b_{n-2}) = (a_1 \text{——} a_n) + \sum_{i=1}^{m} b_{2i} (a_1 \text{——} a_{2i-1})(a_{2i+1} \text{——} a_n),$$

$$+ \sum_{j=i+1}^{m} \sum_{i=1}^{m-1} b_{2i} b_{2j} (a_1 \text{——} a_{2i-1})(a_{2i+1} \text{——} a_{2j-1})(a_{2j+1} \text{——} a_n)$$

$$+ \ldots$$

$$+ (b_2 b_4 \ldots b_{n-2})(a_1 a_3 \ldots a_{n-3} a_{n-1} a_n).$$

$$m = \frac{n-2}{2}$$

(n is even).

Proof

$(a_1 \text{——} a_n) \oplus (b_1 \text{——} b_{n-2})$ results from the sum of two matrices:

$$\underset{\text{A}}{\begin{bmatrix} a_1 & 1 & 0 & . & . & . & . & . & 0 \\ -1 & a_2 & 1 & 0 & . & . & . & . & a_2 \\ 0 & -1 & a_3 & 1 & 0 & . & . & . & 0 \\ . & 0 & -1 & a_4 & 1 & 0 & . & . & a_4 \\ . & . & . & . & . & . & . & . & . \\ . & . & . & . & . & . & . & . & . \\ . & . & . & . & . & . & -1 & a_{n-1} & 1 \\ . & . & . & . & . & . & 0 & -1 & a_n \end{bmatrix}} + \underset{\text{B}}{\begin{bmatrix} 0 & 0 & . & . & . & . & . & . & 0 \\ 0 & b_2 & 0 & . & . & . & . & . & 0 \\ . & 0 & 0 & 0 & . & . & . & . & 0 \\ . & . & 0 & b_4 & 0 & . & . & . & 0 \\ . & . & . & . & . & . & . & . & . \\ . & . & . & . & . & . & b_{n-2} & 0 & 0 \\ . & . & . & . & . & . & . & 0 & -1 \\ . & . & . & . & . & . & . & . & 0 \end{bmatrix}}.$$

Using a back-substitution method, zero substitution in A will, by reasoning given earlier, yield the first term of the expansion. When a single finite b column is substituted, a determinant of the following form results:

$$\begin{vmatrix} a_1 & 1 & 0 & . & . & . & . & . & . & 0 \\ -1 & a_2 & 1 & . & . & . & . & . & . & a_2 \\ 0 & -1 & a_3 & . & 1 & . & . & . & . & . \\ . & 0 & -1 & . & a_{i-1} & 0 & . & . & . & 0 \\ . & . & 0 & . & -1 & b_i & 1 & . & . & a_i \\ . & . & . & . & 0 & 0 & a_{i+1} & . & . & 0 \\ . & . & . & . & . & . & -1 & . & . & . \\ . & . & . & . & . & . & . & . & a_{n-1} & 1 \\ . & . & . & . & . & . & . & . & -1 & a_n \end{vmatrix}.$$

The evaluation of this yields $(a_1 \text{——} a_{i-1})\, b_i\, (a_{i+1} \text{——} a_n)$, thus the second term results as a sum over all i (i is even).

The third term follows when combinations of two finite b columns are considered.

The final term occurs when all the finite b columns are substituted.

4.2. *Rule for splitting*

$$\begin{aligned}
&(a_1 \text{——} a_r,\ a_{r+1} \text{——} a_n) \oplus (b_1 \text{——} b_r,\ b_{r+1} \text{——} b_{n-2}) \\
&= (a_1 \text{——} a_r)\,(a_{r+1} \text{——} a_n) + (a_1 \text{——} a_{r-1})\,(a_{r+2} \text{——} a_n) \\
&\quad + \sum_{i=\lfloor (r+1)/2 \rfloor}^{m} b_{2i} \{(a_1 \text{——} a_r)\,(a_{r+1} \text{——} a_{2i-1}) + (a_1 \text{——} a_{r-1})\,(a_{r+2} \text{——} a_{2i-1})\} \\
&\qquad \times \{(a_{2i+1} \text{——} a_n)\} \\
&\quad + \sum_{i=1}^{\lfloor r/2 \rfloor - 1} b_{2i} \{(a_1 \text{——} a_{2i-1})\}\, \{(a_{2i+1} \text{——} a_r)(a_{r+1} \text{——} a_n) \\
&\qquad + (a_{2i+1} \text{——} a_{r-1})(a_{r+2} \text{——} a_n)\} \\
&\quad + \sum_{j=i+1}^{m} \sum_{i=\lfloor (r+1)/2 \rfloor}^{m-1} b_{2i} b_{2j} \{(a_1 \text{——} a_r)(a_{r+1} \text{——} a_{2i-1}) + (a_1 \text{——} a_{r-1})(a_{r+2} \text{——} a_{2i-1})\} \\
&\qquad \times \{(a_{2i+1} \text{——} a_{2j-1})(a_{2j+1} \text{——} a_n)\} \\
&\quad + \sum_{j=\lfloor (r+1)/2 \rfloor}^{m} \sum_{i=1}^{\lfloor r/2 \rfloor - 1} b_{2i} b_{2j}\, (a_1 \text{——} a_{2i-1}) \{(a_{2i+1} \text{——} a_r)(a_{r+1} \text{——} a_{2j-1}) \\
&\qquad + (a_{2i+1} \text{——} a_{r-1})(a_{r+2} \text{——} a_{2j-1})\} \times \{(a_{2j+1} \text{——} a_n)\} \\
&\quad + \sum_{j=i+1}^{\lfloor r/2 \rfloor - 1} \sum_{i=1}^{\lfloor r/2 \rfloor - 2} b_{2i} b_{2j}\, (a_1 \text{——} a_{2i-1})(a_{2i+1} \text{——} a_{2j-1}) \\
&\qquad \times \{(a_{2j+1} \text{——} a_r)(a_{r+1} \text{——} a_n) + (a_{2j+1} \text{——} a_{r-1})(a_{r+2} \text{——} a_n)\} \\
&\quad + \ldots \\
&\quad + \Big(\prod_{i=1}^{(n-2)/2} b_{2i} \Big) \Big(\prod_{j=1}^{n/2} a_{2j-1} \Big) a_n.
\end{aligned}$$

Proof

This follows simply by applying (4.1) and the rule for splitting cumulants (Herrero and Willoner 1966).

4.3. *Expansion by the a_n term*

$$
\begin{aligned}
&(a_1 \text{——} a_n) \oplus (b_1 \text{——} b_{n-2}) \\
&= (a_1 \text{——} a_{n-1})\, a_n + (a_1 \text{——} a_{n-2}) \\
&\quad + \sum_{i=1}^{m} b_{2i}\, (a_1 \text{——} a_{2i-1}) \{(a_{2i-1} \text{——} a_{n-1})\, a_n + (a_{2i+1} \text{——} a_{n-2})\} \\
&\quad + \sum_{j=i+1}^{m} \sum_{i=1}^{m-1} b_{2i} b_{2j}\, (a_1 \text{——} a_{2i-1})(a_{2i+1} \text{——} a_{2j-1}) \\
&\qquad \times \{(a_{2j+1} \text{——} a_{n-1}) a_n + (a_{2j+1} \text{——} a_{n-2})\} \\
&\quad + \ldots \\
&\quad + \Big(\prod_{i=1}^{(n-2)/2} b_{2i} \Big) \Big(\prod_{i=1}^{n/2} a_{2j-1} \Big) a_n .
\end{aligned}
$$

Proof

This follows by applying the rule for expanding cumulants by the final term to the expansion of (4.1).

4.4. *Rules for partial derivatives*

Let $\mathscr{A} = (a_1 \text{——} a_n) \oplus (b_1 \text{——} b_{n-2})$

4.4.1. *Differentiation by an a_r term*

$$
\begin{aligned}
\frac{\partial \mathscr{A}}{\partial a_r} &= (a_1 \text{——} a_{r-1})\, (a_{r+1} \text{——} a_n) \\
&\quad + \sum_{i=[(r+1)/2]}^{m} b_{2i}\, (a_1 \text{——} a_{r-1})\, (a_{r+1} \text{——} a_{2i-1})\, (a_{2i+1} \text{——} a_n) \\
&\quad + \sum_{i=1}^{[r/2]-1} b_{2i}\, (a_1 \text{——} a_{2i-1})\, (a_{2i+1} \text{——} a_{r-1})\, (a_{r+1} \text{——} a_n) \\
&\quad + \sum_{j=i+1}^{m} \sum_{i=[(r+1)/2]}^{m-1} b_{2i} b_{2j}\, (a_1 \text{——} a_{r-1})(a_{r+1} \text{——} a_{2i-1})(a_{2i+1} \text{——} a_{2j-1})(a_{2j+1} \text{——} a_n) \\
&\quad + \sum_{j=[(r+1)/2]}^{m} \sum_{i=1}^{[r/2]-1} b_{2i} b_{2j}\, (a_1 \text{——} a_{2i-1})(a_{2i+1} \text{——} a_{r-1})(a_{r+1} \text{——} a_{2j-1}) \\
&\qquad \times (a_{2j+1} \text{——} a_n) \\
&\quad + \sum_{j=i+1}^{[r/2]-1} \sum_{i=1}^{[r/2]-2} b_{2i} b_{2j}\, (a_1 \text{——} a_{2i-1})(a_{2i+1} \text{——} a_{2j-1})(a_{2j+1} \text{——} a_{r-1})(a_{r+1} \text{——} a_n) \\
&\quad + \ldots \\
&\quad + \Big(\prod_{i=1}^{(n-2)/2} b_{2i} \Big) \Big(\prod_{j=1}^{n/2} a_{2j-1} \Big) \frac{a_n}{a_r} \left\{ \delta_n{}^r \frac{1}{a_n} + \sum_{j=1}^{n/2} \delta_{2j-1}{}^r \right\}
\end{aligned}
$$

$\delta_j{}^i$ is the Kronecker delta.

Proof

Apply rule 4.3 to 4.2 gives:

$$
\begin{aligned}
&(a_1 \text{——} a_r, a_{r+1} \text{——} a_n) \oplus (b_1 \text{——} b_r, b_{r-1} \text{——} b_{n-2}) \\
&= \{(a_1 \text{——} a_{r-1})\, a_r + (a_1 \text{——} a_{r-2})\}\,(a_{r-1} \text{——} a_n) + (a_1 \text{——} a_{r-1})(a_{r-2} \text{——} a_n) \\
&\quad + \sum_{i=[(r+1)/2]}^{m} b_{2i}\,\{[(a_1 \text{——} a_{r-1})a_r + (a_1 \text{——} a_{r-2})]\,(a_{r-1} \text{——} a_{2i-1}) \\
&\qquad\qquad + (a_1 \text{——} a_{r-1})(a_{r-2} \text{——} a_{2i-1})\} \times \{(a_{2i+1} \text{——} a_n)\} \\
&\quad + \sum_{i=1}^{[r/2]-1} b_{2i}\,(a_1 \text{——} a_{2i-1})\{[(a_{2i+1} \text{——} a_{r-1})a_r + (a_{2i+1} \text{——} a_{r-2})]\,(a_{r+1} \text{——} a_n) \\
&\qquad\qquad + (a_{2i+1} \text{——} a_{r-1})(a_{r+2} \text{——} a_n)\} \\
&\quad + \sum_{j=[(r+1)/2]}^{m} \sum_{i=1}^{[r/2]-1} b_{2i} b_{2j}\,(a_1 \text{——} a_{2i-1})\{[(a_{2i+1} \text{——} a_{r-1})a_r + (a_{2i+1} \text{——} a_{r-2})] \\
&\qquad\qquad \times (a_{r+1} \text{——} a_{2j-1}) + (a_{2i-1} \text{——} a_{r-1})(a_{r+2} \text{——} a_{2j-1})\} \\
&\qquad\qquad \times (a_{2j+1} \text{——} a_n) \\
&\quad + \sum_{j=i+1}^{[r/2]-1} \sum_{i=1}^{[r/2]-2} b_{2i} b_{2j}\,(a_1 \text{——} a_{2i-1})(a_{2i+1} \text{——} a_{2j-1})\{[(a_{2j+1} \text{——} a_{r-1})a_r \\
&\qquad\qquad + (a_{2j+1} \text{——} a_{r-2})]\,(a_{r+1} \text{——} a_n) + (a_{2j+1} \text{——} a_{r-1})(a_{r+2} \text{——} a_n)\} \\
&\quad + \sum_{j=i+1}^{m} \sum_{i=[(r+1)/2]}^{m-1} b_{2i} b_{2j}\{[(a_1 \text{——} a_{r-1})a_r + (a_1 \text{——} a_{r-2})]\,(a_{r+1} \text{——} a_{2i-1}) \\
&\qquad\qquad + (a_1 \text{——} a_{r+1})(a_{r+2} \text{——} a_{2i-1})\}(a_{2i+1} \text{——} a_{2j-1})(a_{2j+1} \text{——} a_n) \\
&\quad + \ldots \\
&\quad + \left(\prod_{i=1}^{(n-2)/2} b_{2i}\right)\left(\prod_{j=1}^{n/2} a_{2j-1}\right) a_n .
\end{aligned}
$$

Differentiation w.r.t. a_r leads to the formula given.

Notice must be taken, however, in the evaluation of the accumulants. As $\partial \mathscr{A}/\partial a_r = |C_r|$, where C_r is the co-factor of the a_r term, when r is even the a_r term appears in two columns of the H matrix, thus $\partial \mathscr{A}/\partial a_r$ is the sum of two co-factors, one of these is unity. Thus evaluation follows the rules for cumulants. However, when a b_{2i} column is substituted (4.1) and $r < n-2$, $2i > r$ this unity co-factor now becomes zero. When $r = n-2$, $2i < r$, the two co-factors are $a_{n-1}\, a_n$ and 1 because $2i \ngtr n-2$. Otherwise the split accumulants are evaluated as indicated earlier.

4.4.2. *Differentiation by a b_r term* (r is always even)

$$
\begin{aligned}
\frac{\partial \mathscr{A}}{\partial b_r} &= (a_1 \text{——} a_{r-1})\,(a_{r+1} \text{——} a_n) \\
&\quad + \sum_{i=1}^{r/2-1} b_{2i}\,(a_1 \text{——} a_{2i-1})(a_{2i+1} \text{——} a_{r-1})(a_{r+1} \text{——} a_n) \\
&\quad + \sum_{j=[(r+1)/2]}^{m-1} b_{2j}\,(a_1 \text{——} a_{r-1})(a_{r+1} \text{——} a_{2j-1})\,(a_{j+1} \text{——} a_n) \\
&\quad + \ldots \\
&\quad + \left(\prod_{i=1}^{m-1} b_{2i}\right) \frac{a_n}{b_r} \left(\prod_{j=1}^{n/2} a_{2j-1}\right).
\end{aligned}
$$

Proof

Consider the expansion of (4.1), differentiating w.r.t. b_r leads directly to the above expression.

4.5. *Other algebraic rules*

It is possible to extend the algebra to include rules for other manipulations, however this is fairly straightforward. and the ones developed are sufficient in the present context.

5. Evaluation of accumulants by recurrence formula

A similar formula to that which is used for continuants (Bartlett 1930) is also applicable here.

If $C_n=(a_1\text{——}a_n)$, then $C_r=a_r C_{r-1}+C_{r-2}-\sum_{s=1}^{[r/2]}\delta_{2s}{}^{n}$,

$C_0=1$,

$C_1=a_1$,

$C_2=a_1a_2+1$,

$C_3=a_3(a_1a_2+1)+a_1$,

$C_n=a_nC_{n-1}+C_{n-2}-\sum_{s=1}^{[n/2]}\delta_{2s}{}^{n}$.

6. Analysis of multi-loop feedback and feed-forward networks

Multi-loop feedback networks having one or more feed-forward paths have proved to be useful (Holt and Sewell 1965). If the hybrid matrix for fig. 3 is assembled according to the method given, it will be found to be non-square. However, if the network is fed from a voltage source it is possible to produce a square matrix. In this case it will only be possible to consider voltage transfer functions.

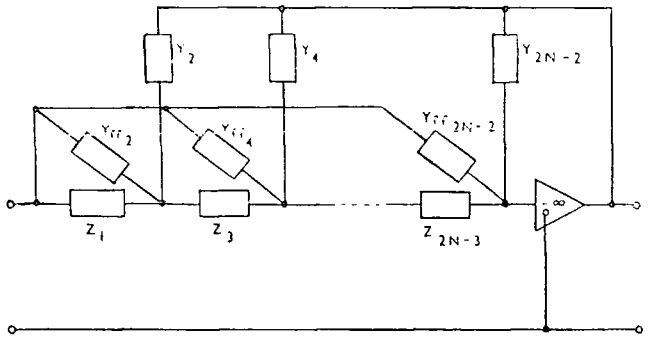
If the currents through the feed-forward paths are written as:

$$e_0 Y_{ffi},$$

the H matrix equation takes the form:

$$\begin{bmatrix} e_0 \\ e_0'Y_{ff2} \\ 0 \\ e_0Y_{ff4} \\ . \\ . \\ e_0Y_{ff2N-4} \\ 0 \\ e_0Y_{ff2N-2} \end{bmatrix} = \begin{bmatrix} Z_1 & 1 & 0 & . & . & . & . & . & 0 \\ -1 & Y_2+Y_{ff2} & 1 & 0 & . & . & . & . & Y_2 \\ 0 & -1 & Z_3 & 1 & 0 & . & . & . & 0 \\ . & 0 & -1 & Y_4+Y_{ff4} & 1 & . & . & . & Y_4 \\ . & . & . & . & . & . & . & . & . \\ . & . & . & . & . & . & . & . & . \\ . & . & . & . & . & -1 & Y_{2N-4}+Y_{ff2N-4} & 1 & Y_{2N-4} \\ . & . & . & . & . & 0 & -1 & Z_{2N-3} & 0 \\ . & . & . & . & . & 0 & 0 & -1 & Y_{2N-2} \end{bmatrix} \begin{bmatrix} i_1 \\ e_2 \\ i_3 \\ e_4 \\ . \\ . \\ e_{2N-4} \\ i_{2N-3} \\ e_{2N} \end{bmatrix}$$

Fig. 3



Multiple-loop feedback system with feed-forward.

Evaluating the appropriate co-factors yields the voltage transfer function:

$$G_{21} = -\frac{e_{2N-2}}{e_0} = \frac{(-1)^{2N-1} + \sum_{i=1}^{N-1} Y_{ff2i}(Z_1 \text{——} Z_{2i-1}) \oplus (Y_{ff2} \text{——} Y_{ff(2i-2)}) \times (-1)^{2N-2i+1}}{(Z_1 \text{——} Y_{2N}) \oplus (Y_{ff2} \text{——} Y_{ff(2N-4)})}$$

For a double ladder the expression is:

$$G_{21} = \frac{(-1)^{2N-1} + \sum_{i=1}^{N-1} Y_{ff2i}(Z_1 \text{——} Z_{2i-1}) \oplus \begin{Bmatrix} (Y_{23} \text{——} Y_{(2i-2)(2i-1)}) \\ (Y_{ff2} \text{——} Y_{ff(2i-2)}) \end{Bmatrix} (-1)^{2N-2i+1}}{(Z_1 \text{——} Y_{2N}) \oplus \begin{Bmatrix} (Y_{23} \text{——} Y_{(2N-2)(2N-1)}) \\ (Y_{ff2} \text{——} Y_{ff(2N-4)}) \end{Bmatrix}}$$

7. Conclusions

Computer programmes have been written using the algebra of accumulants, and have been found to be fast and accurate. The main advantage of accumulants is that partial derivatives can be computed with ease, thus presenting an ideal analysis method for inclusion in iterative synthesis. The derivatives are also of value in sensitivity work.

The splitting technique enables a large structure to be dissociated into a number of small analysis problems and thus alleviating the demand for large storage on a machine at any particular instant.

The method is also suitable for literal analysis by computer.

Acknowledgments

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PAPER 13

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Active circulator systems†

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A general method for interconnecting active circulators is described. Various circuits which are derived from the general system possess properties which are of significance in active filter synthesis.

1. Introduction

It has been demonstrated recently (Rollett 1968) how versatile active multi-port circulators can be, when used in conjunction with resistors and capacitors to produce active filter networks. This communication attempts to establish a general interconnection system for multi-port circulators.

2. General configuration

Consider the following system :

$$Gc_i = S_i^r \Big] Gc_{i-1} \Big[S_i^l + \sum_{j=1}^{n_i} \Big\{ S_{ij}^r \Big] \alpha_{ij} K_{ij} Gcc_{ij} K_{ij} \Big[S_{ij}^l \Big\},$$

$i = 1 \ldots n$.

Gc_n overall circulator admittance matrix. It is skew-symmetric and of order m_n. $Gc_0 = 0$. n is the number of parallel systems.

Gcc_{ij} individual admittance matrix of the jth circulator in the ith path, order m_{ij}.

n_i number of individual circulators in the ith parallel path.

K_{ij} phase relation matrix. In order to specify the phase relationship between the ports of a circulator, the basic phase pattern of an odd order circulator is assumed for the Gcc_{ij} matrix. The K_{ij} matrix is a diagonal one containing $+1$, -1 and written as $\{1, -1 \ldots 1\}$, it is also of order m_{ij}.

α_{ij} a constant which determines the circulation sequence and assumes the value $+1$ or -1 according to whether the circulator exhibits a positive or negative sequence respectively.

The constants S are shift parameters used to maintain correct order and sequence in the matrix addition. Their value determines how many unconnected nodes (zero rows and columns) are to be added into the matrix.

S_i^r indicates a shift of the Gc_{i-1} matrix to the right, i.e. zero rows and columns added to the left-hand side of Gc_{i-1}.

S_i^l indicates a left shift of Gc_{i-1}.

S_{ij}^r, S_{ij}^l are similarly defined but operate on the Gcc_{ij} matrix.

† Communicated by the Author.

To prevent the generation of a singular set of system equations the following constraints must be obeyed :

$$S_1^{r}{}_{,\,j+1} = S_{1j}{}^{l} = \max\,(m_{1,\,j+1} :\ m_{1j}) - 1,$$

$$S_i{}^{r} \leqslant (m_{i1} - 1),\ S_i{}^{l} \leqslant (m_{i\,m_i} - 1).$$

The equation given above will generate a large number of possible ways to connect circulators. Some of these have relevance in practical systems : the ones discussed subsequently represent a few of significance.

2.1. *Two circulators in parallel, one of negative circulation sequence*

$n = 2$, $n_1 = 1$, $n_2 = 1$, $K_{11} = K_{21} = I$ (I = identity matrix. The circulators are of odd order and assumed equal) $\alpha_{11} = +1$, $\alpha_{21} = -1$,

$$S_2{}^{r} = S_2{}^{l} = S_{11}{}^{r} = S_{11}{}^{l} = S_{21}{}^{r} = S_{21}{}^{l} = 0 :$$

$$G_{c_2} = g_{cc_{11}} \begin{bmatrix} 0 & 1 & -1 & \dots & -1 \\ -1 & 0 & 1 & \dots & 1 \\ 1 & -1 & 0 & \dots & -1 \\ \cdot & \cdot & \cdot & \dots & \cdot \\ \cdot & \cdot & \cdot & \dots & \cdot \\ 1 & -1 & 1 & \dots & 0 \end{bmatrix} + g_{cc_{21}} \begin{bmatrix} 0 & -1 & 1 & \dots & 1 \\ 1 & 0 & -1 & \dots & -1 \\ -1 & 1 & 0 & \dots & 1 \\ \cdot & \cdot & \cdot & \dots & \cdot \\ \cdot & \cdot & \cdot & \dots & \cdot \\ -1 & 1 & -1 & \dots & 0 \end{bmatrix}.$$

This is an interesting configuration, as it represents a circulator with a reduced circulation conductance. Since inductors produced by these systems are inversely proportional to the circulation conductance squared, this system presents a method of producing increased inductance values without loss of Q. With a single circulator, reduction in Q occurs with reduction in g_c because the effects of amplifier parameters are no longer negligible.

With $g_{cc_{11}} = g_{cc_{21}}$ a null matrix results, giving rise to a singular system of little significance. For $g_{cc_{11}} > g_{cc_{21}}$ a circulator of positive sequence and reduced conductance is obtained ; similarly for $g_{cc_{21}} > g_{cc_{11}}$ one of reduced conductance but negative sequence results. In normal applications (i.e. impedance inversion) the two latter produce identical results.

Practical investigations of this reduced conductance property have been carried out, using third-order (3-port) circulators containing operational amplifiers (Rollett and Greenaway 1968). Encouraging results have been obtained, although care has to be exercised in selecting the resistances which determine the g_{cc} of the individual circulators.

Another interesting aspect of this configuration is the prospect of producing a balanced circulator from two unbalanced ones. The matrix of a balanced circulator is skew-symmetric with identical entries ; if, however, the circulator is unbalanced but still reciprocal between the ports, the matrix remains skew-symmetric but the entries are not equal. A second circulator may be used in the above connection to ensure identical conductances at, and between, all the ports.

2.2. *Two circulators in parallel, one of negative sequence, and 1-port overlap*

The significance of this connection is demonstrated simply using third-order circulators :

$n=2,\ m_1=3,\ n_1=1,\ n_2=1,\ m_2=3,\ K_{11}=I,\ K_{21}=I,\ \alpha_{11}=+1,\ \alpha_{21}=-1,$

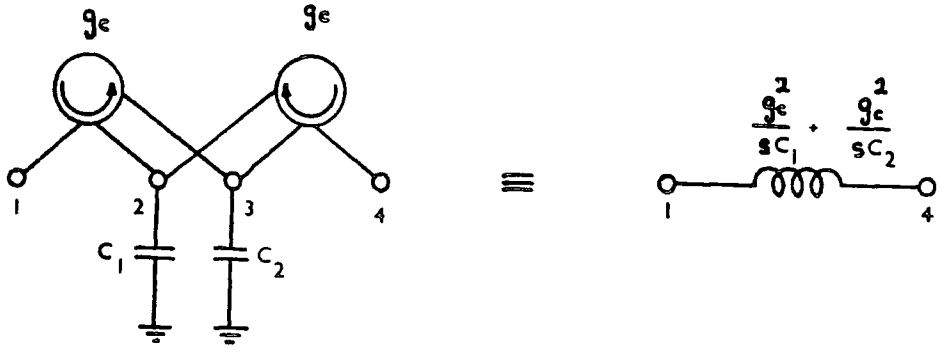
$S_{11}{}^r=S_{11}{}^l=0,\ S_2{}^r=0,\ S_2{}^l=1,\ S_{21}{}^l=0,\ S_{21}{}^r=1:$

$$G_{c_2}=g_{cc_{11}}\left[\begin{array}{ccc:c} 0 & 1 & -1 & 0 \\ -1 & 0 & 1 & 0 \\ 1 & -1 & 0 & 0 \\ \hdashline 0 & 0 & 0 & 0 \end{array}\right]+g_{cc_{21}}\left[\begin{array}{c:ccc} 0 & 0 & 0 & 0 \\ \hdashline 0 & 0 & -1 & 1 \\ 0 & 1 & 0 & -1 \\ 0 & -1 & 1 & 0 \end{array}\right].$$

If $g_{cc_{11}}=g_{cc_{21}}=g_c$ and capacitors are connected across ports 2, 3 as indicated in the figure, the admittance matrix becomes

$$\left[\begin{array}{cccc} 0 & g_c & -g_c & 0 \\ -g_c & sC_1 & 0 & g_c \\ g_c & 0 & sC_2 & -g_c \\ 0 & -g_c & g_c & 0 \end{array}\right]$$

Eliminating nodes 2, 3 from this matrix by pivotal condensation reveals a floating inductor between nodes 1, 4, and hence a method for producing an ungrounded inductor from two grounded capacitances.



Realization of a floating inductance from two grounded capacitances.

3. Conclusions

There are many possible configurations which remain to be investigated, the few shown here demonstrate interesting effects which result from interconnected circulators. One higher order combination examined has the parameters :

$$n=2,\ n_1=1,\ m_1=4,\ n_2=1,\ m_2=3,\ K_{21}=I,\ \alpha_{11}=+1,\ \alpha_{21}=+1,$$
$$K_{11}=\{1,\ 1,\ -1,\ -1\},\ S_{11}{}^r=S_{11}{}^l=S_2{}^r=S_2{}^l=0,\ S_{21}{}^r=0,\ S_{21}{}^l=1.$$

This circuit demonstrates an improved circulation conductance for one section of the resultant circulator. It may be of use in higher-order circulator filter networks. With the higher-order configurations attention to the phase relation matrices is necessary to maintain stability.

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PAPERS 14 + 15

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Symbolic Analysis for Computer-Aided Circuit Design—The Interpolative Approach

J. K. FIDLER AND J. I. SEWELL

Abstract—Symbolic analysis using direct matrix and interpolation-formula methods are discussed. The techniques accommodate passive networks and active networks containing general frequency-dependent devices, themselves represented by rational-function matrices. Subsequently, this leads to the development of partitioned analysis. The suppression of numeric common factors and the determination of the order of complexity of the network are synonymous problems, and simple algorithmic solutions emerge. Simple rules for the choice of sample points leading to accurate analysis are given. Implementation yields a very fast computer-analysis method capable of accuracies comparable with other current techniques.

INTRODUCTION

THE INCREASED application of the computer in designing electrical networks has emphasized the need for efficient analysis programs which are particularly useful in iterative synthesis. In this area of work, symbolic analysis, in which the network functions are obtained as functions of s, the complex frequency variable, with either literal or numeric coefficients, becomes quite attractive.

The traditional approach to symbolic network analysis using topological techniques has the inevitable time-consuming tree-generation problem for nontrivial networks. The straightforward manipulation of polynomial matrices is also unsatisfactory due to the generation of common factors [1], [2], although progress has been made in suppressing these [3], [4]. Eigenvalue techniques [5] also offer much promise in this area. Interpolative symbolic analysis, originally proposed for passive networks [1], [6], [7], presents an alternative approach. This technique involves the determination of the coefficients of the describing polynomials by subjecting the network to random excitations which lead to either the inversion of a purely numeric matrix or the evaluation of an interpolation formula. The computer implementation provides a very fast analysis.

In the analysis of real active networks, device modeling presents a complex problem. However, provided the device can be regarded as linear, a matrix can always be made to fit the device characteristics, although in general this matrix will contain symbolic rational-function entries.

FORMULATION OF SYNTHETIC ANALYSIS

The general network to be considered contains resistors, capacitors, inductors, and general active devices. A general active element is one which may have any degree of frequency dependence and can itself only be described by a symbolic rational-function matrix. An entry of the nodal admittance matrix Y will have the form

$$y_{ij}(s) = \frac{n_{ij}(s)}{d_{ij}(s)}.$$

Suppression of the internal nodes will yield a terminal matrix Y^r with entries

$$y^r_{ij}(s) = \frac{n^r_{ij}(s)}{d^r_{ij}(s)}$$

where r signifies a reduced matrix. The problem then is to determine the coefficients of these polynomials.

A fundamental theorem of algebra states that a polynomial of mth degree is uniquely defined by the value at $m + 1$ values of its argument. Thus if a network matrix determinant or cofactor is evaluated at $m + 1$ frequencies, the resultant determinant values completely define the corresponding mth-degree network-function polynomial. If a sample value k_p (complex) is substituted for s in Y, $y_{ij}(k_p)$ will have a finite complex value and application of pivotal condensation to this matrix will reduce it to an appropriate size $Y^r(k_p)$ evaluated at k_p. This process is repeated for $m + 1$ frequencies $s = k_p$, $p = 0 \cdots m$, where m is the maximum order of the polynomials in the final reduced matrix.

If $F(s) = a_m s^m + a_{m-1} s^{m-1} + \cdots + a_1 s + a_0$, then

$$[K][A] = [\Delta] \tag{1}$$

where $[\Delta]$ is a vector of functional values, $[A]$ is a vector of the required coefficients, and $[K]$ is the $(m + 1) \times (m + 1)$ Vandermonde matrix of sample points.

By exploiting the standard form of the Vandermonde matrix, a solution for the coefficient vector may be obtained directly from

$$[A] = [K]^{-1}[\Delta]. \tag{2}$$

An algorithm by Traub [8] has been used for the inversion of $[K]$ and it provides a fast and, for samples within certain bounds, accurate solution. The numerators and denominators of the rational functions of the reduced matrix are assembled by repeating this process.

The main advantage which accrues from such a strategy is that once $[K]$ has been inverted, it may be used for a variety of analyses, providing the sample frequencies chosen remain the same. A second point is that the accuracy of the inverse matrix can be improved subsequently at will. By using an

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iterative technique [9] for a small number of cycles (not more than 6), improvements of 3–4 orders of magnitude in the error of the inverse, for matrices of up to order 30, have been achieved. The only drawback is the increase in time required for this extra process, the overall analysis time being more than doubled.

A second method can be derived by manipulation of (1) to give the Lagrange interpolation formula [10]:

$$F(s) = \sum_{r=0}^{m} \left\{ \Delta(k_r) \prod_{\substack{i=0 \\ i \neq r}}^{m} \left[\frac{(s - k_i)}{(k_r - k_i)} \right] \right\}. \tag{3}$$

For ease of computation in either (2) or (3) it would seem reasonable to assign real values to the sample frequencies k_i, and hence, only real arithmetic is required throughout. Several workers have adopted this latter approach [7], but it has been the experience of the present authors that while, in some cases, satisfactory results may be obtained, there are situations where the error introduced into the coefficients becomes significant to the extent that in certain examples the results are totally meaningless. The error incurred is found to be quite sensitive to the locations of the sample frequencies on the real axis. This may be shown as follows:

Let

$$\Delta(k_i) = \Delta(k_0) + \epsilon_i, \epsilon_0 = 0$$

where the quantities ϵ_i indicate the difference between the ith determinant value $\Delta(k_i)$ and a reference value, arbitrarily assigned to $\Delta(k_0)$.

Equation (3) now becomes

$$F(s) = \sum_{r=0}^{m} \left\{ \Delta(k_0) \prod_{\substack{i=0 \\ i \neq r}}^{m} \left[\frac{(s - k_i)}{(k_r - k_i)} \right] \right\} + \sum_{r=0}^{m} \cdot \left\{ \epsilon_r \prod_{\substack{i=0 \\ i \neq r}}^{m} \left[\frac{(s - k_i)}{(k_r - k_i)} \right] \right\}. \tag{4}$$

The first term on the right-hand side of (4) expresses the interpolation of a constant function, and therefore must contribute to the a_0 coefficient. The remaining coefficients a_i are thus solely determined by the second term in (4). The indication is therefore that the coefficients a_i rely mainly on the differences between determinant values ϵ_i, and if these differences are of the same order as the roundoff error incurred in the determinant computation, gross coefficient error will ensue. The sample frequencies should therefore be chosen at the points where the network function is undergoing change, that is, in active areas of the s-plane.

In the general case, the computation of (2) or (3) for complex samples may seem somewhat daunting; however, if the samples are chosen in as many complex-conjugate pairs as possible, the property of network functions that $\Delta(\bar{s}) = \overline{\Delta(s)}$ may be recognized, the bar denoting complex conjugate. Thus the number of determinant evaluations will be reduced, requiring $\frac{1}{2}(m + 1)$ for m odd and $((m/2) + 1)$ for m even. Taking m as odd, (3) becomes

$$F(s) = \sum_{r=0}^{(m-1)/2} \left[\left\{ R_e[\Delta(k_r)] + \frac{(s + \sigma_r)}{\omega_r} I_m[\Delta(k_r)] \right\} \prod_{\substack{i=0 \\ i \neq r}}^{(m-1)/2} \cdot \left\{ \frac{s^2 + 2\sigma_i s + \sigma_i^2 + \omega_i^2}{(\sigma_r + \sigma_i)^2 - \omega_r^2 + \omega_i^2 + j2\omega_r(\sigma_r + \sigma_i)} \right\} \right]. \tag{5}$$

In the case of imaginary samples which have particular relevance in frequency-selective networks, further simplification is possible, giving, for m odd,

$$F(s) = \sum_{r=0}^{\frac{1}{2}(m-1)} \left[\left\{ R_e[\Delta(j\omega_r)] + \frac{s}{\omega_r} I_m[\Delta(j\omega_r)] \right\} \prod_{\substack{i=0 \\ i \neq r}}^{\frac{1}{2}(m-1)} \cdot \left\{ \frac{(s^2 - \omega_i^2)}{(\omega_i^2 - \omega_r^2)} \right\} \right]. \tag{6}$$

An equation for n even may be derived, but it is computationally more cumbersome. In practice, (6) is used for both m odd and even, in the latter case selecting the next highest (odd) integer for m. Although this overspecifies the interpolation, it is easily shown that the required number of determinant evaluations is not increased.

It will be noted that the only complex arithmetic required in (6) is that involved in the computation of the quantities $\Delta(j\omega_i)$. This is just the type of computation made in the more conventional discrete frequency analysis, and so techniques used in maintaining high accuracy in such calculations may be employed here. Since the limits in the summations and products of (6) have been roughly halved, error propagation will be further reduced.

It has been pointed out [11] that a similar reduction process can be derived for the direct inversion approach. If $F(s)$ is evaluated at sample value $+k_j$ giving Δ_j^+ and at $-k_j$ giving Δ_j^-, adding and subtracting the polynomial equations yields

$$z_j^{(1)} = \frac{\Delta_j^+ + \Delta_j^-}{2} = \sum_{i=0}^{\lfloor (m-1)/2 \rfloor} a_{2i} k_j^{2i} \tag{7}$$

$$z_j^{(2)} = \frac{\Delta_j^+ - \Delta_j^-}{2k_j} = \sum_{i=0}^{\lfloor m/2 \rfloor} a_{2i-1} k_j^{2i-2}. \tag{8}$$

Taking $m + 1$ distinct samples, (7) and (8) become

$$[Z^{(1)}] = [K^{(1)}][A^{(1)}]$$

$$[Z^{(2)}] = [K^{(2)}][A^{(2)}]$$

where $[A^{(1)}]$ and $[A^{(2)}]$ are column vectors of even and odd coefficients, respectively, and $[K^{(1)}]$ and $[K^{(2)}]$ are Vandermonde matrices of samples.

When m is odd, $[K^{(1)}] = [K^{(2)}]$, and when m is even, this identity can be assured by increasing m by unity. Hence,

$$[A^{(1)}] = [K^{(1)}]^{-1}[Z^{(1)}]$$

$$[A^{(2)}] = [K^{(1)}]^{-1}[Z^{(2)}].$$

The Vandermonde matrix is approximately half the size ($(m + 1)/2$, m odd; $(m/2) + 1$, m even) of that required in (2), and again, only one inversion is required. If imaginary samples

are used, $\Delta(-j\omega) = \overline{\Delta(j\omega)}$, then $[Z^{(1)}]$ and $[Z^{(2)}]$ can be formed with half the number of determinant evaluations.

As the samples in $[K^{(1)}]$ are now either all positive or negative, this contravenes the rules for maximum accuracy as described later, although halving the order does improve the accuracy.

Evaluation of Sampled Responses and Order of Complexity

In the work on passive networks [1], [6], [7] the nodal matrix was considered as a polynomial matrix. Now, however, a general element of $Y(s)$ consists of a numerator and denominator polynomial which independently contribute to $n'_{ij}(s)$ and $d'_{ij}(s)$; hence, it is necessary to retain the individual numeric values $n_{ij}(k_p)$ and $d_{ij}(k_p)$ for the same reason. If straightforward reduction is now used to determine $\Delta(k_p)$, then difficulties will arise due to the buildup of numeric common factors. It is obvious that these common factors occur for the same reasons as the algebraic ones in the inversion of matrices in symbolic analysis [4], and an adaptation of the factor suppression techniques used in that work is appropriate here.

A new term at any stage in a pivotal condensation process is given by

$$y'_{ij} = \frac{n_{ij}n_{kk}d_{ik}d_{kj} - n_{ik}n_{kj}d_{ij}d_{kk}}{d_{ij}d_{kk}d_{ik}d_{kj}} \cdot \frac{d_{kk}}{n_{kk}}$$

where k is the pivot node. Now d_{kk} cancels; hence,

$$n'_{ij} = n_{ij}n_{kk}d_{ik}d_{kj} - n_{ik}n_{kj}d_{ij}d_{kk} \qquad d'_{ij} = d_{ij}d_{ik}d_{kj}n_{kk}.$$

A further stage of reduction gives

$$n''_{ij} = n'_{ij}n'_{k-1,k-1}d'_{i,k-1}d'_{k-1,j} - n'_{i,k-1}n'_{k-1,j}d'_{ij}d'_{k-1,k-1}$$

$$d''_{ij} = d'_{ij}d'_{i,k-1}d'_{k-1,j}n'_{k-1,k-1}.$$

Forming the quotient $y''_{ij} = n''_{ij}/d''_{ij}$ reveals a considerable cancellation of terms. First, a change in subscript k to $k+1$ and $k-1$ to k aids computer formulation; if y_{kk} is the current pivot, then

1) the pivotal denominator d_{kk} always cancels;
2) the previous pivotal numerator $n_{k+1,k+1}$ cancels;
3) the terms $d_{i,k+1}$, $d_{k+1,j}$, $d_{k+1,k}$, and $d_{k,k+1}$ cancel.

This leads to the following reduction algorithm:

$$n'_{ij} = (n_{ij}n_{kk}d_{ik}d_{kj} - n_{ik}n_{kj}d_{ij}d_{kk})/(n_{k+1,k+1}d_r)$$

$$d'_{ij} = d_{ij}d_{ik}d_{kj}/d_r$$

where

$$d_r = d_{i,k+1}d_{k+1,j}d_{k+1,k}d_{k,k+1}.$$

The nodes are usually ordered such that the suppression process selects the largest value of k for the first pivot. Then the initial conditions are $n_{k+1,k+1} = 1$ and operations involving d_r do not take place. After the final step of reduction, it is necessary to multiply the denominators d_{ij} by $n_{k\ \min\ k\ \min}$, as the n_{kk} factor in the formation of d'_{ij} has been suppressed in anticipation of cancellation at the next stage, which of course does not occur.

Obviously, numeric common factors in themselves do not lead to problems as severe as those arising from algebraic ones, but they are directly related to the latter in connection with the calculation of the polynomial order, which must be evaluated precisely. In the absence of a satisfactory method for calculating the order of complexity of networks containing complex (rational-function) active devices, an algorithm has been developed to determine m from the known orders of the polynomial in the nodal matrix. The basic order of the polynomials in the data is stored in an integer array of equivalent dimensions to the nodal rational-function array. At each stage of the pivotal reduction, simple manipulation of the integer array will yield the order of the required polynomials.

Program Operation

Programs utilizing both approaches have been written and used on an ICL 1905 E and a PDP-10 in both batch process and conversational modes. Considerable experience has been gained in the analysis of both active and passive networks using these techniques. Polynomials, with wide-ranging coefficients, of order up to 39 are currently being generated with coefficients accurate to at least 4 significant figures. To compute the complete 2 × 2 admittance matrix in rational form for a fourth-order active multiloop circuit takes 3 s and a seventh-order passive elliptic filter ($\theta = 60°$) takes 7 s with a loss of only 1 significant figure. A better than 50-percent improvement in time over the conventional techniques was obtained in the analysis of a network yielding a third/fourth-order rational transfer function when evaluated at only 8 frequency points.

The accuracy of the results is controlled to a large extent by the choice of samples. The conjugate pair $j\omega$-axis interpolation formula has been found to be relatively insensitive to this choice owing to the reduced computational effort required. In some cases it has been found that samples distributed evenly over both sides of the real or imaginary axis yield optimum results. This may be a good default choice when more specific information is not available concerning the approximate behavior of the circuit undergoing analysis.

In the matrix implementation, the sample-point selection controls the accuracy of inversion of the Vandermonde matrix. In Traub's method [8] the samples are always considered as symmetrical, and practice has shown that for both real and imaginary samples this criterion is again required. It has been found that as the order of the functions increases, the need to choose sensible sample points increases too.

Partitioned Analysis

In the iterative synthesis situation there may be sections of the network whose parameters are constant throughout the optimization routine, and therefore it seems redundant to repeat the analysis of these sections at each step of iteration. Decomposing the networks into sections provides a solution to this and to the problem of large networks beyond the scope of a medium-sized computer. Another problem is that active devices quite often have large-gain parameters which in

straightforward reduction cause numerical overflow after a number of steps. A solution is provided by appropriate choice of subnetworks ensuring suitable embedding for the active elements. A similar reason for choosing a partition to improve the analysis occurs when the network has widely ranging element values.

This symbolic analysis method can be adapted for partitioned analysis; as the results of one analysis are in rational-function form, these may be used as data for further analyses. The procedure is to suppress all the internal nodes in each section using the methods outlined; the resultant rational matrices are then summed and the final nodes eliminated.

There is a limit to the number of partitions for optimum analysis, as there is obviously a point beyond which more effort is being expended in separating and recombining the network than in actual analysis. Networks having less than six nodes require more time for partitioned analysis. Studies indicate that an optimum also occurs when each partition contains approximately the same number of nodes. With some simple networks such as *RC* ladders with 20 nodes, experiments indicate up to 85-percent improvement in analysis time. Further, this technique allows a different choice of samples for each partition. Hence, one section can be analyzed using complex samples, another using an imaginary set, and yet another with a real set.

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Letters to the Editor

A Note on the Computation of Large-Change Sensitivities

TOM DOWNS

Abstract–A method of efficiently computing large-change sensitivities is described. The approach is more general than an existing method in that it is directly applicable to several network functions.

One measure of derivative sensitivity for a network function F with respect to a network element e is given by the following:

$$S_e^F = \frac{e\Delta F}{F\Delta e}. \tag{1}$$

First-derivative sensitivity is usually useful as a guide only in cases where very small changes in element values are made. For larger changes, we may define the finite-change sensitivity function

$$\delta_e^F = \frac{e\Delta F}{F\Delta e} \tag{2}$$

where ΔF is the change in F resulting from a finite change Δe in e.

It was shown recently [1] that if F is represented by the ratio N/D,

$$\delta_e^F = \frac{S_e^F}{1 + \Delta e D'/D} \tag{3}$$

where D' is the derivative of D with respect to e.

Equation (3) may be used to provide simple methods for the evaluation of the change ΔF in the network function F due to a finite change Δe in the network element e.

In [2], a method of computing the change in a response voltage due to a finite change in a network element was described. The network was current driven, and therefore the function of interest was transfer impedance. For a single input current flowing from the reference node into node k, the voltage at node m is given by

$$V_m = Z_{mk} = \frac{\Delta_{km}}{\Delta}$$

where Δ is the determinant of the nodal admittance matrix and Δ_{km} is

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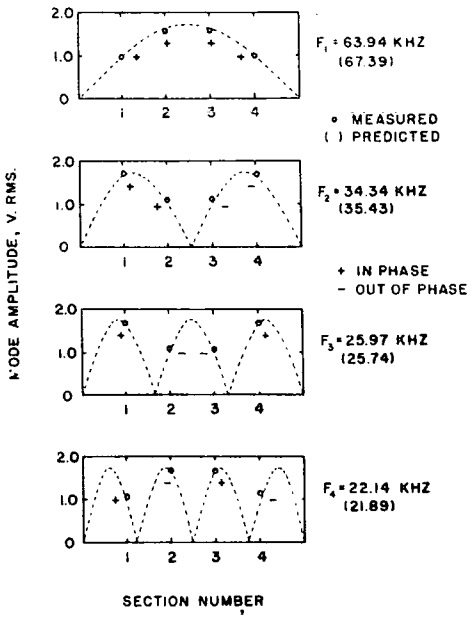

Fig. 2. Modes of a four-section ladder oscillator.

is substituted into (1). We avoid these cases, and at the same time satisfy (6) by choosing N such that $N + 1$ is a prime number.

These results were verified by constructing a ladder oscillator with $C = 1000$ pF, $L = 14.6$ mH, and using operational amplifiers and diodes to approximate $J(v_i)$. For $N = 4$, the individually observed standing wave patterns and mode frequencies, as shown in Fig. 2, were in close agreement with theoretical values obtained from (3), (4), and (7). All standing wave modes were observed for $N = 1$, 2, 4, and 6, i.e., for $N + 1$ a prime number, but not for $N = 3$, 5, 7, and 8.

The ladder oscillator presented here differs from other multimode oscillators [8], [9] in that its mode of oscillation can be ascertained from the relative phase of the node voltages without measuring the frequency. The oscillator has also been realized as an active RC circuit by replacing the inductors with gyrators and capacitors [10].

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Correction to "Symbolic Analysis for Computer-Aided Circuit Design—The Interpolative Approach"

J. K. FIDLER AND J. I. SEWELL

In the above paper,[1] on p. 739, (5) should be replaced with

$$F(s) = \sum_{r=0}^{(m-1)/2} \left[\left\{ \frac{(\mathrm{Im}\,[\Delta(k_r)]\,\mathrm{Re}\,[P_r] - \mathrm{Im}\,[P_r]\,\mathrm{Re}\,[\Delta(k_r)])(s - \sigma_r) + (\mathrm{Re}\,[\Delta(k_r)]\,\mathrm{Re}\,[P_r] + \mathrm{Im}\,[\Delta(k_r)]\,\mathrm{Im}\,[P_r])\omega_r}{\omega_r(\mathrm{Re}^2\,[P_r] + \mathrm{Im}^2\,[P_r])} \right\} \cdot \prod_{\substack{i=0 \\ i \neq r}}^{(m-1)/2} (s^2 - 2\sigma_i s + \omega_i^2) \right] \quad (5)$$

where

$$P_r = \prod_{\substack{i=0 \\ i \neq r}}^{(m-1)/2} \{(\sigma_r - \sigma_i)^2 + \omega_i^2 - \omega_r^2 + j2\omega_r(\sigma_r - \sigma_i)\}$$

and in (6) on the same page the minus sign between $(s^2 - \omega_i^2)$ should be plus, such that the last bracket of that expression reads $(s^2 + \omega_i^2)/(\omega_i^2 - \omega_r^2)$.

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[1] J. K. Fidler and J. I. Sewell, *IEEE Trans. Circuit Theory*, vol. CT-20, pp. 738–741, Nov. 1973.

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$$A_{n-2,3} = A_{n,2} + h_{n-2}A_{n-1,3} + H_{n-2}A_{n-1,2}$$
$$\vdots$$
$$A_{1n} = A_{3,n-1} + h_1 A_{2n} + H_1 A_{2,n-1}. \quad (24)$$

The general form for (24) is

$$A_{j,k} = A_{j+2,k-1} + h_j A_{j+1,k} + H_j A_{j+1,k-1},$$
$$j = n-1, n-2, \cdots, 1, \quad k = 2,3,\cdots,n+1-j. \quad (25)$$

Equations (21), (22), and (25) are used to obtain the continued fraction inversion.

V. Conclusion

Two general formulas have been derived for the continued fraction expansion and inversion of the Cauer third form. The algorithms established are the generalized Routh algorithm and these formulas are most appropriate to digital computer programs.

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Symbolic Analysis of Networks by Partitioned Polynomial Interpolation

C. FRIDAS AND J. I. SEWELL

***Abstract*—A method is given for improving the accuracy of the coefficients of network polynomials of high order produced by symbolic analysis on a computer. By partitioning the polynomials into sets of coefficients the order of the individual matrices involved is reduced and so is the error when these are inverted. The problem is reduced to the inversion of only two Vandermonde matrices. Considerable increases in accuracy are demonstrated.**

Introduction

AT THE present time there is considerable interest in symbolic analysis which generally implies the analysis of networks by computer to yield the characterization of the network functions as rational functions of the frequency variable s with numeric coefficients. Techniques evolved so far fall into the groups of topological, eigenvalue [1], matrix inversion [2], and interpolative methods [3], [4]. It is also possible to generate polynomials with literal coefficients and an efficient method for semiliteral analysis has recently been announced [5].

As the complexity of the network increases, so do the orders of the resultant polynomials, and the problem of coefficient accuracy arises. In fact, although the polynomial orders may be correct, gross coefficient errors are not uncommon when the system order exceeds fifteen.

One method which has been successfully applied to the analysis of high-order systems is to partition the network [6], and the results show improvement in accuracy and speed of analysis.

The technique to be described now involves polynomial partitioning in an attempt to increase accuracy and speed of symbolic analysis on a computer.

Polynomial Interpolation and Partitions

Following the interpolative approach [4] and considering any required polynomial

$$f(s) = a_0 + a_1 s + a_2 s^2 + \cdots + a_m s^m$$

subjecting the network to $m+1$ samples of the variable s, s_i (complex) will enable the coefficients a_i to be determined from

$$F = \sigma A \quad (1)$$

where A is the column vector of coefficients, F the column vector of sampled responses, and σ the $(m+1) \times (m+1)$ Vandermonde matrix of samples. A may be found by direct inversion or interpolation formulas. In direct inversion, error in the determination of A comes from two

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sources; first the evaluation of elements of F the control of which is discussed elsewhere, and second in the formation of σ^{-1}. There are numerous methods [7] which exploit the special form of the Vandermonde matrix to produce good inversion techniques; however, there is generally a tradeoff between speed and accuracy. It is apparent that as order increases, then both of these parameters suffer. It is also possible to improve the accuracy of the inverse using an iterative method [4], but again there is a penalty on speed.

Consider the system equation divided into p parts of equal order $h = (m + 1)/p$ such that $h \leq 15$. If h is not integer, add unity to the order, this only has the effect of producing a zero leading coefficient. Then for part q, (1) yields

$$\begin{bmatrix} f(s_i) \\ f(s_{i+1}) \\ \vdots \\ f(s_{i+h-1}) \end{bmatrix} = \begin{bmatrix} 1 & s_i & s_i^2 & \cdots & s_i^m \\ 1 & s_{i+1} & s_{i+1}^2 & \cdots & s_{i+1}^m \\ \vdots & \vdots & \vdots & & \vdots \\ 1 & s_{i+h-1} & s_{i+h-1}^2 & \cdots & s_{i+h-1}^m \end{bmatrix} \begin{bmatrix} a_0 \\ a_1 \\ \vdots \\ a_m \end{bmatrix}. \quad (2)$$

The sample matrix is not square since all the coefficients can only be determined with all the samples. However, on partitioning the coefficients into sets containing h each, (2) becomes

$$\begin{bmatrix} f(s_i) \\ f(s_{i+1}) \\ \vdots \\ f(s_{i+h-1}) \end{bmatrix} = \begin{bmatrix} 1 & s_i & s_i^2 & \cdots & s_i^{h-1} \\ 1 & s_{i+1} & s_{i+1}^2 & \cdots & s_{i+1}^{h-1} \\ \vdots & \vdots & \vdots & & \vdots \\ 1 & s_{i+h-1} & s_{i+h-1}^2 & \cdots & s_{i+h-1}^{h-1} \end{bmatrix} \begin{bmatrix} a_0 \\ a_1 \\ \vdots \\ a_{h-1} \end{bmatrix} + \begin{bmatrix} s_i^h & s_i^{h+1} & s_i^{h+2} & \cdots & s_i^{2h-1} \\ s_{i+1}^h & s_{i+1}^{h+1} & s_{i+1}^{h+2} & \cdots & s_{i+1}^{2h-1} \\ \vdots & \vdots & \vdots & & \vdots \\ s_{i+h-1}^h & s_{i+h-1}^{h+1} & s_{i+h-1}^{h+2} & \cdots & s_{i+h-1}^{2h-1} \end{bmatrix} \cdot \begin{bmatrix} a_h \\ a_{h+1} \\ \vdots \\ a_{2h-1} \end{bmatrix} + \cdots + \begin{bmatrix} s_i^{(p-1)h} & s_i^{(p-1)h+1} & s_i^{(p-1)h+2} & \cdots & s_i^m \\ s_{i+1}^{(p-1)h} & s_{i+1}^{(p-1)h+1} & s_{i+1}^{(p-1)h+2} & \cdots & s_{i+1}^m \\ \vdots & \vdots & \vdots & & \vdots \\ s_{i+h-1}^{(p-1)h} & s_{i+h-1}^{(p-1)h+1} & s_{i+h-1}^{(p-1)h+2} & \cdots & s_{i+h-1}^m \end{bmatrix} \cdot \begin{bmatrix} a_{(p-1)h} \\ a_{(p-1)h+1} \\ \vdots \\ a_m \end{bmatrix}$$

which can be rewritten as

$$F_q = \sigma_q A_0 + D_q^1 \sigma_q A_1 + \cdots + D_q^{p-1} \sigma_q A_{p-1}$$

where

D_i^k = diag $(s_i^{kh}, s_{i+1}^{kh}, \cdots, s_{i+h-1}^{kh})$

σ_q Vandermonde matrix of samples $s_i, s_{i+1}, \cdots, s_{i+h-1}$

A_k column vector of coefficients $a_k, a_{k+1}, \cdots, a_{k+h-1}$

F_q column vector of sampled responses $f(s_i), f(s_{i+1}), \cdots, f(s_{i+h-1})$.

Hence for $q = 0,1,\cdots,p-1$ and $i = qh + t, t = 0,1,\cdots, h-1$, (1) becomes

$$\begin{bmatrix} F_0 \\ F_1 \\ \vdots \\ F_{p-1} \end{bmatrix} = \begin{bmatrix} \sigma_0 & D_0^1\sigma_0 & D_0^2\sigma_0 & \cdots & D_0^{p-1}\sigma_0 \\ \sigma_1 & D_1^1\sigma_1 & D_1^2\sigma_1 & \cdots & D_1^{p-1}\sigma_1 \\ \vdots & & \vdots & & \vdots \\ \sigma_{p-1} & D_{p-1}^1\sigma_{p-1} & D_{p-1}^2\sigma_{p-1} & \cdots & D_{p-1}^{p-1}\sigma_{p-1} \end{bmatrix} \cdot \begin{bmatrix} A_0 \\ A_1 \\ \vdots \\ A_{p-1} \end{bmatrix}. \quad (3)$$

To solve for the coefficients a general matrix inversion routine would be required. However, if $D_q^k = b_q^k I$, I being the unit matrix and b_q^k some complex constant, then (3) becomes

$$F = \Sigma C A \quad (4)$$

where Σ = diag $(\sigma_0, \sigma_1, \cdots, \sigma_{p-1})$ and C is a modified Vandermonde matrix. The problem is the selection of samples such that (4) is invertible in a Vandermonde sense. Now the general element of D_q^k is s_r^{kh}; hence $s_r^{kh} = b_q^k$; take the kth positive root as $s_r^h = b_q e^{j2r\pi}$. Therefore $s_r = b_q^{1/h} e^{j(2r\pi/h)}, r = 0,1,\cdots, h-1$. One obvious solution is to locate these samples on a circle of radius $|b_q^{1/h}|$, giving $b_q = \rho_q^h e^{j\phi_q h}$, where ρ_q is the radius used for the set of coefficients q and ϕ_q is some initial angle for that same set. This yields a threefold choice in the method for determining $b_q \forall q$; the radius can be changed between coefficient sets, with ϕ_q constant, the initial set angle can be changed with ρ_q constant, and a mixture of these two can be used. Therefore a general entry of C is $D_q^k = \rho_q^{kh} e^{(j\phi_q kh)} I$, and it is possible to compute A from $A = C^{-1}\Sigma^{-1}F$ using Vandermonde matrix inversion only, as Σ^{-1} = diag $(\sigma_0^{-1}, \sigma_1^{-1}, \cdots, \sigma_{p-1}^{-1})$ and σ_i is Vandermonde too.

A still further improvement can be achieved. If the change in b_q is simple, then as the samples of σ_0 are $s_0, s_1, \cdots, s_{h-1}$ those of σ_q can be $k_q s_0, k_q s_1, \cdots, k_q s_{h-1}$ or $\sigma_q = \sigma_0 K_q$ where K_q = diag $(1, k_q, k_q^2, \cdots, k_q^{h-1})$, k_q being a complex quantity. Thus $\sigma_q^{-1} = K_q^{-1}\sigma_0^{-1}$ and Σ^{-1} can be obtained by inverting only one Vandermonde matrix.

This method has removed some degree of arbitrariness concerning the sample locations in the complex plane. Certain further constraints govern the choice of circular sample locations. Time savings can be made in computing the sampled responses when conjugate samples are used, and with ρ_q = constant $\forall_q$ this property can only be

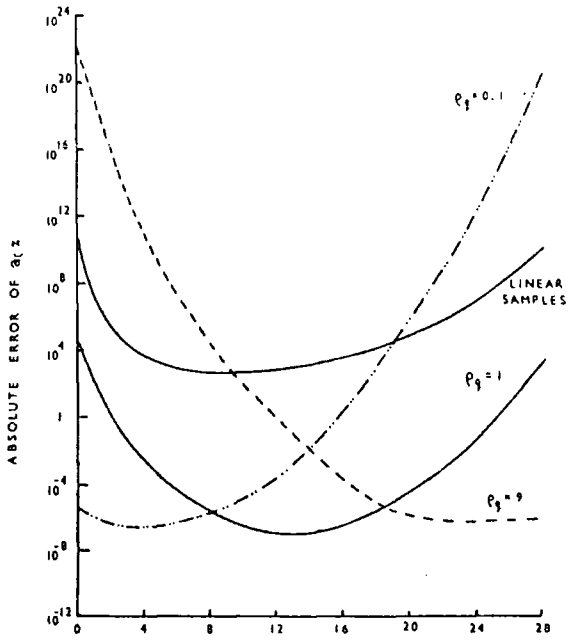

Fig. 1. Coefficient error distribution for a 29th-order polynomial.

realized when $\phi_q = 0$, which is restricted to one set of coefficients. On the other hand when $\phi_q = 0 \forall q$ and ρ_q is varied, then this property is true in each set. However, as is shown later, there is not complete liberty in varying ρ_q. Some compromise is obviously true for the variable ρ_q and ϕ_q situation.

Program Application

The technique can be used in the analysis of all the networks to which the interpolative approach has been applied, that is, passive networks and active ones containing general active devices with any order of frequency dependence. To investigate the accuracy of the method a 29th-order *RC* ladder was analyzed and the coefficients of one of the polynomials compared with those produced by a continuant method which can be assumed to produce maximum accuracy for such a network. With ρ_q constant and ϕ_q variable, Fig. 1 shows the coefficient error for complete analysis with different sample radii. With a relatively large radius large error occurs in the lower coefficients and the opposite is true for a small radius. Unity radius yields the medium-order coefficients to maximum accuracy. The coefficient errors for the straightforward matrix inversion with real samples is also shown for comparison. An improvement is obtained when one complete analysis is computed with $\rho_q = 1 + \delta$ ($\delta \ll 1$) and one with $\rho_q = 1 - \delta$, each contributing a set of coefficients with maximum accuracy. Useful results have been obtained with ϕ_q constant and ρ_q variable, but it is obvious that for maximum accuracy ρ_q can only be varied over a limited range of values.

TABLE I
Comparative Computer Program Requirements

NETWORK	PARAMETER	LINEAR SAMPLES	CIRCULAR SAMPLES WITH PARTITION
30-NODE	TIME (SECS.)	39	70
	STORE (WORDS)	21K	19K
40-NODE	TIME (SECS.)	72	113
	STORE (WORDS)	27K	22K

Table I shows relative time and storage requirements on an ICL 1905E. The linear samples correspond to samples on the real axis for the straightforward Vandermonde matrix inversion; computation time is for the complete $2 \times 2Y$ matrix. The trend of the graphs of Fig. 1 is applicable in these examples.

When the circular sample points are used, computation time is increased mainly because of the complex arithmetic. The main conclusion is that polynomial partitioning does improve the coefficient accuracy very significantly and also has the effect of reducing the storage requirement, but with some penalty in speed.

If polynomial partitioning is coupled with network partitioning it appears that the time and accuracy bounds for high-order networks can be successfully overcome.

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PAPER 19

Network partition methods for use in symbolic analysis by interpolation

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Symbolic analysis of networks of high order and complexity is not a straightforward process. The problems encountered are usually enormous demands for computer storage and time together with inaccurate results. A number of methods are presented which can drastically reduce the computer requirements and in some cases keep the computational error to a minimum. The principle of the methods is to partition the networks into a number of parts, and techniques of division and recombination are developed.

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In recent years a variety of techniques for the symbolic analysis of networks have been developed. These generally fall into the categories, topological, eigenvalue[1], matrix inversion[2], state space[3] and interpolative[4]. The analysis has been extended to produce polynomials with completely literal[5], semi-literal[5] and numerical coefficients in both passive and active networks. More recently[6], requirements in tolerance, statistical, and stability analysis have demanded the production of the whole inverse matrix. This is a more difficult problem to tackle generally, and the difficulties encountered with the symbolic analysis of large networks are sufficient to justify restricted attention to their solution alone although partition methods are of value in the above analysis areas. Any form of symbolic analysis will require more computer time than straightforward numerical methods, hence speed is a vital concern.

As the order of the network is increased, inevitable problems with the computer requirements for speed and storage are encountered. The computation error apparent in the results also gives considerable cause for concern. Some techniques have been developed which do improve the performance for higher order networks and these include partitioned polynomial interpolation[7] and use of the Fast Fourier Transform[8]. However, with large increase in network complexity, these difficulties still increase in severity and sparse matrix methods and network partition techniques[10] provide ways of tackling the problem.

The principle and advantages of partitioning large networks is not new and has been amply explored in frequency and time domain analysis since the early days of Kron. Not only can large networks be considered, but, especially in the case of electronic circuits such as integrated amplifiers in which many sections are duplicated, the symbolic solution of these circuits can be stored and called as required. Many networks are ill-conditioned, and by partitioning and suitable normalization, various difficult sections with drastic component difference from the norm can be accommodated. The application to symbolic analysis is not as straightforward as initially anticipated[9] because of the interruption of common factor suppression mechanisms[4]. However, the improvements due to partitioning can amount to 90% increases in speed for some networks and it would therefore seem necessary to overcome the effects which impede true partitioning in symbolic work.

One solution to the elimination of common factors on partition uses an artificial loading technique[10]. The methods outlined now obviate the need for any artificial elements.

NETWORK PARTITION

In Figure 1 let N represent a network with a nodal admittance matrix $\mathbf{Y}$; the sets S, I, E containing all internal and external nodes respectively, hence $S = I \cup E$. The nodes are numbered in such a way so that if $\lambda_i \in E$, and $\mu_j \in I$, then $\lambda_i < \mu_j \; \forall \; i, j$. Dividing N into d parts in an arbitrary way, N_i, $i = 1,2, \cdots, d$, then the sets S_i, I_i, E_i may be defined as for N. Clearly, $S_i \subset S$, $I_i \subset I$ and $E_i \subset I$, $\forall i$.

Let C_{ij} be a set defining the common nodes between N_i, N_j; thus $C_{ij} = E_i \cap E_j$. Define n, μ, ϵ as the total number of elements in S, I, E respectively, and similarly n_i, μ_i, ϵ_i for S_i, I_i, E_i.

A straightforward analysis of N can be achieved as indicated previously[4]. An improved condensation formula for evaluating the sampled responses is:

$$n'_{ij} = (n_{ij}n_{kk}d^0_{ik}d^0_{kj} - d^0_{ij}d^0_{kk}n_{ik}n_{kj})/n_{k+1,k+1}$$

$$d'_{ij} = d_{ij}\left(\prod_{l=k}^{n} d_{il}d_{lj}\right)\left(\prod_{g=k}^{n}\prod_{h=k}^{n} d^0_{gh}\right) \qquad (1)$$

where d^0_{gh} is the denominator of the gh entry of the nodal admittance matrix,

$$k = n, \; n-1, \; n-2, \cdots, \epsilon+1 \text{ and } i, j = 1, 2, \cdots, k-1$$

The terms n'_{ij}/d'_{ij} and n_{ij}/d_{ij} are the new and old numerator and denominator, entries of the admittance matrix. The pivotal condensation formula needs to be applied $n - \epsilon + 1$ times and the reduction procedure to be repeated for every sample point (a value of the complex frequency). Sparse

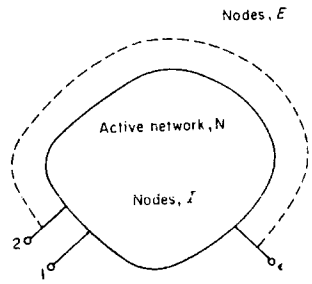

FIGURE 1. General network N

matrix methods and optimal ordering of pivots can be used at this stage to improve the accuracy.

When analysing a network by partition the network may be divided into an arbitrary number of parts, but for simplicity a two part division, Figure 2, is considered. Let N_A, N_B be the two subnetworks and y_{ij}^A, y_{ij}^B be the general entries of the nodal admittance matrices $\mathbf{Y}_A$ and $\mathbf{Y}_B$ respectively.

Thus, if y_{ij} is the general entry of $\mathbf{Y}$, then

$$y_{ij} = y_{ij}^A + y_{ij}^B$$

Similarly, the following relations are valid:

(a) $y_{ij}^A = 0\ \forall j$ and $i \in (S_B - C_{AB})$ with $i \leftrightarrow j$

(b) $y_{ij}^B = 0\ \forall j$ and $i \in (S_A - C_{AB})$ with $i \leftrightarrow j$

(c) y_{ij}^A, y_{ij}^B may take any values for $\{i, j\} \subset C_{AB}$

In cases (a) and (b) the entries of $\mathbf{Y}$ are formed entirely from N_B and N_A respectively, whereas for case (c) both subnetworks may contribute.

Set $y_{ij} = n_{ij}/d_{ij}$, then equation (2) becomes

$$\frac{n_{ij}}{d_{ij}} = \frac{n_{ij}^A}{d_{ij}^A} + \frac{n_{ij}^B}{d_{ij}^B},$$

$$n_{ij} = n_{ij}^A d_{ij}^B + n_{ij}^B d_{ij}^A,\ d_{ij} = d_{ij}^A d_{ij}^B \tag{3}$$

The first stage of analysis would be completed when all nodes in I_B are eliminated. Where

$$I_B = \{n,\ n-1,\ n-2, \cdots n - \mu_B + 1\}$$

Using the entries given by equation (3) in the reduction formula gives:

$$n'_{ij} = (n_{ij}^A d_{ij}^B + d_{ij}^A n_{ij}^B) n_{nn} d_{in} d_{nj} - (d_{ij}^A d_{ij}^B) d_{nn} n_{in} n_{nj},$$

$$d'_{ij} = (d_{ij}^A d_{ij}^B) d_{in} d_{nj}.$$

But,

$$y_{ik}^A = y_{kj}^A = 0\ \forall i,j \text{ for } k \in I_B.$$

Thus,

$$y_{ik} = y_{ik}^B \text{ and } y_{kj} = y_{kj}^B.$$

Re-arranging equation (3) gives

$$\frac{n'_{ij}}{d'_{ij}} = \frac{n_{ij}^A}{d_{ij}^A} n_{nn}^B + \frac{n_{ij}^{'B}}{d_{ij}^{'B}},\ i, j = 1, 2, \cdots, n-1$$

Next, elimination of node $n-1$ produces

$$\frac{n''_{ij}}{d''_{ij}} = \frac{n_{ij}^A}{d_{ij}^A} n_{n-1,n-1}^{'B} + \frac{n_{ij}^{''B}}{d_{ij}^{''B}},\ i, j = 1, 2, \cdots, n-2 \tag{4}$$

Clearly, for k node eliminations, $\{n, n-1, n-2, \cdots, n-k+1\} \subset I_B$, equation (4) would be of the form

$$\frac{n_{ij}^k}{d_{ij}^k} = \frac{n_{ij}^A}{d_{ij}^A} (n_{n-k+1,n-k+1}^{k-1})^B + \frac{(n_{ij}^k)^B}{(d_{ij}^k)^B},\ i, j = 1, 2, \cdots, n-k \tag{5}$$

When all the internal nodes of N_B are eliminated, the intermediate state of the semi-reduced system has the form:

$$\mathbf{Y}_I = \mathbf{Y}_A p_B + \mathbf{Y}_B^r \tag{6}$$

where $\mathbf{Y}_I$ is an intermediate admittance matrix, $\mathbf{Y}_B^r$ the reduced matrix of $\mathbf{Y}_B$ and p_B the last previous pivotal numerator, i.e.

$$p_B = (n_{n-k+1,n-k+1}^{k-1})^B.$$

An important observation is that equation (5) may also be produced by analysing N_B independently and computing p_B.

The next stage of analysis may be executed by eliminating the internal nodes I_A, which is the set $I_A = \{n - \mu_B, n - \mu_B - 1, \cdots, n - \mu_B - \mu_A + 1\}$. On eliminating the kth node in I_A, $n - \mu_B - k + 1$, the new matrix entries are given by:

$$\frac{n_{ij}^{\mu_B+k}}{d_{ij}^{\mu_B+k}} = \left(\frac{n_{ij}^k}{d_{ij}^k}\right)^A p_B + \left(\frac{n_{ij}^{\mu_B}}{d_{ij}^{\mu_B}}\right)^B (n_{n-k+1,n-k+1}^{k-1})^A \tag{7}$$

$i, j = 1, 2, \cdots, n - \mu_B - k.$

On eliminating all the nodes in I_A, we have

$$\frac{n_{ij}^{\mu_B+\mu_A}}{d_{ij}^{\mu_B+\mu_A}} = \left(\frac{n_{ij}^{\mu_A}}{d_{ij}^{\mu_A}}\right)^A p_B + \left(\frac{n_{ij}^{\mu_B}}{d_{ij}^{\mu_B}}\right)^B p_A \tag{8}$$

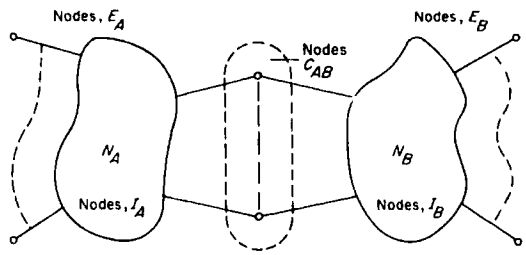

FIGURE 2. Two part division networks

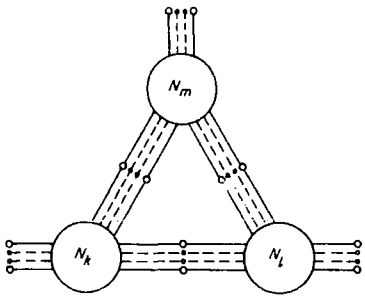

FIGURE 3. General partition structure

where

$$p_A = (n^{\mu_A - 1}_{n-\mu_A+1, n-\mu_A+1})^A$$

the last pivotal numerator.

The new intermediate system, derived from equation (8), would then be of the form

$$\mathbf{Y}'_I = \mathbf{Y}^r_A p_B + \mathbf{Y}^r_B p_A \tag{9}$$

with $P = p_A p_B$ the (dummy) last pivotal numerator, $\mathbf{Y}'_I$ is a new admittance matrix.

The third and final stage may be concluded by eliminating all the interconnecting nodes, C_{AB}, using the full reduction formula. On completion the required terminal matrix $\mathbf{Y}^r$ is produced in symbolic form.

The procedure may be generalized for the multiple partition structure as displayed in Figure 3. Assume a d part division of N and let N_1 be the first subnetwork to be selected. With $\mathbf{Y}^1_I$ as the first intermediate matrix and analysing N_i independently, the following system may be constructed

$$\mathbf{Y}^1_I = \mathbf{Y}^r_1 + p_1 \sum_{i=2}^{d} \mathbf{Y}_i \tag{10}$$

where p_1 is the last pivotal numerator of the analysis of N_1.

Rearranging equation (10) gives

$$\mathbf{Y}^1_I = \left(\mathbf{Y}^r_1 + p_1 \sum_{i=3}^{d} \mathbf{Y}_i\right) + p_1 \mathbf{Y}_2.$$

Selecting N_2 as the next subnetwork, analysis will yield

$$\mathbf{Y}^2_I = \left(\mathbf{Y}^r_1 + p_1 \sum_{i=3}^{d} \mathbf{Y}_i\right) p_2 + p_1 \mathbf{Y}^r_2$$

with $P = p_1 p_2$ as the last (dummy) pivotal numerator.

Rearranging

$$\mathbf{Y}^2_I = \mathbf{Y}^r_1 p_2 + \mathbf{Y}^r_2 p_1 + p_1 p_2 \sum_{i=3}^{d} \mathbf{Y}_i.$$

Generally, after analysis of the kth part, the system may be given by

$$\mathbf{Y}^k_I = P_k \sum_{i=1}^{k} \frac{\mathbf{Y}^r_i}{p_k} + P_k \sum_{i=k+1}^{d} \mathbf{Y}_i \tag{11}$$

where

$$P_k = \prod_{i=1}^{k} p_i \text{ and } k = 1, 2, \cdots, d-1.$$

When $k = d - 1$, the last intermediate matrix is given by

$$\mathbf{Y}^{d-i}_I = P_{d-1} \sum_{i=1}^{d} \frac{\mathbf{Y}^r_i}{P_i} \tag{12}$$

Elimination of all the interconnecting nodes results in $\mathbf{Y}^r$.

Therefore in general, for network partition purposes, a network may be described by its symbolic terminal matrix and its last pivotal numerator. Once these two parameters are known, subnetworks may be considered arbitrarily and the analysis procedure yields a solution without the normal common factors.

POLYNOMIAL INTERCONNECTION METHODS

Double coupling

The principle of this partition method is to select one subnetwork, and perform symbolic analysis. Then select a new one, analyse this, and combine the two independent solutions. The resultant interconnected system may be analysed by eliminating all the interconnecting nodes between the two parts. The result is the symbolic terminal matrix of the network consisting of these two subnetworks. A third part is selected and the process is repeated. This iterative method may be described by

$$\mathbf{H}_{k+1} = \mathbf{H}^r_k p_{k+1} + P_k \mathbf{Y}^r_{k+1} \quad k = 1, 2, \cdots, d-1,$$

$$\mathbf{H}_1 = \mathbf{Y}_1,$$

where $\mathbf{H}_k$ is the admittance matrix of the kth interconnected system, $\mathbf{H}^r_k$ is the reduced matrix and p_k the last pivotal numerator.

When $k = d - 1$,

$$\mathbf{H}_d = \mathbf{H}^r_{d-1} p_d + P_{d-1} \mathbf{Y}^r_d$$

Elimination of the interconnecting nodes of N_d would generate $\mathbf{H}^r_d$ which is the required solution $\mathbf{Y}^r$.

Simultaneous coupling

The difference between this method and the previous one is that both the internal nodes of the new part and the interconnecting nodes with the current interconnected system are eliminated in one step instead of in two separate ones.

Define the admittance matrix $\mathbf{G}_k$ of the kth interconnected system by

$$\mathbf{G}_k = \mathbf{G}^r_{k-1} + \mathbf{P}_{k-1}\mathbf{Y}_k, k = 1, 2, \cdots, d.$$

$$\mathbf{G}^r_0 = 0, P_0 = 1,$$

where P_k is the last pivotal numerator of the reduced system $\mathbf{G}_k$.

If $k = 1$, then $\mathbf{G}_1 = \mathbf{Y}_1$. The first stage of analysis is to eliminate all internal nodes of N_1 producing the matrix $\mathbf{G}^r_1$ and the polynomial p_1. Next, with $k = 2$, $\mathbf{G}_2 = \mathbf{Y}^r_1 + p_1\mathbf{Y}_2$. Elimination of nodes in I_2 and the interconnecting nodes C_{12} gives $\mathbf{G}^r_2$ and p_2. The procedure continues until $k = d$, when the required solution is given by $\mathbf{Y}^r = \mathbf{G}^r_d$.

The network partition method relying on artificial loading[10] can be derived from the theory of simultaneous coupling. Let $\mathbf{Y}'_k$ be the contribution of the kth subnetwork to that part of the admittance matrix $\mathbf{G}_k$ which is affected by both the previous combined system and the new part. Thus;

$$\mathbf{G}_k = \mathbf{G}^r_{k-1} + P_{k-1}(\mathbf{Y}_k - \mathbf{Y}'_k + \mathbf{Y}'_k)$$

and

$$\mathbf{G}_k = \mathbf{G}^r_{k-1} + P_{k-1}\mathbf{Y}'_k + P_{k-1}(\mathbf{Y}_k - \mathbf{Y}'_k)$$

or

$$\mathbf{F}_k = \mathbf{F}^r_{k-1} + P_{k-1}\mathbf{Y}^-_k$$

where

$$\mathbf{F}_k = \mathbf{G}_k, \mathbf{F}^r_{k-1} = \mathbf{G}^r_{k-1} + P_{k-1}\mathbf{Y}'_k \text{ and } \mathbf{Y}^-_k = \mathbf{Y}_k - \mathbf{Y}'_k.$$

Thus, the admittance $\mathbf{F}_k$ of the kth combined system may be formed from the current analysis, the last pivotal numerator and the augmented matrix $\mathbf{Y}^-_k$. The interconnecting elements of the kth part determine the form $\mathbf{Y}'_k$ and thus their role is now more significant, so complicating the partitioning process.

Independent coupling

In this method, each subnetwork is analysed independently producing $\mathbf{Y}^r_i$ and p_i from $\mathbf{Y}_i$. A single interconnected system may be constructed with an admittance matrix $\mathbf{Y}_I$ given by

$$\mathbf{Y}_I = P\sum_{i=1}^{d}\frac{\mathbf{Y}^r_i}{p_i}$$

where

$$P = \prod_{i=1}^{d} p_i,$$

the last dummy pivotal numerator of the above system. On elimination of all the interconnecting nodes, $\mathbf{Y}^r = \mathbf{Y}^r_I$.

THE NUMERICAL INTERCONNECTION METHOD

Generally, the analysis of relatively simple networks by the interpolative approach is efficient and quite accurate. But for very high orders and ill-conditioned systems the accuracy would tend to degrade after the solutions are interconnected.

Instead, numerical interconnection can be used when the terminal matrix $\mathbf{Y}^r$ will be given numerically for every frequency point. The results would be more accurate but generally more effort is required and only the frequency domain response can be determined.

THE SYMBOLIC INTERCONNECTION METHOD

It is possible to directly express the symbolic terminal matrix of a two part interconnected system in terms of the two individual solutions and hence substitution will produce the general partitioned analysis.

For simplicity, consider two subnetworks N_A, N_B with only one interconnecting node. $\mathbf{Y}^r_A$, $\mathbf{Y}^r_B$ are their terminal matrices and p_A, p_B the last pivotal numerators. If $\mathbf{Y}_I$ is the admittance matrix of the interconnecting system then

$$\mathbf{Y}_I = \mathbf{Y}^r_A p_B + \mathbf{Y}^r_B p_A \tag{13}$$

with $P = p_A p_B$ as the dummy last pivotal numerator.

If y^A_{ij} and y^B_{ij} are the general entries of $\mathbf{Y}^r_A$ and $\mathbf{Y}^r_B$, respectively, if node 1 is input and node 2 output, then

$$\mathbf{Y}_I = \begin{bmatrix} y^A_{11}p_B & 0 & y^A_{12}p_B \\ 0 & y^B_{22}p_A & y^B_{21}p_A \\ y^A_{21}p_B & y^B_{12}p_A & y^A_{22}p_B + y^B_{11}p_A \end{bmatrix} \tag{14}$$

Elimination of the interconnecting node gives $\mathbf{Y}^r_I$, of which y_{ij} is its general entry.

For the general case $y_{ij} = n_{ij}/d_{ij}$ and all y_{ij} may be given in terms of y^A_{ij}, y^B_{ij} and p_A, p_B as:

$$n_{11} = p_B N^A_{11} d^B_{11} + d^A_{22} d^A_{12} d^A_{21} n^A_{11} n^B_{11},\ d_{11} = D^A_{11} d^B_{11}$$

$$n_{12} = -n^A_{12} n^B_{12},\ d_{12} = d^A_{12} d^B_{12}$$

$$n_{21} = -n^A_{21} n^B_{21},\ d_{21} = d^A_{21} d^B_{21}$$

$$n_{22} = p_A N^B_{11} d^A_{22} + d^B_{11} d^B_{12} d^B_{21} n^A_{22} n^B_{22},\ d_{22} = D^B_{11} d^A_{22}$$

where

$$N^A_{11} = (n^A_{11} n^A_{22} d^A_{12} d^A_{21} - d^A_{11} d^A_{22} n^A_{12} n^A_{21})/p_A,$$

$$D^A_{11} = d^A_{11} d^A_{22} d^A_{12} d^A_{21}$$

and similarly for B^B_{11}, D^B_{11}.

The terms $N^A_{11}, D^A_{11}, N^B_{11}, D^B_{11}$ may be obtained from the individual analyses of N^A and N^B in the same way as n^A_{ij}, d^A_{ij}, n^B_{ij}, d^B_{ij} are obtained.

It is possible to continue the analysis in an iterative manner by considering n_{ij}, d_{ij} as the solution of a single part and selecting a new part. However, the terms N_{11}, D_{11} and p for the analysed interconnected system need to be com-

puted. A further application of the pivotal condensation formula yields

$$N_{11} = n^A_{11}d^A_{22}d^A_{12}d^A_{21}N^B_{11} + n^B_{22}d^B_{22}d^B_{12}d^B_{21}N^A_{11}$$

$$D_{11} = D^A_{11}D^B_{11}$$

and

$$P = p_B n^A_{22} d^B_{11} + p_A n^B_{11} d^A_{22}$$

The major error at this stage is polynomial division and as this is not encountered in the formation of $\mathbf{Y}^r_I$, computation error is expected to be kept to a minimum. In fact, the accuracy of the interconnection polynomials is only slightly inferior to that of the fundamental ones.

An attempt to generalize symbolic interconnection to cater for a number of interconnection nodes has encountered problems with the enormous number of polynomial combinations required.

COMPARISON OF THE NETWORK PARTITION METHODS

The number of arithmetic operations required to be executed in each method of analysis is a good indicator of the relative efficiency. Since the straightforward symbolic analysis is the basis of all partition methods, it is also considered as the basis for estimating the computing time.

If T is the estimated computing time, then

T = (effort to load the numerical nodal admittance matrix for all samples)
+ (effort to compute all the polynomial responses)
+ (effort to invert the Vandemonde matrix)
+ (effort to compute the polynomial coefficients)

Assuming an n-node, e-terminal network having N_G conductances, N_R resistors, N_C capacitors, N_L inductors, with R as the total number of coefficients of the polynomials representing the active devices, then from the Appendix

$$\begin{aligned} T = {} & (m+1)(12R + 32Q + 112N_R + 128N_L + 84N_C + \\ & 68N_G) \\ & + 25(m+1)[n(n-1)(2n-1) - e(e-1)(2e-1)] \\ & + 11m(m+1) \\ & + 26e^2(m+1)^2 \end{aligned} \qquad (15)$$

where m is the maximum order and Q is the total number of entries of all matrices entered as data.

To facilitate comparison a very simple RC ladder network has been selected. Equation (15) then reduces to

$$T = 13n^4 + 178n^2 - 162n,$$

since $N_G = N_C = m = n - 1$, e = 2. It is to be noted that the complex conjugate[4] and passivity properties have been used. Now assume the network is divided into d identical subnetworks each of r nodes; then for

Independent coupling:

$$T_A = 13(r-1)d^4 + 13(3r-2)d^3 + (133r^2 - 110r + 16)d^2 + (13r^4 + 178r^2 + 80r - 113)d + 110,$$

Double coupling:

$$T_B = 44(r-1)^2d^3 + (66r^2 + 152r + 55)d^2 + (798r^2 + 1242r + 686)d - (133r^2 + 332r),$$

Simultaneous coupling:

$$T_C = 44(r-1)^2d^3 + (7r^4 + 13r^3 + 98r^2 - 29r - 204)d^2 + (6r^4 + 26r^3 + 75r^2 - 57r + 159)d - (39r^3 + 40r^2 - 14r),$$

Symbolic interconnection:

$$T_D = (9r^2 - 8r - 1)d^2 + (13r^4 + 169r^2 - 136r)d - (18r + 2)$$

The degree of approximation in the estimated computer time is displayed in Figure 4. The actual times are taken from computations on an ICL 1905E, and the difference between actual and estimated is accounted for as routine machine calling times. Figure 5 shows the relative merits of the various partition methods and the following conclusions may be drawn:

(i) Tearing the network into relatively large subnetworks may not produce the best results.
(ii) The analysis speed may fall with the increase in the number of parts.
(iii) There exists an optimum number of parts for which the computation time is a minimum.
(iv) It is possible to analyse large networks within practical limits.

Conclusions (ii) and (iii) may not be immediately apparent for the symbolic interconnection technique but they can be verified by observing the continuously decreasing separation of the curves for equal increases in the number of parts. The curves will cross each other for very large networks. This phenomenon is due to the relatively low effort required for interconnection.

In Figure 6 the existence of an optimum number of parts is displayed. Comparing the network partition methods

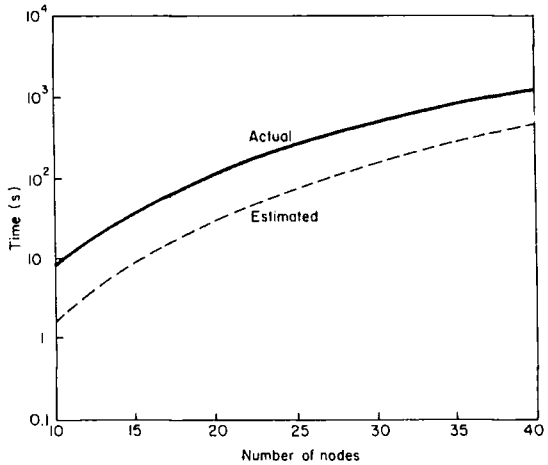

FIGURE 4. Actual and estimated computing times for straightforward analysis

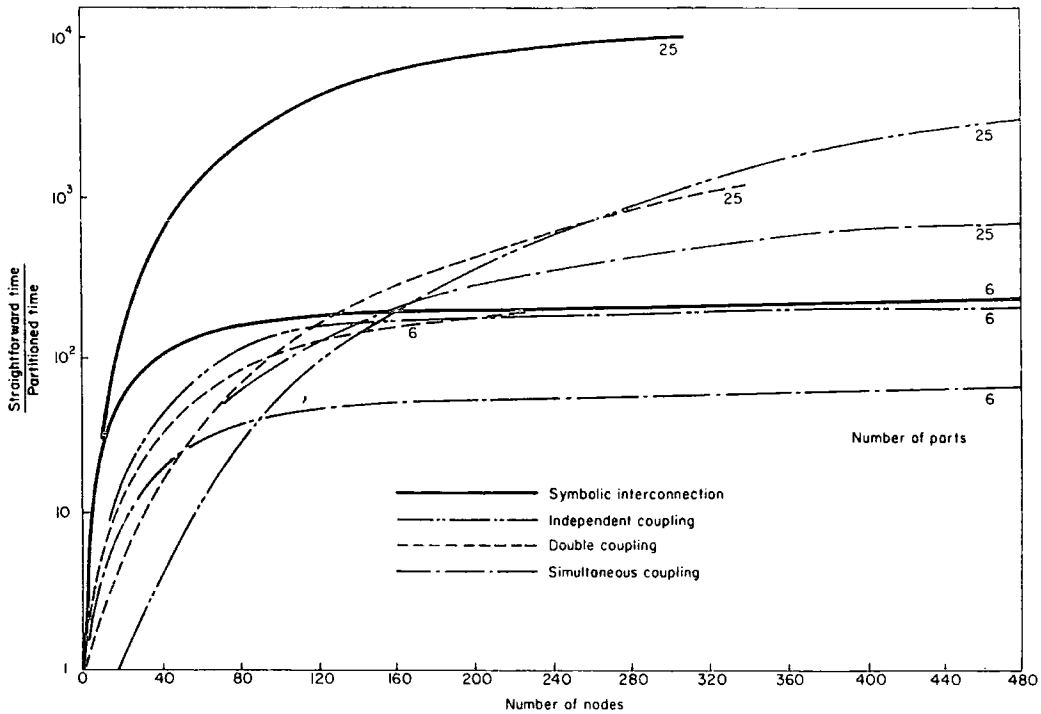

FIGURE 5. Performance characteristics of the partition methods

it may be seen that the symbolic interconnection has the greatest speed, while the independent coupling method takes the second place for a relatively small number of parts. The performance of independent coupling rapidly deteriorates for a large number of parts.

The first three network partition techniques have similar accuracy, especially when polynomial partitioning[7] is used. However, the symbolic interconnection method shows very considerable increases in accuracy. As no interpolation is required for the computation of polynomials of the intermediate interconnected systems, the error is reduced to a minimum. Typical error performance of symbolic interconnection is shown in Figure 7. The high accuracy property of this method is a very attractive feature and it is hoped that a similar characteristic will be repeated for the general multiple node symbolic interconnection case.

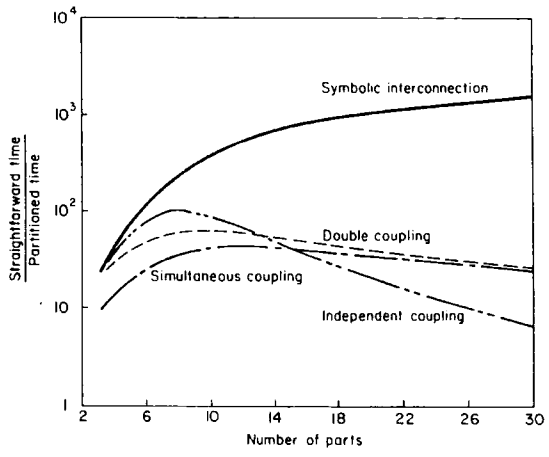

FIGURE 6. Speed comparison of the partition methods for a 61 node RC-ladder

The comparative performances of the partition methods when applied to a conventional high input-impedance amplifier circuit, Figure 8, are given in Table 1; a two part division is used. The times quoted are those experienced in computing the overall 2 x 2 admittance matrix in symbolic form. Because of the relatively low order of the network, the improvements due to partition are less dramatic than encountered with higher order circuits. This is particularly true of the symbolic interconnection case whose performance easily exceeds the other methods for higher order networks.

More impressive results have been obtained in the analysis of larger active networks, for instance, partitioned analysis (double coupling) of the SN 72741 amplifier improved the analysis time by 70% to 4 secs. For medium sized networks up to 100 nodes the partitioned methods work quite efficiently. An active network with 144 nodes proved about the present limit, the restrictions on network complexity come mainly from accuracy problems in the resultant polynomial coefficients. Very large polynomials generally have a wide range of coefficient magnitudes and the smaller ones are easily submerged by the consequences of a finite word length. Further errors occur in the evaluation of the sampled responses in very high order systems, although numerical methods for controlling these are available. Simple inversion of the Vandermonde matrix would often lead to serious errors due to ill-conditioning. A number of methods are known for overcoming this; two alternatives[7, 8] have been used in this work.

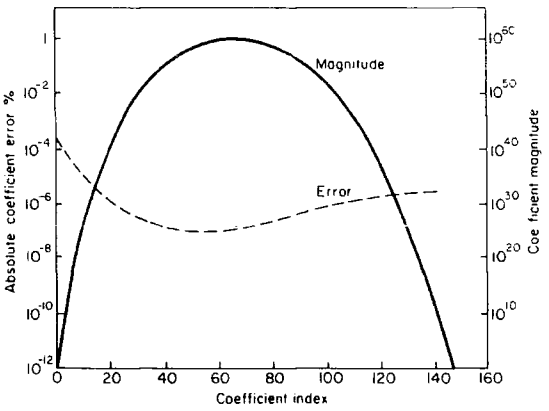

FIGURE 7. Error distribution for the symbolic interconnection method (22-part division of a 146 node ladder)

Obviously when large networks are considered there are problems with the amount of data required. Efforts have been made to reduce the user participation needed, some thought is required concerning the sections to be partitioned, but once the nodes in each part are specified, the remaining process is fully automatic. New subnetwork nodes can be chosen as required. The library concept has been used to great advantage, symbolic matrices for transistors, amplifiers or subnetworks which occur frequently are computed and stored. Both internal and external library facilities are available. This has proved especially useful in the analysis of large integrated circuits.

CONCLUSION

It has been shown that it is possible to perform efficient symbolic analysis of general active networks by partitioning the network into a number of parts. All the methods discussed avoid the generation of common factors without recourse to an artificial loading technique used earlier.

The network partition technique has special significance in computing sensitivities, as intermediate results of current work is showing. Because of the large number of variables that would be involved in completely literal symbolic analysis of high order networks, such analysis is not contemplated.

TABLE 1. Comparative performance parameters of partition methods in amplifier analysis

Method	Parameter	Computer Requirements	Figure of Merit Straightforward/ Partition
Straightforward	Time (s)	9	–
	Store (k words)	13.2	–
Double coupling	Time (s)	5	1.80
	Store (k words)	13.6	0.97
Simultaneous coupling	Time (s)	7	1.29
	Store (k words)	11.9	1.11
Independent coupling	Time (s)	4	2.25
	Store (k words)	16.0	0.85
Symbolic interconnection	Time (s)	6	1.50
	Store (k words)	17.1	0.77

But the partition methods can be easily applied to semi-literal analysis to some advantage.

It would seem that the difficulties in symbolic analysis caused by speed, storage and error problems for high order networks, can be contained so that successful analysis of active and passive networks can be achieved.

For extremely large networks the polynomials would be of such high order and the computation error of such magnitude that symbolic analysis could hardly be envisaged. Conventional methods for numerical analysis at each frequency will always be faster in determining numerical responses of one type or another. For these networks, such methods together with partitioning and sparse matrix techniques should be used.

Financial support of the Science Research Council is acknowledged.

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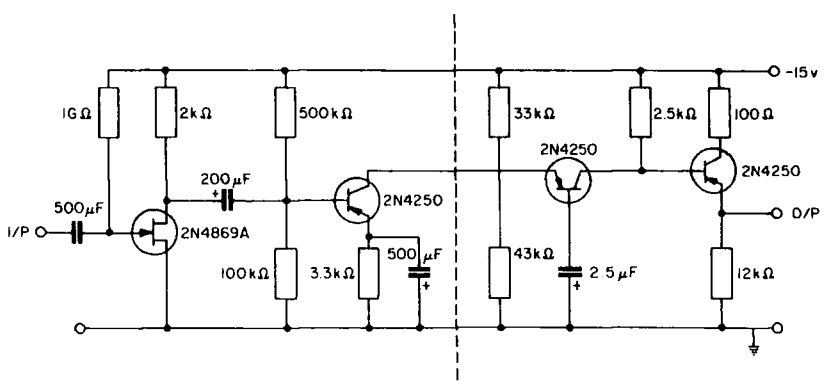

FIGURE 8. High input-impedance amplifier circuit

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APPENDIX

ESTIMATION OF COMPUTING TIME

The pivotal condensation formula is used in reducing the numerical nodal admittance matrix to its terminal form. At an intermediate stage, say, when reducing the kth order matrix to one of order $(k-1)$ the formula is applied $(k-1)^2$ times.

If T_{cond} is the effort required to reduce a matrix from order n to order e, which is equivalent to an n-node e-terminal network for $m+1$ samples, then

$$T_{\text{cond}} = (m+1)\sum_{k=e+1}^{n}(k-1)^2$$

repetitions of the reduction formula

$$= \frac{1}{6}(m+1)[n(n-1)(2n-1) - e(e-1)(2e-1)]$$

For passive networks the nodal admittance matrix is symmetric; using this properly gives

$$T_{\text{cond}_p} = (m+1)\sum_{k=e+1}^{n}\frac{1}{2}(k-1)(k-2)$$

repetitions of the reduction formula

$$= \frac{1}{6}(m+1)[n(n^2-1) - e(e^2-1)]$$

Translating these into equivalent addition operations, assuming the computing time for subtraction is equal to that for addition, multiplication is 2.2 × (addition) and division 4.4 × (addition) reveals that one execution of the condensation formula suitable for complex arithmetic requires the equivalent of 148 additions. Thus,

$$T_{\text{cond}} = 25(m+1)[n(n-1)(2n-1) - e(e-1)(2e-1)]$$

additions for active networks

and

$$T_{\text{cond}_p} = 25(m+1)[n(n^2-1) - e(e^2-1)] \text{ additions.}$$

Computation of the polynomial responses usually takes most of the total analysis time. But other operations such as matrix loading, (generation of the nodal admittance matrix at each sample), Vandermonde matrix inversion, and computation of the polynomial coefficients cannot be neglected when an accurate estimate of computational effort is being sought.

Again in terms of equivalent additions the matrix loading effort for all samples

$$= (m+1)(112N_R + 128N_L + 84N_C + 68N_G + 32Q + 12R) \text{ additions,}$$

effort for Vandemonde matrix inversion using a Fast Fourier Transform version

$$= 11m(m+1) \text{ additions,}$$

and effort for final computation of all polynomial coefficients (matrix multiplication)

$$= 26e^2(m+1)^2 \text{ additions.}$$

Thus, the total effort

$$T = (m+1)(12R + 32Q + 112N_R + 128N_L + 84N_C + 68N_G)$$
$$+ 25(m+1)[n(n-1)(2n-1) - e(e-1)(2e-1)]$$
$$+ 11m(m+1)^2 + 26e^2(m+1)^2 \text{ equivalent additions.}$$

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Symbolic network sensitivities using partition methods†

C. PHRYDAS‡ and J. I. SEWELL‡

Straightforward symbolic analysis methods have been frequently used to generate the sensitivities of the network functions with respect to the elements. With these techniques the computer requirements tend to become excessive for large networks. A network partition and interconnection method has been developed in an attempt to increase the efficiency of analysis and has been applied successfully. The network is divided into an arbitrary number of parts with an arbitrary interconnection. First- and second-order derivatives are considered.

1. Introduction

The sensitivities of network responses to element variations are very important in circuit design and therefore efficient means for their computation have been sought. A popular method has made use of the adjoint network concept ; it is quite fast and applicable in both time and frequency domains (Director and Rohrer 1969 a, b). Matrix inversion techniques are an important alternative (Sud 1975) but generally require repetition at each frequency point. Large change sensitivities (Goddard *et al.* 1971) are also valuable and have found application in statistical design (Butler 1971).

Differential sensitivities in symbolic form (Cutteridge and Di Mambro 1970, 1971) tend to be more general and efficient than the single frequency point techniques. The use of interpolation is evident in these techniques. Since improvements to the accuracy of the interpolative methods have been made (Fridas and Sewell 1974, Singal and Vlach 1974) they hold greater appeal. Still further increases in accuracy are possible using an iterative correction procedure (Fridas and Sewell 1975).

Partition methods have been employed to good effect (Fridas and Sewell 1976) in the analysis of high order active networks. General improvement in speed and accuracy were experienced. In this work the network partitioning methods are developed to produce first- and second-order sensitivities.

2. Differential sensitivities

Let $\mathcal{N}$ be a linear active network with n nodes, of which e are terminal nodes, and having a nodal admittance matrix Y, Fig. 1. In the usual notation G, Γ, C represent the conductance, inverse inductance and capacitance components of Y. A is an active device matrix whose entries are rational functions in s :

$$Y = G + A + \frac{\Gamma}{s} + sC = \frac{1}{s}\left[\Gamma + s(G + A) + s^2 C\right]$$

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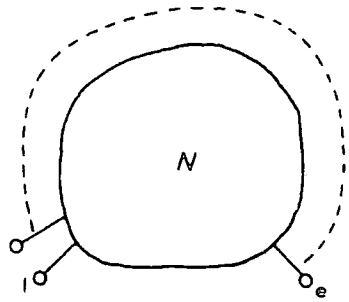

Figure 1. General network $\mathcal{N}$.

The network performance can be represented by the terminal admittance matrix Y^r of order e (often 2×2) obtained from Y by elimination of all the internal nodes of $\mathcal{N}$. A general entry of Y^r is

$$y_{ij}{}^r = \frac{|Y_{ij}|}{|Y_D|} = \frac{N_{ij}}{D}$$

where Y_{ij} and Y_D are appropriate co-factor matrices. As $N_{ij} = f(y_{rs})$, where y_{rs} is a general entry of Y, then

$$\frac{\partial N_{ij}}{\partial x_k} = \sum_{r=1}^{n} \sum_{s=1}^{n} \frac{\partial N_{ij}}{\partial y_{rs}} \frac{\partial y_{rs}}{\partial x_k}, \quad \forall i, j = 1, 2 \ldots e \text{ and } k = 1, 2 \ldots V \tag{1}$$

where x_i is a network element, of which there are V in number. The term $\partial y_{rs}/\partial x_k$ is easily computed, $\partial N_{ij}/\partial y_{rs}$ is more difficult to determine. A similar expression applies to the denominator

$$\frac{\partial D}{\partial x_k} = \sum_{r=1}^{n} \sum_{s=1}^{n} \frac{\partial D}{\partial y_{rs}} \frac{\partial y_{rs}}{\partial x_k} \tag{2}$$

The second-order derivatives follow :

$$\frac{\partial^2 N_{ij}}{\partial x_k \partial x_l} = \sum_{r=1}^{n} \sum_{s=1}^{n} \sum_{p=1}^{n} \sum_{q=1}^{n} \frac{\partial^2 N_{ij}}{\partial y_{rs} \partial y_{pq}} \frac{\partial y_{rs}}{\partial x_k} \frac{\partial y_{pq}}{\partial x_l} + \sum_{r=1}^{n} \sum_{s=1}^{n} \frac{\partial N_{ij}}{\partial y_{rs}} \frac{\partial^2 y_{rs}}{\partial x_k \partial x_l}, \quad \forall k = 1, 2 \ldots V-1 \quad \forall l = k+1, k+2 \ldots V \tag{3}$$

A similar expression results for $\dfrac{\partial^2 D}{\partial y_{rs} \partial y_{pq}}$. In computing entry sensitivities it is obvious that a passive component may contribute to only one or four entry terms.

2.1. *Computation of entry sensitivities*

Let

$$\frac{\partial N_{ij}}{\partial y_{rs}} = c_{sr}{}^{ij}$$

and

$$\frac{\partial D}{\partial y_{rs}} = c_{sr}{}^{d}$$

where C^{ij}, C^{d} are adjoint matrices, whose entries are determined in general by the following procedure :

$$n_{ij}{}^{(r)} = \{n_{ij}{}^{(r-1)} n_{kk}{}^{(r-1)} - n_{ik}{}^{(r-1)} n_{kj}{}^{(r-1)}\}/n^{(r-2)}{}_{k+1,\,k+1}, \quad j = 1, 2 \ldots k$$
$$b_{ij}{}^{(r)} = \{b_{ij}{}^{(r-1)} n_{kk}{}^{(r-1)} - n_{ik}{}^{(r-1)} b_{kj}{}^{(r-1)}\}/n^{(r-2)}{}_{k+1,\,k+1}, \quad j = 1, 2 \ldots n$$

for $k = n, n-1, \ldots e+1$; $i = 1, 2 \ldots k-1$ and $r = n-k+1$.

Initially $n_{ij}{}^{(0)} = n_{ij}$; $b_{ij}{}^{(0)} = \delta_{ij}$ (Kronecker delta) ; $n^{(-1)}{}_{n+1,\,n+1} = 1$. When $r = n-e$ these operations are halted and $n_{ij}{}^{(r)} = n_{ij}{}^{(n-e)}$:

$$d^{(r)} = n^{(n-e-1)}{}_{e+1,\,e+1}$$

Now let

$$d_i = n_{ii}{}^{(n-e)}, \quad i = 1, 2 \ldots n$$
$$n_{ij}{}'^{(0)} = n_{ij}{}^{(n-e)} \quad \text{and} \quad b_{ij}{}'^{(0)} = b_{ij}{}^{(n-e)}$$
$$n_{ij}{}'^{(r)} = \{n_{ij}{}'^{(r-1)} n_{kk}{}'^{(r-1)} - n_{ik}{}'^{(r-1)} n_{kj}{}'^{(r-1)}\}/d_{k+1}$$
$$b_{ij}{}'^{(r)} = \{b_{ij}{}'^{(r-1)} n_{kk}{}'^{(r-1)} - n_{ik}{}'^{(r-1)} b_{kj}{}'^{(r-1)}\}/d_{k+1}$$

$k = n-1, n-2 \ldots e+1$; $i = k+1, k+2 \ldots n$; $j = 1, 2 \ldots n$ and $r = n-k$.

The adjoint matrices will be of order $n-e+1$ but for uniformity and ease of programming the higher order is retained and borders of zero rows and columns retained. Hence if $n_{ij}{}'' = n_{ij}{}'^{(n-e-1)}$ and $b_{ij}{}'' = b_{ij}{}'^{(n-e-1)}$ and $p, q = 1, 2 \ldots e$

$$c_{jq}{}^{pq} = b_{pj}{}'', \quad j = e+1, e+2 \ldots n$$
$$c_{pj}{}^{pq} = 0, \quad j = 1, 2 \ldots e ; \; j \neq q$$
$$c_{pq}{}^{pq} = b_{pp}{}''$$
$$c_{ij}{}^{pq} = 0, \quad i = 1, 2 \ldots e \text{ and } i \neq p ; \; j = 1, 2 \ldots n$$
$$c_{ji}{}^{pq} = \{b_{ij}{}'' n_{pq}{}'' - n_{iq}{}'' b_{pj}{}''\}/n_{e+1,\,e+1}{}'^{(0)}, \quad i, j = e+1, e+2 \ldots n$$
$$c_{pi}{}^{pq} = \{b_{ip}{}'' n_{pq}{}'' - n_{iq}{}'' b_{pp}{}''\}/n_{e+1,\,e+1}{}'^{(0)}, \quad i = e+1, e+2 \ldots n$$
$$c_{ij}{}^{pq} = 0, \quad i = e+1, e+2 \ldots n ; \; j = 1, 2 \ldots e ; \; j \neq q$$

Finally

$$c_{ij}{}^{d} = c_{ij} = 0, \quad i = 1, 2 \ldots n ; \; j = 1, 2 \ldots e$$
$$c_{ij}{}^{d} = b_{ij}{}'', \quad i, j = e+1, e+2 \ldots n$$

The polynomials of Y^r, C^{ij} and C^{d} are therefore determined by interpolation at an appropriate number of samples. Hence a classical sensitivity measure

$$S_{x_k}{}^{ij} = x_k \left(\frac{\partial N_{ij}}{\partial x_k} / N_{ij} - \frac{\partial D}{\partial x_k} / D \right) \tag{4}$$

can then be computed for each response function with respect to the desired elements.

3. Network partition and sensitivities

The network $\mathcal{N}$ can be divided into a number of subnetworks with arbitrary interconnections. A double coupling method (Fridas and Sewell 1976) is chosen; the process selects two connected subnetworks $\mathcal{N}_A$, $\mathcal{N}_B$, Fig. 2. Each subnetwork is analysed independently, the solutions combined and a solution for the interconnected subsystem produced. A new subnetwork is selected, analysed, combined with the previous solution and a new interconnected subsystem formed. This is repeated over all subnetworks.

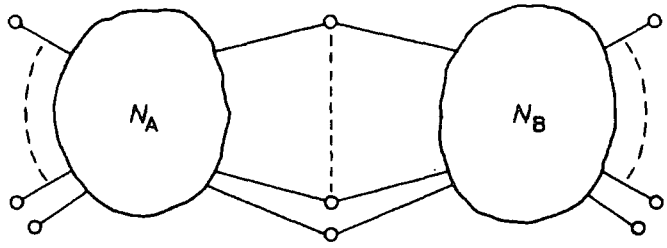

Figure 2. The subnetworks $\mathcal{N}_A$, $\mathcal{N}_B$ and their interconnection.

If Y_A, Y_B are the terminal admittance matrices of $\mathcal{N}_A$, $\mathcal{N}_B$ after interpolation and X_A, X_B are the sets of elements in each part respectively. Define the matrices Λ_A, Λ_B as

$$Y_A = \frac{1}{p_A}\Lambda_A \quad \text{and} \quad Y_B = \frac{1}{p_B}\Lambda_B$$

where p_A, p_B are the last pivotal numerators generated when analysing $\mathcal{N}_A$, $\mathcal{N}_B$. Then the augmented matrix Y_I of the interconnected system $\mathcal{N}_I$ is

$$Y_I = \Lambda_A p_B + \Lambda_B p_A \tag{5}$$

A typical numerator entry of Y_I will be

$$n_{ij}^{I} = n_{i_A j_A}^{A} p_B + n^{B}_{i_B j_B} p_A \tag{6}$$

$i, j = 1, 2 \ldots e_I$; $i_A, j_A = 1, 2 \ldots e_A$; $i_B, j_B = 1, 2 \ldots e_B$, where e_I, e_A, e_B are the number of terminals $\mathcal{N}_I$, $\mathcal{N}_A$, $\mathcal{N}_B$ respectively.

Let the functions in the reduced matrix be N_{ij}/D and all the first- and second-order derivatives with respect to $x_i \in X_I$ are required where $X_I = X_A \cup X_B$.

It is known that in partitioned analysis the last pivotal numerator required to be removed as a common factor in the first stage of reduction of the combined system is $P = p_A p_B$. Assume that Y_I is reduced to its terminal matrix

with P being removed appropriately; hence $N_{ij}=P^{-(n_I-e_I)}N_{ij}'$ and $D=P^{-(n_I-e_I-1)}D'$. Direct differentiation will give

$$\frac{\partial N_{ij}}{\partial x_k}=\frac{1}{P^t}\frac{\partial N_{ij}'}{\partial x_k}-t\frac{\partial N_{ij}}{P}\frac{\partial P}{\partial x_k} \tag{7}$$

$$\frac{\partial^2 N_{ij}}{\partial x_k\partial x_l}=\frac{1}{P^t}\frac{\partial^2 N_{ij}'}{\partial x_k\partial x_l}-\frac{t}{P}\left(\frac{\partial N_{ij}}{\partial x_k}\frac{\partial P}{\partial x_l}+\frac{\partial N_{ij}}{\partial x_l}\frac{\partial P}{\partial x_k}\right)$$
$$-t(t-1)\frac{N_{ij}}{P^2}\frac{\partial P}{\partial x_k}\frac{\partial P}{\partial x_l}-t\frac{N_{ij}}{P}\frac{\partial^2 P}{\partial x_k\partial x_l} \tag{8}$$

where $t=n_I-e_I$.

Similar expressions for the derivatives of D can be determined. Following the derivations of the Appendix gives

$$\frac{\partial N_{ij}'}{\partial x_k}=\sum_{r=1}^{n_I}\sum_{s=1}^{n_I}\frac{\partial N_{ij}'}{\partial n_{rs}^I}\frac{\partial n_{rs}^I}{\partial x_k} \tag{9}$$

$$\frac{\partial^2 N_{ij}'}{\partial x_k\partial x_l}=\sum_{r=1}^{n_I}\sum_{s=1}^{n_I}\sum_{\substack{p=1\\p\neq r}}^{n_I}\sum_{\substack{q=1\\q\neq s}}^{n_I}\left(\frac{\partial^2 N_{ij}'}{\partial n_{rs}^I\partial n_{pq}^I}\right)\left(\frac{\partial n_{rs}^I}{\partial x_k}\right)\left(\frac{\partial n_{pq}^I}{\partial x_l}\right)$$
$$+\sum_{r=1}^{n_I}\sum_{s=1}^{n_I}\left(\frac{\partial N_{ij}'}{\partial n_{rs}^I}\right)\left(\frac{\partial^2 n_{rs}^I}{\partial x_k\partial x_l}\right) \tag{10}$$

and the derivatives of D are produced similarly.

Now if Z_{rs}^{IJ} and Z_{rs}^{D} are the general entries of adj (Y_I^{IJ}) and adj (Y_I^{D}) respectively it can be shown that the common factor P can be extracted as

$$Z_{rs}^{IJ}=P^{t-1}Z_{rs}'^{IJ}\quad\text{and}\quad Z_{rs}^{D}=P^{t-2}Z_{rs}'^{D} \tag{11}$$

Hencing combining eqns. (7), (8), (9), (10), (11) and setting

$$\frac{\partial N_{ij}'}{\partial n_{rs}^I}=P^{t-1}\frac{\partial N_{ij}''}{\partial n_{rs}^I}$$

and by Jacobi's theorem

$$\frac{\partial^2 N_{ij}''}{\partial n_{rs}^I\partial n_{pq}^I}=\frac{1}{P^2N_{ij}}\left(\frac{\partial N_{ij}''}{\partial n_{rs}^I}\frac{\partial N_{ij}''}{\partial n_{pq}^I}-\frac{\partial N_{ij}''}{\partial n_{rq}^I}\frac{\partial N_{ij}''}{\partial n_{ps}^I}\right)$$

gives

$$\frac{\partial N_{ij}}{\partial x_k}=\frac{1}{P}\sum_{r=1}^{n_I}\sum_{s=1}^{n_I}\left(\frac{\partial N_{ij}''}{\partial n_{rs}^I}\right)\left(\frac{\partial n_{rs}^I}{\partial x_k}\right)-t\frac{N_{ij}}{P}\frac{\partial P}{\partial x_k} \tag{12}$$

$$\frac{\partial^2 N_{ij}}{\partial x_k\partial x_l}=\frac{1}{PN_{ij}}\sum_{r=1}^{n_I}\sum_{s=1}^{n_I}\sum_{\substack{p=1\\p\neq r}}^{n_I}\sum_{\substack{q=1\\q\neq s}}^{n_I}\left\{\left(\frac{\partial N_{ij}''}{\partial n_{rs}^I}\frac{\partial N_{ij}''}{\partial n_{pq}^I}-\frac{\partial N_{ij}''}{\partial n_{rq}^I}\frac{\partial N_{ij}''}{\partial n_{ps}^I}\right)\right.$$
$$\left.\times\left(\frac{\partial n_{rs}^I}{\partial x_k}\right)\left(\frac{\partial n_{pq}^I}{\partial x_l}\right)\right\}$$
$$+\frac{1}{P}\sum_{r=1}^{n_I}\sum_{s=1}^{n_I}\left(\frac{\partial N_{ij}''}{\partial n_{rs}^I}\right)\left(\frac{\partial^2 n_{rs}^I}{\partial x_k\partial x_l}\right)-\frac{t}{P}\left(\frac{\partial N_{ij}}{\partial x_k}\frac{\partial P}{\partial x_l}+\frac{\partial N_{ij}}{\partial x_l}\frac{\partial P}{\partial x_k}\right)$$
$$-t(t-1)\frac{N_{ij}}{P^2}\left(\frac{\partial P}{\partial x_k}\right)\left(\frac{\partial P}{\partial x_l}\right)-t\frac{N_{ij}}{P}\frac{\partial^2 P}{\partial x_k\partial x_l} \tag{13}$$

Again, similar expressions obtain for the derivatives of D.

The derivatives of N_{ij}'' or D'' can be produced by multiplying the corresponding derivatives of N_{ij}' and D' by the appropriate power of P. However, large powers of P can cause problems on the computer and it is therefore expedient to compute the derivatives of N_{ij}'' and D'' directly by taking the factor P into account in the initial stage of the analysis of $\mathcal{N}_I$.

Differentiation of eqn. (6) completes the necessary algebra. Terms of the form

$$\frac{\partial n_{ij}{}^{I}}{\partial x_{\mathrm{A}}} = \frac{\partial n_{i_{\mathrm{A}}j_{\mathrm{A}}}{}^{\mathrm{A}}}{\partial x_{\mathrm{A}}} P_{\mathrm{B}} + n_{i_{\mathrm{B}}j_{\mathrm{B}}}{}^{\mathrm{B}} \frac{\partial P_{\mathrm{A}}}{\partial x_{\mathrm{A}}}$$

are produced for elements in the networks $\mathcal{N}_{\mathrm{A}}$ and $\mathcal{N}_{\mathrm{B}}$.

The first- and second-order derivatives as well as the network functions can be computed from the analyses of subnetworks. The network function numerators, last pivotal numerator and their derivatives are all that are required. The process may be repeated for an arbitrary number of parts.

4. Results

The partitioned method for deriving first- and second-order network sensitivities has been applied to both passive and active networks. Mainly for comparison purposes a 30-node RC ladder was chosen and the sensitivities of the 2-port admittance functions with respect to a number of the elements computed. Using a straightforward technique without partition and computing first- and second-order sensitivity polynomials of the above functions with respect to six elements required 105 sec and 16·4 K words of store on

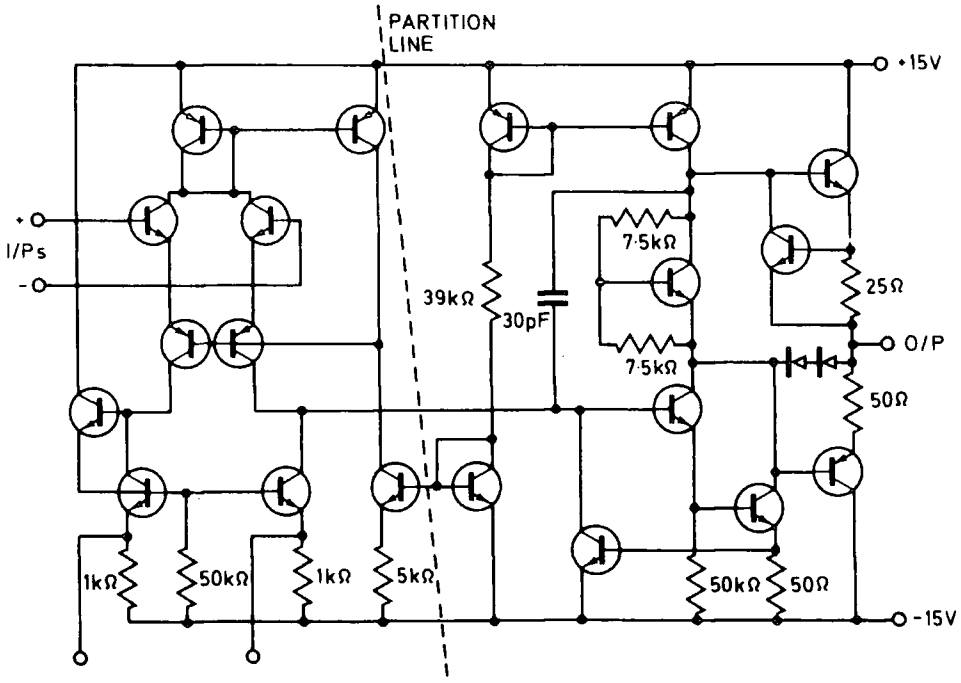

Figure 3. The SN 72741 operational amplifier.

an ICL 1904S. Partitioning and using four sections with eight nodes in each only needed 22 sec of computer time but 18·2 K words of store, the interconnecting process being responsible for the extra storage needed. The same problem using a 3-part division required 33 sec and 18·6 K store. Similar performance ratios are experienced when more elements are considered in the sensitivity analysis and for higher-order networks. Storage problems determine the upper bound on network order and number of elements considered.

Figure 3 shows a typical active network which has been analysed by these means ; the circuit is that of the SN 72741 operational amplifier. To produce the first-order sensitivity functions for one element required 17 sec and 12·8 K store, the repetition of the calculation for the first-order sensitivities of up to seven elements only needed 18 sec and 12·8 K store.

The accuracy of the computed coefficients is typical of interpolative methods. It can be improved by partitional polynomial interpolation (Fridas and Sewell 1974) or the FFT (Singal and Vlach 1974). Iterative improvement techniques can be employed, and of particular significance here are those concerned with improving the accuracy of the adjoint matrix (Fadeev and Fadeeva 1963).

Appendix

Let $u=f(x_1, x_2, \ldots, x_n)$ where $x_i=x_i(t_1, t_2, \ldots, t_m)$ and t_k are independent variables.

Assuming the continuity of derivatives involved gives (Sokolnikoff 1939)

$$\frac{\partial f}{\partial t_k}=\sum_{i=1}^{n}\frac{\partial f}{\partial x_i}\frac{\partial x_i}{\partial t_k} \tag{A 1}$$

Equation (9) follows directly from (A 1).

Differentiating eqn. (A 1) with respect to t_l, gives

$$\begin{aligned}
\frac{\partial^2 f}{\partial t_k \partial t_l} &= \frac{\partial}{\partial t_l}\sum_{i=1}^{n}\frac{\partial f}{\partial x_i}\frac{\partial x_i}{\partial t_k} \\
&= \sum_{i=1}^{n}\left\{\frac{\partial^2 f}{\partial x_i \partial t_l}\frac{\partial x_i}{\partial t_k}+\frac{\partial f}{\partial x_i}\frac{\partial^2 x_i}{\partial t_k \partial t_l}\right\} \\
&= \sum_{i=1}^{n}\frac{\partial}{\partial x_i}\left(\frac{\partial f}{\partial t_l}\right)\frac{\partial x_i}{\partial t_k}+\sum_{i=1}^{n}\frac{\partial f}{\partial x_i}\frac{\partial^2 x_i}{\partial t_k \partial t_l} \\
&= \sum_{i=1}^{n}\left\{\frac{\partial}{\partial x_i}\sum_{j=1}^{n}\frac{\partial f}{\partial x_j}\frac{\partial x_j}{\partial t_l}\right\}\frac{\partial x_i}{\partial t_k}+\sum_{i=1}^{n}\frac{\partial f}{\partial x_i}\frac{\partial^2 x_i}{\partial t_k \partial t_l} \\
&= \sum_{j=1}^{n}\left(\sum_{i=1}^{n}\left\{\frac{\partial^2 f}{\partial x_i \partial x_j}\frac{\partial x_j}{\partial t_l}+\frac{\partial f}{\partial x_j}\frac{\partial^2 x_j}{\partial x_i \partial t_l}\right\}\right)\frac{\partial x_i}{\partial t_k}+\sum_{i=1}^{n}\frac{\partial f}{\partial x_i}\frac{\partial^2 x_i}{\partial t_k \partial t_l} \\
&= \sum_{j=1}^{n}\sum_{i=1}^{n}\left(\frac{\partial^2 f}{\partial x_i \partial x_j}\right)\left(\frac{\partial x_i}{\partial t_k}\right)\left(\frac{\partial x_j}{\partial t_l}\right)+\sum_{i=1}^{n}\left(\frac{\partial f}{\partial x_i}\right)\left(\frac{\partial^2 x_i}{\partial t_k \partial t_l}\right)
\end{aligned} \tag{A 2}$$

since in network analysis

$$\frac{\partial x_j}{\partial x_i} = 0, \quad \forall i, j$$

Equation (10) has been derived from eqn. (A 2) and the properties

$$|A| = \sum_{i=1}^{n} a_{ij} |A_{ij}| (-1)^{i+j} = \sum_{j=1}^{n} a_{ij} |A_{ij}| (-1)^{i+j}$$

and

$$\frac{\partial^2 |A|}{\partial a_{ij} \partial a_{ik}} = \frac{\partial^2 |A|}{\partial a_{kj} \partial a_{lj}} = 0$$

which impose constraints on the summation parameters.

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PAPERS 24 + 30

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Analysis of Active Switched-Capacitator Networks

JOHN I. SEWELL

Abstract—It is shown that amplifier matrices can be included in the nodal equation formulation for the analysis of switched-capacitor networks. This avoids any requirements for equivalent circuits and enables a straightforward application to computer analysis. For ideal operational amplifiers constraint theory is shown to be applicable.

The theory and design of switched-capacitor (SC) networks is receiving much attention at the present time. The analysis of SC networks is proceeding along a number of avenues, the basic ones being nodal techniques [1], and equivalent circuit methods [2], [3]. The second method has some appeal from the practical insight view, but involves the determination and application of equivalent circuits that are not exactly simple. The nodal analysis requires a large number of equations, $2n$, where n is the number of nodes, but these can be assembled in a logical manner and the method is particularly attractive for computer analysis of SC networks since many standard matrix methods can be employed.

For a passive network, containing only capacitances and switches with half cycle operation, the $2n \times 2n$ definite nodal matrix $\hat{Y}$ is determined from

$$\begin{bmatrix} \hat{I}^e \\ \hat{I}^o \end{bmatrix} = \left[\begin{array}{c|c} I^e C S^e & -z^{-1} I^e C S^o \\ \hline -z^{-1} I^o C S^e & I^o C S^o \end{array}\right] \begin{bmatrix} V^e \\ V^o \end{bmatrix} \tag{1}$$

or

$$\hat{I} = \hat{Y} V.$$

The nomenclature of [1] is retained, $\hat{I}^e$ $\hat{I}^o$ being the vectors of even and odd phase currents; V^e, V^o are the even and odd nodal voltage vectors; S^e, S^o the even and odd switching matrices; I^e, I^o the even and odd network current matrices; C the capacitance nodal admittance matrix; and $z^{-1} = e^{-sT}$ where τ is half the clock period. The $\hat{Y}$ matrix is always symmetric for a passive network, and the main diagonal terms are positive, but in contrast to the ordinary definite admittance matrix the signs of all off diagonal terms are not necessarily negative. Some rows and columns are zero so, by definition, these and the corresponding variables can be eliminated; however, it is wise to examine the inclusion of active devices before executing this step.

When active devices are present in the network, assemble the nodal matrix for the passive part $\hat{Y}_p$ as indicated. Now an ordinary amplifier will be operational during the even and odd switching phases and therefore will contribute equally to even and odd equations hence

$$\begin{bmatrix} \hat{I}_A^e \\ \hat{I}_A^o \end{bmatrix} = \left[\begin{array}{c|c} Y_A & 0 \\ \hline 0 & Y_A \end{array}\right] \begin{bmatrix} V^e \\ V^o \end{bmatrix}$$

or

$$\hat{I}_A = \hat{Y}_A V.$$

The Y_A matrix, for instance, may be any of those quoted for various types of amplifier [4] or indeed the admittance matrix of any active device. Addition of the active and passive matrices will yield the complete nodal matrix

$$\hat{Y} = \hat{Y}_p + \hat{Y}_A.$$

As expected, $\hat{Y}$ is not symmetric for an active network.

Some simple rules for the assembly of the matrices now emerge. When writing down the switching matrices S^e, S^o all port voltages must be retained as independent variables and all voltages at amplifier terminals must remain as independent variables. When constructing the current matrices I^e, I^o the currents at either the network ports or the amplifier terminals must not become zero.

After the assembly of the $\hat{Y}$ matrix, inspection will show the *corresponding* rows and columns that are zero, these are now eliminated to produce a reduced matrix $\hat{Y}_R$. It is then possible to determine, by cofactor methods, the appropriate transfer functions from $\hat{Y}_R$. For general analysis it is probably more informative to apply pivotal condensation to $\hat{Y}_R$ and obtain the four-port y-matrix

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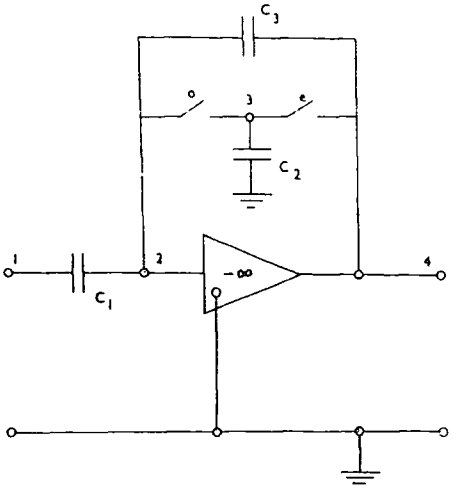

Fig. 1. Switched-capacitor lossy differentiator.

$$\begin{bmatrix} \hat{I}_1^e \\ \hat{I}_n^e \\ \hat{I}_1^o \\ \hat{I}_n^o \end{bmatrix} = \begin{bmatrix} y_{11}^{ee} & y_{1n}^{ee} & y_{11}^{eo} & y_{1n}^{eo} \\ y_{n1}^{ee} & y_{nn}^{ee} & y_{n1}^{eo} & y_{nn}^{eo} \\ y_{11}^{oe} & y_{1n}^{oe} & y_{11}^{oo} & y_{1n}^{oo} \\ y_{n1}^{oe} & y_{nn}^{oe} & y_{n1}^{oo} & y_{nn}^{oo} \end{bmatrix} \begin{bmatrix} V_1^e \\ V_n^e \\ V_1^o \\ V_n^o \end{bmatrix}$$

where node 1 is input and node n is output. In practical networks quite a number of the y-parameters will be zero. Clearly the input admittance during even phase switching is

$$\left.\frac{I_1^e}{V_1^e}\right|_{V_1^o = V_n^o = V_n^e = 0} = y_{11}^{ee}.$$

Similarly the voltage transfer functions, for even sampling input and output

$$G_{n1}^{ee}(z) = \frac{V_n^e}{V_1^e} = \frac{-y_{n1}^{ee}}{y_{nn}^{ee}}$$

for even sampling input and odd sampling output

$$G_{n1}^{oe}(z) = \frac{V_n^o}{V_1^e} = \frac{-y_{n1}^{oe}}{y_{nn}^{oo}}$$

provided, of course, these functions exist practically. The number of characteristic functions available in an SC network is obviously potentially greater than in a conventional active network.

When ideal operational amplifiers are the active elements in the network it is possible to utilize conventional constraint theory [5] in the analysis. Consider an ideal voltage amplifier with voltage gain $-m$ and connected between nodes i, j, hence

$$V_j = -m V_i \quad \text{or} \quad V_i = \frac{-V_j}{m}$$

in an SC network the constraint becomes $V_i^o = -V_j^o/m$, $V_i^e = -V_j^e/m$ hence the column $i(odd)$ is divided by m and subtracted from $V_j(odd)$, column $i(odd)$ is then discarded and similarly with columns $i(even)$ and $j(even)$. The rows involving $\hat{I}_j^o$ and $\hat{I}_j^e$ are redundant, since these express the current outputs from a voltage source, and are, therefore, discarded. The matrix $\hat{Y}_C$ once more is square, but cofactor techniques have now to be used in evaluating the required characteristic functions as there is no longer a direct relationship between the rows and columns of the matrix and the network nodes. Of course, when $m \to \infty$ the process merely amounts to striking out columns $i(odd)$, $i(even)$ and rows $j(odd)$, $j(even)$.

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When a difference amplifier is present then this may be characterized by $V_k = m(V_i - V_j)$. Hence $V_k^e/m = V_i^e - V_j^e$ and $V_k^o/m = V_i^o - V_j^o$ and when $m \to \infty$, $V_i^e = V_j^e$, $V_i^o = V_j^o$ thus column $i(even)$ is added to column $j(even)$ and the former discarded; column $i(odd)$ is added to column $j(odd)$ and the former discarded. Again, the current outputs from the voltage source are arbitrary, hence rows $k(even)$ and $k(odd)$ are discarded. At the present time, the application of difference amplifiers in SC networks in not considered especially practical for capacitor grounding reasons since no virtual earth exists at the input.

Consider the circuit of the lossy differentiator shown. Take the passive network alone, then following the rules given:

$$S^o = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad I^o = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

$$S^e = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad I^e = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix}$$

$$C = \begin{bmatrix} C_1 & -C_1 & 0 & 0 \\ -C_1 & C_1 + C_3 & 0 & -C_3 \\ 0 & 0 & C_2 & 0 \\ 0 & -C_3 & 0 & C_3 \end{bmatrix}.$$

Substituting in (1) gives:

$$\begin{bmatrix} \dot{I}_1^e \\ \dot{I}_2^e \\ \dot{I}_3^e \\ \dot{I}_4^e \\ \dot{I}_1^o \\ \dot{I}_2^o \\ \dot{I}_3^o \\ \dot{I}_4^o \end{bmatrix} = \begin{bmatrix} C_1 & -C_1 & 0 & 0 & -z^{-1}C_1 & z^{-1}C_1 & 0 & 0 \\ -C_1 & C_1 + C_3 & 0 & -C_3 & z^{-1}C_1 & -z^{-1}(C_1 + C_3) & 0 & z^{-1}C_3 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -C_3 & 0 & C_3 & 0 & -z^{-1}(C_2 - C_3) & 0 & -z^{-1}C_3 \\ -z^{-1}C_1 & z^{-1}C_1 & 0 & 0 & C_1 & -C_1 & 0 & 0 \\ z^{-1}C_1 & -z^{-1}(C_1 + C_3) & 0 & -z^{-1}(C_2 - C_3) & -C_1 & C_1 + C_2 + C_3 & 0 & -C_3 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & z^{-1}C_3 & 0 & -z^{-1}C_3 & 0 & -C_3 & 0 & C_3 \end{bmatrix} \begin{bmatrix} V_1^e \\ V_2^e \\ V_3^e \\ V_4^e \\ V_1^o \\ V_2^o \\ V_3^o \\ V_4^o \end{bmatrix}.$$

Eliminate zero columns and rows $3(even)$, $3(odd)$, to give $\dot{Y}_R$. Apply the amplifier constraints, hence remove columns $2(even)$, $2(odd)$ and rows $4\ (even)$, $4(odd)$ to give matrix Y_C

$$\begin{bmatrix} \dot{I}_1^e \\ \dot{I}_2^e \\ \dot{I}_1^o \\ \dot{I}_2^o \end{bmatrix} = \begin{bmatrix} C_1 & 0 & -z^{-1}C_1 & 0 \\ -C_1 & -C_3 & z^{-1}C_1 & z^{-1}C_3 \\ -z^{-1}C_1 & 0 & C_1 & 0 \\ z^{-1}C_1 & -z^{-1}(C_2 - C_3) & -C_1 & -C_3 \end{bmatrix} \begin{bmatrix} V_1^e \\ V_4^e \\ V_1^o \\ V_4^o \end{bmatrix}.$$

With even input sampling $V_1^o = 0$, $\dot{I}_1^o = 0$ so remove column and row $1(odd)$ and from the remaining matrix

$$G_{41}^{ee}(z) = \frac{V_4^e}{V_1^e} = \frac{\Delta_{12}}{\Delta_{11}} = \frac{C_1(1 - z^{-2})}{C_3 - z^{-2}(C_3 - C_2)}$$

which is the transfer function of a lossy differentiator.

For odd input sampling $V_1^e = 0$, $\dot{I}_1^e = 0$, so remove column and row $1(even)$ and from the remaining matrix

$$G_{41}^{oo}(z) = \frac{V_4^o}{V_1^o} = \frac{\Delta_{23}}{\Delta_{22}} = \frac{-C_1(1 - z^{-2}[C_3 - C_2])}{C_3(1 - z^{-2}[C_3 - C_2])} = -\frac{C_1}{C_3}$$

which, of course, is an inverting amplifier.

Matrix techniques can be applied to the analysis of active SC networks in a straightforward manner and afford a powerful approach for examination of the many performance functions of these networks. They have special significance in computer analysis since the task of generating equivalent circuits is avoided completely.

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well be replaced by the double d.f.t. processes.[5] However, this is not a matter for consideration, because the main purpose of this letter is to show how to apply the sampling theorem to s.a.w. filter analysis. The discussion can be applied easily to other time-consuming s.a.w. filter analysis, such as equivalent circuit analysis or bulk spurious response analysis, as long as τ_{min} and τ_{max} are determinable beforehand.

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INCLUSION OF AMPLIFIER FINITE GAIN AND BANDWIDTH IN ANALYSIS OF SWITCHED-CAPACITOR FILTERS

Indexing terms: Amplifiers, Switched-capacitor networks

The exact mathematical solution of the amplifier finite gain and bandwidth problem in switched-capacitor filter networks is presented. The theory is incorporated into a computer analysis program and typical results for a filter circuit are included.

The analysis and design of switched-capacitor (s.c.) networks is developing very rapidly. A matrix method for the analysis of active s.c. networks[1] affords a straightforward technique, particularly suited to implementation as a computer program. Ideal operational amplifiers have been considered, and finite but real amplifier admittance parameters are easily accommodated. The effects of frequency-dependent amplifier parameters, especially the gain, are very important and will be considered here.

For simplicity, take an s.c. network containing capacitances, operational amplifiers, and switches with half cycle operation (2-phase nonoverlapping clock); then the $2n \times 2n$ definite nodal matrix $\hat{Y}$ is determined from:

$$\begin{bmatrix} \hat{I}^1 \\ \hat{I}^2 \end{bmatrix} = \begin{bmatrix} \hat{Y}_p^{11} & \hat{Y}_p^{12} \\ \hat{Y}_p^{21} & \hat{Y}_p^{22} \end{bmatrix} \begin{bmatrix} \hat{V}^1 \\ \hat{V}^2 \end{bmatrix} + \begin{bmatrix} \hat{Y}_A^{11} & \hat{Y}_A^{12} \\ \hat{Y}_A^{21} & \hat{Y}_A^{22} \end{bmatrix} \begin{bmatrix} \hat{V}^1 \\ \hat{V}^2 \end{bmatrix}$$

or $\hat{I} = [\hat{Y}_p + \hat{Y}_A]V$.

$\hat{I}^1$, $\hat{I}^2$ and V^1, V^2 are the phase-1 and phase-2 currents and voltages; $\hat{Y}_p$ is the passive part matrix assembled in an accepted manner.[2] Because of frequency-dependent amplifier parameters, the active matrix $\hat{Y}_A$ will not have the simple form as indicated previously.[1]

For a typical operational amplifier, the gain can be expressed as $m = -a_0/(b_0 + b_1 s)$, a single pole in the s-domain. A simple voltage amplifier has a Y_A matrix given by

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ -my_{22} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

If y_{22} is assumed to be a real constant, normalised to unity, then in a switched network the frequency-dependent current term during any time interval n is given by

$$I_n = \frac{1}{T}(q_n - q_{n-1}) = \frac{1}{T}\int_{n-1}^{n} i(t)\,dt$$

$$= \frac{1}{T}\int_{n-1}^{n} \mathcal{L}^{-1}\left[\frac{a}{b_0 + b_1 s} V(s)\right] dt$$

where T is the sampling period. This becomes

$$I_n = \frac{a_0}{Tb_1}\int_{n-1}^{n}\int_{0}^{t} e^{-(b_0/b_1)(t-\tau)}V(\tau)\,d\tau\,dt$$

$$= \frac{a_0}{Tb_1}\int_{0}^{n} e^{-(b_0/b_1)t}\int_{0}^{t} e^{(b_0/b_1)\tau}V(\tau)\,d\tau\,dt$$

$$- \frac{a_0}{Tb_1}\int_{0}^{n-1} e^{-(b_0/b_1)t}\int_{0}^{t} e^{(b_0/b_1)\tau}V(\tau)\,d\tau\,dt$$

$$= -\frac{a_0}{Tb_0}\int_{0}^{n} e^{-(b_0/b_1)(n-\tau)}V(\tau)\,d\tau + \frac{a_0}{Tb_0}\int_{0}^{n} V(t)\,dt$$

$$+ \frac{a_0}{Tb_0}\int_{0}^{n-1} e^{-(b_0/b_1)(n-1-\tau)}V(\tau)\,d\tau - \frac{a_0}{Tb_0}\int_{0}^{n-1} V(t)\,dt$$

Let $a_0/b_0 T = \alpha$, $b_0/b_1 = \beta$, and since an s.c. network is a discrete system

$$I_n = -\alpha\sum_{i=0}^{n} e^{-\beta(n-i)}V(i) + \alpha\sum_{i=0}^{n} V(i)$$
$$+ \alpha\sum_{i=0}^{n-1} e^{-\beta(n-1-i)}V(i) - \alpha\sum_{i=0}^{n-1} V(i)$$

Applying the convolution theorem of the z-transformation[3] yields

$$I(z) = \frac{-\alpha V(z)}{1 - z^{-1}e^{-\beta T}} + \frac{\alpha V(z)}{1 - z^{-1}} + \frac{\alpha z^{-1}V(z)}{1 - z^{-1}e^{-\beta T}} - \frac{\alpha z^{-1}V(z)}{1 - z^{-1}}$$
$$= \alpha\frac{(z^{-1} - z^{-1}e^{-\beta T})V(z)}{1 - z^{-1}e^{-\beta T}}$$

This may be written as the sum of even and odd terms of a series:

$$I(z) = \alpha(z^{-1} - z^{-1}e^{-\beta T})V(z)\left\{\sum_{j=0}^{\infty} z^{-2j}e^{-2j\beta T} + \sum_{j=0}^{\infty} z^{-(2j+1)}e^{-(2j+1)\beta T}\right\}$$

or in closed form

$$I(z) = \frac{\alpha z^{-1}(1 - e^{-\beta T})V(z)}{(1 - z^{-2}e^{-2\beta T})} + \frac{\alpha z^{-2}(1 - e^{-\beta T})e^{-\beta T}}{(1 - z^{-2}e^{-2\beta T})}V(z)$$

Now $\hat{I} = \hat{I}^1 + \hat{I}^2$, and $V = V^1 + V^2$, so splitting the current equation into direct-phase and delayed-phase components gives

$$\hat{I}^1 = \frac{\alpha z^{-1}(1 - z^{-1}e^{-2\beta T})V^1(z)}{(1 - z^{-2}e^{-2\beta T})} - \frac{\alpha z^{-1}e^{-\beta T}(1 - z^{-1})V^2(z)}{(1 - z^{-2}e^{-2\beta T})}$$

$$\hat{I}^2 = \frac{\alpha z^{-1}(1 - z^{-1}e^{-2\beta T})V^2(z)}{(1 - z^{-2}e^{-2\beta T})} - \frac{\alpha z^{-1}e^{-\beta T}(1 - z^{-1})V^1(z)}{(1 - z^{-2}e^{-2\beta T})}$$

Each amplifier with a frequency-dependent gain will produce terms of this nature which contribute entries to all four partitions of $\hat{Y}_A$.

This theory has been incorporated into an analysis program for s.c. networks. Analysis of a number of active s.c. filter networks gives results which correspond to practical circuits using amplifiers of finite gain and bandwidth.

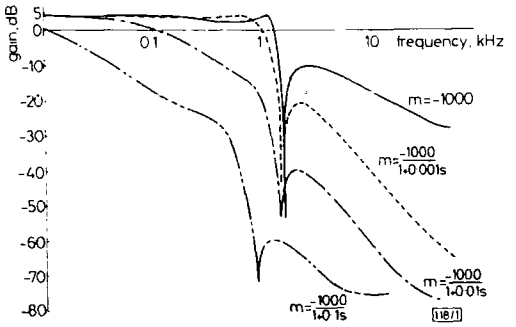

Fig. 1 *Response of third-order elliptic lowpass s.c. filter*

Typical computed responses obtained for a third-order elliptic s.c. filter[4] with a clock frequency of 100 kHz are shown in Fig. 1. The increasing distortion of the transfer function due to the amplifier limitations is clearly apparent.

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SIMPLE SELF-CENTRING TECHNIQUE FOR MOUNTING MICROSPHERE COUPLING LENS ON A FIBRE

Indexing terms: Optical fibres, Optical transmission

A simple and accurate self-centring method of mounting a microsphere coupling lens on a fibre endface is described. In over 85% of cases tried, the lenses were centred on the fibre axis to within 3 μm. The lenses yield a laser-fibre coupling efficiency of about 65%.

The light power which can be launched into an optical fibre from a diode laser by simple butt coupling is small, being limited by the fibre acceptance angle. Several coupling techniques have been reported which increase the coupling efficiency.[1,6] Of these, the microsphere lens glued onto the fibre endface provides one of the highest coupling efficiencies.[6] The high efficiency arises in part from the ability to select lenses of a particular radius and refractive index so as to approach optimum coupling. Also, the highly spherical quality of such microspheres[7] eliminates the type of curvature control problem involved in fabricating a lens at the end of the fibre.[1,3] However, the small microsphere lens size (typically 70–100 μm), combined with the need to centre the lens accurately (typically to within several micrometres) brings about difficulties in lens mounting.

The method reported previously for mounting microsphere lenses is the laser-light assisted alignment technique of Khoe *et al.*[8,9] In this technique, a laser beam is launched into a fibre and the output emission pattern is viewed on a screen. A microsphere lens is brought to the output end and is then positioned with high-accuracy micropositioners until the pattern becomes centred on the same point as the original pattern. It is then glued onto the fibre end.

This process is complicated, and it is quite difficult to hold the microsphere lens. We report here a simple, accurate and production-oriented technique for lens mounting. A typical microsphere lens attached to a fibre end is shown in Fig. 1. In the mounting procedure, the end of the fibre is first properly cleaved and cleaned, and adhesive is applied to it by dipping.

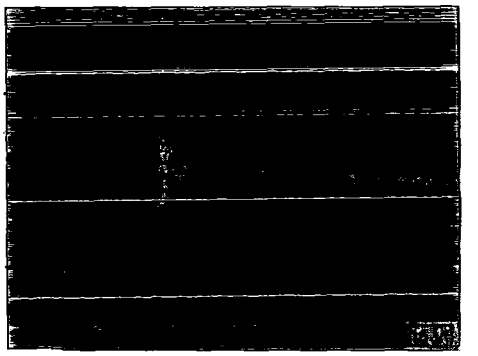

Fig. 1 *Photograph of mounted microsphere lens*

With the aid of micromanipulators and a low-power microscope, the fibre end is roughly centred over a microsphere lens and lowered so that the epoxy contacts the lens. The epoxy then holds on to the lens by surface tension so that it is picked up as the fibre moves upwards. Due to the combination of adhesive surface tension and gravity, the lens moves until it is on, or very close to, the fibre axis. Thus the technique can be described as self-centring.

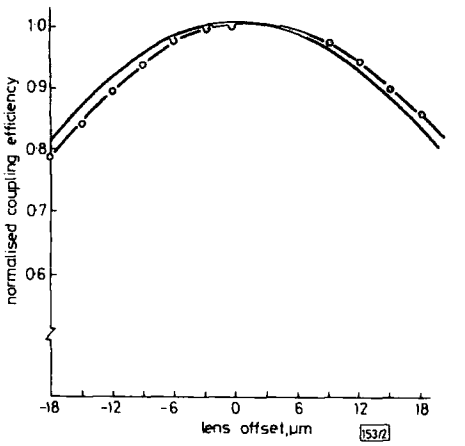

Fig. 2 *Calculated dependence of normalised coupling efficiency on lens offset. Curves for offset parallel and perpendicular to laser junction plane are shown*

——— parallel
—·— perpendicular

plastic, namely Delryn, was used to provide the required expansion as shown in Fig. 4. The dielectric disc is suspended on a stainless-steel screw to allow initial height adjustment. The length of the Delryn section was computed for $\Delta f = 40$ MHz over the temperature range -50 to $+100$°C. From Fig. 3*b*, 40 MHz compensation requires d to vary from 0 to 0·1 mm. The length L is then calculated from the formula

$$L = \frac{d}{\alpha \cdot \Delta T}$$

$$L = 7{\cdot}2 \text{ mm}$$

where α = coefficient of linear expansion = 9×10^{-5}/°C for Delryn.

The circuit in Fig. 2 has a total frequency change of only 16 MHz over the temperature range -50 to $+100$°C, in comparison with an uncompensated value of 48 MHz.

The degree of compensation can be altered by using either different materials or different dimensions for the differential expansion system and different physical sizes and dielectric constants for the disc. Thus trapatt diodes with different frequency/temperature characteristics can be accommodated in the design.

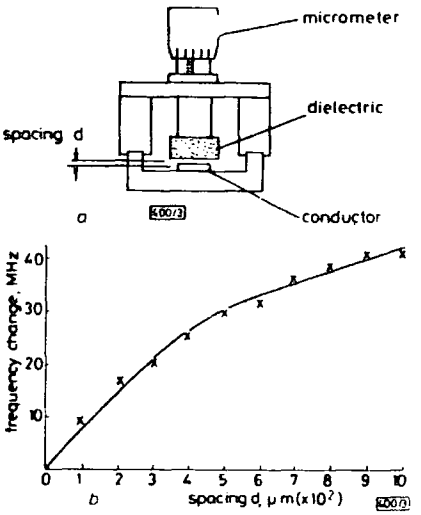

Fig. 3

a Calibration rig
b Frequency change against spacing

A similar arrangement of suspended dielectric disc but without the differential expansion system provides a convenient method of mechanically tuning the oscillator frequency. This could be incorporated at another point on the delay line and would then be totally independent of the compensation system.*

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8th June 1981

Reference

1 DAVIES, R., BOOTH, P., and NEWTON, B.: 'An improved TRAPATT oscillator', *IEEE Trans.*, 1980, **MTT-28**, p. 171

* Technique reported by the Plessey Co. some years ago on their FET MIC amplifiers.

ERRATA

Authors' corrections

WILSON, B.: 'Low-distortion high-output class B current convertor using error feedforward', *Electron. Lett.*, 1981 **17**, (13), pp. 461–463

In Fig. 1*a* the central box should read:

class D
dumper D

LAU, J., and SEWELL, J. I.: 'Inclusion of amplifier finite gain and bandwidth in analysis of switched-capacitor filters', *Electron. Lett.*, 1980, **16**, (12), pp. 462–463

In the final equation for I_n, halfway down column two of p. 462, the upper limits of the first two summations should read $n-1$, and the upper limits of the last two should read $n-2$.

The first and third terms of the next equation for $I(z)$ have an $e^{-\beta T}$ multiplier; this results in a common multiplier z^{-1} being removed from the remaining equations for $I(z)$. The final equations are therefore:

$$I^1 = \frac{\alpha(1-e^{-\beta T})V^1(z)}{1-z^{-2}e^{-2\beta T}} + \frac{\alpha z^{-1}e^{-\beta T}(1-e^{-\beta T})V^2(z)}{1-z^{-2}e^{-2\beta T}}$$

$$I^2 = \frac{\alpha(1-e^{-\beta T})V^2(z)}{1-z^{-2}e^{-2\beta T}} + \frac{\alpha z^{-1}e^{-\beta T}(1-e^{-\beta T})V^1(z)}{1-z^{-2}e^{-2\beta T}}$$

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PAPER 26

Digital active network analysis

F.G.A. Coupe, B.Sc., Ph.D., and J.I. Sewell, B.Sc., Ph.D., C.Eng., M.I.E.E., Sen. Mem.I.E.E.E.

Indexing terms: *Active networks, Filters, Analogue-digital conversion*

Abstract: An analysis technique is presented and developed which enables analogue active networks and digital filters to be combined into a new type of network, the digital active network. The potential effects of limit cycle noise are extensively considered and for a practical example both the results of computer analysis and actual measurements are given.

1 Introduction

Analogue active networks and their associated mathematics have been very extensively investigated in recent years, as have digital filters and sample data systems in general. This paper derives techniques for combining both topics in order to make a new range of circuit realisations, digital active networks.

A simple approach to this new technique could be to feed a digital filter with N input ports from N voltage sensors and feed the filter outputs to N current generators. By strapping the voltage sensor inputs to the current generator outputs, one type of N-port digital active network can be created. However, this does not meet the initial criterion of truly mixing analogue active networks with digital filters, and hence it is necessary to analyse the whole concept very carefully.

Digital active network theory may be used to extend greatly the theory of digital filters by enabling analogue components to be mixed with these filters, and by showing how the digital equivalent can be designed of gyrators, circulators, impedance convertors, impedance inverters and so on. The exact nature of every possible application cannot be explored in this paper.

However, it is the purpose of this paper to present a coherent analysis of digital active networks through which detailed applications may be designed. Conversely it is clear that there must be a theoretical basis which can describe what happens in a digital active network and so a coherent theory is a better start than an approximate design method.

2 Digital transadmittance amplifiers

In order to make an N-port digital active network it is most convenient to choose the admittance matrix as a starting point because of the ease with which transadmittance amplifiers (analogue or digital) may be designed.

Digital transadmittance amplifiers (d.t.a.) may be conveniently defined to follow their analogue counterparts, a block diagram being shown in Fig. 1. The presence of analogue-to-digital (a.d.) and digital-to-analogue (d.a.) convertors is not obligatory as charge-coupled (c.c.d.) or bucket-bridge (b.b.d.) devices could be used. However, they are included because they modify the stability of a digital admittance matrix. The overall transfer function of the d.t.a. may be defined as the pulse transfer function (p.t.f.) of the d.t.a., namely

$$y(z) = I(z)/V(z) = gf(z) \quad (1)$$

where g is the scaling constant and $f(z)$ is the digital-filter transfer function.

The scaling constant can be implemented as a 4-quadrant digital multiplier if sign reversal is required or defined by the reference voltage input to the d.a. convertor; this latter option will normally restrict the scaling to 2-quadrant operation.

Fig. 2 shows the block diagram of an arbitrary sampled analogue admittance. By definition

$$I(s) = H(s)\,V^*(s) \quad (2)$$

where $H(s)$ is the analogue Laplace-domain transfer function and $V^*(s)$ the sampled Laplace input voltage. In order to analyse the output state at the sampling instants it is expedient to hypothetically sample, thus

$$I^*(s) = [H(s)V^*(s)]^* \quad (3)$$

which is conventionally rewritten

$$I^*(s) = H^*(s)V^*(s) \quad (4)$$

However, the sampling of a Laplace variable may be written thus[1,2,3]

$$V^*(s) = \frac{1}{T_s}\sum_{r=-\infty}^{\infty} V(s + jrw_s) \quad (5)$$

where T_s is the sampling period and thus the sampling process has modified the units of $V^*(s)$ by dividing by time. Thus, to correct for this, eqn. 4 must be rewritten as

$$I^*(s) = T_s H^*(s)V^*(s) \quad (6)$$

This point has been mentioned but not derived.[4]

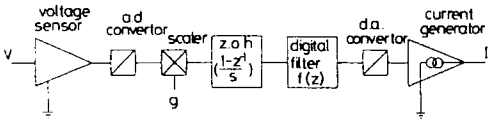

Fig. 1 *Block diagram of digital amplifier*

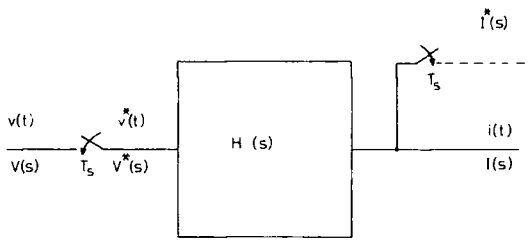

Fig. 2 *Sampled analogue admittance*

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Now $H(s)$ may be defined generally:

$$H(s) = \frac{\sum_{i=0}^{n} a_i s^i}{\sum_{i=0}^{m} b_i s^i} \tag{7}$$

and $H^*(s)$ defined using eqn. 5:

$$H^*(s) = \frac{1}{T_s} \sum_{r=-\infty}^{\infty} H(s + jrw_s) \tag{8}$$

When $n > m$, the series for $H^*(s)$ is divergent and hence $H^*(s)$ cannot be found; $H(s)$ may be said to be untransformable.

By the same definition

$$\left[\frac{1}{H(s)}\right]^* = T_s \sum_{r=-\infty}^{\infty} \left\{\frac{1}{H(s + jrw_s)}\right\} \tag{9}$$

When $n \geqslant m$, the series for $\{1/H(s)\}^*$ is now convergent, and hence $1/H(s)$ is transformable.

Now consider the product of two Laplace transfer functions $H_1(s)$ and $H_2(s)$ where

$$H(s) = H_2(s)H_2(s) \tag{10}$$

If $H_1^*(s)$ and $H_2^*(s)$ can be found then $H^*(s)$ can also be found. However, if either cannot be found then neither can $H(s)$ be found.

Now the network in Fig. 2 has been arbitrarily defined such that $H(s)$ is an admittance, but it may be rearranged as in Fig. 3 to become an impedance and hence eqn. 6 can be rewritten as

$$V^*(s) = \frac{1}{T_s H^*(s)} I^*(s) \tag{11}$$

Thus the Z-transform may be written

$$I(z)|_{n \leqslant m} = T_s H(z) I(z) \tag{12}$$

$$I(z)|_{n > m} = T_s \frac{1}{Z\left[\frac{1}{H(s)}\right]} I(z) \tag{13}$$

This result is important in the analysis which follows.

3 Digital admittance matrix

A digital admittance matrix may be formed by interconnecting digital amplifiers such that each digital amplifier simulates an element of an admittance matrix. As each digital amplifier would normally contain an a.d. and d.a. convertor, a considerable simplification can be made by using only one a.d. convertor at each port which feeds each digital amplifier in any given column. Furthermore the output of each digital amplifer in any given row can be added before d.a. conversion. Another simplification would be to multiplex the d.a. convertor used in the voltage sensing a.d. convertor for use as the current generating d.a. convertor.

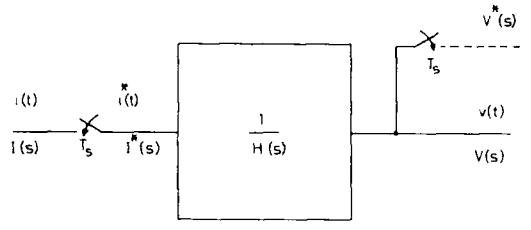

Fig. 3 *Sampled analogue impedance*

A digital admittance matrix has been defined as the pulse transfer function of each element of the analogue admittance matrix. Now by definition each element of the analogue admittance matrix convolves with either a sampled or unsampled port voltage:

$$I(s) = Y_1(s)V(s) + Y_2(s)V^*(s) \tag{14}$$

where each variable is now defined as a matrix.

As $Y_2(s)$ represents the transfer functions of the digital amplifers present it is intrinsically possible to find $Y_2^*(s)$ and hence $Y_2(z)$. Now in order to analyse the state of the N output currents at the sampling instants it is convenient to introduce hypothetical samplers which will sample both the input voltage and output current at each port. Thus eqn. 14 becomes

$$\begin{aligned} I^*(s) &= [Y_1(s)V^*(s)]^* + [Y_2(s)[V^*(s)]^*]^* \\ &= T_s[Y_1^*(s) + Y_2^*(s)]V^*(s) \end{aligned} \tag{15}$$

If $Y_1^*(s)$ can be found then the Z-transform of eqn. 15 produces the digital admittance matrix $Y(z)$:

$$Y(z) = T_s Z\{Y(s)\} \tag{16}$$

If any element of $Y_1(s)$ cannot be transformed then $Y(s)$ must be manipulated to produce a transformable admittance matrix. Eqn. 13 showed that the inverse of the transform of the inverse could be used instead. This may be applied to $Y(s)$ by dividing through the row containing the untransformable element by that element and may be repeated as may times in a row as necessary.

This may be done in matrix form by defining a diagonal matrix with elements consisting of the products of the untransformable elements in $Y_1(s)$:

$$Y_U = \begin{bmatrix} y_1 & 0 & \cdots & 0 \\ 0 & y_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & y_n \end{bmatrix} \tag{17}$$

where the general element y_i may be defined:

Y_i = (product of untransformable elements in ith row)

Now, by definition,

$$Y_1(s) = Y_U Y_U^{-1} Y_{1(s)} \tag{18}$$

However, the term $Y_U^{-1} Y_1(s)$ is transformable because dividing through by the untransformable elements yields an entirely transformable matrix. Thus eqn. 14 becomes

$$Y_U^{-1} I(s) = [Y_U^{-1} Y_1(s)V(s) + Y_U^{-1} Y_2(s)V^*(s)] \tag{19}$$

and, after hypothetical sampling,

$$T_s[Y_U^{-1}]^* I^*(s) = [Y_U^{-1} Y(s)]^* V^*(s) \tag{20}$$

Each sampled term may now be Z-transformed to give the digital admittance matrix:

$$Y(z) = \frac{1}{T_s}[Z\{Y_U^{-1}\}]^{-1}[Z\{Y_U^{-1}Y(s)\}] \quad (21)$$

The digital impedance matrix may be similarly derived by rearranging eqn. 20 before taking the Z-transform:

$$Z(z) = T_s[Z\{Y_U^{-1}Y(s)\}]^{-1}[Z\{Y_U^{-1}\}] \quad (22)$$

and this is clearly the inverse of eqn. 21.

In order to use conventional definitions, $Z(z)$ is used to mean the digital impedance matrix, and may be distinguished from the process of taking the Z-transform such as $Z\{Y_U^{-1}\}$ by the type of brackets used. Hence whatever mixture of analogue components and digital amplifiers has been chosen, it is always possible to find the digital admittance and impedance matrices, providing of course that one or other is not singular.

4 Limit cycle noise

If the digital amplifiers within a digital active network incorporate amplitude quantisation because of a.d. and d.a. convertors then this effect may be conventionally represented as uncorrelated noise inputs to each digital amplifer.[5] Hence quantisation noise will also be present as a noise current at the output of each digital amplifier, and these noise currents may excite the whole digital active network to show limit cycle oscillations.

For the purpose of this analysis all N a.d. convertors in an arbitary N-port digital active network will be assumed to be identical, that is they have the same number of equal sized quantisation steps which are also aligned. If these quantisation levels are not aligned then quantisation noise can be serious, but the amplitude of any noise effect at any frequency can be predicted and enough bits used in the a.d. convertors to reduce these effects to an acceptable level.

Consider an admittance matrix $Y_N(s)$ consisting of only those elements of $Y(s)$ derived from digital amplifiers which include amplitude quantisation. Thus the noise output current $I_N(s)$ will be

$$I_N(s) = Y_N(s)V_N^*(s) \quad (23)$$

By taking the Z-transform

$$I_N(z) = Y_N(z)V_N(z) \quad (24)$$

Now $I_N(z)$ will excite the whole digital active network by way of the digital impedance matrix:

$$V_0(z) = Z(z)Y_N(z)V_N(z) \quad (25)$$

and thus a voltage transfer matrix $A_N(z)$ may be defined:

$$A_N(z) = Z(z)Y_N(z) \quad (26)$$

Now the elements of the column vector $V_N(z)$ will all be equal by the present definition. Furthermore the elements of $V_0(z)$ are also inputs to the same digital amplifier. Thus $V_N(z)$ will become a column vector with all elements set to 1, and scaled by an r.m.s. voltage V_s related to the quantisation step size ΔV:

$$V_s = \sqrt{\frac{(\Delta V)^2}{12}} \quad (27)$$

Hence $A_N(z)$ is superseded by a voltage-transfer vector $Q_N(z)$ where

$$q_j(z) = \sum_{i=1}^{N} a_{ij}(z) \quad (28)$$

and $q_j(z)$ is the jth element of $Q_N(z)$.

Now the whole digital active network will display limit-cycle oscillations if at any frequency

$$|q_j(z)| > 1 \quad (29)$$

z may take any value within the Nyquist range that maximises $|q_j(z)|$. However, the necessary value to cause oscillation must lie between 1 and 2 because although the noise will have been amplified by $q_j(z)$, it will not have exceeded another quantisation boundary. Thus

$$|q_j(z)| \geqslant k \quad (30)$$

where $1 < k \leqslant 2$.

If the a.d. convertors are accurately aligned then k takes its maximum value and eqn. 30 may be rewritten

$$|q_j(z)| \geqslant 2 \quad (31)$$

Any mismatch in the a.d. convertors will reduce the value of k causing the digital active network to be potentially more unstable. A special case occurs if every element of $Y(s)$ is derived from a digital amplifer:

$$Y_N(z) = Y(z) \quad (32)$$

and hence

$$A_N(z) = U \quad (33)$$

where U is the identity matrix; U is used to avoid confiicting with the current vector I. Thus under these conditions eqn. 31 can never be satisfied because

$$|q_j(z)| = 1 \quad (34)$$

Hence a digital active network constructed solely from digital amplifiers cannot show limit cycle noise providing that a.d. convertors are identical and aligned.

The limit cycle oscillation analysis has considered only the effect of amplitude quantisation producing amplified quantisation noise. The actual amplitude depends on the absolute size of ΔN and thus, for a given dynamic range, a large number of quantisation levels is preferable. The presence of numerical round-off in the other stages of the digital amplifier will also affect the limit-cycle criterion.[6,7,8,9] However, coefficient accuracy will only be a problem in digital active networks[10] if the coefficients

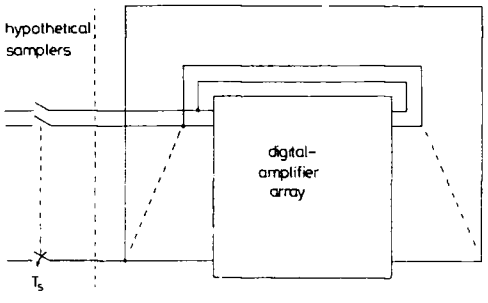

Fig. 4 *Digital-amplifier array*

in each element come from digital filters rather than from analogue circuit components, because the latter have values which cannot be rounded off.

5 Element resolution

In a digital amplifier the presence of an amplitude quantiser introduces an uncertainty into any attempted measurement of the transadmittance. Hence the overall amplifier operation may be written as

$$I_i + \Delta I = (y_{ij} + \Delta y_{ij})(V_j + \Delta V) \tag{35}$$

for the element y_{ij}. The fractional error in y_{ij} will be

$$\left.\frac{\Delta y_{ij}}{y_{ij}}\right|_{max} = \frac{\Delta I}{I_i} + \frac{\Delta V}{V_j} \tag{36}$$

However, by definition $\Delta V < \frac{1}{2}$ l.s.b. and thus I will not change, making $\Delta I = 0$. Hence

$$\left.\frac{\Delta y_{ij}}{y_{ij}}\right|_{max} = \frac{\Delta V}{V_j} \tag{37}$$

However, $V_j/\Delta V$ is the number of quantisation levels M in the a.d. convertor and thus

$$\left.\frac{\Delta y_{ij}}{y_{ij}}\right|_{max} = \frac{1}{M} \tag{38}$$

Hence no digital amplifier transadmittance may be measured to an accuracy greater than $\frac{1}{M}$.

6 Example: digital gyrator

A 2-port capacitively loaded digital gyrator forms a suitable example to illustrate the analysis of a digital active network, and it is shown in Fig. 5. The basic equations describing the gyrator may be written down:

$$\begin{aligned} I_1(s) &= (g + sC_1)V_1(s) + f_1(s)\,V_2^*(s) \\ I_2(s) &= -f_2(s)V_1^*(s) + sC_2\,V_2(s) \end{aligned} \tag{39}$$

where

$$f_1(s) = g_1\left\{\frac{1-\exp(-sT_s)}{s}\right\}\exp(-sK_1T_s)$$

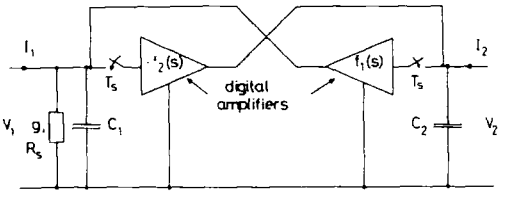

Fig. 5 *Two-port capacitively loaded digital gyrator*

$$f_2(s) = -g_2\left\{\frac{1-\exp(-sT_s)}{s}\right\}\exp(-sK_2T_s)$$

Now by definition $(g + sC_1)$ and sC_2 cannot be transformed and thus Y_U may be written as

$$Y_U(s) = \begin{bmatrix} (g+sC_1) & 0 \\ 0 & sC_2 \end{bmatrix} \tag{40}$$

Thus the inverse is

$$Y_U^{-1}(s) = \begin{bmatrix} \dfrac{1}{g+sC_1} & 0 \\ 0 & \dfrac{1}{sC_2} \end{bmatrix} \tag{41}$$

Further

$$Y_U^{-1}(s)Y(s) = \begin{bmatrix} 1 & g_1\dfrac{\{1-\exp(-sT_s)\}}{s(g+sC_1)}\exp(-sK_1T_s) \\ -g_2\dfrac{\{1-\exp(-sT_s)\}}{s^2C_2}\exp(-sK_2T_s) & 1 \end{bmatrix} \tag{42}$$

Eqn. 41 may be Z-transformed to give

$$Y_U^{-1}(z) = \begin{bmatrix} \dfrac{1}{C_1}\left(\dfrac{z}{z-\alpha}\right) & 0 \\ 0 & \left(\dfrac{1}{C_2}\dfrac{z}{z-1}\right) \end{bmatrix} \tag{43}$$

where

$$\alpha = \exp(-gT_s/C_1) \tag{44}$$

Eqn. 42 similarly gives

$$Z\{Y_U^{-1}(s)Y(s)\} = \begin{bmatrix} 1 & \dfrac{g_1}{g}z^{-K_1}\left(\dfrac{1-\alpha}{z-\alpha}\right) \\ -\dfrac{g_2}{C_2}T_s\dfrac{z^{-K_2}}{z-1} & 1 \end{bmatrix} \tag{45}$$

Thus $Y(z)$ may now be obtained

$$Y(z) = \frac{1}{T_s}\begin{bmatrix} C_1\left(\dfrac{z-\alpha}{z}\right) & g_1C_1\dfrac{(1-\alpha)z^{-K_1-1}}{g} \\ -g_2T_sz^{-K_2-1} & C_2\left(\dfrac{z-1}{z}\right) \end{bmatrix} \tag{46}$$

and by inversion

$$Z(z) = T_s \frac{\begin{bmatrix} \frac{z^{K_1+K_2+1}(z-1)}{C_1} & -g_1 z^{K_2+1}\frac{(1-\alpha)}{gC_2} \\ \frac{g_2 T_s}{C_1 C_2} z^{K_1+1} & \frac{z^{K_1+K_2+1}(z-\alpha)}{C_2} \end{bmatrix}}{M(z)} \quad (47)$$

where

$$M(z) = z^{K_1+K_2}(z-1)(z-\alpha) + T_s\frac{(1-\alpha)g_1 g_2}{gC_2} \quad (48)$$

The digital gyrator as defined is a mixture of analogue components and digital amplifiers, and thus it is possible that limit-cycle oscillations may be present with certain sets of component values. Thus the voltage-transfer vector (see Section 4) must be derived.

$Y_N(z)$ may be written down thus

$$Y_N(z) = \begin{bmatrix} 0 & g_1 z^{-K_1} \\ -g_2 z^{-K_2} & 0 \end{bmatrix} \quad (49)$$

and thus the noise-voltage-transfer matrix $A_N(z)$ will be

$$A_N(z) = T_s \frac{\begin{bmatrix} \frac{g_1 g_2(1-\alpha)z}{gC_2} & \frac{g_1 z^{K_2+1}(z-1)}{C_1} \\ \frac{-g_2^{(z-\alpha)z^{K_1+1}}}{C_2} & \frac{g_1 g_2 T_s z}{C_1 C_2} \end{bmatrix}}{M(z)} \quad (50)$$

Thus the voltage-transfer vector $Q_N(z)$ may be written

$$Q_N(z) = T_s \frac{\begin{bmatrix} \frac{g_1}{C_1} z^{K_2+1}(z-1) + \frac{g_1 g_2(1-\alpha)z}{gC_2} \\ \frac{-g_2}{C_2}(z-\alpha)z^{K_1+1} + \frac{g_1 g_2 T_s z}{C_1 C_2} \end{bmatrix}}{M(z)} \quad (51)$$

In order to determine whether limit-cycle oscillations can be present theoretically, the two elements of the above vector must be evaluated for a range of frequencies, for values of z, and for various values of the components g, g_1, g_2, C_1 and C_2.

In order to verify the theoretical analysis the two elements z_{11} and z_{21} of the digital impedance matrix were studied for a particular set of component and parameter values shown in Table 1 by computer program and practical experiment.

Table 1: Component values for digital gyrator example

Parameter	Parameter meaning	Value
f_s	sampling frequency	26·6 kHz
T_s	sampling period	18·75 μs
C_1	port-1 shunt capacitance	9·6 μF
C_2	port-2 shunt capacitance	10 μF
g_1, g_2	transconductances	10 mS
R_s	port-1 shunt resistance	50, 100, 200, 300 400, 500 Ω
K_1, K_2	fractional delay	1

7 Computer analysis

The denominator $\{M(z)\}$ of the digital impedance matrix in eqn. 48 was analysed to find the pole positions, and the modulus of the roots nearest the unit circle are listed in Table 2. Clearly these roots will lie within the unit circle and hence the digital gyrator will be stable.

Table 2 also shows the resonant frequency and the magnitude of z_{11} and z_{21} at that frequency. Figs. 6 and 7 show the frequency responses for the magnitudes of z_{11} and z_{21} as a continuous line. From the prediction in eqn. 31 no limit cycle noise is to be expected with the shunt resistor set to 50 or 100 Ω. A noise voltage will occur, however, when the gyrator is excited by an external signal generator with the shunt resistance set to 100 Ω, but this will not be self sustaining.

Table 3 shows the limit-cycle noise-voltage peak gains at the two ports of the digital gyrator together with the expected r.m.s. noise voltage. This assumes a quantisation step size of 125 mV which gives an r.m.s. noise voltage of 36·1 mV. With the shunt resistance set to 50 Ω no peak in either voltage gain was discernible. No account has been taken of the filtering effect of the resonance of the capacitively loaded digital gyrator.

8 Practical experiment

A digital machine was constructed (Fig. 5) which consisted

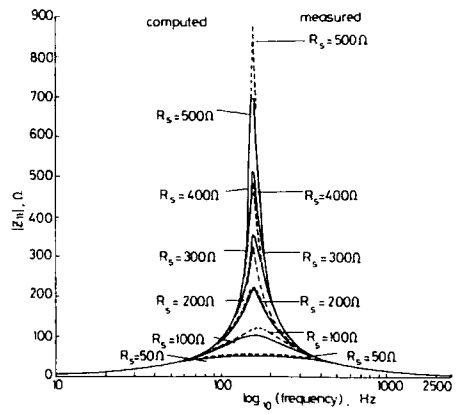

Fig. 6 *Computed and measured frequency response for z_{11}*

Table 2: Results from computer analysis of digital gyrator

Sampling period = 18·75 μs	Shunt resistance, Ω					
	50	100	200	300	400	500
modulus of largest denominator root	0·9812	0·9908	0·9957	0·9973	0·9981	0·9986
resonant frequency, Hz	162·11	162·11	162·11	162·11	162·11	162·11
Z_{11} peak impedance, Ω	52·46	107·00	226·46	362·08	517·26	697·07
Z_{21} peak impedance, Ω	–	–	227·97	358·64	509·79	685·13

Table 3: Predicted limit cycle noise amplitude

	Shunt resistance, Ω					
	50	100	200	300	400	500
port-1 voltage gain	–	1·5209	3·1389	5·0019	7·1406	9.6166
port-1 r.m.s. noise voltage, mV	–	54·9	113·3	180·5	257·7	347·0
port-2 voltage gain	–	1·0474	2·4929	4·2852	6·3671	8·7841
port-2 r.m.s. noise voltage, mV	–	37·8	90·0	154·6	229·8	317·0

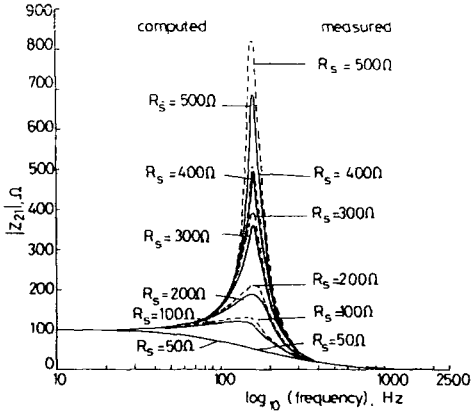

Fig. 7 *Computed and measured frequency response for* z_{21}

of two cross-coupled identical digital amplifiers. Each digital amplifier contained a 5-bit voltage-sensing a.d. convertor, or 4-quadrant digital multiplier and a 10-bit current generating d.a. convertor. The relevant parameters and component values are shown in Table 1.

The digital amplifiers were aligned by setting the input to the 4-quadrant multiplier to maximum and adjusting the current generating d.a. convertor reference voltage until a transconductance of 10 mS was obtained. The a.d. convertor was multiplexed between the two amplifiers but because of circuit complexities two separate d.a. convertors were used.

The frequency responses for the magnitude of the digital-input impedance z_{11} and forward-transfer impedance z_{21} were measured and are plotted in Figs. 6 and 7 as a broken line. The measured frequency responses have taken into account the limit cycle oscillations present when $R_g = 200$, 300, 400 and 500 Ω. These oscillations were found as theory predicted.

9 Conclusions

The main advantage of digital active networks are that they extend digital filters to include both passive analogue components and active analogue circuit configurations. They do not enhance, strictly, analogue active networks because the presence of even one sampling stage in a network means that digital-filter analysis techniques must be employed.

The extension to digital filters is fundamental, because whereas a digital filter may be regarded as processing the complete signal, the digital active network partitions the signal into measures of voltage and current. Hence the conventional analogue concept of impedance, admittances etc. can be extended to make digital impedances, digital admittances etc. This does not apply to ordinary digital filters.

Hence with the advent of digital active networks, digital filters are now able to perform all the funcitons and have all the properties of their analogue counterparts.

10 Acknowledgment

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COMPACT MATRIX SCHEME FOR USE IN COMPUTER ANALYSIS OF SWITCHED-CAPACITOR NETWORKS

Indexing terms: Circuit theory and design, Switched-capacitor networks, Computer analysis

The matrices that normally occur in the analysis of multiphase switched-capacitor networks are quite large and very sparse. A technique is presented which reduces the matrix order and increases the fill. Storage requirements are minimised and the arithmetic handling of large arrays is reduced without recourse to sparse matrix procedures.

For the analysis of multiphase switched-capacitor (SC) networks a number of basic matrix representations are possible. The modified nodal approach (MNA) does have advantages deriving from the structure of the matrix, but will generally require manipulation to avoid singularities and sparse techniques to improve the numerical routines. Here a definite nodal admittance method[1–3] is favoured since it allows simple reduction in order and increased fill techniques to be implemented. Network parameters can be computed in a straightforward manner by condensation and cofactor techniques.

For a multiphase SC network, the T_c periodic clock signal (the total period over which all the switching sequences are completed), is divided into p basic time intervals of length $T = T_c/p$. During each basic time interval no switch signal is varied. Let I^i, V^i $(1 \le i \le p)$ be the nodal current and voltage vectors for each basic time interval, and for the kth clock interval define $I_k^i = (\{kp + (i-1)\}T)$ and $V_k^i = V(\{kp + (i-1)\}T)$. Then, for one complete cycle,

$$I_k^1 = \frac{[C]}{T}\{V_k^1 - V_{k-1}^p\}$$

$$I_k^2 = \frac{[C]}{T}\{V_k^2 - V_k^1\}$$

$$\vdots \qquad \vdots$$

$$I_k^p = \frac{[C]}{T}\{V_k^p - V_k^{p-1}\}$$

where C is the definite capacitance matrix of the network; it is very easy to write down by inspection and is easily assembled in a program. Let $Y^{ij} = [C^{ij}]/T$ relate the currents during interval i and voltages during interval j.

Applying the z-transformation gives the matrix

$$\begin{bmatrix} I^1 \\ I^2 \\ I^3 \\ \vdots \\ I^p \end{bmatrix} = \begin{bmatrix} Y^{11} & 0 & 0 & \cdots & 0 & -z^{-1}Y^{1p} \\ -z^{-1}Y^{21} & Y^{22} & 0 & & 0 & 0 \\ 0 & -z^{-1}Y^{32} & Y^{33} & & 0 & 0 \\ \vdots & & & & & \\ 0 & 0 & 0 & & -z^{-1}Y^{pp-1} & Y^{pp} \end{bmatrix} \begin{bmatrix} V^1 \\ V^2 \\ V^3 \\ \vdots \\ V^p \end{bmatrix}$$

or $I = YV$.

The C^{ij} are of lower order than C in general and can be derived from it by contraction representing the switching process. The nodes in the reduced matrix are renumbered to generate a minimal set M^i for time interval i. Repeating this for all the time intervals introduces a global minimal set of nodes M_G and a minimal set of equations. For a network $\mathcal{N}$ with N physical nodes, the total number of relevant nodes in a time interval is $m^i = N - n_s^i$, where n_s^i is the number of switches closed during interval i; then $M^i = \{1, 2, 3 \ldots m^i\}$, and the total number of rows or columns in Y is $\bar{m} = \sum_{i=1}^{p} m^i$. For sensitivity and other studies it is essential not to lose the original node identities, so an index vector is used to record all movements of rows and columns. The complete index vector is a concatenation of the interval index vectors and simply maps the definite capacitance matrix C into all the Y^{ij}.

However, it is apparent that Y will still be a very sparse matrix. Sparse techniques could be used, but these can be avoided by the following method. Note that all the on-diagonal partitions of Y are frequency independent and that all off-diagonal portions have a z^{-1} multiplier and are frequency dependent. Commence with interval p and remove, by pivotal condensation, all nodes apart from the input and output nodes and any others to be retained for sensitivity calculations and the like. This yields a matrix of the form

$$\begin{bmatrix} Y_r^{11} & 0 & 0 & \cdots & 0 & z^{-2}Y_r^{1,p-1} & -z^{-1}Y_r^{1p} \\ -z^{-1}Y^{21} & Y^{22} & 0 & & 0 & 0 & 0 \\ 0 & z^{-1}Y^{32} & Y^{33} & & 0 & 0 & 0 \\ \vdots & & & & & & \\ 0 & 0 & 0 & & -z^{-1}Y^{p-1,p-2} & Y_r^{p-1,p-1} & 0 \\ 0 & 0 & 0 & \cdots & 0 & -z^{-1}Y_r^{p,p-1} & Y_r^{pp} \end{bmatrix}$$

where Y_r^{ij} indicates a reduced matrix. This process is repeated down to interval 2 and yields

$$\begin{bmatrix} Y^{11} + (-1)^p z^{-p} Y_r^{11} & (-1)^{p-1} z^{-(p-1)} Y_r^{12} & (-1)^{p-2} z^{-(p-2)} Y_r^{13} & \cdots & -z^{-1}Y_r^{1p} \\ -z^{-1}Y^{21} & Y^{22} & (-1)z^{-p}Y^{23} & \cdots & z^{-1}Y_r^{2p} \\ z^{-2}Y^{31} & -z^{-1}Y_r^{32} & Y_r^{33} & \cdots & -z^{-2}Y_r^{3p} \\ \vdots & & \vdots & & \vdots \\ (-1)^{p-1} z^{-(p-1)} Y_r^{p1} & (-1)^{p-2} z^{-(p-2)} Y_r^{p2} & (-1)^{p-3} z^{-(p-3)} Y_r^{p3} & \cdots & Y_r^{pp} \end{bmatrix} = \hat{Y}$$

$\hat{Y}$ is much more compact than Y, of lower order and greater density. In fact Y need never be created, the submatrices of $\hat{Y}$ can be generated sequentially when needed and the space reused for other submatrices in the successive condensation steps. For transfer function calculations only array storage of $[m^{(1)} + 2(p-1)]^2 + [m^{(1)}]^2$ is required, compared with $\bar{m}^2$ for Y.

Ordinary operational amplifiers without frequency dependence can be accommodated very easily.[3] Since the operation of both is continuous and without storage, a typical current equation becomes

$$I^i((n+1)T) = \frac{[C]}{T}\{V^i((n+1)T) - V^{i-1}(nT)\} + [Y_A]V^i((n+1)T)$$

The definite matrix Y_A contains all the conductance terms due to the amplifiers in the network. Only the Y^{ii} submatrices will contain terms from Y_A and their inclusion via the index vector follows the pattern outlined.

Having assembled $\hat{Y}$, the sampled transfer functions are computed, first by further pivotal condensation of internal nodes from the top left-hand submatrix. Multiple sampled transfer functions exist, p^2 in theory, in practice only a limited number of these may be of importance, but a general program must have the capability of computing all the accessible transfer functions or whichever ones are specified by a user. Consider one input time interval excitation and compute all the transfer functions with respect to output voltages at all the time intervals. This is accomplished by setting to zero all the unwanted input excitations, other than I_{in}^i and V_{in}^i, say. Removing all the rows and columns corresponding to these entries gives a reduced matrix Y_R.

$$\begin{bmatrix} I_{out}^1 \\ I_{out}^2 \\ \vdots \\ I_{in}^i \\ I_{out}^i \\ \vdots \\ I_{out}^p \end{bmatrix} = [Y_R] \begin{bmatrix} V_{out}^1 \\ V_{out}^2 \\ \vdots \\ V_{in}^i \\ V_{out}^i \\ \vdots \\ V_{out}^p \end{bmatrix}$$

By this stage Y_R is small, and application of Cramer's rule is quite efficient giving the transfer function $H^{ij} = (\Delta_R^{ij}/\Delta_R^{ii})\ \forall\ j$.

The calculation of Δ_R^{ii} is required once. The process is repeated for transfer functions with respect to all input time intervals. The frequency loop is deferred until this stage when the size of matrix is an absolute minimum; this leads to computations of maximum speed and accuracy. Scaling of matrices is used throughout to ensure maximum accuracy.

This routine has been implemented in the program SCNAP 2, and improvements in speed by a factor of 3 over that experienced with program SCNAP[4] on 2-phase SC circuits have been achieved. On an ICL 1904s computer analysis of multiphase examples yielded encouraging performance figures, for a 5th-order elliptic filter[5] (four time slots, 20 nodes), 56K store and 0·3 s/frequency point, and for a 7th-order Chebyshev filter[6] (six time slots, 31 nodes), 60K store and 0·8 s/frequency point. Comparative figures from the same program mounted on an IBM 360/195 show speed increases by a factor of 10 but at some cost to storage.

For amplifiers with frequency dependence the matrices no longer retain features that permit a compact formulation. More general routines have to be used and no simple time-saving techniques can be invoked.

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FIRST-ORDER THEORY OF THE FIVE-PORT SYMMETRICAL STAR JUNCTION

Indexing terms: Microwave circuits and systems, Reflectometers

It is shown that, from the three conditions of (*a*) five-fold symmetry, (*b*) reciprocity and (*c*) freedom from loss, useful constraints can be found on the elements of the scattering matrix of a symmetrical five-port star junction. These constraints can be used to set limits to the possible positions q_i of the centres of the q-circles when the five-port junction is used as an element in a six-port reflectometer.

Introduction: Hansson and Riblet[1] have demonstrated that a five-port symmetrical star junction can be used as a key component in a six-port reflectometer of the kind described by Engen in an excellent review article.[2] The basic properties of such junctions have been known for many years, and were elegantly derived by Montgomery *et al.*[3] from symmetry considerations.

The principal result is that, if the five-port junction is completely matched, power entering any one port will be equally shared amongst the other four ports if they are terminated by matched loads. Moreover, the phase difference between a port adjacent to the source port and a port not adjacent to the source is 120°.

In the reflectometer application, the five-port is connected as shown in Fig. 1.

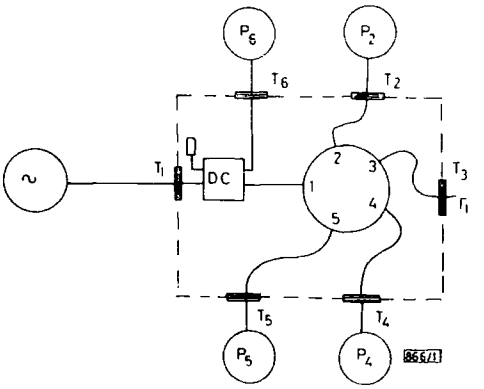

Fig. 1 *5-port junction in 6-port reflectometer instrument*

The unknown is connected to port 3 and its reflection coefficient Γ_1 is determined by the intersection of three circles whose radii are found from the powers P_2, P_4 and P_5 normalised to the forward power P_6.

If the junction is perfect, if the power meters are perfectly matched, and if the directional coupler DC is perfect the centres of the circles will be at -2 and at $2\exp[\pm j(\pi/3)]$ in the complex reflection-coefficient plane. A change in the reference planes, maintaining symmetry, will simply rotate the three centres around the origin without changing their relative positions.

We ask how far from these ideal positions the centres may move if the five-port whilst remaining symmetrical, reciprocal and loss-free, is not perfectly matched, again assuming a perfect directional coupler and perfectly matched power meters. We assume, therefore, that its scattering matrix can be written in the form

$$[S] = \begin{bmatrix} \gamma & \alpha & \beta & \beta & \alpha \\ \alpha & \gamma & \alpha & \beta & \beta \\ \beta & \alpha & \gamma & \alpha & \beta \\ \beta & \beta & \alpha & \gamma & \alpha \\ \alpha & \beta & \beta & \alpha & \gamma \end{bmatrix} \tag{1}$$

from which the unitary matrix condition gives the following equations:

$$\left.\begin{aligned} |\gamma|^2 + 2|\alpha|^2 + 2|\beta|^2 &= 1 \\ \gamma\alpha^* + \alpha\gamma^* + \alpha\beta^* + \beta\alpha^* + \beta\beta^* &= 0 \\ \gamma\beta^* + \beta\gamma^* + \alpha\beta^* + \beta\alpha^* + \alpha\alpha^* &= 0 \end{aligned}\right\} \tag{2}$$

The ideal values of α and β are

$$\left.\begin{aligned} \alpha_0 &= \tfrac{1}{2}\exp\left(j\frac{\pi}{3}\right) \\ \beta_0 &= \tfrac{1}{2}\exp\left(-j\frac{\pi}{3}\right) \end{aligned}\right\} \tag{3}$$

We now assume that α and β depart slightly from the values given by eqn. 3 and write

$$\left.\begin{aligned} \alpha &= \alpha_0 + \delta\alpha \\ \beta &= \beta_0 + \delta\beta \end{aligned}\right\} \tag{4}$$

and treat $\delta\alpha$, $\delta\beta$ and $\gamma\ \{= |\gamma|\exp(j\phi)\}$ as small quantities.

With suitably redefined reference planes, and neglecting

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Circuits and Systems Letters

Improved z Plane Polynomial Interpolative Analysis of Switched-Capacitor Networks

D. G. JOHNSON AND J. I. SEWELL

Abstract—**The accuracy of interpolated polynomials in z is considerably improved using a transformed sampling plane and the FFT. This is further enhanced when the transformation is coupled with partitioned polynomial interpolation. One solution to the problem of over-interpolation also follows.**

Polynomial interpolation schemes have been employed successfully in the past to the analysis of continuous networks, active and passive. A number of current computer programs for analysising switched capacitor networks [1], [2] have adopted similar routines in the z plane.

If a typical transfer function is $H(z)=N(z)/D(z)$ the individual polynomials of type

$$F(z)=\sum_{i=0}^{n} a_i z^i$$

can be determined by interpolating with $n+1$ samples $\{z_i\}$ and $n+1$ correspondingly sampled responses $F(z_i)$. The process corresponds to solving $A=\sigma^{-1}F$ where σ is the Vandermonde matrix of samples $\{z_i\}$. Now σ^{-1} can be formed using a Traub technique [3]. Alternatively any standard interpolation method (Langrange, etc.) could be used for the process. The samples $\{z_i\}$ can be chosen anywhere in the complex plane, with some preference for a circular array, which generally gives best accuracy. It transpires [4] that if a circle of unity radius and centre $\{0,0\}$ is used, then $\sigma^{-1}F$ is exactly equivalent to performing an FFT. This has many computational attractions, as much effort has been invested in providing extremely fast and accurate FFT routines.

However, two problems arise with the application of the FFT to the analysis of SC networks. The first is due to the very compact pole–zero locations associated with standard filter functions when displayed in the z plane. These tend to congregate in a small segment within the unit circle, a process which is exaggerated with increase in function order and complexity. Bandpass functions generally present the most severe case. A useful test network for evaluation purposes is a sixth-order bandpass filter, whose pole–zero locations are shown in Fig. 1. For maximum accuracy of the z polynomial coefficients, the system should be sampled in the region close to the poles and zeros, where the function is most sensitive to small changes in pole–zero position. Clearly, for a set of sample points uniformly distributed around the unit circle there will be some points distant to the left of the singularities and hence the response vectors associated with these will be almost coincident and certainly form a mechanism for numerical inaccuracies. The error function shown in Fig. 2 is the difference between the response of the filter computed by a standard frequency analysis program SCNAP 2 and that from the polynomials produced by basic FFT interpolation. This displays

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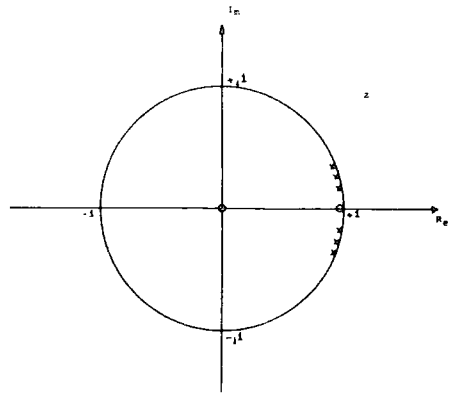

Fig. 1. Pole–zero plot for 6th order SC bandpass filter.

the result of the error mechanism and is really not acceptable. Table 1 shows the peak magnitude error for a number of filters, from which an ominous trend is clearly visible.

Consider the two planes w and z, Fig. 3. These are related by $z-1=w\cdot r$ where r is the radius of a new sampling circle centered on $\{1,0\}$. Performing an FFT with a normal set of samples from the unit circle in w and a corresponding set of sampled responses derived from the circle in z will yield

$$F(w)=\sum_{i=0}^{n} a_i' w^i.$$

Replacing w by $(z-1)/r$ gives

$$F(z)=\sum_{i=0}^{n} a_i'(z-1)i_r - i.$$

Equating coefficients with

$$F(z)=\sum_{i=0}^{n} a_i z^i$$

gives

$$a_i=\sum_{k=i}^{n} a_k' r^{-k} C\binom{k}{i}(-1)^{(k+i)}$$

with

$$C\binom{k}{i}=k!/i!(k-i)!,$$

the set of pseudo coefficients $\{a_i'\}$ is, therefore, easily convertible into the actual set of coefficients $\{a_i\}$. Of course the frequency response can always be evaluated from $F(w)$ anyway. The results of applying this technique to the same filter are given in columns 1–3 of Table II and show the routine to be very effective.

Whilst the reduction in error is significant, it is possible to improved the performance even further. High order systems are likely to feature several compact groups of poles–zeros, particularly bandpass structures. To really enhance accuracy, consider the possibility of employing a number of sample circles of

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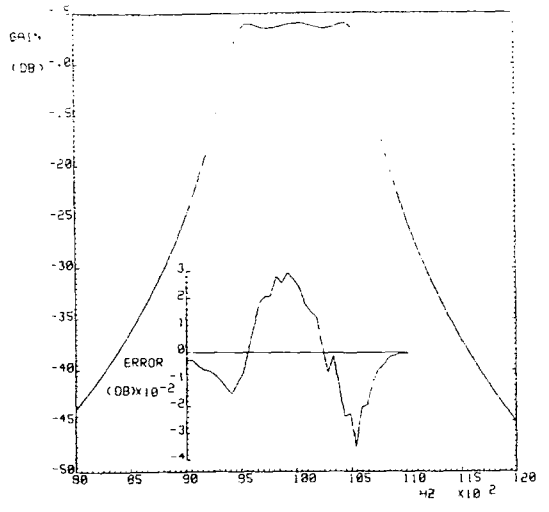

Fig. 2. Frequency response and magnitude error function from interpolative analysis.

TABLE I
PEAK MAGNITUDE ERROR FOR VARIOUS FILTERS WITH BASIC FFT

Type of Circuit	No. of Nodes	No. of Phases	Peak Magnitude Error dB
1st Order Butterworth L.P.	8	1	1.4×10^{-10}
3rd Order Elliptic L.P.	17	2	2.5×10^{-7}
4th Order Elliptic L.P. (MOSSER)	20	4	7.2×10^{-3}
4th Order Elliptic L.P.	22	4	1.3×10^{-4}
6th Order B.P.	29	3	1×10^{-2}

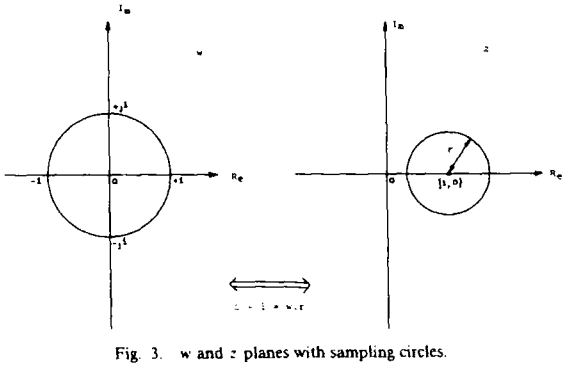

Fig. 3. w and z planes with sampling circles.

TABLE II
ERRORS FOR BANDPASS FILTER WITH VARIOUS FFT INTERPOLATION SCHEMES

	FFT sample circle Radius=1 Centre= 0.0	FFT sample circle Radius=1 Centre= 1.0	FFT sample circle, Radius=0.4 Centre= 1.0	Partitioned FFT Numerator Radii=0.1,0.6 Denominator Radii=0.15,0.3 Centre=1.0	Partitioned FFT Numerator=0.1,0.6 Denominator=0.1,0.2, 0.25,0.3 Centre=1.0
Peak Magnitude Error dB	1.5143×10^{-2}	4.6951×10^{-3}	5.1607×10^{-5}	2.8251×10^{-5}	2.1496×10^{-5}
Peak Phase Error Deg.	2.1464×10^{-1}	3.0757×10^{-2}	1.4133×10^{-4}	1.9708×10^{-4}	1.1751×10^{-4}

different radii selected to describe the sensitive regions. This can be achieved most effectively by partitioned polynomial interpolation [5].

Take a sample circle centered on $z=1$ with radius r_0 and consider a set of l samples around that circle say Z_0, these yield a set of sampled responses F_0. A new set of l samples, simply related by $Z_i = b_i Z_0$ $(i \neq 0)$ with b_i as a complex constant, will yield a new set of samples responses F_i. In general for p partitions, there will be p sets of sample points and p sets of sampled responses giving:

$$\begin{bmatrix} F_0 \\ F_i \\ \vdots \\ F_{p-1} \end{bmatrix} = \begin{bmatrix} \sigma_0 & D_0\sigma_0 & D_0^2\sigma_0 & \cdots & D_0^{p-1}\sigma_0 \\ \sigma_1 & D_1\sigma_1 & D_1^2\sigma_1 & \cdots & D_1^{p-1}\sigma_1 \\ \vdots & \vdots & \vdots & & \vdots \\ \sigma_{p-1} & D_{p-1}\sigma_{p-1} & D_{p-1}^2\sigma_{p-1} & & D_{p-1}^{p-1}\sigma_{p-1} \end{bmatrix} \begin{bmatrix} A_0 \\ A_1 \\ \vdots \\ A_{p-1} \end{bmatrix}$$

where A is the vector of required coefficients, $A_0 = \{a_0, a_1, \cdots, a_{l-1}\}$, $A_1 = \{a_l, a_{l+1}, \cdots, a_{2l-1}\}, \cdots$, $D_i = \text{diag}\{z_{il}, z_{il+1}, \cdots, z_{(i+1)l-1}\}$ and σ_i is a Vandermonde matrix of the ith set of samples Z_i. Let $D_i = C_i I_l$, hence $z_i = C_i^{-l} e^{j2\pi k/l} = r_i e^{j2\pi k/l}$ where $k = 0, 1, 2, \cdots, l-1$. So $C_i = r_i^l$. Also $b_i = r_i / r_0$ then $\sigma_i = \sigma_0 B_i$, where $B_i = \text{diag}\{1, b_i, b_i^2, \cdots, b_i^{l-1}\}$. Hence:

$$\begin{bmatrix} A_0 \\ A_1 \\ \vdots \\ A_{p-1} \end{bmatrix} = \begin{bmatrix} 1 & C_0 & C_0^2 & \cdots & C_0^{p-1} \\ 1 & C_1 & C_1^2 & \cdots & C_1^{p-1} \\ \vdots & \vdots & \vdots & & \vdots \\ 1 & C_{p-1} & C_{p-1}^2 & \cdots & C_{p-1}^{p-1} \end{bmatrix}^{-1} \cdot \begin{bmatrix} B_0^{-1} & \times & \sigma_0^{-1} & F_0 \\ B_1^{-1} & \times & \sigma_0^{-1} & F_1 \\ \vdots & & \vdots & \\ B_{p-1}^{-1} & \times & \sigma_0^{-1} & F_{p-1} \end{bmatrix}$$

each $\sigma_0^{-1} F_i$ involves the transformed FFT as outlined. The inversion of the $[C]$ matrix presents few problems since its order is equal to the number of partitions which is usually quite small, and as it is a Vandermonde matrix a Traub technique can be used. The calculation of B_i^{-1} is trivial.

The two final columns of Table II show the further improvements in accuracy with partitioned polynomial interpolation, a scheme with 2 partitions in the numerator and 4 in the denominator providing the best results.

The partitioned polynomial approach also provides a solution to a second problem with the FFT, that is overinterpolation. As the number of samples presented to an FFT routine must satisfy 2^n, it will generally be necessary to round up to the nearest integer satisfying this condition. This means having to evaluate the system response more times than necessary. Worst cases occur for orders of 2^n (requiring 2^n+1 sample points) which must be rounded up to 2^{n+1}, giving 2^n-1 over evaluations and almost doubling the computer time for system evaluations. By using a partitioned polynomial approach considerable savings can be made, particularly with higher order functions and when the order lies in the lower part of some FFT band order. In general if the order n satisfies $2^i < n+1 < (2^{i+1}-2^{i-1})$ for some integer i, then partitioning the system requires fewer function evaluations than the basic FFT. In some instances quite considerable savings can be made.

The application of a transformed sample plane and polynomial partitioning to interpolative analysis of SC filters demonstrates improvements in accuracy and the number of function evaluations on even moderate order networks. It is expected that in analysis of high-order SC networks these routines should produce significant improvements in accuracy and computer time. This is a subject of further work.

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Harmonic Retrieval by FIR Digital Filters

G. ORLANDI AND G. MARTINELLI

***Abstract*—A new algorithm is proposed for determining the FIR filter for estimating the frequencies of a process consisting of sinusoids in white noise. The algorithm is based on an extensive use of the constrained predictor and is characterized by a very fast convergence.**

The use of finite impulse response (FIR) filters for the spectral analysis of a process is well known. When the process to be analyzed consists of M sinusoids in white noise, the frequencies f_i of the sinusoids are estimated by the roots of the polynomial transfer function of the filter. On the basis of the theory developed by Pisarenko [1], Thompson proposed an iterative method for determining the taps of the filter. The method [2] consists of minimizing the output power of the filter under the constraint that the length of its tap vector D_p be equal to 1. The minimization is carried out by an iterative gradient procedure, which suffers by a very serious problem of slow convergence [3]. The problem is overcome by the algorithm proposed in [4], which determines D_p by an extensive use of the adaptive predictor. Further improvements are, however, possible by using the constrained version of the predictor [5], as will be shown in the present letter. The resulting algorithm is faster than that proposed in [4] and allows a reduced computational cost.

In the following we will use the notations:

1) D_N is the tap vector of the predictor filter of order N, i.e.,

$$D_N^t = [d_0 \quad d_1 \quad \cdots \quad d_N] \tag{1}$$

where $d_0 = 1$ and t denotes transposition. The value of D_N will be adaptively computed by the method proposed in [6].

2) $P(z)$ is the polynomial transfer function of the filter, i.e.,

$$P(z) = \sum_{k=0}^{N} d_k z^{-k}. \tag{2}$$

The roots of $P(z)$ give an estimate of the frequencies of the sinusoids of the process. These roots take on the form $e^{-j2\pi f_i}$, $i = 1,2,\cdots,M$, since we will use $N = 2M$ and $P(z)$ is constrained to have its roots on the unit circle.

3) $D_{B,H}(z)$ is the tap vector of the constrained predictor of order $2H$ [5]. It results

$$D_{B,H} = \begin{bmatrix} D_{2H-1} \\ 0 \end{bmatrix} + \begin{bmatrix} 0 \\ D'_{2H-1} \end{bmatrix} \tag{3}$$

where the prime denotes the reversion of the components of D_{2H-1};

4) $D_p(z)$ is the tap vector which satisfies the constraint required by Thompson's method [2], i.e.,

$$\sum_{k=0}^{N} d_k^2 = 1. \tag{4}$$

The new algorithm we propose is based on the following expression for the tap vector D_p (not normalized):

$$\begin{aligned} D_p &= D_{B,M} + \sum_{i=1}^{M} a_i V_i \\ V_i^t &= \Big[\underbrace{0\cdots0}_{M-i}\ D_{B,i}^t\ \underbrace{0\cdots0}_{M-i}\Big], \qquad i = 1,2,\cdots,M-1 \\ V_M^t &= \Big[\underbrace{0\cdots0}_{M}\ 1\ \underbrace{0\cdots0}_{M}\Big] \end{aligned} \tag{5}$$

where $D_{B,i}$, $i = 1,2,\cdots,M$ is obtained by (3) with $H = i$. Such a formulation results in a very simple expression for the output power W of the filter in the ideal case of an infinite number of samples, i.e.,

$$W = 2\left[E_{2M-1}(1-K_{2M}) + \sum_{i=1}^{M-1} a_i^2 E_{2i-1}(1-K_{2i})\right] + a_M^2 E_0 \tag{6}$$

where E_{2i-1} is the output power of the predictor of order $2i-1$; K_{2i} is the $(2i)$th reflection coefficient of the predictor of order $2M$; E_0 is the input power. As a consequence of (6), the value of

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SYMBOLIC ANALYSIS OF IDEAL AND NON-IDEAL SWITCHED CAPACITOR NETWORKS

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ABSTRACT

Techniques for the analysis of switched-capacitor (SC) networks by computer means are well developed, particularly in the time and frequency domains. Symbolic methc is have been derived for ideal SC networks (no resistances or finite amplifier bandwidths). For networks of practical size symbolic analysis to produce totally literal coefficients is out of the question, but polynomials with numerical coefficiants and semi-literal coefficients are feasible results. These have considerable attraction in optimisation and fine graphical work. In the ideal case the inverse of a rational matrix H(z) is required; whereas the more general case, which includes all resistive effects, will involve the inverse of a rational matrices in both continuous and discrete variables H (s,z). A general scheme has been developed for the symbolic analysis of both ideal and non-ideal SC networks.

SYMBOLIC ANALYSIS OF IDEAL SC NETWORKS

One method for effecting the symbolic analysis of SC networks (ideal and non-ideal) employs a topological formulation [1]. Here a compact MNA formulation has been utilised, with switching introduced via contraction and a compaction scheme [2] for multiphase networks. Totally arbitrary multiphase switching arrangements can be accommodated. In standard MNA form [3]:

$$\begin{bmatrix} \underline{F}_1 & 0 & & 0 & -z^{-1}\underline{G}_1 \\ -\underline{G}_2 & \underline{F}_2 & & 0 & 0 \\ & \ddots & \ddots & & \\ & & \ddots & \ddots & \\ & & & -\underline{G}_p & \underline{F}_p \end{bmatrix} \begin{bmatrix} \underline{X}_1 \\ \underline{X}_2 \\ \vdots \\ \underline{X}_p \end{bmatrix} = \begin{bmatrix} \underline{U}_1 \\ \underline{U}_2 \\ \vdots \\ \underline{U}_p \end{bmatrix} \qquad \ldots.(1)$$

where $\underline{F}_i$ is the present state matrix, $\underline{G}_i$ the previous state matrix, $\underline{U}_i$ the present state excitation vector and $\underline{X}_i$ present state response vector.

Rewrite as

$$\left[\underline{A} + z^{-1}\underline{B}\right]\underline{X} = \underline{U}$$

where

$$\underline{A} = \begin{bmatrix} \underline{F}_1 & 0 & & \\ -\underline{G}_2 & \underline{F}_2 & & \\ & \ddots & \ddots & \\ & & -\underline{G}_p & \underline{F}_p \end{bmatrix} \quad \text{and} \quad \underline{B} = \begin{bmatrix} & & -z^{-1}\underline{G}_1 \\ & \bigcirc & \\ & & \end{bmatrix} \qquad \ldots.(2)$$

If $|A| \neq 0$ then a sequence for the inverse of the system matrix can be determined by a Kader method [4]

$$\begin{aligned} &\text{let } d_o = |A|, \quad \underline{N}_o = \text{adj } \underline{A}_o \quad (\text{adj } \underline{A}_o = d_o \underline{A}^{-1}) \\ &d_1 = \text{tr}\left[\underline{B}\,\underline{N}_o\right] \qquad \underline{N}_1 = \underline{A}^{-1}\left[d_1 \underline{I} - \underline{B}\underline{N}_o\right] \\ &\vdots \qquad\qquad \vdots \qquad\qquad \vdots \qquad\qquad \vdots \\ &d_k = \frac{1}{k}\,\text{tr}\left[\underline{B}\,\underline{N}_{k-1}\right], \quad \underline{N}_k = \underline{A}^{-1}\left[d_k \underline{I} - \underline{B}\underline{N}_{k-1}\right] \qquad \ldots.(3) \\ &\vdots \qquad\qquad \vdots \qquad\qquad \vdots \qquad\qquad \vdots \\ &d_n = |B| \qquad\qquad \underline{N}_n = \text{adj } \underline{B} \end{aligned}$$

where n is determined by rank $\underline{B}$. This gives a maximum value for n, in practice the degree is usually less and zero coefficients may be suppressed.

Then

$$H(z) = \left[\underline{A} + z^{-1}\underline{B}\right]^{-1} = \frac{\sum_{i=0}^{m} \underline{N}_1 z^{-i}}{\sum_{i=0}^{n} d_i z^{-1}} = \frac{\sum_{i=0}^{m} \underline{N}_i z^{-i}}{D(z)} \qquad \ldots.(4)$$

where D(z) is the denominator common to all terms and $m \leq n$.

If $|A| = 0$ and $|B| = 0$ then define a new variable $z = \hat{z} + e$ where e = constant, of such a value to ensure that the matrix pencil $[eB+A]$ is regular. A Kader sequence will then produce $\underline{N}(z)$ and $D(\hat{z})$. Application of Pascal's triangle will effect $\hat{z} \to z$ and return the coefficients of $\underline{N}(z)$ and D (z).

SYMBOLIC ANALYSIS OF NON-IDEAL SC NETWORKS

The more general case of symbolic analysis, when switch resistance (on and off) and finite amplifier bandwidth are taken into account, is slightly more involved but utilises the above algorithm to great affect. The MNA differential equations in generalised state space form for node voltages v(t) and branch currents i(t) in time slot Δ_k are:

$$\begin{bmatrix} G_k & A_k \\ B_k & D_k \end{bmatrix} \begin{bmatrix} v(t) \\ i(t) \end{bmatrix} + \begin{bmatrix} C & O \\ O & O \end{bmatrix} \begin{bmatrix} \dot{v}(t) \\ O \end{bmatrix} = \begin{bmatrix} j(t) \\ e(t) \end{bmatrix} \qquad \ldots.(5)$$

where $\underline{G}_k$ - conductance matrix, $\underline{C}$ - capacitance matrix, the other matrices provide loop and node links. In compact form

$$\underline{G}_{ke}\,\underline{x}(t) + \underline{C}_e\dot{\underline{x}}(t) = \underline{U}(t) \qquad \ldots.(6)$$

The singular nature of $\underline{C}_e$ needs to be recognised in the extended state transition matrix. An alternative approach is to use the standard singular perturbation rule.

$$\begin{aligned} \underline{C}\,\dot{\underline{v}}(t) &= -\underline{G}_k\underline{v}(t) - \underline{A}\,\underline{i}(t) + \underline{j}(t) \\ \varepsilon\,\underline{I}\,\dot{\underline{i}}(t) &= -\underline{B}_k\underline{v}(t) - \underline{D}\,\underline{i}(t) + \underline{e}(t) \end{aligned} \qquad \ldots.(7)$$

with $0 < \varepsilon << 1$ a regular state space formulation results [6,7,8].

$$\underline{G}_{ke}\underline{x}(t) + \underline{C}_e(\varepsilon)\,\dot{\underline{x}}(t) = \underline{U}(t) \qquad \ldots.(8)$$

Both formulations have been examined and conclusions regarding the accuracy of the state transition matrix determined.

The final nodal voltages and branch currents at the end of timeslot $\Delta_k + \ell T$ with sinusoidal excitations are given by [5]:

$$\underline{x}(t_{k+1}+\ell T) = \underline{P}_k\underline{x}(t_k+\ell T) + \left[\underline{I}e^{j\Omega t_{k+1}} - \underline{P}_k e^{j\Omega t_k}\right]\underline{M}_k(j\Omega)\begin{bmatrix}\hat{J}\\ \hat{E}\end{bmatrix}e^{j\Omega\ell T} \qquad \ldots.(9)$$

where $\underline{M}_k(j\Omega) = \left[G_{ke} + j\Omega C_e\right]^{-1}$ and $\underline{P}_k$ is the state transition matrix appropriate to either formulation above. Using the s transformation and substituting $s = j\Omega$, $W_k = e^{j\Omega t_k}$ gives

$$\begin{bmatrix} \underline{I} & & & -z^{-1}\underline{P}_1 \\ -\underline{P}_2 & \underline{I} & & \\ & \ddots & \ddots & \\ & & -\underline{P}_{\rho-1} & \underline{I} \\ & & & -\underline{P}_\rho \quad \underline{I} \end{bmatrix} \begin{bmatrix} \underline{X}_1 \\ \underline{X}_2 \\ \vdots \\ \underline{X}_{\rho-1} \\ \underline{X}_\rho \end{bmatrix} = \begin{bmatrix} \underline{M}_1(s) & & & -z^{-1}\underline{P}_1\underline{M}_1(s) \\ -\underline{P}_2\underline{M}_2(s) & \underline{M}_2(s) & & \\ & \ddots & \ddots & \\ & & -\underline{P}_{\rho-1}\underline{M}_{\rho-1}(s) & \underline{M}_{\rho-1}(s) \\ & & -\underline{P}_\rho\underline{M}_\rho(s) & \underline{M}_\rho(s) \end{bmatrix} \begin{bmatrix} \underline{U}_1W_1 \\ \underline{U}_2W_2 \\ \vdots \\ \underline{U}_{\rho-1}W_{\rho-1} \\ \underline{U}_\rho W_\rho \end{bmatrix}$$

with $S(z) = \sum_{i=-\infty}^{\infty} e^{j\Omega\ell T} z^{-i}$ .... (10)

In compact form equation (10) becomes

$$\left[PI(z)\right]\underline{X}(z) = \left[PM(s,z)\right]\underline{U}\,S(z)$$

and $$\underline{X}(z) = \left[PI(z)\right]^{-1}\left[PM(s,z)\right]\underline{U}\,S(z) \qquad \ldots.(11)$$

The frequency domain response follows immediately from substitution in equation (11).

$$\begin{bmatrix} \underline{V}(\omega) \\ \underline{I}(\omega) \end{bmatrix} = \sum_{k=1}^{\rho} a_k(\omega) \begin{bmatrix} \underline{V}_k(e^{j\omega T}) \\ \underline{I}_k(e^{j\omega T}) \end{bmatrix} \bar{W}_{k+1} \qquad \ldots.(12)$$

where $\bar{W}_{k+1} = e^{-j\omega t_{k+1}}$

and $a_k(\omega) = \{\, 2 \sin\left[\omega\,(t_{k+1} - t_k)/2\right] e^{j\omega(t_{k+1}-t_k)/2}\, e^{j\omega t_{k+1}}\} / T\omega$

It will be noted that the form of the matrix $\left[PI(z)\right]$ is very similar to that of the original ideal SC system matrix in equation (1), so the Kader sequence of equations (3) applies directly in finding

$$\left[PI(z)\right]^{-1} = \frac{\sum_{i=o}^{m} \underline{NP}_i z^{-i}}{\sum_{i=o}^{n} dp_i z^{-i}} = \frac{\underline{NP}(z)}{DP(z)}$$

$m \leq n$

The inverse $\underline{M}_k(s) = \left[G_{ke} + sC_e\right]^{-1}$ is also obtainable from a Kader sequence. In this instance $\underline{C}_e$ is generally singular and $\underline{G}_{ke}$ may well be singular also. However a shift of variable to ensure a regular matrix pencil is used to overcome any singularity problems. The resultant form will be

$$\underline{M}_k(s) = \frac{\sum_{i=1}^{m} (\underline{NM}_i)_k s^i}{\sum_{i=1}^{n} (dm_i)_k s^i} = \frac{\underline{NM}_k(s)}{DM_k(s)}$$

$m \leq n$

substitution in equation (11) gives equation (13). Computation of frequency response follows in a straightforward manner.

STATE TRANSITION MATRIX APPROXIMANT

In order to compute the true dynamic behaviour of the SC network it is essential to have a good approximation for $\underline{P}_k$. This can be a time consuming process and if care is not taken, considerable concern can arise as to the validity of the $\underline{P}_k$ computed.

In general, it has been found that an application of the I_{MN} approximant [9] gives stable and accurate results in an economic time.

$$\begin{bmatrix} \underline{X}_1 \\ \underline{X}_2 \\ \cdot \\ \cdot \\ \cdot \\ \underline{X}_p \end{bmatrix} = \frac{1}{DP(z)} \begin{bmatrix} \underline{NP}_{11}(z) & \underline{NP}_{12}(z) & \cdots & \underline{NP}_{1p}(z) \\ \underline{NP}_{21}(z) & \underline{NP}_{22}(z) & \cdots & \underline{NP}_{2p}(z) \\ \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot \\ \underline{NP}_{p1}(z) & \underline{NP}_{p2}(z) & \cdots & \underline{NP}_{pp}(z) \end{bmatrix} \begin{bmatrix} DM_1(s) & & & \\ & DM_2(s) & & \\ & & \cdot & \\ & & & DM_p(s) \end{bmatrix}^{-1} \begin{bmatrix} \underline{NM}_1(s) & & & -z^{-1}\underline{P}_1\underline{NM}_1(s) \\ -\underline{P}_2\underline{NM}_2(s) & \underline{NM}_2(s) & & \\ & \cdot & \cdot & \\ & & \cdot & \\ & & -\underline{P}_p\underline{NM}_p(s) & \underline{NM}_p(s) \end{bmatrix} \begin{bmatrix} U_1 W_1 \\ U_2 W_2 \\ \cdot \\ \cdot \\ U_p W_p \end{bmatrix} S(s) \quad \ldots.(13)$$

For the regular state space form

$$\underline{P}_k = \frac{1}{\Delta t} \sum_{i=1}^{N} K_i \left[\alpha_i / \Delta t \, \underline{I} + \underline{C}_e^{-1}(\varepsilon) \underline{G}_{ke} \right]^{-1} \quad \ldots.(14)$$

where Δt is the time step and α_i, K_i are easily predetermined [10]. The order of approximation N is also determined as in [9], and may require $N=10$. For the generalised state space description it can be shown that

$$\underline{P}_k = \frac{1}{\Delta t} \sum_{i=1}^{N} K_i \left[\alpha_i / \Delta t \, \underline{C}_e + \underline{G}_{ke} \right]^{-1} \underline{C}_e \quad \ldots.(15)$$

The MNA equations for the non-ideal SC network produce a stiff system, largely due to the values of switch G_{on} and G_{off}. It has been found that equation (15) normally gives the best answers and therefore the generalised state space MNA formulation has been adopted. Incidentally if a NAM description is used the size of the matrix is smaller and slightly better conditioned, this may have relevance in the analysis of large SC networks.

RESULTS AND CONCLUSIONS

A program SCNAP 3 written in Fortran 77 has been used to analyse a variety of SC filter networks both for the ideal and non-ideal situations. The results compare very favourably with those produced by frequency domain programs. Fig 1 shows typical results for a 5th order SC elliptic lowpass filter with both ideal and non-ideal switches.

The initial step to produce the various polynomials is obviously the most time consuming part of the analysis. The advantages follow after this, since many points of frequency analysis can be computed by simple polynomial evaluation. This has significant implications in noise analysis. Other direct applications are in optimisation and partitioned analysis of large SC filter networks.

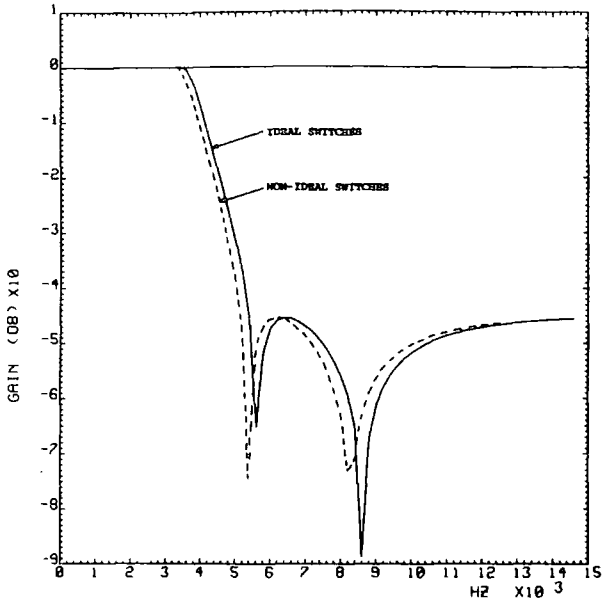

Fig. 1. Fifth Order Elliptic Lowpass SC Filter

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PAPER 33

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EFFICIENT COMPUTER TECHNIQUES FOR THE EXACT ANALYSIS OF ALL NON-IDEAL EFFECTS OF SWITCHED-CAPACITOR NETWORKS IN THE TIME DOMAIN

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ABSTRACT

The paper addresses the problem of designing software to compute the detailed time domain analysis of potentially large switched-capacitor (SC) networks. Instead of simulating side effects such as clock-feedthrough and offsets, charge based models of the devices are incorporated and charge conservation is ensured throughout by using these models, charge state variables and tight tolerances. To compute the fine detail required, the analysis times are likely to be substantial. Hence every attempt is made to speed up the routines using interpretive code generation and sparse matrix techniques. The accuracy of solution is also important and various accuracy control routines are considered. Optimal pivoting techniques and dynamic store management are utilised. The SCNAPNIT program can be applied to SC networks of a wide variety, with filtering and non-filtering applications. Continuous-time networks can also be analysed in an efficient manner.

INTRODUCTION

With the continuing interest in switched-capacitor (SC) networks and their wider application to non-filtering applications, the need for CAD tools is of prime importance. In response to this demand many different analysis techniques and programs emerged [1]. The initial time-domain approaches were soon followed by frequency domain methods. These programs perform the analyses assuming all circuit elements are ideal and are therefore primarily of use as tools for verification of theoretical designs and exploring various design alternatives. Unfortunately due to practical device non-idealities (e.g. finite amplifier GB, finite switch conductance), fabricated devices deviate from their theoretically predicted performances. These effects have been crudely modelled by replacing resistors in macromodels by switched-capacitor equivalents [2], introducing fixed DC sources for amplifier offsets, or in the case of clock feedthrough by simple capacitive coupling subnetworks [3]. The major advantage of these ideal analyses is that they are very efficient, both in computational speed and memory requirements, and can therefore easily and accurately cope with large networks [4]. The disadvantage is that they lack the ability to model actual non-ideal circuit behaviour.

More sophisticated mathematical approaches employing state space formulations have incorporated accurate analysis of linear resistive effects. These techniques have demanded large computing times and still only provide a limited linear analysis of the SC networks.

To accurately model the effects of clock-feedthrough, clock wave-form variation distortion, power supply variations, resistive parameters, finite amplifier GB and switch and amplifier offsets, full non-linear switch and amplifier models are required. Currently the most reliable and accurate numerical techniques for solving these nonlinear networks are time-domain simulation programs employing sophisticated numerical integration methods. The major drawback of this approach is that it is computationally intensive and therefore the characteristics of the equations to be solved should be taken into account in an attempt to reduce or streamline the computations.

The second important aspect of accurate circuit simulation is device modelling, specifically MOSFET switches. Accurate models have been developed [5], [6] for the DC and dynamic intrinsic and extrinsic devices. It is essential that device models and their implementation conserve charge to ensure accurate and correct simulation.

Although a number of efficient schemes already exist for the time-domain analysis of SC networks, a new implementation is developed here, initially as a test vehicle for some of the computational techniques and secondly as part of an overall suite of second generation SC design and analysis programs. The equation formulation philosophy, interpretive code generation, optimal pivoting techniques and dynamic store management are then ultilised in the development of the complete non-ideal time-domain analysis program.

IDEAL TIME-DOMAIN ANALYSIS

The efficient time-domain analysis of ideal SC networks [4], is based on techniques for efficiently assembling and solving the system of equations

$$\begin{bmatrix} \underline{A}_1 & & & \\ -\underline{B}_2 & \underline{A}_2 & & \\ & \ddots & \ddots & \\ & & -\underline{B}_0 & \underline{A}_0 \end{bmatrix} \begin{bmatrix} \underline{x}_{1+k_0} \\ \underline{x}_{2+k_0} \\ \vdots \\ \underline{x}_{0+k_0} \end{bmatrix} = \begin{bmatrix} \underline{w}_{1+k_0} + \underline{B}_1 \underline{x}_{k_0} \\ \underline{w}_{2+k_0} \\ \vdots \\ \underline{w}_{0+k_0} \end{bmatrix} \quad k=0,1,\ldots \qquad (1)$$

The method of equation formulation has a dramatic effect on the size and sparsity of the resulting matrices. To allow the inclusion of voltage sources (dependent and independent), tableau type formulation methods are desirable for their generality and sparsity properties. A feature of these methods is the need for a pivoting algorithm to ensure that a non-zero diagonal is obtained, which then alters the structure of the matrices [4]. A comparison between the formulation methods discussed in [1] as well as the mixed nodal tableau (MNT) [7] on the basis of operation counts for the LU decomposition of the resulting matrices, found the MNA formulation [8] to be the best approach. By transferring as much of the matrix processing to a pre-processing stage, the time-domain response is obtained very efficiently. Taking into account the block-matrix structure of equation (1), the sparsity of blocks $\underline{A}_i$ and $\underline{B}_i$, and the form of the MNA equations used to assemble equation (1), a highly efficient block compaction algorithm typically reduces the system of equations by 50-90%. This reduced matrix is then re-ordered to achieve a minimal operation count and LU decomposed using a sparse variant of Gaussian elimination. To obtain the time-domain response these LU factors are used repeatedly in a forward elimination and back substitution, therefore to obtain maximum efficiency a code generation scheme [9] is used to generate code for the solution process.

NONIDEAL TIME-DOMAIN ANALYSIS

To ensure charge conservation, it is necessary to select charges as the state variables for the MOSFET capacitances [10], leading to the set of first order nonlinear algebraic differential equations

$$\frac{d}{dt}\underline{q}(\underline{x}) + \underline{G}\underline{x} + \underline{f}_2(\underline{x}) = \underline{w}(t) \quad t \in [0,T] \qquad (2)$$

where $\underline{q}(\underline{x})$ is the charge function, $\underline{q}(\underline{x}) = \underline{C}\underline{x} + \underline{f}_1(\underline{x})$

$\underline{f}_1$ is the nonlinear charge function

$\underline{f}_2$ is the nonlinear current function

$\underline{x}$ contains the unknown node voltages and branch currents

$\underline{w}(t)$ contains the time-dependent excitations

These networks typically consist of tightly coupled circuit blocks having a large number of feedback loops with widely differing circuit time-constants. Due to these characteristics, the third generation simulation techniques [11] are not suited to solving these networks. To overcome the problem of the 'stiffness' of the equations, an implicit numerical integration technique [12] is used to discretize equation (2). This technique has the added benefits that it directly handles equation (2) in its implicit form, together with any algebraic equations. By accumulating charges in the vector $\underline{q}(\underline{x})$ and then applying the numerical integration to this vector, the resulting method is more accurate and efficient than individually integrating the MOSFET terminal charges.

The numerical integration technique used is a backward difference approximation to the derivative (predictor), followed by a corrector based on Gear's approach [12]. The order 1 method is used as a starter and thereafter the order 1 and order 2 formulas are used in a variable-order, variable time-step manner. The order is limited to 2 to allow the inclusion of PWL nonlinearities [13]. Because of the large number of breakpoints in the clock signal excitation common to SC networks and the consequent requirements for resetting to low order, the higher order methods are not involved. The discretization of equation (2) leads to a set of nonlinear equations

$$\underline{f}(\underline{x}_n, t_n) = 0 \qquad (3)$$

which must be solved at each time-point t_n. A modified Newton-Raphson algorithm is used to solve equation (3), which leads to the iteration

$$\underline{J}(\underline{x}_n^k)\Delta\underline{x}^{k+1} = -\underline{f}(\underline{x}_n^k)$$

$$\underline{x}_n^{k+1} = \underline{x}_n^k + \Delta\underline{x}^{k+1} \qquad (4)$$

where $\underline{J}(\underline{x}_n^k)$ is the Jacobian evaluated at $\underline{x}_n^k$. Each iteration requires the solution of a set of linear equations. Fortunately the nonzero structure of the Jacobian does not change from iteration to iteration. It is sparse and normally diagonally dominant. Therefore sparse matrix techniques [14] can be used to great effect. The iteration (4) is terminated when the iterations satisfy the convergence criteria. The usual criteria is based on the node voltages and nonlinear currents meeting specified error tolerances. These checks are not sufficient to ensure convergence and may lead to charge nonconservation [10]. Therefore the terminal nodes of dynamic and nonlinear devices are checked to satisfy the convergence criteria

$$|V^{k+1} - V^k| \leq \varepsilon_v + \varepsilon_r \max\left\{|V^{k+1}|, |V^k|\right\}$$

The terminal charges of capacitors and MOSFETS are checked to satisfy

$$|Q^{k+1} - Q^k| \leq \varepsilon_q + \varepsilon_r \max\left\{|Q^{k+1}|, |Q^k|\right\}$$

and the currents of nonlinear devices are checked to satisfy

$$|I^{k+1} - I^k| \leq \varepsilon_i + \varepsilon_r \max\left\{|I^{k+1}|, |I^k|\right\}$$

where ε_v, ε_q and ε_i are the absolute voltage, charge and current tolerances respectively and ε_r is the relative tolerance.

The overall algorithm for solving equation (2) is given below.

```
REPEAT
  evaluate the time-dependent excitations
  predict the unknown vector x^(n+1)
  REPEAT
     evaluate the linear and nonlinear current
                                        equations
     evaluate the linear and nonlinear charge
                                        equations
     integrate the charge vector and add to the
                                   current vector
     evaluate the partial derivatives and form
                                  the Jacobian
     LU decompose the Jacobian
     solve the linearised system for x^(n+1)
  UNTIL converged or exceeded maximum number of
                                        iterations
  IF iteration limit exceeded THEN
     reduce time-step
  ELSE
     check LTE and select new time-step
     IF LTE does not exceed limit THEN
        save the time-point
        update backward information
     END IF
  END IF
UNTIL time > T
```

A major feature of SC networks is the switch clocking waveforms. These waveforms are usually specified as piecewise linear (PWL) excitations. Due to the discontinuities in the first derivative of these excitations, convergence problems are encountered during transient analysis, possibly even time-point lockup [15]. To overcome this, source breakpoint detection [15] can be used, whereby a time-step is selected so that the breakpoint coincides with the mesh point and the integration method can then be restarted from order 1. Although this technique is reliable, it is wasteful as a small timestep is forced and the integration method must be restarted. By representing the clock excitations with cubic splines, which have continuous first and second derivatives, these problems are overcome and experimentation indicates that the use of splines allows bigger timesteps to be taken near the clock breakpoints. The internal cubic spline representation [16] can be automatically generated from a user PWL specification.

The NR method requires the solution of a set of simultaneous linear equations at each iteration. These equations are given by the Jacobian matrix of the system whose structure does not change during the iterations. The matrix is sparse and consists of a large number of topological entries ±1, which arise from the MNA constituent equations. To take full advantage of these properties an interpretive code generation approach [17] is used. This method introduces extra op-codes to handle the topological values, therefore enabling redundant multiplications by +1 and -1 to be eliminated. Since only the non-zero operations of the Crout algorithm are performed in a loop-free form, the LU factorization and backsubstitution steps required to solve equations are efficiently performed. The interpretive op-code instruction set is given in figure 1.

IMPLEMENTATION AND CONCLUSIONS

The above techniques are being implemented in a program SCNAPNIT, forming part of an overall suite of SC design and analysis programs (SCNAP series II), sharing a common user interface SCNAPIN. Typical modern SC filter systems involve in excess of 25 time slots and over 50 nodes. The application of these techniques to ideal analysis of such systems has demonstrated the efficiency of the approach.

The non-ideal time analysis program SCNAPNIT is applied to two typical SC networks and the results are shown in figures 2 and 3. The first example is a 5th order elliptic filter [18] with 6 clocks and 20 nodes. A complete MOS model is used for the switches and the output waveform clearly shows clock feedthrough and continuous I/O effects in two clock phases. The second example is a bandpass filter implemented in GaAs with a 4-phase clocking scheme designed to reduce clock-feedthrough. Again precise detail of effects due to complete switch models can be discerned. Applications of this program are not limited to SC filters, but include many new applications of SC technology, for example A to D converters and SSB generators or other forms of switching circuits; providing the tools for detailed studies of non-ideal circuit behaviour.

Of particular importance in SC filter design is the study of distortion effects due to signal dependent clock feedthrough, and non-linearities of amplifiers, switches and stray-capacitances. Because of the harshness of these nonlinearities, a frequency domain approach e.g. Volterra series method is unable to provide an accurate insight into distortion in these structures. A time-domain approach together with Fourier Analysis of the steady-state response of the network is the most viable approach to give a full and detailed distortion analysis.

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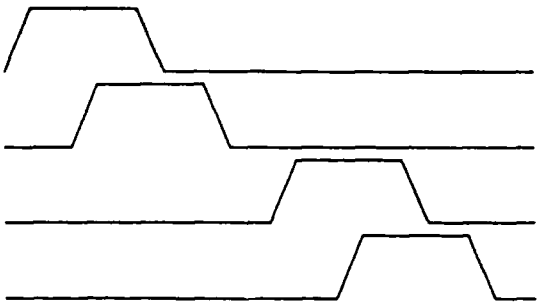

Fig.3a Clock waveforms for bandpass filter

Instruction			Op-code
SUM	=	0	1a
SUM	=	1	2a
SUM	=	-1	3a
SUM	=	V(a)	4a
SUM	=	SUM - 1	5
SUM	=	SUM + 1	6
SUM	=	SUM - V(a)	7a
SUM	=	SUM + V(a)	8a
SUM	=	SUM - V(a)*V(b)	9ab
V(a)	=	SUM/PIVOT	10
V(a)	=	-SUM	11
V(a)	=	SUM	12
PIVOT	=	V(a)	13a
PIVOT	=	SUM	14
SUM	=	B(a)	15a
SUM	=	X(a)	16a
SUM	=	SUM - X(a)	17a
SUM	=	SUM + X(a)	18a
SUM	=	SUM - V(a)*X(b)	19ab
X(a)	=	SUM/V(a)	20a
X(a)	=	SUM	21
X(a)	=	-SUM	22
STOP			23

Figure 1 Interpretive op-codes

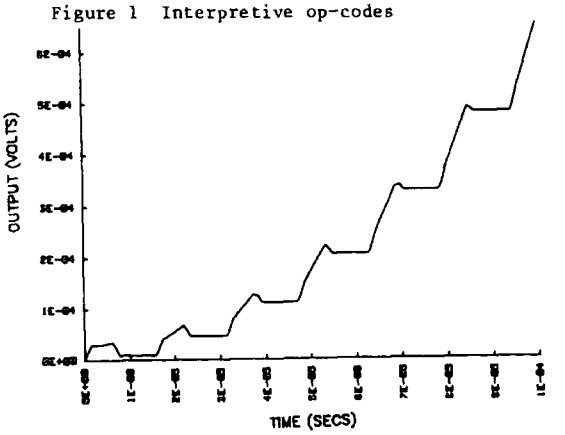

Fig.2 Time response of 5th order Nossek filter with 500Hz sinusoidal excitation

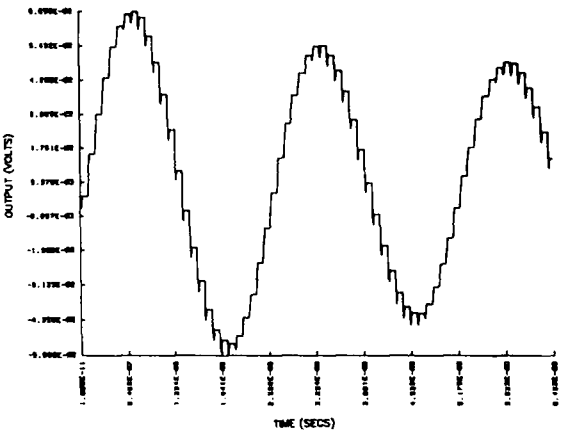

Fig.3b Impulse response for bandpass filter

PAPER 36

General analysis of large linear switched capacitor networks

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Indexing terms: Networks, Circuit theory and design, Matrix algebra, Algorithms

Abstract: A new time and frequency domain analysis method is presented for nonideal switched capacitor networks that is orders of magnitude faster than existing techniques. This efficiency is achieved by developing a formulation such that a continuous AC analysis is not required; this allows the system to be solved as an entirely discrete one. A special compression technique reduces the solution of this discrete system to that of solving the network in one phase only. This final solution step, which ordinarily requires $O(v^3)$ operations (v is the matrix order), is rendered more efficient by reducing the system to upper Hessenberg form in a preprocessing step, when the solution cost is reduced to $O(v^2)$ operations. Sparse matrix techniques, optimal ordering and interpretive code generation are all used to advantage. Performance is compared with existing programs.

1 Introduction

Interest in the design of switched capacitor (SC) networks is being sustained by extension of the range of operational frequencies using gallium arsenide fabrication, by the introduction of large SC systems involving complex decimation and interpolation circuits, and by the incorporation of both filtering and non-filtering applications. It is also noticeable that SC networks form a very important special subset of general switched networks and it would be attractive if any analysis scheme is equally applicable to the general case, if possible.

The history of the development of programs for the analysis of ideal SC circuits is well attested and numerous programs find support in the field. However, the struggle to produce efficient software for the analysis of nonideal SC networks (with finite switch resistances R_{on}, R_{off} and amplifier GB) has proven to be quite a different story.

Three broad approaches to the analysis of nonideal SC networks are discernable. The derivation of an equivalent circuit that could then be incorporated into a traditional continuous time frequency analysis (AC) programs [1, 2] was an early suggestion which still finds support. This method suffers from general inaccuracies of the equivalent circuit and is limited to baseband analysis only. A variant of this approach is to include that analytic solution of the time domain response of single pole amplifiers in the ideal solution of the SC network [3]. Although restricted to two-phase second-order sections, quite accurate results are often attainable. A similar derivation [4] facilitated the incorporation of such ideas into an admittance matrix formulation for computer implementation, though again the calculation of amplifier imperfections was only approximate. The technique of simulating resistance by bilinear switched capacitances, clocked at a high multiple of the switching frequency, is a simple and effective brute force approach, but requires extravagant computer resources [5].

The second approach tackles the more general situation when switch resistances are included together with the nonideal amplifiers. The behaviour of such networks can only be fully described by differential difference equations. General state-space formulations have been proposed [6–8] and , although entirely valid, comprehensive computer implementation of these appears difficult and inefficient. The residual importance of these attempts are concepts that established a foundation for later developments.

The most attractive schemes utilise MNA-based methods to overcome the crucial problems of equation formulation attendent on the latter approach [9]. The various computer implementations have demonstrated the validity of the method and have been restricted only by the approximations inherent in the methods employed for computation of the extended state transition matrices required [9], by difficulties in using symbolic analysis for large nonideal SC networks [10], by the requirement for AC analyses in each clock phase at each frequency point, or by restricted spectral analysis [11].

The need for more efficient nonideal SC analysis software is dictated by two major requirements. In the second phase of SC circuit design, it is generally necessary to perform sensitivity and noise analysis [12], together with an emerging desire to undertake various forms of circuit optimisation; all these demand much speedier and more accurate routines than currently available. The present bound on size of network for analysis in reasonable time with acceptable accuracy occurs at 50 nodes (v) and 10 time-slots (N), or $vN = 500$. It is necessary to overcome this size boundary to facilitate the design of future SC systems with $500 < vN < 1000$ or even higher.

The scheme described in this paper is an attempt to overcome these various problems. It utilises the MNA formulation together with an accurate and reliable method for calculating the extended state transition matrices. An accurate time and frequency method for

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transforming the nonideal SC network into a totally discrete system is developed and previous restrictions to sample and hold inputs [13] are avoided: therefore, full spectral analysis is possible. Extended sparse matrix methods [14, 15] in conjunction with interpretive code generation have been employed where appropriate, and a wide range of matrix and numerical conditioning techniques are utilised. Finally, the program performance is compared with a number of standard programs operating under exactly the same conditions.

2 Definitions

Consider a periodically switched linear network controlled by clock signals $\phi_i(t)$ with a common switching period T, i.e.

$$\phi_i(t + T) = \phi_i(t) \quad \forall t, i \tag{1}$$

where ϕ_i is the state of clock i, either on or off.

Using the definitions in Reference 16, each period T is partitioned into N time-slots:

$$I_{n,k} = (nT + \sigma_{k-1}, nT + \sigma_k] \quad k = 1, \ldots, N \tag{2}$$

such that the clock signals (and therefore the network) does not vary in $I_{n,k}$. Here k denotes the kth time-slot. As shown in Fig. 1, these time-slots are not necessarily of equal duration.

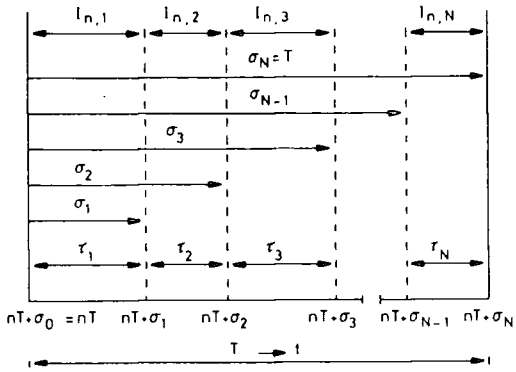

Fig. 1 *Definitions for a N-slot switched linear network*

Define the signals

$$v_k(t) = \begin{cases} v(t) & t \in I_{n,k} \\ 0 & \text{otherwise} \end{cases}$$

$$v_{n,k}(t) = v_k(nT + \sigma_{k-1} + t) \quad 0 < t \leq \tau_k$$
$$= v(nT + \sigma_k - \tau_k + t) \tag{3}$$

$$v_k(nT + \sigma_k) = v(nT + \sigma_k)^- \tag{4}$$

That is, $v_{n,k}(t)$ are functions of time, and $v_k(nT + \sigma_k)$ are sequences of values at the instants just prior to switching.

Define the Z-transform

$$\sum_{n=0}^{\infty} v_k(nT + \sigma_k)z^{-n} = V_k(z) \quad k = 1, \ldots, N-1$$

$$\sum_{n=0}^{\infty} v_N(nT)z^{-n} = V_N(z) \tag{5}$$

and therefore

$$\sum_{n=0}^{\infty} v_N(nT + \sigma_N)z^{-n} = \sum_{n=0}^{\infty} v_N(nT + T)z^{-n}$$
$$= z(V_N(z) - V_N(0)) = zV_N(z) \tag{6}$$

since $V_N(0) = 0$.

3 Time domain analysis

In each time-slot $I_{n,k}$ of the nth switching period $(nT, (n+1)T]$ a periodically switched linear network can be represented by the system differential equation

$$C_k \dot{v}_{n,k}(t) + G_k v_{n,k}(t) = w_{n,k}(t) \quad k = 1, \ldots, N \tag{7}$$

where $w_{n,k}(t)$ is the vector of excitations; $v_{n,k}(t)$ is the vector of unknown system variables; C_k and G_k are constant $(v \times v)$ matrices of capacitance and conductance, determined using the MNA formulation method [9]. In the following, the range of subscripts for k $(k = 1, \ldots, N)$ is dropped for brevity but is assumed throughout unless otherwise stated.

Using the time domain solution method presented in the Appendix we approximate the excitation by mth order polynomials

$$w_{n,k}(t) \approx \sum_{i=0}^{m} \alpha_{i,k}^n t^i \tag{8}$$

where $\alpha_{i,k}^n$ are the coefficients of the polynomial approximations of $w_k(t)$ in the interval $I_{n,k}$. For instance, in the time domain a square wave can be exactly represented by a simple polynomial. Sinusoidal approximations will be required for frequency response considerations, and because of the small time increments involved (owing to the switching frequency) the polynomial approximations for sinusoidal signals are very accurate; typically orders $m = 3$ to 9 ensure errors of $< 10^{-9}$. Substituting expr. 8 in eqn. 7 gives the new system differential equation

$$C_k \dot{v}_{n,k}(t) + G_k v_{n,k}(t) = \sum_{i=0}^{m} \alpha_{i,k}^n t^i \tag{9}$$

Following the steps in the Appendix, the solution of eqn. 9 is

$$v_{n,k}(t) = P_k(t)C_k v_{k-1}(nT + \sigma_{k-1}) + \sum_{i=0}^{m} \alpha_{i,k}^n B_{i,k}(t) \tag{10}$$

where

$$P_k(t) = \mathscr{L}^{-1}\{[sC_k + G_k]^{-1}\} \tag{11}$$

$$B_{i,k}(t) = \mathscr{L}^{-1}\left\{[sC_k + G_k]^{-1} \frac{i!}{s^{i+1}}\right\} \tag{12}$$

$v_{k-1}(nT + \sigma_{k-1})$ are the initial conditions.

A recurrence relation giving the sequence of final states of the system within each time-slot is obtained by substituting $t = \tau_k$ in eqn. 10

$$v_k(nT + \sigma_k) = P_k v_{k-1}(nT + \sigma_{k-1}) + \sum_{i=0}^{m} \alpha_{i,k}^n B_{i,k} \tag{13}$$

where

$$P_k = P_k(\tau_k)C_k \tag{14}$$

$$B_{i,k} = B_{i,k}(\tau_k) \tag{15}$$

The coefficients $\alpha_{i,k}^n$ are obtained by defining

$$h_k = \frac{\tau_k}{m} \tag{16}$$

$$f_{l,k}^n = w_{n,k}(lh_k) \tag{17}$$

and then applying eqn. 53, which gives

$$\alpha_{i,k}^n = \sum_{l=0}^{m} \gamma_{li} f_{l,k}^n \tag{18}$$

Eqn. 13 requires the matrices P_k, given by eqn. 14, and the vectors $B_{i,k}$, given by eqn. 15. Using the definition of the extended state transition matrix (eqn. 11), and applying an IMN approximant of even order M [27], then eqn. 54 gives

$$P_k(\tau_k) \approx \sum_{i=1}^{M/2} \mathrm{Re}\,[2K_i/\tau_k[z_i/\tau_k C_k + G_k]^{-1}] \quad (19)$$

Similarly applying the excitation response approximation (expr. 55) to eqn. 12 gives

$$B_{i,k}(\tau_k) \approx \sum_{j=1}^{M/2} \mathrm{Re}\left[\frac{2K_j/\tau_k\, i!}{(z_j/\tau_k)^{i+1}}\,[z_j/\tau_k C_k + G_k]^{-1}\right] \quad (20)$$

Guidelines for selecting the order of polynomial approximation m are given in the Appendix and the IMN approximant order M and constants of approximation K_i and Z_i elsewhere [27]. The IMN approximant is reputed to be stable and accurate over a wide range of systems applications and this has certainly proved true in the SC network applications outlined here with $M \leqslant 10$.

4 Z-domain analysis

In the general analysis of switched networks it is obviously essential to have an efficient frequency analysis. It would be possible to perform a Fourier transform on a time domain solution, but however efficiently this might be implemented it is hardly likely to provide an acceptable solution. Previous attempts [6–10] at nonideal analysis become very time-consuming at this point of transformation into the Z-domain, primarily because of the need for AC analysis in each clock phase at each frequency point. Fortunately, with the present formulation, a fairly straightforward solution is at hand.

To obtain the Z-domain series of final states $V_k(z)$ for $k = 1, \ldots, N$, we need to take the Z-transform of eqn. 13 and solve for $V_k(z)$.

The Z-transform of eqn. 13 is

$$V_k(z) = P_k V_{k-1}(z) + \Sigma W_k(z) \quad (21)$$

where

$$\Sigma W_k(z) = \sum_{n=0}^{\infty}\left[\sum_{i=0}^{m} \alpha_{i,k} B_{i,k}\right] z^{-n} = \sum_{i=0}^{m} B_{i,k}\left(\sum_{l=0}^{m} \gamma_{li}\, W_k(z) z^{(lh_k - \tau_k)/T}\right) \quad (22)$$

Eqn. 21 can be written in matrix form as

$$\begin{bmatrix} I & & -P_1 \\ -P_2 & I & \\ & \vdots & \\ & & -P_N z I \end{bmatrix}\begin{bmatrix} V_1(z) \\ V_2(z) \\ \vdots \\ V_N(z) \end{bmatrix} = \begin{bmatrix} \Sigma W_1(z) \\ \Sigma W_2(z) \\ \vdots \\ z\Sigma W_N(z) \end{bmatrix} \quad (23)$$

5 Solving the discrete system

A substantial amount of frequency independent preprocessing can be performed in solving eqn. 23. The approach used is based on the method developed in Reference 16 for ideal SC networks. First, all the P_k are frequency independent, hence these can be precomputed using eqn. 19 and stored. Similarly the $B_{i,k}$ in eqn. 15 are independent of frequency and are precomputed using eqn. 20 and stored.

Performing a block Gaussian elimination on eqn. 23

$$(zI - E)V_N(z) = \sum_{k=1}^{N} E_k \Sigma W_k(z) \quad (24)$$

where

$$E = P_N P_{N-1} \cdots P_2 P_1 \quad (25)$$

$$E_k = \begin{cases} P_N P_{N-1} \cdots P_{k+1} & k = 1, \ldots, N-1 \\ I & k = N \end{cases} \quad (26)$$

Matrices E and E_k are frequency independent and are only computed once prior to frequency analysis. The multiplication by E_k can be distributed over the summation in the excitation $\Sigma W_k(z)$ as a preprocessing step, giving

$$\Sigma W_k(z) = \sum_{i=0}^{m} F_{i,k} \sum_{l=0}^{m} \gamma_{li}\, W_k(z) z^{(lh_k - \tau_k)/T} \quad (27)$$

where

$$F_{i,k} = E_k B_{i,k}. \quad (28)$$

Eqn. 24 then reduces to

$$(zI - E)V_N(z) = \sum_{k=1}^{N} \Sigma W_k(z) \quad (29)$$

which can be very efficiently solved for $V_N(z)$ using methods discussed below. The solutions for $V_k(z)$ for $k = 1, \ldots, N-1$ are then obtained by block back-substitution,

$$V_1(z) = P_1 V_N(z) + \Sigma W_1(z)$$
$$V_k(z) = P_k V_{k-1}(z) + \Sigma W_k(z) \quad k = 2, \ldots, N-1 \quad (30)$$

Using the direct Gauss elimination method to solve eqn. 29 requires $O(v^3)$ flops. This cost is excessive for large networks, especially when many frequency points are evaluated. It can be reduced to $O(v^2)$ flops by transforming the system to upper Hessenberg form, which only needs to be done once, in a frequency-independent step. This method, which has been applied to the frequency analysis of linear systems [17], has also been used in SC frequency analysis [11].

A general matrix E can always be reduced to Hessenberg form by stabilised elementary transformations [18]

$$H = T^{-1} P^{-1} E P T \quad (31)$$

where T is a triangular transformation matrix and P is a permutation matrix. The transformation matrix T and Hessenberg matrix H can be determined in approximately $5/6v^3$ flops using real arithmetic throughout.

Applying the stabilised elementary transformation to eqn. 29 gives

$$PT(zI - T^{-1} P^{-1} E P T) T^{-1} P^{-1} V_N(z) = \sum_{k=1}^{N} \Sigma W_k(z) \quad (32)$$

which may be written in a simplified form as

$$(zI - H)y = b \quad (33)$$

where

$$H = T^{-1} P^{-1} E P T$$
$$y = T^{-1} P^{-1} V_N(z) \quad (34)$$
$$b = T^{-1} P^{-1} \sum_{k=1}^{N} \Sigma W_k(z) \quad (35)$$

To form the vector b, the inverse of T is not actually calculated as the equivalent operation is accurately and efficiently obtained by the process of back-substitution using matrix T. A substantial amount of this calculation can be performed as a preprocessing step by rewriting

eqn. 35 as

$$\boldsymbol{b} = \sum_{k=1}^{N} \Sigma \boldsymbol{W}_k^p(z) \tag{36}$$

where

$$\Sigma \boldsymbol{W}_k^p(z) = \sum_{i=0}^{m} \boldsymbol{J}_{i,k} \sum_{l=0}^{m} \gamma_{li} W_k(z) z^{(lh_k - \tau_k)/T} \tag{37}$$

and

$$\boldsymbol{J}_{i,k} = \underline{\boldsymbol{T}}^{-1} \boldsymbol{P}^{-1} \boldsymbol{F}_{i,k} \tag{38}$$

Eqn. 33 is solved using the direct LU approach. By taking advantage of the structure of the Hessenberg matrix, both terms of zero/nonzero and real/complex structure, the computation is reduced from $4/3v^3$ to $2v^2$ flops. The forward elimination and back-substitution steps together require approximately $2v^2$ flops. Finally, the required solution $\boldsymbol{V}_N(z)$ is determined by multiplying y by the transformation matrix, which requires a further v^2 flops. The total solution process then requires approximately $5v^2$ flops, which is a dramatic improvement over the direct approach.

6 Frequency analysis

To solve the discrete system (eqn. 23) for a particular frequency ω_0, substitute

$$z = e^{j\omega_0 T} \tag{39}$$

Applying Poisson's formula to $\Sigma \boldsymbol{W}_k(z)$ gives

$$\begin{aligned}\Sigma \boldsymbol{W}_k(e^{j\omega T}) &= \sum_{n=0}^{m} \left[\sum_{i=0}^{m} \left(\sum_{l=0}^{m} \gamma_{li} \right.\right. \\ &\quad \left.\left. \times W_k(nT + \sigma_k + lh_k - \tau_k) \right) \boldsymbol{B}_{i,k} \right] e^{-jn\omega T} \\ &= \frac{1}{T} \sum_{n=0}^{\infty} \left[\sum_{i=0}^{m} \boldsymbol{B}_{i,k} \sum_{l=0}^{m} \gamma_{li} W(\omega - n\omega_s) \right. \\ &\quad \left. \times \exp\left(j(\omega - n\omega_s)(\sigma_k + lh_k - \tau_k)\right) \right] \end{aligned} \tag{40}$$

Now, it is shown in Reference 16 that

$$\sum_{n=0}^{\infty} W(\omega - n\omega_s) e^{j(\omega - n\omega_s)\sigma_k} = 2\pi e^{j\omega_0 \sigma_k} \tag{41}$$

which is independent of n. Using this result in eqn. 40 gives

$$\Sigma \boldsymbol{W}_k(e^{j\omega_0 T}) = \frac{2\pi}{T} \sum_{i=0}^{m} \boldsymbol{B}_{i,k} \sum_{l=0}^{m} \gamma_{li} e^{j\omega_0(\sigma_k + lh_k - \tau_k)} \tag{42}$$

Applying window functions to the output signals [19] and taking into account the $\sin x/x$ sampling effect and possibly unequal time-slots, the frequency response of the system is given by [16]

$$\boldsymbol{S}_n = \sum_{k=1}^{N} D_{k,n} \boldsymbol{V}_k(e^{j\omega_0 T}) \tag{43}$$

where

$$D_{k,n} = \frac{e^{-j\omega\sigma_{k-1}} - e^{-j\omega\sigma_k}}{j\omega T} \quad k \neq N \tag{44}$$

$$D_{N,n} = e^{j\omega_0 T} \frac{e^{-j\omega\sigma_{N-1}} - e^{-j\omega\sigma_N}}{j\omega T} \tag{45}$$

and

$$\omega = \omega_0 + n\omega_s$$

Assembling all the above leads to the following overall algorithm for the frequency domain analysis:

(*a*) *Preprocessing independent of frequency and n*

(i) Formulate the matrices $\boldsymbol{G}_k$ and $\boldsymbol{C}_k$ and the vectors $\boldsymbol{W}_k$

(ii) Calculate $\boldsymbol{P}_k$ matrices using eqns. 14 and 19

(iii) Calculate $\boldsymbol{B}_{i,k}$ vectors using eqn. 20 for $i = 0, \ldots, m$

(iv) Calculate matrix $\boldsymbol{E}$ using eqn. 25

(v) Calculate $\boldsymbol{F}_{i,k}$ vectors using eqn. 28 for $i = 0, \ldots, m$

(vi) Transform matrix $\boldsymbol{E}$ to upper Hessenberg form $\boldsymbol{H}$ using eqn. 31

(vii) Calculate vectors $\boldsymbol{J}_{i,k}$ using eqn. 38

(*b*) *Frequency analysis independent of n*

(i) Prepare matrix $(e^{j\omega_0 T}\boldsymbol{I} - \boldsymbol{H})$

(ii) Build RHS of eqn. 33 using eqns. 36 and 37

(iii) Solve eqn. 33 for $\boldsymbol{V}_N(e^{j\omega_0 T})$ using the Hessenberg method

(iv) Calculate $\boldsymbol{V}_k(e^{j\omega_0 T})$ using eqn. 30

(*c*) *Spectral analysis*

(i) For selected n calculate weights $D_{k,n}$ using eqns. 44 and 45

(ii) Calculate $\boldsymbol{S}_n$ using eqn. 43

8 Results

The theory developed above was implemented in the program QUICKSCNAP using 16-digit double-precision arithmetic throughout. In the preprocessing section maximum use is made of sparse techniques, utilising new interpretive code and optimal ordering algorithms [15]. Full matrix techniques are used in the frequency response calculations. A dynamic storage allocation scheme is used throughout. Numerical accuracy has been checked by comparison with measured results and with a selection of computed results from other established programs, when agreement was better than five significant figures. A representative sample of large SC networks is references in Table 1.

Table 1: Examples used for comparison

	Description
1	6th order Chebychev bandpass filter [20]
2	11th order elliptic lowpass filter [21]
3	7th order Chebychev lowpass filter [22]
4	15th order elliptic lowpass, LUD design [23]
5	SPFT elliptic bandpass filter system [24]
6	18th order elliptic bandpass filter [25]

The run statistics for a selection of these programs SCNAPNIF and SCNAPIF [14], SWITCAP [5] and QUICKSCNAP are shown in Tables 2–5. All results are

Table 2: Run statistics for QUICKSCNAP

Example	Number of nodes	Number of slots	Pre-Pr. sec	Time/pt, sec	Storage, words
1	28	2	5.55	0.114	16890
2	41	4	22.7	0.320	39944
3	30	6	12.4	0.234	27002
4	69	2	47.6	0.679	95210
5	86	36	14.52	13.44	824944
6	77	5	93.4	1.512	145854

Table 3: Run statistics for SCNAPNIF

Example	Number of nodes	Number of slots	Pre-Pr., sec	Time/pt, sec	Storage, words
1	28	2	35.7	5.37	39682
2	41	4	265.0	28.65	100489
3	30	6	141.0	18.32	71070
4	69	2	377.0	74.11	230217
5	86	36	—	—	—
6	77	5	1308.0	216.0	368254

Table 4: Run statistics for SCNAPIF

Example	Number of nodes	Number of slots	Pre-Pr., sec	Time/pt, sec	Storage, words
1	28	2	0.64	0.046	51849
2	41	4	1.94	0.161	57162
3	30	6	1.32	0.137	53276
4	69	2	2.33	0.237	74415
5	86	36	103.0	17.48	456383
6	77	5	5.88	1.156	410674

Table 5: Run statistics for SWITCAP

Example	Number of nodes	number of slots	Pre-Pr., sec	Time/pt, sec	Storage words
1	28	2	6.14	0.207	11852
2	41	4	—	—	—
3	30	6	—	—	—
4	69	2	25.9	1.621	34188
5	86	36	—	—	—
6	77	5	—	—	—

from implementations on a μVAX II computer, run under VMS. It can be seen that the storage requirements for QUICKSCNAP compare favourably with other programs. For analysis of large nonideal (finite amplifier GB and switch R_{on} and R_{off}) SC networks, Tables 2 and 3 give a fair comparison against currently available software, indicating improvements in speed by a factor of 200. The preprocessing times also show a speedup factor of 10, directly attributable to the enhanced sparse techniques utilised. Note that Example 5 is beyond the capibility of program SCNAPNIF. Tables 4 and 5 show performance figures produced by programs specifically designed for the analysis of ideal SC networks, and it is interesting to observe that although QUICKSCNAP undertakes a complete nonideal analysis, comparison shows that its performance lies between SCNAPIF and SWITCAP, being approximately twice as fast as the latter. While SWITCAP can approximate a nonideal analysis, the run times are in terms of hours. SWITCAP requires that the network is not disjointed in any clock phase, and this explains the limited selection of successful examples in Table 5; although a straightforward fix is possible, this requires modification of the circuit by the user.

Similar conclusions are apparent from the graphs shown in Figs. 2 and 3, which display the relative performances of the programs for two-phase SC networks.

9 Conclusions

A new analysis scheme has been demonstrated to maintain accuracy, while providing orders of magnitude improvement in speed of analysis. The computational cost of the analysis increases linearly with the number of time-slots and quadratically with the number of nodes. This affords the user a facility to breach the existing $vN = 500$ boundary, while containing time and storage requirements within bounds typical of generally available small computers. It is expected that this will provide a sound basis for noise and sensitivity analysis, with extension to optimisation studies.

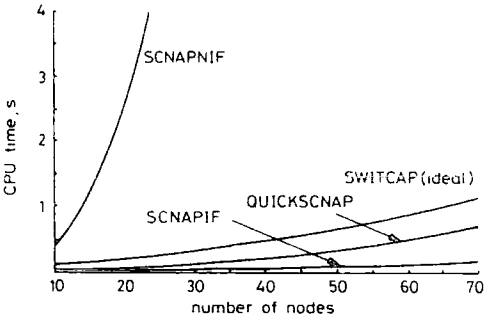

Fig. 2 *Comparison of run-times per frequency point*

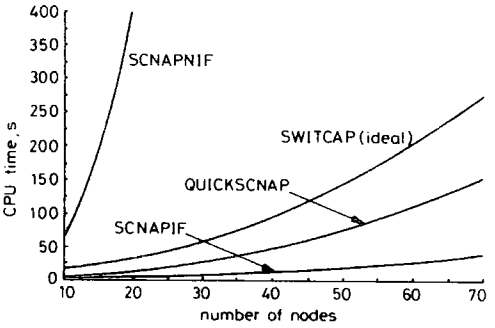

Fig. 3 *Comparison of overall run-times (150 frequency points)*

The frequency analysis algorithms are highly suited to vectorisation, which could provide further dramatic improvements when implemented on a suitable processor.

10 Acknowledgment

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12 Appendix: The stepping inverse Laplace transform (SILT) method

Consider the algebraic-differential system

$$C\dot{x}(t) + Gx(t) = w(t) \quad x(0) = X_0 \tag{46}$$

where $x(t)$ is the unknown response vector, $w(t)$ is the excitation vector, C and G are constant real matrices. The SILT method provides an attractive solution technique for eqn. 46. The excitation vector is approximated by the vector of mth order polynomials,

$$P_m(t) = \sum_{k=0}^{m} \alpha_k t^k \tag{47}$$

Substituting eqn. 47 into eqn. 46 and taking the Laplace transform,

$$X(s) = [sC + G]^{-1}\left\{CX_0 + \sum_{k=0}^{m} \frac{\alpha_k k!}{s^{k+1}}\right\} \tag{48}$$

The inverse Laplace transform of eqn. 48 is then,

$$x(t) = P(t)Cx(0) + \sum_{k=0}^{m} \alpha_k B_k(t) \tag{49}$$

where

$$P(t) = \mathcal{L}^{-1}\{[sC + G]^{-1}\} \tag{50}$$

called the extended state transition (EST) matrix, and

$$B_k(t) = \mathcal{L}^{-1}\left\{[sC + G]^{-1}\frac{k!}{s^{k+1}}\right\} \tag{51}$$

called the excitation response (ER) matrix.

In lumped linear networks, time zero can be arbitrarily selected by taking into account the initial conditions of the network; therefore, dividing the time axis into equal steps Δt, where $t = n\Delta t$, we have

$$x((n+1)\Delta t) = P(\Delta t)Cx(n\Delta t) + \sum_{k=0}^{m} \alpha_k^n B_k(\Delta t) \tag{52}$$

where α_k^n are the coefficients of the polynomial approximations of $w(t)$ in the interval $[n\Delta t, n\Delta t + \Delta t]$. A closed form expression for the α_k^n can be derived using the Newton-Gregory interpolation formula. After considerable manipulation this becomes

$$\alpha_k^n = \sum_{i=0}^{m} \gamma_{ki}\, w\left(n\Delta t + \frac{i\Delta t}{m}\right) \tag{53}$$

where γ_{ki} are tabulated constants. These constants are easily computed and the constants for orders 1 to 4 are shown in Table 6.

Table 6: Gamma coefficients for orders 1 to 4

1		1	0		
		-1	1		
2	1/2	2	0	0	
		-3	4	-1	
		1	-2	1	
3	1/6	6	0	0	0
		-11	18	-9	2
		6	-15	12	-3
		-1	3	-3	1
4	1/24	24	0	0	0	0
		-50	96	-72	32	-6
		35	-104	114	-56	11
		-10	36	-48	28	-6
		1	-4	6	-4	1

The inverse Laplace transforms (eqns. 50 and 51) are computed using a numerical quadrature approximation of the Laplace tansform inversion integral [26, 27]. The constants for the approximation (K_i and z_i), are tabulated complex constants and for an IMN approximant of even order M these occur in $M/2$ complex conjugate pairs, which allows the computation to be halved. Hence the extended state transition matrix approximation is

$$P(\Delta t) \approx \sum_{i=1}^{M/2} \mathrm{Re}\,[2K_i/\Delta t[z_i/\Delta t C + G]^{-1}] \tag{54}$$

and the excitation response matrix approximation

$$B_k(\Delta t) \approx \sum_{i=1}^{M/2} \mathrm{Re}\left[\frac{2K_i/\Delta t k!}{(z_i/\Delta t)^{k+1}}\,[z_i/\Delta t C + G]^{-1}\right] \tag{55}$$

The above computations can be efficiently implemented using sparse matrix methods [15].

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Efficient Sensitivity Analysis for Large Non-ideal Switched Capacitor Networks

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Abstract **- A new sensitivity analysis method in the frequency domain is presented for non-ideal switched capacitor networks that is more general and efficient than the previously published works. There are no restrictions on the number of clock phases, circuit configuration and input signal type (which can be either continuous or sample-and-hold). By performing a substantial amount of frequency independent pre-processing and using adjoint network techniques, the computational costs are reduced dramatically and a highly efficient method results. The method has been implemented in a SC network analysis program called SCNAP4. Numerical results of the sensitivity analysis of a fifth order elliptic low pass filter are given.**

I. INTRODUCTION

The sensitivity analysis of ideal SC networks is well established and forms part of the designers standard tool-kit. The present trend to extend the application of SC networks to high frequency front-ends with multi-rate clocks raises the serious question of sensitivity of the circuit structures with respect to non-ideal parameters such as switch resistance and finite amplifier parameters - gain/bandwidth, input and output impedances; sensitivity of parasitic capacitances is also required.

A number of programs can undertake various frequency and time domain analysis of non-ideal SC networks [1-4]. A range of techniques have been utilized to increase speed, improve accuracy and cope with large networks and multiple clock waveforms [4]. However an efficient sensitivity analysis of general non-ideal SC networks is conspicuously absent.

The method described, avoids the multiple solution of very large system matrix in the frequency domain and requires only one solution of the system and its adjoint. The pre-processing of a large amount of frequency independent material reduces computation costs and interpretable code generation, polynomial approximation of the excitation, descretization of the whole system and Hessenburg techniques are fully exploited.

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II. GENERAL SENSITIVITY ANALYSIS METHOD FOR ARBITRARY LINEAR NETWORKS

For an arbitrary linear system, $\mathbf{TX} = \mathbf{W}$, where $\mathbf{T}$ is the system matrix, $\mathbf{X}$ is the unknown response vector and $\mathbf{W}$ denotes the excitation vector. If the output of interest Φ (a linear combination of the components of $\mathbf{X}$) is $\Phi = \mathbf{d}^T\mathbf{X}$, where $\mathbf{d}$ is a constant vector and $\mathbf{d}^T$ denotes the transpose, then standard sensitivity theory follows:

The adjoint vector $\mathbf{X}_a$ is defined by $\mathbf{X}_a^T = -\mathbf{d}^T\mathbf{T}^{-1}$ or $\mathbf{T}^T\mathbf{X}_a = -\mathbf{d}$ and the sensitivity of Φ with respect to the vector of parameter changes h is $\frac{\partial\Phi}{\partial h} = \mathbf{X}_a^T\frac{\partial\mathbf{T}}{\partial h}\mathbf{X} - \mathbf{X}_a^T\frac{\partial\mathbf{W}}{\partial h}$

The computational procedure for the adjoint approach can be summarized:

step 1: Solve for $\mathbf{X}$;
step 2: Calculate $\mathbf{X}_a$;
step 3: Formulate $\partial\mathbf{T}/\partial h$ and $\partial\mathbf{W}/\partial h$;
step 4: Calculate $\partial\Phi/\partial h$.

The method is clear and straightforward. The advantage of this procedure is that the vectors $\mathbf{X}$ and $\mathbf{X}_a$ are only calculated once, irrespective of the number of parameters. The transpose solution $\mathbf{X}_a$ can be efficiently obtained using similar steps to those used in solving for $\mathbf{X}$, which does not require another network analysis.

Unfortunately, for non-ideal SC networks, the system matrix $\mathbf{T}$ in the frequency domain cannot be expressed explicitly in terms of circuit parameters. Since $\mathbf{T}$ is not in analytical form, the partial derivative $\partial\mathbf{T}/\partial h$ cannot be performed directly. This problem is due to the extended state transition matrix (EST) which can only be formed by approximation techniques with various degrees of accuracy [2-3].

III. SENSITIVITY ANALYSIS ANALYSIS FOR NON-IDEAL SC NETWORKS

For general linear SC networks, the system matrix equation in z domain can be written in the form [4]

$$\begin{bmatrix} \mathbf{I} & & & -\mathbf{P}_1 \\ -\mathbf{P}_2 & \mathbf{I} & & \\ & \ddots & \ddots & \vdots \\ & & -\mathbf{P}_N & z\mathbf{I} \end{bmatrix} \begin{bmatrix} \mathbf{V}_1(z) \\ \mathbf{V}_2(z) \\ \vdots \\ \mathbf{V}_N(z) \end{bmatrix} = \begin{bmatrix} \Sigma \mathbf{W}_1(z) \\ \Sigma \mathbf{W}_2(z) \\ \vdots \\ z\Sigma \mathbf{W}_N(z) \end{bmatrix} \quad (1)$$

or $\mathbf{TX} = \mathbf{W}$. Here

$$\mathbf{P}_k = \mathbf{p}_k \mathbf{C}_k \quad (2)$$

$$\sum \mathbf{W}_k(z) = \sum_{n=0}^{\infty} [\sum_{i=0}^{m} \alpha_{i,k} \mathbf{B}_{i,k}] z^{-n} \quad (3)$$

where

$$\mathbf{p}_k = \mathcal{L}^{-1}\left\{[\mathbf{G}_k + s\mathbf{C}_k]^{-1}\right\} \quad (4)$$

$$\mathbf{B}_{i,k} = \mathcal{L}^{-1}\left\{[\mathbf{G}_k + s\mathbf{C}_k]^{-1} \frac{i!}{s^{i+1}}\right\} \quad (5)$$

$\mathcal{L}^{-1}$ denotes the inverse Laplace transformation; $\mathbf{p}_k$ is defined as the extended state transition matrix (EST); $\mathbf{B}_{i,k}$ is called the excitation response matrix; $\alpha_{i,k}$ is the coefficient of the m th order polynomial which is used to approximate the excitation; $\mathbf{V}_k(z)$ is a vector of nodal voltages and some branch currents; $\mathbf{G}_k$ is the conductance matrix; $\mathbf{C}_k$ is the capacitance matrix and $\mathbf{I}$ denotes the identity matrix. In the computation of frequency response, $\mathbf{p}_k$, $\mathbf{B}_{i,k}$ are frequency independent, so they can be pre-calculated.

Since $\mathbf{p}_k$ and $\mathbf{B}_{i,k}$ are produced by numerical techniques, the major problem is to determine the partial derivatives of $\mathbf{p}_k$ and $\mathbf{B}_{i,k}$

Differentiate (4) with respect to h

$$\begin{aligned} \frac{\partial \mathbf{p}_k}{\partial h} &= \frac{\partial}{\partial h}\left\{\mathcal{L}^{-1}[\mathbf{G}_k + s\mathbf{C}_k]^{-1}\right\} \\ &= \frac{\partial}{\partial h}\left\{\frac{1}{2\pi j}\int_{c-\infty}^{c+\infty}[\mathbf{G}_k + s\mathbf{C}_k]^{-1} e^{st} ds\right\} \\ &= \frac{1}{2\pi j}\int_{c-\infty}^{c+\infty}\left\{\frac{\partial}{\partial h}[\mathbf{G}_k + s\mathbf{C}_k]^{-1}\right\} e^{st} ds \\ &= \mathcal{L}^{-1}\left\{\frac{\partial}{\partial h}[\mathbf{G}_k + s\mathbf{C}_k]^{-1}\right\} \end{aligned} \quad (6)$$

Define the system matrix in time-slot k as

$$\mathbf{M}_k = \mathbf{G}_k + s\mathbf{C}_k \quad (7)$$

Because $\mathbf{M}_k \mathbf{M}_k^{-1} = \mathbf{I}$ (8)

differentiate (8) with respect to h to obtain

$$\frac{\partial \mathbf{M}_k}{\partial h}\mathbf{M}_k^{-1} + \mathbf{M}_k \frac{\partial \mathbf{M}_k^{-1}}{\partial h} = \mathbf{0} \quad (9)$$

and rewrite as follows

$$\frac{\partial \mathbf{M}_k^{-1}}{\partial h} = -\mathbf{M}_k^{-1}\frac{\partial \mathbf{M}_k}{\partial h}\mathbf{M}_k^{-1} \quad (10)$$

Hence

$$\frac{\partial \mathbf{p}_k}{\partial h} = \mathcal{L}^{-1}\left\{\left[-\mathbf{M}_k^{-1}\frac{\partial \mathbf{M}_k}{\partial h}\mathbf{M}_k^{-1}\right]\right\} \quad (11)$$

The inverse system matrix $\mathbf{M}_k^{-1}$ and the derivative $\partial \mathbf{M}_k/\partial h$ can be calculated easily. Therefore, $\partial \mathbf{p}_k/\partial h$ can now be evaluated by using the I_{mn} [6-7] approximation, the same step as used in calculating the extended state transition matrix $\mathbf{p}_k$. Similarly, $\partial \mathbf{B}_{i,k}/\partial h$ can be evaluated. Both $\partial \mathbf{p}_k/\partial h$ and $\partial \mathbf{B}_{i,k}/\partial h$ are frequency independent and can be pre-calculated. Hence the computation of $\partial \mathbf{T}/\partial h$ and $\partial \mathbf{W}/\partial h$ follow in a straightforward manner and the general procedure for non-ideal sensitivity analysis can be completed. Salient features of the method are:

(a) It is completely general. The analysis is not only applicable to switched capacitor networks, but also to general linear networks. No restrictions are placed on the type of signal, circuit configuration and number of clock phases. Therefore the method is suited for mixed-mode analysis applications.

(b) The method is also very efficient. After pre-processing of all frequency independent equation components, the sensitivity analysis procedure follows a similar pattern used for ideal SC network analysis. Previous non-ideal SC network sensitivity analysis needed three solutions of the large system equations, here only two are needed.

(c) The results of the method are reliable and accurate. The only approximation employed in this method is the I_{mn} approximant which experience has shown to be stable and accurate over wide range of systems applications.

IV. NUMERICAL RESULTS

The above method for sensitivity analysis of non-ideal switched capacitor networks has been implemented in the program SCNAP4. A fifth order elliptic low-pass four phases SC filter [8] is used as an example and illustrated in Fig.1. The sensitivity of the response with respect to C_1 (a capacitor in the circuit) and GB_1 (the gain bandwidth product of opamp 1) are shown in Fig.2a and Fig.2b, respectively. The accuracy of the results have been verified by comparison with those produced by other techniques.

V. CONCLUSIONS

This paper presents a new non-ideal sensitivity analysis scheme for SC networks. The method is both general and efficient. No restrictions are imposed regarding circuit configuration, number of clock phases or excitation signal. The implementation of the method is straightforward. Numerical results confirm the validity

and efficiency of the method.

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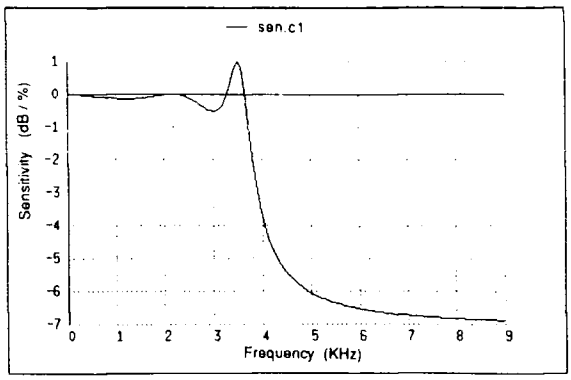

Fig. 2a. Sensitivity with respect to C_1 with nonideal opamps (GB=159kHz)

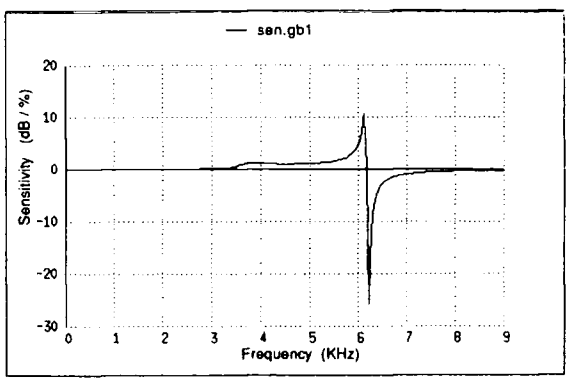

Fig. 2b. Sensitivity with respect to GB_1 with nonideal opamps (GB=159kHz)

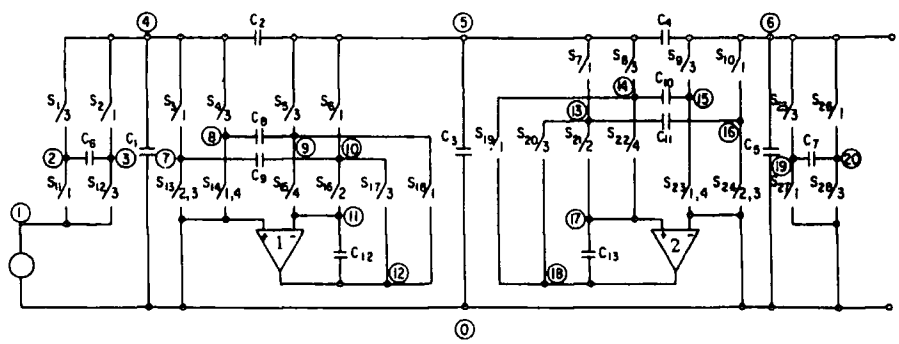

Fig. 1. 5th order elliptic low-pass SC filter

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Efficient noise analysis methods for large non-ideal SC and SI circuits

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ABSTRACT

A fully general and efficient noise analysis method is presented for both switched capacitor and switched-current circuits. The fold-back effects and non-ideal effects such as parasitic resistive time constant have been taken into account. The thermal noise and flicker noise generated by MOS transistors are considered. By utilising the adjoint network technique, only one system solution is needed for noise analysis. In addition, numerical inversion of the Laplace transformation, the Hessenberg technique, extensive sparse matrix routines and interpretable code generation have been used to improve the efficiency of noise analysis. The method has been implemented in SCNAP4 and numerical results are given in the last section.

I INTRODUCTION

Since the early years of last decade, noise analysis for SC circuits has been discussed frequently [1-7]. However most of the presented techniques are only adequate for small circuits. General and efficient methods were seldom mentioned. Recently, switched-current circuits have gained much attention. Naturally, their noise characteristics are of main concern to designers. Generally, two types of noise are considered in SC circuits, white noise from switches and 1/f noise from operational amplifiers. For switched-current circuits, since the MOS transistors operate in saturation regions, both thermal and flicker noise exist.

Unlike the traditional analogue case (switch free), the folding of wideband white noise from high frequency bands to baseband, caused by the sampling nature of switched-circuits, leads to excessive computational costs. Traditionally, in order to calculate the whole noise spectral density, the folding transfer functions from each noise source to output have to be evaluated. For example, a circuit containing m noise sources requires m different system solutions at each frequency point. Furthermore, as the noise bandwidths are normally orders of magnitude higher than the sampling frequency, a very large number of system solutions are needed to cover the wide frequency range for taking folding effects into account. Therefore, without efficient and general methods, noise analysis is either very time consuming or the results tend to be unreliable.

The method developed in this paper is based on the adjoint network technique which had been successfully applied to non-ideal sensitivity analysis of switched linear networks[8]. For noise analysis, only the adjoint system solution is required and the original system solution is no longer necessary. The L_{mn} approximation for extended transition matrix and Hessenberg technique for solving the adjoint system as well as the pre-processing of a large amount of frequency independent material reduce computation costs dramatically and hence a highly efficient method results. By using spectral analysis technique the fold-back effects can be accurately evaluated. In the following sections, these aspects will be discussed in detail.

II ADJOINT NETWORK TECHNIQUES

The task of noise analysis can be divided into two different aspects,

(a) reducing the overall number of system solutions;

(b) efficient methods for each individual system solution.

The second aspect has already been considered when SCNAP4 was being developed. A solid platform for noise analysis has been built successfully. In the following, we will focus on the first issue.

For general linear switched networks, if the system contains m noise sources, the problem can be described by

$$\begin{bmatrix} I & & & -P_1 \\ -P_2 & I & & \\ & \ddots & \ddots & \vdots \\ & & -P_N & zI \end{bmatrix} \begin{bmatrix} V_1^i(z) \\ V_2^i(z) \\ \vdots \\ V_N^i(z) \end{bmatrix} = \begin{bmatrix} \Sigma W_1^i(z) \\ \Sigma W_2^i(z) \\ \vdots \\ z\Sigma W_N^i(z) \end{bmatrix} \quad (1)$$

or

$$T X_i = W_i \quad (i=0,1,\ldots,m)$$

where T denotes the system matrix in z domain, X_i and W_i are unknown and excitation vectors, respectively. $P_k = p_k C_k$. p_k is defined as the extended state transition matrix, I denotes the identity matrix.

For the ith noise source, the transfer function from the noise source to output can be defined as

$$H_i(\omega) = d^t X_i \tag{2}$$

with d representing a constant vector.

Define the adjoint system as,

$$T^t X_a = -d \tag{3}$$

Substitute (1), (3) into (2) gives

$$H_i(\omega) = -X_a^t W_i \tag{4}$$

Assuming that there is no correlation between the input noise sources, the total noise power spectral density at the output is then calculated by superposition

$$S_T(\omega) = \sqrt{\sum_{n=0}^{p}\sum_{i=1}^{m}|H_i(\omega)|^2 S_i(\omega - n\omega_s)} \tag{5}$$

where $S_i(\Omega)$ is the ith input noise power spectral density and p is the number of bands to be considered. Here the nth band is defined as the frequency interval from $(n-1)\omega_s/2$ to $n\omega_s/2$ where ω_s is the sample frequency. Several comments can be made at this stage.

1) It is evident that after solving the adjoint system (eq. (3)), $H_i(\omega)$ can be obtained directly by merely one subtraction since each W_i contains at most two nonzero entries . Instead of *m* different network analyses, only one adjoint system solution is needed for all *m* noise sources, the original system solution can be saved. Therefore computational efficiency is achieved.

2) The adjoint system is solved by using the Hessenberg approach which has already been proved very effective in frequency domain analysis of switched linear networks.

3) The folding effects from high frequencies to a specific band are evaluated up to a user given noise bandwidth. This is based on the fact that the noise is normally bandlimited by op-amp frequency response and time constant effects from switch resistances and circuit capacitances.

III NOISE ANALYSIS OF SWITCHED-CURRENT CIRCUITS

The noise behaviour of switched-current circuits has received considerable attention since the emergence of switched-current techniques [11-13]. It is wise to choose the basic switched-current memory ceil, as shown in Figure 1, to start with. Both transistors M_1 and M_2 operate in saturation region, hence generate both flicker noise and thermal noise. The flicker noise is modelled as a gate-referred noise which generates a drain noise current. The thermal noise is modelled as a drain-referred noise current. The thermal noise from switches is treated in the same way as that was in SC circuits. By modelling the MOS transistor with a macromodel which consists of linear components, SCNAP4 can be used directly to analyse switched-current circuits. Detailed discussion about the models of MOS transistors for switched-current circuits can be found in [14].

IV NUMERICAL RESULTS

The noise analysis method presented above has been implemented in the program SCNAP4. Two types of noise source (voltage and current) are available, they can be either flicker noise or white noise. The foldover wideband white noise from high frequency bands to baseband can be calculated.

Two examples are given. For SC circuits, a sixth order bandpass filter is selected. The op-amp noise components are given to be $80nV/\sqrt{Hz}$ with corner frequency 1kHz. The output noise spectrum density is illustrated in Figure 2. A close agreement between simulation and results from [5] can be noted. The fold back effects are also shown in Fig. 2. For switched-current circuits, a third-order elliptic ladder is considered. The noise bandwith is about 160MHz and the corner frequency is set to 1KHz. If the reference noise is $1nA/\sqrt{Hz}$, then the circuit response and noise behaviour are illustrated in Figure 3 and Figure 4 respectively. The CPU time for analysing these circuits are given in Table 1. It is evident that even for circuits with moderate size, SCNAP4 is able to give noise analysis results in fairly short time.

V CONCLUSIONS

This paper presents a general and efficient noise analysis method applicable to both SC and SI circuits. Standard circuit non-idealities are included and complete folding effects for broadband noise are incorporated. An adjoint description of the non-ideal network is employed and only the solution of this is required. Numerical results compare well with practical results measured from integrated circuits. The speed of analysis on a relatively model work station indicates that noise analysis of large switched

systems is feasible and the application to some degree of noise optimisation is a realistic possibility.

ACKNOWLEDGEMENT

Z.Q. Shang gratefully acknowledges the financial support of the British Council.

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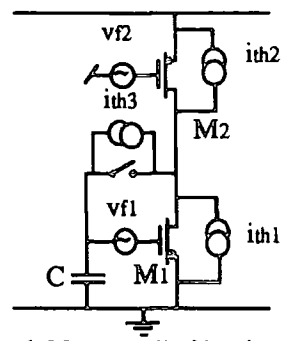

Figure 1. Memory cell with noise sources

Table 1. Statistics of noise simulation on SUN-Sparc ELC station

Circuit name	Signal type	Circuit size	Number of slots	Points per band	Number of bands	Noise analysis(sec)
bp6(SC)	S/H	48	2	100	1	3.76
bp6(SC)	S/H	48	2	100	50	187.69
bp6(SC)	S/H	48	2	100	100	382.25
nos5(SC)	S/H	28	4	100	1	2.62
nos5(SC)	CONT	28	4	100	1	12.13
nos5(SC)	S/H	28	4	100	10	26.81
swc6(SI)	S/H	37	2	100	1	2.41
elp3(SI)	S/H	38	2	106	1	2.92
elp3(SI)	S/H	38	2	106	8	22.77
elp3(SI)	CONT	38	2	106	1	12.14
elp3(SI)	CONT	38	2	106	8	96.13

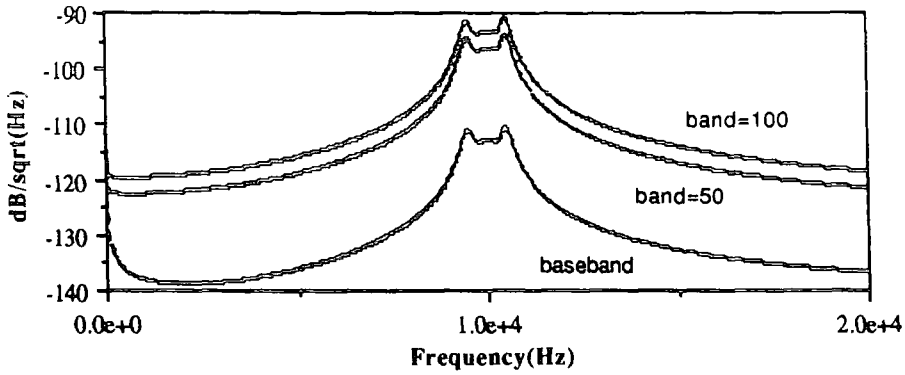

Figure 2. Noise behaviour of sixth-order bandpass SC filter with folding back effects

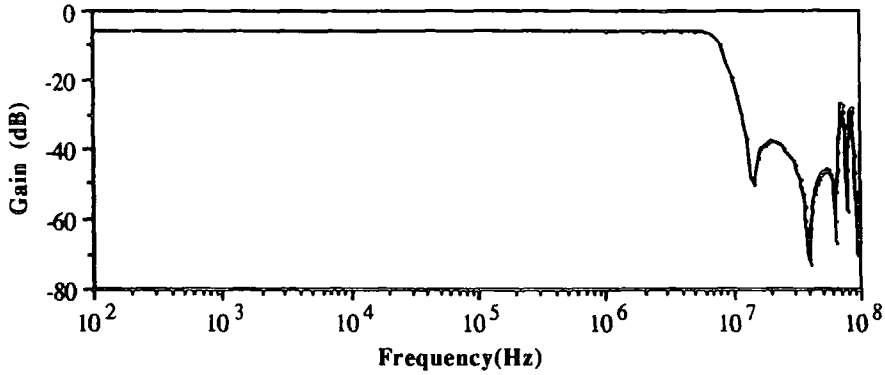

Figure 3. Frequency response of 3rd order elliptic ladder SI circuit

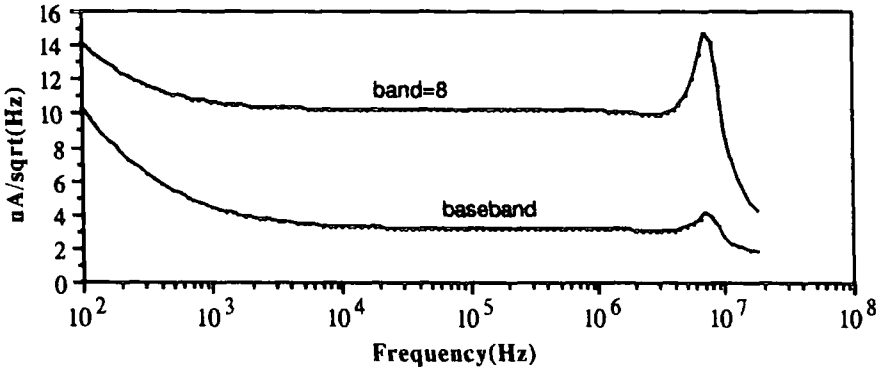

Figure 4. Noise behaviour of 3rd order elliptic ladder SI circuit

6. Communication Circuit Design

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An Adaptive Electronic Circulator for Use in Telephones

R. P. LODGE AND J. I. SEWELL, MEMBER, IEEE

***Abstract*—A design for an adaptive three-port electronic circulator is presented. The circuit has particular use in telephone work and this model can provide isolation when the terminating load varies over the range 200 Ω–1 kΩ. The whole circuit is realizable in microelectronic form.**

INTRODUCTION

THE USE of electronic circulators in telephone systems has been suggested recently [1] and an even more extensive and ambitious scheme has been outlined [2]. The great virtue of the audio circulator is that the design is simple [3], it is easily extendable to an n-port version, and a large variety of combinations are possible [4]. Thus the circulator can be used for all the isolation problems encountered in telephone systems and also in the various filtering requirements [5].

It has been demonstrated [1] that line matching can be achieved in a most accurate way. However this refers only to the static case and will not apply to dynamic matching where there can be changes in line impedance with changing length, quality of line, and terminations. Some form of adaptive circulator is obviously needed to overcome such difficulties.

ADAPTIVE CIRCULATORS

The principles are most easily observed by considering a three-port circulator, which is the lowest order of practical use in telephone work. In a typical handset application [2], the microphone is connected to port-1, the subscribers line to port-2, and the earphone is fed with a signal proportional to the difference of the signals at these two ports. The circulator provides the required isolation on transmit and receive. In the transmit mode, the difference signal will produce the side-tone and, with ideal matching, uniform speech levels are ensured. If the circulator impedance

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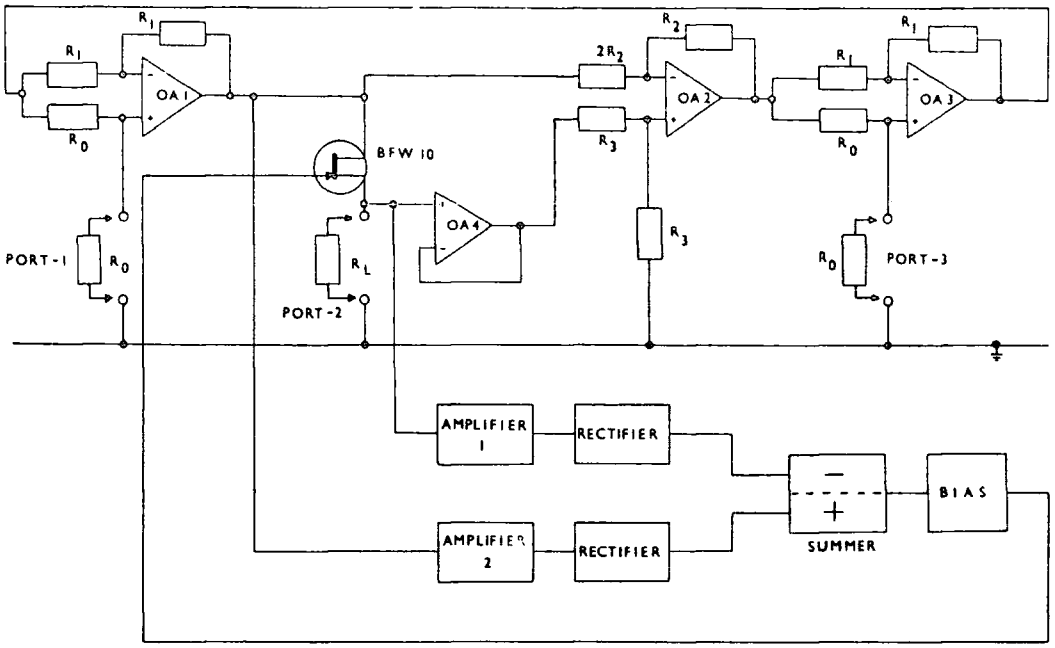

Fig. 1. Adaptive circulator realization.

at port-2 perfectly matches the line, then in the transmit mode there is theoretically zero voltage at port-3, and in the receive mode no signal will appear at port-1. Any mismatch with the line will produce a finite rejection port voltage and it might be assumed that this could be used as a feedback signal to control a voltage variable resistor (VVR) defining the circulation impedance at port-2. However a phase-sensitive rectifier would be required to derive a correction signal, which will vary the impedance in the appropriate direction.

Fig. 1 shows a better alternative circuit for an adaptive circulator. The circulator is balanced when ports-1 and -3 are terminated in R_0 and when the channel resistance of the FET is equal to the load at port-2. If, under these conditions, the input voltage at port-1 is V and there are no other input signals, the output from operational amplifier (OA) 1 is also V. The port-2 voltage is then $V/2$. The differential amplifier formed by OA 2 thus has two equal inputs and, therefore, no signal will appear at port-3. For unbalanced conditions, when the FET channel resistance and the load are different, there is an output from OA 2 and thus the port-3 voltage will be finite. With the gain of amplifier 1 double the gain of amplifier 2, a feedback signal to the FET gate is derived by comparing the actual port-2 voltage with the desired value. It is usually necessary to provide some bias, in series with the correction signal, to ensure that the FET channel resistance is centered on the mean load resistance. As the r_{ds} characteristic is not entirely linear, it is usually necessary to apply local feedback to obtain a wider linear range. For good third-port rejection, the gain round the correction feedback loop should be as high as possible. However, this is restricted by the possibility of oscillation, although this may be removed by some form of damping.

When an input is applied to the second port, simulating an incoming line signal, the feedback mechanism is different. Assuming that there is no input signal at port-1, there is no signal at the inverting input of OA 2. The input voltage divides between the FET and the load resistance, thus the output of the summing amplifier goes negative to a great extent. With a high loop gain and small damping factor, the FET channel becomes cut off and all the signal is passed to OA 4. There will now be isolation at port-1 and an earphone fed with the difference of the port-1 and -2 signals will receive the full incoming one. However this leads to two problems: the adaptive feature is no longer operative as the line feeds the earphone circuit direct; and the circulator suffers from voice switching. A fairly convenient method of overcoming these two difficulties is to provide feedback of the signal at port-3 to the inverting input of OA 1, isolation in the path is required to prevent any feedforward. In the transmit mode, there is no signal at port-3 and operation is as previously described. On receiving an incoming signal at port-2, the extra feedback provides an input for amplifier 2 which will ensure that the FET will not now be cut off. Voice switching is eliminated and the adaptive property retained.

PRACTICAL CIRCUIT

A circuit employing the common 741 amplifier as the basic amplifier unit was constructed. The rectifiers were simply a single diode with a smoothing capacitor; some

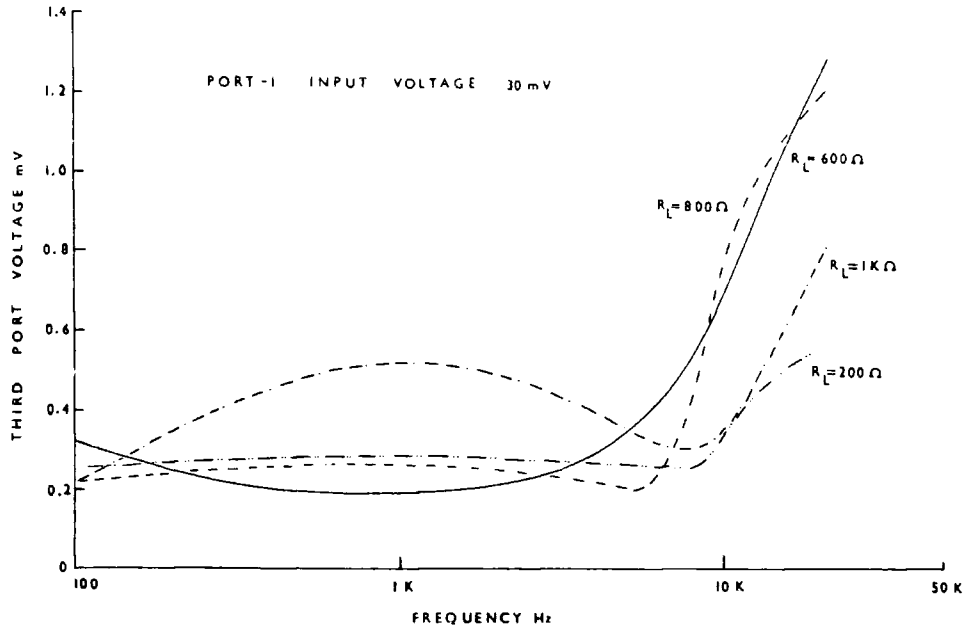

Fig. 2. Rejection characteristics for input to port-1.

buffering with a voltage follower may prove necessary before the summer, again a conventional amplifier circuit. The smoothing capacitors also furnish the required damping and 0.22 μF provides a satisfactory response.

The $r_{ds(ON)}$ value of the FET selected (BFW 10) was in the region of 200 Ω. The initial matching range was chosen as 200–1000 Ω. When the load resistance has some value R_L, the difference voltage generated is

$$V_d = \left| \frac{V_{in}}{2} - \frac{V_{in}R_L}{R_L + r_{ds(ON)}'} \right|$$

where $r_{ds(ON)}'$ is the actual drain-source resistance apparent in the circuit and includes any alteration induced by local feedback; and V_{in} is the input voltage at port-1. For the signal levels ensuring linear operation of this particular circuit, an input voltage of about 30 mV resulted in a maximum value of V_d as 5 mV. The gate-source voltage required for a channel resistance of 1000 Ω for the BFW 10 is −2.1 V, thus a differential gain of about 400 is required. This is realized by the amplifiers preceding the rectifiers, which have adjustable gains to compensate for differing voltage drops across the diodes. An added feature is that these amplifiers also prevent loading of the FET and the line.

Fig. 2 shows some typical response curves, when the circuit was fed with 30 mV at port-1 and the rejection voltage at port-3 is measured. The bias on the FET gate is set to match a 600-Ω load at port-2. It is apparent that within a 5-kHz bandwidth, the rejection is best for loads in the region about 600 Ω. A point of interest is to note that there are wider rejection bands for the greater load deviations; this is due to better controllability of the larger error signals present in these circumstances. Nevertheless the circuit will provide third-port rejections of between 30–40 dB for variations in port-2 terminations over the range 200–1000 Ω, for a 5-kHz band. The isolation characteristics of the circulator when fed with a signal at port-2 and subjected to load variations at port-2 are shown in Fig. 3. The rejection is greater than 44 dB over a 20-kHz bandwidth, there being negligible effect due to load change from 600 Ω until approximately 1 kΩ is reached. This can be expected since the third stage, which is purely resistive and accurately adjusted, is responsible for producing this degree of isolation.

It is therefore possible to conclude that adaptive electronic circulators are quite suitable for telephone usage. Isolation is possible over a good bandwidth, and with more careful design, considering the time constants involved in rectification, FET nonlinearity, and feedback loop gain, together with better amplifiers, a superior performance could be ensured. One disadvantage of the present circuit is the need for low input voltages, as is common with most VVR applications of FET's, since the signal inevitably produces some modulation of the channel resistance. This can be overcome by employing more elaborate gate-drain feedback circuits and using FET's especially designed for VVR work.

The voice-switching problem of the simple circuit is overcome by adding an extra feedback path. The circulator can be used to match complex impedances, but obviously the variable correcting circuits will be more sophisticated.

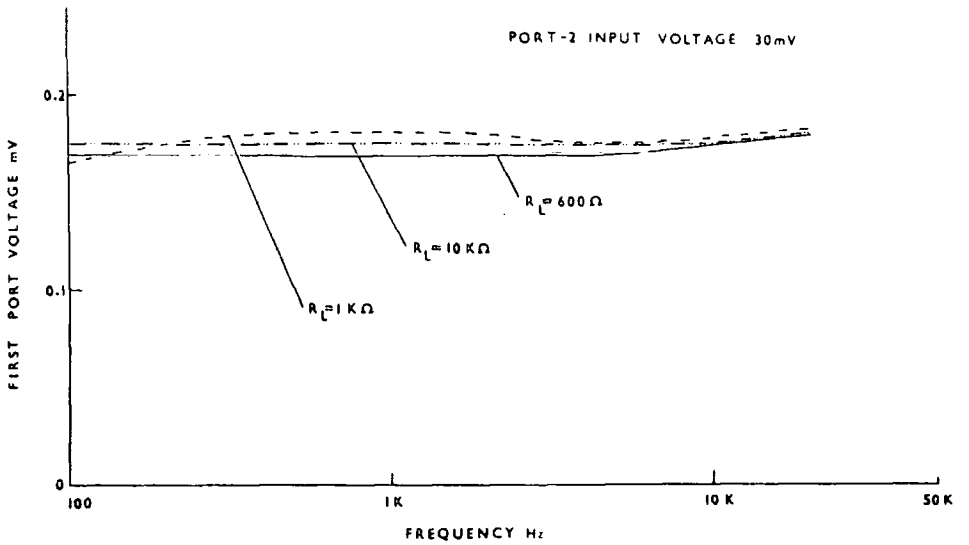

Fig. 3. Rejection characteristics for input to port-2.

The operating conditions considered here would only correspond to unbalanced line working in a telephone system. But with duplication of the circulators [2] normal operation is easily accomplished. An added advantage is that the whole circulator circuit can easily be realized in microelectronic form.

ACKNOWLEDGMENT

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PAPER 23

Concise Papers

An Improved Adaptive Electronic Circulator for Telephone Applications

H. GAZIOGLU, D. A. HOMER, AND J. I. SEWELL, MEMBER, IEEE

Abstract—A previous attempt at realizing an adaptive circulator for telephone applications suffered from limitations due to voice switching problems, resistive part matching only, and some difficulties with adaptive operation for broadband signals. The use of pilot tones enables the circuit to be free from voice switching problems and to accomplish a close impedance match with that of a telephone line. Analysis of the circuit in an adaptive hybrid configuration produces the theoretical bounds on performance. Experimental results display the performance characteristics of the adaptive circuits and various other hybrid circuits on a selection of subscriber lines with a range of terminations.

INTRODUCTION

There is an increasing interest in the inclusion of a variety of electronic features in the telephone subscriber's loop. Apart from dialing facilities and subscriber carrier systems, studies concerned with circuits providing amplification [1, 2], active hybrids [2, 3, 4] and adaptive hybrids [5, 6, 7] are being actively pursued. The previous attempts at realizing adaptive hybrids had a number of limitations, some providing the adaptive feature only at certain frequencies [5] or over a limited frequency band [7]. The adaptive circulator [6] provided only resistive part matching and although some precautions against voice switching were taken, these were not entirely satisfactory; the adaptive operation of the circuit with broadband signals also presented problems.

The possibilities of adaptively matching line impedance changes in the subscriber equipment, at the interface with line amplifiers, or at the 4-wire to 2-wire transition points are assuming increasing importance. The line characteristic is vulnerable to the influence of change in terminations and cable parameters affected by physical means due to either man or nature. The mismatch against static balancing impairs sidetone rejection and reflection characteristics resulting in problems of no small significance.

A further requirement of future developments is to provide isolation and matching characteristics by circuits suitable for mass production by integrated circuit means.

THE ADAPTIVE CIRCULATOR

The basic 3-port circulator is well known [8] and the replacement of one section by an adaptive one has been reported [6]. Attention here will be confined to a different adaptive section which may be used in conjunction with standard sections to form a fully adaptive circulator.

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Consider Fig. 1 and note that the controlling signals are developed from a separate pilot tone and that the impedance measuring and adjustment bridge can have both pilot, transmit and receive voice signals present in one arm simultaneously. The circulator section automatically removes the pilot signal from the isolation path and the voice frequencies are filtered out in the control path. The line input impedance is simulated by an RC circuit, Fig. 2; a three element parallel/series circuit is considered initially, but results are shown for a five element network for more general application. The three element network will suffice for short lines, but the more complex network is necessary for the longer subscriber lines. The possible combinations of length and diameter of cables on subscriber lines is almost infinite. For British Post Office lines, the three networks given in Fig. 2 represent optimum fits to the frequency responses of average overall lengths taken in three groups and typical combinations of Cu cable of differing diameters; a line termination of 600 R was used. Experimentation will show that these networks provide a suitable median from which the adaptive feature can work.

With the three element circuit it is obvious that a 3-term controller could be used. Analysis of such a network demonstrates that the high frequency response is a direct function of the series resistance, whereas the low frequency response is dependent upon both resistances. The break points of the simulated line characteristic can be directly controlled by varying the capacitance value. Hence a control loop employing a pilot tone well above the voice band, say 10 kHz can be used to adjust the high frequency response and another using a pilot tone below the voice band, say 12 Hz, can adjust the low frequency response. A further pilot tone just outside the band, say 5 kHz, can be used to control the capacitance value. However, investigation shows that in practice the high frequency asymptote is of little significance, because the major effect is out of band and anyway this varies little from line to line and with various terminations. Any influence on the upper break frequency can be covered by capacitance control The major change comes at the low frequency end, manifesting itself as quite substantial changes in loop resistance, lower break frequency and slope of the impedance characteristic. For simplicity of analysis a single term controller, operating from a 12 Hz pilot will be investigated in detail. A dual pilot tone circuit, with adaptive parallel R and C elements is of more general application for broadband signals, however extension of the theory is straightforward.

With reference to Fig. 1, for the purposes of analysis, it is not necessary to consider the pilot tone signal but only the components of the transmitted signal E and the received signal V. Assuming ideal operational amplifiers, the output signal of the circulator section is given by:

$$E_o' = \frac{4Z_1 V}{Z_0 + Z_1} + 2E\left[\frac{Z_0 - Z_1}{Z_0 + Z_1}\right]. \tag{1}$$

Now E corresponds to the port-1 voltage, V to the port-2 voltage, the port-3 voltage will be $E_o = E_o'/2$, hence:

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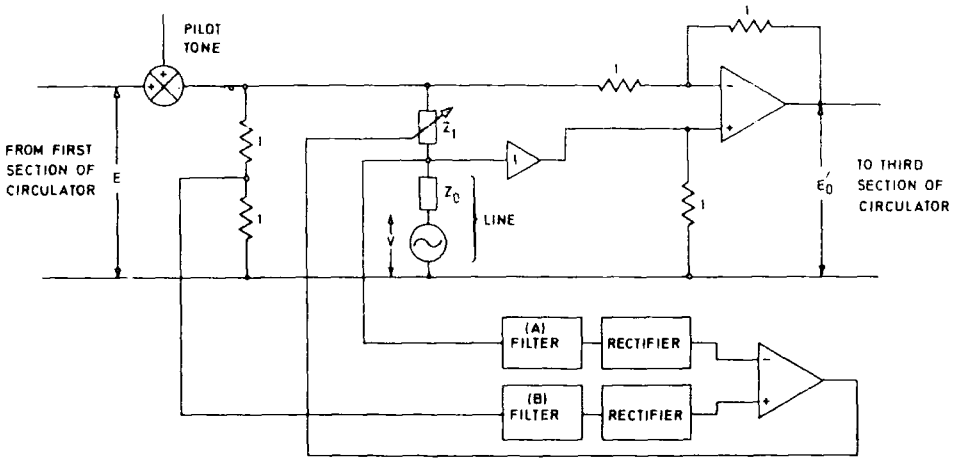

Fig. 1 The adaptive section of a single pilot tone circulator.

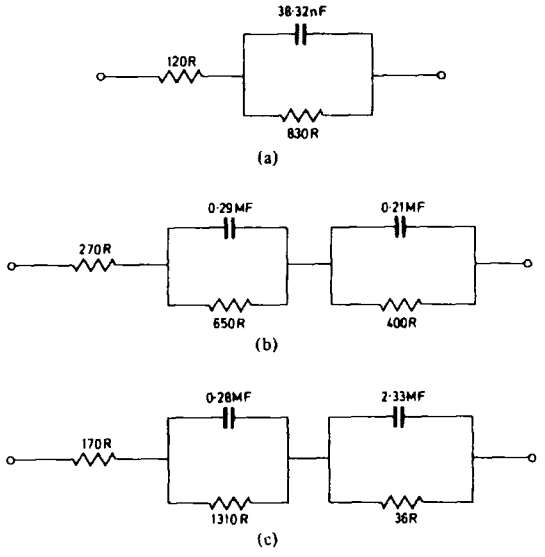

Fig. 2 Optimum balance networks for: (a) 1 km line (mixed diameter Cu) (b) 4 km line (mixed diameter Cu) (c) 7 km line (mixed diameter Cu)

$$E_o = \frac{2Z_1 V}{Z_0 + Z_1} + E\left[\frac{Z_0 - Z_1}{Z_0 + Z_1}\right] \tag{2}$$

$$= E_{oT} + E_{oR}$$

which consists of a transmitted component E_{oT} and a component to be rejected E_{oR}. Set $\alpha = Z_0/Z_1$ then the transfer and rejection ratios become respectively

$$A_T = \frac{E_{oT}}{V} = \frac{2}{\alpha + 1} \tag{3}$$

$$A_R = \frac{E_{oR}}{E} = \frac{\alpha - 1}{\alpha + 1}. \tag{4}$$

Note that the condition for perfect isolation is $Z_0 = Z_1$, and the outgoing signal is completely rejected at port-3. $A_T = 1$ and the incoming signal at port-2 is transferred to port-3 with unity gain.

Substitution of $\alpha = X + jY$ into the expression for the magnitude of equation (3) for some constant value $A_T = K$ gives

$$(X + 1)^2 + Y^2 = \left[\frac{2}{K}\right]^2. \tag{5}$$

Equation (5) represents a circle of center $(-1, 0)$ and radius $2/K$. Similarly for some constant value of $1/A_R = R$ the expression for the magnitude of equation (4) yields

$$\left[X - \frac{R^2 + 1}{R^2 - 1}\right]^2 + Y^2 = \left[\frac{2R}{R^2 - 1}\right]^2 \tag{6}$$

which represents a circle in the XY plane with center $[(R^2 + 1)/(R^2 - 1), 0]$ and radius $2R/(R^2 - 1)$. Constant transfer ratio and rejection ratio circles can be plotted as shown in Fig. 3. As can be seen infinite rejection is obtained at the point $1 + j0$ and this corresponds to the condition $Z_0 = Z_1$. The rejection rapidly decreases as the ratio changes from unity, although the transfer gain is relatively insensitive to the change and remains close to 0 dB.

One of the major roles of this circulator is as an adaptive hybrid in the telephone set, and most of the experimentation has been carried out with that area of operation in mind. If the circulator is to be used in the mode already indicated [6], with the mouthpiece connected to port-1 and the earpiece fed with a signal from across ports-1 and -2 giving a defined sidetone injection, then the transmission properties of the adaptive section are of little consequence as the third section will provide complete isolation anyway. Another connection of the circulator is with the mouthpiece again across port-1, the line across port-2 and the earpiece across port-3. Now an incoming signal is transmitted through the adaptive section and both rejection and transmission characteristics of the section are of

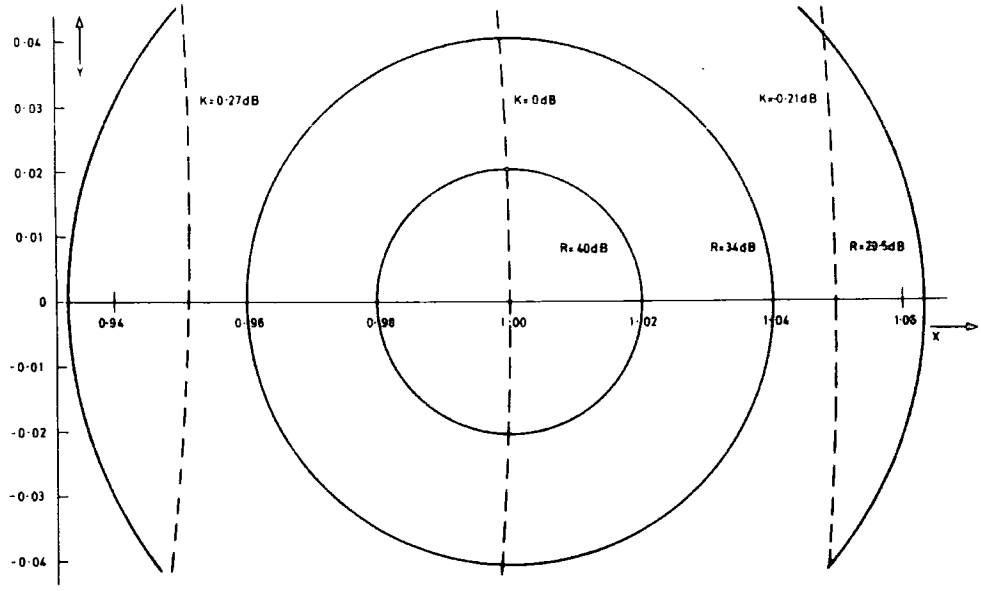

Fig. 3 Constant rejection and transfer loci.

significance. A performance figure can be defined as:

$$PF = \left| \frac{A_T}{A_R} \right| = \frac{2}{|\alpha - 1|} . \tag{7}$$

Substituting $\alpha = X + jY$ and considering constant gain loci gives the equation $(X - 1)^2 + Y^2 = [2/KR]^2$ which represents a circle with center $(+1, 0)$ and radius $2/KR$. A set of these loci can be plotted. It is therefore possible to determine for a specific rejection or performance figure, the accuracy of amplitude and phase match required by the adaptive section. In practice, the rejection and performance figures are approximately the same.

For a rejection of 40 dB over the whole telephone band the conditions are:

$$\begin{aligned} 0.98 &\leqslant |\alpha| \leqslant 1.02 \\ -1.15^\circ &\leqslant \text{Arg}\,\alpha \leqslant 1.15^\circ \end{aligned} \tag{8}$$

which imply that the impendance match should be within ±2% for magnitude and ±1.15° for phase. Less stringent requirements exist for lower rejection specifications; the conditions for 26 dB rejection are:

$$\begin{aligned} 0.91 &\leqslant |\alpha| \leqslant 1.105 \\ -5.7^\circ &\leqslant \text{Arg}\,\alpha \leqslant +5.7^\circ \end{aligned}$$

a magnitude match of about ±9.7% and phase match ±5.7°.

The ideal performance of the circuit was examined on a computer. A program to simulate the frequency responses of lines consisting of a variety of lengths of mixed diameter cables with a range of terminations was written, and the results produced agree with the measured ones taken from artificial lines constructed to British Post Office standards. This program was incorporated into others which simulate the behavior of the single and dual pilot tone adaptive circulators. The results from these programs indicate the possibility of approaching the above theoretical limits.

THE PRACTICAL CIRCUIT

Fig. 4 shows the complete circuit diagram of the dual pilot tone adaptive circulator; all amplifiers are of the 741 operational type. Ports-1 and -3 of the circulator are given 1 kΩ loads for the test purposes, normal telephone connections have already been discussed. The two pilot tones are of 100 mV in amplitude; the lower tone is set at 12 Hz and the upper at 5 kHz. Although the choice of these frequencies outside the telephone band is reasonably random, some restrictions may be imposed by the outside system. For instance, there may be difficulties with the low frequency pilot tone when encountering the AC coupling found in much of the telephone plant, and it might be necessary to restrict the application to metallic facilities. With the high frequency pilot tone the evolving use of loop electronics must be recognized and especially with subscriber carrier systems the possibility of interference should be considered. Filtering of the 12 Hz tone for the low frequency control circuit is achieved by a 4th order low-pass Butterworth filter of the Sallen-Key type. Rectifiers in both control loops are of the active precision type. Because of the location of the 5 kHz pilot tone with respect to the upper edge of the voice band it is necessary to employ a 5th order high-pass elliptic filter in the higher frequency control circuit. The choice of matching networks for short, medium and long subscriber lines is provided via a switch. Quite good results are obtainable, however, by merely using the medium length matching network for all applications. Resistance variation is obtained from the BFW 10 FET with shunt feedback to improve linearity. Capacitance variation is provided by varying the gain of a Miller circuit, again using a FET. Some care has to be exercised in controlling the range of bias on this FET, since the circuit

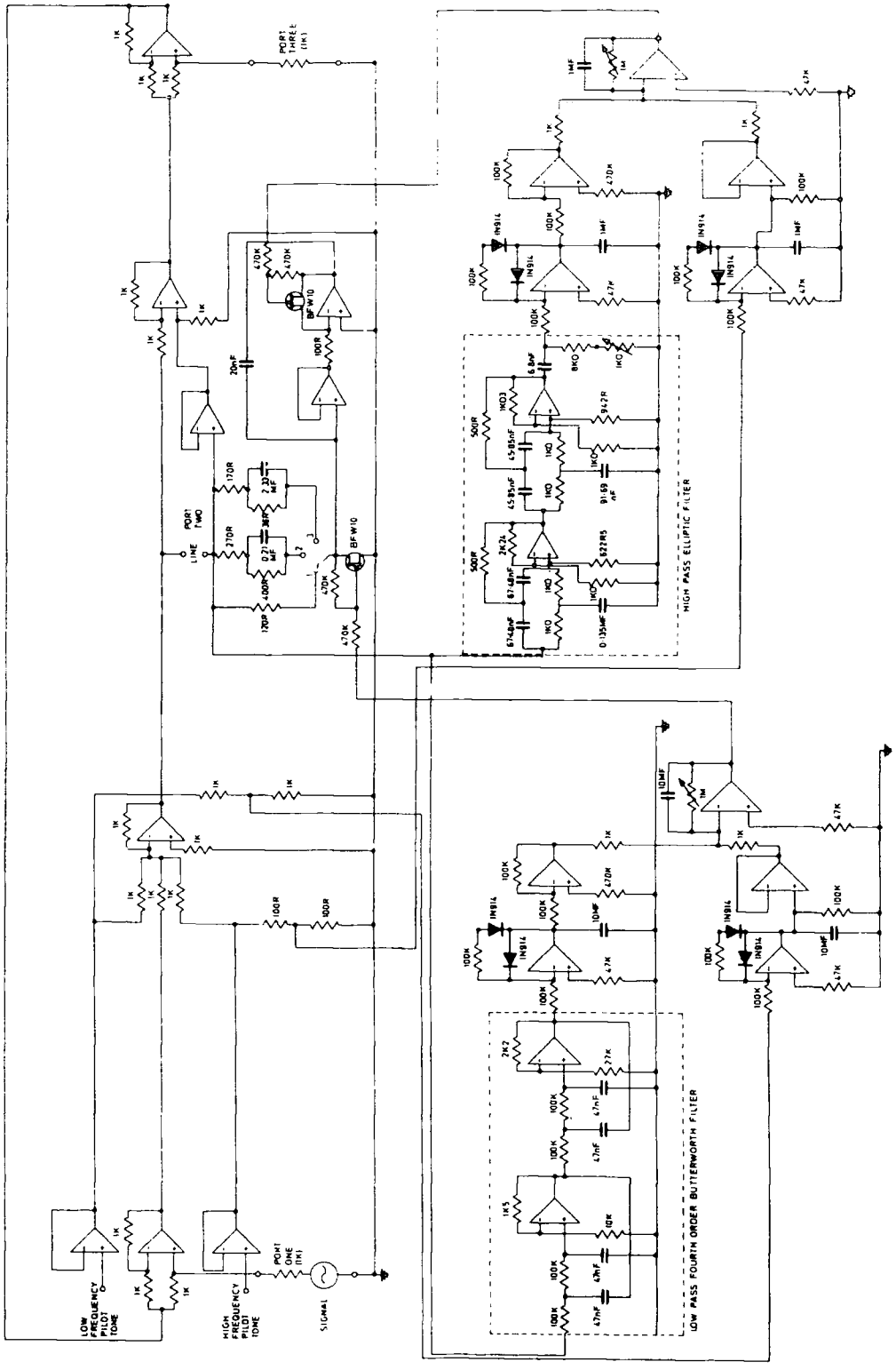

Fig. 4 Circuit diagram of dual pilot tone adaptive circulator.

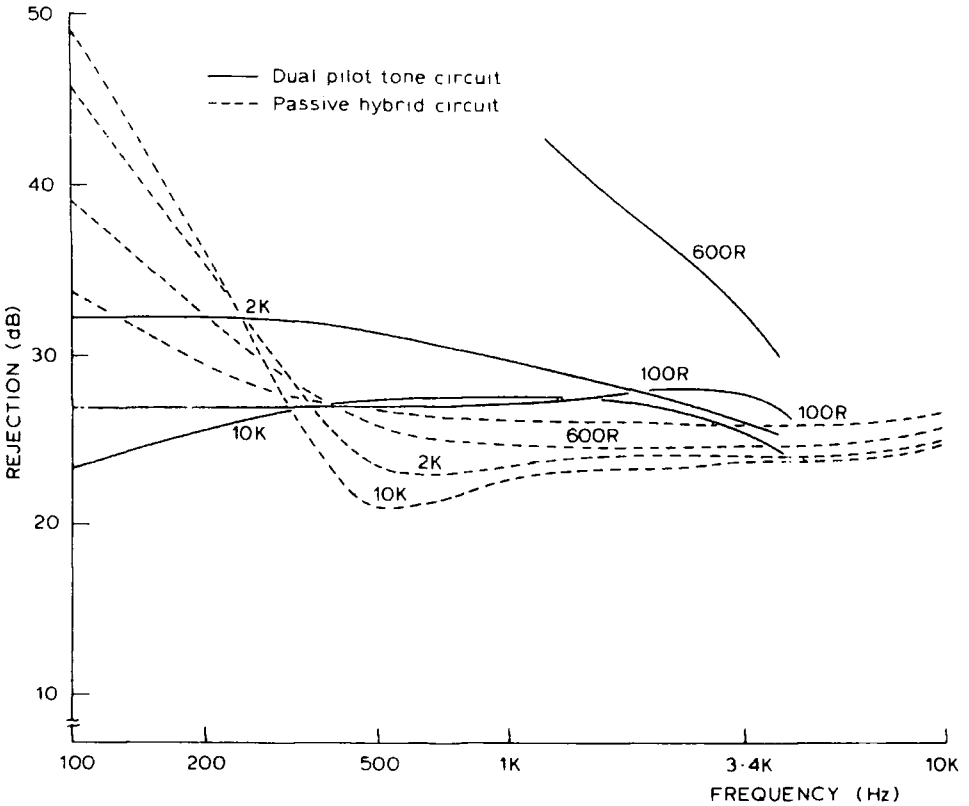

Fig. 5 Adaptive circulator and passive hybrid responses for 1 km mixed line: 0.5 km 0.4 mm Cu + 0.5 km 0.32 mm Cu; terminations as shown.

inevitably produces a variable resistance in parallel with a variable capacitance and this resistance value decreases with negative bias.

Practical measurements were taken using an input signal of 100 mV and results for the rejection between ports-1 and -3 in the dual tone adaptive circulator circuit are compared with the performances of some other possible hybrid circuits in Figs. 5-7. The graphs in Fig. 5 show measured responses of the dual tone adaptive circulator and of the conventional passive hybrid of the BPO 700 type telephone set, under typical short line conditions for a range of terminations. Over the normal telephone band and average terminations improvements in rejection are observed. Fig. 6 demonstrates the improvement due to the addition of the adaptive feature to the circulator when working on a medium length line. The results for the non-adaptive circulator with the passive *RC* matching circuit are computed. There is a moderate improvement for the 600 R termination, to be expected since the nominal components of the passive matching network are derived for a median 4 km line of mixed diameter Cu sections with a 600 R termination. Quite marked improvements are apparent as the terminations are varied, displaying the activity of the adaptive feature. For the longer lines the line impedance is much higher and the FET's are increasingly pressed into a non-linear VVR operating mode when the control is not as linear and fine. The measured responses displayed in Fig. 7 also snow the poorer performance of the single, low frequency, pilot tone model. In practice, operating conditions can occur that cause line terminations to appear largely reactive, this results in some of the rejection curves demonstrating rapidly changing characteristics. However, the results obtained for the range of resistance terminations used, quite adequately encompass the worst performances experienced with both capacitive and inductive terminations. It is therefore reasonable to use these responses as a good indicator of the average performance with practical terminations. The best overall performance achieved from a dual tone circuit was an average in excess of 34 dB rejection over the whole voice band for a line impedance change of 3:1. The characteristics on the whole deteriorate at higher frequencies, but since the out of band behavior of the high frequency asymptote has been ignored, this trend is to be expected. Experiments with the upper pilot tone at 10 kHz indicate a slight improvement in performance figures and the circuit also has the advantage of relaxing the requirements of the high-pass filter for this tone, a feature of some practical importance as a 3rd order elliptic filter will suffice.

The circuit has been completed by the addition of oscillators to provide the pilot tones; these oscillators were of the Wien-bridge type. It is an advantage if circuits for inclusion in telephone sets do not require an independent power source. Experiments in deriving ±15 V supplies from DC power delivered down the line from a central supply indicate that such circuitry could be powered from a local exchange. Some studies on the reduction of power consumption have indicated

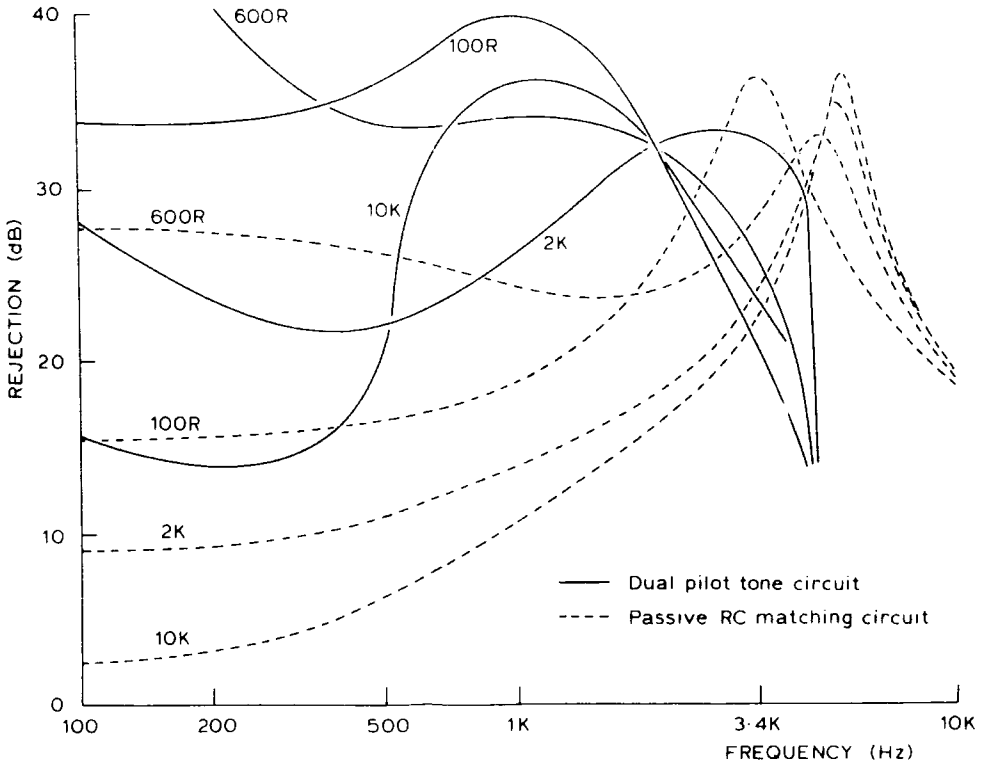

Fig. 6 Adaptive and non-adaptive circulator responses for 5 km mixed line: 1 km 0.4 mm Cu + 2 km 0.5 mm Cu + 2 km 0.63 mm Cu; terminations as shown.

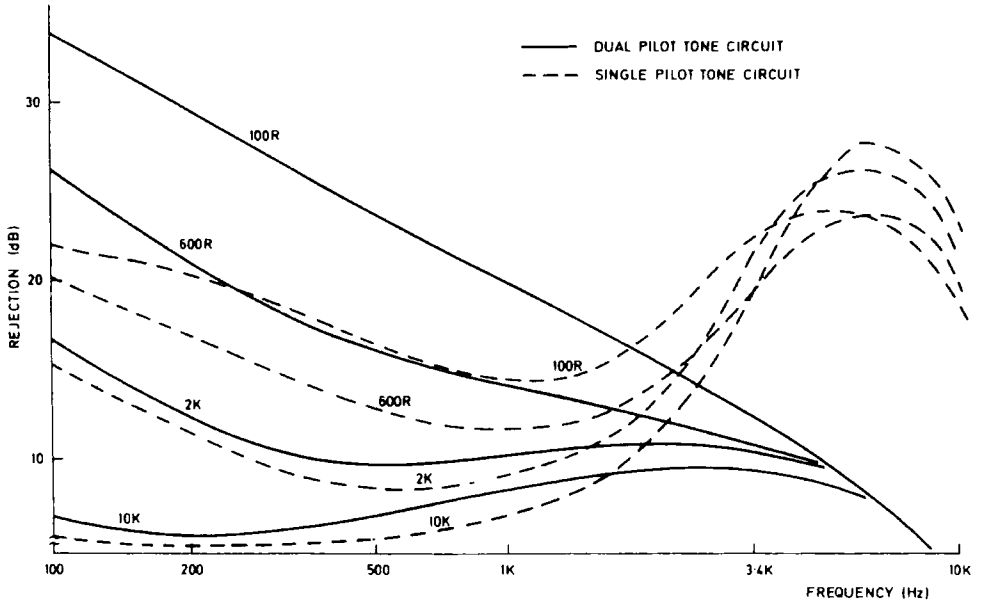

Fig. 7 Adaptive circulator responses for 9 km mixed line: 1 km 0.32 mm Cu + 1 km 0.4 mm Cu + 2 km 0.5 mm Cu + 3 km 0.63 mm Cu + 1 km 0.9 mm Cu + 1 km 0.5 mm Al; terminations as shown.

that circuit simplifications are possible. In actual fact, the circulator loop can be broken and the third stage eliminated without any reduction in the performance factor.

The overall results obtained indicate that the realization of an adaptive hybrid for telephone applications with integrated circuit technology is quite feasible. The theoretical conditions for very high rejection ratios, of the order of 40 dB, are quite strict. For applications requiring such responses under wide variations of line conditions, it will be necessary to employ higher grade operational amplifiers in some positions in the circuit. Detailed analysis of the control system reveals a standing error responsible for about 3 dB loss in rejection. A redesign should be possible here. A more linear and wider range of variation of resistance and capacitance components may be afforded by techniques employing multipliers, with very little increase in area on an integrated circuit.

ACKNOWLEDGMENTS

The authors would like to thank all the referees for help and advice, in particular the suggested comparisons shown in Fig. 6 which aid the demonstration of the adaptive feature.

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Some Effects on Channel Occupancy of Limiting the Number of Available Servers in Small Cell Mobile Radio Systems Using Dynamic Channel Assignment

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Abstract—The performance of large scale multicell mobile radio systems using dynamic channel assignment and having limitations on the number of servers available in each coverage cell was investigated by computer simulation. At low system blocking the traffic carried is determined solely by the server limitations while at higher blocking the traffic carried is determined by channel limitations.

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Performance characteristics have been investigated for large scale mobile radio systems using dynamic channel assignment.[1-9] These systems utilize small radio coverage cells and reuse channels within a metropolitan area. In dynamic channel assignment systems, channels are assigned to serve calls on the basis of instantaneous demand in the system subject only to a prescribed channel reuse constraint, i.e., any channel may be assigned to any cell in the system provided that the channel is not being used within a specified number of cells from that cell at the time that the channel assignment is made. The specified number of cells required between cells that may use the same channel is called the reuse interval. Earlier studies[1-4] assumed that sufficient servers, i.e., radio equipment, were available in each cell to handle any statistical fluctuations in offered traffic; the only restriction on the traffic carrying ability of the system was on the number of radio channels. This permitted the evaluation of the channel assignment algorithms independent of server constraints. It was observed that the number of servers required was seldom greater than the average number of channels available per cell and never greater than twice that average number.[4] A complete description of these earlier studies is included in references 1, 2, and 9. The purpose of this correspondence is to indicate the performance limitations imposed on these systems by limiting the number of servers in each coverage cell.

The system simulated is described in detail in Reference 1. It consisted of a set of square radio coverage areas (cells) arranged to completely cover a large square area. It was assumed that channels could be simultaneously used in every fourth cell (reuse interval of 4). The total number of duplex radio channels allotted to this dynamic channel assignment/reassignment system was 160. This provided 10 channels on the average in each cell. Of the 160 channels, 128 were assigned on a fixed basis with 8 fixed channels per cell. Fixed assigned channels could be used only in the specified cells to which they were allocated. The 32 remaining channels were assigned dynamically and could be used in any cell in the system depending upon instantaneous demand and subject only to the constraints of channel reuse and available servers. The system maximized the number of calls occupying fixed channels and used the dynamic channels only to handle statistical fluctuations in offered traffic. Calls in progress were transferred from dynamic channels to fixed channels whenever possible as described in Reference 1. Call-attempts were generated in the simulation as a Poisson process in time with a specified fixed call-attempt rate in each cell. Call attempts were uniformly distributed in space and the attempts in any given cell were independent of those in all other cells. Attempts that were assigned a channel remained "on" for call durations that were distributed exponentially and had a mean duration of 98 seconds, In this simulation, vehicles making calls were identifiable entities whose locations and movements were stored in the computer. Active calls crossing cell boundaries were treated as new calls in the new cell as described in Reference 1. Data were obtained by counting and storing the number of actual events which occurred as the simulation ran.

The curves in Figure 1 show directly the relationship between the traffic carried (expressed as the average number of

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7. Analysis and Design of Sigma-Delta Modulator Systems

PAPER 46

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A METHOD FOR THE EVALUATION OF MULTIRATE SIGMA-DELTA SYSTEMS

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Abstract - Simulation techniques for sigma-delta based systems are discussed. An extension to the next state simulation method for block diagrams is presented which allows efficient handling of multirate systems. This is achieved by the additional definition of clock dependent inputs for each element to define how the element behaves in a multirate situation.

I. INTRODUCTION

Relatively little has appeared in the literature concerning the simulation of sigma-delta converters. It is widely realised that simulation using traditional analogue simulation tools is not feasible due to the prohibitive CPU time required. Most researchers have managed by using purpose written computer programs which model the difference equations representing the specific sigma delta modulator topology being investigated. The program described here allows the user to describe the structure of complete sigma-delta modulation systems which may contain several sigma-delta ADCs, DACs, sigma-delta based multipliers along with the associated filters in a form similar to a SPICE deck, but at a signal flow graph level [1].

The circuit is described at a system level and consists of a network of gains, delays, quantisers, filters etc. The algorithm then reduces the network description to a list of function calls which can be executed repeatedly to simulate the action of the circuit. This is almost as fast as a purpose written program. Alternatively, the algorithm could be made to produce a C program file for compilation by the computer system's C compiler. The resultant program would be almost indistinguishable from a well written, purpose written program, but would be much quicker to create and easier to modify. Sigma-delta systems are usually multirate and this is handled efficiently.

Many non-idealities can be included, such as finite integrator gain and saturation, linear and nonlinear settling (slew limiting), comparator hysteresis, dc offsets, quantiser level spacing etc. can all be modelled [2]. The method is compatible with (can include) table based techniques [3].

To be most useful, a simulation tool for sigma-delta modulation systems must allow many parameters to be swept through a range of values, eg.: DC input level, integrator offsets, amplitude and frequency of input signal (to determine the variation in SNR), number of quantisation levels or the word length of the digital filters, gain values (to determine sensitivity due to capacitor mismatch, integrator gain and bandwidth). There is also a variety of analyses which may be performed on various signals in the system (eg. the raw output and the decimated output). A flexible approach has been adopted whereby all the signal sources, and all the analysis features (FFT, power spectral estimation, least squares function fitting) are all incorporated as network elements and treated in the same way as simple elements such as gains, delays and quantisers. Most element parameters (such as the gain of elements, or the number of levels in a quantiser) are taken from inputs, which are usually replaced by a constant, but which can be connected to a variable source to allow parameter sweeps.

In the block simulator BLOSIM [4], blocks are interconnected by means of first-in-first-out (FIFO) buffers. This makes sample rate changes very easy to implement. However there is considerable overhead in the buffer management routines which limits the application of this technique to the simulation of sigma-delta systems. Subsequent research has been directed in the field of program compilers for multiple processor DSP [5]. The sample rates in a sigma-delta modulator system are well defined before the simulation commences and are constant (ie. they are synchronous). This fact has been used to devise a block diagram simulation method which retains many of the advantages of BLOSIM (generality, ease of use, hierarchical definition of blocks, block libraries, consistency checks etc.) but handles synchronous multirate circuits more efficiently.

The program executes in the four stages shown in Fig 1. The network description file is first read and comments stripped out and macro definitions expanded. The resulting network of elements is then converted to an unordered list of operations. Each operation is represented by a data structure containing the function to be executed, the input and output nodes, dependent and clock dependent nodes, values of any parameters and any other information required. Lists of pointers to these operations are then created by a scheduler which ensures that the operations are executed in a valid order, and that only nodes which need to be recalculated are actually recalculated in multirate systems. Running the simulation then simply involves executing the operations in the specified order.

II. REPRESENTATION OF MULTIRATE SYSTEMS

Three node types are defined: an *ordinary* node value (eg. the input and outputs of gains, delays and quantisers), a *signal* node or list of values (eg. for complete signals, FFT records, FFT window functions etc.) and a *file* node type (eg. for reading in input signals, printing out results, communicating with other processes such as externally defined elements or graph plotting programs). Evaluating a node involves executing all the operations with outputs connected to that node.

Each *element* as entered by the user, is represented in the computer by a number of *operations*. A single operation may have many inputs (the *dependent* nodes) and a single output, all of which may be simple nodal values, complete signals, or files

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(Fig. 2). The operation also has a number of *clock*-dependent nodal inputs, which determine how the operation will behave in multirate systems. Elements with several outputs are realised by several operations.

Three rules govern the behaviour of all the operations in a multirate system:

1. A *node* will only be calculated if any operation contributing to that node is *known* to be active.
2. An *operation* will only be active if at least one of its clock dependent inputs is connected to a node known to have changed.
3. To allow for rate changes, it is possible to force a node to be either active or not by applying a forced clock to the node. This rule overrides the two above.

The rule for operation ordering is based on the standard precedence rule:

4 a An *operation* cannot be evaluated until all it's inputs (the dependent nodes) are known.

4 b A *node* cannot be recalculated until all the active operations directly contributing to that node satisfy Rule 4a.

Scheduling Algorithm

The scheduling must be done in two passes. The first pass determines which nodes change and therefore must be recalculated, and the second pass then places only the operations which are active into a computable order.

- *Pass One*

```
All nodes are unknown.
Apply rule 3.  This will make some nodes
     known (either to have changed or not)
     and provides a starting point for the
     next stage.
Repeatedly apply rules 1 and 2 to determine
     which other nodes are known to be
     active.
Any nodes which cannot be determined are
     deemed inactive.
```

Now all nodes are known to be either active or not.

- *Pass Two*

```
All nodes which are not active are known
     (because they have not changed).  All
     others are not yet known.
Repeatedly try to evaluate every node.  If a
     node can be evaluated (Rule 4) then add
     to the list of pointers to operations
     all the operations satisfying Rule 2.
     A clear node operation must be entered
     automatically ahead of these.  This
     node is now known.
If any nodes can not be determined, then the
     network contains either a delay free
     loop or has no input - error.
```

The above scheduling algorithm must be invoked once for each distinct set of clock states.

The definition of an operation ensures that the network operation is well defined in multirate systems, even when signals at different rates are combined. Rate changes can have either a mathematical resampling action (ie. output is zero between input samples), or have a sample and hold type response, depending on the connection of the clock dependent inputs. Each operation has six function pointers associated with it (the functions can be empty). These define the run time operation during the very first and very last clock cycle, immediately prior and immediately after each simulation run, and during a warm up period (to allow filter transients to die down) and during the actual simulation period. The system can be simulated many times in a single program run.

The user does not need to understand how the network of elements entered is transformed into a network of operations and the user never comes into contact with the clock dependent inputs. The modular approach adopted allows new element definitions to be added easily without altering the core of the program.

Some Common Elements Expressed as Operations

Gain elements including nonlinear gains such as saturation, overflow, absolute value, quantisers, piecewise-linear non-linearities, dB/linear conversion etc. are each represented as a single operation (Fig. 3). The left hand clock dependent input ensures that the output is recalculated whenever the input changes. The right hand clock dependent input ensures that the operation is included in any recalculation of the output node, even if the input has not changed. Input elements are similar to gain elements but with no dependent node. The output of a signal source usually has a forced clock applied to provide a starting condition for the algorithm.

The delay element is represented by two operations (Fig. 4). This is because the output must be available for calculation before the input has been calculated. The definition of a delay element effectively "opens up" any loops (loops must contain a delaying element) and changes the topology from having loops to a tree structure, without any loops. Referring to Fig. 4, 'delay 1' is dependent on 'delay 2' and so 'delay 2' is always executed first. The link between the two operations is not realised using a node ensuring that no loops are formed. Note that all this is hidden from the user who simply enters an instruction line 'delay x1 x2' to implement a delay from node x1 to node x2.

Sample-rate changes are implemented by a modified linear gain element. For both the mathematical resample (Fig. 5), and the sample & hold element (Fig. 6), the new sample rate is forced upon the output node (making use of Rule 3, above). A decimating FIR filter (Fig. 7) is efficiently realised using a cascade of a circular buffer operation followed by an FIR operation which takes a vector dot product of the vector of previous inputs with the filter coefficients. The rate change is implemented between the two operations so that the vector product is taken only when necessary. This scheme also works for non-decimating FIR filters. Interpolating FIR filters are more efficiently realised by a poly phase structure [1].

More complex elements can have several outputs. The additional outputs come from additional operations dependent on the output of the main operation.

Significant memory can be saved when implementing certain operations which act on complete signals, eg FFTs, by performing the operation in place, where the output data is stored in the same memory locations as the input data. The destruction of the input data can be delayed by assigning the outputs of all operations dependent on the input to the FFT (or other) element as dependent nodes to the FFT element. This gives the illusion of separate input and output nodes even although storage is not assigned to both. Elements which can use this technique include the FFT, PSD (for conversion of a FFT record to a squared magnitude spectrum), log_sig (for conversion to a dB scale) and various signal shortening operations to reduce the number of data points for graph plotting.

III. THE PROGRAM IN USE

Fig. 8 shows a simple sigma delta modulator in flow graph form suitable for simulation. The nodes must be labelled and entered as a net list. An input signal must also be included which can be built up from a variety of ac and dc sources, or taken from a file. The output must also be sent to file (which can be either a terminal, disk file, or a UNIX pipe to an external program). Normally some form of analysis would be done on the output before it is sent to a file. The 'sweep' element is similar to a dc source except that its value changes from one simulation to the next (but within the same program run). This may be used to modulate the input signal (either the amplitude or frequency) or to adjust the value of some of the gains, or to adjust the word-lengths in digital systems. This provides great flexibility and is very simple to use.

Normally, built in, single operation integrators would be used for the integrators in Fig. 8. These can include non-ideal effects [2]. By quantising the input and modelling numerical overflow properly, digital systems can be simulated in the same manner. Both analogue and digital elements may exist in the same system.

Determination of SNR, THD and IMD.

The SNR, THD and IMD can be estimated by performing a least squares fit of a number of reference signals (eg. DC, the input signal and its harmonics) onto the output of the modulator [6]. This can be done in either in the time or the frequency domain. The least squares element has several inputs which are signals (the reference signals) and a number of outputs representing the signal power, the noise power, the proportion of each reference signal in the signal being analysed and the power of each of reference signal. These can be then be combined to calculate the SNR, THD, IMD as required. Fig. 9. shows the analysis part of a network. The user constructs the analysis network in the same way as for Fig. 8. Each block represents a single element, which may be composed of several operations. The SDM could be that of Fig. 8. Its output is stored to form a signal. The multirate logic automatically ensures that the least squares estimation, ratio, dB conversion, rectangular to polar and print operations are only executed only once, after each simulation run. The great flexibility afforded by the above technique arises by not splitting the simulation and analysis parts of the program.

IV. CONCLUDING REMARKS

A method for efficient simulation of multirate sigma-delta systems has been presented. The algorithm has been encoded using the 'C' language, under the UNIX operating system. The program has proved to be very useful and powerful. The program has been used to evaluate many different topologies and has replicated the results of the purpose written programs used to analyse a third order cascade [7], a fourth order single loop ADC [8] and a converter with a multibit quantiser but with single bit feedback [9].

ACKNOWLEDGMENTS

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FIGURES

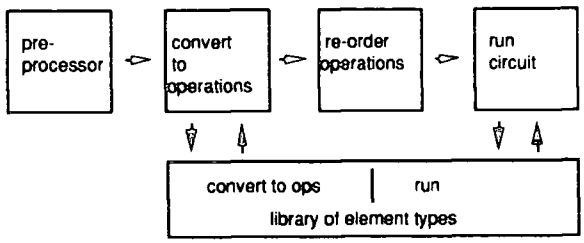

Fig. 1 The program runs in four stages and makes use a large library of element types.

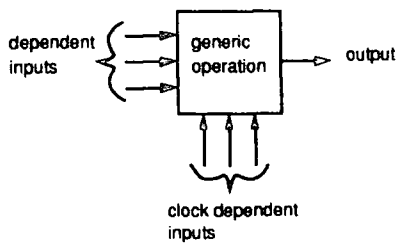

Fig. 2 Each operation has a single output, but can be dependent on several input nodes. The clock dependent inputs determine the exact behaviour of operations in multirate networks.

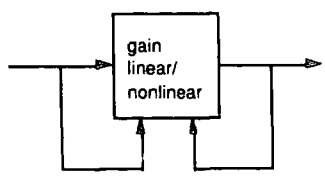

Fig 3 Representation of a simple gain.

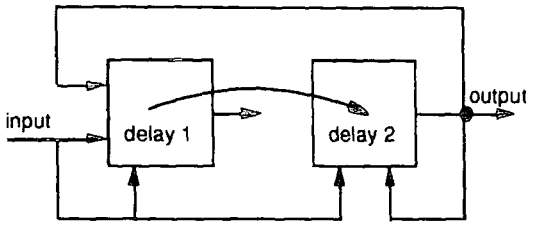

Fig. 4 The delay element is composed of two operations which are executed at different times.

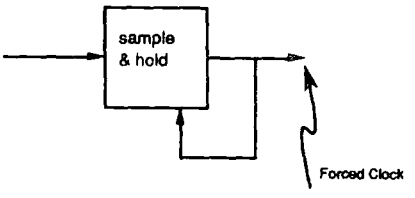

Fig. 6 The sample and hold operation is executed at the rate of the output.

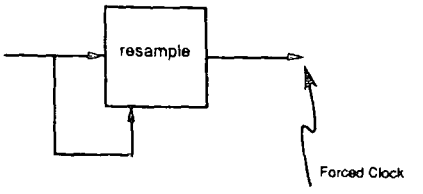

Fig. 5 The resample operation is only executed when the input changes and the output node is active (as determined by the forced clock).

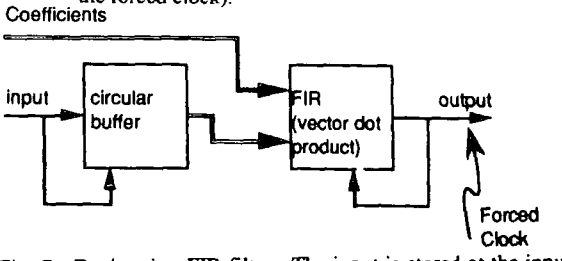

Fig. 7 Decimating FIR filter. The input is stored at the input rate, but the output is only calculated at the lower rate.

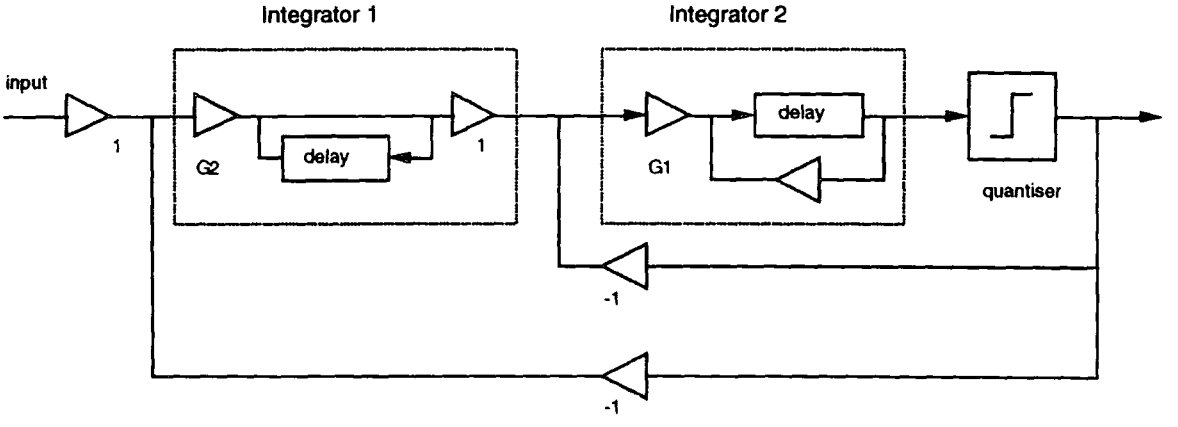

Fig. 8 A second order sigma-delta modulator [10]. For simulation, the nodes must be labelled and the system entered as a net list.

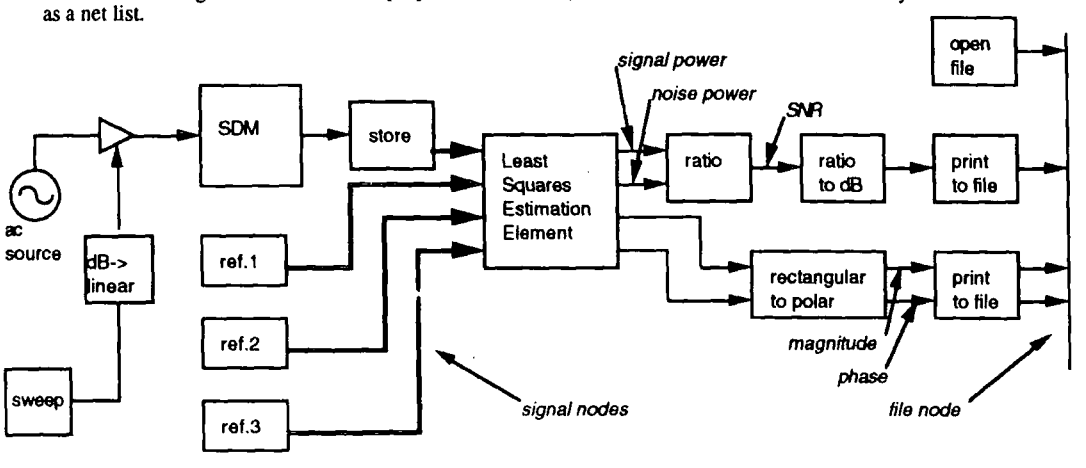

Fig.9. Block diagram representation of a simple analysis.

PAPER 50

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Design of High Order Audio Sigma-Delta Modulators with Minimum Weighted Noise

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Abstract - This paper discusses the design of sigma-delta modulators specifically for digital audio. Approximation techniques for the signal transfer function and the noise transfer function are described which give an audible noise improvement over classical functions. The noise transfer function shapes the quantisation noise to be least audible to the ear, while the signal transfer function is given preemphasis to match the dynamic range of the modulator to the dynamic range of typical audio sources. These functions are then transformed into switched capacitor networks for the loop filter in an ADC. These give a combined improvement of 24 dB in weighted SNR for the example modulator, a seventh order, 32 times oversampling one bit modulator.

I. INTRODUCTION

Sigma-delta modulation has recently become the preferred method for conversion between analogue and digital domains for audio signals. The main reason for this is the inherently high linearity which can be achieved with standard CMOS IC processes without the need for trimming. This paper discusses the design of the loop filter transfer functions for higher order modulators which are optimised for the particular case of audio.

Three areas of audio sigma-delta modulator design are described here. Firstly, the determination of stable noise transfer functions (NTF) designed using arbitrary approximation methods so as to minimise the audible effect of quantisation noise. The possibilities of introducing preemphasis into the signal transfer function (STF) are then introduced and a direct method for the design of analogue loop filters is given. The paper concludes with an example.

To avoid confusion with standard filter terminology, the terms *signal band* and *noise band* are used here. The signal band refers to the audio region (typically 0 to 20kHz) and is the stop band of the NTF and is contained in the pass band of the STF. The noise band refers to all other frequencies.

II. NTF and STF DESIGN

The design of the loop filter starts with the determination of a stable denominator. Two numerators are required for this denominator: a high pass function for the NTF and a lowpass function for the STF. These functions can then be transformed to give a single loop filter.

A. NTF/STF denominator design

The key to the design of stable high order sigma-delta loops is the NTF denominator. The poles must be chosen to limit the high frequency gain to be around 3 dB [1]. It is also necessary to ensure that the coefficient of the highest power in the denominator is unity - this ensures that the sigma-delta loop is not delay free [4]. There is no constraint on where in the unit circle the poles may lie; the constraint is that the multipling constant must be unity while the high frequency gain must be around +3 dB. A convenient way to satisfy these requirements is to use Butterworth or Inverse Chebyshev high pass filter pole positions and to adjust the cutoff frequency to move the poles towards or away from the unit circle to adjust the gain to the desired value. A simple computerised iteration process can be used to achieve this.

B. NTF numerator design

The zeros of the NTF can be chosen almost independently from the poles because, for reasonable oversampling rates, moving the zeros through the signal band has very little effect on the response in the noise band. Rather than using classical approximations (either Butterworth with all zeros at DC, or inverse Chebyshev with an equiripple noise response), the method adopted here involves placing the zeros so as to minimise the audible effect of the shaped quantisation noise. Fig. 1 shows the typical response of the ear to low level sounds. This curve, referred to as the F-curve, was derived

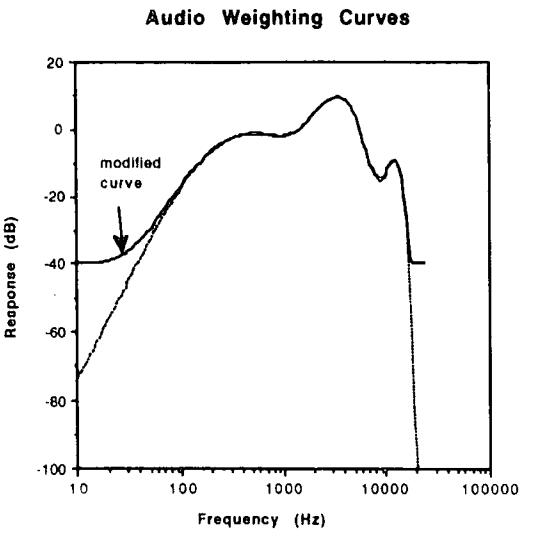

Fig.1 The shape of the F-curve which models the frequency response of the ear.

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from ISO data [2]. To limit high audio frequency noise to more typical levels, this curve is modified so as to flatten out at -40 dB.

We want to minimise:

$$\int_{\text{signal band}} |W(z)|^2 \frac{|N(z)|^2}{|D(z)|^2} dz \qquad (z = e^{j\omega}) \qquad (1)$$

with $$N(z) = \sum_{i=0}^{i=n} a_i z^i, \quad a_0 = 1 \qquad (2)$$

and D(z) is a stable denominator and W(z) is the chosen weighting function. Thus we want to fit $\sum_{i=1}^{i=n} a_i z^i$ to the constant -1 over the signal band, with a frequency dependant weighting function. This is achieved by using least squares techniques. Direct solution from the normal equations proved to be numerically problematic, but good results were obtained using a singular value decomposition method [3]. The order of the problem can be halved by forcing the zeros to lie of the unit circle:

For n even:

$$\textit{fit:} \quad \sum_{i=1}^{n/2} a_i (z^{n-i} + z^i) \quad \textit{to} \quad z^n + 1$$

$$a_i = a_{n-i} \;, \; \frac{n}{2} + 1 \le i \le n \qquad (3)$$

(ie. coefficients are symmetric)

For n odd:

$$\textit{fit:} \quad \sum_{i=1}^{(n-1)/2} a_i (z^{n-i} - z^i) \quad \textit{to} \quad z^n - 1$$

$$a_i = -a_{n-i} \;, \; \frac{n+1}{2} \le i \le n \qquad (4)$$

(ie. coefficients are anti-symmetric)

In both cases the weighting function is:

$$W(z) = |F(z)Dec(z)| \qquad (5)$$

where F(z) is the F-curve and Dec(z) is the Decimation filter response. The magnitude of Dec(z) can often be assumed to be 1/STF over the signal band so as to give an overall flat signal response.

The functions are evaluated over a mesh of frequencies throughout the signal band. If the real decimation filter response is known, then the mesh can be carried into the noise band to take into account the noise which is aliased back into the signal band.

C. STF Design

Only the numerator of the STF can be designed independently from the NTF. A number of possibilities are available. Once choice would be a constant (or a constant multiplied by a power of z^{-1}). This gives a low pass response with flat response through out the audio band with a lot of attenuation at high frequencies. An alternate choice would be to place the zeros on top of the STF poles (which are the same as the NTF poles). This is seen to reduce the capacitance spread after scaling. However unless an additional summer is used, the order of the numerator is constrained to be one less than the denominator (for the cascaded resonator topology) and so at least one pole must remain uncancelled. For odd n, the result is a smooth first order lowpass STF with cutoff well beyond the signal band.

Alternatively, the STF may be modified to include some pre-emphasis. For audio, this can give some improvement by better matching the dynamic range as a function of frequency of the audio source material to the ADC. Typically less dynamic range is required at high frequencies and this can be traded for more dynamic range at low frequencies. The pre-emphasis can be removed by the decimation filter to give an overall flat frequency response, but with a frequency dependant overload range. It should be noted, however, that "peaky" responses imply large Q factors which cause the time-domain response from the input to the comparator to exhibit overshooting and ringing in response to transient inputs such as step functions. The overshoot can take the modulator beyond its stable region. Thus the amount of preemphasis that can be applied in practice is limited.

III. LOOP FILTER REALISATION

For the case of analogue to digital converters it is possible to directly convert the NTF and STF into the capacitance values used in the cascaded switched capacitor (SC) resonator topology . The loop filter is formed by a cascade of the first and second order sections shown in Fig. 2 [4]. Each section has a cascade input, and feed-ins from the signal input and comparator feedback signal. This topology can also be used for digital modulators. The capacitor values could be determined by solving the difference equations representing the network to determine the transfer function in terms of the capacitor values and then solving the sets of equations arising by equating coefficients of z. This is cumbersome for higher orders and is not amenable to automated design by computer. A general design procedure is described here.

For the first order section in Fig 2.:

$$\frac{Y}{X} = \frac{f_i z^{-1}}{1 - z^{-1}} \qquad (6)$$

and for the second order section:

$$\frac{Y}{X_1} = \frac{f_i z^{-2}}{1 + (b-2)z^{-1} + z^{-2}} \qquad (7a)$$

$$\frac{Y}{X_2} = \frac{f_{i+1} z^{-1}(1 - z^{-1})}{1 + (b-2)z^{-1} + z^{-2}} \qquad (7b)$$

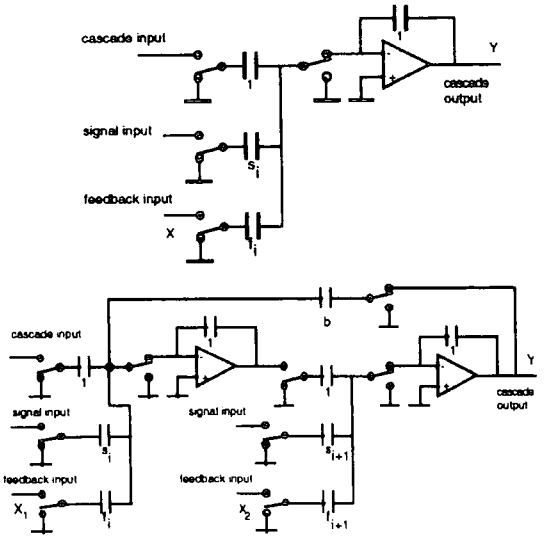


Fig.2 The first and second order sections used to build up high order loop filters.

As only capacitor ratios are required, the integrating capacitors and the coupling capacitors are initially chosen as unit capacitances, leaving only the resonance capacitors (b) and the signal and the feedback feed-in capacitors unknown (s_i and f_i). The final values of the unit capacitances will be determined by scaling the network to limit maximum signal swings and minimum capacitances.

Knowing the STF and NTF, the design of the loop filter is straight forward. From Fig 3.:

$$NTF = \frac{N_{ntf}}{D_{ntf}} = \frac{Y}{Q} = \frac{D}{D + N_Q} \quad => \quad \frac{N_Q}{D} = \frac{D_{ntf} - N_{ntf}}{N_{ntf}} \qquad (8)$$

and:

$$STF = \frac{N_{stf}}{D_{stf}} = \frac{Y}{X} = \frac{N_{sig}}{D + N_Q} \quad => \quad N_{sig} = N_{stf} \qquad (9)$$

Thus from (8), the zeros of the NTF form the poles of the sigma-delta loop filter. The zeros are easily obtained from the NTF coefficients because they are known to lie on the unit circle. The loop filter therefore has poles on the unit circle and so is not stable and the response is quite unlike standard filter responses. The resonance capacitors (b in Fig. 2) can be determined directly by equating coefficients of the NTF numerator (N_{ntf}), and the denominator of (7b). As in ordinary cascaded biquad filter design, there is a choice over section ordering Experience has shown that implementing the lowest frequency zeros toward the input lowers the final capacitance spread.

The feedback capacitor values (f_i) can be obtained from the solution of:

$$\mathbf{A} \cdot \underline{f} = \underline{N_Q} \qquad (10)$$

where $\underline{f}$ is the column vector of unknown capacitances, $\underline{N_Q}$ is the column vector of desired loop filter numerator coefficients and the columns of **A** contain the coefficients of the transfer functions from each feedback input to the output which are now known as the values of the b coefficients have already been determined. The transfer function coefficients for **A** are easily determined from the representation of the loop filter given in Fig 4. The seventh order loop

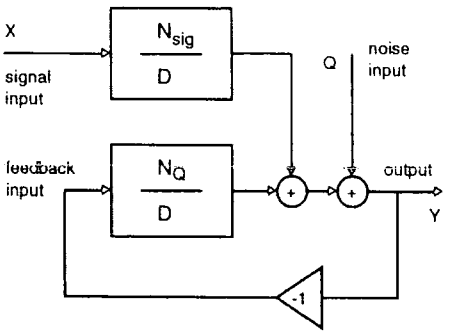
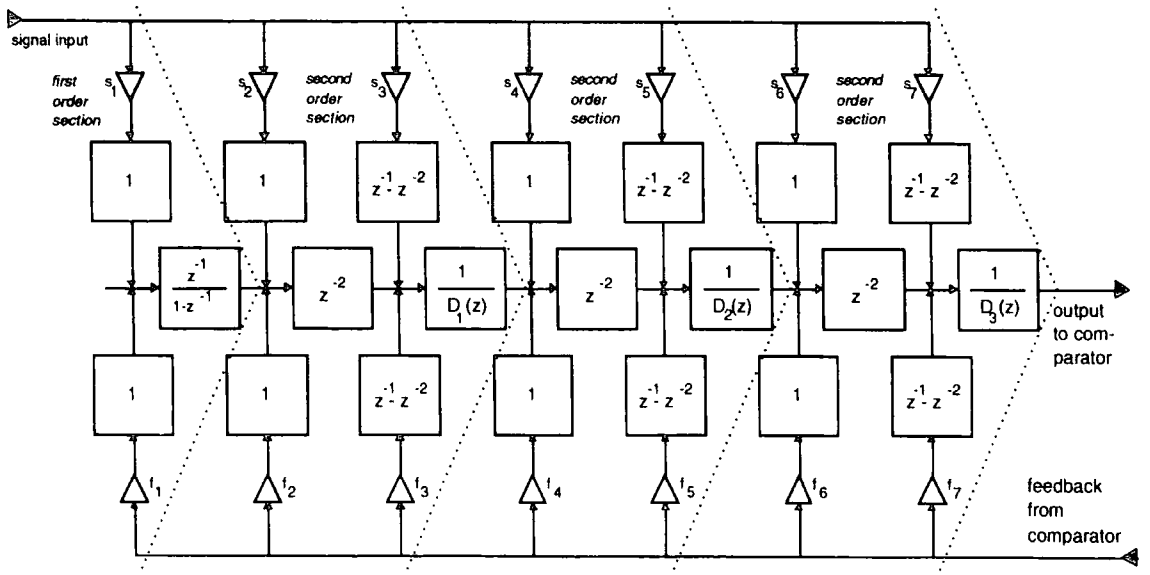


Fig. 3 Linear model of sigma-delta loop. Both the NTF and STF are realised using the same circuit and so share common poles.

filter consists of a cascade of one first order section and three second order sections. The coefficients f_i and s_i are equivalent to the feed-in capacitors in Fig.2, and the $D_i(z)$ represent the second order section denominators as in (7). Each b_i is implemented by a single resonator feedback capacitor. Assuming the NTF denominator has highest power of z equal to unity, the loop filter will contain the necessary one sample delay. Thus the *n*th order loop filter transfer function has a numerator with only *n* non-zero coefficients as opposed to *n* +1 for a general *n*th order polynomial. These *n* coefficients are used to determine the *n* unknown feed-in capacitors (f_i) by the set of equations (10). Since $N_{stf} = N_{sig}$ (9), the same approach can be used to obtain the input capacitance values (s_i).

The loop must then be simulated in the time domain and capacitors scaled to limit the maximum internal swings. It is possible to reduce capacitance spread by reducing some of the internal signal swings. While in the case of ordinary SC filters this is at the expense of dynamic range, the action of the noise shaping serves to greatly reduce the effect of thermal noise from the integrators and switches towards the comparator. Only the noise from the first op-amp and the switches around it (and to a lesser extent, the second) are critical to the performance of the complete modulator.



$$D_i(z) = 1 + (b_i - 2) z^{-1} + z^{-2}$$

Fig. 4 Simplified representation for a seventh order loop filter.

This whole procedure (including simulating for the purposes of scaling) has been automated and can convert NTFs and STFs of any order into SC loop filters. The output files are suitable for direct analysis and simulation by the SCNAP suite, SWITCAP and a discrete time simulator. The topology and this method are also applicable for bandpass systems.

IV. EXAMPLE

The example is a very high order (7th), very low oversampling ratio (32) modulator. This was chosen to investigate the potential performance of very low oversampling one bit modulators. The bit rate at the output of this modulator is only a factor of two over ordinary 16 bit pulse code modulation (PCM).

Fig. 5 shows the NTF and STF compared to a classical design and in Fig 6 the NTF curves have been weighted by the F-curve and decimator response. As a result of the weighting function, the optimised response exhibits a zero near the frequency where the ear is most sensitive. The weighted SNR curves shown in Fig 7 show significant kinks at around -50 dB input signal. This is due to signal correlated components in the signal band. However with the application of 1st order high pass dither applied in front of the comparator (at a level comparable to the maximum signal swing), these components disappear with little impact on SNR or dynamic range.

Of the two classical designs shown, the Butterworth one (all NTF zeros at DC) performs better under the F-curve weighting than the inverse Chebyshev design. This is because the noise power in the Butterworth case is most significant at the high audio frequencies where the ear is very insensitive, and has less power in the low audio frequency range where the ear is most sensitive.

The improvement in weighted SNR due to optimum placing of NTF zeros was 16 dB and an additional 8 dB improvement gained by adding the preemphasis to the STF.

The STFs were given a DC gain of -6 dB so that the modulator becomes unstable for inputs above 0 dB (0 dB defined to be power in a sinusoid with peak amplitude equal to the quantiser output.) The onset of instability can be detected and with proper design it is possible to limit multiple reset cycles from the output to give a cleanly overloading system [4].

The simulations were all performed using a multirate discrete time simulator [5].

V. CONCLUSIONS

It has been shown that significant audio improvement can be achieved in sigma-delta modulator designs by shaping the NTF and STF with non-classical functions. The direct transformation of these functions into SC loop filters has also been illustrated. The methods should also be applicable to other application areas where a non-flat noise spectrum and/or non-flat overloading characteristics are appropriate.

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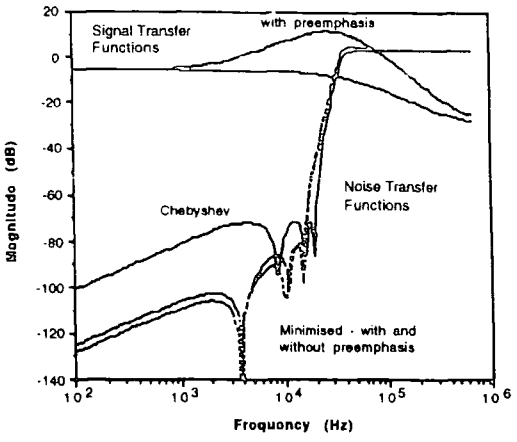

Fig. 5 Unweighted signal and noise transfer functions.

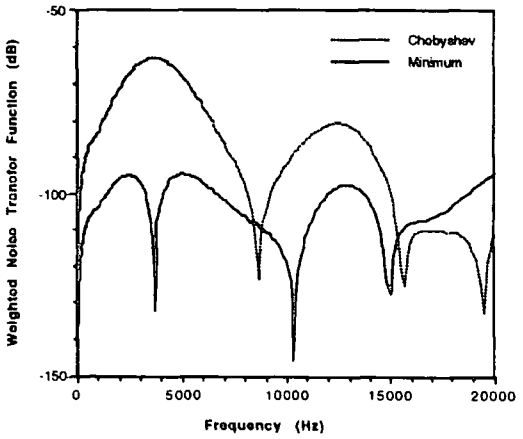

Fig. 6 Weighted noise transfer functions.

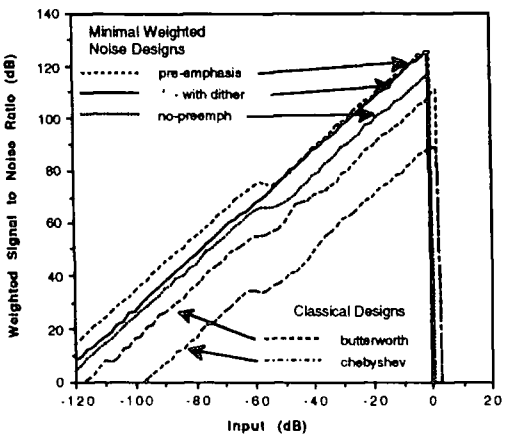

Fig. 7 Comparison of weighted noise performance of 7th order sigma-delta modulators with various NTFs and STFs.

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Proceedings of IEE Colloquium on Oversampling Techniques and Sigma-Delta Modulation, London, March 1994.

Issues in the Design of Low Oversampling Ratio Single Bit Sigma-Delta Modulators

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Abstract The linear delta modulator is shown to be a special case of the more general sigma-delta modulator, in which the signal and noise transfer functions are equal. Thus the extensive knowledge of delta-modulator systems may be applied to sigma-delta modulators and the more recent research interest in sigma-delta modulators applied to further refine delta modulator systems. High order sigma-delta systems may be designed which retain the single pole -6dB/octave overloading characteristics, but with the advantages of higher order noise shaping. Techniques for adaptive step size, both instantaneous and syllabic may be adopted to give companding operation. By damping the loop integrators slightly, the cutoff phenomenon may be used to give a noise gating effect.

These techniques have been used for a design study for the integration of a switched capacitor speech coder/decoder with a bit rate of 32kbits/s to 64kbits/s. The resulting system gives a significant performance improvement with similar complexity compared with a linear pulse code (PCM) approach using the same bit rate. In this application, there is no requirement for digital decimators and interpolators to process the digital data.

Introduction The recent interest in oversampled sigma-delta modulators has been mainly due to the availability of high performance analogue and high density VLSI digital IC processes making inherently linear A/D and D/A conversion possible. Earlier interest in the closely related oversampled single bit system, the delta modulator, was not because of the inherent linearity of the 2 level quantiser, but for its simplicity of conveying analogue information digitally with a low bit rate. The motivation for this work was to provide a robust and low cost method for digitising and reconstructing speech signals on a mixed signal IC process. It is often cheaper in terms of silicon area to implement functions in the analogue domain rather than digitally when using an analogue process. The use of a process with well defined analogue characteristics is mandated by system requirements such as signal coding/decoding, companding, soft limiting, signalling tone generation/detection, general purpose ADCs and DACs (used for signal strength measurements, battery monitoring, battery temperature monitoring etc), power supply regulation and monitoring, power-on reset functions, loudspeaker drivers, microphone amplifiers, signal level trims and volume controls. The methods described here have been used to design sigma-delta modulators, suitable for speech applications with low bit rates, which can be implemented in a cost effective manner on a mixed signal IC process. The digital signal format used, an unframed single bit between 32 - 64 ksamples/s corresponds to oversampling ratios between four and eight.

Equivalence of Delta and Sigma-Delta Modulators In the basic delta modulator, the input is applied after the loop filter, just before the quantiser. The basic sigma-delta modulator differs in that the signal is applied in front of the loop filter. In general the signal input may be applied anywhere in the noise shaping loop to perturb

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the system idling and so encode the input. The general sigma-delta loop is shown in Figure 1. For a delta modulator $N_{SIG} = D$, while for a basic sigma-delta modulator $N_{SIG} = N_Q$. The signal transfer function (STF) is defined as the transfer function from the signal input to the output and the noise transfer function (NTF) is defined as the transfer function between the quantiser and the output (assuming that the quantiser has been replaced by a linear gain).

Optimisation of Signal and Noise Transfer Functions The signal transfer function may be designed to match the long term spectrum of the speech input (typically between -6dB and -12dB per octave over 300-3kHz) while the noise transfer function may be optimised with a higher order function to push noise away from the ears most sensitive frequency ranges within the signal band [1]. However with low oversampling ratios the noise shaping performance quickly becomes limited by the information capacity of the bitstream output [2].

Figure 2 shows how the quantisation noise in a third order delta-modulator can be rejected at the frequencies where the ear is most sensitive. This modulator gives an SNR of 33dB over a 4kHz bandwidth (eight times oversampling). The delta modulated signal is reconstructed using an integrator and a lowpass filter to remove most of the quantisation noise.

The loop filter is implemented on silicon using standard switched capacitor filter methods.

Companding Step size adaptation, as used in delta-modulator systems [3], can also be used for sigma-delta modulation. This allows the oversampling ratio to be significantly reduced while maintaining a single bit output per sample (Figure 3). Syllabic companding extracts low frequency envelope information from the encoded bit stream using a coincidence detector, which looks for strings of three or four ones or zeros in the bit stream, together with a filter of time constant of the order of 10ms. The coincidence detector has zero output, except when the last three or four samples are all the same. This indicates that the modulator is potentially overloaded and that the step size should be increased. The output of the coincidence detector is low pass filtered with a cutoff frequency which allows the signal level variations to pass through. The filtered coincidence level may be used directly to set the step size. Different companding ratios may be implemented by changing the gain or shape of the mapping between the filtered coincidence signal and the step size.

For syllabic companding it is necessary to encode and extract the signal level from the bit stream in order to determine the current step size. This is done by considering the effective operating point on an un-companded system. Figure 4 shows the limited dynamic range of an un-companded second order sigma-delta modulator and Figure 5 shows the corresponding filtered coincidence levels. The 3-bit algorithm gives a better indication of the operating point over the amplitude region with best SNR performance. The coincidence level is used to convey the signal envelope information. Figure 6 shows the coincidence level and corresponding step size for a companded system, and Figure 7 shows how the SNR vs input amplitude curve of Figure 4 has been "stretched" out over a wider dynamic range.

The long time constant required by the syllabic filter is better implemented using simple digital methods rather than with switched capacitors. This gives more flexibilty in the forming of the current step size from the coincidence filter output. The filter can be efficiently implemented using a digital rate multiplier or with bit serial techniques. For speech, the attack time constant is made smaller than the decay time constant in order to provide a better match to the envelope of syllables. The variable step size required in the analogue feedback path can be implemented by using a range of feedback capacitors and also by switching the capacitor to the reference several times within a single sample period. The non-linear function for mapping coincidence rate to step size may be

effected with no additional cost over a linear mapping.

The use of a coincidence detector is less effective for the third order system. To operate the higher order system in its stable region requires that the input is smaller (maximum peak -6dB relative to the feedback level) and consequently long trains of ones or zeros cannot occur. Syllabic companding can be implemented however, by extracting the magnitude of the reconstructed signal and using the magnitude to adapt the step size [5]. Companding causes the modulator to be used near its optimum operating point for wider ranges of signal levels. For high order systems this can assist system stability - any tendency to go unstable will be counteracted by an increase in step size.

An alternate form of companding again looks for patterns in the recent history of the bit stream, but adapts the step size immediately relative to its previous size.

Noise Gating and Offset Cancellation By deliberately damping the loop integrators slightly, the modulator can be forced into a ...1010101010... output pattern for very small inputs. This contains no base band power and so the back ground quantisation noise can be made to disappear in the absence of a speech input. This effect is normally considered a defect in sigma-delta systems [4] but is widely used for delta-modulator systems [5]. Offset cancellation can be provided in much the same way as for μ-law and A-law PCM systems. The bitstream is integrated. Ideally there will be an equal number of ones and zeros in the output and any deviation from this is fed back to reduce the offset.

Bit Errors Since each of the bits in the bitstream carries equal weight to all the others, analysis of the effect of bit errors is simplified. A single bit error results in an impulse of twice the current step size. A single bit error will have negligible effect on the step size. Because of the oversampling, most of the energy in the impulse is removed by the subsequent filter. The effect of a bit error in a non-oversampled PCM system can be far greater, resulting in a full scale impulse with little subsequent filtering.

Conclusions A variety of low bit rate, low complexity, coders have been studied with a view to their cost and practicality for integration. Simulations have been performed using real speech signal sources to compare performance. Recent work has allowed sigma-delta modulators to be optimised for speech applications. A number of techniques, originally devised for delta modulation, have also been employed.

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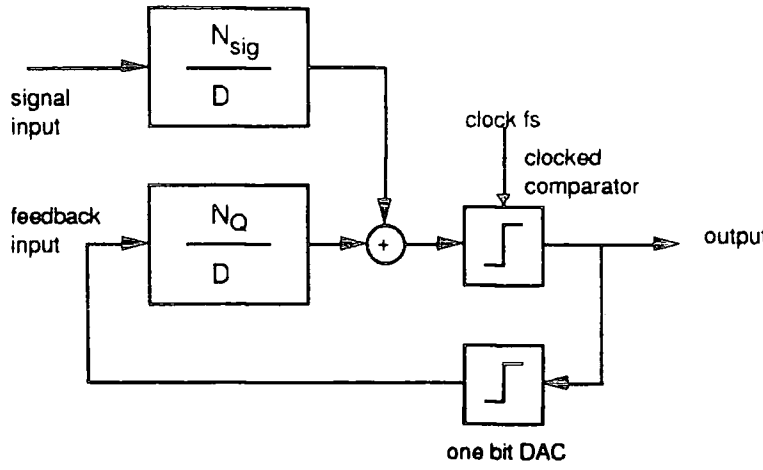

Fig. 1. General Model for Delta and Sigma-Delta Modulators.

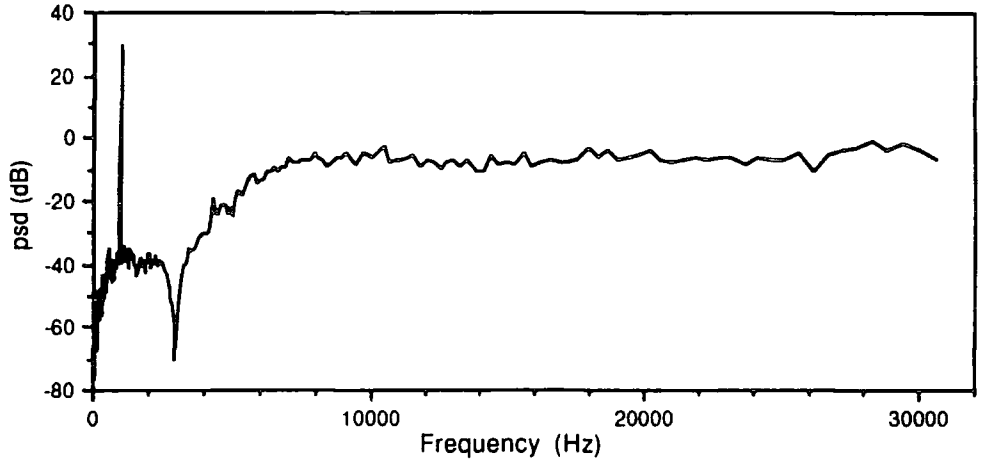

Fig. 2. Unfiltered output spectrum of a third order delta modulator

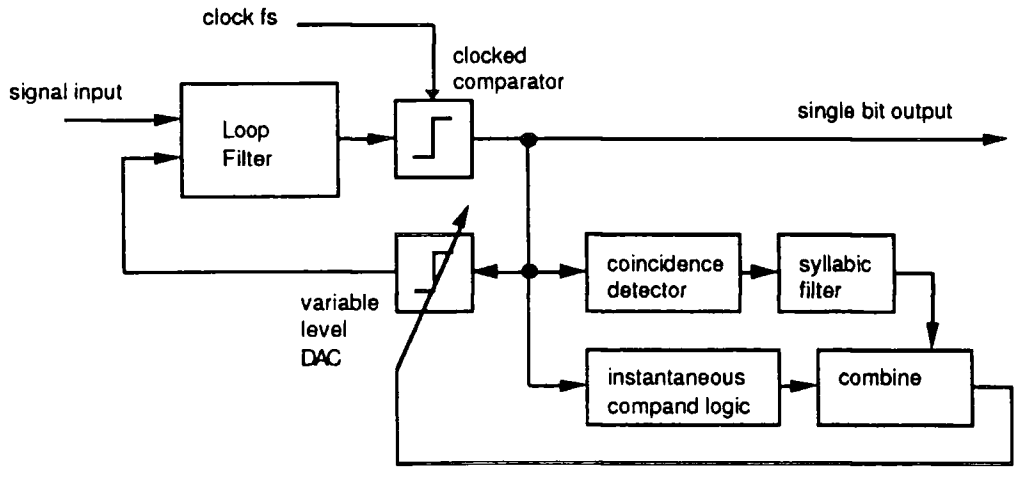

Fig 3. Companding Sigma-Delta Modulator

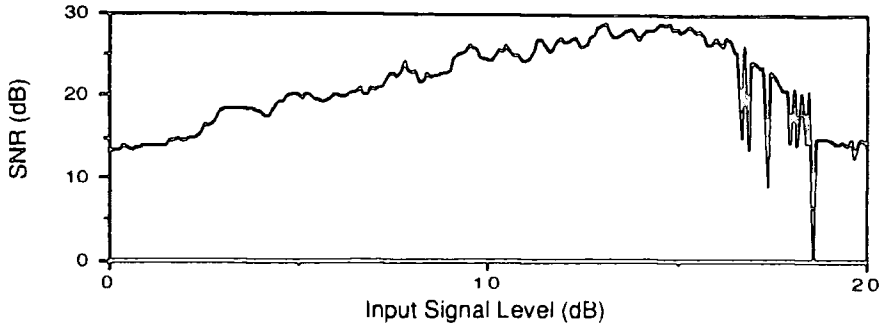

Fig.4. SNR vs input level for second order system.

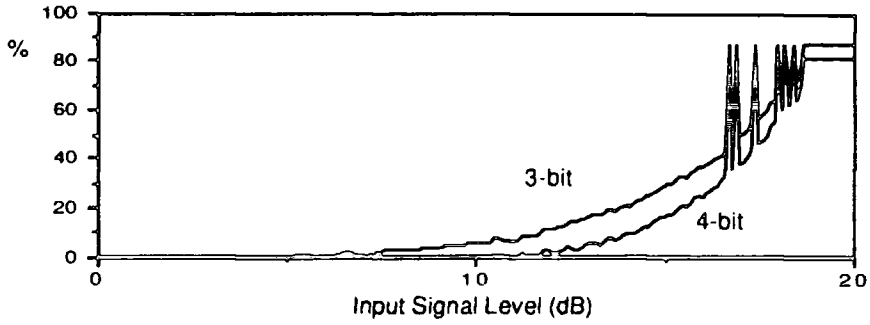

Fig. 5. Coincidence detector output for second order system.

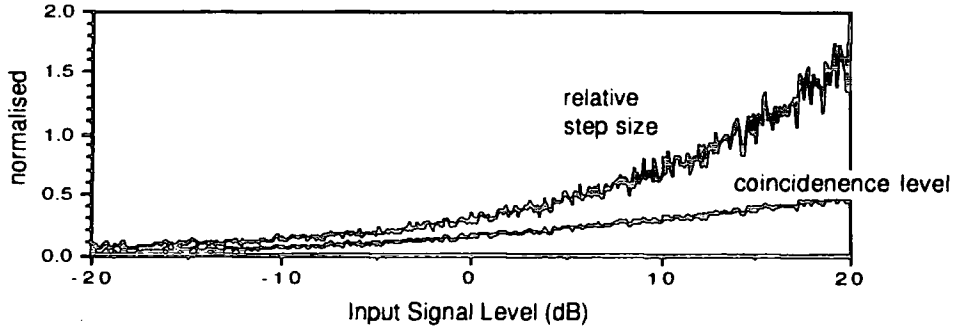

Fig.6. Recovered coincidence level and derived step size for companded system.

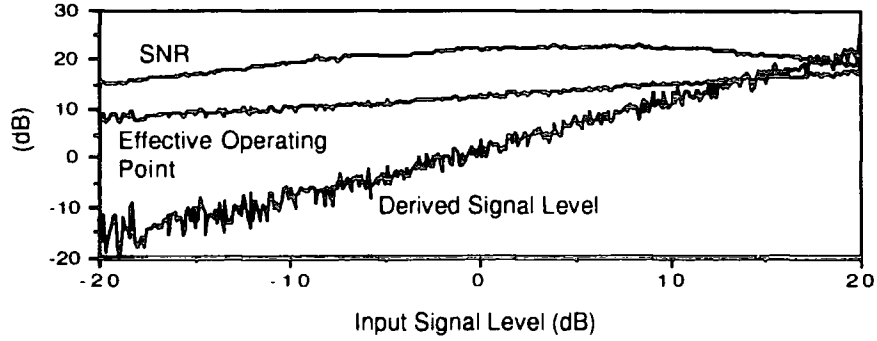

Fig. 7. Derived signal level, effective operating point and resultant SNR for companded system.

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The Application of Redundant Number Systems to Digital Sigma-Delta Modulators

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ABSTRACT

The speed at which a digital sigma-delta modulator can operate is limited by the latency of the loop filter. A digital sigma-delta modulator is presented which overcomes the problem of long adder carry propagation delays. The design is sixth order and implemented using a single pipelined resonator section.

INTRODUCTION

Digital sigma-delta modulators are increasingly being used in oversampled digital to analogue converters [1]. Since the modulator operates on oversampled data, the circuitry used must be fast. Conventional pipelining techniques cannot be applied to increase throughput due to the recursive nature of the loop. This paper discusses a technique which overcomes this problem.

A sigma-delta modulator consists of a loop filter and a comparator in a feedback loop. If the comparator is considered as an additive noise source, then the transfer functions from the input to the output, and from the noise source to the output can be determined. These are termed the signal transfer function (STF) and noise transfer function (NTF) respectively. Proper design of the loop filter ensures the modulator is stable. The signal transfer function is designed to pass the signals of interest while the noise transfer function is designed to reshape the noise spectrum appearing at the output so that there is little noise in the frequency band of interest. A digital implementation of a sigma-delta modulator must perform all the calculations required to obtain a single output sample before work can start on the next sample. This dependency of the current output on the immediately previous one limits the application of pipelining techniques to speeding up the loop operation. The delay between an input and its corresponding output is termed the latency. For high speed operation it is important to minimise the latency in feedback loops.

Recent work has overcome this latency problem for the case of high speed infinite impulse response (IIR) filters [2]. This has been achieved by adopting a redundant number system instead of the two's complement number system normally used for digital signal processing applications.

REDUNDANT NUMBER SYSTEMS

In a redundant number system, the individual digits can take on more values than the radix of the number system. In this paper only the signed binary number representation (SBNR) will be used. Valid SBNR digits are -1, 0, and +1 and each digit has a significance of two times that of the digit to its left (as in normal binary). Thus the numbers $0\bar{1}.0\bar{1}$, $\bar{1}0.11$, $0\bar{1}.11$ all represent the decimal value -1.25. The symbol $\bar{1}$ is used to indicate a weight of -1. The advantage of the redundant number system is that additions can be performed without long carry propagation chains. Figure 1 shows a SBNR adder. Each adder cell consists of three subcells A, B and C which perform an addition of digits with various ranges of values. The final result is in the same SBNR format as the input and the carry/borrows can only propagate a maximum of two digits. Thus the addition time is independent of the word length. A detailed discussion for implementing these cells is given in [2].

Ideally, in a properly designed sigma-delta modulator, the additions will never overflow, although this is difficult to guarantee. Furthermore, the left most cells may produce

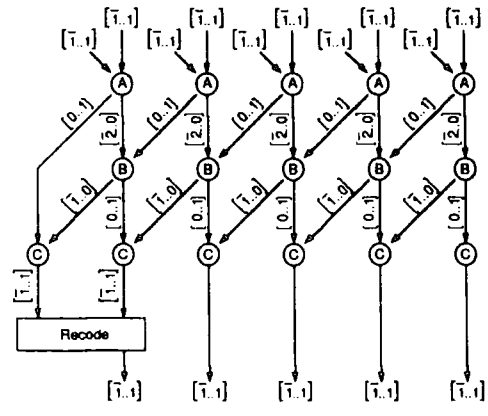

Figure 1. Fully parallel adder using SBNR arithmetic

carry/borrows even when overflow has not occurred. The cases of the two most significant digits as $1\bar{1}$ and $\bar{1}1$ must be recoded as 01 and $0\bar{1}$ to limit word length growth. Definite overflows 11 and $\bar{1}\bar{1}$ and possible overflows 10 and $\bar{1}0$ must also be caught and the output set to an appropriate saturation level.

The SBNR adder of Figure 1 may be used directly to construct a high speed sigma-delta modulator. However there is a further feature of redundant arithmetic which may be exploited. When conventional two's complement arithmetic is used in a systolic type structure, it is the least significant bits which are performed first since the more significant bits depend on the least significant bits through carry propagation. This is not the case with redundant arithmetic which allows the order of execution to be reversed giving systolic type structures which operate most significant digit (msd) first. This is in line with the requirements for a sigma-delta modulator where it is only the top few digits of the filter output which are required. Data skewed msd first has the property that gains of less than one may be performed with negative latency. This is illustrated in Figure 2. Parallel data enters at the top and is skewed such that the digits become available in groups of three. However after the right shift by three digits (a divide by eight operation), the digit representing the output is available before the digit of equal significance has entered at the top. Thus the divide by eight operation can be considered to have a latency of -1.

SIGMA-DELTA TOPOLOGY

The sigma-delta modulator topology used in this work is based on a loop filter constructed from the cascade of integrators and resonators [3]. Figure 3 shows a single resonator. The gains s1 and s2 are for scaling only and are initially assumed to be unity. The values of the comparator

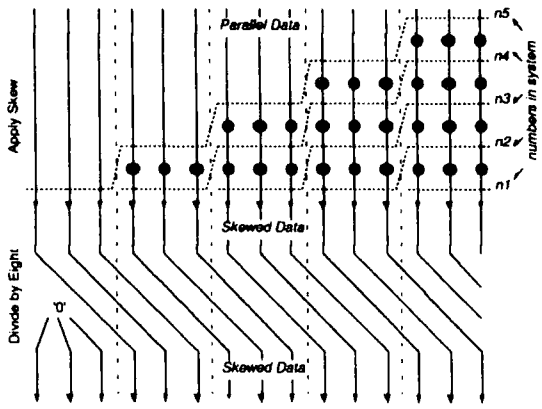

Figure 2. Parallel to skewed data conversion followed by divide by eight operation

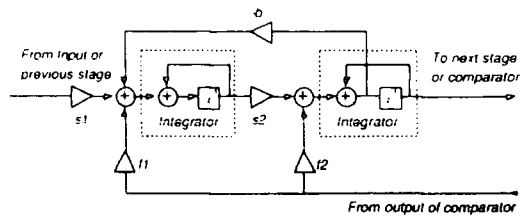

Figure 3. Second order resonator used for loop filter

feedback coefficients (f1 and f2) are determined by the solution of a set of linear equations involving the desired zeros of the open loop filter obtained by algebraic manipulation of the NTF [4]. Since the input to the gains f1 and f2 can only take on the values +1 and -1, no multiplier circuit is required. The values of the resonator coefficients (b) are directly related to the open loop poles which are at the same locations on the z-plane as the NTF zeros. This is the only gain for which a full SBNR number needs to be multiplied.

The single delay around the two integrator loop places stringent demands on the latency of the integrators. For baseband sigma-delta modulators an additional delay can be tolerated. The poles move off the unit circle giving the NTF zero at a similar frequency as before, but not infinitely deep. The depth of the NTF notches is of little consequence to the output noise level.

It can be shown that the magnitude of the coefficient b in the feedback loop is small while the feedback coefficients tend to be much larger. If the feedback coefficient is sufficiently truncated the addition of the two words can be achieved by merging the two words rather than by an arithmetic circuit.

SBNR ADDER

For the example sigma-delta modulator, it was decided that the data would be skewed by one pipeline delay every third digit, as was illustrated in Figure 2. This allows parallel computation of the top three digits which are required in parallel by the comparator. Three numbers need to be added for each integrator. Rather than cascading two dual input adders of the type in Figure 1, a two stage design was derived using the carry save concept of conventional two's complement arithmetic. This is shown in Figure 4. Three SBNR numbers are added and the effect of transfer propagation limited to the next three more significant digits. This adder produces its output after a one clock cycle delay from the pipeline cuts indicated.

SBNR COMPARATOR

The sigma-delta modulator requires a comparator. In conventional two's complement arithmetic, the output of the

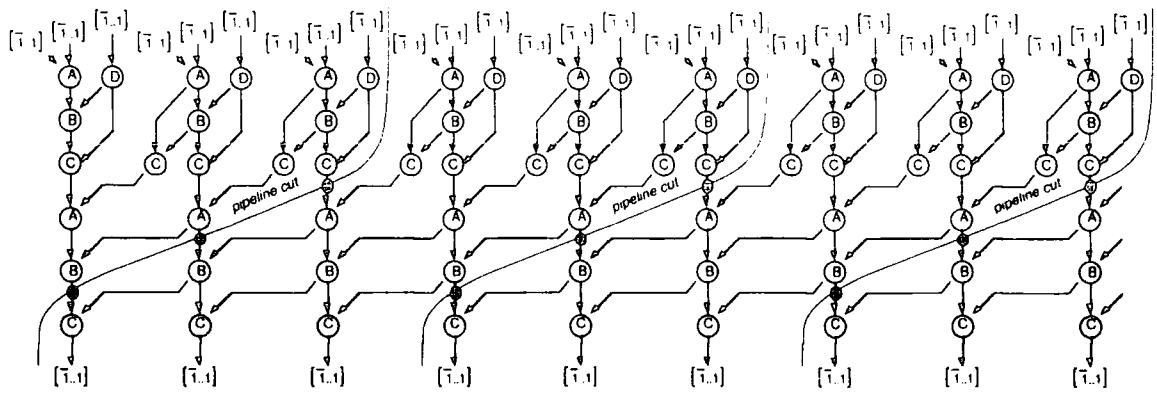

Figure 4. Three input pipelined adder operating on three at a time skewed data

comparator is simply the sign bit of the input. However this is the result of a long carry propagation chain. In SBNR there is no specific sign bit. The sign of the overall number is the sign of the left most non-zero digit. Logic is required to extract this from a parallel SBNR word. Fortunately the comparator performance in sigma-delta modulators is non-critical because any errors are reshaped with the full noise shaping function of the loop. In practice only the top three or four digits need to be examined as the additional truncation noise is less significant than the quantisation error.

In the circuit presented, the comparator has one full pipeline delay in which to come to its decision and the speed of the comparator circuitry is not a limiting factor.

SBNR SIGMA DELTA MODULATOR

A sixth order modulator consisting of a cascade of three resonators was designed (Figure 5). The signal transfer function was designed with signal band gain of -6dB to ensure that a full amplitude input signal (+1..-1) did not cause the modulator to become unstable. The noise transfer function was designed with Butterworth poles so that the signal transfer function could have a low pass Butterworth response and be implemented with a single feed-in coefficient into the first integrator.

Each integrator output in the cascaded resonator topology is dependent only on the previous output of the previous integrator. This fact is used to calculate the data in the three resonators by using a single pipelined resonator with three pipeline delays corresponding to a single z^{-1} delay. The coefficients to the single resonator are multiplexed and the state information for the three resonators contained in the pipelines (Figure 6). The multiplexers are arranged such that the function of the third resonator is performed first, followed by the second and then the first. This is to allow the comparator to come to a decision and for the feedback coefficients (with sign applied by the comparator output) to start entering the adder pipelines as early as possible. The single pipeline delay on each of the three inputs of the two adders represent the pipeline delay internal to the adder.

Note that whilst it is convenient to consider the resonator in Figure 6 as being multiplexed, this is not truly the case. At the same time as one adder is computing the most significant digit of the output, other parts of the same adder are computing other digits of the other resonators and even different digits of the previous values of the same word. The multiplexer for adjusting the scaling gain (between 1/32, 1/4 and 1/2) and the multiplexer for feeding the output of one resonator back into the input for the next must both take the skew into account. These multiplexers are actually taking different digits from each of their inputs to form the output.

The number in brackets beside some of the gain blocks indicates negative effective latency. These numbers need be taken into account when counting pipeline delays around loops. Note that there is the correct multiple of three pipeline delays around all the resonator loops. However there are only five delays around the loop which links the output of the resonator back to its input. This ensures that the data representing the output of the first resonator arrives at the right time to be interpreted as input to the second and similarly for data leaving the output of the second resonator and entering the third. The output of the final resonator is not feed back to the input - during this time the system input is sampled and multiplexed into the first integrator.

The scaling factors were chosen to the nearest power of two in order to roughly equalise the signal amplitudes at each of the integrator outputs. The resonator coefficients were also quantised to powers of two. Because the resonator coefficients are small (1/128) two extra pipeline delays become available which allows closing the resonator loop with only three pipeline delays (corresponding to a single z-1 delay) and so giving NTF zeros which lie exactly on the

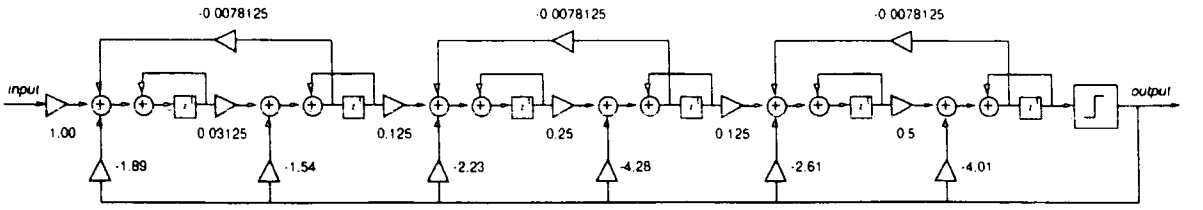

Figure 5. Block diagram of sixth order sigma-delta modulator

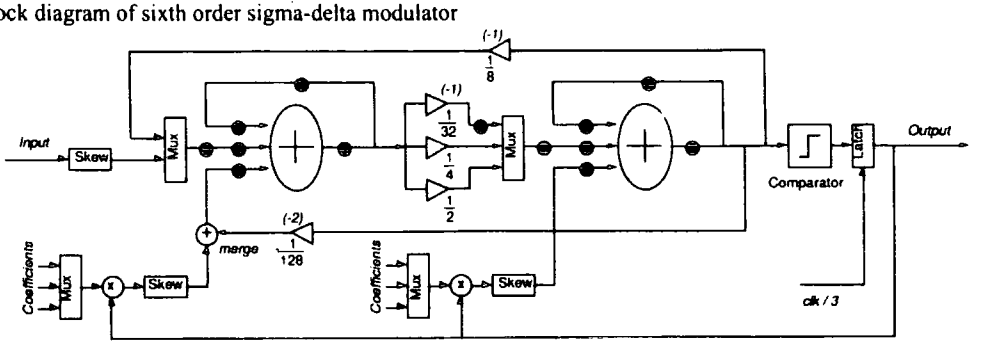

Figure 6. Sixth order sigma-delta modulator using single pipelined resonator section

unit circle. Additional adders could use the three additional delays available to place the NTF zero frequencies more accurately. It is likely that a low latency SBNR multiplier could be used to give programmable NTF zero frequencies with arbitrary precision.

Since the two's complement number system is a subset of SBNR there is no hardware overhead in converting input in two's complement form to the SBNR form required by the first adder. The word length of all SBNR data was 5 integer digits and 20 fractional digits and this could be increased without decreasing the throughput rate.

The sixth order system of Figure 6 has been simulated at the gate level using a commercial digital simulator. The output spectrum (Figure 7) shows the expected sixth order shaping

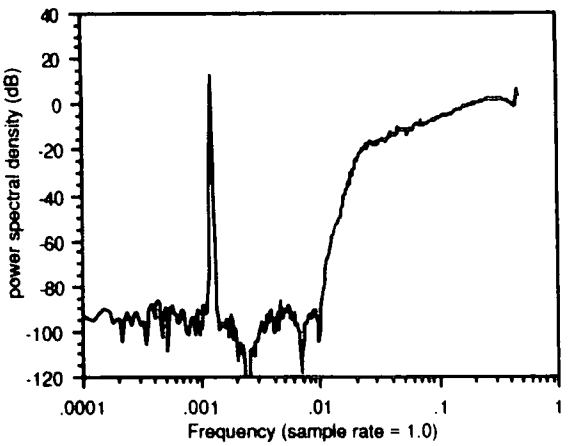

Figure 7. FFT of output of sixth order system

with an undistorted single tone. The signal to noise ratio from this simulation is 85dB with the input 20dB smaller than full scale. The modulator was designed for an oversampling ratio of 50.

This paper has concentrated on using SBNR arithmetic. The fact that it was desirable to calculate three digits in parallel suggests that a higher radix redundant number system may be more suitable and more efficient in hardware.

CONCLUSIONS

Features of SBNR arithmetic have allowed the design of a sixth order modulator (Figure 6) which produces a new sample every third clock cycle, with the clock rate limited by a single proprogation delay through the adder of Figure 4. Many other design decisions could have been made, ranging from fully parallel designs where the order and word length could both increase without affecting throughput, to more heavily pipelined systems using a single adder.

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8. Publications on Educational Initiatives

PAPER 11

A course in computer-aided electronic circuit design for undergraduates

A. G. Martin and J. I. Sewell

An undergraduate course in electronic circuit design utilizing a computer as its main aid is described. Experiences in designing and running such a course for thirty students are discussed. The application to the design of linear circuits only is outlined, but conclusions indicate that such courses are so successful that expansion to other design spheres would be equally rewarding. The importance of a controlled introduction to the computer as the most significant design tool available is stressed, so that the student appreciates the power at his finger-tips and does not become disenchanted with the computer as merely a machine which runs programming exercises.

The problem of including a course which demands the use of a computer by undergraduates in engineering curricula has been of interest for some time. It is of course essential that the student engineer acquire a respect for computational techniques and especially that he develop a sense of how best to set a computer to work.

With computer-aided instruction, as with any means of learning, the object must be to create an initial exercise which the student thinks he can solve. Once guided on to the right path the student should uncover a succession of further goals, providing stimulation to learn for himself. Open-ended problems of this sort are often met by the designer and though design teaching is often omitted from engineering courses it can provide a natural slot for computer familiarization.

A well-constructed computer-aided design course introduced at an early opportunity can demonstrate the power of computational techniques without the student first stumbling through the constructed problems of introductory programming. As well as stimulation, some disincentives must be made apparent, by pointing out that inspired paper work produces quicker but fewer results and by careful user monitoring to prevent wastage. An appropriate moment in an open-ended problem can be chosen for introducing time limits so that cut and try has to be replaced by planned optimization.

Design projects

Electronic design work has been a feature of the undergraduate course at the University of Hull for some time. Projects are introduced just before the halfway stage in the course, when about 40h of circuit theory and electronics course-work have been given. The design laboratory is intended to act as a focus to encourage the student to consolidate the analytical techniques he has just learned.

The motivation for learning in such a course is the prospect of producing with some independent effort a successful circuit in a real design situation. Past experience has shown that the point of unreality is reached when, having produced a suitable design, the student wishes to breadboard his ideas for final proof. Particular points of friction occur with designs marginally near the specification when neither student nor tutor is sure of the performance. The policy of requiring designs to be proved on paper because of the impossibility of breadboarding many modern designs is rarely convincing. Computer checking of designs not only eliminates the breadboard problem because it is quicker but also acquaints the embryonic designer with a modern technique. If additionally, as in this case, the student is meeting computer aid for the first time, an immediate effective demonstration of its versatility is achieved.

A simplified representation of modern circuit-design philosophy is given by the design flow chart in Figure 1. Some details of certain real-life situations have been omitted and the chart is terminated prematurely since no details of computer aids for circuit production are included. However, such material can be found elsewhere and anyway it is not particularly significant for a first design course. In the time allowed for the design course it is not possible to complete the whole scheme, and therefore certain steps are omitted or left for the brighter student. Hence in the computer-analysis step only a.c. steady-state analysis was undertaken by all students. A limited number of students did arrive at the stage of undertaking a simple tolerance analysis of the circuit on the machine. However, this process could not amount to more than investigating worst-case effects on circuit response.

Convincing the student that he can solve the problems is a matter of posing suitable problems. The student is invited to choose one from the following three:

1. **Transistor pre-amplifier.** Design an a.c. pre-amplifier which has an input impedance greater than 1 MΩ and a voltage gain of 20 ± 1. The maximum output

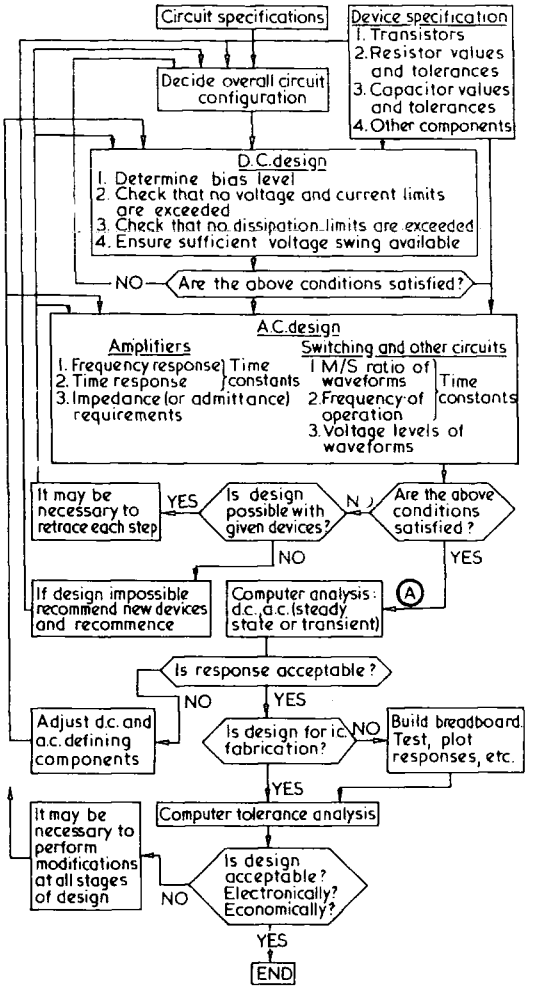

Figure 1. A basic flow chart for modern circuit design.

voltage swing is to be less than 1 volt pk–pk and the pre-amplifier is intended to drive a high-impedance load such as an oscilloscope. The pre-amplifier gain must be within the specified limits from 30 Hz to 100 kHz.

2. **Phase-shift oscillator.** Design an RC phase-shift oscillator to generate a frequency of 1592 Hz. The oscillator is intended to produce a small sinusoidal signal which will be fed into a high-input-impedance amplifier before output to an external load.
3. **Current-amplifier.** Design a transistor amplifier with a current gain of 10 having an input impedance of less than 100 Ω and an output impedance of greater than 10 kΩ.

A measure of reality is introduced by allowing only two transistors, two power supplies 0–30 V d.c. and a virtually unlimited supply of resistors and capacitors of standard values and tolerances. The student is presented with complete manufacturers' data sheets on the transistors (Mullard BC 108) and has to decide which have any relevance to his situation. The resistor information shows all the values available from stores with power and tolerance ratings; similar information on capacitors gives values, tolerances, voltage ratings and type of fabrication. The component selection which he makes can then be criticized on the grounds of availability, cost, too good or too poor quality.

The computer experiment

The initial stages of the design course progressed from the shock of the unfamiliar requirement of innovation, through problem selection and the sorting of component data and analytical skills, to eventual hand analysis of chosen circuit configurations. It was expected that most students would then check their designs and possibly correct one or two faults. However, tight time scheduling and the prospect of success encouraged a keen nucleus to finish early. Line-printer output produced a catalytic effect on the work rate of the rest of the class.

It was found that the average student required about 12h of class time to produce a prototype circuit ready for computer analysis (point A on the flow chart, Figure 1). The remaining 12h of the course were required to complete the a.c. analysis on the computer, which of course revealed more defects than the simple theoretical analysis, and to perform the necessary modifications at any or all of the steps indicated.

The circuit-analysis program used was the general circuit analysis program GCAP 1 by Redac Software Ltd. It was run under the George 3 operating system, with a suitable macroprogram on an ICL 1905E. The macro is designed to counter some of the expected problems with inexperienced computer users. As classes are of thirty students, it would be wasteful to load the program for each student. The macro loads the program once, and if any error occurs in a data set, it skips to the next data file and so on until the whole batch has been processed. Data input is via cards and the output is on a line printer. Two supervisory print-outs are also given, one of which lists all the students in a particular run for the tutor's record. The other print-out provides a detailed analysis of the loading and running of each file and hence is valuable in diagnosing run-time errors.

Results of the experiment

While the computer analysis of voltage and current amplifiers only consolidates knowledge already learned, the students attempting the design of oscillator circuits are faced with new (to the student) conceptions. Previous classwork has shown how simple unstable circuits can be analysed by hand. A circuit model has to be derived which is an accurate representation yet which cannot contain a closed loop, since the resulting instability will not be acceptable to the program.

A simple but effective technique has been evolved and is illustrated by the typical final design shown in Figure 2. The method is to break the feedback loop at the point of low sensitivity after the emitter follower. In coding the circuit for the computer the open loop is given the correct loading by repeating enough of the input circuitry, which in this case would be the common emitter stage. A reasonable estimate is made for the driving source resistance. Straightforward analysis as an amplifier is thus possible and the desired result is a gain of unity with a phase shift of 0° or 360° at the specified frequency. The model depends on representing the closed loop as a section of an infinite line circuit.

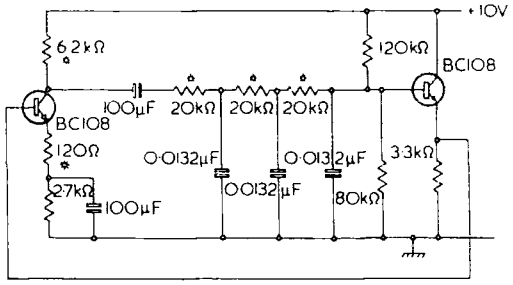

Figure 2. Final design of a phase-shift oscillator. The resistors marked with an asterisk have 2% tolerance. The remainder have 10%.

In actuality there are sub-steps, in that the first computer run provides a more precise output impedance for re-use as the driving source impedance. Next the circuit excluding the amplifier would be analysed to yield the required gain and the loading on the amplifier output. Neither of these are usually accurately calculable by approximate hand methods. After the feedback and possibly the phase have been adjusted, a final run is made to check the response of the complete circuit.

Concluding comments

Perhaps the best measure of the success of a teaching course is the difference between the expected and the actual response. All students succeeded in making a computer analysis of their design, correcting the defects revealed and making one or two further analyses. Quite a number, about a third of the class, reached the weaned state of independent investigation of the properties of their circuits. Early expectations were thus far exceeded.

In retrospect the significant spur to completing the initial effort, which takes around 12h, perhaps spread over a longer period, were the first returns of computer results. One of the jobs of the tutors is then to identify a few front-runners, who may not necessarily have shown the best previous performance, and to optimize the moment at which their efforts come to fruition.

The object of creating a gradually evolving real design environment, where the student no longer tackles lecture course problems which often necessarily have unique solutions, has to some extent been met. The students are forced to re-examine their knowledge and to complete their understanding while their designs are in progress. One spin-off which might be further developed would be to introduce, as the course progresses, the real-life problems of deadlines and organization of time and effort.

From the flow diagram of Figure 1, it can be seen that the course has concentrated on a simplified path through the chart. Obviously any course is limited mainly by time available, and hence only the design of linear circuits was done. The computer was used only for a.c. analysis and to some extent for tolerance analysis. Further extension would therefore include d.c. analysis and perhaps a Monte Carlo approach for the sensitivity. In the sphere of switching circuits it is reasonable to envisage an entire course subsequent to the one described. It appears, however, that such courses would demand at least 24 or perhaps 36h of design laboratory time. Hence, much serious thought must be given how to modify existing engineering degree courses so that such vital and stimulating exercises may be introduced.

The computer is inextricably involved in the routine of design in engineering and can provide that exciting aspect of engineering course-work which seems to have been somewhat elusive in the last decade.

Acknowledgements

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He joined the University of Hull in 1968 as a lecturer in the Department of Electronic Engineering, and is conducting research into computational methods in network theory, the design of active network devices, and the production of educational computer aids.

PAPER 27

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A DEGREE-ENHANCEMENT SCHEME IN ELECTRONIC ENGINEERING

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1 INTRODUCTION

The British educational system has traditionally enjoyed a reputation of worldwide acceptance, and in many ways it has considerable export significance. In recent years there has been growing disquiet that the education, training and status of our engineers at large, may not be as satisfactory as had been so tacitly assumed. The result of initiatives taken by the Institution of Electrical Engineers to tackle this problem, in the sphere of electrical and electronic engineering education, was the Merriman Report[1]. More recently the Finniston Inquiry has made its report on the larger problem of the whole of engineering education and training.

It is an inevitable result of such investigations that certain general principles are enunciated and some overall goals are stipulated, but the implementation of these remains very much a local problem. In practice the translation into actuality may prove to be a somewhat painful and major upheaval. However, the mere fact that such initiatives cause us to examine our educational methods with a critical eye is in itself beneficial. Nowhere is this more true than in electronic engineering. Rapidly advancing technology needs to be communicated to students in the right context and against the right background. It is all too easy to add on 'frill-thrill' courses and convince ourselves that we are up-to-date. The mature educator must from time to time examine the core material in the light of current developments, and seek to develop a coherent story so that the freshly-educated engineer is able to comprehend the significance of new developments and assess their significance with respect to immediate and future needs.

It had become increasingly obvious that the preparation of engineers to assume the highest levels of design and development roles in industry was going to require higher-grade courses at university. It is also true that not all students would be able to cope with such courses and it would be unwise to produce overqualified graduates for certain positions. Hence the emergence of multilevel degree courses of varying length and content. At the present time it is not easy to predict the exact nature and style of the various options. But for the

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This paper was first presented at the *Conference on Electronic Engineering in Degree Courses — Teaching for the 80's* at the University of Hull, England, in March 1980.

sake of stability within departments during the transition period, which may last a number of years, some concrete plans have to be made and adhered to.

Since the degree courses in electronic engineering at the University of Hull had traditionally consisted of four years full-time study, it was somewhat logical to consider the pursuance of the proposals for 'enhanced' degrees where the basic academic unit was four years in length.

2 BASIC ELEMENTS OF ENHANCEMENT

Following the Merriman Report, the I.E.E. issued a guide[2] outlining the contents of degree courses in electrical and electronic engineering, which would be the normal route to qualification as a chartered engineer in the future. The salient points are listed and the ensuing course proposals are an attempt to implement these in the light of local circumstances and resources.

(i) The complete course will be about five years in duration.
(ii) The enhanced course will contain 20–30% more academic material than existing undergraduate courses.
(iii) The industrial involvement will be of about 18 months' duration.
(iv) There will be close links between the educational establishment and employers of electronic engineers. A proper integration of practical and theoretical studies is sought, with no rigid separation of industrial and academic aspects of engineering.
(v) The course should contain topics such as industrial organisation, communication and man-management skills.
(vi) The major technical components of the course will be supported by suitable practical and project work, and contain elements of the design approach.
(vii) The entry grades of A-level (General Certificate of Education, Advanced Level) candidates should total nine points or over, equivalent requirements being demanded for other qualifications.

Superimposed upon these requirements are extra ones felt to be necessary for the complete operation of the courses in the university environment.

(a) The course should offer some degree of choice of specialisation at the highest level possible.
(b) There should be adequate provision for those students who find the enhanced course studies too demanding, and need a safety net of a Pass Degree course of non-enhanced standard.
(c) It is not at all clear that overseas students will wish to complete the full enhancement requirements, and provision for a non-enhanced alternative is necessary.

3 PROPOSED COURSE STRUCTURE

Fig. 1 shows a schematic diagram of the structure of the course. Points to note are the escape routes at the end of the second and third years of academic work, on to the non-enhanced Pass course. The industrial experience component is satisfied by periods in industry during the third and fourth years and

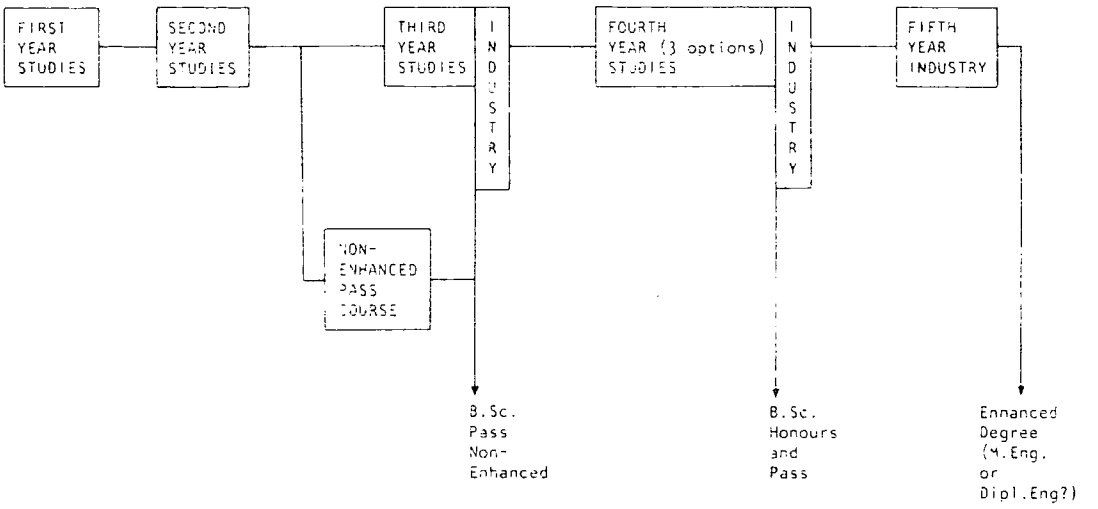

FIG. 1 Enhanced degree scheme.

by a complete year during the fifth year. The fourth year of academic study offers three options to the student, who can specialise in communications, automatic control or computer engineering. On completion of the fourth year, the B.Sc. degree is awarded with the usual gradings of Honours and Pass categories. Overseas students and those not wishing to proceed to full enhancement may terminate at this point. To complete the enhanced course, students must submit a dissertation on their industrial training and experience at the end of the fifth year, when the fully enhanced degree will be awarded (Dipl.Eng., M.Eng. or whatever).

The complete details of the academic content of each year are shown in Figs. 2 and 3. It is perhaps easiest to consider each year as consisting of a block of basic subjects, which begin with the foundations of electronic and mathematical studies and develop in natural progression. Hence, in the first year this comprises mathematics, combinational logic and integrated logic circuits, computer appreciation, electronic circuits, circuit theory, electromagnetics, system dynamics, mechanics and engineering drawing. Core subjects in the

FIRST YEAR	SECOND YEAR	THIRD YEAR
Mathematics	Electronic Systems and Feedback	Digital Electronics
Combinational Logic and Integrated Logic Circuits	Electronic Devices	Micro Computer Systems
Computer Appreciation	Introductory Telecommunications	Telecommunications
Electronic Circuits	Network Analysis	Systems Theory
Circuit Theory	Electromagnetism	Automatic Control
Electromagnetics	Digital Electronic Systems	Aerials, waveguides, Transmission Lines, Optical Waveguides
System Dynamics	Practical Circuit Design	Mathematics
Atomic Physics	Mathematics	Signals Analysis
Mechanics	Computer Programming	Design Engineering
Engineering Drawing	Business Studies	Business Studies
Technical Communication	Engineering and Environment	Laboratory work
Industrial Processes and Design	Solid State Technology	
BASIC Programming	Laboratory Work	
Laboratory work		

FIG. 2 Course outline for first three years of study.

B.Sc.(HONS) ELECTRONIC COMMUNICATIONS ENGINEERING	B.Sc.(HONS) ELECTRONIC CONTROL AND ROBOT ENGINEERING	B.Sc.(HONS) MICROELECTRONIC AND COMPUTER ENGINEERING
Passive Network Synthesis Active Network Synthesis Information Theory and Coding Digital Communications Microwave Techniques Radar Systems Communication Systems and Satellites Digital Filters and Signal Processing Engineering Management Project	Multivariable Control Systems Digital Filters and Signal Processing Advanced Techniques in Control Actuators and Sensory Feedback Robot Applications and System Design Non-linear Systems Software Engineering High Level Software Systems Engineering Management Project	Advanced Logic Systems Computer Architecture Microprocessor System Design Software Engineering High Level Software Systems Information Theory and Coding Digital Communications Digital Filters and Signal Processing Engineering Management Project

FIG. 3 Course outline of options available in fourth year of study.

second year are electronic systems and feedback, electronic devices, introductory telecommunications, network analysis, electromagnetism, digital electronic systems, mathematics, and solid state technology. In the third year these are digital electronics, microcomputer systems, telecommunications, systems theory, automatic control, aerials, waveguides, transmission lines, optical waveguides, mathematics and signals analysis. The fourth year presents three options of electronic specialisation with a few subjects common to two or more options.

Added to the basic core are other essential and interlinking features which progress from year to year. Fig. 4 shows the practical and project content. The proportion of project work is increased steadily year by year until in the fourth year each student undertakes a major project investigation which may be directly related to an industrial problem. Fig.5 displays the influence of the computer in electronic engineering education. It is necessary now, more than ever[3], to ensure the correct balance of these studies. All graduates should feel competent in using both general machines for problem solving and the more

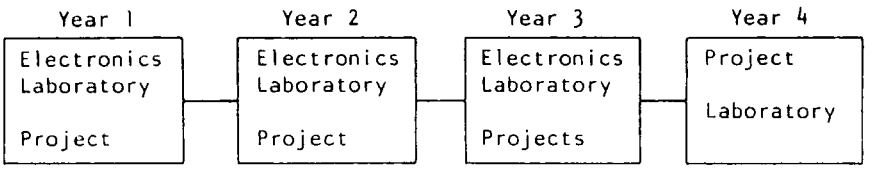

FIG. 4 Laboratory and project work scheme.

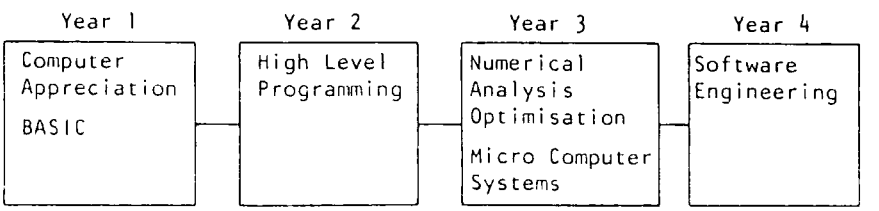

FIG. 5 Computer education scheme.

dedicated system for particular application resulting from microprocessors. Hence the teaching of BASIC not only serves as an introduction to programming, but has greater significance at a later stage in specific machine controlled systems. In the third year there is an interesting balance between essential computer mathematics such as numerical analysis and optimisation, and microprocessor programming and operating systems. Low level software is taught to some options in the fourth year.

An important feature of the course is the integration of lectures given by industrialists. This is shown for the various years in Fig. 6. Some subjects are of a general nature whereas others draw upon specialised knowledge available only from engineers actively engaged in the industrial scene. A considerable amount of liaison already exists in the project work attempted by the fourth year students. The design concept features heavily in this area of the course.

Finally, the business aspects of the course are shown in Fig. 7. Some of these subjects are common with the last grouping. Business studies includes such subjects as the balance sheet, work trees, cash flow, and marketing; it is completed by a substantial business game on the computer.

4 CONCLUSIONS

There is a sense in which engineering degree courses have never been easy. They have always covered a wide range of introductory subjects and therefore the workload imposed on students is usually heavier than in some other disciplines. Fortunately these aspects have not proved completely unacceptable in the past, since the motivation provided by vocational studies tends to prevail. It is essential however, when attempting to implement the proposals for enhancement, to maintain a correct balance of subjects in such a manner that the student can recognise that his specialised technical knowledge is expanding at a rate which exceeds his growing appreciation of general engineering ambience. The problem is nowhere more critical than in electronic engineering where there is the constant pressure of new technology. But what value is this

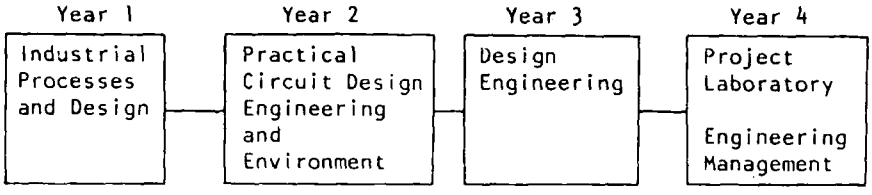

FIG. 6 Industrial lecturers' input.

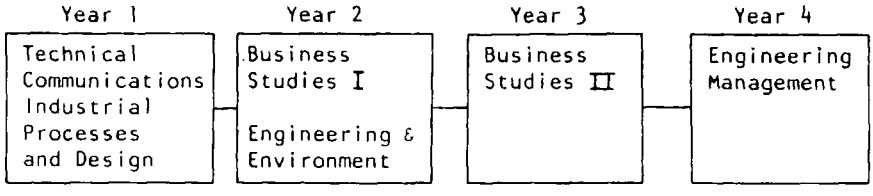

FIG. 7 Business elements of course.

knowledge if no-one is capable of manufacturing and marketing the product? If the student engineer can be educated in a more complete manner, without danger of overload, then the future is a bright one, provided he can be subsequently employed in a stimulating and demanding industrial environment. Unfortunately many modern changes in education have actually resulted in diluting the standards of entry, teaching and examination; to go forward without care and vigilance by the universities and the professional bodies could reduce even the most laudable schemes to little more than a shroud for compromise and failure.

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ABSTRACTS-ENGLISH, FRENCH, GERMAN, SPANISH

A degree-enhancement scheme in electronic engineering

A scheme is outlined which has a five year structure, with a fully integrated academic and industrial training programme. The academic content is discussed in detail and includes main core subjects, laboratory and project work, computer education, industrial lecturers' input and business elements of the course.

Un cours de degré élevé en ingéniérie électronique

Le schéma d'un cours est esquissé, d'une durée de cinq ans, suivant un programme complètement intégré du point de vue académique et apprentissage industriel. Le contenu académique est discuté en détails et comprend les sujets principaux, les laboratoires et projets, l'informatique, les données relatives aux conférenciers industriels et les éléments commerciaux du cours.

Ein Projekt zur Graderhöhung in der elektronischen Technik

Das umrissene Projekt hat eine 5-Jahr-Struktur mit einem völlig integrierten akademischen und industriellen Ausbildungsprogramm. Der akademische Inhalt wird im einzelnen besprochen; er schliesst die hauptsächlichen Stammfächer, Labor- und Projektarbeiten, Computerunterricht, Beiträge von Lehrern aus der Industrie und wirtschaftliche Elemente des Kursus ein.

Un plan de intensificación gradual en ingenieria electrónica

Se perfila un plan, estructurado en cinco años, en el que se integra completamente un programa de entrenamiento industrial y académico. Se discute con detalle el contenido académico del curso: los temas principales, los trabajos de laboratorio y proyecto, la formación en computadores, las intervenciones de los profesores de la industria y los conocimientos elementales sobre negocios.

9. Papers under Review

PAPER 56

EFFICIENT DESIGN OF LADDER-BASED ACTIVE FILTERS AND EQUALISERS

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ABSTRACT

Ladder-based active filters continue to attract attention from designers because of their low sensitivity property. In this paper matrix methods for ladder-based-filter and equaliser design are outlined. A modified and extended canonical realisation is presented and applied to active-RC, SC and transconductor-capacitor filter design. A filter and equaliser compiler based on the proposed method is described. As an example, a 5th-order Elliptic lowpass filter and a 6th-order group delay equaliser have been designed. It is shown that the order of the equaliser can be reduced by the application of special techniques for the approximation of the filter transfer function. The comparison of sensitivity between a cascade of biquadratic stages and the ladder-based realisation is given. Lower sensitivities to component tolerance for both filter and equaliser are displayed by the ladder-based design. The test results of the designed filter and equaliser are also given.

1. INTRODUCTION

The oldest and probably best known method of active filter design is a cascade approach. This commences by factorising a prescribed high-order transfer function into a product of second-order terms, which are then realised by an appropriate choice of active biquadratic sections. This method offers many attractions; principally it is straightforward to implement and various practical circuit requirements are almost automatically satisfied, such as dynamic range scaling which can be ensured by simple voltage or current scaling in each section, and in SC realisations the capacitance spread is generally quite modest. Consequently, many of the filter compilers available[1] adopt this approach as standard. However for high order monolithic filters, the cascading of biquadratic sections leads to an unacceptably high sensitivity of the response to component parameter variations. It is well known that appropriately designed LC ladders have very low sensitivities to component tolerance and hence active filters simulating the internal workings of doubly terminated RLC ladder prototypes are widely used in high precision integrated filters. Passive ladder prototypes for standard lowpass approximations are readily available from filter tables and component values of all other types of frequency response (bandpass, bandstop and highpass) can be obtained by applying standard frequency transformation and scaling

methods. Alternatively, computer programs can be used to generate a passive ladder automatically for more general approximations. Various techniques have been introduced which allow the expert user to optimise the prototype ladder development in order to reduce the component spread and sensitivity of the subsequent active realisation. The prototype ladder can often become unrealisable in passive terms, but still have feasible high performance active implementations.

Progress from a prototype ladder to an active realisation can follow "direct " simulation, when unwanted elements such as inductance or resistance are replaced by simulated elements, or "signal flow graph" simulation which involves the representation of selected currents and voltages (or combinations) of the prototype by proportionate voltages, currents or charges in the active circuit. A powerful matrix based approach[2] has been developed recently and applied to the design of SC, active-RC, and digital ladder filters and equalisers. In the case of SC filters this has led to configurations which are far from intuitively obvious but which offer improved performance with respect to parameters such as settling time and capacitance spread. The matrix approach has also been used to develop novel filter structures, ideally suited for transconductor-C realisation[5].

This paper presents various solutions to the problem of efficient active realisation of ladder-based designs. One difficulty concerning canonic realisation of certain filter functions has been recognised previously[6]; here, a general solution and a wide range of its implementations are examined. The application of advanced approximation techniques[7] also permits minimal realisations and improved performances in filter/equaliser design. The filter compiler incorporating these techniques is demonstrated and results from a fabricated video filter and group delay equaliser are presented.

2. REVIEW OF MATRIX BASED FILTER AND EQUALISER DESIGN METHODS FOR ACTIVE CIRCUITS

A passive ladder can be represented by the standard nodal admittance matrix equation

$$\mathbf{J} = (\mathbf{G}+s\mathbf{C}+s^{-1}\Gamma)\mathbf{V} \qquad (1)$$

Where **V** is a vector representing the nodal voltages and **J** is a vector representing the input current sources. **G**,**C**, and Γ are admittance matrices formed by the contributions of resistors, capacitors and inductors respectively. Equation (1) represents a set of equations of second order in the Laplacian variable s. It is well known that a set of linear first order algebraic equations can represent a signal flow graph and be realised by active building blocks[8]. The matrix method[2] enables direct decomposition of the second order matrix

to give two inter-related first order equations, and these first order systems are then directly implemented using the active building blocks.

2.1) Matrix methods for Active-RC Ladder-Based Filter Design

Either the $\mathbb{C}$ or the Γ matrix can be factorised, leading to left and right decompositions respectively.

Factorise the $\mathbb{C}$ into

$$\mathbb{C} = \mathbb{C}_l \mathbb{C}_r \tag{2}$$

The following pair of equations is equivalent to (1)

$$(s^{-1}\Gamma + \mathbf{G})\,\mathbf{V} + \mathbf{C}_l\mathbf{W} = \mathbf{J} \tag{3a}$$

$$\mathbf{C}_r\,\mathbf{V} - s^{-1}\mathbf{W} = \mathbf{0} \tag{3b}$$

where $\mathbf{W}$ is the vector of intermediate variables.This decomposition is called *RC Left Decomposition*. The actual methods employed to perform the decomposition indicated in equation (2) are those commonly known to preserve the sparsity of the matrices: LU, UL and the direct methods which decompose any matrix A into **AI** or **IA**[2].

If Γ is factorised as

$$\Gamma = \Gamma_l \Gamma_r \tag{4}$$

then the *RC Right Decomposition* method is obtained and the following pair of equations is equivalent to (1)

$$(\mathbf{C} + s^{-1}\mathbf{G})\mathbf{V} + s^{-1}\Gamma_l\mathbf{W} = s^{-1}\mathbf{J} \tag{5a}$$

$$-s^{-1}\Gamma_r\mathbf{V} + \mathbf{W} = \mathbf{0} \tag{5b}$$

For the above decompositions, in order to maintain the sparsity of the matrix, no matrix inverse is involved. If inverse matrix is used in the design process, some special circuits can be obtained.

RC Left Inverse Decomposition

If the auxiliary variables are defined by $\mathbf{W} = s\mathbf{C}\mathbf{V}$ and (3b) is multiplied by $\mathbf{C}^{-1}$ then the design equations become

$$(s^{-1}\Gamma + \mathbf{G})\mathbf{V} + \mathbf{W} = \mathbf{J} \quad (6a)$$

$$\mathbf{V} - \mathbf{C}^{-1}s^{-1}\mathbf{W} = \mathbf{0} \quad (6b)$$

RC Right- Inverse Decomposition

Choosing $\mathbf{W} = s^{-1}\Gamma\mathbf{V}$ and multiplying (5b) by Γ^{-1} the system equations become

$$(\mathbf{C} + s^{-1}\mathbf{G})\mathbf{V} + s^{-1}\mathbf{W} = s^{-1}\mathbf{J} \quad (7a)$$

$$-s^{-1}\mathbf{V} + \Gamma^{-1}\mathbf{W} = \mathbf{0} \quad (7b)$$

The equations (3,5,6,7) are equivalent to (1). Each set can be realised by active-RC circuits. In these equations the matrix multiplied by s^{-1} is called integrated matrix and it will be observed that in the active-RC circuit realisation, the entries in the integrated matrices are realised by resistors and the entries in non-integrated matrices are identified with capacitors. It can be shown that equation (6) yields a minimum capacitor realisation while (7) produces a minimum resistor realisation[2].

2.2) Matrix Methods for SC Ladder-Based Filter Design

The design of a switched-capacitor filter starts from the prototype system equation (1), which after bilinear transformation becomes

$$\left[\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}\mathbf{C} + \frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}}\Gamma + \mathbf{G}\right]\mathbf{V} = \mathbf{J} \quad (8)$$

Rearranging gives

$$\left[\frac{1}{\psi}\mathbf{A} + \phi\mathbf{B} + \mathbf{D}\right]\mathbf{V} = \mathbf{J}(1+z) \quad (9)$$

$$\left[\frac{1}{\phi}\mathbf{A} + \psi\mathbf{B} + \mathbf{D}\right]\mathbf{V} = \mathbf{J}(1+z^{-1}) \quad (10)$$

where

$$\mathbf{A} = 2\mathbf{C}/T + T\Gamma/2 + \mathbf{G} \text{ for left matrix decomposition} \quad (11a)$$

$$\mathbf{A} = 2\mathbf{C}/T + T\Gamma/2 - \mathbf{G} \text{ for right matrix decomposition} \quad (11b)$$

$$\mathbf{B} = 2T\Gamma \quad (11c)$$

$$\mathbf{D} = 2\ \mathbf{G} \quad (11d)$$

$$\Phi = 1/(1-z^{-1}) \quad (11e)$$

$$\Psi = z^{-1}/(1-z^{-1}) \quad (11f)$$

The bilinear transformation has the advantage of both stability and exactness. Unfortunately, bilinear integrators are sensitive to the stray capacitance and are not practically useful. Instead a modified SC ladder-based structure utilising LDI integrators[2] can be formed.

Factorise the matrix **A** and the *SC Left Decomposition* is obtained as

$$(\Phi\mathbf{B}+\mathbf{D})\mathbf{V} + \mathbf{A}_l\mathbf{W} = 2\mathbf{J} \quad (12a)$$

$$\mathbf{A}_r\mathbf{V} + \Psi\mathbf{W} = \mathbf{A}_l^{-1}\mathbf{J} \quad (12b)$$

Factorise the matrix **B** and the *SC Right Decomposition* is obtained as

$$(\mathbf{A} + \Phi\mathbf{D})\mathbf{V} + \mathbf{B}_l\mathbf{W} = -\mathbf{J} \quad (13a)$$

$$-\Psi\mathbf{B}_r\mathbf{V} + \mathbf{W} = -2\mathbf{B}_l^{-1}\mathbf{J} \quad (13b)$$

Again, the standard numerical techniques for matrix decomposition of **A** or **B** yield a range of circuit implementations whose suitability in various applications have been examined[2]. For the sake of completeness, the two inverse decompositions are shown, though no economical SC circuits are known to result from their application.

SC Left Inverse Decomposition

$$(\Phi\mathbf{B} + \mathbf{D})\mathbf{V} + \mathbf{W} = (1+z)\mathbf{J} \quad (14a)$$

$$\mathbf{V} + \Psi\mathbf{A}^{-1}\mathbf{W} = \mathbf{0} \quad (14b)$$

SC Right Inverse Decomposition

$$(\mathbf{A} + \Phi\mathbf{D})\mathbf{V} + \Phi\mathbf{W} = \mathbf{J}(1+z^{-1})/(1-z^{-1}) \quad (15a)$$

$$-\Psi\mathbf{V} + \mathbf{B}^{-1}\mathbf{W} = \mathbf{0} \quad (15b)$$

Generally the SC Left Decompositions demonstrate excellent properties regarding component spread and dynamic range for bandpass designs. However, these structures sometimes need more opamps in circuit realisation. They are not suitable for lowpass filter design because of a peak in sensitivity at zero frequency.

The SC Right Decomposition approaches can demand fewer opamps in circuit realisation and they demonstrate good sensitivity performance for lowpass designs. Undesirably large component spread and poor dynamic range are unfortunately observed for certain bandpass designs.

2.3) Matrix Methods for Transconductor-C Ladder-Based Filter Design

There are two main types of ladder-based transconductor-capacitor canonical filter realisations, these are due to Topological Decomposition and Inverse Decomposition. Inverse Decomposition is again divided into Right and Left Inverse Decomposition. The building blocks for circuit realisation utilise both conventional transconductors Fig.1(a) and low impedance input transconductors[9] Fig.1(b). In Fig.1(a) the capacitor C_j can only realise a bidirectional path when driven by internal nodes. To facilitate the realisation of some decompositions, low impedance input transconductors or transconductor/opamp stages are required, these also have the added attraction of nullifying the effects of parasitic capacitance.

TC Topological Decomposition

In the topological decomposition,

$$\Gamma=\mathbf{A}\mathbf{D}\mathbf{A}^{T} \tag{16}$$

where **D** is a diagonal matrix of the inverse inductance values of the prototype, **A** is a conventional incidence matrix of inductors. The auxiliary variables are defined by:

$$\mathbf{W}=(sg)\text{-}1\mathbf{D}\mathbf{A}^{T}\mathbf{V} \tag{17}$$

where g is a scaling factor with the dimension of transconductance, often set as $g=1/\alpha R$ where the R is the ladder filter terminal resistor and α takes an optimum value close to the fractional bandwidth of the filter.

Substituting (16) and (17) into (1) and rearranging gives

$$s^{-1}g^2\mathbf{A}\mathbf{W} + (g\mathbf{C}+s^{-1}g\mathbf{G})\mathbf{V} = s^{-1}g\mathbf{J} \quad (18a)$$

$$g\mathbf{D}^{-1}\mathbf{W} + s^{-1}\mathbf{A}^T\mathbf{V} = \mathbf{0} \quad (18b)$$

If the prototype ladder is equally terminated, the filter can be realised with one value of transconductance. In a transconductor-capacitor realisation, the entries in non-integrated matrices are realised by capacitors while the components in integrated matrices are implemented by transconductances. All non-integrated matrices in the Topological Decomposition are symmetrical, so realisation can utilise both conventional and low impedance input transconductor structures. The auxiliary voltages **W** are directly proportional to the currents in the inductors of prototype ladder. The topological decomposition will generally lead to equivalent leapfrog topologies in active-RC and SC and transconductance-capacitor designs, if conventional transconductors are used. In the bandpass case, this decomposition cannot be guaranteed to generate stable active circuits and alternative decompositions are required[5].

TC Right Inverse Decomposition

The auxiliary variables are defined by

$$\mathbf{W}=(s^{-1}\Gamma\mathbf{V})/g \quad (19)$$

The resulting design matrix equations are:

$$g\Gamma^{-1}\mathbf{W} - s^{-1}\mathbf{V} = \mathbf{0} \quad (20a)$$

$$s^{-1}g^2\mathbf{W} + (g\mathbf{C} + s^{-1}g\mathbf{G})\mathbf{V} = s^{-1}g\mathbf{J} \quad (20b)$$

In (20b), the integrated vector V is premultiplied by the matrix **G**. Only when the prototype ladder has equal resistance at both terminations, would the transconductor-capacitor filter require one transconductance value in the complete realisation. Because all the non-integrated matrices in TC Right Inverse Decomposition are symmetrical, it can be realised both using conventional transconductor and low impedance input transconductor building blocks.

TC Left Inverse Decomposition

The Left Inverse Decomposition results from decomposing the **C** matrix into two matrices as (2). Defining the vector of auxiliary variables by

$$\mathbb{W} = (s\mathbb{C}_r\mathbb{V})/g \tag{21}$$

The general *TC Left Inverse Decomposition* design equations are obtained by substituting (21) into (1) and rearranging:

$$g^2\Gamma^{-1}\mathbb{C}_l\mathbb{W} + (s^{-1}g + g\Gamma^{-1}\mathbb{G})\mathbb{V} = g\Gamma^{-1}\mathbb{J} \tag{22a}$$
$$-s^{-1}g\mathbb{W} + \mathbb{C}_r\mathbb{V} = \mathbb{0} \tag{22b}$$

Only low impedance input transconductors can be used in the realisation of Eq.(22a,b), because some of the non-integrated matrices are asymmetric. For $\mathbf{C}_l = \mathbf{I}$ and $\mathbf{C}_r = \mathbf{C}$, the *TC Left-IC Decomposition* can be obtained from (22a,b) as:

$$g^2\Gamma^{-1}\mathbf{W} + (s^{-1}g + g\Gamma^{-1}\mathbf{G})\mathbf{V} = g\Gamma^{-1}\mathbf{J} \tag{23a}$$
$$-s^{-1}g\mathbf{W} + \mathbf{C}\mathbf{V} = \mathbf{0} \tag{23b}$$

Since Γ^{-1} and $\mathbf{C}$ are generally full and tridiagonal respectively, a relatively large number of capacitors is required in the circuit realisation. However since all non-integrated matrices ($\Gamma^{-1}\mathbf{G}$ and $\mathbf{C}$) are symmetric, they can be implemented using conventional transconductors.

When $\mathbf{C}_l = \mathbf{C}$ and $\mathbf{C}_r = \mathbf{I}$, the *TC Left-CI Decomposition* is obtained:

$$g^2\Gamma^{-1}\mathbf{C}\mathbf{W} + (s^{-1}g + g\Gamma^{-1}\mathbf{G})\mathbf{V} = g\Gamma^{-1}\mathbf{J} \tag{24a}$$
$$-s^{-1}g\mathbf{W} + \mathbf{V} = \mathbf{0} \tag{24b}$$

This requires fewer capacitors than Left-IC because the only coupling capacitors are those of the product matrix $\Gamma^{-1}\mathbf{C}$, these coupling paths must be implemented using low impedance inputs since $\Gamma^{-1}\mathbf{C}$ is generally asymmetric. A singularly good application [5] of this decomposition is for prototypes where $\mathbf{C} = \Gamma$, when $\Gamma^{-1}\mathbf{C}=\mathbf{I}$ which is very sparse and symmetric, and produces a highly efficient realisation with conventional transconductors.

The important feature of equations (22-24) is that all of the integrated vectors are multiplied by a single constant g, this allows the equations to be implemented as a transconductor-capacitor circuit with a single value of transconductance.

2.4) Allpass Ladder-Based Transconductor-Capacitor Design

The equalisation of group delay is becoming increasingly important with high frequency applications such as video communication systems. In analogue systems this equalisation is often provided by one or more allpass biquadratic stages. However, where the equaliser required is of order greater than two, sensitivity considerations would indicate that it is preferable to use a ladder derived circuit. A ladder-based technique has been developed for digital implementation[10] and extended to SC realisations[11]. It is essential to incorporate the advantages of this approach into the design of transconductor-C equalisers for direct application in high frequency environments.

Consider allpass transfer functions of the form

$$H(s) = k\frac{P(-s)}{P(s)} \tag{25}$$

where P(s) is Hurwitz polynomial of order n and k = 1 if n is odd order and k = -1 if n is even. The polynomial P(s) is separated into odd and even parts:

$$P(s) = E(s) + O(s) \tag{26}$$

Define

$$Y(s) = \begin{cases} \dfrac{E(s)}{O(s)} & \text{if n is even} \\ \dfrac{O(s)}{E(s)} & \text{if n is odd} \end{cases} \tag{27}$$

Substituting (26) and (27) into (25) gives

$$H(s) = \frac{1 - Y(s)}{1 + Y(s)} = 1 - \frac{2}{1 + Y(s)} \tag{28}$$

Since P(s) is Hurwitz, Y(s) can be expanded as a continued fraction, and equation (28) can then be realised as the combination of a singly terminated RLC ladder and an active summing stage. The singly terminated passive ladder network part can be simulated by a transconductor-C circuit using the above matrix decomposition method and the overall transconductor-C group delay equaliser structure is shown in Fig.2.

3. CANONICAL REALISATION FOR LADDER-BASED DESIGN

An analogue VLSI design is a multiple criteria optimisation procedure. One objective in this procedure is to use a minimum number of active components, since these usually occupy relatively large area, consume power, and are sources of noise. With the development of personal communication equipment, these considerations will assume even more importance in VLSI circuit design. In active-RC and SC filter design, it is generally accepted that one-opamp-per-pole realisations are canonical for low sensitivity realisation. Circuit configurations with less than one opamp per pole are usually quite sensitive to component deviations, and in the SC case, they would usually require more switches, capacitors, and clock waveforms. For transconductor-C filter ladder-based realisations with conventional transconductors, two extra transconductors are needed for realisation of the passive prototype ladder terminations. We define ***a canonical transconductor-C filter with conventional transconductors as a one-transconductor-per-pole realisation plus two termination transconductors, each possessing the same value of transconductance. A transconductor-C filter with conventional transconductors, which has one-transconductor-per-pole and two termination transconductors, with a small number ($\leq$ 3) of different transconductance values, is defined as quasi-canonical realisation.*** If the transconductor-C filter is realised using low impedance transconductors, two transconductors for the termination realisation can be replaced by capacitance branches. Therefore we define ***a canonical transconductor-C filter with low impedance input transconductors as a one-transconductor-per-pole realisation, each possessing the same value of transconductance. A transconductor-C filter with low impedance input transconductors, which has one-transconductor-per-pole, with a small number ($\leq$ 3) of different transconductance values, is defined as quasi-canonical realisation.***

Previous work has shown that the problem of finding a canonical ladder-based active filter can be solved by finding a canonical ladder prototype[6]. The conditions required for a transfer function to be realisable by a canonical doubly-terminated ladder are that numerator of the transfer function of a canonical even-order doubly-terminated ladder is an odd polynomial, and that the numerator of the transfer function of an odd-order doubly-terminated ladder is an odd polynomial if $|C|$ is non-singular or an even polynomial if $|\Gamma|$ is non-singular. For most filter design problems the numerator of the transfer functions are polynomials with purely even or odd terms. So the numerator parity alone determines where a given transfer function can be realised by a canonical ladder. The solution is to augment the transfer function, unrealisable by canonical ladder, to produce a transfer

function which is realisable by canonical ladder, and when the ladder is simulated by an active circuit the original transfer function behaviour is then restored by a change in input circuitry. If H(s) is a transfer function with all its zeros on the imaginary axis or at infinity, then parity manipulation can be effected by s, 1/s, $s/(s^2+\omega_i^2)$. The parity of the modified transfer function H'(s) facilitates realisation by a canonical prototype ladder. A system realising the original transfer function H(s) can be obtained by multiplying the input vector $\mathbb{J}$ by the inverse of the modifying function.

$$(sC+s^{-1}\Gamma + G)V=s^{-1}\mathbb{J} \quad (29a)$$
$$(sC+s^{-1}\Gamma + G)V=sJ \quad (29b)$$
$$(sC+s^{-1}\Gamma + G)V=(s+\omega_i^2 s^{-1})J \quad (29c)$$

3.1) Canonical Ladder Simulation By Active-RC Circuits

In an active-RC circuit realisation, for *RC Left Decomposition* form, the system (29a-c) can be decomposed in the following ways.

$$C_l W + (s^{-1}\Gamma + G)V = s^{-1}J \quad (30a)$$
$$-s^{-1}W + C_r V = 0 \quad (30b)$$

$$C_l W + (s^{-1}\Gamma + G)V = 0 \quad (30c)$$
$$-s^{-1}W + C_r V = C_l^{-1}J \quad (30d)$$

$$C_l W+(s^{-1}\Gamma+G)V=\omega_i^2 s^{-1}J \quad (30e)$$
$$-s^{-1}W+C_r V=C_l^{-1}J \quad (30f)$$

Now canonical active-RC networks can be obtained directly from equations (30). These circuits use n opamps, where n is the order of original transfer function H(s). The coefficients of s^{-1} on the right-hand-side of the equations are implemented by resistors. The different parity arrangements and decompositions available lead to different circuit realisation efficiency. Eq.(30a,b) produce the same topological structure as the original one, the only difference is that the input capacitance is changed to resistance. Analysis of Eq.(30c,d) and (30e,f) shows that canonical realisation generally leads to the introduction of extra passive components. However, if UL or IA decompositions are used, the number of input branch elements can be minimised. For those two decompositions, only the input node is changed in case Eq.(30c,d) or one additional resistor is added in case (30e,f). If other decompositions are used, they can introduce up to N (number of nodes in prototype ladder) extra input capacitor or resistor branches.

For *RC Right Decomposition*, the systems take the form

$$(\mathbb{C} + s^{-1}\mathbb{G})\mathbb{V} + s^{-1}\Gamma_l\mathbb{W} = \mathbb{0} \quad (31a)$$
$$-s^{-1}\Gamma_r\mathbb{V} + \mathbb{W} = -s^{-1}\Gamma_f^{-1}\mathbb{J} \quad (31b)$$

$$(\mathbb{C} + s^{-1}\mathbb{G})\mathbb{V} + s^{-1}\Gamma_l\mathbb{W} = \mathbb{J} \quad (31c)$$
$$-s^{-1}\Gamma_r\mathbb{V} + \mathbb{W} = \mathbb{0} \quad (31d)$$

$$(\mathbf{C} + s^{-1}\mathbf{G})\mathbf{V} + s^{-1}\Gamma_l\mathbf{W} = \mathbf{J} \quad (31e)$$
$$-s^{-1}\Gamma_r\mathbf{V} + \mathbf{W} = -s^{-1}\Gamma_f^{-1}\omega_i^2\mathbf{J} \quad (31f)$$

Eq.(31c,d) demonstrates a very efficient canonical form with input branches changed from resistance to capacitance. The equations of (31a,b) and (31e,f) can only be efficiently realised by UL or IA decompositions, since $\Gamma_f^{-1}\mathbf{J}$ produces a vector with only one non-zero entry, which can be produced by one input branch only.

When *RC Left Inverse Decomposition* is used, the system is

$$\mathbf{W} + (s^{-1}\Gamma + \mathbf{G})\mathbf{V} = s^{-1}\mathbf{J} \quad (32a)$$
$$-s^{-1}\mathbf{C}^{-1}\mathbf{W} + \mathbf{V} = \mathbf{0} \quad (32b)$$

$$\mathbf{W} + (s^{-1}\Gamma + \mathbf{G})\mathbf{V} = \mathbf{0} \quad (32c)$$
$$-s^{-1}\mathbf{C}^{-1}\mathbf{W} + \mathbf{V} = \mathbf{C}^{-1}\mathbf{J} \quad (32d)$$

$$\mathbf{W} + (s^{-1}\Gamma + \mathbf{G})\mathbf{V} = \omega_i^2 s^{-1}\mathbf{J} \quad (32e)$$
$$-s^{-1}\mathbf{C}^{-1}\mathbf{W} + \mathbf{V} = \mathbf{C}^{-1}\mathbf{J} \quad (32f)$$

Equations (32a,b) can be very efficiently realised with the input branch changing from a capacitor to a resistor. Realisation of equations (32c, d) would introduce N extra capacitors, but without a resistive input branch. The system equations (32e,f) introduce N extra capacitors plus the original resistor input branch. In the case of (32c, d) and (32e,f), the characteristic minimum capacitor realisation of *RC Left Inverse Decomposition* would be lost.

For RC *Right Inverse Decomposition* the system is rewritten as

$$(\mathbb{C} + s^{-1}\mathbb{G})\mathbb{V} + s^{-1}\mathbb{W} = \mathbb{0} \quad (33a)$$
$$-s^{-1}\mathbb{V} + \Gamma^{-1}\mathbb{W} = -s^{-1}\Gamma^{-1}\mathbb{J} \quad (33b)$$

$$(\mathbb{C} + s^{-1}\mathbb{G})\mathbb{V} + s^{-1}\mathbb{W} = \mathbb{J} \quad (33c)$$
$$-s^{-1}\mathbb{V} + \Gamma^{-1}\mathbb{W} = \mathbb{0} \quad (33d)$$

$$(\mathbb{C} + s^{-1}\mathbb{G})\mathbb{V} + s^{-1}\mathbb{W} = \mathbb{J} \quad (33f)$$
$$-s^{-1}\mathbb{V} + \Gamma^{-1}\mathbb{W} = -s^{-1}\Gamma^{-1}\omega_i{}^2\mathbb{J} \quad (33f)$$

Realisation of equations (33a,b) and (33e,f) would introduce N extra resistors. No capacitor input branch is needed in equations(33a,b) while one capacitor input is needed for (33e,f) realisation. Tl e minimum resistor feature may be lost in canonical realisation. Equations (33c,d) can be efficiently realised with only the change of the original resistive input branch to a capacitive one.

The following example illustrates the improvements possible. A 6th-order elliptic lowpass active-RC filter is designed using the canonical design method and left-UL decomposition. The simulated circuit response is shown in Fig.3, which exactly agrees with the approximation. The circuit realisation contains 6 opamps, 13 capacitors and 11 resistors. If a canonical design approach were not available, then a 7th-order elliptic active-RC would be necessary , requiring 8 opamps, 17 capacitors and 14 resistors.

3.2) Canonical Ladder Simulation by Switched-Capacitor Circuits

SC Left Decomposition canonical realisations for systems (29a), (29b) and (29c) become

$$\mathbf{A}_l\mathbf{W} + (\Phi\mathbf{B} + \mathbf{D})\mathbf{V} = 2\mathbf{T}\Phi\mathbf{J} \quad (34a)$$
$$-\Psi\mathbf{W} + \mathbf{A}_r\mathbf{V} = \mathbf{A}_l{}^{-1}\mathbf{T}\mathbf{J}/2 \quad (34b)$$

$$\mathbf{A}_l\mathbf{W} + (\Phi\mathbf{B} + \mathbf{D})\mathbf{V} = \mathbf{0} \quad (34c)$$
$$-\Psi\mathbf{W} + \mathbf{A}_r\mathbf{V} = 2\mathbf{A}_l{}^{-1}\mathbf{J}/\mathbf{T} \quad (34d)$$

$$\mathbf{A}_l\mathbf{W} + (\Phi\mathbf{B} + \mathbf{D})\mathbf{V} = 2\mathbf{T}\Phi\omega_i{}^2\mathbf{J} \quad (34e)$$
$$-\Psi\mathbf{W} + \mathbf{A}_r\mathbf{V} = \mathbf{A}_l{}^{-1}(\mathbf{T}\omega_i{}^2/2+2/\mathbf{T})\mathbf{J} \quad (34f)$$

The circuit realisation of Eq.(34a,b) and (34e,f) retains the basic topology with only the introduction of 2 more switches and 1 more capacitor. The circuit realisation of Eq.(34c,d)

is very efficient, since $\mathbb{J}$ has only one non-zero input and if A_l^{-1} is an upper triangular matrix, which occurs when UL or IA decompositions are selected, only one input branch is required.

SC Right Decomposition canonical realisation for systems (29a), (29b) and (29c) are

$$(\mathbb{A} + \Phi\mathbb{D})\mathbb{V} + \Phi\mathbb{B}_l\mathbb{W} = T\mathbb{J}/2 \quad (35a)$$
$$-\Psi\mathbb{B}_r\mathbb{V} + \mathbb{W} = -2T\Psi\mathbb{B}_l^{-1}\mathbb{J} \quad (35b)$$

$$(\mathbf{A} + \Phi\mathbf{D})\mathbf{V} + \Phi\mathbf{B}_l\mathbf{W} = 2\mathbf{J}/T \quad (35c)$$
$$-\Psi\mathbf{B}_r\mathbf{V} + \mathbf{W} = \mathbf{0} \quad (35d)$$

$$(\mathbf{A} + \Phi\mathbf{D})\mathbf{V} + \Phi\mathbf{B}_l\mathbf{W} = (T\omega_i^2/2+2/T)\mathbf{J} \quad (35e)$$
$$-\Psi\mathbf{B}_r\mathbf{V} + \mathbf{W} = -2T\Psi\mathbf{B}_l^{-1}\omega_i^2\mathbf{J} \quad (35f)$$

Eqns.(35a,b) and (35e,f) will yield identical topologies, having $2N$ more switches than a realisation based on Eq.(13a,b). However, Eqns.(35c,d) lead to a very efficient circuit realisation with N fewer capacitor input branches than demanded by Eqns.(13a,b; e,f).

The *SC Left Inverse Decomposition* canonical realisation form can be written as

$$\mathbf{W} + (\Phi\mathbf{B} + \mathbf{D})\mathbf{V} = 2T\Phi\mathbf{J} \quad (36a)$$
$$-\Psi\mathbf{A}^{-1}\mathbf{W} + \mathbf{V} = \mathbf{A}^{-1}T\mathbf{J}/2 \quad (36b)$$

$$\mathbf{W} + (\Phi\mathbf{B} + \mathbf{D})\mathbf{V} = \mathbf{0} \quad (36c)$$
$$-\Psi\mathbf{A}^{-1}\mathbf{W} + \mathbf{V} = 2\mathbf{A}^{-1}\mathbf{J}/T \quad (36d)$$

$$\mathbf{W} + (\Phi\mathbf{B} + \mathbf{D})\mathbf{V} = 2T\Phi\omega_i^2\mathbf{J} \quad (36e)$$
$$-\Psi\mathbf{A}^{-1}\mathbf{W} + \mathbf{V} = \mathbf{A}^{-1}(T\omega_i^2/2+2/T)\mathbf{J} \quad (36f)$$

The realisation of Eq.(36c,d) introduces N more capacitors, and Eq.(36a,b) and (36e,f) have same topologies which introduce $2(N-1)$ switches and $2N$ capacitors.

The *SC Right Inverse Decomposition* canonical realisation forms are

$$(\mathbf{A} + \Phi\mathbf{D})\mathbf{V} + \Phi\mathbf{W} = T\mathbf{J}/2 \quad (37a)$$
$$-\Psi\mathbf{V} + \mathbf{B}^{-1}\mathbf{W} = -2T\Psi\mathbf{B}^{-1}\mathbf{J} \quad (37b)$$

$$(\mathbb{A} + \Phi\mathbb{D})\mathbb{V} + \Phi\mathbb{W} = 2\mathbb{B}^{-1}\mathbb{J}/T \quad (37c)$$

$$-\Psi\mathbb{V} + \mathbb{B}^{-1}\mathbb{W} = \mathbb{0} \quad (37d)$$

$$(\mathbb{A} + \Phi\mathbb{D})\mathbb{V} + \Phi\mathbb{W} = (T\omega_i^2/2+2/T)\mathbb{J} \quad (37e)$$

$$-\Psi\mathbb{V} + \mathbb{B}^{-1}\mathbb{W} = -2T\Psi\mathbb{B}^{-1}\omega_i^2\mathbb{J} \quad (37f)$$

Eq.(37c,d) can produce an efficient circuit realisation and Eq.(37a,b) and (37e,f) have same topologies which have $2(N-1)$ more switches and N more capacitors.

The UL and IA decompositions are recommended for all cases of canonic SC filter design, since they minimise the number of the input branches significantly and generally produce efficient circuit configurations.

A typical 8th-order bandpass filter which satisfies the specification of a speech processing channel is designed by canonical techniques using the Left-UL decomposition. The simulated circuit response is shown in Fig.4 and closely agrees with the approximation. The design statistics for different circuit designs is given in Table I, and the sensitivity comparison of a ladder-based design and a cascade based design is given in Fig.5. The lower curve is the sensitivity characteristics of Left-UL realisation and the upper curve is the sensitivity characteristics of Sedra's[12] biquad cascade realisation. The index of multiparameter sensitivity is defined as

$$S(\omega) = 8.686\left\{\sum_i\left[\frac{c_i}{|H(\omega)|}\frac{\partial|H(\omega)|}{\partial c_i}\right]^2\right\}^{1/2} / 100.0$$

where C_i is an individual circuit capacitance.

	Left-UL	Left-IA	Right-UL	Right-IB	E-F Type[13]	Sedra
No. Opamps	8	8	8	8	8	8
No. C	32	32	32	32	28	28
No. SW	34	34	38	38	34	40
Total C	340.76	319.87	355.61	409.20	424.72	392.54
C Spread	57.57	54.31	56.15	53.97	77.26	72.93

Table I. Statistics of 8th-order SC bandpass filter realisation

3.3) Canonical Ladder Simulation by Transconductor-Capacitor Circuits

a)*TC Topological Decomposition*

The design equations for a canonical topological decomposition are

$$\mathbf{CV} = -s^{-1}[\mathbf{AgW} + \mathbf{GV}] \quad (38a)$$
$$\mathbf{W} = (sg)^{-1}[\mathbf{DA}^{T}\mathbf{V} - \mathbf{JA}^{-1}] \quad (38b)$$

$$\mathbf{CV} = s^{-1}[s\mathbf{J} - \mathbf{AgW} - \mathbf{GV}] \quad (38c)$$
$$\mathbf{W} = (sg)^{-1}\mathbf{DA}^{T}\mathbf{V} \quad (38d)$$

$$\mathbf{CV} = s^{-1}[s\mathbf{J} - \mathbf{AgW} - \mathbf{GV}] \quad (38e)$$
$$\mathbf{W} = (sg)^{-1}[\mathbf{DA}^{T}\mathbf{V} - \mathbf{JA}^{-1}\omega_i^{2}] \quad (38f)$$

The validity of these equations is dependent upon the matrix **A** being square and having an inverse, which is not usually the case. Even when A is square-invertable, the implementation of $s^{-1}\mathbf{A}^{-1}\mathbf{J}$ in Eq.(38b) and $s^{-1}\mathbf{A}^{-1}\omega_i^{2}\mathbf{J}$ in Eq.(38f) would introduce a extra *N* (dimension of **A** matrix) transconductors with different transconductance values, and this destroys the main advantage of a ladder-based transconductor-capacitor filter. However, Eq.(38c,d) will always yield an efficient circuit structure no matter what form **A** matrix assumes.

b) *TC Right Inverse Decomposition*

The canonical realisations are written as

$$\mathbf{CV} = -s^{-1}(\mathbf{GV} + g\mathbf{W}) \quad (39a)$$
$$\Gamma^{-1}\mathbf{W} = (sg)^{-1}(\mathbf{V} - \Gamma^{-1}\mathbf{J}) \quad (39b)$$

$$\mathbf{CV} = \mathbf{J} - s^{-1}(\mathbf{GV} + g\mathbf{W}) \quad (39c)$$
$$\Gamma^{-1}\mathbf{W} = (sg)^{-1}\mathbf{V} \quad (39d)$$

$$\mathbf{CV} = \mathbf{J} - s^{-1}(\mathbf{GV} + g\mathbf{W}) \quad (39e)$$
$$\Gamma^{-1}\mathbf{W} = (sg)^{-1}(\mathbf{V} - \omega_i^{2}\Gamma^{-1}\mathbf{J}) \quad (39f)$$

The terms $(sg)^{-1}\Gamma^{-1}\mathbf{J}$ in Eq.(39b) and $(sg)^{-1}\omega_i{}^2\Gamma^{-1}\mathbf{J}$ in Eq.(39f) can only be realised by N extra transconductors with different transconductance values. However for Eq.(39c,d), an efficient circuit realisation can be obtained.

c)*TC Left Inverse Decomposition*

Only the canonical realisation for Eq.(23) is given here, the other variations on the *TC Left Inverse Decomposition* method give exactly the same results. The canonical equations can be written as

$$\mathbf{CV} = s^{-1}g\mathbf{W} \tag{40a}$$
$$g^2\Gamma^{-1}\mathbf{W} = s^{-1}g\Gamma^{-1}\mathbf{J} - g\Gamma^{-1}\mathbf{GV} - s^{-1}g\mathbf{V} \tag{40b}$$

$$\mathbf{CV} = s^{-1}g\mathbf{W} + \mathbf{J} \tag{40c}$$
$$g^2\Gamma^{-1}\mathbf{W} = -g\Gamma^{-1}\mathbf{GV} - s^{-1}g\mathbf{V} \tag{40d}$$

$$\mathbf{CV} = s^{-1}g\mathbf{W} + \mathbf{J} \tag{40e}$$
$$g^2\Gamma^{-1}\mathbf{W} = s^{-1}g\Gamma^{-1}\omega_i{}^2\mathbf{J} - g\Gamma^{-1}\mathbf{GV} - s^{-1}g\mathbf{V} \tag{40f}$$

The terms $s^{-1}g\Gamma^{-}\mathbf{J}$ in Eq.(40b) and $s^{-1}g\Gamma^{-1}\omega_i{}^2\mathbf{J}$ in Eq.(40f) can only be realised by N extra transconductors with different transconductance values. Only Eq.(40c,d) can be realised by canonical form.

As an example, we consider the design of an 8th-order Butterworth bandpass transconductor-C filter. The transfer function for this filter is of the form

$$H(s) = \frac{s^4}{(s^2 + p_1^2)(s^2 + p_2^2)(s^2 + p_3^2)(s^2 + p_4^2)} \tag{41}$$

Because the transfer function has even order denominator with even order numerator, a canonical prototype ladder cannot be realised. Actually, the ladder derived from the transfer function is shown in Fig.6, which has 5 nodes, so it requires fifth order matrices, which in turn would lead to a tenth order transconductor-capacitor filter as shown in Fig.7. If a canonical design approach is applied, the transfer function is changed to the form

$$H(s) = \frac{s^3}{(s^2 + p_1^2)(s^2 + p_2^2)(s^2 + p_3^2)(s^2 + p_4^2)} \tag{42}$$

and a modified ladder is obtained as in Fig.8. This is now a four node network, and using any of the design equations (38c,d), (39c,d) or (40c,d), a canonical realisation can be implemented. Fig.9 shows the canonical realisation circuit structure of Eq(39c,d). Compared to the non-canonical realisation in Fig.7, two transconductors can be eliminated.

3.4) Mixed Variable Representation Approach for Canonical Ladder-Based Transconductor-Capacitor Filter Design

The canonical filter design method above is called Transfer Function Modification Approach, in which we focus on finding a canonical ladder prototype, and then using matrix design method to obtain a canonical transconductor-capacitor filter. Because the limitation of equal transconductance in transconductor-capacitor filter design, a large number of designs cannot be realised in canonical form. To overcome the difficulty, an alternative canonical design approach called Mixed Variable Representation Approach is developed. Instead of finding a canonical ladder prototype, we try to find the best variable representation in order to get a canonical transconductor-capacitor design from a non-canonical ladder prototype. Generally a non-canonical ladder prototype contains more nodes than a canonical ladder and this number also exceeds the number of poles being realised. Hence when a voltage variable representation is used the size of matrix is increased and this leads to more transconductors in a transconductor-capacitor filter realisation. It is also noticed that the extra nodes are usually introduced by series LC or LR branches. In a Mixed Variable Representation Approach, both voltage and current variables are selected in a non-canonical prototype ladder to form vector V, and a compact matrix form is obtained. Then the standard matrix design method is used to achieve a canonical transconductor-capacitor implementation. The application of this approach and the selection of the variables are very much dependent upon the structure of the non-canonical ladder. To demonstrate the application of the approach, we redesign the 8th-order Butterworth filter using the Mixed Variable Representation Approach. Examining the circuit in Fig.6, we notice that there are five nodes in the prototype ladder, so using a nodal voltage representation would require fifth order matrices in matrix design method, which in turn would lead to a tenth order transconductor filter. Instead, we can construct the vector V from two nodal voltages (V_1 and V_3), and the currents through the two LC series branches (I_2 and I_4). We use voltage (VI2 and V_{I4}) proportional to the currents and the terminating resistance, in order to preserve dimensional consistency. It is not necessary to simulate the output voltage (V_5) of the passive ladder explicitly, because all of I_4 passes through the termination resistor and V_{I4} can therefore be treated as the output voltage. For the mixed voltage-and-current representation of the eighth order Butterworth bandpass ladder the matrices are:

$$J=\begin{pmatrix}\frac{V_{in}}{R}\\0\\0\\0\end{pmatrix},V=\begin{pmatrix}V_1\\V_{12}\\V_3\\V_{14}\end{pmatrix},G=\frac{1}{R}\begin{pmatrix}1&1&0&0\\1&0&-1&0\\0&1&0&-1\\0&0&-1&1\end{pmatrix}, \qquad (43a,b,c)$$

$$C=\begin{pmatrix}C_1&0&0&0\\0&\frac{-L_2}{R^2}&0&0\\0&0&C_3&0\\0&0&0&\frac{-L_4}{R^2}\end{pmatrix},\Gamma=\begin{pmatrix}\frac{1}{L_1}&0&0&0\\0&\frac{-1}{R^2C_2}&0&0\\0&0&\frac{1}{L_3}&0\\0&0&0&\frac{-1}{R^2C_4}\end{pmatrix} \qquad (43d,e)$$

Substituting (43a,b,c,d,e) into the left-decomposition equations (23a,b) gives the transconductor-capacitor ladder shown in Fig.10. Again a circuit realisation with eight transconductors is obtained, though fewer capacitors are now required. A SPICE simulation of the fully differential version is shown in Fig.11.

4. FILTER AND EQUALISER DESIGN COMPILER: XFILT

The field of filter automation is now fairly mature, however it is still a challenging area with the continuing development of VLSI technology. Most filter compilers developed today are normally devoted to only one design strategy and technology and are usually restricted to the design of cascade biquad or provide very limited ladder-based structures (often leapfrog). These restrictions limit the designer's ability to combine and compare techniques and examine the benefits of different topologies. For these reasons, a new active filter and equaliser compiler called XFILT[14] has been developed to implement passive-RLC, active-RC, switched-capacitor and transconductor-capacitor filters and equalisers and incorporates a wide variety of filter structures proposed for ladder-based realisations together with more conventional biquad configurations.

The XFILT system structure is shown in Fig.12. A graphical interface utilises standard X11[15] and is provided both as a user friendly interface to the designer and as a system manager of all the software in XFILT. It offers a menu-driven interface for checking and facilitating the entry of design parameters. The specifications of the filter can be read in from menus or existing files. The menu-driven interface can prompt the user for the input needed and reject incorrect input. Graphical display is another characteristic of the

interface. The graphs of the approximation function and different circuit responses are given. A special feature of the XFILT graphical interface is that it provides a graphical editor, utilising this the user can specify/modify arbitrary, or classical magnitude and group delay templates with a mouse.

A range of standard approximation functions, Butterworth, Chebyshev, Inverse-Chebyshev, Elliptic, Bessel and Legendre are available. In the arbitrary magnitude design mode, the desired amplitude response of the filter is specified by a pair of piece-wise linear boundaries (a template) of amplitude against frequency. Approximation routine[7] will attempt to fit a response within the upper and lower boundary. The points where the approximation touches the upper boundary in the passband and $-\infty$ in the stopband are referred to as touch points. Manipulation of these touch points in an interactive manner facilitates great flexibility in design. For instance, high order touch points in the passband can ease group delay equalisation requirements and reduce sensitivity whereas in the stopband they can create deep, high order notches for single frequency rejection. A touch point editor allows the user to specify the sequence, type (fixed or free) and order of the touch points in each band of the characteristic.

The filter circuit design falls into two structural categories: cascade biquad and passive ladder simulation. Ladder simulation requires a passive ladder prototype which can either be synthesised internally or read from an external file. There are three ladder prototype synthesis modes: *expert* for experienced designers whereby complete control is exercised over the classes and sequence of pole/zero removals; *interactive* in which only the sequence of removals is selected and *automatic* when no manual intervention is necessary. All ladder-based filter structures are derived by matrix decomposition methods given in Section 2. In the cascade biquad mode, a variety of designs are available, including type-E, type-F and all-pass biquads. The structure of the software enables the addition of any required biquadratic sections, active-RC, SC and transconductor-C, in an easy manner.

Analysis facilities for frequency response, group delay, and amplitude sensitivity are provided. The embedded general simulator is SCNAP4[16], though SPICE and SWITCAP can also be called.

Because of circuit non-idealities such as finite amplifier gain-bandwidth and switch resistance (in SC circuits), the filter response may not correspond precisely with the approximation function. To improve the circuit designed, a template-correction based optimisation method has been developed. The method is completely general and is applicable to SC, active-RC, and transconductor-C filters. The software generates an error function based on circuit simulation results and approximation transfer function, this is

then used to modify the template. The software automatically produces a new approximation and circuit realisation. The main attraction of this approach is the low order optimisation space, which always corresponds to the order of the original filter. The process is quick and converges for realistic deviations due to practical circuit non-idealities.

5. LADDER-BASED TRANSCONDUCTOR-C FILTER AND EQUALISER DESIGN EXAMPLE

For a lowpass video filter with specifications of passband edge frequency 1MHz, stopband edge frequency 1.887MHz, passband ripple 0.28dB and stopband attenuation 50.5dB, a 5th-order elliptic ladder prototype will satisfy the requirements. Using the above matrix decomposition method, a fully differential transconductor-C circuit realisation is given in Fig.13, where all transconductors have the same value, and Fig.14 gives the SPICE simulation result of the circuit. The transconductance spread is 1 and the capacitance spread is 23.54. If a cascade of biquadratic stages is used, it is not possible to have equal valued transconductances, but the alternative equal valued capacitance realisation demands a transconductance spread of 7.3×10^6! Fig.15 shows the sensitivity comparison between a ladder-based realisation and a cascade biquad configuration, and the obvious advantage of ladder-based structure is clearly apparent.

The filter group delay variation within the passband is 1.1μs, whereas the original specifications require a maximum variation of 0.4μs. An initial 12th-order equaliser design, which reduces the group delay variation to 0.13 μs with an equal ripple behaviour, was considered. However with the help of XFILT compiler, the maximum group delay variation can still be satisfied by utilising a 6th-order equaliser, though the equal ripple behaviour no longer applies. The comparative sensitivity analysis for the ladder-based equaliser and a typical cascaded biquad equaliser is shown in Fig.16; the ladder-based structure is again significantly better. A fully differential realisation of the 6th-order equaliser is given in Fig.17. The filter and equaliser were fabricated on a 1 micron CMOS process, having double polysilicon and double metal and using a 5V power supply. Fig.18 shows the overall amplitude response of the filter and equaliser, the measured results are typical ones from the range obtained . It will be noted from the circuit response, that there is a loss of attenuation in the stopband including the disappearance of the second notch, though the level of stopband attenuation remains within specification. This retention of performance is due to deliberately allowing an initial filter approximation with a very generous stopband attenuation to absorb process variations and inaccuracies, and deterioration due to noise, though the noise level in the passband is typically -128dBm. The passband response of the fabricated circuit shows some variation in ripple level and corner frequency. Detailed investigation of the equaliser amplitude response

shows an arbitrary rippling behaviour over the passband of up to 1.1dB, whereas the computed amplitude response of the all-pass equaliser shows a completely flat characteristic over a wide frequency range. These variations in equaliser response can be directly attributed to the accuracy problems in realising the very wide spread in capacitance 2120:1 (transconductance spread is 1). It was also noted that the dynamic range of the equaliser was considerably less than the filter. It is now possible to utilise various signal scaling techniques at different stages of transconductance-C ladder-based designs and it would be sensible to invoke these in any re-design. The group delay responses, Fig.19, show very effective equalisation within the passband, the initial computed group delay variation of the filter is 1.02μs and the equalised value reduces to 0.395μs, the actual response of the combined circuit shows a variation of only 0.1μs which easily satisfies the initial specification.

Use of XFILT has enabled further improvements to the equaliser. Simply increasing the number of iterations in the group delay approximation stage improves the equal ripple nature of the response at no extra cost in circuit terms. A more significant improvement in silicon area can be achieved by utilising the arbitrary amplitude approximation facility for the filter. The use of a 4th order touch point near the band edge reduces the group delay variation of the filter to 0.72μs and thus lowers the equalisation requirements considerably. Fig.20(a) gives the passband response of the modified filter and Fig.20(b) shows the comparison of modified filter group delay and original filter group delay. A 4th-order equaliser can now be used. There is a cost of about 4dB loss of attenuation in the stopband of the filter.

6. CONCLUSION

Efficient ladder-based active filters and equalisers for active-RC, SC, and transconductor-capacitor are presented. The canonical realisations of these filters are studied. Several examples are given to demonstrate that the proposed canonical design method can be used to considerable advantage. The XFILT software development has been based on the ladder filter design methods given here, together with many cascade designs. A practical video filter and equaliser IC implementation example is presented and the test results are given.

7. ACKNOWLEDGEMENTS

Technical support in the implementation and testing of the video filter and equaliser by Wolfson Microelectronics is gratefully acknowledged. This work was supported by the Science and Engineering Research Council and the Department of Trade and Industry.

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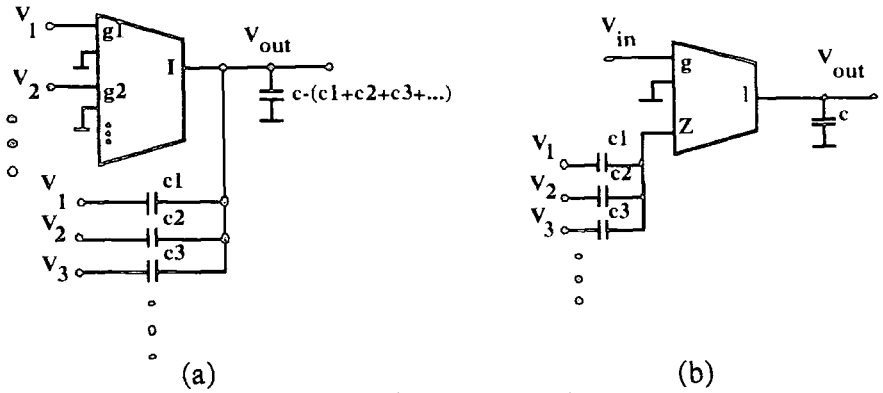

(a) (b)

Fig.1(a) First order section using a conventional transconductor
Fig.1(b) First order section using a low impedance input transconductor

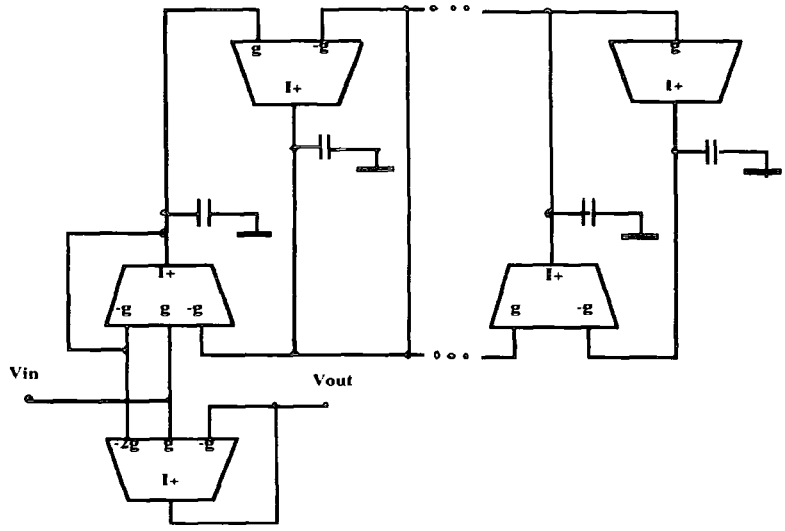

Fig.2 Transconductor-C ladder based group delay equaliser structure

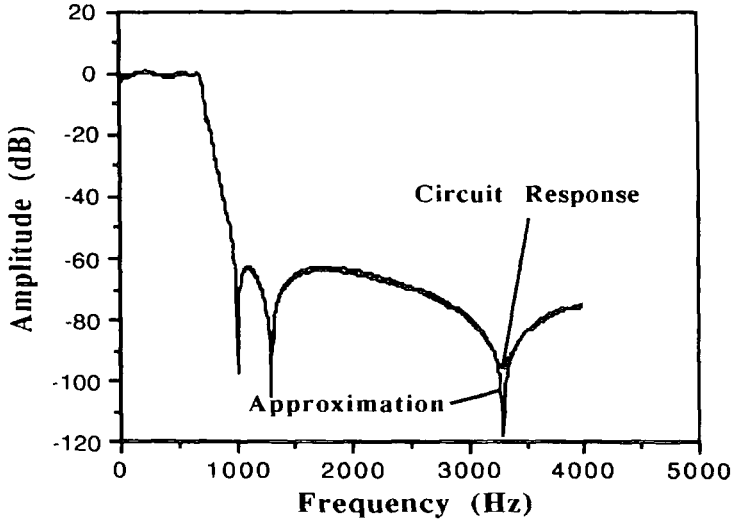

Fig.3 6th-order Elliptic canonical active-RC lowpass filter response

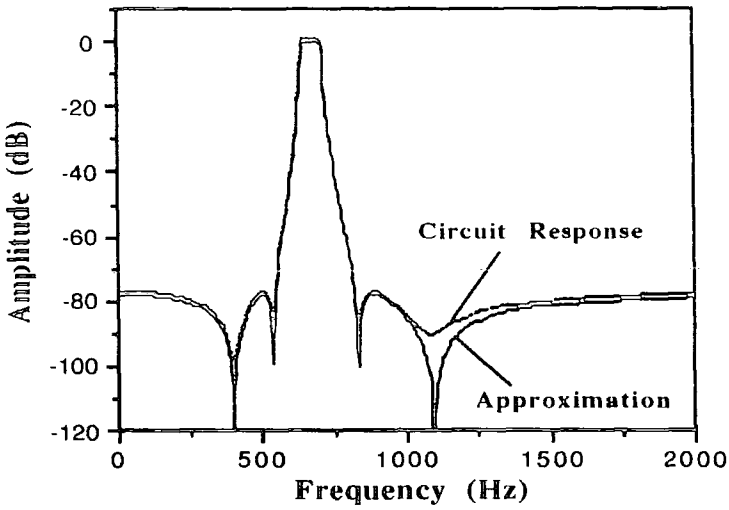

Fig.4 8th-order Elliptic canonical SC bandpass filter response

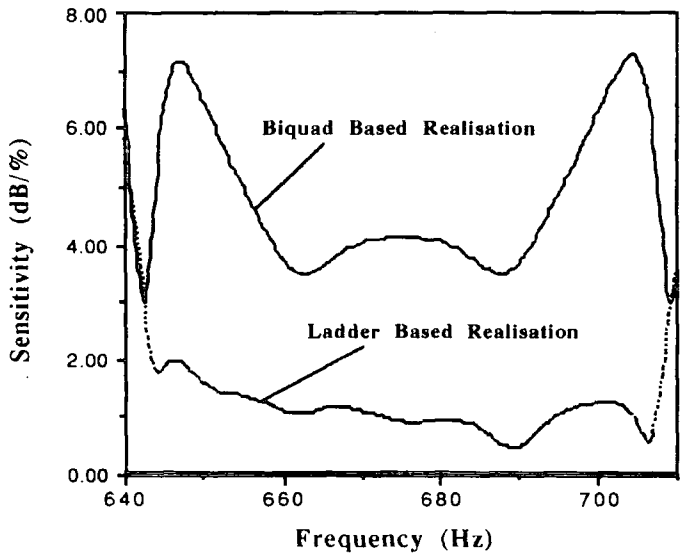

Fig.5 Sensitivity comparison of SC ladder based and biquad based filters

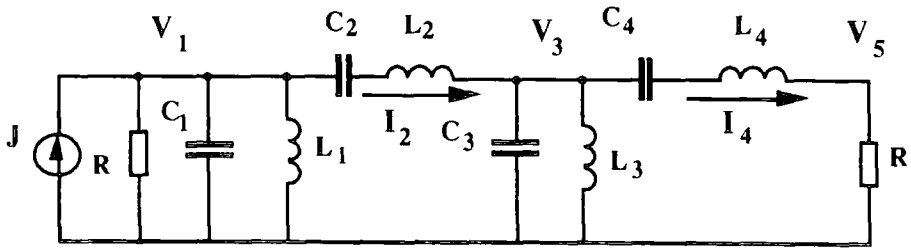

Fig.6 8th-order Butterworth bandpass ladder prototype

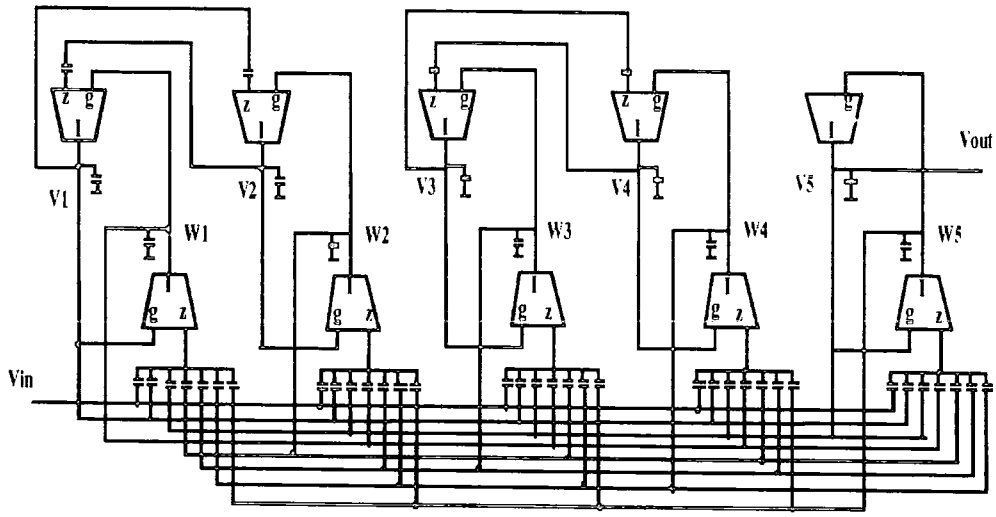

Fig.7 Transconductor-C filter based on prototype in Fig.6

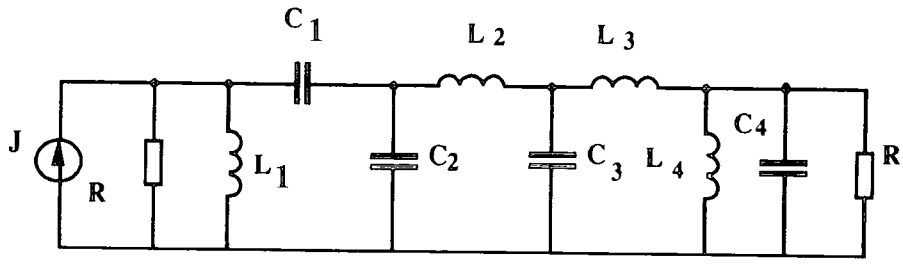

Fig.8 Modified 8th-order Butterworth bandpass ladder prototype

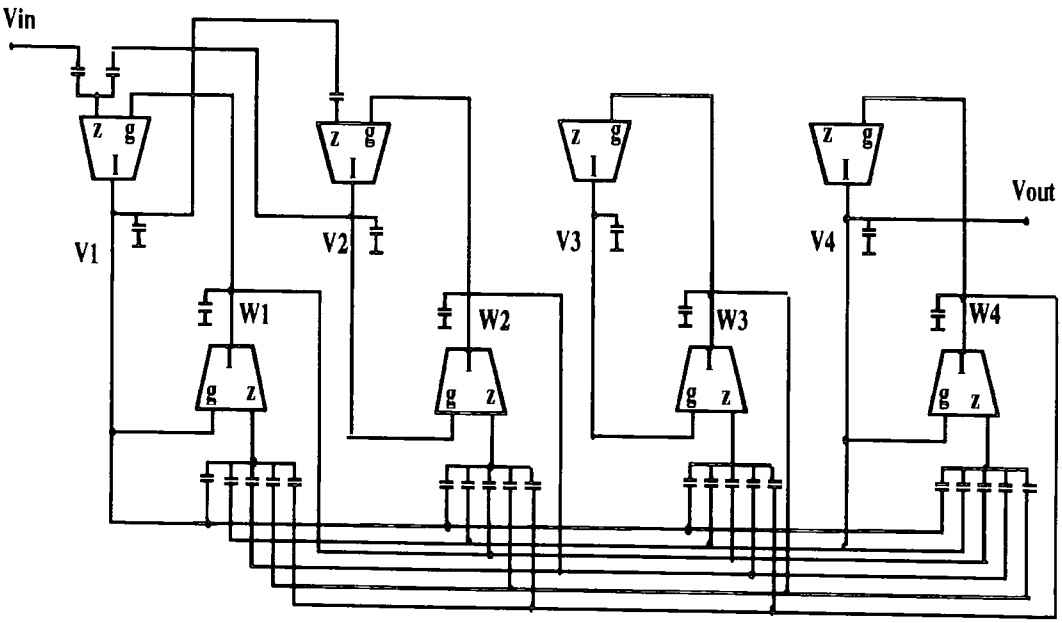

Fig.9 Transconductor-C filter based on modified prototype

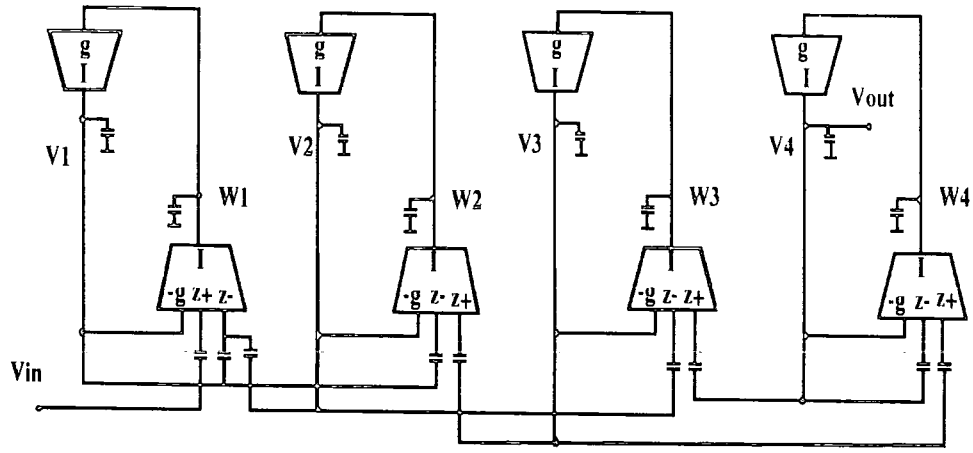

Fig.10 Transconductor-C filter designed by mixed variable representation approach

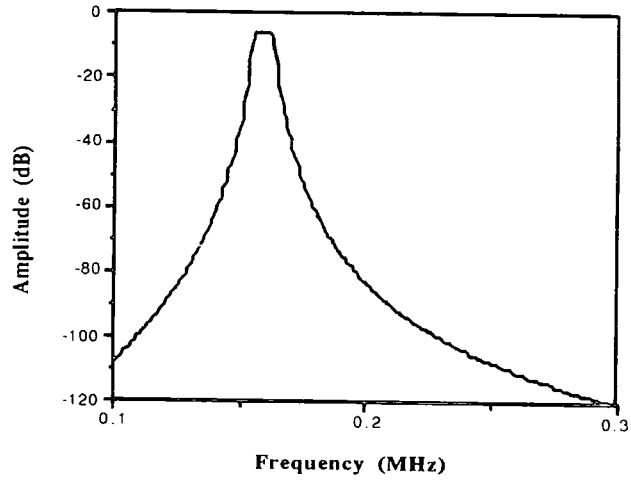

Fig.11 SPICE simulaton of 8th-order Butterworth transconductor-C ladder filter

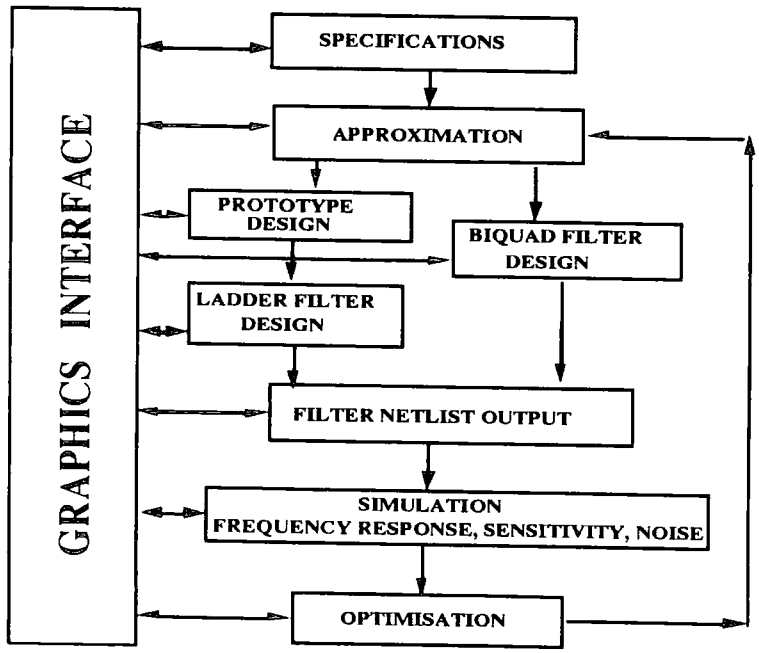

Fig.12 XFILT structure block diagram

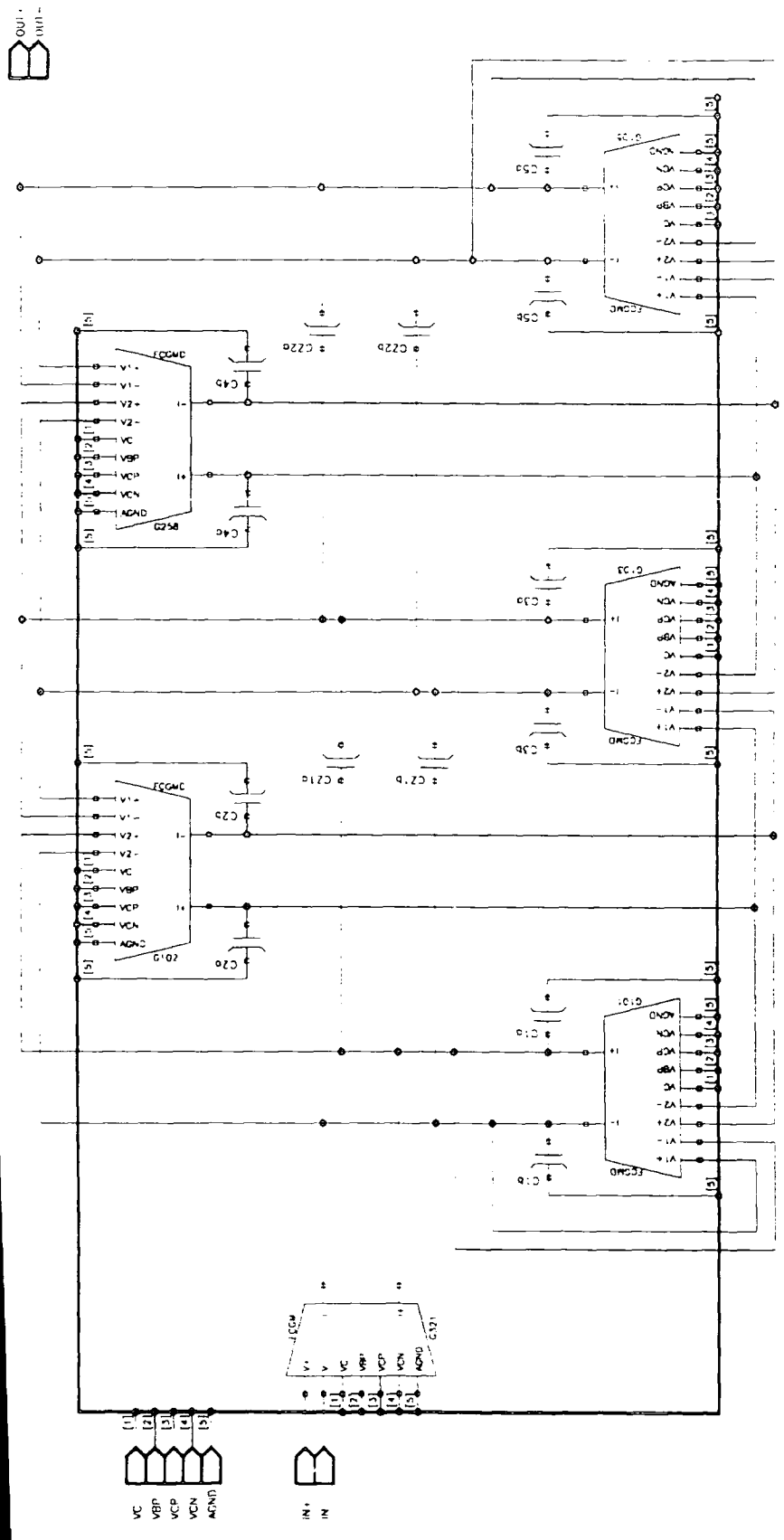

Fig.13 Fully differential 5th-order transconductor-capacitor video filter circuit

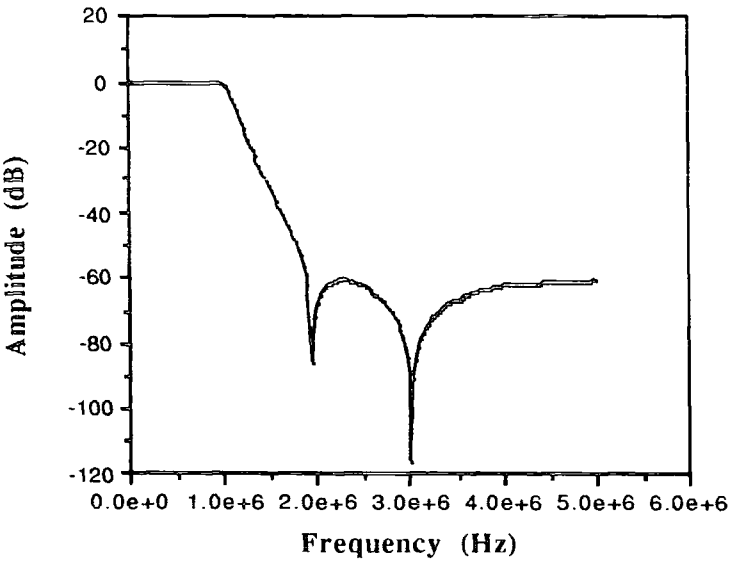

Fig.14 SPICE simulation of transconductor-C video filter response

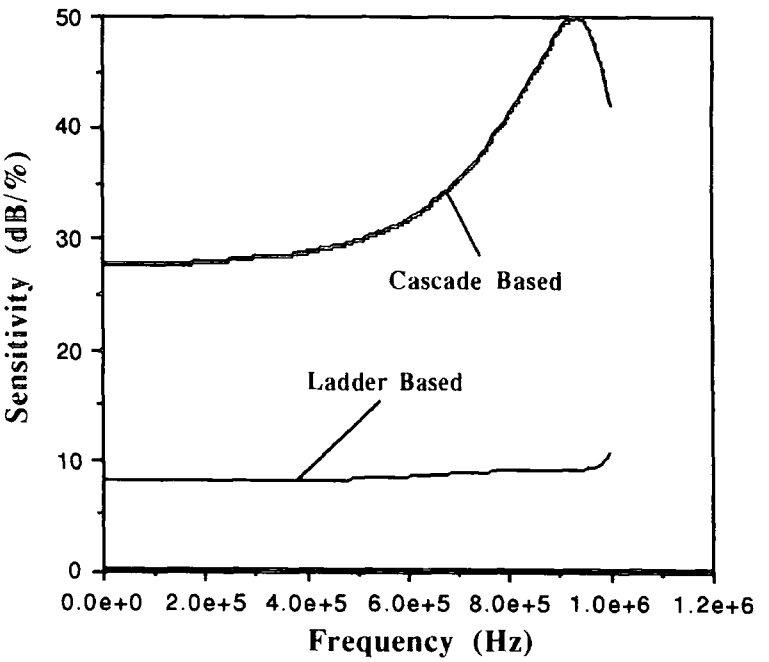

Fig.15 Passband sensitivity of video filters

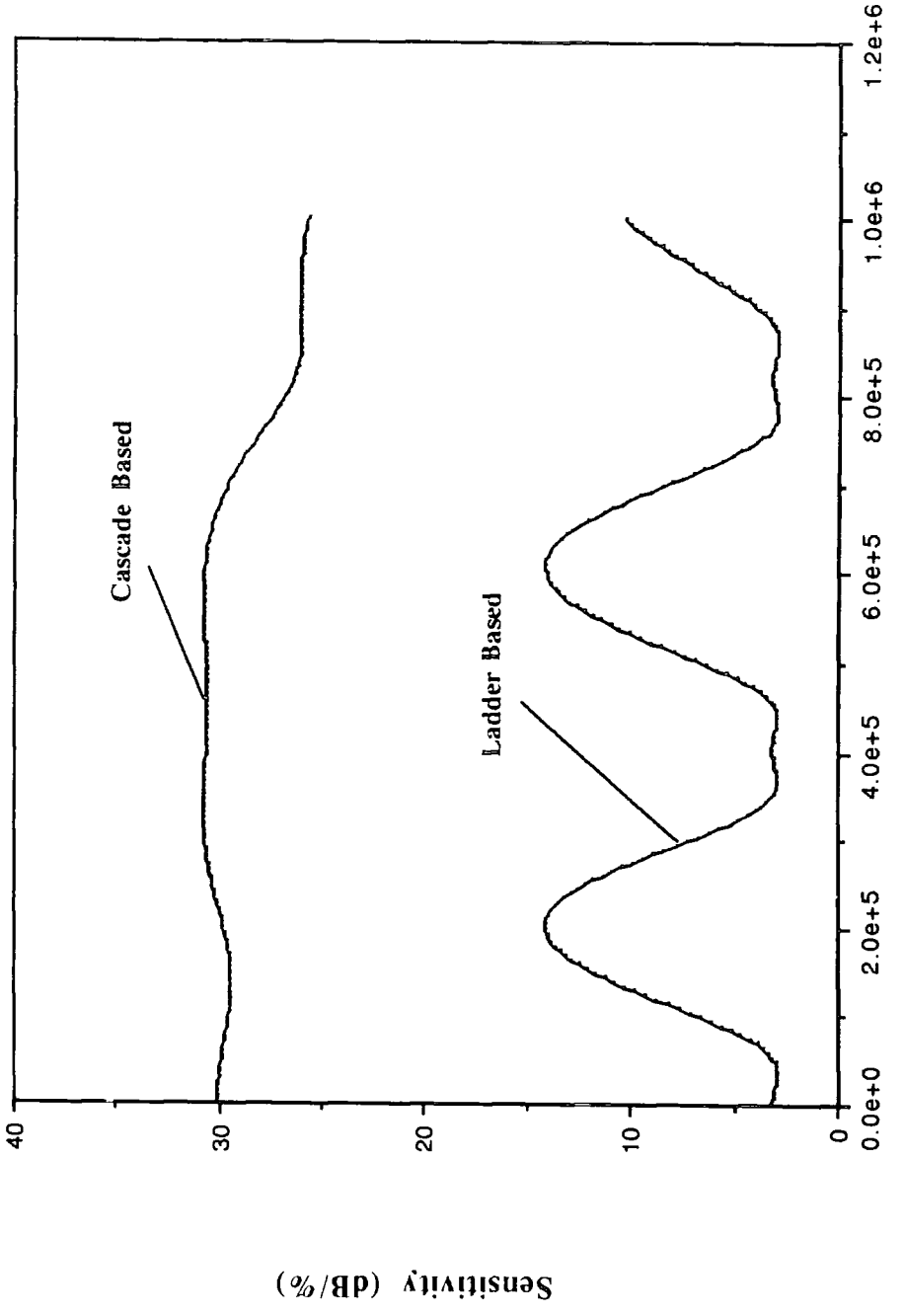

Fig.16 Video equaliser sensitivity comparison

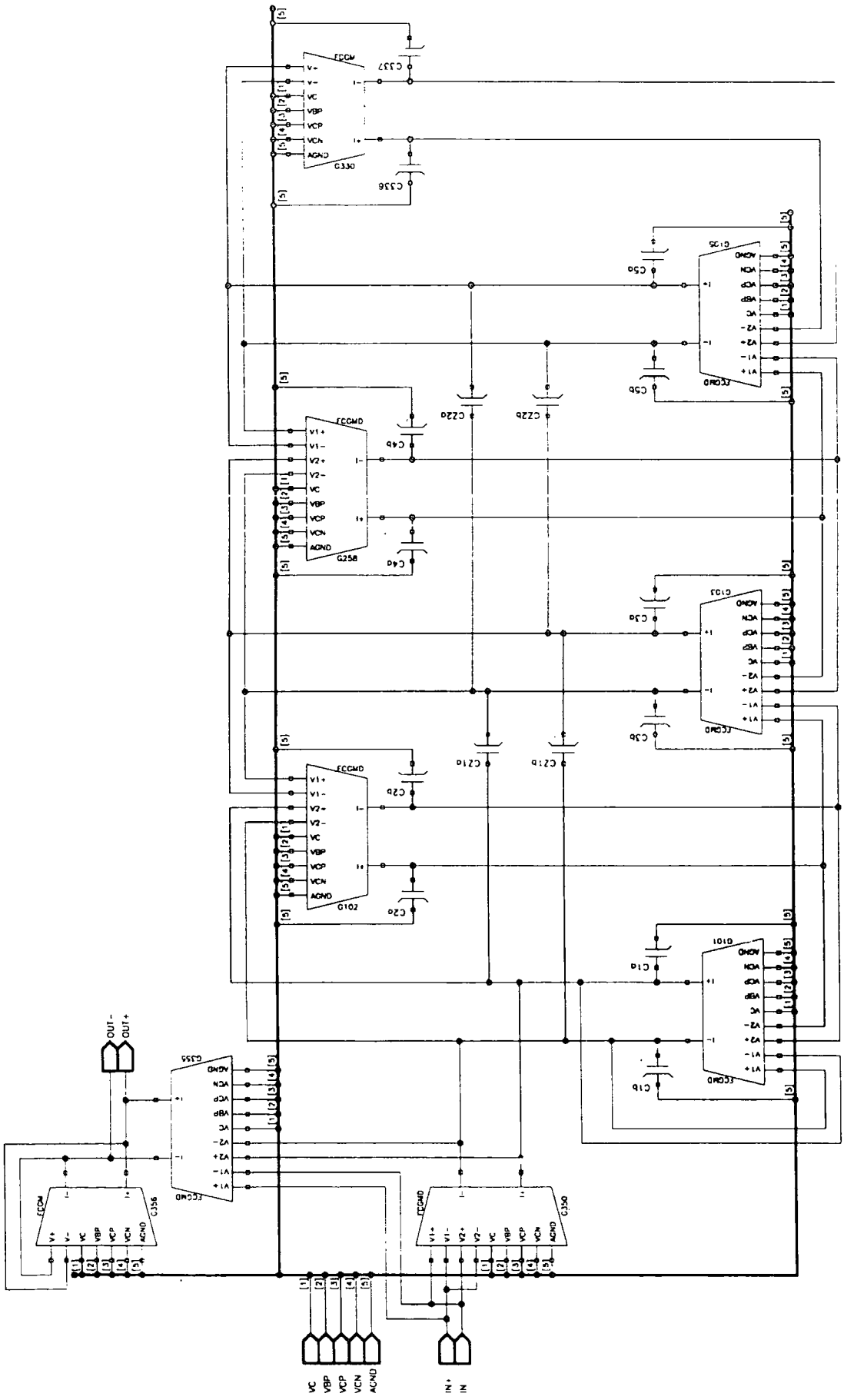

Fig.17 Fully differential 6th-order transconductor-C video equaliser circuit

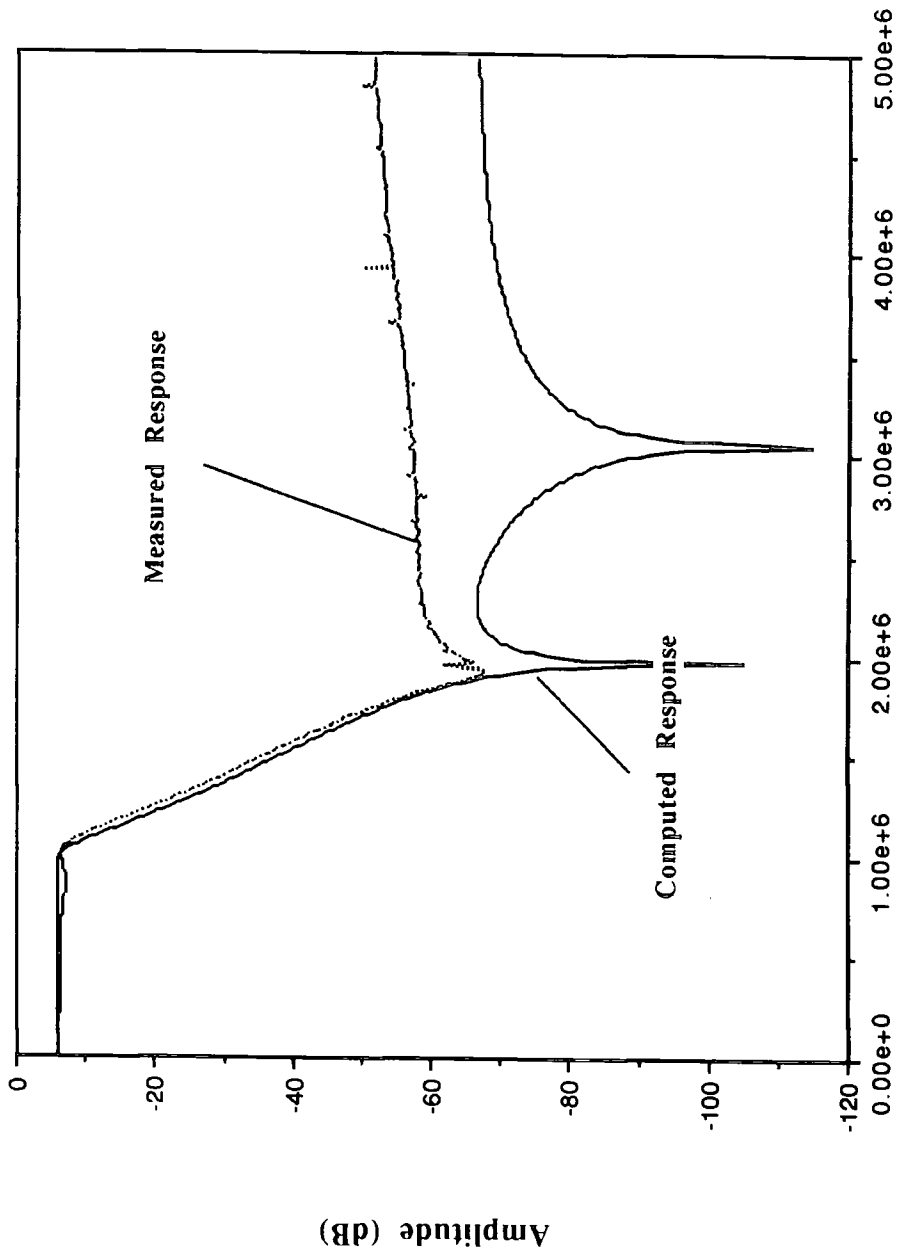

Fig.18 Overall amplitude response of filter and equaliser

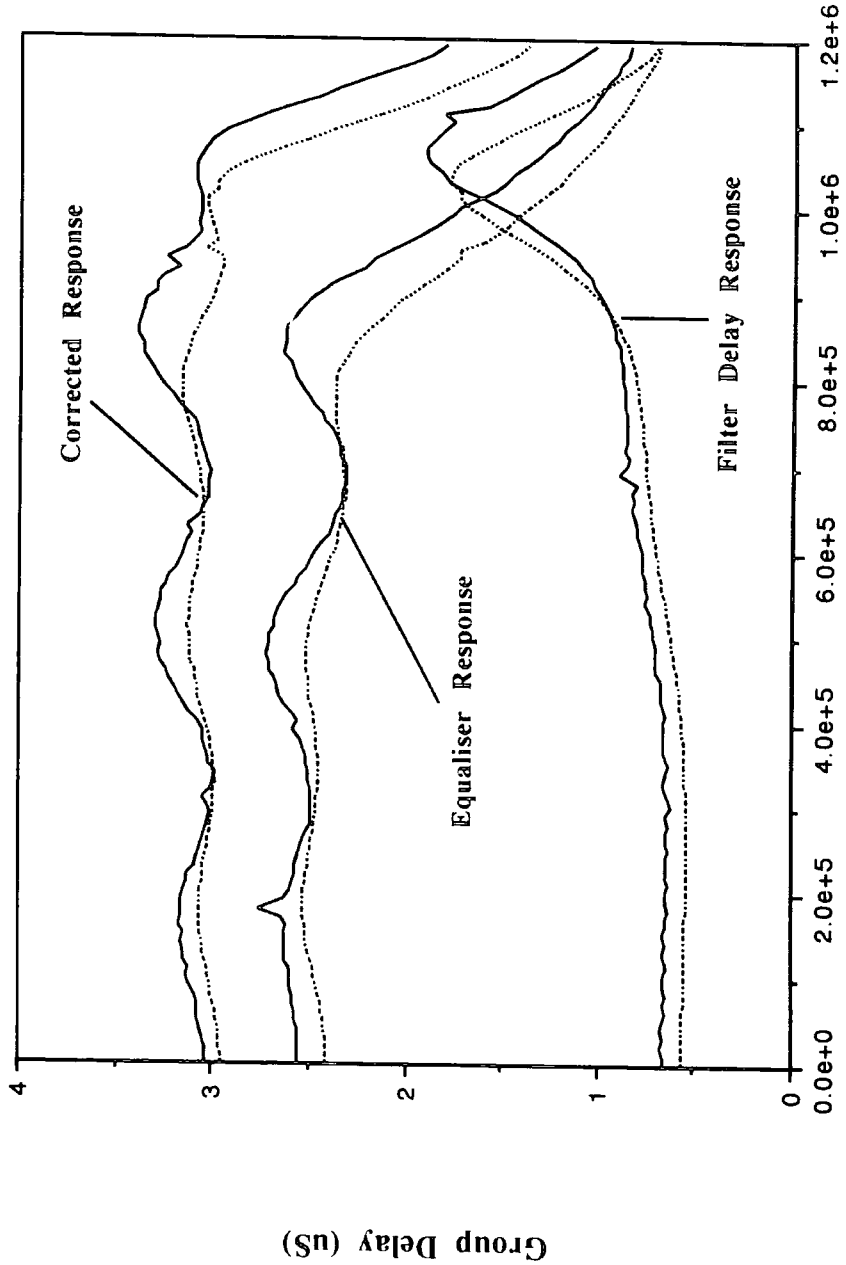

Fig.19 Filter and equaliser group delay responses

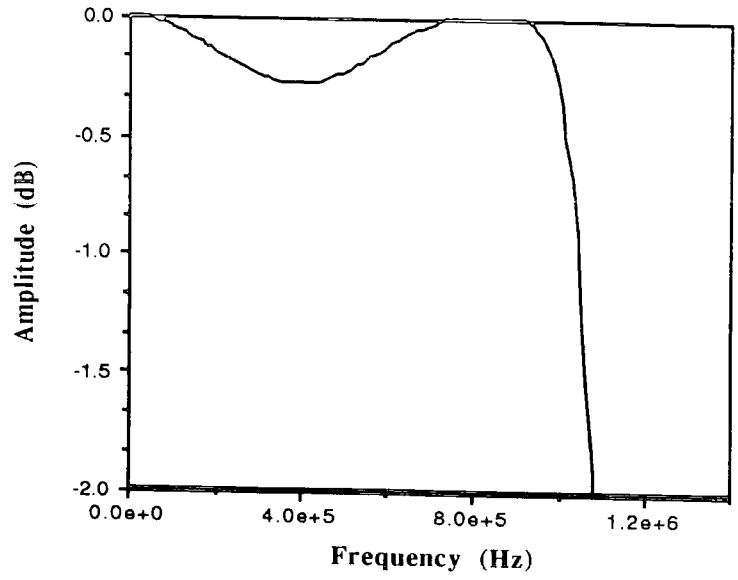

Fig.20(a) Video filter passband response using a 4th order touch point

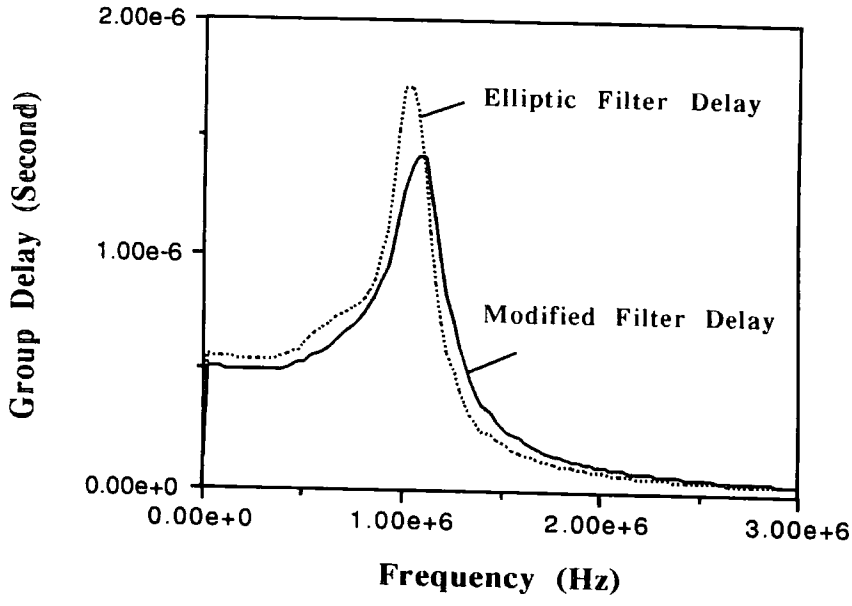

Fig.20(b) 4th order equaliser group delay response

FIGURE CAPTIONS

Fig.1(a) First order section using a conventional transconductor

Fig.1(b) First order section using a low impedance input transconductor

Fig.2 Transconductor-capacitor ladder-based group delay equaliser structure

Fig.3 6th-order Elliptic canonical active-RC lowpass filter response

Fig.4 8th-order Elliptic canonical SC bandpass filter response

Fig.5 Sensitivity comparison of SC ladder-based and cascade based filters

Fig.6 8th-order Butterworth bandpass ladder prototype

Fig.7 Transconductor-capacitor filter based on prototype in Fig.6

Fig.8 Modified 8th-order Butterworth bandpass ladder prototype

Fig.9 Transconductor-capacitor filter based on modified prototype

Fig.10 Transconductor-C filter designed by mixed variable representation approach

Fig.11 SPICE simulation of 8th-order Butterworth transconductor-C ladder filter

Fig.12 XFILT structure block diagram

Fig.13 Fully differential 5th-order transconductor-capacitor video filter circuit

Fig.14 SPICE simulation of transconductor-C video filter response

Fig.15 Passband sensitivity of video filters

Fig.16 Video equaliser sensitivity comparison

Fig.17 Fully differential 6th-order transconductor-C video equaliser circuit

Fig.18 Overall amplitude response of filter and equaliser

Fig.19 Filter and equaliser group delay responses

Fig.20(a) Video filter passband response using a 4th order touch point

Fig.20(b) 4th-order video equaliser group delay response

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ACCURATE SEMI-SYMBOLIC ANALYSIS OF LARGE NON-IDEAL SWITCHED LINEAR NETWORKS

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ABSTRACT

In this paper, an accurate semi-symbolic analysis method based on polynomial interpolation techniques for large non-ideal switched linear networks (SC and SI) is presented. For the computation of frequency responses, the semi-symbolic method demonstrates significant improvements in speed over direct numerical methods and this increases with circuit size. It is shown that semi-symbolic techniques can be used in the computation of noise for circuits containing a limited number of clock waveforms but the performance rapidly deteriorates with network size. Examples demonstrate the comparative speed and accuracy performance over a range of circiuts.

1. INTRODUCTION

The symbolic analysis of linear analogue circuits has attracted the attention of many researchers over a considerable peroid of time. Many algorithms and techniques have been developed and from these determinant and flow graph methods appear to be favoured in terms of flexiblity and efficiency [1-15]. All approaches suffer from restrictions inherent to the problem, the escalation of computer time and memory requirements with increase in circuit size. Two typical solutions proposed are expression approximation[16] and hierarchial decomposition[17],some improvements have resulted. However, despite all the effort, these methods still experience great difficulty with medium to large networks. Whilst attention has been focussed on continuous-time analogue circuits, some work has ben carried out on the symbolic analysis of ideal SC networks[18] and only exploratory investigations have been reported into the semi-symbolic analysis of non-ideal SC networks[19] and noise performance [20].

The only realistic scheme for large networks of any type is a semi-symbolic one, when polynomials in s or z or both, with purely numeric coefficients, are generated. It is well known that generation of polynomials by interpolation is a very efficient technique. However, the generation of polynomials in mixed variables (s,z) is really the basic requirement for the analysis of non-ideal switched networks (SC or SI), and this adds to the complexity of the interpolation problem.

The main contribution of this paper is the generation of modified polynomials in a single variable z by interpolation, as required for analysis of large non-ideal switched linear networks. It is demonstrated that high accuracy can be manintained for large networks and the application to the computation of frequency responses is very attractive. The extension to noise computation in switched linear networks is considered.

2. POLYNOMIAL INTERPOLATION METHOD

A large non-ideal switched linear network can be described by a system of equations the in z domain [21]

$$\begin{bmatrix} \mathbf{I} & & & -\mathbf{P}_1 \\ -\mathbf{P}_2 & \mathbf{I} & & \\ & \ddots & \ddots & \\ & & -\mathbf{P}_M & z\mathbf{I} \end{bmatrix} \begin{bmatrix} \mathbf{V}_1(z) \\ \mathbf{V}_2(z) \\ \vdots \\ \mathbf{V}_M(z) \end{bmatrix} = \begin{bmatrix} \Sigma\mathbf{W}_1(z) \\ \Sigma\mathbf{W}_2(z) \\ \vdots \\ z\Sigma\mathbf{W}_M(z) \end{bmatrix} \quad (1)$$

where $\mathbf{P}_k = \mathbf{p}_k\mathbf{C}_k$

$\mathbf{C}_k$ is the capacitance matrix of the kth time-slot and $\mathbf{p}_k$ is the extended state transition matrix. The r.h. side contains polynomial approximations to the excitation vectors and appropriate sampling weighting factors, the vector V contains node voltages and branch currents. Since the $\mathbf{p}_k$ matices and components of the r.h. side vector can only be assembled by numerical techniques, closed form symbolic solutions for the system responses are impossible to obtain. However, a polynomial interpolation scheme provides a natural solution, this can be summarised as follows:

```
for(i=0; i<P; i++) { /* P is polynomial degree */
    solve T(z_i)V = W;
    calculate D(z_i) = det T(z_i);
    N(z_i) = D(z_i)V;
}
DFT (FFT) to generate the numerator polynomial;
DFT(FFT)to generate the denominator polynomial;
```

For a system like (1), the denominator of the transfer function can be determined by
$D(z_i) = \det(z_i\mathbf{I} - \mathbf{E})$ where $\mathbf{E} = \mathbf{P}_M\mathbf{P}_{M-1}\cdots\mathbf{P}_1$

For continuous-time systems, the above procedures are straightforward, in the switched network case some care has to be taken. This can demonstrated in a simple 2-phase clock system when:

$$\begin{bmatrix} \mathbf{I} & -\mathbf{P}_1 \\ -\mathbf{P}_2 & z\mathbf{I} \end{bmatrix}\begin{bmatrix} \mathbf{H}_1(z) \\ \mathbf{H}_2(z) \end{bmatrix} = \begin{bmatrix} \mathbf{B}_1 e^{j\omega\sigma_1} \\ \mathbf{B}_2 e^{j\omega\sigma_2} \end{bmatrix} \qquad (2)$$

solving the matrix equation (2) gives

$$\begin{bmatrix} \mathbf{H}_1(z) \\ \mathbf{H}_2(z) \end{bmatrix} = \begin{bmatrix} \mathbf{B}_1 e^{j\omega\sigma_1} + \dfrac{\mathbf{P}_1\mathbf{B}_2 e^{j\omega\sigma_2} + \mathbf{P}_1\mathbf{P}_2\mathbf{B}_1 e^{j\omega\sigma_1}}{z\mathbf{I} - \mathbf{P}_2\mathbf{P}_1} \\ \dfrac{\mathbf{B}_2 e^{j\omega\sigma_2} + \mathbf{P}_2\mathbf{B}_1 e^{j\omega\sigma_1}}{z\mathbf{I} - \mathbf{P}_2\mathbf{P}_1} \end{bmatrix}$$

The denominator polynomial is obtained from
$D(z) = \det(z\mathbf{I} - \mathbf{P}_2\mathbf{P}_1)$
and the numerators are determined by

$$\begin{pmatrix} N_1(z) \\ N_2(z) \end{pmatrix} = D(z)\begin{pmatrix} H_1(z) \\ H_2(z) \end{pmatrix}$$

The numerator and denominator polynomials are then generated by interpolation using a DFT(FFT). When the frequency response is evaluated from the resultant polynomials and compared with directly computed results, the error is quite considerable, even for small circuits. For a small SC treble tone control filter, the error reponse for one of the transfer functions is shown in Fig.1, graph (a). The reason for this is that

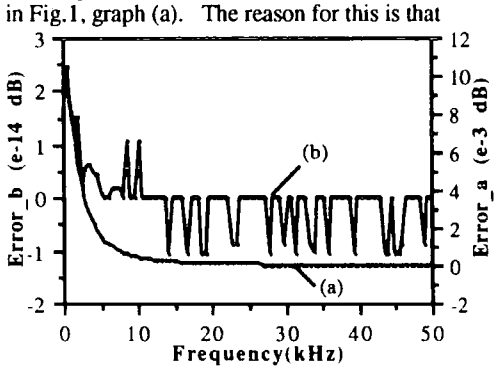

Fig 1. Error of $H_2(\omega)$ (a) direct interpolation, (b) modified interpolation

fractional powers of z are intoduced by the time-slot weighting factors and if the polynomials are re-defined to account for this, very high orders result and low accuracy follows. There is a simple solution, again consider a 2-phase system and separately excite each time-slot:

$$\begin{bmatrix} \mathbf{I} & -\mathbf{P}_1 \\ -\mathbf{P}_2 & z\mathbf{I} \end{bmatrix}\begin{bmatrix} \mathbf{H}_{11}(z) \\ \mathbf{H}_{12}(z) \end{bmatrix} = \begin{bmatrix} \mathbf{B}_1 \\ \mathbf{0} \end{bmatrix} \qquad (3)$$

$$\begin{bmatrix} \mathbf{I} & -\mathbf{P}_1 \\ -\mathbf{P}_2 & z\mathbf{I} \end{bmatrix}\begin{bmatrix} \mathbf{H}_{21}(z) \\ \mathbf{H}_{22}(z) \end{bmatrix} = \begin{bmatrix} \mathbf{0} \\ \mathbf{B}_2 \end{bmatrix} \qquad (4)$$

Then

$$\begin{pmatrix} \mathbf{H}_1 \\ \mathbf{H}_2 \end{pmatrix} = \begin{pmatrix} \mathbf{H}_{11} & \mathbf{H}_{12} \\ \mathbf{H}_{21} & \mathbf{H}_{22} \end{pmatrix}\begin{pmatrix} e^{j\omega\sigma_1} \\ e^{j\omega\sigma_2} \end{pmatrix}$$

The error resulting from evaluation of H_2 interpolated polynomials is given in Fig.1, graph (b) and shows a great improvement in accuracy. Table 1 shows this technique applied to a wide range of SC circuits and several deductions can be made. Potentially all M^2 (M is the number of time slots) need to be interpolated, though some are zero in the majority of circuits and interpretive code makes most matrix arithmetic common. This approach effectively needs M solutions of equation (1) at each sample frequency, whereas a numerical simulator such as SCNAP4[21] needs one solution for each frequency point required. The DFT(FFT) process takes much less time than the computation of sampled frequency responses. Once all transfer functions have been interpolated, repetitive expression evaluation is more efficient than direct matrix solution, though for multirate circuits the efficiency gains decrease because of the increased number of transfer functions. The polynomial interpolation methods can preserve acuracy even in the analysis of quite large circuits.

3. SYMBOLIC METHOD FOR NOISE EVALUATION

By utilising transpose techniques, all transfer functions from each noise source to the output can be obtained by solving an adjoint system. The problem can be formulated as

$$\phi_i = \tilde{\mathbf{d}}^t\mathbf{T}^{-1}\mathbf{W}_i$$

Define the adjoint system as

$$\mathbf{T}^t\mathbf{X}_i^a = -\tilde{\mathbf{d}}$$

The noise contribution of each noise source is then calculated by,

$$\phi_i = -\mathbf{X}_i^a\mathbf{W}_i$$

Again, for a simple a 2-phase switched linear network, the adjoint system is

$$\begin{bmatrix} \mathbf{I} & -\mathbf{P}_2^t \\ -\mathbf{P}_1^t & z\mathbf{I} \end{bmatrix}\begin{bmatrix} \mathbf{X}_1^a \\ \mathbf{X}_2^a \end{bmatrix}_i = -\begin{bmatrix} \tilde{\mathbf{d}}D_1 \\ \tilde{\mathbf{d}}D_2 \end{bmatrix}$$

where D_k are sin(x)/x factors.

After two adjoint system solutions at one sampling frequency, noise transfer functions can be interpolated from:

$$\begin{pmatrix} \mathbf{X}_1^a \\ \mathbf{X}_2^a \end{pmatrix}_i = \begin{pmatrix} \mathbf{X}_{11}^a & \mathbf{X}_{12}^a \\ \mathbf{X}_{21}^a & \mathbf{X}_{22}^a \end{pmatrix}_i\begin{pmatrix} D_1 \\ D_2 \end{pmatrix}$$

The total noise power spectral density at the output is calculated by superposition

$$S_T(\omega) = \sqrt{\sum_{n=0}^{p}\sum_{i=0}^{m}|\phi_i|^2 S_i(\omega - n\omega_s)}$$

where $S_i(\Omega)$ is the ith input noise source power spectral density and p is the number of bands to be considered. Two circuits were tested and the run time statistics are illustrated in Table II. These show that for switched linear networks, the symbolic method for noise evaluation is less efficient than its numerical counterpart and an examination of the relative theoretical computational costs will provide an explanation for this.

4. THEORETICAL COSTS OF EXPRESSION EVALUATION AND MATRIX SOLUTION

Two basic definitions are utilised. A flop (floating point operation) is defined to be the time required for a particular computer system to execute the C code

A += C* D

Similarly, a trop (trigonometric function operation) is the time required for execute another C code

A += B*cos(C*D)

In SCNAP4, the last time-slot matrix solution takes about $5N^2$ flops, where N is the matrix dimension. The solutions of all other slots require another $2(M-1)N^2$ flops, this makes a total of $(2M+3)N^2$ flops per frequency point. Fig 2a shows clearly the $(2M+3)N^2$ dependence of matrix solution approach. For symbolic expression evaluation, the network has M^2 transfer functions to be calculated, it requires about $2PM^2$ trops where P is the polynomial degree. The PM^2 dependence of the expression evaluation is shown in Fig. 2b

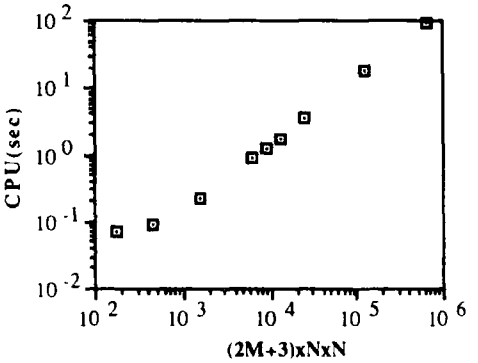

Fig. 2a $(2M+3)N^2$ dependence of matrix solution approach

Let $\alpha = (2M+3)N^2$, $\beta = \gamma(2PM^2)$, where γ is a computer system related constant. On a SUN-Sparc ELC station, one trop takes about nine times longer than one flop, therefore $\gamma = 9$. α and β are two useful

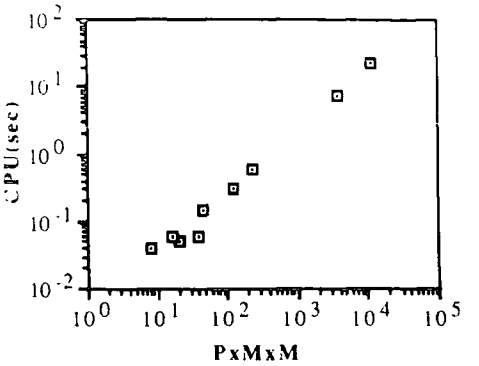

Fig.2b PM^2 dependence of the expression evaluation

theoretical factors when comparing the computational efficiency of numerical and symbolic approaches. Generally, $\alpha > \beta$ which means expression evaluation is faster than numerical matrix solution. For instance with the treble tone control filter, these two factors can be calculated as follows

$$\alpha = (2\times 2+3)\times 8^2 = 448$$

$$\beta = 9\times(2\times 4\times 2^2) = 288$$

The ratio $\alpha:\beta \approx 0.09:0.06$ which are the values in the tf example entry in Table I. Since β increases quadratically with respect to the number of time-slots, expression evaluation for multirate circuits is expected to be less efficient than for 2-phase circuits.

The total cost situation for noise analysis by expression evaluation becomes more significant. If a circuit has m noise sources, the total cost is $m\beta$. Now, in large non-ideal switched linear networks where there are many switches and other active devices, m is likely to be very large, hence the application of symbolic techniques to noise analysis is not very feasible. This trend can be seen in Table II, where limited noise evaluation at only 100 frequency points compares poorly with full SCNAP4 noise analysis [22].

5. CONCLUSIONS

An application of a semi-symbolic analysis method to large non-ideal switched-linear networks is presented. Accuracy and speed are compared with an equivalent numerical simulator. Noise calculation utilising symbolic expression evaluation approach is proposed, but it is shown to be of limited efficiency.

ACKNOWLEDGEMENT

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circuit name	circuit size	No.of slots	polyn. degree	sample (sec)	DFT (sec)	expr. cal. (100 pts)	SCNAP4 (100 pts)	peak err (dB)
spft	112	24	20	241.14	16.42	23.61	89.06	1e-8
lp10	60	16	15	24.26	4.46	7.25	17.99	1e-9
nos11	48	4	15	1.17	0.33	0.59	3.47	1e-5
bp8	43	2	11	0.20	0.06	0.15	1.70	1e-9
bp6	36	2	10	0.15	0.04	0.06	1.18	1e-6
nos5	24	4	8	0.27	0.12	0.31	0.88	1e-11
bp2	15	2	5	0.05	0.03	0.05	0.23	1e-10
tf	8	2	4	0.03	0.01	0.06	0.09	1e-14
int	5	2	2	<0.01	0.01	0.04	0.07	1e-14

Table I. Performance of the polynomial interpolation method

circuit name	circuit size	No. of slots	polyn. degree	sample (sec)	DFT (sec)	symbolic. (sec)	SCNAP4 (sec)
tf	8	2	4	0.04	0.07	>1.03	0.09
bp6	36	2	10	0.80	1.59	>7.74	2.11

Table II. Run time statistics of symbolic method for noise evaluation.

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A SYSTEMATIC APPROACH FOR LADDER BASED SWITCHED-CURRENT FILTER DESIGN

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ABSTRACT

A systematic approach for ladder based switched-current (SI) filter design is described. Low sensitivity and low parameter spread SI circuits realised by both existing and novel structures can be derived from the proposed approach. The method can be applied to all the filter types and is well suited for computer aided implementation. Techniques to improve dynamic range and reduce circuit parameter spread are also presented. A 10th-order bandpass filter is used to demonstrate the utility of the approach.

1. INTRODUCTION

In recent years much research has been directed towards the development of switched-current filters. In this paper, we present a systematic approach for ladder SI filter design. The method can produce eight different realisation structures from one prototype ladder, all maintain the low sensitivity property, but demonstrate a range of maximum ratios of transistor aspect ratios and the sums . The designer can slect the smallest maximum ratio of transistor aspect ratios to maintain accuracy in realisation and the minimum sum to obtain low power and small area realisations. The familiar leapfrog SI design method used by many filter designers is shown to be a special case within the general structures. The approach is an exact simulation of a prototype ladder and does not involve any approximation [1-2]. The bilinear transformation is adopted, but use of bilinear integrators is avoided, this leads to simplification of existing circuit structures [3-4]. The approach is totally general and applicable to any filter type (lowpass, bandpass, bandstop, highpass and allpass) without recourse to special techniques [5-6]. Moreover, the approach is very suitable for computer aided implementation and has already been implemented in a filter design system.

2. MATRIX BASED SWITCHED-CURRENT FILTER DESIGN

A passive ladder can be represented by the matrix equation

$$(sC + s^{-1}\Gamma + G)V = J \qquad (1)$$

where V and J are vectors representing the nodal voltages and input current source and G, C and Γ are matrices representing the contributions of conductors, capacitors and inductors respectively. To improve circuit realisation efficiency, alternating signs are introduced in V i.e, let $V = [V_1\ -V_2\ V_3\ -V_4\ .....]$. This ensures that all the entries in (1) are positive. Since the operational blocks in SI circuits process currents, all prototype variables must be transformed to current variables using a scaling resistor (chosen to be $1\,\Omega$ for convenience). The equation (1) then can be represented as

$$(sC + s^{-1}\Gamma + G)I = J \qquad (2)$$

After bilinear transformation

$$s \rightarrow \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}} \qquad (3)$$

equation (2) becomes

$$\left[\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}C + \frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}}\Gamma + G\right]I = (1+z^{-1})J \qquad (3)$$

Multiplying the system through by $(1+z^{-1})/(1-z^{-1})$ and some manipulation gives

$$\left[\frac{1}{\phi}A + \psi\Gamma + D\right]I = (1+z^{-1})J \qquad (4)$$

where

$$\psi = \frac{z^{-1}}{1-z^{-1}} \qquad (4a)$$

$$\phi = \frac{1}{1-z^{-1}} \qquad (4b)$$

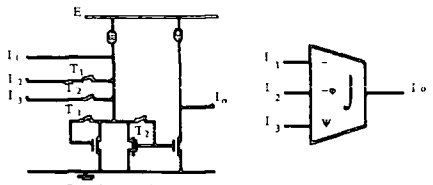
$$A = \frac{2}{T}C + \frac{T}{2}\Gamma - G \qquad (4c)$$

$$B = 2T\Gamma \qquad (4d)$$

$$D = 2G \qquad (4e)$$

The operators ψ and ϕ can now be realised by SI building blocks. However equation (4) is still a second order equation. To implement an SI filter, equation (4) needs to be decomposed into two first order equations by the introduction of a vector of intermediate variables. A typical second-generation SI memory cell based first order SI building block as shown in Fig.1 is used in the implementation of each first order equation. It has a transfer function:

$$I_o = -I_1 - \frac{1}{1-z^{-1}} I_2 + \frac{z^{-1}}{1-z^{-1}} I_3 \qquad (5)$$



(a)Typical circuit (b) Block symbol

Fig.1 SI Filter First Order Building Block

In practice, any enhanced type memory cell can be employed to form a first order building block, such as cascode, regulated cascode, folded cascode, or class AB memory cells.

2.1. LEFT MATRIX DECOMPOSITION APPROACH

Either the **A** or the **B** matrix can be factorised, leading to left and right decomposition respectively. Factorise the matrix A into

$$\mathbf{A} = \mathbf{A}_l\mathbf{A}_r \qquad (6)$$

The eqn.(4) can be expressed as

$$\mathbf{A}_l\mathbf{X} = -(\psi\mathbf{B}+\mathbf{D})\mathbf{I}+(1+z^{-1})\mathbf{J} \qquad (7a)$$

$$\mathbf{A}_r\mathbf{I} = \phi\mathbf{X} \qquad (7b)$$

For convenience in circuit realisation, let $\mathbf{W}=-\mathbf{X}$, and equation (7) becomes

$$\mathbf{A}_l\mathbf{W} = (\psi\mathbf{B}+\mathbf{D})\mathbf{I}-(1+z^{-1})\mathbf{J} \qquad (8a)$$

$$\mathbf{A}_r\mathbf{I} = -\phi\mathbf{W} \qquad (8b)$$

where W is the vector of intermediate variables. Using the building block in Fig.1, equations (8) can be realised by SI circuits. The one-to-one correspondence between the circuit elements and the matrix entries indicates that the efficiency of the SI implementation is related to the sparsity of the system matrices. To maintain the sparsity of the matrices, the well known LU, UL, or the direct methods which decompose matrix A into $\mathbf{AI_u}$ or $\mathbf{I_uA}$ ($\mathbf{I_u}$ is the identity matrix) can be used. A standard representation of the circuit produced by left decomposition of a typical 6th-order matrix system is shown in Fig.2.

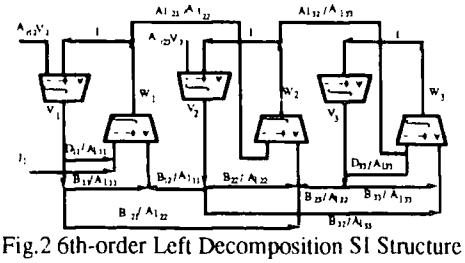


Fig.2 6th-order Left Decomposition SI Structure

Four relevant left decompositions follow:

Left-LU Decomposition

Let $\mathbf{A}=\mathbf{LU}$ (where L and U are the lower and upper triangular matrices respectively) then Eq.(8) becomes

$$\mathbf{LW} = (\psi\mathbf{B}+\mathbf{D})\mathbf{I}-(1+z^{-1})\mathbf{J} \qquad (9a)$$

$$\mathbf{UI} = -\phi\mathbf{W} \qquad (9b)$$

Left-UL Decomposition

If A is decomposed as $\mathbf{A}=\mathbf{UL}$, the system design equations are

$$\mathbf{UW} = (\psi\mathbf{B}+\mathbf{D})\mathbf{I}-(1+z^{-1})\mathbf{J} \qquad (10a)$$

$$\mathbf{LI} = -\phi\mathbf{W} \qquad (10b)$$

Left-IA Decomposition

For the case $\mathbf{A}=\mathbf{I_uA}$, the design equations are

$$\mathbf{W} = (\psi\mathbf{B}+\mathbf{D})\mathbf{I}-(1+z^{-1})\mathbf{J} \qquad (11a)$$

$$\mathbf{AI} = -\phi\mathbf{W} \qquad (11b)$$

Left-AI Decomposition

If $\mathbf{A}=\mathbf{AI_u}$, the following equations are obtained

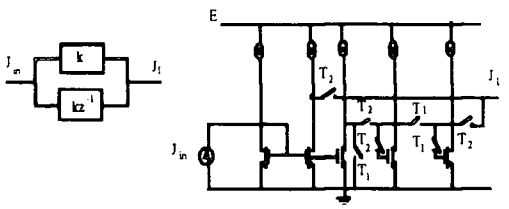
$$\mathbf{AW} = (\psi\mathbf{B}+\mathbf{D})\mathbf{I}-(1+z^{-1})\mathbf{J} \qquad (12a)$$

$$\mathbf{I} = -\phi\mathbf{W} \qquad (12b)$$

After matrix scaling, the input current J_1 in Fig.2 can be represented as

$$J_1 = k(1+z^{-1})J_{in} \qquad (13)$$

where J_{in} is prototype ladder input current and k is a constant. The schematic diagram for the realisation of J_1 is shown in Fig.3(a) and a suitable circuit realisation is given in Fig.3(b).



(a) (b)

Fig.3 Left Decomposition Input Factor SI Realisation

2.2. RIGHT MATRIX DECOMPOSITION APPROACHES

Matrix **B** can also be factorised as

$$\mathbf{B} = \mathbf{B}_l\mathbf{B}_r \qquad (14)$$

which leads to a group of right matrix decomposition methods. The following pair of equations is equivalent to Eq.(4).

$$\mathbf{AI} = -\phi(\mathbf{B}_l\mathbf{W}+\mathbf{DI})+\mathbf{J}(1+z^{-1})/(1-z^{-1}) \qquad (15a)$$

$$\mathbf{W} = \psi\mathbf{B}_r\mathbf{I} \qquad (15b)$$

From equations (15a) and (15b), a typical 6th-order system realisation structure can be obtained as shown in Fig.4.

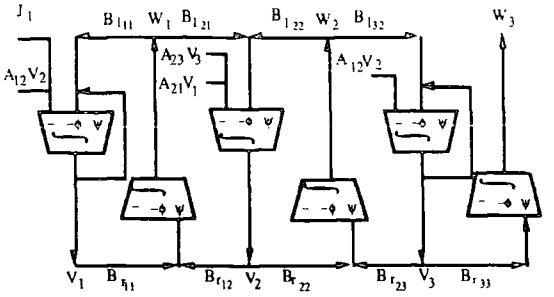


Fig.5 6th-order Right Decomposition SI Structure

Four right decompositi ns follow:

Right-LU Decomposition

If **B** is decomposed as **B=LU**, the design equations are

$$\mathbf{AI} = -\phi(\mathbf{LW}+\mathbf{DI})+\mathbf{J}(1+z^{-1})/(1-z^{-1}) \quad (16a)$$

$$\mathbf{W} = \psi\mathbf{U} \quad (16b)$$

For the lowpass case, the Right-LU Decomposition results in identical circuit structures to those derived by a leapfrog approach.

Right-UL Decomposition

Let **B=UL**, the system design equations become

$$\mathbf{AI} = -\phi(\mathbf{UW}+\mathbf{DI})+\mathbf{J}(1+z^{-1})/(1-z^{-1}) \quad (17a)$$

$$\mathbf{W} = \psi\mathbf{L} \quad (17b)$$

Right-IB Decomposition

If **B=IB**, the system design equations are

$$\mathbf{AI} = -\phi(\mathbf{BW}+\mathbf{DI})+\mathbf{J}(1+z^{-1})/(1-z^{-1}) \quad (18a)$$

$$\mathbf{W} = \psi\mathbf{I} \quad (18b)$$

Right-BI Decomposition

For **B=BI**, the following design equations are obtained

$$\mathbf{AI} = -\phi(\mathbf{IW}+\mathbf{DI})+\mathbf{J}(1+z^{-1})/(1-z^{-1}) \quad (19a)$$

$$\mathbf{W} = \psi\mathbf{B} \quad (19b)$$

The input current J_1 in Fig.5 is

$$J_1 = J_{in}\frac{1+z^{-1}}{1-z^{-1}} \quad (20)$$

This can be realised by any bilinear SI integrator. Fig.5 is the realisation structure based on the basic building block in Fig.1.

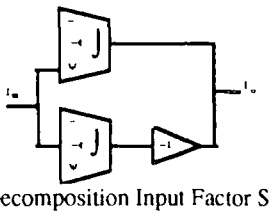


Fig.5 Right Decomposition Input Factor SI Realisation

3. CIRCUIT SCALING FOR SI FILTERS

Two kinds of scaling are involved in the matrix design approach, these are maximum dynamic range scaling and minimum transistor ratio scaling. Scaling within a general matrix system is very straightforward, for left and right decomposition methods, the equation

$$\mathbf{MX} = \mathbf{J} \quad (23)$$

can be utilised.

In the dynamic range scaling phase, a frequency sweep analysis of the filter passband is performed, to determine the maximum signal levels of the internal currents. Scaling can be done by multiplying column j of M by the maximum value of the variable X_j for all variables in X. This is equivalent to creating a new variable X_j/X_{jmax}, where X_{jmax} is the maximum value attained by X_j.

The ratio of maximum to minimum element value in **M** determines the transistor aspect ratios in SI circuit. For each row of equation in (21), a minimum entry can be found. By dividing each entry in the same row by the smallest entry, a scaled equation is obtained. The transistor aspect ratio can be reduced as long as the maximum and minimum elements are not within the same row of equations.

4. DESIGN EXAMPLE

The design method for ladder SI filter has already been implemented in XFILT[7]. An example of 10th-order bandpass filter is given here to show the utility of the approach. The filter has 1.5dB passband ripple with passband extending from 800kHz to 1.2MHz, 50dB stopband attenuation and a sampling frequency of 10MHz. The matrix entries translate directly to ratios of transistor width/length ratios (elsewhere called circuit coefficient values or simply g_m ratios). Comparative design results are shown in Table I, where the Left-UL is seen to be the most efficient realisation. By trying the all design methods, we can achieve, about 39.04% reduction in g_m spread and 38.73% reduction in g_m sum. The simulated Left-UL circuit response is shown in Fig.6 and Fig.7 shows the circuit schematic with the biasing circuits omitted. To compare the sensitivity performance, the total multiparameter sensitivity simulation over all g_ms has been carried out. The sensitivity simulation results of a comparative biquad realisation, having a maximum g_m spread of 63.78, are also presented in Fig.8. It is clear that the ladder based design demonstrates lower passband sensitivity, especially in the vicinity of the corner frequencies.

	Integs	SWs	g_m Spread	g_m Sum
Left-LU	10	34	16.32	813.04
Left-UL	10	34	14.55	727.02
Left-IA	10	34	21.93	1038.44
Left-AI	10	34	18.83	909.01
Right-LU	12	36	16.11	830.77
Right-UL	12	36	18.00	923.38
Right-IB	12	36	23.87	1186.68
Right-BI	12	36	16.11	836.49

Table I. Comparative design results for 10th-order bandpass SI filters

5. CONCLUSION

A new approach to realise exact ladder based SI filters has been presented. The bilinear transformation is used in the design procedures. Eight different SI ladder based structures can be obtained from one prototype ladder. Therefore it provides SI filter designers with a choice of circuit realisations based on different requirements such as power, area, maximum transistor aspect ratios, sensitivity or noise performance. Techniques to improve dynamic range and reduce circuit parameter spread are also presented. The proposed approach is well suited for a computer implementation and is already incorporated into the XFILT filter design system.

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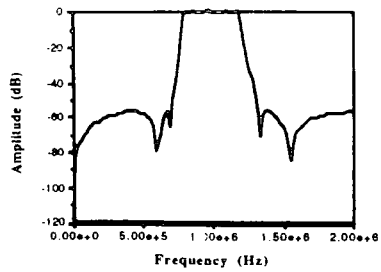

Fig.6 10th-order bandpass SI filter response

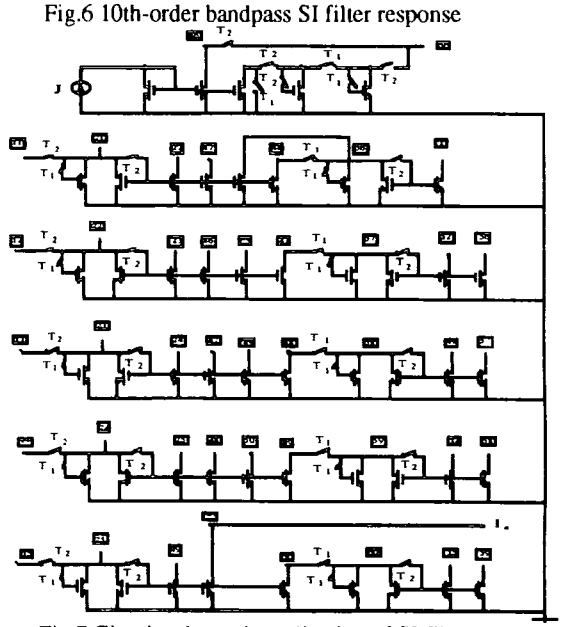

Fig.7 Circuit schematic realisation of SI filter

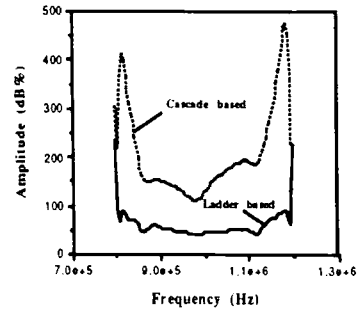

Fig.8 Sensitivity simulation of the SI bandpass filter

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MULTIRATE SC AND SI FILTER SYSTEM DESIGN BY XFILT

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ABSTRACT

Strategies and algorithms for multirate SC and SI filter design are presented in this paper. By using analogue multirate signal processing techniques, much more efficient SI or SC circuit realisations can be obtained. The paper shows how multirate systems can be synthesized within the filter design system XFILT.

1. INTRODUCTION

Analogue multirate signal processing techniques have developed in order to address some of the problems encountered in the progress towards single chip realisation of communication front-end systems and the extension to high frequency applications. The main aim of multirate SC systems is to relax the specifications of the anti-aliasing filters and the speed of some amplifiers, and also reduce the total capacitance and spread in narrow bandpass filters[1-3]. The interest in multirate SI systems is driven by similar arguments regarding containment of parameter spread and sum, and pre-filtering requirements.

2. MULTIRATE SYSTEM STRUCTURE

Fig.1 An analogue sampled-data filter system

The typical structure of an analogue sampled-data filter system, is illustrated in Fig.1. Traditionally only one clock frequency was employed in these systems. To improve system performance and reduce the cost, the sampled data filter can be a cascade of several sampled data filters using different sampling frequencies, as shown in Fig.2. Most popularly, the sampled data filter

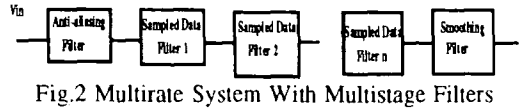


Fig.2 Multirate System With Multistage Filters

following the anti-aliasing filter becomes a decimator and the final sampled data filter becomes an interpolator, Fig.3.

Fig.3 Multirate System With a Decimator and Interpolator

To obtain much further reductions of the area, component spread and speed requirements; a multistage, multirate decimator and interpolator structure was developed, Fig.4. This structure also yields considerable savings in power consumption[4].

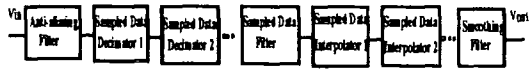


Fig.4 Multirate System With Multistage Decimator and Interpolator

Alternatively, another structure shown in Fig.5 can also be used to optimise the system performance.

Fig.5 Another multirate system

The decimators and interpolators have numerous implementations and the sampled data filter realisations divide into ladder-based and biquad configurations, each with a variety of circuit implementations in SC and SI. The scope for optimisation at the system level is quite apparent and the multirate extensions to XFILT [5] attempt to address this.

3. MULTIRATE SYSTEM DESIGN STRATEGIES

Various strategies for decomposing the design into multirate and multistage sections are known. An alternative scheme can be developed by consdering Fig.6 where a decimator implements a sampling rate decrease from MF_S to F_S and an interpolator implements a sampling rate increase from F_S to LF_S.

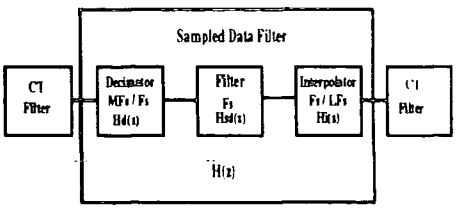


Fig.6 Multirate system design example

The transfer function of any decimator or interpolator can be expressed as

$$H_{d/i}(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_K z^{-K}}{1 + a_1 z^{-1} + a_2 z^{-2} + \ldots + a_N z^{-N}} \qquad (1)$$

where the unit delay period corresponds to the high sampling period $1/MF_S$ in decimator case or $1/LF_S$ in the interpolator case. A well known modification of the original z-transfer function (1) leads to [6].

$$H_{d/i}(z) = \frac{(b_0 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_K z^{-K}) \sum_{i=0}^{N(M-1)} c_i z^{-i}}{1 + d_1 z^{-1M} + d_2 z^{-2M} + \ldots + d_K z^{-KM}} \qquad (2)$$

$H_{d/i}(z)$ can be decomposed into two parts. Decompose $H_{d/i}(z)$ as:

$$H_{d/i}(z) = H_1(z)H_2(z) \qquad (3)$$

where

$$H_1(z) = \left[(b_0 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_K z^{-K}) \sum_{i=0}^{N(M-1)} c_i z^{-i} \right] \qquad (4)$$

and

$$H_2(z) = \frac{1}{1 + d_1 z^{-1M} + d_2 z^{-2M} + \ldots + d_N z^{-NM}} \qquad (5)$$

$H_1(z)$ is of FIR transfer function form with sampling frequency MF_C and can be realised by a FIR decimator structure. $H_2(z)$ is of the IIR transfer function form with sampling frequency F_S and can be realised by an IIR decimator.

The transfer function for the whole sampled data system is

$$H(z) = H_D(z)H_{SD}(z)H_I(z) \qquad (9)$$

where $H_D(z)$ represents the decimator transfer function, $H_{SD}(z)$ for middle filter transfer function and $H_I(z)$ for the interpolator transfer function. For the decimator and interpolator, the transfer function can also be expressed as low sampling frequency and high sampling frequency parts.

$$H_I(z) = H_{Ilow}(z)H_{Ihigh}(z) \qquad (10)$$

and

$$H_D(z) = H_{Dlow}(z)H_{Dhigh}(z) \qquad (11)$$

Therefore the whole system transfer function can be expressed as

$$H(z) = H_{Dhigh}(z)H_{Dlow}(z)H_{SD}(z)H_{Ilow}(z)H_{Ihigh}(z) \qquad (12)$$

Instead of following the traditional way by designing the decimator, SD filter and interpolator in straight cascade, a new design methodology is proposed consisting of two FIR filters with the higher sampling frequency and one IIR filter with the lower sampling frequency whose transfer function is

$$H_F(z) = H_{Dlow}(z)H_{SC}(z)H_{Ilow}(z) \qquad (13)$$

Correction of sin(x)/x effects is generally required in multirate designs and this is readily facilitated by XFILT within one section .

4. MULTIRATE FILTER DESIGN EXAMPLE

4.1 SI BANDPASS FILTER DESIGN

A simple example will illustrate the improvements that can be obtained in SI filter design. A video frequency bandpass filter with a passband from 4.25MHz to 6.8MHz, stopbands from 0.1Hz to 3.75MHz and from 7.25MHz to 60MHz, passband ripple 2dB and stopband attenuation 30dB, can be realised by an 8th-order elliptic filter using a cascade of four SI biquads with a single sampling frequency of 72MHz. Two critical parameters in the circuit realisation of SI filters are g_m spread (deriving from the spread of transistor aspect ratios) and g_m sum. A small g_m spread will maintain the accuracy of filter response and a small g_m sum will lead to a lower power consumption. The design results are given in Table I. To reduce the spread of transistor aspect ratio and g_m sum, a multirate multistage structure is adopted as shown in Fig.7, where the lowpass filter has a 72MHz sampling frequency and the highpass filter has a sampling frequency of 36MHz. The lowpass filter also has an anti-aliasing function up to 67MHz. The lowpass filter is realised by cascaded biquads and has a g_m sum of 547.81 units and a g_m spread of 26.19. The highpass filter is a ladder derived structure and has a g_m sum of 437.42 and a g_m spread of 19.79. The overall multirate SI system has a g_m sum of 985.23 and a g_m spread of 26.19. The multirate design technique has reduced the g_m sum by

40.0% and the g_m spread by 86.4%. The overall frequency response is given in Fig.8.

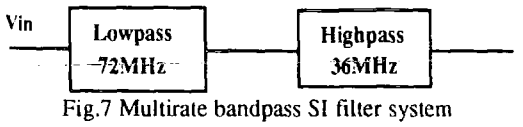


Fig.7 Multirate bandpass SI filter system

	g_mSpread	g_mSum
Single Rate	192.78	1651.73
Multirate	26.19	985.23

Table I. SI Filter Design Results

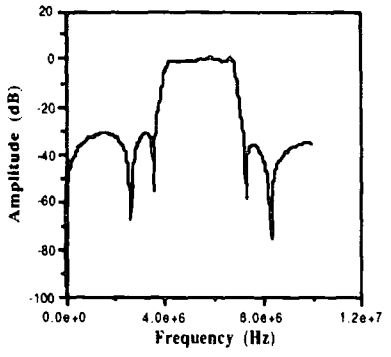


Fig.8 SI multirate bandpass filter response

4.2. NARROW BANDPASS BASEBAND FILTER DESIGN

The design of a narrow band SC bandpass filter is often complicated by large capacitance spread. One solution is shown in Fig.9. The centre bandpass filter with low sampling frequency will reduce capacitance ratio but give rise to unwanted alias and image frequency-translated components at low frequencies, which have to be attenuated using an anti-aliasing filter and an anti-imaging filter, respectively, with increased selectivity.

The design example [4] here is a bandpass filter with maximum ripple 0.28dB, desired midband frequency is 20kHz, and corresponding -3dB bandwidth is 480Hz. It is required that a minimum rejection of 40dB of the alias signals up to 300kHz. Below 300kHz, the frequency bands of the input continuous-time spectrum that relate to the desired system passband have to be attenuated, also by a minimum of 40dB.

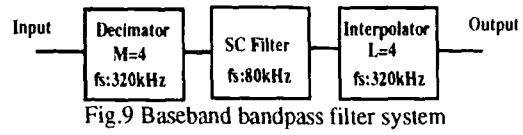
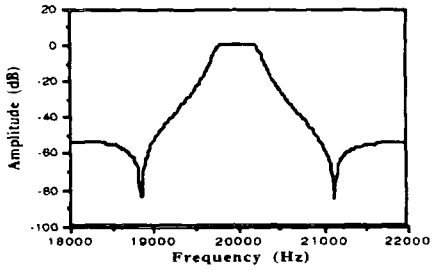


Fig.9 Baseband bandpass filter system

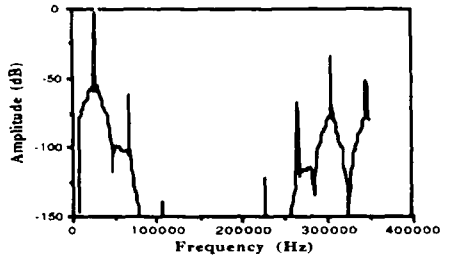
Table II shows the comparison of three different design results. Design 1 is a traditional design using a single rate clock of 320kHz. Design 2 obtains an optimum total capacitance and capacitance spread, with a reduction of 8dB of the signal handling capability of the SC filter[4] and Design 3 is without loss of signal handling capability[4]. Design 4 is a multirate system produced by XFILT, here the SC bandpass filter is realised by a ladder structure and the decimator and interpolator are implemented by cascading F-damped biquads. From Table II it can be seen that multirate systems have significant advantages over a single rate system in capacitance spread. Design 4 also leads to 64.86% and 39.19% reductions in capacitance spread and total capacitance respectively. Figs.10(a) and (b) give the filter responses around midband and over a wide frequency band. The cost of a multirate structure is the introduction of more opamps, switches and clock waveforms.

	Total C	C Spread	OPs	No. C	No. SW	No. Clock WF
Design 1	717.35	221.23	6	25	32	2
Design 2	972.50	87.80	12	57	75	9
Design 3	1002.3	151.10	12	57	75	9
Design 4	436.36	77.73	14	57	72	4

Table 2. Comparison of Baseband Bandpass Filter Design



(a)



(b)

Fig.10 Frequency response of baseband filter

4.3 SINGLE-PATH FREQUENCY-TRANSLATED SWITCHED-CAPACITOR BANDPASS FILTER SYSTEM

The single-path frequency-translated (SPFT) approach is a paricularly effective solution to the very narrow band

filter problem. The basic design performance parameters for a typical 80Hz bandwidth filter at 20 kHz are quoted from [1] and shown in Table 3, where Design 1 is a single rate realisation, and Design 2 a multirate implementation. The parameters of the scheme produced by XFILT are given as Design 3, and the overall system is shown in Fig.11.

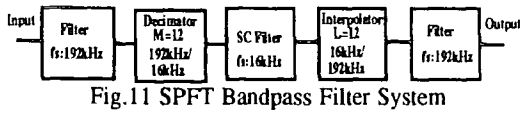
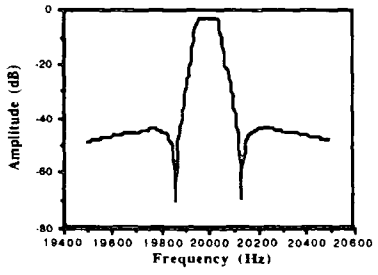
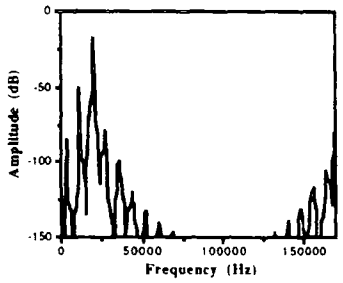


Fig.11 SPFT Bandpass Filter System

The first and last filters are simple 2nd order bandpass sections, the decimator and interpolator both have bandpass characteristics and the centre filter is ladder derived. Only 4 clock waveforms are used and the whole structure is strays-free.



(a)



(b)

Fig.12 SPFT system response

5.CONCLUSION

In this paper, some strategies and algorithms for multirate SC and SI filter design by XFILT have been presented. Several design examples demonstrate the utility of the multirate XFILT in producing improved solutions to difficult filter problems.

ACKNOWLEDGEMENTS

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	Total C	C Spread	No. OP	No. C	No. SW	No. Clock WF
Design 1	7942.70	1396.00	6	25	32	2
Design 2	1147.6	87.8	13	64	113	17
Design 3	434.39	66.22	14	59	78	4

Table 3. Comparison of SPFT System Realisation