A Low-Power, Reconfigurable Fabric Body Area Network for Healthcare Applications

by

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Abstract

Body Area Networks (BANs) are gaining prominence for their capability to revolutionize medical monitoring, diagnosis and treatment. This thesis describes a BAN that uses conductive fabrics (e-textiles) worn by the user to act as a power distribution and data communication network to sensors on the user's body. The network is controlled by a central hub in the form of a Base Station, which can either be a standalone device or can be embedded inside one of the user's portable electronic devices like a cellphone. Specifications for a Physical (PHY) layer and a Medium Access Control (MAC) layer have been developed that make use of the asymmetric energy budgets between the base station and sensor nodes in the network.

The PHY layer has been designed to be suitable for the unique needs of such a BAN, namely easy reconfigurability, fault-tolerance and efficient energy and data transfer at low power levels. This is achieved by a mechanism for dividing the network into groups of sensors. The co-designed MAC layer is capable of supporting a wide variety of sensors with different data rate and network access requirements, ranging from EEG monitors to temperature sensors. Circuits have been designed at both ends of the network to transmit, receive and store power and data in appropriate frequency bands. Digital circuits have been designed to implement the MAC protocols.

The base station and sensor nodes have been implemented in standard 180nm 1P6M CMOS process, and occupy an area 4.8mm^2 and 3.6mm^2 respectively. The base station has a minimum power consumption of 2.86mW, which includes the power transmitter, modulation and demodulation circuitry. The sensor nodes can recover up to 33.6μW power to supply to the biomedical signal acquisition circuitry with peak transfer efficiency of 1.2%.

Thesis Supervisor: Anantha P. Chandrakasan
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Chapter 1

Introduction

1.1 Background

Advances in low-power circuit design [1] have allowed computing to move to ever more smaller and power-efficient platforms. Nowhere has this revolution been more pronounced than in the domain of personal electronics, with the rapid proliferation of cellphones, tablets and laptops to the remotest parts of the world; devices that can do more than huge computers of the 1950s that took up a whole room, and at a fraction of the cost. Today, they are an integral part of our lives, affecting our work, entertainment and interactions with other people.

However, there is still one very important aspect of our lives where personal electronics have only begun to make a significant difference: healthcare. There has been a recent increase in the development and sales of some portable medical monitoring devices, such as pulse rate meters, temperature and blood pressure sensors, etc., but we are still far away from fully realizing the full potential of low-power electronics. Medical diagnostics and treatment is mainly limited to hospitals and doctors' clinics, and uses bulky equipment whose form factors haven't changed much in the past 30 years. A paradigm shift is needed in the way patient data is gathered and interpreted and the way patients are treated.

1.2 Motivation

An estimated 100,000 people die each year in the US as a result of treatable medical conditions, such as heart disease [2]. This figure is higher than most other causes of deaths, such as cancer, AIDS, road accidents, etc. This problem is more acute in developing regions of the world, where healthcare facilities severely lack the ability to fulfil the demand and emergency services are almost non-existent. Today's advanced sensors [3, 4, 5] can measure biological signals with microwatts of power. CMOS technology also offers the possibility of intergrating communication circuitry onto the same die, further reducing size and cost. The quality of healthcare that can be offered can be readily improved by using Body Area Networks (BAN) for continuous monitoring of vital signs [6]. Transferring data from sensors to a healthcare provider is realized as a two-step process: from the sensors to a local base station (like a cellphone) and from the base station to a healthcare provider using conventional data networks, as shown in Figure 1-1

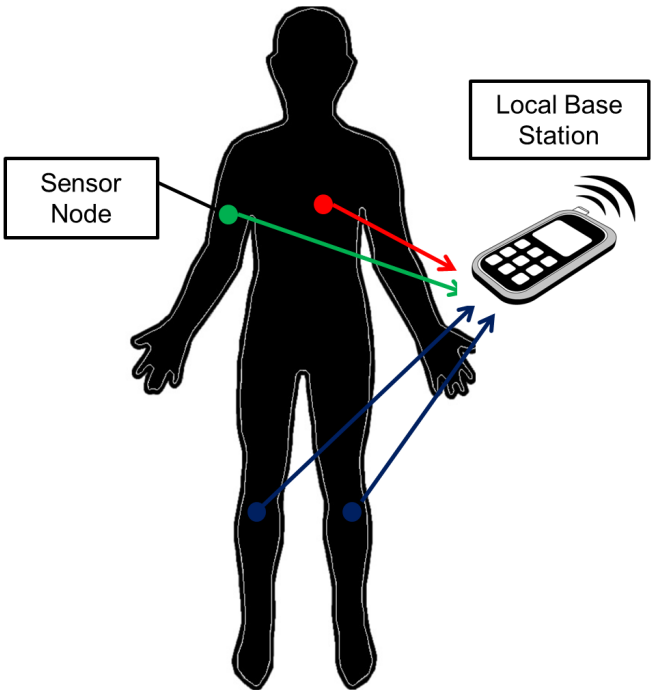


Figure 1-1: Body Area Network with Communication Link to the External World

However, some key challenges remain. The reduction in power consumption of biomedical sensors has not been accompanied by a commensurate increase in the cost of communication [7, 8, 9]. In fact, the power budget of most such SoCs is now dominated by the power required to transmit and receive information. BANs can be designed using e-textiles instead of radios. Conductive channels on clothing can be used to transact data with sensors placed all around the body. Additionally, the same network can also be used to deliver power to the sensors. This method has the potential to avoid most of the problems that plague low-power radios in BANs, such as high path loss around the human body and interference in the unlicensed bands they operate in.

1.3 Thesis Contributions

This thesis addresses the challenge of designing a Body Area Network using conductive fabrics capable of handling the tasks of power delivery and data transaction with sensor nodes placed around the body. Characteristics unique to medical BANs have been used to lower network power. These include the use of a star topology and that most health monitoring sensors acquire data at such low rates that data can be buffered and transmitted in bursts to the base station. The main contributions of the thesis to the area of Fabric BAN (FBAN) network design are listed below

- **Reliability**: Since conductive fabrics are exposed to wear and tear from prolonged use and frequent washing, a fault-tolerant network architecture for medical BANs has been developed using redundant access paths in order to improve network reliability. Further, the developed architecture is capable of operating effectively despite the poor tolerances of circuits fabricated on clothing.

- **Low Cost**: The designed network avoids the use of multiple active components on the e-textiles that increases routing complexity and cost. All active components reside on a single chip that is not bonded to the fabric. The only circuit components on fabric are screen-printed passives, which reduces produc-

tion cost.

- **Resonant Power Transfer**: A resonant power transfer scheme to sensors has been proposed, and a detailed theoretical background consistent with the implemented circuits is presented.

- **Bidirectional Data Transfer**: Modulation schemes have been implemented that push most of the communication complexity to the base station. Messages from the base station (downlink) are modulated with the transmitted power signal as carrier and with a very high SNR to reduce receiver power at the sensor nodes. Backscatter (impedance) modulation is used for messages from the sensors (uplink) that reduce the modulation effort at the sensors to the order of a few fJ/bit.

- **Access Protocols**: A complete Data Link Layer (DLL) has been custom-designed along with the Physical (PHY) layer of the network. This layer specifies the packet structures, error detection, and Medium Access Control (MAC) protocols for the network. The custom-DLL allows the network to take advantage of features offered by the network architecture, while avoiding the power overhead of standard DLLs that is unnecessary for medical BANs.

- **Flexibility**: The proposed Fabric BAN is flexible enough to allow different kinds of sensors with diverse functions and bandwidth requirements to co-exist within the same network, by the use of a hybrid MAC scheme.

A block diagram of the proposed system is shown in Figure 1-2. Sensor nodes of a band-aid patch form factor are placed on the body of the user and are connected to the fabric network through an inductive link. A single inductor on clothing may be shared by multiple sensors. Sensors can have different front-end acquisition circuitry for measuring different signals, but share a common network module. The network module handles modulation, demodulation, data buffering, power recovery and network access decision-making. Power transmitted by the base station and bi-directional data traffic are multiplexed on the same channel on fabric. The base

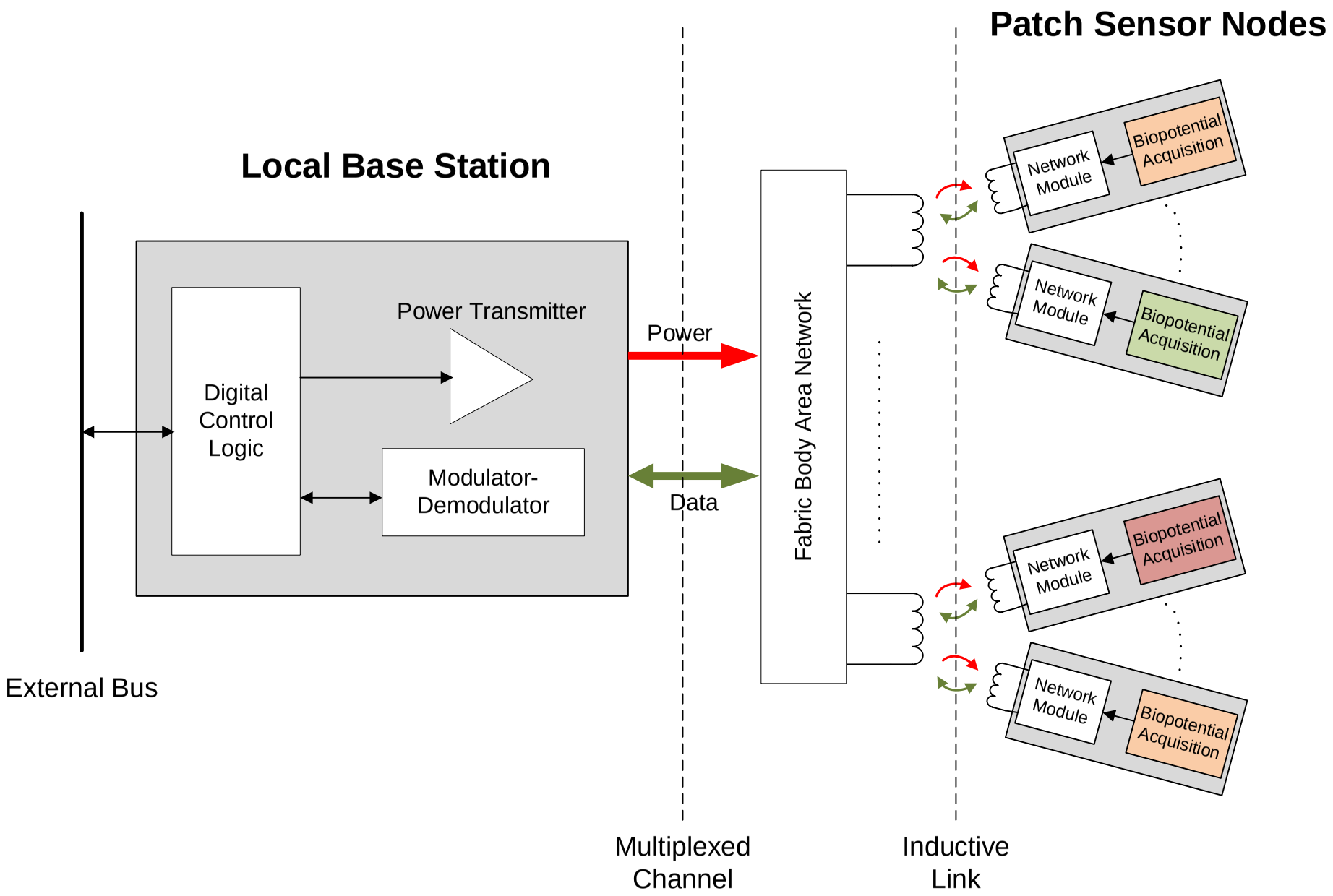


Figure 1-2: Block Diagram for the Proposed Fabric Body Area Network (FBAN)

station contains RF power transmiter circuits, modulators, demodulators and digital logic that implements the custom DLL. The digital logic on the base station can be interfaced with the I/O bus of the electronic device carried by the user it resides in.

1.4 Thesis Outline

Chapter 2 of the thesis will present an overview of previous research done in the field of Body Area Networks using e-textiles, and develop specifications for the architecture and DLL of the designed network. Chapter 3 presents the conductive fabrics used for the network and lists some of their characteristics. Chapter 4 presents circuits used for transmitting power to the sensor nodes and circuits used at the sensor node to convert it to DC power. Chapter 5 presents the circuits used for modulation and demodulation of uplink and downlink data. Chapter 6 presents the DLL used, with the packet structures, MAC protocols and error detection scheme used. Details of CMOS implementation and measurement results are presented in Chapter 7. Finally, Chapter 8 presents a summary of the work done and future research work possible in the area.

Chapter 2

Design Targets

The previous chapter presented the motivation behind designing Medical BANs using conductive fabrics. This chapter presents a brief overview of existing BAN schemes, both standardized and academic. An architecture for the BAN is proposed and the accompanying network access scheme is discussed.

2.1 Wireless BAN Design Space

The IEEE 802.15.6 Wireless Body Area Network (WBAN) standard [10] specifies a detailed PHY and MAC layer structure for WBANs. It supports three PHYs, as listed below

Human Body Communication (HBC): This technique uses the human body as the transmission channel to communicate with sensors. Transceivers operate at frequencies high enough not to have large attenuation constants, but not too high for the body to start acting as an antenna and interfering with radios in other bands. This falls in the $10-100$MHz range. Thus, signals can be localized to the human body and a cellular network architecture need not be considered. Nevertheless, such networks can still pick up interfering signals emitted by other radios in the band. Communication at up to 2Mb/s with 0.1nJ/bit have been demonstrated in [11, 12]. However, steps need to be taken to ensure the integrity of the signal at the receiver in the presence of high-power interferers.

Ultra-Wideband (UWB) Radios: UWB radios operate by transmitting extremely short duration GHz-frequency pulses wirelessly that distribute the transmitted energy over a 500MHz-wide band. This ensures that the transmitted power spectral density is below the FCC masks for unintended radiators. Ultra-low power operation is achieved by avoiding the use of power-hungry gigahertz oscillators and phase-locked loops (PLLs), and instead using purely digital architectures. A 17.5pJ/pulse transmitter and a 110pJ/bit receiver have been reported in [8] and [13] respectively. However, these radios still have to contend with high-power commercial narrowband radios operating within the transmitted bandwidth.

Narrowband (NB) Radios: These radios usually operate in one of the unlicensed Industrial, Scientific and Medical (ISM) bands. Narrowband radios designed for WBANs are intended for operating over distances in the range of 1-2m, and use architectures suitable for operation at low power. State-of-the-art narrowband transmitters and receivers using Film Bulk Acoustic Resonators (FBARs) [14, 15] can operate at 483pJ/bit and 180pJ/bit respectively at 1Mbps.

None of these PHYs listed above is suitable for ultra low-power and compact sensors without any local energy source. HBC has a transmit mask with a limit of -36dBm on the maximum transmitted power, in order to avoid potential tissue damage and interference with critical medical aids such as pacemakers. UWB also has a spectral mask to prevent interference with narrowband radios operating over the wide bandwidth. NB radios are more suitable, but most unlicensed bands correspond to regions with high attenuation constants, which makes power transfer inefficient. Electronics integrated with the clothing a person wears offer the capability to combine wireline transmission on clothing with a wireless link that can operate at extremely low power due to the proximity of clothes to the body. This permits the use of near-field coupling in order to operate at a lower frequency, and hence lower power. Thus, e-textile BANs have a great potential to simultaneously deliver power to sensors in the network and transact data with them.

2.2 Previous Work

Although no commercial standard for FBANs exists, a number of e-textile BANs for medical purposes have been proposed in literature. The network presented in [16] uses fabrics with conductive wires interwoven among the threads. Links to the sensor nodes are completely wireline with a snap-button that connects the clothing to the sensor. The same link is used to transmit both power and data. Although this helps in achieving extemely energy-efficient communication through supply-rail coupling, it lacks quick reconfigurability and can be cumbersome for users. A similar fully-wireline communication scheme is proposed in [17] for sleep monitoring by linking sensors placed around the head.

A chest band using conductive fabrics has been proposed in [18]. The chest band has the capability to connect inductively to multiple sensors of a band-aid patch form factor in order to deliver power and transact data. However, the chest band has to be tightly fitted on the user's body for operation and it adds an additional piece of clothing, which could cause discomfort to the user. It also limits the regions where sensors can be placed to be covered by the network. The design presented in this thesis will aim to integrate such inductively-linked sensors using everyday clothing, and deliver power and transact data with them, thus leading to better coverage of all parts of the body without sacrificing comfort. Some features of existing designs are compared with features in the proposed design in Table 2.1.

2.3 Network Architecture

Figure 2-1 shows the top-level Fabric Body Area Network (FBAN) schematic on a shirt, as an example. The base station is connected to traces on the fabric by means of a snap-button interface *matrix*. The base station would typically reside in, and be powered by a portable electronic device carried by the user. Sensors are of a band-aid form factor, and are connected to the network by means of a near-field inductive link formed between an inductor on the shirt and an inductor on the band-

Feature	**Mercier, et al. [16]**	**Lee, et al. [17]**	**Yoo, et al. [18]**	**This Work**
Communication Mode	Wireline	Wireline	Inductive-Coupling+ Wireline	Inductive-Coupling+ Wireline
Power Transfer Mode	Wireline	Wireline	Inductive	Resonant Inductive
Reconfigurability	Limited	Moderate	High	High
Coverage	Extensive	Localized	Localized	Extensive
Fault-Tolerant	No	No	No	Yes

Table 2.1: Comparison of Features of Previous Work with Proposed Design

aid sensor patch. Each of the snap-buttons links to a group of three inductors, which are connected in parallel with each other. For simplicity, the connections to only one of the inductor terminals are shown. The three parallelly-connected inductors form a *sub-network*, and have more than one path from the snap-button matrix to the group. The entire network consists of a group of such sub-networks, each with as many or as few inductors as required that are placed at strategic locations where there is a possibility of acquiring health data. The use of such a network architecture has several advantages.

Since power is to be transmitted to the sensors via inductive links, it is imperative to only transmit power to those inductors on the clothing that actually have sensors underneath the clothing to prevent wastage of energy. Since the network is intended to be used for all kinds of healthcare sensors with inductors placed at all possible spots where data can be acquired, it is obvious that not all users will have all possible kinds of sensors on their bodies and hence a lot of the inductors would have no sensor underneath. Inductor locations can be grouped into sub-networks depending on the type of data a sensor placed at a particular location might acquire. For example, places where ECG data can be acquired have inductors that are in the same sub-network. This functional classification allows sub-networks to be turned on and off depending on what kind of sensors a user has on their body. Further, the network also allows multiple sensors to be connected via the same inductor.

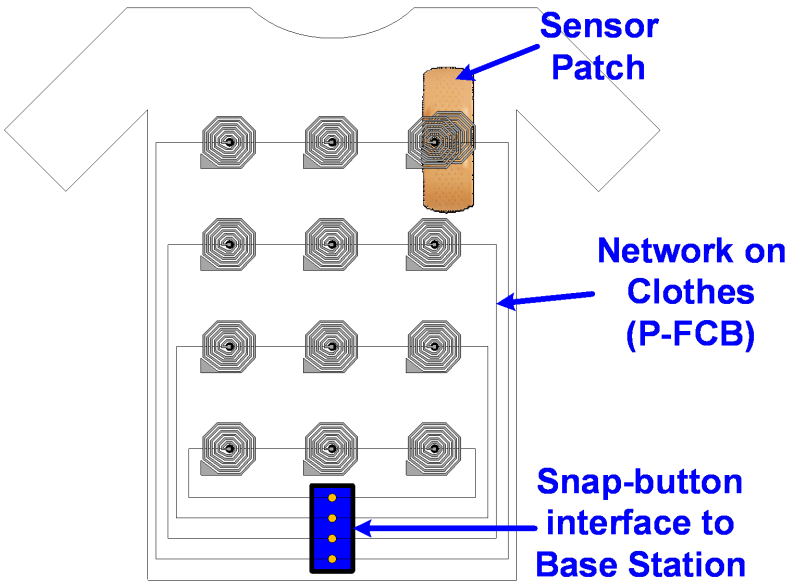


Figure 2-1: Example of a Fabric BAN on a Shirt. The return paths for the inductor currents are not shown for simplicity.

Since each sub-network has more than one path going to all inductors, network robustness against one of the conductive paths getting open-circuited increases. This is an extremely important issue for networks on conductive fabrics. Since clothes are subject to the rigors of daily use and are washed regularly, the possibility of conductive traces eroding away to increase the trace resistance or even form an open-circuit is quite high. Having redundancy in the network allows for greater fault-tolerance and lesser need to replace the conductive clothing.

The network has a star topolgy, with only two possible kinds of data packets, from the base station to the sensor nodes and from the sensor nodes to the base station. The former is called *downlink* while the latter is called *uplink*. Table 2.2 summarizes the nomenclature.

	Downlink (*Multicast*)	**Uplink** (*Unicast*)
Transmitter	Base Station	Sensor Node
Receiver	Sensor Node	Base Station

Table 2.2: Nomenclature for Network Data Traffic

The block diagram of the base station for the network is shown in Figure 2-2. Groups of parallel inductors are fabricated on conductive fabric to form sub-networks. Each sub-network has its dedicated RF oscillator, power amplifier (PA) and downlink modulator. A resonant LC tank is used to increase the voltage amplitude across the inductors, which translates to a larger voltage at the secondary. A controller decides which sub-networks to turn on depending on the user's input about the kind of sensors on the body that need to be connected to the network. This way, messages can be broadcast to *all* sensors in the network, or just to sensors in any subset of the group of sub-networks. Uplink data from different sub-networks is combined asynchronously to form a single uplink stream. This is necessary since the MAC (discussed in Section 6.2) has modes wherein the base station does not know which sensor node will be the next one to transmit. The on-chip digital baseband circuitry performs the tasks of network scheduling, error checking and external memory interfacing. The base station designed is capable of supporting two sub-networks with up to two inductors each.

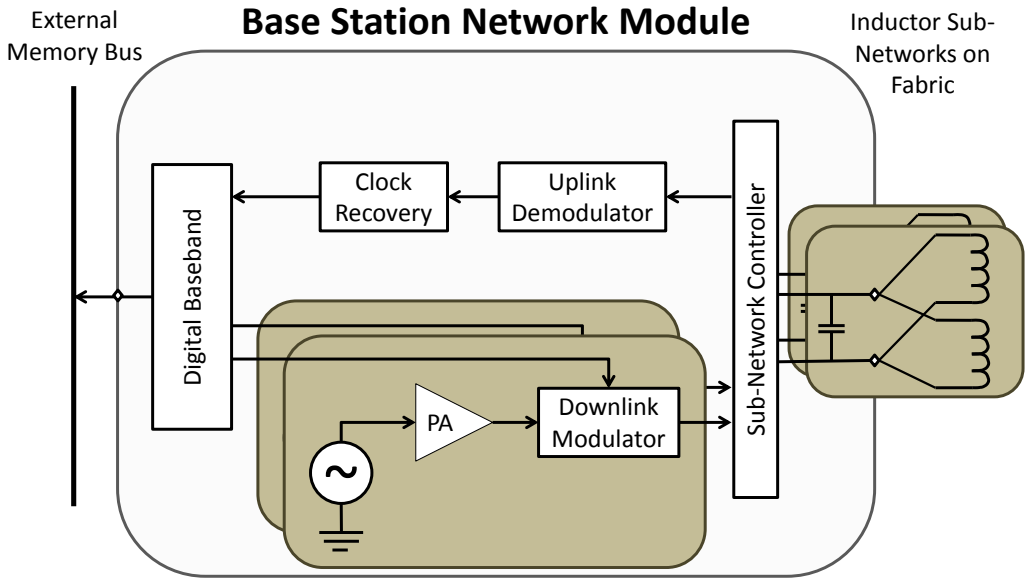


Figure 2-2: Block Diagram for Base Station

The block diagram for the sensor node is shown in Figure 2-3. A Sensor Node Network Module that can interface to any healthcare sensor front-end is proposed. The

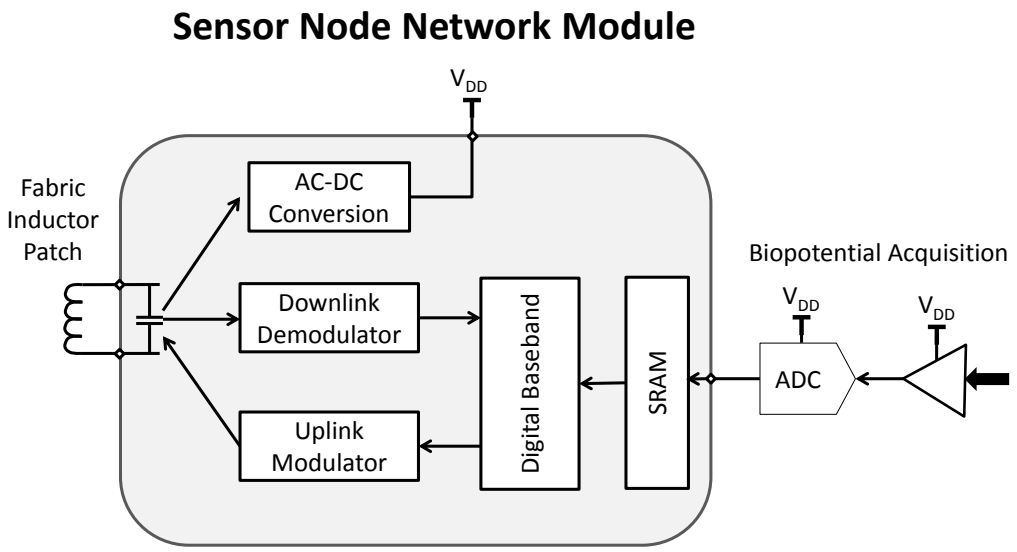


Figure 2-3: Block Diagram of Sensor Node with Front-End and Network Module

Analog Front-End (AFE) of the sensor consists of an analog amplifier and an ADC. The ADC output is buffered in an SRAM, which has been integrated in the network module. The SRAM is interfaced with an impedance modulator in order to transmit uplink data. A demodulator is also included to receive network access and configuration instructions from the base station. An AC-DC converter has been implemented for powering all circuits in the sensor, along with modulation and demodulation circuitry for uplink and downlink respectively. The on-chip digital baseband handles the job of interpreting messages sent by the base station and error-coding the transmitted packets. An inductor patch forms the inductive link to the network, and is part of a resonant LC tank with an on-chip capacitor.

2.4 Network Access Protocols

An efficient network access mechanism is needed to manage the potentially large number of sensors that might be connected to the proposed fabric BAN. Medium Access Control (MAC) protocols popularly used in BANs like Bluetooth, Zigbee and IEEE 802.15.6 support a number of features that are unnecessary for a BAN on conductive fabrics. Using any of these MAC schemes would result in a huge energy

overhead. The custom-designed Data Link Layer that contains the MAC has a number of salient features well-suited for fabric BANs, as listed below

- Sensor nodes access the network on a "listen-before-transmitting" basis. This allows the sensor nodes to go into sleep mode for an indefinitely long period of time without the need for clock synchronization with the base station at regular intervals.

- Since sensor nodes do not start transmitting before the base station instructs them to do so, a half-duplex link is sufficient. The base station maintains priority over transmission and ceases transmitting when it has instructed a sensor to start transmitting.

- A wide variety of sensor nodes, with different network access needs, are supported by the network. This is done by dividing network time into slots, each with access schemes suited to a particular kind of sensor node. The ratio in which this division is done can be altered based on the kinds of sensors in the network.

- A simple, yet effective error-detection scheme using Cyclic Redundancy Check (CRC) has been employed to protect against occasional packet errors. An Automatic Repeat Request (ARQ) scheme has also been implemented that tries to decrease error rates in successive re-transmissions of the same message.

The network access protocols implemented can support up to 16 sensors. Thus, the network can support up to 16 sensors linked to up to four wearable fabric inductors. The design can be easily scaled to support more sensors and more fabric inductor locations.

Chapter 3

Printed Circuits on Fabric

The previous chapter developed the specifications for the architecture and protocols associated with the BAN to be designed. This chapter presents an overview of the fabrics used in the network. The manufacturing process, electrical and mechanical properties of the conductive fabrics are presented. Characteristics of passives (resistors, inductors and capacitors) fabricated on the fabrics are also presented.

3.1 Fabrication Techniques

Numerous approaches have been presented for integrating electronics into textiles. Early attempts, mainly pursued by the Center for Wearable Computing at the Swiss Federal Institute of Technology (ETH), Zurich and Georgia Institute of Technology, Atlanta [19] were focused on wearable computing. These approaches relied on insulated conductive wires interspersed among the threads of the fabric, as described in [20]. Gigahertz transmission lines [21] and antennas [22] were designed by ETH Zurich, while on the digital side Georgia Tech developed the Smart Shirt [23] and the Wearable Motherboard™ [24]. While capable of forming interconnects and packages on fabric, these fabrication methods suffer from several drawbacks. Owing to the way yarn is woven to make a fabric, only perpendicular routing is possible. Moreover, physical properties of the conductive wires like the diameter, thermal expansion coefficient and Young's Modulus need to be matched with the yarn, which severely

restricts the choice of fabric.

The work described in this thesis uses fabrics that are produced through a different process. Conductive fabrics are produced using the screen-printing method described in [25, 26]. A conductive ink paste composed primarily of silver in an adhesive mixture can be used on a variety of fabric substrates. In mimicking the process used to manufacture electronic circuits on semiconductors itself, the screen-printing method offers portability of manufacturing steps between the two. Wires as thin as $200\mu m$ spaced as close as $200\mu m$ apart can be realized on fabrics with dense thread counts and fine fibers. However, fabrics produced using the screen-printing technique have smaller bandwidth compared to fabrics that use interwoven wires due to the large parasitic substrate capacitance.

3.2 Electrical Characteristics and Robustness

This section presents a brief overview of the measured electrical characteristics of e-textiles fabricated on a polyester substrate as described in [26]. The DC sheet resistance of a $10\mu m$ thick and 1mm wide wire on an unwashed fabric has been measured to be $0.23\Omega/\square$. Washing and wear and tear due to everyday use affects the DC resistance very strongly. In tests performed by Kim et al., the DC resistance value of the wires is reported to have increased by upto 40x after 20 washes, which indicates rapid thinning leading ultimately to an open connection. Coating the wires with a passivation material such as polyurethane reduces the effects of washing up to only a 2x increase after 50 washes.

The AC line impedance of a $10\mu m$ thick Ground-Signal-Ground coplanar waveguide printed on a $100\mu m$ fabric substrate has been measured to be 201.8Ω. The waveguide has 21.8pF/m parallel capacitance and 891.3nH/m series inductance. S_{21} measurements show a 3dB cutoff frequency at 80MHz with approximately 0.5dB loss at DC. Both DC and AC characteristics show little variation with wrinkling of the fabric. Table 3.1 provides a summary of the electrical characteristics.

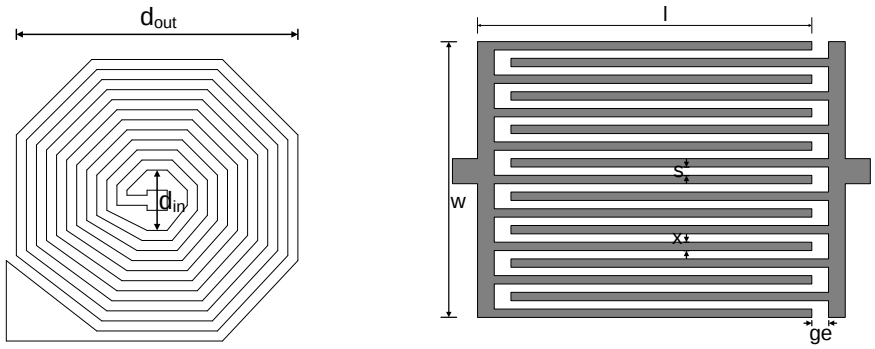
Property	Value
DC Resistance ($T = 10\mu m$, $W = 1$mm)	2.3Ω/cm
AC Line Impedance	201.8Ω
s_{21} 3dB Bandwidth	80MHz
Parallel Capacitance (C_p)	21.8pF/m
Series Inductance (L_s)	891.3nH/m

Table 3.1: Electrical Characteristics of Screen-Printed Wires on Polyester Substrate [26]

3.3 Passive Components

Resistors

Resistors can be realized on fabric using a meandering structure similar to integrated circuits on silicon. Like silicon, it is difficult to get large resistance values in a limited area due to small sheet resistance. A 300mm long and 1mm thick meandering wire occupying a space of 25mm×25mm yields only 85Ω resistance, which corresponds to a sheet resistance of 0.28Ω/□.



(a) Octagonal Spiral Inductor

(b) Interdigitated Capacitor

Figure 3-1: Layout of Passive Components on Fabric

Inductors

Inductors can be realized using square, hexagonal or octagonal spirals. An octagonal spiral inductor is shown in Figure 3-1(a). The inductance value is given by

Equation 3.1, which has been derived in [27].

$$L = K_1 \mu \frac{n^2 d_{avg}}{1 + K_2 f} \tag{3.1}$$

where d_{avg} is the arithmetic mean of the inner and outer diameters, n is the number of turns, μ is the permeability of the fabric, which can be approximated as μ_0, the permeability of free space and f, the *fill ratio* is defined as

$$f = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \tag{3.2}$$

The constants K_1 and K_2 are 2.25 and 3.55 respectively for octagonal spiral inductors. The inductor in Figure 3-1(a), designed with $n = 6$, $d_{in} = 6$mm, $d_{out} = 32$mm and wire thickness of 1mm evaluates to $L = 1.8\mu H$. The inductors have $Q \approx 8$ in the $20 - 40$MHz range[1] and self-resonant frequency $f_c \approx 100$MHz, beyond which they are capacitive.

Capacitors

Both parallel-plate and interdigitated capacitors can be fabricated on fabric. An interdigitated finger capacitor is shown in Figure 3-1(b), where s is the finger spacing, x is the finger width, l is the finger length, w is the terminal width and ge is the end gap. The capacitance value is given by Equation 3.3, which has been derived in [28].

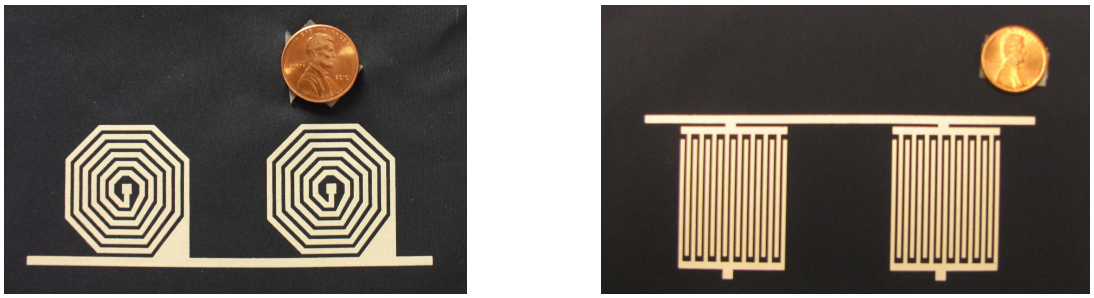
$$C = \frac{\epsilon_r \epsilon_0 + 1}{d} l[A_1(n-3) + A_2]. \tag{3.3}$$

In Equation 3.3, n is the number of fingers and ϵ_r is the relative permittivity of the fabric. A_1 and A_2 represent the contributions of the internal and two external fingers of the capacitor respectively and are functions of (t/x), where t is the thickness of the wire. The evaluated capacitance of a capacitor with $x = 1$mm, $s = 1$mm, $n = 8$, $t = 10\mu m$, $ge = 2$mm, $l = 38$mm and $w = 33$mm is 16pF.

[1] Section 4.2 elaborates on the choice of the inductance and capacitance values and the frequency range of interest

3.4 Measured Component Values

Fabric inductors and capacitors with specifications as described in Section 3.3 were fabricated on a polyester substrate, as shown in Figure 3-2. Inductance and Capacitance values in the desired frequency range of $20 - 30$MHz were measured using a Network Analyzer. Twelve inductor and capacitor samples were analyzed, and the average inductance and capacitance values were observed to be $1.4\mu H$ and 20pF respectively compared to $1.8\mu H$ and 16pF expected from Equation 3.1 and Equation 3.3.



(a) Spiral Inductors (b) Interdigitated Capacitors

Figure 3-2: Passives Fabricated on Polyester Substrate

Histograms for the measured inductance and capacitance values are shown in Figure 3-3. Even though the sample size is small, variations up to 50% can be observed in some of the samples. This indicates extremely poor tolerances, which are due to fabric-to-fabric variation and imprecisions of the screen-printing process.

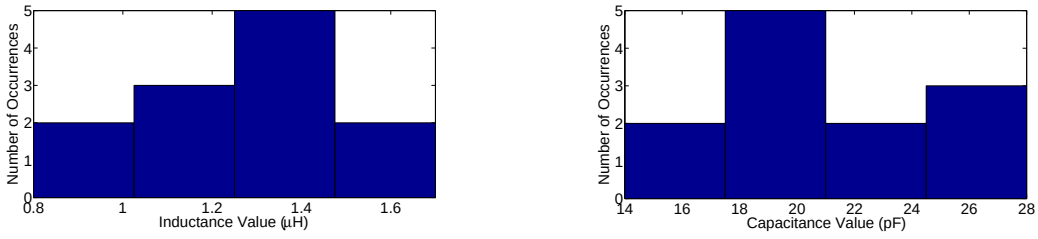


Figure 3-3: Measured Component Values of Passives on Fabric. Expected Inductance and Capacitance Values were 1.8μH and 16pF respectively.

The quality factor (Q) and self-resonant frequency (f_R) of the inductors as measured by the network analyzer were $Q \approx 8$ in the $20 - 40$MHz frequency range and

$f_R \approx 100$MHz. The inductive coupling coefficient between the inductors on fabric is extremely sensitive to variations between fabrics as well as the operating conditions, like the profile of wrinkles on fabric, etc. Table 3.2 lists some measured coupling coefficient values.

Distance between Inductors	**Coupling Coefficient (k)**
5mm	0.08
3mm	0.14
2.5mm	0.2
2mm	0.24

Table 3.2: Inductive Coupling Coefficient Values for Different Spacings Between Inductors

Chapter 4

Wireless Power Transfer

The previous chapter presented an overview of the fabrics and passive components fabricated on them that are used in the network. This chapter develops the theory for inductive power transfer through coupled resonators. Specifications for network parameters are developed based on limitations enforced by the fabric characteristics as well as regulatory authorities. The circuits for resonant AC power transmission and AC-DC conversion at the sensors are also presented.

4.1 Theoretical Overview

This section presents a brief theoretical overview of power transfer through inductive links, as described in [29]. Figure 4-1 shows the setup used, with side 1 being the primary and side 2 being the secondary. The load resistance R_L on the secondary is the equivalent AC resistance of the circuit that converts AC power to DC. A resonant RLC tank circuit is used on the primary side to achieve maximal voltage across the inductor. A tank is also used on the secondary side to increase the voltage input to the rectification circuit. It is assumed that both the primary and secondary networks have the same resonant frequency.

In Figure 4-1, $Z_1(s)$ is the series combination of L_1 and R_1, while $Z_2(s)$ is the series combination of L_2, R_2 and the parallel combination of C_2 and R_L. A detailed mathematical treatment of the mechanism of power transfer through inductively-

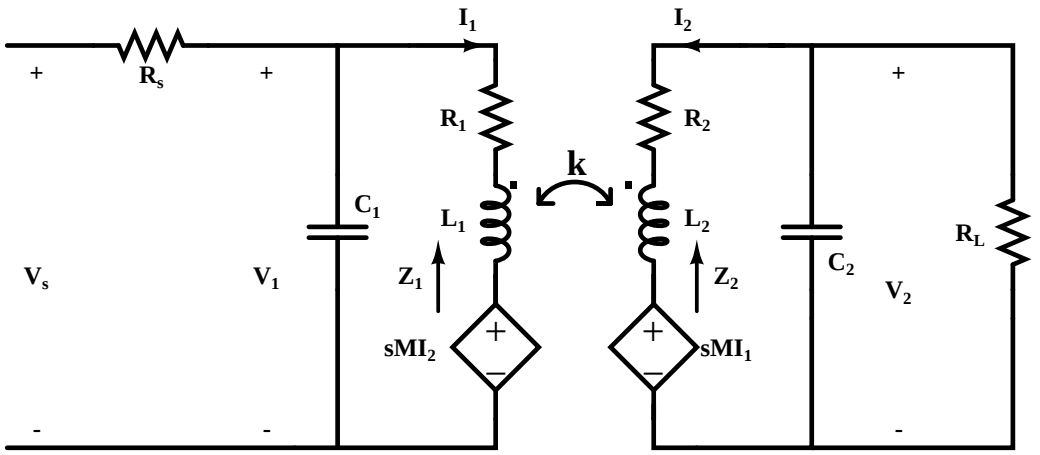


Figure 4-1: Power Transfer through Inductively-Coupled Resonators

coupled resonators is presented in Appendix B. The power transfer efficiency from the source on the primary side to the load on the secondary side is

$$\eta = \eta_1 \cdot \eta_2 \tag{4.1}$$

$$= \left(\frac{Q_1'^2 R_1 \left(1 + k^2 Q_1 Q_2'\right)}{R_s + Q_1'^2 R_1 \left(1 + k^2 Q_1 Q_2'\right)} \cdot \frac{k^2 Q_1 Q_2'}{1 + k^2 Q_1 Q_2'} \right) \cdot \left(\frac{Q_2}{Q_2 + Q_L} \right) \tag{4.2}$$

where Q_1, Q_1', Q_2 and Q_2' are the unloaded and loaded quality factors of the primary and secondary resonators respectively, Q_L is the quality factor of the load and k is the inductive coupling coefficient.

4.2 Link Design

The measurement results presented in Section 3.4 show that the fabric inductors self-resonate at around 80MHz, beyond which they behave as capacitors. Further, the s_{21} parameter of wires screen-printed on fabric has a 3-dB cutoff frequency at 80MHz. Given these constraints, it is preferable for the inductive links to operate a few octaves below these frequency values. Also, even though inductive links have limited far-field energy, it is advisable to operate in an unlicensed band nevertheless to avoid interfering with sensitive radios in licensed bands. Inductors are not good at picking up far-field radiation and hence interference from other radios transmitting in

the same band is not an issue. A study of available frequency bands in the $5-30$MHz range [30] yields three unlicensed ISM bands at 6.78MHz, 13.56MHz and 27.12MHz. The 27.12MHz is the most appropriate band to operate in for the following reasons

1. The bandwidth in the 27.12MHz band is 326kHz, compared to 40kHz in the 6.78MHz band and 14kHz in the 13.56MHz band.

2. LC oscillators at 27.12MHz need L and C values of the order of $1\mu H$ and a few tens of pF. Both can easily be obtained by on-fabric spiral inductors and interdigitated capacitors that measure $3-4$cm in each dimension. Capacitors of these values can also be easily realized on a chip with reasonable area.

3. The frequency band is still sufficiently away from the inductors' self-resonant frequency and the s_{21} 3-dB cutoff frequency.

As outlined in Section 3.3 and Section 3.4, the screen-printed inductors on fabric have poor quality factors. Assuming the quality factor of the LC circuits are limited by the inductor alone[1] leads to $Q_1, Q_2 \approx 8$. In order to get a sense of the power numbers involved, assume that the rectification circuit at the secondary needs to supply $30\mu A$ at $1.8V$, with a 50% power conversion efficiency and an AC input voltage amplitude $V_{ac,in} \approx 2.4V$. Assuming unity power factor at the input of the rectification circuit, i.e. the power transfer frequency perfectly matches the resonant frequency of the secondary tank, the recitifier consumes an AC input current $I_{ac,in} \approx 90\mu A$. This corresponds to $R_{L,ac} = 26.7k\Omega$.

With an inductor value $L \approx 1.4\mu H$ and capacitor value $C \approx 24$pF oscillating at 27MHz, $Q_L = 110$. Since $Q_2 \ll Q_L$, $Q_2' \approx Q_2$ which implies that the primary efficiency given by Equation B.15 is invariant with the load. It also leads to the total efficiency being dominated by the secondary, and can be increased by keeping Q_L, and hence $R_{L,ac}$ as low as possible. This increases $R_{L,srs}$, the effective series AC load resistance, and causes more power to be dissipated across the load than across R_2. For $L_1 = L_2 = 1.4\mu H$, $C_1 = C_2 = 24$pF, $Q_1 = Q_2 = 8$ and $R_s = 1.3k\Omega$, the transfer

[1] subsection 4.3.2 justifies this assumption

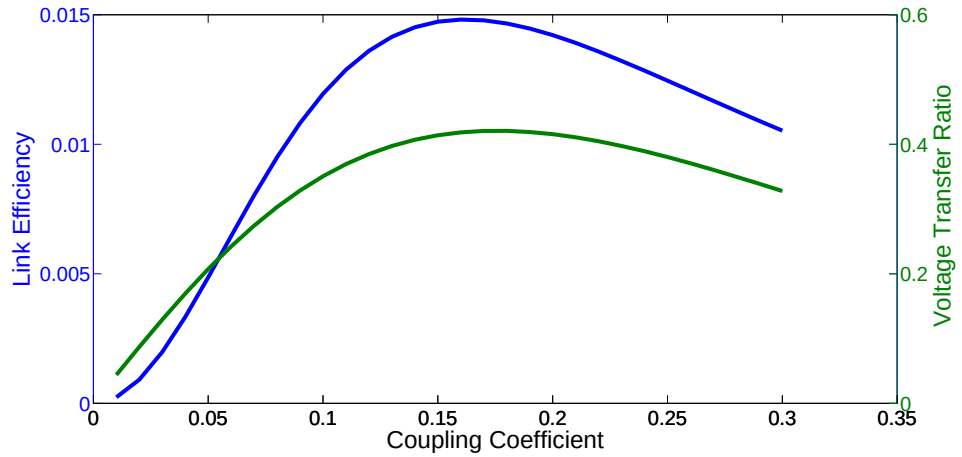


Figure 4-2: Simulated Link Efficiency and Voltage Transfer Ratio vs Coupling Coefficient. Calculated for $R_L = 26.7k\Omega$, $R_s = 1.3k\Omega$, $L_1 = L_2 = 1.4\mu H$, $C_1 = C_2 = 24$pF, $Q_1 = Q_2 = 8$.

characteristics are plotted in Figure 4-2. More details for the case where the inductive coupling coefficient $k = 0.1$ are summarized in Table 4.1.

Parameter	**Value**
Primary Efficiency (η_1)	18%
Secondary Efficiency (η_2)	6.8%
Total Efficiency ($\eta = \eta_1 \cdot \eta_2$)	1.2%
Voltage Transfer Ratio $\left\lvert\frac{V_2(s)}{V_s(s)}\right\rvert$	0.35

Table 4.1: Inductive Power Transfer Characteristics for Coupling Coefficient $k = 0.1$

Figure 4-2 shows that for the given link parameters, an inductive coupling coefficient value $k \approx 0.15$ is optimal for maximum power transfer efficiency and for generating maximum voltage across the input terminals of the rectification circuit, which leads to better AC-DC conversion performance.

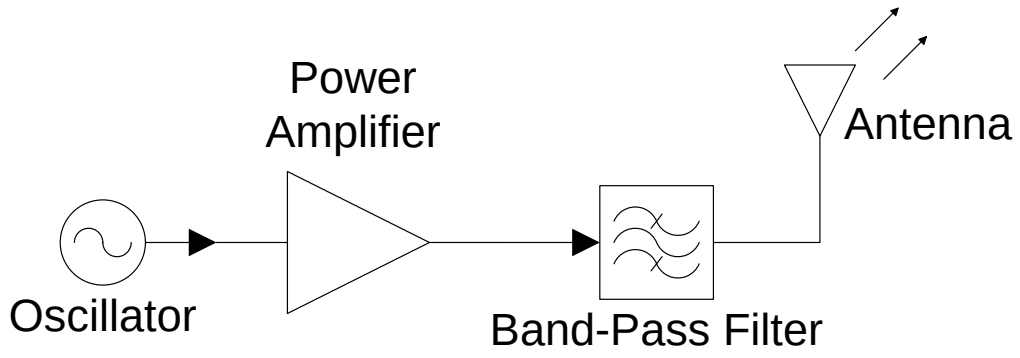


Figure 4-3: Generic RF Transmitter Architecture

4.3 Near-Field Power Transmitter

4.3.1 Conventional RF Transmitters

Figure 4-3 shows a generic RF transmitter architecture, without the data modulation blocks. The oscillator may consist of a PLL, which up-converts a stable crystal output frequency to RF. Using a PLL for generating RF is costly in terms of power because of the high-speed frequency dividers, precision phase detectors and charge pumps used. However, PLLs do offer a very good combination of low phase noise, tunability and stability. Approaches to generating RF outputs without using PLLs usually fall under one of the following categories

- **Ring Oscillators**: Low power, good tunability, poor phase noise and stability, imprecise center frequency
- **LC Oscillators**: Moderate power, moderate tunability, good phase noise but poor stability, moderately precise center frequency
- **Resonator-based Oscillators**: Low power, limited tunability, excellent phase noise and stability, extremely precise center frequency

The power amplifier is usually implemented as a push-pull (switching) amplifier (Class-D or higher) to achieve better power efficiency compared to linear amplifiers [31]. This makes the output band-pass filter essential, in order to eliminate harmonics generated by the switching action. A separate resonator is used in the oscillator to set

the center frequency since most resonators have very high quality factors and cannot operate at high power.

4.3.2 Chosen Transmitter Architecture

In a design with a constrained power budget that prevents the use of a PLL-based oscillator, the remaining alternatives are the ones described in subsection 4.3.1. Although ring oscillators are extremely low-power, they would need additional complex circuitry to continuously track and correct their output frequency to the desired 27MHz ISM band. A crystal oscillating at the transmission frequency would have to be off-chip. The only option remaining is to use an LC oscillator. However, an fully on-chip LC oscillator would need an inductor of the order of $1\mu H$ in order to keep the capacitor in the range of a few tens of pF, which is not achieveable in current CMOS technologies within resonable area. An off-chip LC network would only add to the power and cost of the system. A simple way to deal with this problem is to use a combined oscillator-PA topology that uses the same LC network for both tuning the oscillator and filtering the output of the PA, as shown in Figure 4-4.

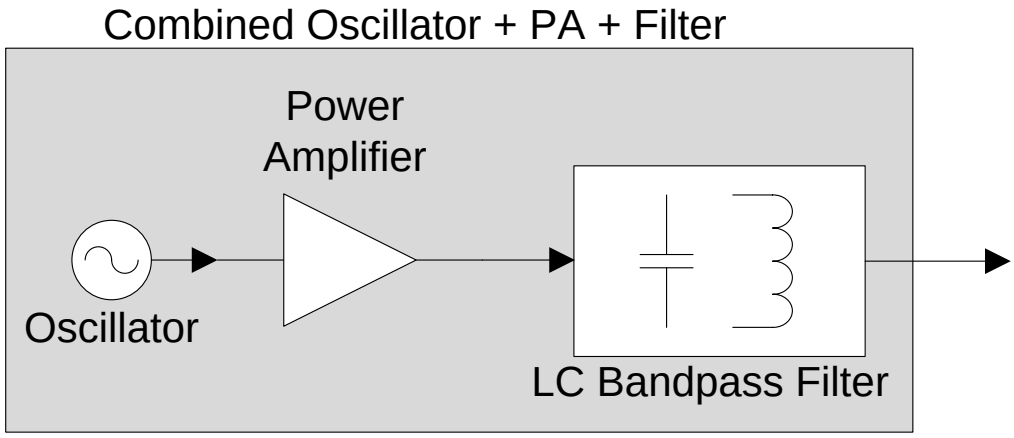


Figure 4-4: Oscillator Architecture Used for Power Transfer. The band-pass filter contains inductors on fabric and serves both to filter the PA output and to set the center frequency of the oscillator.

In an e-textiles based inductive power transfer scheme, the inductor in the output band-pass filter should preferably be on fabric so that it can serve the purpose of

being a part of the filter as well as the near-field emitter, as well as being a part of tuning network for the oscillator. As noted in Section 3.4, screen-printed fabric passives (both inductors and capacitors) suffer from extremely poor tolerances and poor quality factors. This prevents the use of a fully on-fabric band-pass LC filter at the output. Since the inductor is necessary for transmitting power to the sensor nodes, the capacitor can be moved on-chip. This permits tuning out the inductance variations to maintain the same output frequency. Additionally, the quality factor of the tuning network is now dominated by the inductor, since CMOS on-chip capacitors have a much higher quality factor [32]. A detailed analysis of self-tuned resonant power- and data-transfer using coupled inductors and Class-E power amplifiers is provided in [33].

4.3.3 Modified Colpitt's Oscillator

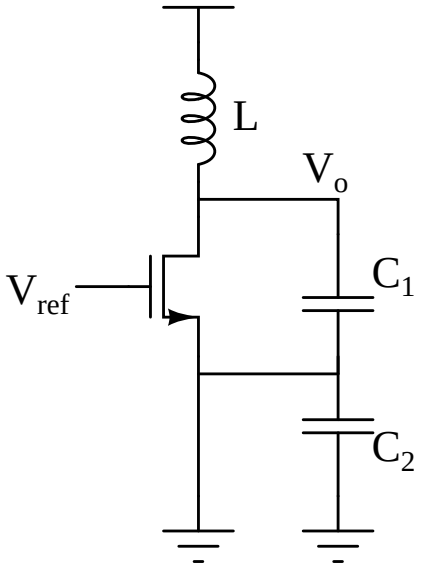


Figure 4-5: Commonly used Colpitt's Oscillator Circuit in Common-Gate Configuration

A Colpitt's oscillator is a suitable choice for the design since it requires one inductor and two capcitors. The inductor can be on fabric while the two capacitors can be on-chip, with the entire LC network simultaneously doing the job of the output filter and oscillator tuning network, as explained in subsection 4.3.2. Figure 4-5 shows a

commonly used Colpitt's oscillator implementation [34]. While this oscillator topology is well-known for its robustness and reliability, there are a few reasons why it could cause issues in the system if used as is.

- The capacitors C_1 and C_2 are of the order of picofarads. In order to maintain capacitor linearity and hence frequency stability, Metal-Insulator-Metal capacitors (MIMcaps) need to be used. The top- and bottom-plate parasitic capacitances of the MIMcaps are not negligible for such large capacitors. Since the node between C_1 and C_2 is not AC ground, the parasitic capacitance from this node will affect the oscillator performance.

- One of the terminals of the inductor is AC ground, while the other oscillates about a DC operating point. If the two terminals can be made to oscillate in opposite phase, the voltage generated at the secondary would double and so would the efficacy of the rectification circuit.

- Since the oscillator is linear, it is not possible to generate high output power at high efficiency.

The oscillator topology shown in Figure 4-6 addresses all the issues associated with the Colpitt's oscillator. It also has the same expression for the output frequency as the Colpitt's oscillator. Both the capacitors have one terminal connected to AC ground, and hence can absorb parasitics at the top plate. None of the inductor terminals are connected to AC ground, which offers the possibility of driving them differentially. The voltage V_{ref} is a mid-band reference that can be derived from the power rails. The linear differential amplifier is followed by a class-D push-pull amplifier within the oscillator loop itself. The PA achieves efficient power amplification without the need for a separate output filter. The capacitors C_1 and C_2 have 3 bits of tuning for eliminating output frequency variations arising from the inductor. The PA has 2 bits of tuning for changing the output power level. In the lowest-power setting, the output oscillation amplitude is limited by the switch resistance of the PA, which is reduced as additional parallel PA's are turned on. Under maximum-power, the PA operates

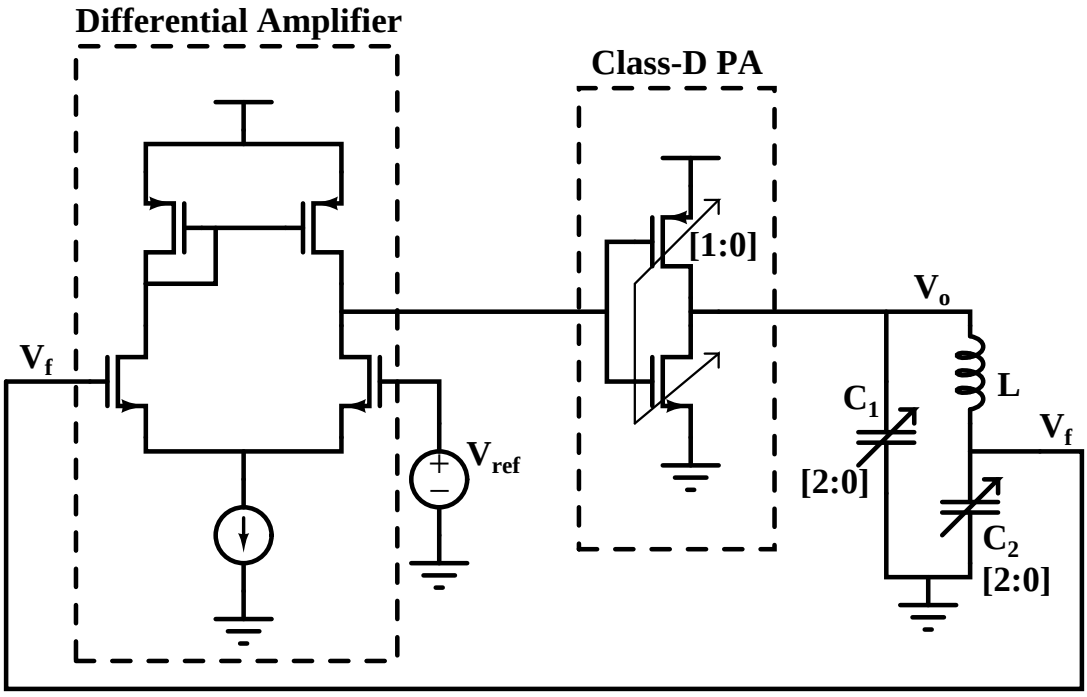


Figure 4-6: Oscillator Topology Used

as a true Class-D amplifier with rail-to-rail swing at the output. Gate bias to the additional PA's is set such that both the switches are off when the PA is not being used. This avoids the use of large transistors in series. The capacitor C_1 absorbs the parasitic output capacitance of all PA's connected in parallel. The entire circuit is built using thick-gate oxide transistors, and can be operated at a higher supply voltage in order to increase the voltage across the rectifier circuit at the input of the sensor nodes.

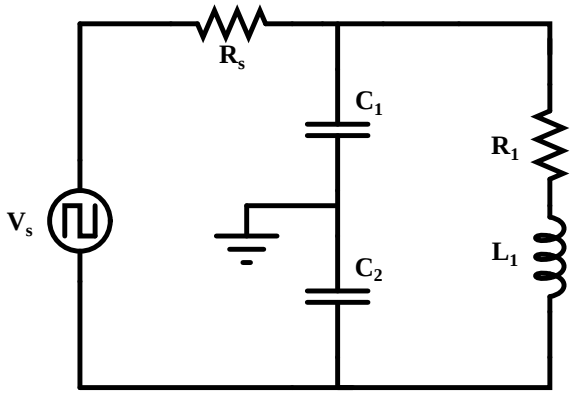


Figure 4-7: Thevenin Equivalent Model of Oscillator

A simplified Thevenin representation of the circuit in Figure 4-6 under oscillation is shown in Figure 4-7. The class-D power amplifier under oscillation is represented by square wave voltage source at the oscillation frequency. The resistor R_s represents the resistance of the switching transistors in the PA. Resistor R_1 includes real part of both the inductor and the reflected secondary impedance. This representation closely matches the primary side of Figure 4-1.

Oscillator Loop Gain Analysis

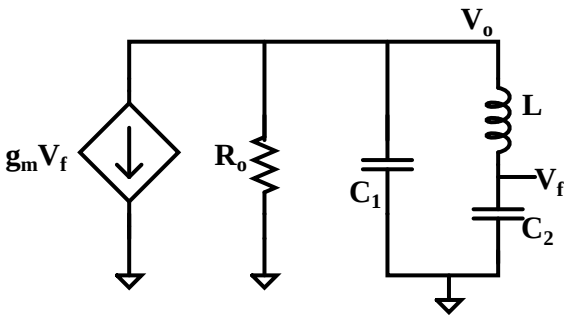


Figure 4-8: Small-Signal Model of Oscillator

Figure 4-8 shows the small-signal model of the oscillator. The poles of the differential amplifier and the push-pull amplifier are assumed to be at a frequency much higher than the circuit's operating frequency and are therefore neglected. The transconductance parameter g_m is the combined effect of the voltage amplification of the differential amplifier and the transconductance of the push-pull amplifier. The output resistance R_0 is the combination of the output resistance of the push-pull amplifier and the resistance of the inductor, parallelized at the resonant frequency using the dual of Equation B.8.

Figure 4-9 shows the block diagram of the feedback path. Here, C_{eq} equals the series combination of C_1 and C_2.

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \tag{4.3}$$

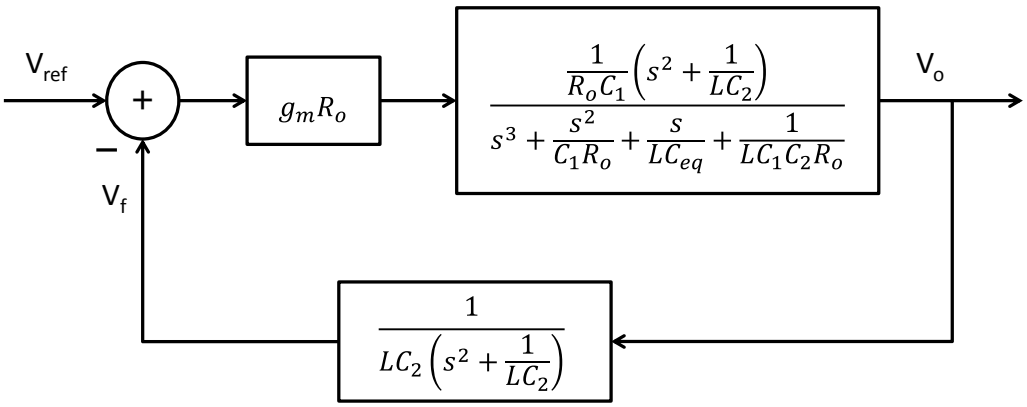


Figure 4-9: Small-Signal Feedback Diagram of Oscillator

The loop gain of the oscillator is

$$L(s) = -\frac{g_m R_o}{LC_1C_2R_o s^3 + LC_2 s^2 + R_o\left(C_1 + C_2\right)s + 1} \tag{4.4}$$

. It is clear that the value of the loop gain is real at DC and at $s^2 = (LC_{eq})^{-1}$. At $s = \pm j/\sqrt{LC_{eq}}$, the voltage across the inductor is

$$\begin{aligned} V_L(s) &= V_o(s) - V_f(s) && (4.5)\\ &= V_o(s)\left(\frac{s^2LC_2}{s^2LC_2 + 1}\right) && (4.6)\\ &= V_o(s)\left(\frac{-C_2}{-C_2 + C_{eq}}\right). && (4.7) \end{aligned}$$

If $C_{eq} = 0.5C_2$, then $V_L(j\omega_0) = 2V_o(j\omega_0)$ and the inductor can be driven differentially. Fixing C_2 also fixes C_1 as

$$C_1 = C_2 = 2C_{eq}. \tag{4.8}$$

Under this condition, it can be checked that at DC, the loop gain has a phase of 180° while at $\omega = \left(\sqrt{LC_{eq}}\right)$, the loop gain has a phase of 360°. Hence, the circuit oscillates at this frequency provided it has sufficient gain. This choice of the capacitor values has another advantage. Given a desired frequency of operation and inductance value, choosing $C_1 = C_2$ is the most area-optimal solution for getting the required C_{eq}. Also, under this condition, the connection to ground at the node between capacitors C_1 and

C_2 in Figure 4-7 can be removed since $C_1 = C_2$ and $V_0 = -V_f$. With the ground connection removed, Figure 4-7 exactly matches the primary side in Figure 4-1 with tank capacitance $C_1||C_2$.

Root-Locus Analysis

The loop gain for the oscillator in Equation 4.4 has 3 poles. For the component values $L = 1.4\mu H$, $C_1 = C_2 = 48pF$ and $R_o = 1.3k\Omega$ such that $\omega_0 = \left(2\pi\sqrt{LC_{eq}}\right)^{-1} \approx$ 27MHz, the poles are located at $p_1 = -8$Mrad/s, $p_2, p_3 = -4 \pm j172$Mrad/s. Figure 4-10 shows that once the closed-loop poles enter the right-half plane they never return back to the left-half plane. This implies that there is only a lower bound on the DC loop gain for oscillations to take place. Simulations show that the loop oscillates across PVT corners and fabric variations. This is expected since the feedback action is expected to bias the inverter formed by the class-D PA around the switching threshold, which has a high small-signal gain.

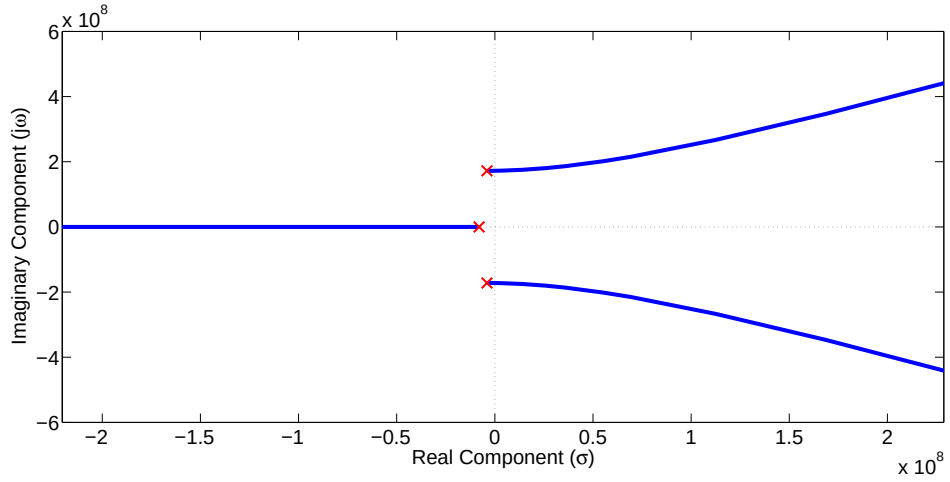
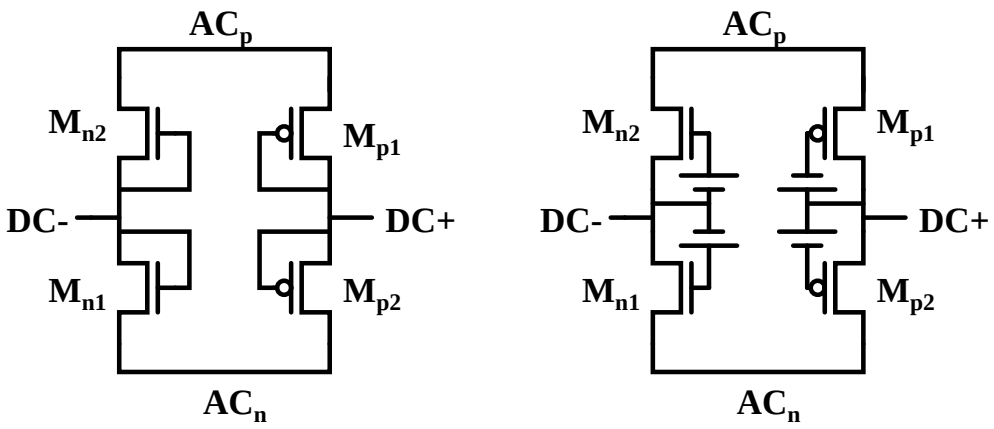


Figure 4-10: Feedback Root Locus Plot of Oscillator Circuit

4.4 AC-DC Conversion at Sensor Node

At the sensor nodes of the network, the wireless AC power radiated by the base station is gathered and rectified to supply DC power. This section deals with the design of the power converter that does this job.

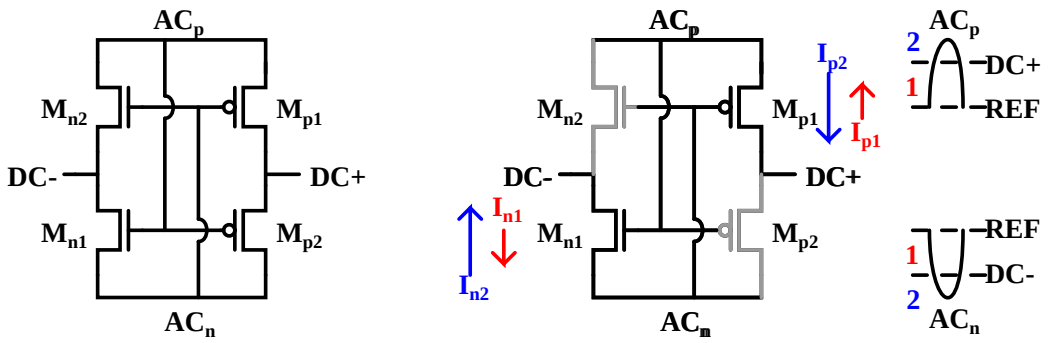


(a) With Diode-Connected Transistors (b) With Threshold Adjustment

Figure 4-11: Two Traditional Full-Bridge CMOS Rectifier Topologies

Although rectifiers can be built to work with very high efficiency using devices with low forward voltage and large reverse blocking capability such as Schottky diodes, such a rectifier would not be integrable in regular CMOS technologies. Figure 4-11 shows some traditional CMOS full-bridge rectifier topologies. Connecting the transistors in diode-connected configuration is the simplest way to replace the diodes in a full-bridge rectifier with MOS transistors. However, directly connecting the gate to the drain of these devices severely affects the output DC power obtainable since the DC voltage must settle to at least V_T below the peak AC value, and even lower when it has to supply a larger current. To address this issue, [35] uses voltage sources to boost the gate overdrive beyond the peak AC value by one V_T and hence bring the DC output close to it. However, such a solution does not permit a fully-integrated design. [36] achieves the same result using charge stored on ferroelectric capacitors. While this solution is fully integrable on silicon, processes with ferroelectric capacitors are still uncommon and costly. The Adaptive Threshold Rectifier in [18] uses an initialization stage that samples the threshold voltage across a MOS capacitor. This approach works very well for older CMOS technologies, but is unsuitable for newer technologies that have high gate-leakage.

The sensor node energy harvester uses self-synchronous full-bridge rectifier blocks [37, 38, 39]. The implementation of this rectifier block is shown in Figure 4-12(a).



(a) Rectifier Schematic (b) Functioning Mechanism

Figure 4-12: Self-Synchronous Rectifier and Functioning Mechanism

All transistors are connected such that their gate terminals are driven by AC phase opposite to the one driving the source. The functioning mechanism under steady state in one of the AC phases is shown in Figure 4-12(b). In this figure, the voltage REF is a common reference terminal for all nodes in the rectifier. In the phase shown, the gate of M_{p1} is pulled to a lower voltage, while the voltage of the source increases. The transistor M_{n1} has its gate pulled to a higher voltage and drain pulled to a lower voltage.

Figure 4-13 shows simulated current waveforms for I_{Mp1} and I_{Mn1}. When the positive AC input voltage is below the DC+ node voltage, current flows out of the DC+ node. However, this current is not large since the gate drive is small. Current flows into the DC output terminal once the positive AC input value crosses the DC+ node voltage. Since this period also corresponds to maximal gate drive, the amount of total charge going into the DC+ terminal is more than the amount of charge coming out of it. The same thing happens in opposite at the DC- terminal. The actual magnitude of the DC outputs depends on the amount of DC output current demanded by the load, such that the net charge flowing into the DC+ and out of DC- in one half-cycle corresponds to the net charge flowing into the load during the same period.

The transistors M_{p2} and M_{n2} also conduct during the phase shown in Figure 4-12(b), although ideally they are supposed to be off. However, since the gate drive of both transistors is lesser than M_{p1} and M_{n1} respectively during this phase, the

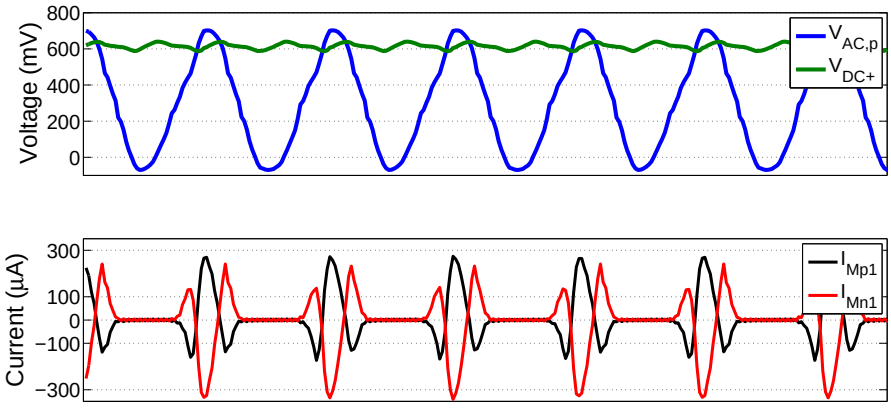


Figure 4-13: Simulated Rectifier Current Waveforms

amount of current that these transistors conduct is much smaller, and has little effect on the DC output voltage. The current conduction mechanism works the same way in the opposite phase, with the roles of the transistors reversed.

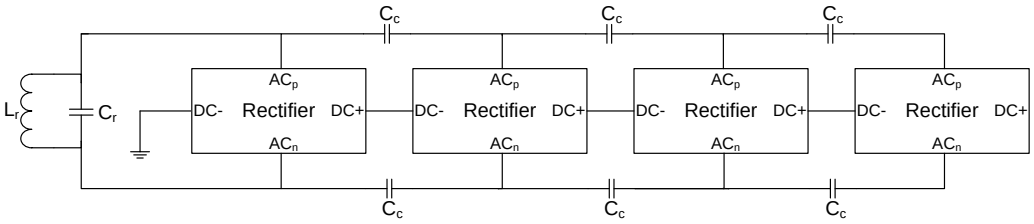


Figure 4-14: Rectifiers Connected in Series to Boost DC Output

From the approximate input voltage amplitude to the AC-DC converter calculated in Section 4.2, it is evident that a single rectifier cannot produce sufficient V_{DD} to power circuits in the sensor node. In order to produce the necessary V_{DD}, four rectifiers have been connected in series [40] as shown in Figure 4-14. The AC coupling capacitors C_c provide the DC offset between adjacent rectifiers. Also, the fabric inductor receiving wireless power from the base station L_r forms a resonant tank with an on-chip capacitor C_r, which serves to increase the voltage across the power converter. The capacitor C_r can be made to absorb some of the input parasitic capacitors of the individual rectifiers, and thus can reduce switching losses across these capacitors by recycling the energy stored under resonance.

The DC output voltage of the series combination of rectifiers is not the voltage produced by each rectifier if working alone times the number of rectifiers, as one might expect. In fact, the total voltage obtained is less than this value due to a variety of reasons

1. The total DC output resistance increases with more rectifiers, which reduces the total output DC voltage.

2. The AC path impedance increases as one goes down the series rectifier chain due to the reactances of the coupling capacitors adding up. The value of C_c cannot be increased indefinitely owing to chip area constraints.

3. As more and more rectifiers are connected in series, the nMOS devices in the rectifiers further down the chain have higher threshold voltages due to body-biasing and hence are less effective. This problem arises only in CMOS processes without triple-well capability.

Simulations of the rectifier under different coupling constants show that connecting up to four rectifiers produces enough DC output voltage to power the sensor node circuitry in most cases. In fact, adding a fifth rectifier provides only marginal benefit and may, under very weak coupling, contribute negative DC voltage to the total output.

Chapter 5

PHY Design and Communication Circuitry

The previous chapter discussed the theory and implementation of inductive power transfer. This chapter focuses on the physical layer (PHY) of the data network. A review of inductive data links in literature is presented. The choices for modulation schemes for downlink (base station to sensor nodes) and uplink (sensor nodes to base station) are explained. A theoretical analysis of the links is performed and the implemented circuits are presented.

5.1 Existing Inductive Data Links

Various approaches have been reported for communicating to and from biomedical sensors, both implanted and on the body. A summary of some existing inductive data links is presented in Table 5.1.

In a BAN built on fabric, inductors are costly in terms of area and state-of-the-art biomedical implants and sensor patches [45] are too small to allow efficient coupling with multiple inductors. Further, the power budget on such sensor nodes demands extremely low transmit and receive powers, which does not permit the use of FSK or PSK modulators/demodulators. [46] describes a novel feedback scheme for powering sensors inductively and using information from the sensors to increase

	Ghovanloo, TCAS '04 [41]	**Ghovanloo, TCAS '06 [42]**	**Simard, TBCAS '10 [43]**	**Mandal, TBCAS '08 [44]**
Modulation Scheme	FSK	FSK (Downlink) PWM ASK (Uplink)	Offset QPSK	PWM ASK (Downlink) Imp. Modn. ASK (Uplink)
Power Transfer Capability	No	Yes	Yes	No
Data Transfer	Uplink only	Bidirectional	Bidirectional	Bidirectional
No. of Inductor Pairs	Single	Multiple	Multiple	Single

Table 5.1: Summary of Previously Published Inductive Links

transfer efficiency. Data transfer is done by a switch across the secondary which modulates the load impedance, and can be perceived at the primary. Since driving the switch requires much less power than actively generating a carrier and modulating it for transmission, this method (known as impedance modulation) is an ideal candidate for extension to data transfer from sensors.

5.2 Downlink Communication

Downlink communication refers to communication from the base station to the sensor nodes. This section provides an overview of the modulation schemes chosen and describes the circuits used in the link.

5.2.1 Modulation Scheme Used

Although most of the network data traffic is from the sensor nodes to the base station, the network needs to handle traffic in the other direction as well. Messages transmitted from the base station to the sensor node could include sensor configuration instructions and network-related commands, such as going to/waking up from sleep or initiation of uplink data transfer. However, even though receiving data is usually more complex than transmitting, the receiver circuitry on the sensor nodes must not

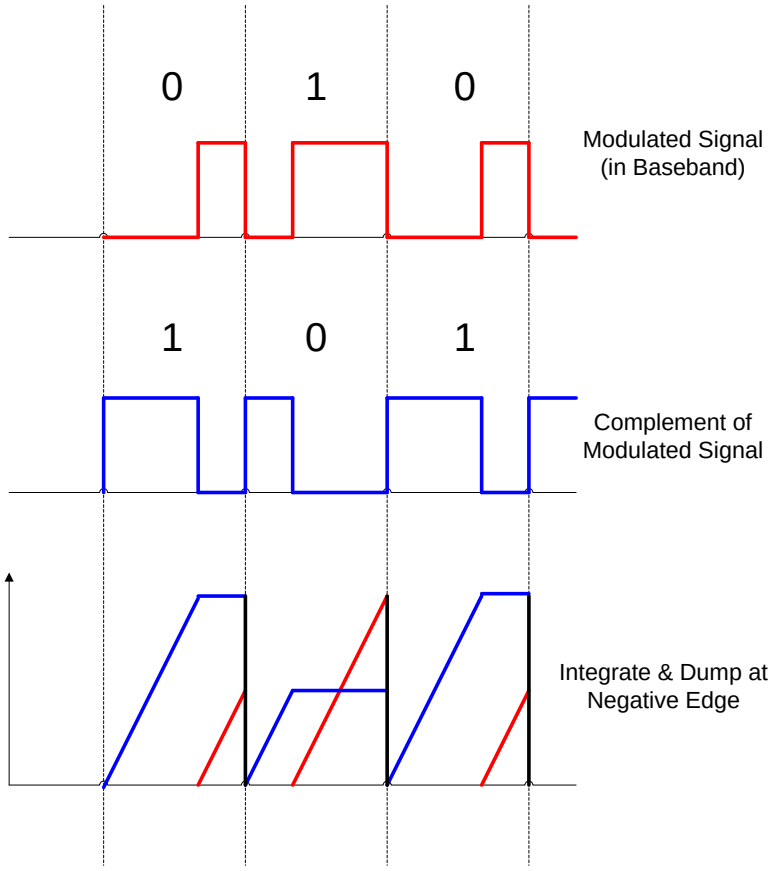


Figure 5-1: PWM Modulated Signal and Demodulation Scheme

have significant power overhead. This needs to be taken care of by using appropriate modulation schemes and messaging protocols.

In order to keep the receiver circuitry at the sensor simple, a modulation scheme that does not need clock recovery is required. This can be achieved by using a Return-to-Zero (RZ) signaling scheme. A common RZ signaling scheme used is Pulse-Width Modulation (PWM). In PWM, bits are encoded into the width of a train of pulses. Usually one of the edges of all pulses in the pulse train is synchronized to a clock. The location of the other edge is varied according to the bit encoded in the particular pulse. Figure 5-1 shows how data is encoded as a PWM signal and how it can be demodulated. Since the negative edges of the pulses in Figure 5-1 are synchronized, a longer pulse (which signals a '1') implies that the preceding duration where there was no pulse is shorter. Sensing and comparing the durations when the pulse was absent and when it was present allows demodulation without any clock recovery.

Figure 5-1 depicts a $25-75\%$ width modulation for representing logic 0 and logic 1. This ensures optimum performance with the detection mechanism used. Since the required data rate for the downlink is very small, the cycle time for pulses in the downlink transmission has been chosen to be $1/12^{th}$ of the uplink transmission bitrate. This permits the use of digital integrate and dump schemes with the on-board sensor node clock intended for uplink transmission. Choosing a digital scheme reduces the area by avoiding the use of large integrating capacitors.

In order to transmit the PWM signal over an inductive link to a sensor node, it needs to be modulated on an RF carrier. The 27MHz signal used for power transfer can be modulated with the PWM waveform using On-Off Keying (OOK). OOK, being incoherent, allows the sensor to recover the original PWM signal for demodulation by simple envelope detection. Since the downlink is only meant for carrying sensor and network confiuration instructions, data traffic is extremely sporadic and consists of small packets. This low duty cycle ensures that the amount of power that can be transferred remains unaffected.

5.2.2 Transmitter

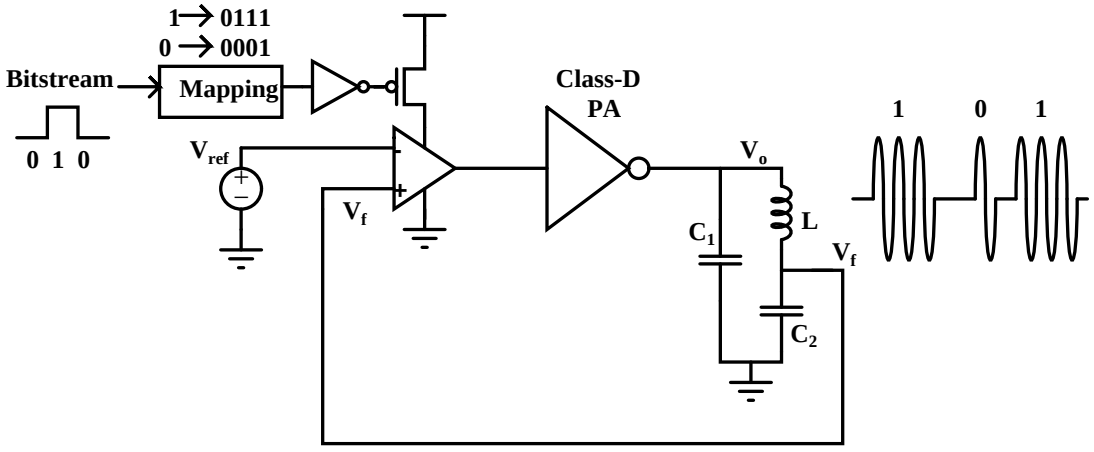


Figure 5-2: Scheme for Generating PWM Signals with OOK[1]

Figure 5-2 shows the power transmitter on the base station integrated with the

[1]The OOK output in Figure 5-2 is highly exaggerated. Each PWM pulse is long enough and contains enough sinusoidal pulses for the low-pass filter of the envelope detector to be effective.

pulse-width modulator. The modulator takes as input the the binary-coded downlink packet and converts it to a baseband pulse-width modulated signal using a one-to-one digital mapping of the input bits. The modulated signal goes to a power switch that turns on/off the supply to the differential amplifier in the oscillator loop. Oscillations are produced whenever a modulated output is HIGH. When the modulated output is LOW, the differential amplifier does not get power and the feedback loop is broken, causing the oscillations to die down. This technique of controlling the oscillations is efficient since large power transistors to control the PA are avoided, the supply to the linear amplifier is cut off, and the class-D PA being just a CMOS inverter has negligibly small static power. Since the PWM output is at a frequency much lower than the oscillator output, the time taken for the oscillator to start-up or die down is negligible compared to the actual pulse widths. Hence, OOK modulation is achieved with minimal additional circuitry. The digital mapper and the logic generating the downlink packets is designed such that the PWM output remains HIGH when there is no downlink message to be transmitted, and thus allows power transfer to take place unhindered.

5.2.3 Receiver

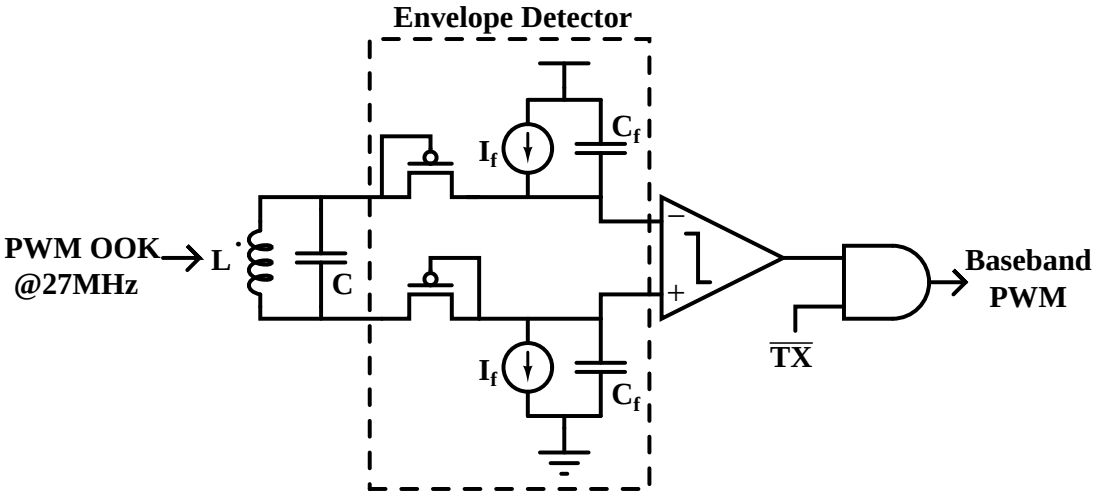


Figure 5-3: Envelope Detector Circuit for Recovering PWM Signal

Receiving messages transmitted from the base station to the sensor node is done in

two steps. The first step, shown in Figure 5-3 extracts the PWM waveform from the On-Off Keyed (OOK) waveform using a common envelope detector topology. Again, since the envelope is modulated at a frequency much lower than those associated with the oscillator steady-state or start-up transients, the time taken by the oscillator to start up and shut down does not affect the demodulation. The top branch of the envelope detector shown in Figure 5-3 extracts the negative (below DC) envelope while the bottom branch extracts the positive (above DC) envelope. The envelope detector topology used avoids the need for large resistors. The time constant of the low pass filtering is given by Equation 5.1.

$$\tau_f = \frac{C_f}{g_{m,diode}} \tag{5.1}$$

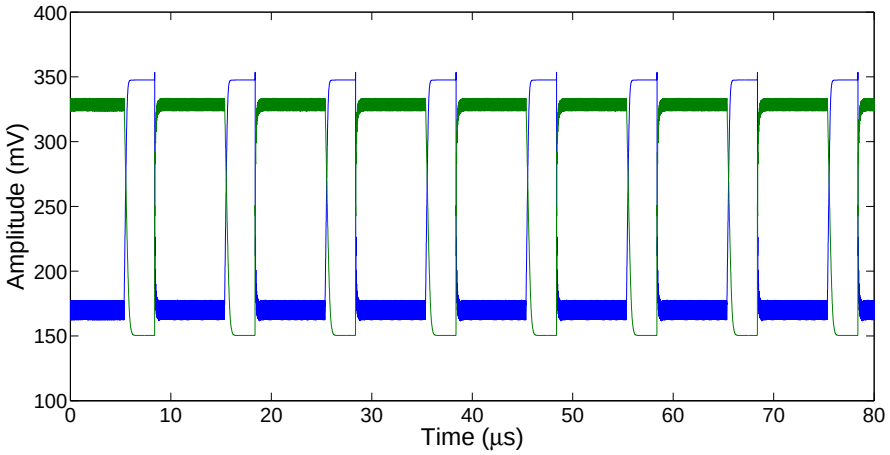


Figure 5-4: Simulated Outputs of Envelope Detector at Sensor Node Receiver

$g_{m,diode}$ is the transconductance of the diode-connected transistor, which can be calculated from the current I_f using the subthreshold transconductance formula. For I_f = 100nA and C_f = 500fF, the filter cutoff frequency is 1.2MHz, which is small enough to reject the carrier at 27.12MHz but large enough not to attenuate the PWM signal. The forward voltage drop of the diode-connected transistors allows the outputs of the two branches to be fed into a standard comparator designed without any deliberate offset, as shown in Figure 5-4. The output of the comparator is gated

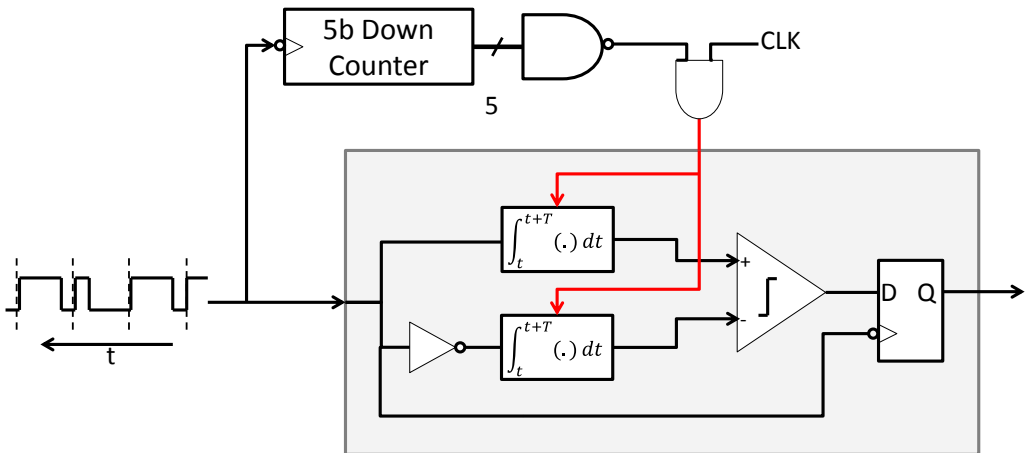


Figure 5-5: Digitally-Implemented Demodulator for PWM Signals

in order to prevent unintentional demodulation of messages transmitted by the sensor node, which also appear as ASK signals across the inductor at the sensor node. This will be discussed further in Section 5.3.

Figure 5-5 shows the digital demodulator used at the sensor node. The output of the envelope detector and its complement are passed through digital "integrate-and-dump" circuits, represented as definite integral blocks in the figure. Integration is done digitally from one negative edge of the input waveform to the next as shown in Figure 5-1, by using the sensor node clock to count the number of cycles for which the input of the block is HIGH. The outputs are fed to a digital comparator whose output is latched at the subsequent negative edge. A counter keeps count of the number of bits left to be demodulated and gates the clock going into the demodulator once the downlink packet has been received. The bit-width of the counter shown in Figure 5-5 corresponds to the downlink packet size, which is described in Section 6.4.

5.3 Uplink Communication

Uplink communication refers to communication from the sensor nodes to the base station. This section presents a theoretical analysis of the modulation scheme chosen and describes the circuits used in the link.

5.3.1 Modulation Scheme Used

Data transfer from sensor nodes to the base station constitutes a major portion of the network traffic. Uplink messaging needs to be relatively fast, but should involve minimal transmission effort by the sensor nodes. Impedance modulation is well-suited for these requirements. It involves turning on and off a switch connected across the sencondary inductor in Figure 5-6, which only adds the switch to the existing power transmission system shown in Figure 4-1. A theoretical background for impedance modulation can be developed by extending the analysis for inductive power outlined in Section 4.1.

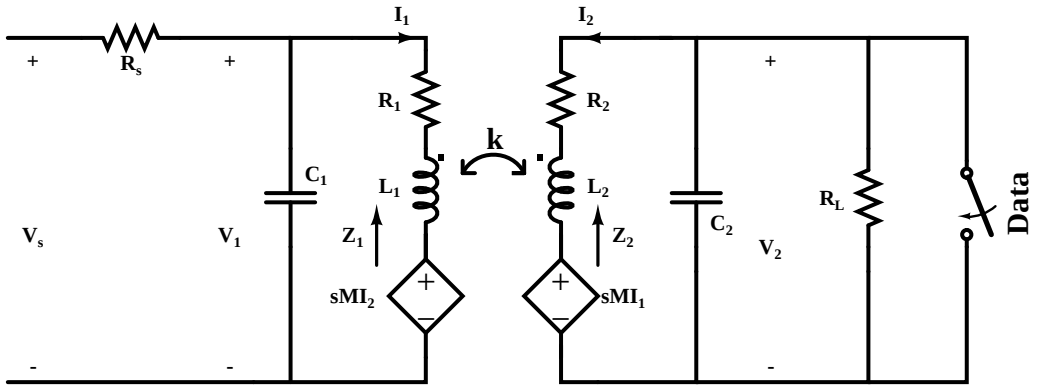


Figure 5-6: Schematic for Uplink Data Transmission using Impedance Modulation

When the secondary is a short-circuit, the secondary impedance in Figure 5-6 is $Z_2(s) = sL_2$. Using Equation B.7, the reflected impedance at the primary is

$$Z_{rfl,sc}(j\omega_0) = \frac{-\omega_0^2 M^2}{Z_2(s)} \tag{5.2}$$

$$= ksL_1 \tag{5.3}$$

which uses the relation $M = k\sqrt{L_1 L_2}$ and assumes $L_1 = L_2$. Under this condition, the impedance of the inductive branch of the tank is

$$Z_1(s) = \omega_0 L_1 \left(1 - k^2\right) + R_1. \tag{5.4}$$

When the switch at the secondary in Figure 5-6 is opened, the only load across the

tank is the rectifier, which presents an AC resistance R_L. Under this condition, from Equation B.14

$$Z_1(j\omega_0) = \omega_0 L_1 + R_1\left(1 + k^2 Q_1 Q_2'\right) \tag{5.5}$$

where Q_2' is the loaded quality factor of the secondary and is given by Equation B.13. Since Q_2' is dominated by the quality factor of the inductor in the tank at the secondary ($Q_2' = Q_2$), the amount of impedance modulation observed is independent of whether the recitifer is kept connected when the switch is open (which presents R_L across the tank) or is disconnected. Converting the resistor in series with the primary inductor in both cases to a parallel resistance gives

$$\left|\frac{V_1(j\omega_0)}{V_s(j\omega_0)}\right|_{sc} = \frac{Q_1^2 R_1}{R_s + Q_1^2 R_1} \tag{5.6}$$

$$\left|\frac{V_1(j\omega_0)}{V_s(j\omega_0)}\right|_{oc} = \frac{Q_1'^2 R_1\left(1 + k^2 Q_1 Q_2\right)}{R_s + Q_1'^2 R_1\left(1 + k^2 Q_1 Q_2\right)}. \tag{5.7}$$

Q_1' is the loaded quality factor of the primary. The modulation index m is defined as the relative change in the amplitude of the AC signal upon switching from one binary data value to the other. The expression

$$\left|\frac{V_1(j\omega_0)}{V_s(j\omega_0)}\right|_{oc} = \left|\frac{V_1(j\omega_0)}{V_s(j\omega_0)}\right|_{sc}(1 - m) \tag{5.8}$$

gives

$$m = 1 - \frac{Q_1'^2 R_1\left(1 + k^2 Q_1 Q_2\right)}{R_s + Q_1'^2 R_1\left(1 + k^2 Q_1 Q_2\right)} \cdot \frac{R_s + Q_1^2 R_1}{Q_1^2 R_1}. \tag{5.9}$$

Using the same link parameters used in Section 4.2, i.e. $Q_1 = Q_2 = 8$, $R_s = 1.3k\Omega$ and $R_1 = 30\Omega$, the variation of the modulation index m with change in the inductive coupling coefficient is plotted in Figure 5-7.

Figure 5-7 shows that as expected, the modulation index increases as the coupling coefficient is increased. At a reasonable value of $k = 0.1$, the modulation index is $m = 0.21$. The bitrate used for uplink can range from 300kbps to 1Mbps. Even though no pulse shaping is performed on the uplink data before transmission due to power constraints, the main lobe of the uplink data spectrum lies fully within the

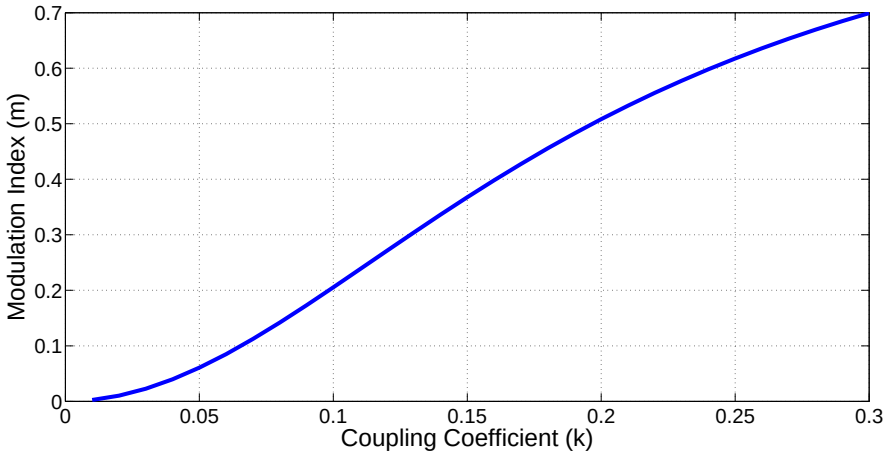


Figure 5-7: Variation of Impedance Modulation Index at Receiver Input vs. Inductive Coupling Coefficient

326kHz bandwidth of the 27.12MHz ISM band at the lowest data rate. Although the uplink data spectrum is not accommodated in the 27.12MHz band at higher data rates, transmission can still be safely carried out since near-field coupling, which dies down as $1/d^4$ in power [47], is used. Moreover, since the modulation index is small, the energy outside the center frequency is 14dB below the carrier.

The transmitter for the impedance modulation link can be implemented by using just a switch that is driven by a digital signal representing the serialized data. The receiver circuitry on the base station is a lot more complex. Figure 5-8 shows the signal waveforms as they are observed across the secondary and primary tanks when the transmitting switch is modulated. The receiver needs a sensitive demodulation circuit to resolve the small differences in AC amplitude that signal a binary 1 or 0. Further, since the signaling scheme is Non-Return-to-Zero (NRZ) in order to use bandwidth efficiently, a Clock-Data Recovery (CDR) block that uses a Phase-Locked Loop (PLL) is required. The network is divided into two sub-networks, as described in Section 2.3, which are driven by separate oscillators. Under conditions where it is not known a priori at the base station which sensor node will be transmitting next, the impedance modulation data modulated on these two separate carriers needs to be multiplexed. The output of the multiplexer is then analyzed by the digital circuitry for processing and storage.

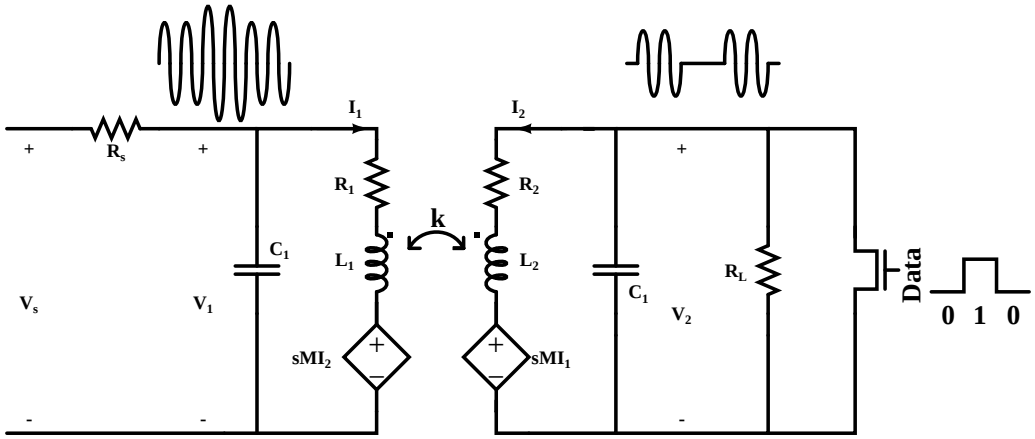


Figure 5-8: Signal Waveforms for Impedance Modulation Data Transfer

5.3.2 Transmitter

The impedance modulation transmitter is an NMOS switch that is modulated by the serialized data output of the digital circuitry that interfaces with the AFE and ADC. The switching transistor in Figure 5-8 is chosen such that the gate drive is sufficiently higher than the V_T of the device and the width of the device is large enough for it to effectively short circuit the inputs of the rectifier.

5.3.3 Receiver

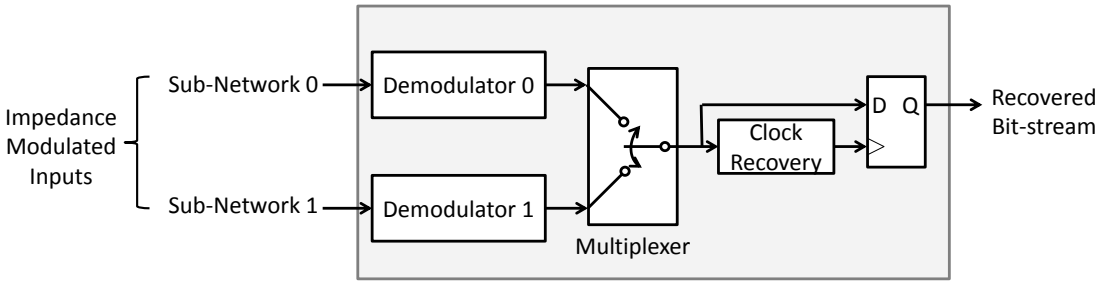


Figure 5-9: Block Diagram of Impedance Modulation Receiver

Figure 5-9 shows a block diagram of the receiver at the base station. Data coming in from the two sub-networks is processed by two separate demodulators, which give binary bitstream outputs. The demodulator outputs go to a multiplexer which chooses the bitstream that is toggling, indicating incoming data from that

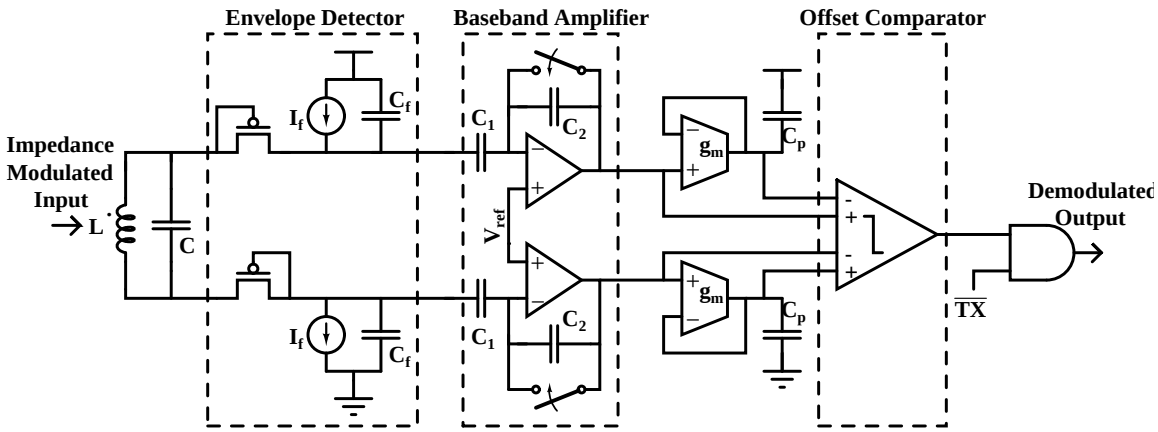


Figure 5-10: Demodulator at Impedance Modulation Receiver

sub-network. The output of the multiplexer goes to a CDR circuit that recovers the transmit clock and latches the input data with respect to it. Each of these blocks is described in detail in the subsequent sections.

Demodulator

Figure 5-10 shows a schematic of the demodulator that forms the first block of the receiver in Figure 5-9. The input to the demodulator is an ASK signal with a modulation index $m \approx 0.2$ as shown in Figure 5-7. The first step in demodulation is envelope detection, shown in Figure 5-10. The upper branch of the envelope detector recovers the negative (below DC) envelope of the signal while the lower branch recovers the positive envelope. The filter parameters used are $I_f = 500\text{nA}$ and $C_f = 3\text{pF}$. From Equation 5.1, this gives a low-pass cutoff frequency of $f_c \approx 4.4\text{MHz}$, which is sufficiently low to reject the carrier at 27.12MHz but high enough to let the bitstream at 300kbps-1Mbps pass. The envelope detector circuitry is operated at the higher supply voltage running the oscillator and power amplifier.

Unlike the downlink receiver, the uplink receiver has to demodulate a weaker ASK-modulated signal. Hence, additional amplification stages are required before making a decision. The outputs of the envelope detector are amplified using single-stage op-amps with capacitive feedback. The use of capacitors instead of resistors in the feedback eliminates loading constraints on the DC bias current of the amplifier,

and provides a decoupling capacitance that allows the rest of the demodulator to be operated at the nominal supply voltage, which reduces power. The charge on capacitive feedback network is initialized using pass-gate switches that are turned on at system reset and at intermediate points, both during and after packet reception. The controls for the switches come from the digital circuitry that recovers information from the bitstream, and will be covered in detail in Section 6.4. A mid-rail reference voltage is generated for initialization using two sets of back-to-back PMOS diode-connected transistos connected from V_{DD} to ground. Variations in the diodes do not affect the circuit since any drift from the mid-rail value is reflected in both the amplifiers. The outputs of the baseband amplifiers go to a low-pass $g_m - C$ filter.

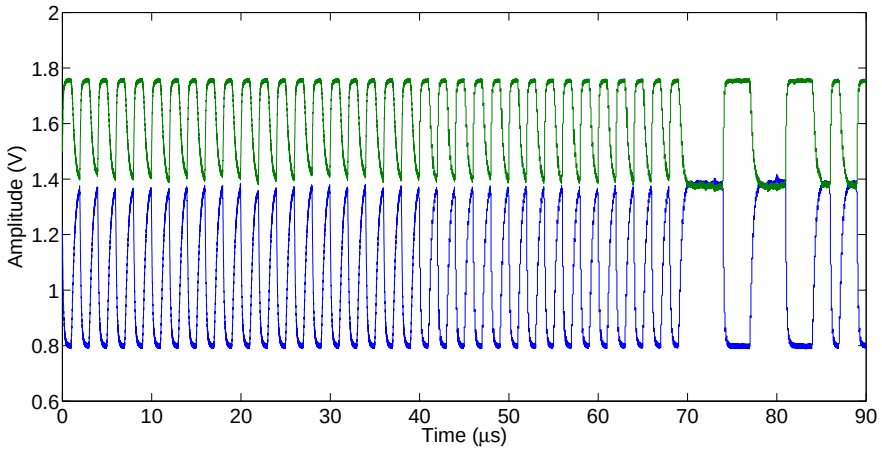


Figure 5-11: Simulated Waveforms at Output of Uplink Demodulator Baseband Amplifier

The necessity of this filter is justified by the simulated waveforms of the amplification stage output shown in Figure 5-11. Since the calibration is done under with the transmitted bit either at 0 or 1, the DC levels of the toggling signals at the output of the baseband amplifier are not the same. The $g_m - C$ filter uses a very small bias current to generate a small g_m in order to recover the DC level of the signal without using a large capacitor. Achieving the same with a passive R-C filter requires large resistors, large capacitors, or both. The filter cutoff is set to be low enough to reject the baseband signal but not so low that it takes a long time for the filter output to settle. Although the same job can be done by introducing a programmable offset

into the comparator, this approach was disregarded since it would require additional comparator calibration steps before operation.

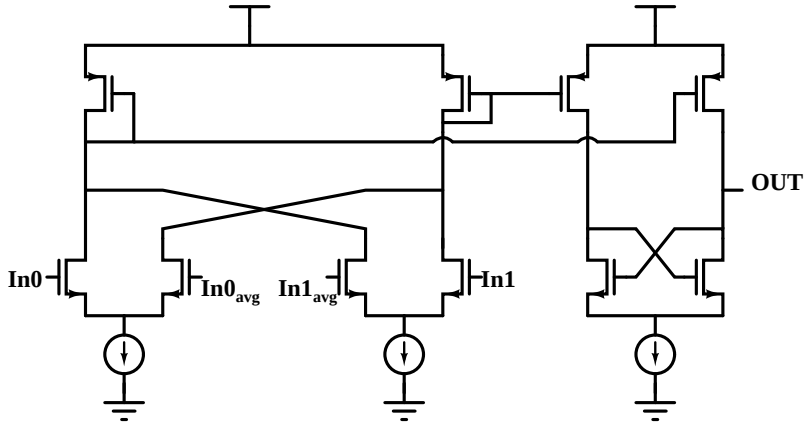


Figure 5-12: Offset-Compensated Comparator used in Uplink Demodulator

The outputs of the amplifiers and the filters are sent to a 4-input comparator shown in Figure 5-12. The first stage of the comparator references each output of the amplifier to its DC reference value, and compares the result. The second stage of the comparator consists of cross-coupled transistors driven by differential AC current sources. The cross-coupled transistors are cascoded with a DC current source in order to increase the gain around the switching threshold for faster, and more sensitive response.

Multiplexer

The digital demodulated outputs from the two sub-networks are passed to a multiplexer. Although building a digital multiplexer is a trivial affair, the job at hand is made complicated by the absence of a "select" input to the multiplexer due to the lack of knowledge at the base station about the origin of incoming data that is yet to come. A simple solution for this problem could be to monitor each sub-network for a fixed amount of time before switching to the other. However, in order to detect incoming data from a sub-network, the PLL in the clock recovery circuit must be given sufficient time to start-up and lock. The start-up and lock routine would then need to be performed upon every switch, which leads to larger power consumption

and higher probability of missing packets.

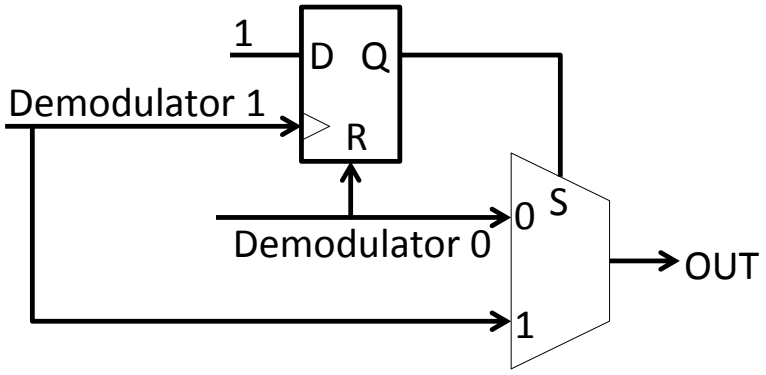


Figure 5-13: Multiplexer to Select Between 2 Sub-Network Uplink Demodulator Outputs

Instead, the solution that has been employed in Figure 5-13 is to let the multiplexer detect which input is toggling and automatically select that input. This assumes that data is coming in from only one sub-network at any given time. This has been taken care of by the MAC protocol described in Section 6.2. The demodulator outputs are fed to a D-flip flop with an aynchrnonous reset. The output of the flip-flop acts as the select input of a 2:1 multiplexer. The outputs of the demodulator are LOW when no data is being transmitted. If data starts coming in from Sub-Network 0, the multiplexer is configured to select the output of Demodulator 0. The multiplexer select input stays at the same value till data starts coming in from Sub-Network 1, upon which the multiplexer is configured to select Demodulator 1. This implementation of the multiplexer causes the loss of at most one bit of the preamble, which can be tolerated since the preamble of the packet contains no information and is only used for locking the PLL.

Clock-Data Recovery

A block diagram of the PLL used is shown in Figure 5-14. It consists of a Phase Detector (PD), Frequency Detector (FD), Charge Pump (CP), Loop Filter (LF) and a Voltage-Controlled Oscillator (VCO). Since the required output frequency of the clock is quite low (300kHz-1MHz), the PLL is operated at the output frequency and

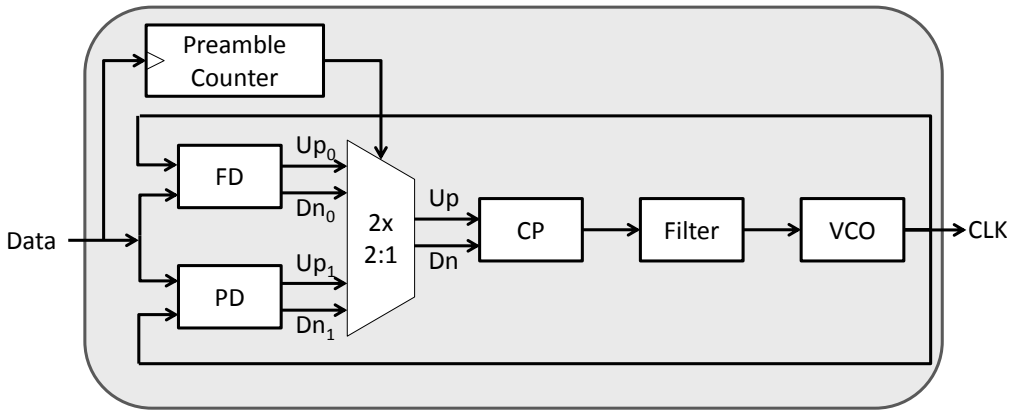
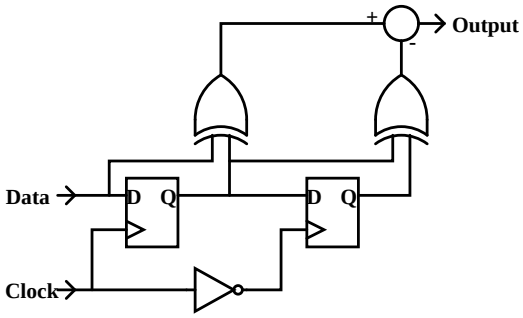
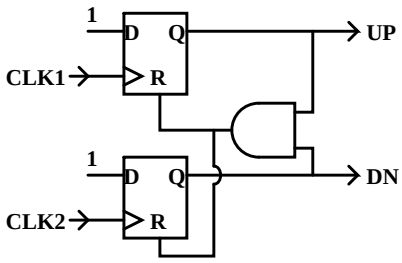


Figure 5-14: Block Diagram of PLL used for CDR

no clock division is used in the feedback path. Each block in Figure 5-14 is described in detail in the following paragraphs.



(a) Hogge Phase Detector. The output is decoded to produce the Up and Dn inputs for the CP.



(b) Frequency Detector

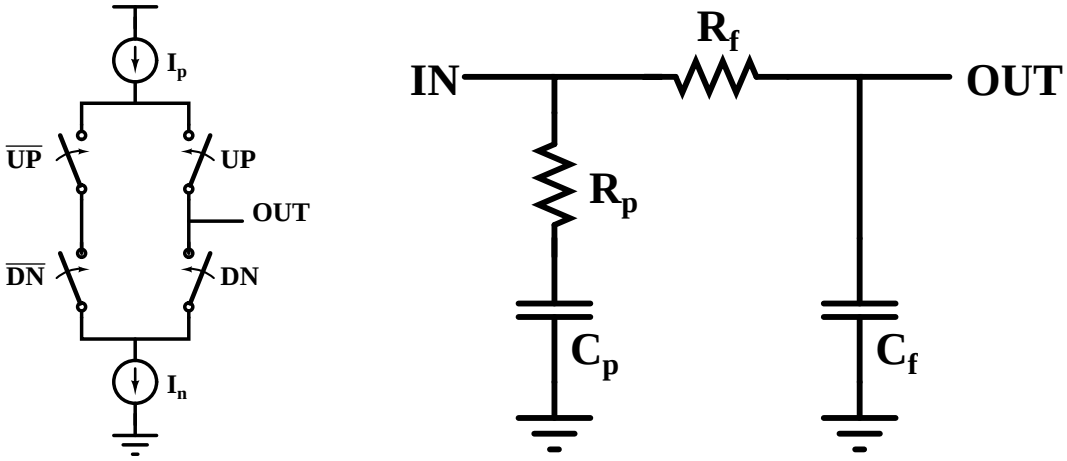
Figure 5-15: Schematic of Phase and Frequency Detectors Used

The PD is implemented as a Hogge Phase Detector [48], as shown in Figure 5-15(a). Incoming data is sampled by the recovered clock, and the sampled data is re-sampled by the complement of the recovered clock. Under lock, the positive edge of the recovered clock is offset by a half-bit period duration compared to the incoming data, as shown in [31]. The phase detector constant K_D for the Hogge PD is

$$K_D = \frac{V_{DD}}{2\pi} \tag{5.10}$$

Each uplink packet contains a preamble of alternating 1's and 0's that allows the PLL to lock on to the transmitting clock. Since the packets could be widely separated

in time, the data input to the PLL can remain stable at a single value for a long time. This would pull the VCO input voltage close to zero and stop the clock oscillations. From the schematic of the Hogge PD in Figure 5-15(a), it can be inferred that the detector fails to lock when the clock is not oscillating. In order to avoid this issue, the loop keeps a separate Frequency Detector (FD) selected between packets, as shown in Figure 5-14. As the preamble of an uplink packet arrives, the FD causes the loop to act as a Frequency-Locked Loop (FLL) and control can subsequently be passed to the PD. The schematic of the FD is shown in Figure 5-15(b).



(a) Charge Pump (b) Loop Filter

Figure 5-16: Schematic of Charge Pump and Loop Filter Used in PLL

The charge pump used is shown in Figure 5-16(a). Switches have been implemented with cascoded transistors. The circuit contains a bypass path for the current when both signals UP and DN are LOW, which ensures the voltage across the current sources, which are implemented by current mirrors, does not go to zero. This, and the use of cascode transistors prevents the charge pump output voltage from drooping between successive clock edges and creating spurs in the output spectrum. The current sources I_p and I_n source and sink $10\mu A$ of current respectively.

The loop filter used is shown in Figure 5-16(b). The resistor $R_p = 10k\Omega$ and capacitor $C_p = 2$nF form the zero in the PLL transfer function that prevents the loop from becoming unstable. $R_f = 100\Omega$ and $C_f = 100$pF form the pole that restores the -40dB/decade slope of the transfer function beyond the unity gain crossover frequency.

The capacitors C_p and C_f are off-chip. Since $C_f \ll C_p$, the transfer function of the loop filter can be approximated as

$$\frac{V_{OUT}(s)}{I_{IN}(s)} = \frac{1}{sC_p} \cdot \frac{1 + sC_pR_p}{1 + sC_fR_p}. \tag{5.11}$$

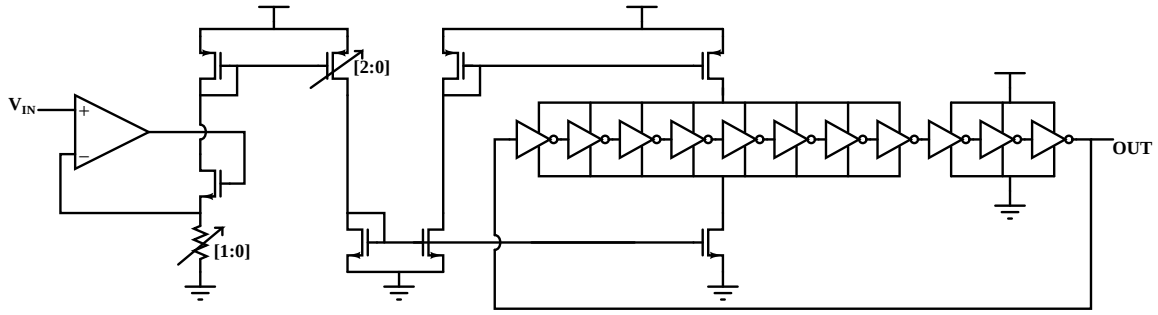


Figure 5-17: Schematic of Voltage-Controlled Ring Oscillator

The VCO used is shown in Figure 5-17. It is a ring oscillator with 11 inverters, where eight inverters that are current-starved, and the other three ensure the output clock has a small enough rise and fall time. The input stage of the VCO needs to change the current-source value according to the input voltage. Directly loading the preceding stage with the resistor is not advisable since it would load the VCO control line, leading to undesired droop in the voltage and spurs in the output spectrum. Controlling the current through a transistor connected in common-drain configuration introduces an error with both static and dynamic components due to the V_{GS} of the transistor. The feedback configuration used allows the current to be linearly controlled by the input voltage without any effect from the transistor parameters. The VCO is provided with two bits of tuning for changing the VCO constant, and three bits of tuning for changing the center frequency. The latter three bits are automatically initialized upon startup by using the loop as an FLL. The tuning bits are adjusted while the system reset is asserted so that the output of the PLL is locked to the local clock at the base station, which is in the same range as the sensor node transmit clock frequency.

Figure 5-18 shows a plot of the simulated VCO characteristics. The output fre-

quency is linear over a wide input voltage range. From the slope of the plot, the VCO constant is found to be $K_{VCO} = 800\text{kHz/V}$ under a particular tuning-bit setting.

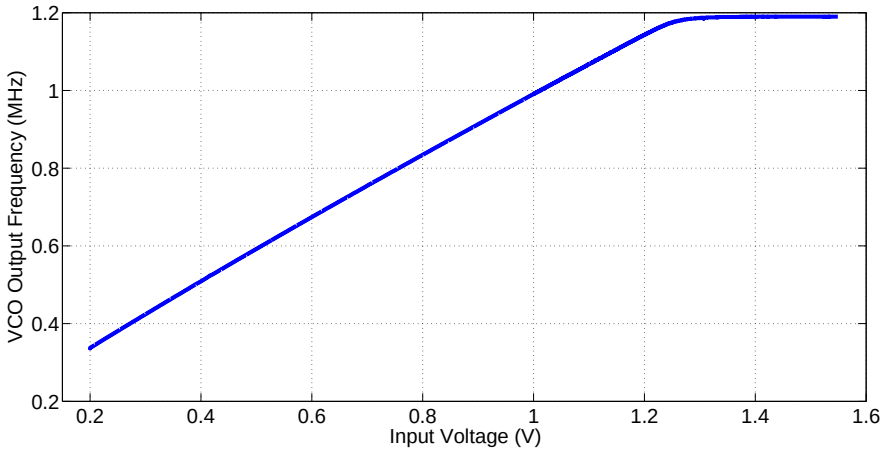


Figure 5-18: Simulated VCO Output Characteristics

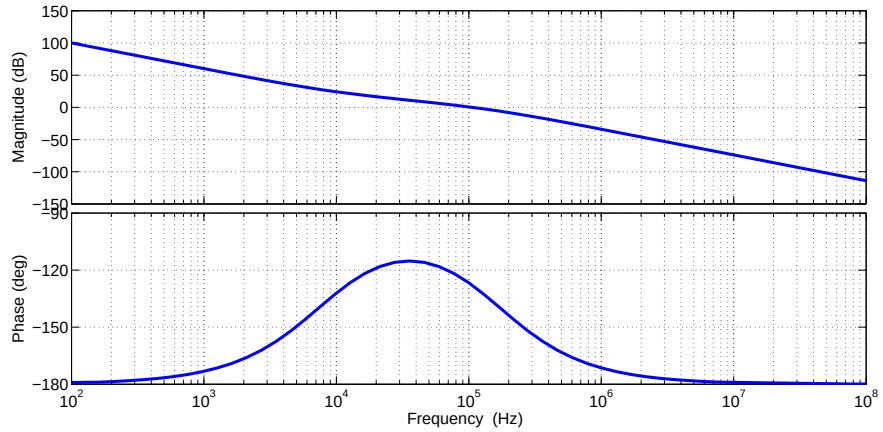


Figure 5-19: Open Loop Frequency Response of PLL

The loop transfer function of the PLL is

$$L(s) = -\frac{I_{cp}K_{VCO}}{s^2C_p} \cdot \frac{1 + sC_pR_p}{1 + sC_fR_p}. \tag{5.12}$$

At 1rad/s, the magnitude of the loop transfer function is $L(s = j \cdot 1rad/s) = 4 \times 10^9$, with a zero at 50krad/s and a pole at 1Mrad/s. The theoretically calculated frequency response of the loop gain is shown in Figure 5-19. The magnitude of the loop gain

initially falls as −40dB/decade, before hitting the zero. It crosses the unity gain (0dB) line at approximately 100kHz, with a phase margin of 50°. The crossover point is one decade away from the nominal frequency at which it is supposed to operate for the given bit settings, which is 1MHz. The maximum phase margin of the loop for any value of gain above 0dB is greater than 60°. The loop gain returns to the original −40dB/decade slope and −180° phase close to the loop operating frequency so that it has a zero steady state error to a ramp input in the phase, which is useful for a fast start-up.

Chapter 6

Data Link Layer

The previous chapter discussed the PHY layer for the network. This chapter presents the next layer in the seven-layer OSI model for networks: the Data Link Layer (DLL). A brief literature review of existing MAC protocols for BANs is presented. The custom-MAC designed for the network is also presented, including a network configuration routine. Finally, the packet structures and error-coding schemes used are described.

6.1 Network Architecture Considerations

As described in Section 2.3, the network is divided into two sub-networks to improve power-transfer efficiency. Inductors within a sub-network are connected in parallel to each other using multiple paths for network reliability and fault-tolerance. Hence, messages transmitted by the base station (downlink) to a sensor node in a particular sub-network are also transmitted to all other sensor nodes in that sub-network. While this is unnecessary for messages that are intended for only one sensor, it is useful for broadcasing beacons across the network. Section 6.2 describes the MAC protocols used for the network and outlines the necessity for having easy broadcast capability. Messages transmitted by the sensors (uplink) are also, in theory, available to all other sensors in the network which could create data security issues. However, in order to be demodulated by other sensor nodes, the uplink packet has to go through two

inductive hops, each with approximately 1% power efficiency. Demodulating such weak signals is beyond the power budget of the sensors in the network.

6.2 Medium Access Control (MAC)

Design of the MAC sub-layer primarily revolves around the network access scheme used. There are many ways in which network resources can be shared among nodes, some of which are listed below. Brief descriptions of how each of the schemes work are provided in Appendix C.

- Contention Access (CA)
- Carrier-Sense Multiple Access (CSMA)
- Time-Division Multiple Access (TDMA)
- Frequency-Division Multiple Access (FDMA)
- Code-Division Multiple Access (CDMA)

Several MAC schemes have been reported in literature for Wireless Sensor Networks (WSNs) and Wireless BANs (WBANs). MAC protocols for the former have been reported in [49, 50, 51], but they are not suited for low-power BAN applications. Commercial standards, such as IEEE 802.11, Bluetooth and IEEE 802.15.4/Zigbee [52] also include excessive overhead for supporting peer-to-peer networks and a variety of PHYs. A TDMA MAC for WBANs is proposed in [53], but such a scheme is wasteful for sensors with extremely low transmit duty cycles. A MAC solution specifically devised for Wireless BANs in a star/single-hop topology is presented in [54], but it has several features making it unsuitable for use with low-power sensors in the desired network. It requires sensors to go to sleep for a pre-determined amount of time, after which both the sensor and the base station wake up. This sets an upper-bound on the maximum sleep time due to timing offsets between the sensor and the base-station. Moreover, it relies on CSMA, which is untenable for the sensors sending

data through load modulation, which would have to go through two inductive hops for another sensor to recognize.

MAC solutions for fabric BANs have also been presented in previous research. [16] presents a MAC for a fully-wireline fabric BAN that uses a TDMA scheme with a star topology. It supports CA peer-to-peer networking only in the absence of a central node. A MAC for a fabric Personal Area Network (PAN) is presented in [55], which uses a CA scheme to link electronic circuits on different layers of clothing. The Fabric BAN needs to be designed to act as a general-purpose network capable of handling various kinds of biomedical sensors with different network access requirements. These can range from sensors that need to stream data continuously at rates of the order of 10kbps, such as ECG, EEG and EMG sensors [56, 3] to sensors that need to send small packets of information every couple of minutes or hours, such as body temperature, blood glucose or blood oxygenation monitors.

TDMA schemes are well suited for networks with sensors that transmit information regularly. Sensors that stream ECG, EEG or EMG waveforms are ideal candidates for TDM access mechanisms. However, assigning fixed timeslots to sensors that transmit infrequently is wasteful of network resources. On the other hand, CA schemes, while good for infrequent transmitters, lead to excessive collision rates and network inefficiency with high transmit-duty cycle sensors. A hybrid TDMA-CA scheme has been implemented in this work to address this issue. Sensor nodes are classified as *stream*-mode or *burst*-mode sensors, depending on whether they are high- or low-duty cycle transmitters respectively. The base station, which is the hub of the network, determines the type of each sensor joining the network. The base station initially assigns a a fixed timeslot to each stream-mode sensor in the network, whose duration depends on the number of stream-mode nodes in the network. Upon cycling through all the stream-mode nodes, the base station opens up a CA period for burst-mode nodes to transmit, if they choose to. Owing to the network architecture, burst-mode sensors are incapable of doing CSMA, and hence packets have a non-zero collision probability. In order to address this, the network includes error detection and Automatic Repeat Request (ARQ) capability, which is discussed in detail in

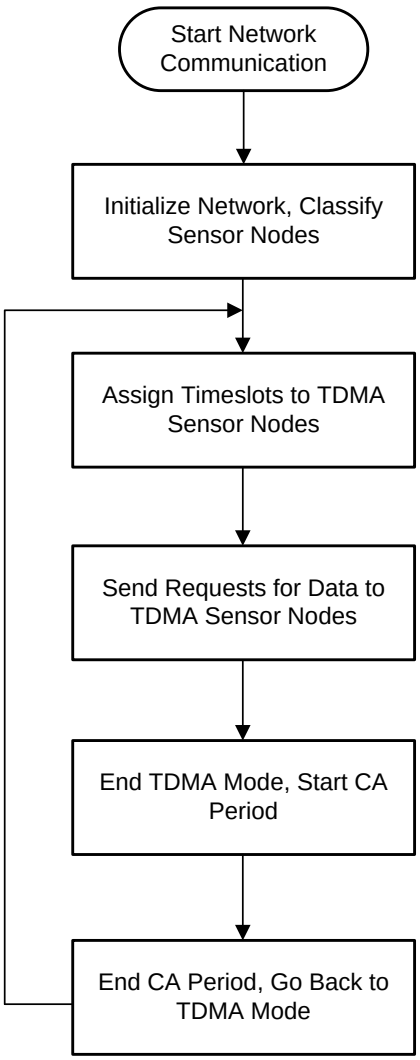


Figure 6-1: Top-Level Flowchart for MAC used in Fabric BAN. Details of downlink data sent to and uplink data coming from each sensor are not shown in this diagram.

Section 6.5. A top-level flowchart for the MAC is shown in Figure 6-1.

The designed MAC scheme avoids the need for clock synchronization between the base station and the sensors. Both in TDMA and in CA mode, the sensor node follows a "listen-before-transmit" principle, which eliminate the possibility of mistimed transmissions. This allows sensor nodes to go to sleep for arbitrarily long periods of time before waking up, receiving power, receiving appropriate instructions and then transmitting data.

6.2.1 Time-Division Multiplexing

Figure 6-2 shows a flowchart for the network during TDMA mode. The base station maintains a list of all stream-mode sensors from a network initialization routine. In the TDMA mode, each stream-mode sensor is allocated a fixed time period for transmitting data back to the base-station. The allotted time is communicated as the maximum packet size that can be transmitted by the addressed sensor. The network can handle a maximum packet size of 4KB, which gives a maximum allotted time slot of 32ms at 1Mbps. Stream-mode sensors are configured to transmit at the highest bitrate possible due to the large volume of data they transmit. The received packet is checked for errors and an ARQ is issued in case errors are found. Once the packet is succesfully received or the limit on the number of erroneous transmissions is reached, the base station sends an acknowledgement (ACK) packet and moves to the next sensor, repeating the same routine.

6.2.2 Contention Access

The network enters CA mode once all the stream-mode sensors have transmitted data. A flowchart for the network during CA mode is shown in Figure 6-3. The start of the CA mode is signaled by the base station to all sensors using a beacon. Each sensor node has a Psuedo-Random Bit Sequence (PRBS) generator which generates a random number upon receiving the CA beacon. A decision on whether to transmit in the current CA cycle is taken by comparing the PRBS value against a transmission probability, which is preset depending upon the function of the sensor and the frequency with which it needs to access the network. If a decision is taken to transmit in the current CA cycle, another PRBS is used to generate a random time-offset from the start of the CA period at which to start transmitting. This is done to prevent packets from multiple sensors colliding at the start of the CA period, and the rest of the CA period remaining unused. In case of packet transmission errors, the base station sends an ARQ to the particular sensor, otherwise it sends an ACK. In case errors prevent the base station from knowing the network ID of the sensor node that

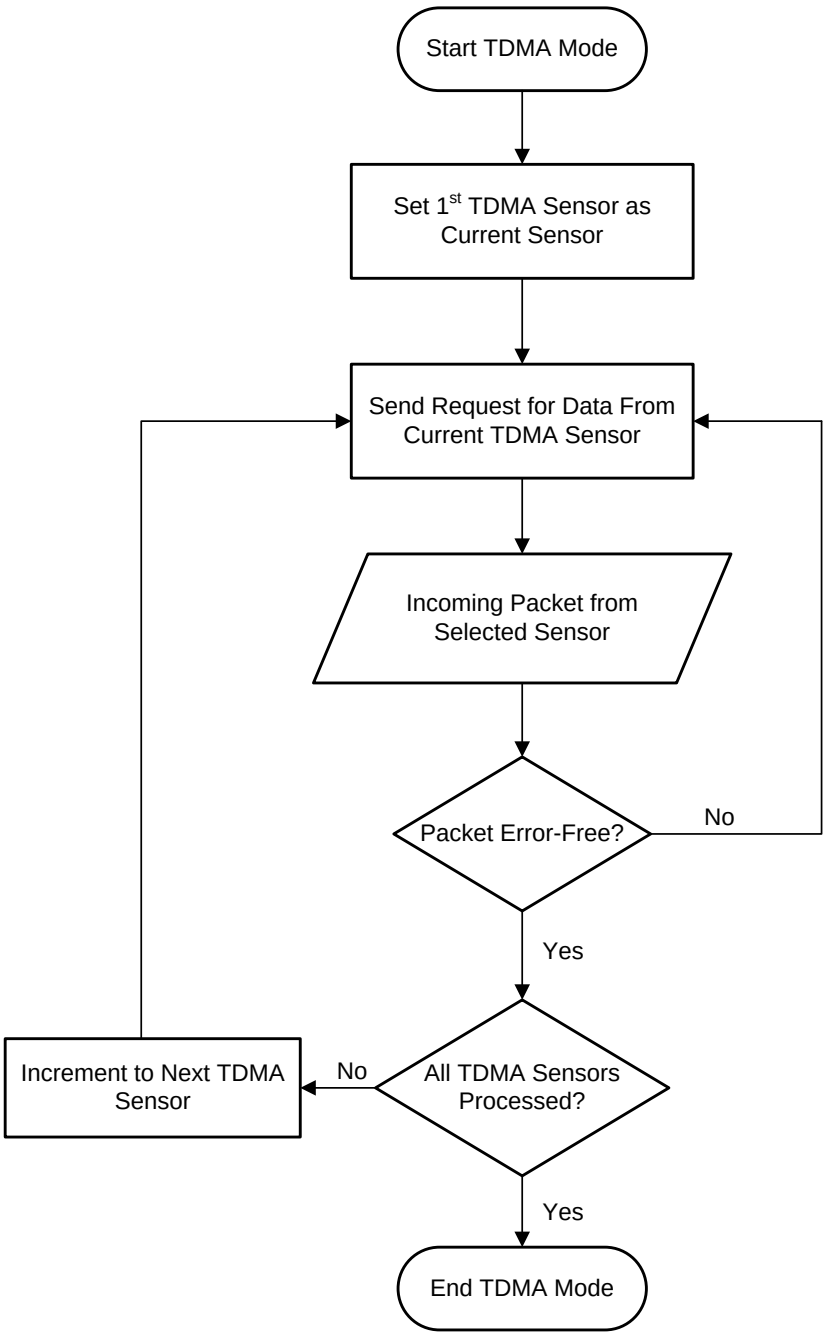


Figure 6-2: Flowchart for TDMA Communication with Sensor Nodes

sent the packet, the base station does not respond to the incoming packet. This lets the transmitting sensor to know that its transmission was not received succesfully. The end of the CA period is signaled to all sensors using a separate beacon.

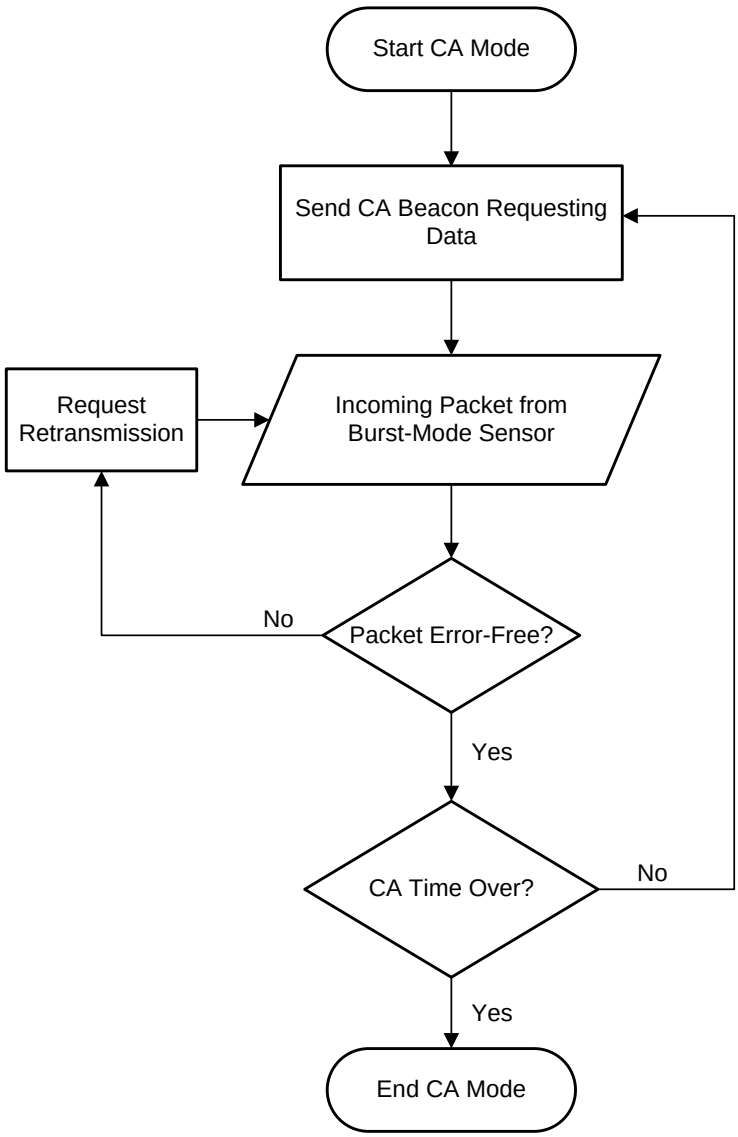


Figure 6-3: Flowchart for CA-Mode Communication with Sensor Nodes

6.3 Network Initialization

Upon startup, the base station has to initialize the network in order to transact data with the sensors. A flowchart for the network configuration routine is shown in Figure 6-4. Upon staring the power amplifier that transmits power across the inductive link, the base station waits for 8 seconds for the sensor nodes connected to the network to charge up the DC storage capacitors. It then transmits a configuration beacon to all sensors in the network. Upon receiving this beacon, all sensors in the network automatically defer their response in a manner similar to the CA mode

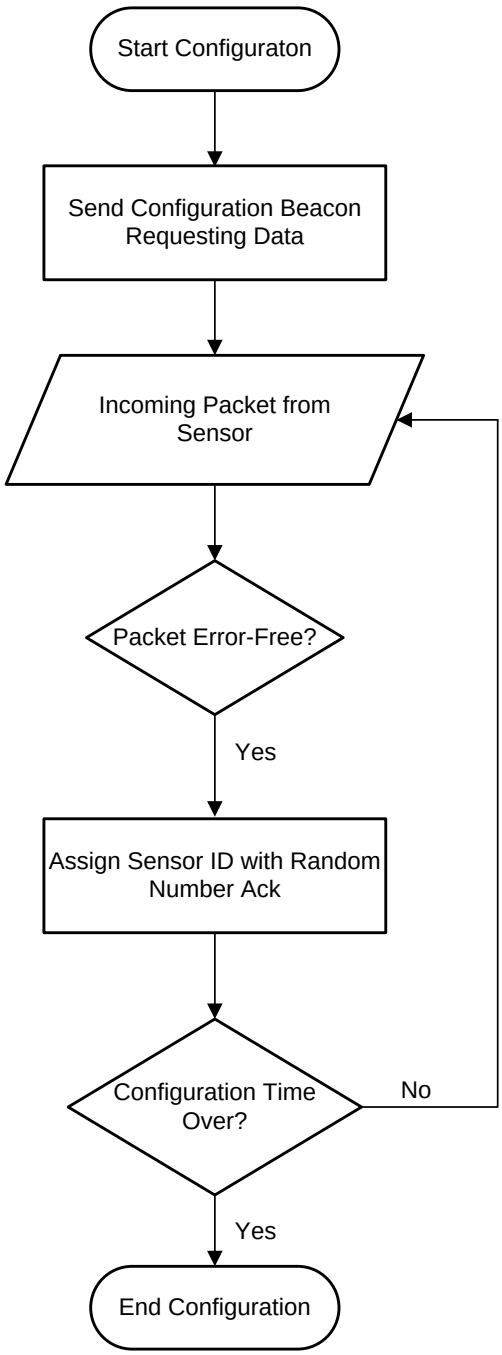


Figure 6-4: Flowchart for Network Configuration Mode

described in Section 6.2. Each sensor transmits a packet containing information about its network access requirements and a PRBS-generated random number. The base station, upon receiving this packet, uses the random number as an ACK and assigns the sensor's network ID and programs it as a stream- or burst-mode sensor.

If two uplink packets collide causing the base station to produce a garbled message the base station cannot understand, it does not respond. The absence of an ACK lets the affected sensors know that they have to try transmitting again. If the base station receives and acknowledges the wrong random number, the sensor node does not accept the ID assignment and tries again.

6.4 Packet Structure

6.4.1 Uplink

Figure 6-5 shows the packet structure used for uplink communication. The packet consists of a 256-bit synchronization sequence of alternating 1's and 0's, which allows the PLL at the base station to lock on to the transmit clock. A 16-bit preamble containing the transmitting sensor's ID follows the sync sequence, which is followed by a 12-bit message size (in bytes). The data payload is split into segments of 16, 32, 64 or 128 bytes, depending on a 2-bit encoded segment size field in the downlink packet preceding the uplink. A 16-bit CRC checksum is generated for each segment for error detection. This enables the base station to detect packet collisions in CA mode and other network errors.

6.4.2 Downlink

Three examples for different kinds of packets used for downlink communication are shown in Figure 6-6. Each packet has a 4-bit header that corresponds to the message

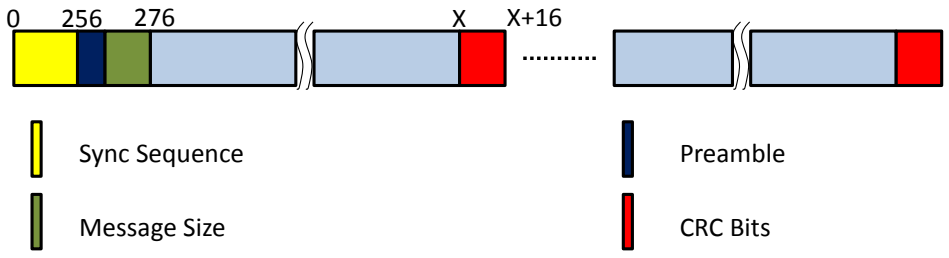


Figure 6-5: Packet Structure for Uplink Communication

type. During network configuration, the first beacon sent out contains just the header. All packets except the CA start and end beacons contain the addressed sensor ID as the next 8-bits of the packet. The following bits vary according to the packet header

- For sensor ID assignment, the 8-bit random number acknowledgement follows.
- For TDMA and CA packet request, the 2-bit encoded segment size and 10-bit encoded message size follow.
- For ARQ, the 2-bit encoded new segment size and 8-bit encoded error location follow.

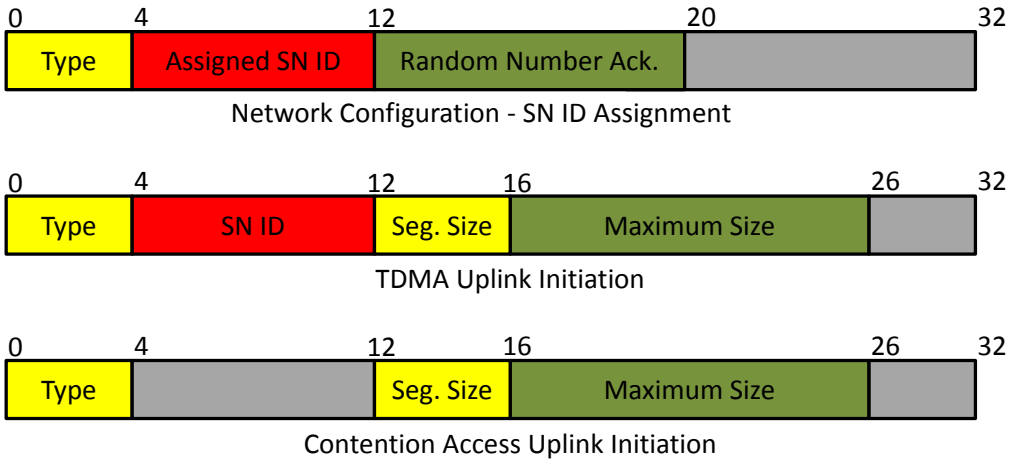


Figure 6-6: Packet Structure for 3 Packet Types used in Downlink

6.5 Error Detection and ARQ

An error detection scheme is provided with uplink communication in order to ensure Quality of Service (QoS). As discussed in Section 6.4, each uplink packet is divided into segments. Each of these segments contains a 16-bit trailing Cyclic Redundancy Check (CRC) checksum. The 16-bit CRC checksum is implemented using the CRC-16-CCITT polynomial, which goes as $x^{16} + x^{12} + x^5 + 1$. This polynomial is widely used in protocols such as Bluetooth. A discussion on CRC error detection can be found in [57].

The base station uses this checksum to check the validity of the transmitted data. In case of an error in one of the segments, the base station asks the transmitting sensor to retransmit *everything* including and after the erroneous segment. This is done in order to minimize downlink transmit time by avoiding transmitting information about each erroneous segment. Moreover, it is simple and very effective for burst errors, which are highly likely due to dynamic changes in the network parameters. The retransmission is attempted with a smaller segment size, in an effort to get more segments across without errors. Each communication cycle with a sensor node can contain at most 4 attempts with errors, after which the base station ceases asking for retransmissions and moves on.

Error detection is not employed in downlink packets because of the high SNR involved. Moreover, if the downlink signal received at the sensor is too weak for error-free detection, there is no possibility of using the same signal to power up the sensor node.

Chapter 7

Implementation and Testing

This chapter presents the CMOS implementations for the designed base station and sensor node network modules. The test setup used is described and results are presented.

7.1 CMOS Implementation and PCB Design

The base station and sensor node network modules were implemented in TSMC 180nm 1P6M Mixed-Signal technology. The base station die occupies an area of 2.2mm×2.2mm and contains 64 pads. It contains two 27MHz power transmitters for two sub-networks, along with their associated on-chip capacitors for the oscillator tuning networks, associated OOK PWM modulators and impedance modulation demodulators. The outputs of the demodulators are multiplexed and passed through a CDR circuit for data recovery. The digital baseband implements the DLL and has a gate count of 1630 gates. Figure 7-1 shows a die photograph of the base station.

The sensor node die occupies an area of 2mm×1.8mm and has 50 pads. It takes as input the data measured by the Analog Front-End (AFE) and converter by the ADC of the biomedical acquisition circuits and buffers it in an SRAM. The 4KB SRAM has been generated using a standard compiler. Inductively-transferred power is rectified and stored on a 100μF off-chip capacitor. The digital baseband interprets the instructions from the base stations and has a gate count of 1230 gates. Figure 7-2

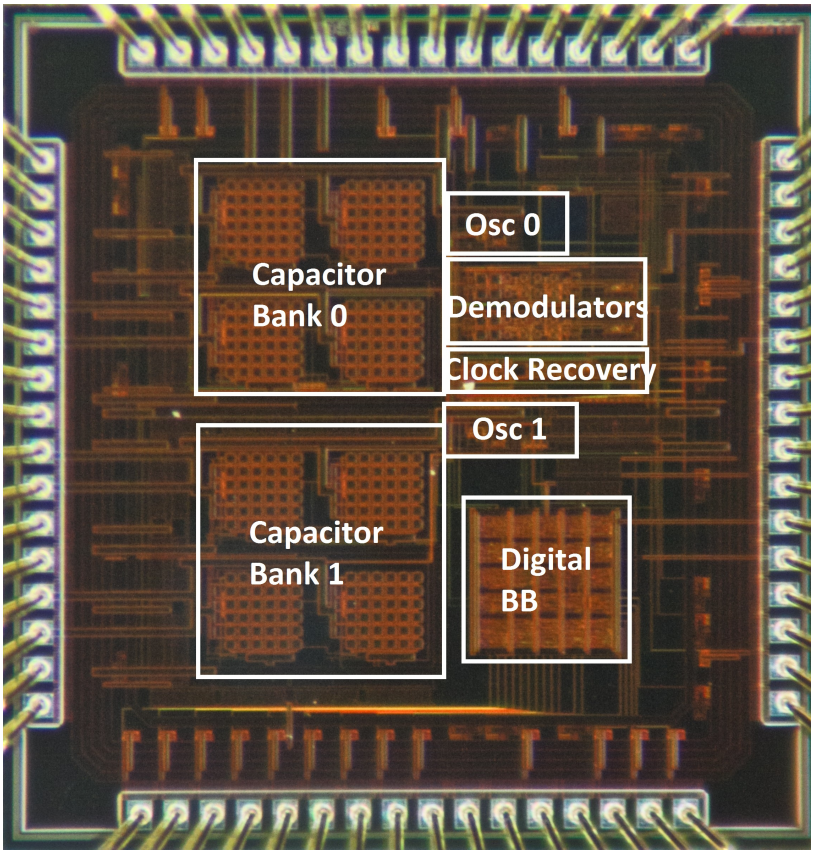


Figure 7-1: Die Photgraph of Base Station

shows a die photograph of the sensor node network module.

All pads were wire-bonded to the package. Since the frequency of operation is well below 100MHz, both dies were packaged in a 64-pin TQFP package in order to allow for the use of the same socket. A 4-layer Printed Circuit Board (PCB) was designed to test both chips. An Opal Kelly FPGA testing kit with a Xilinx Spartan-6 FPGA was used to configure the shift registers that store the tuning bits for the analog blocks in the chip and to implement the digital MAC. The PCBs contain an interface to the FPGA module, level converters and in the case of the sensor node, voltage regulators and storage capacitors for the rectified DC output.

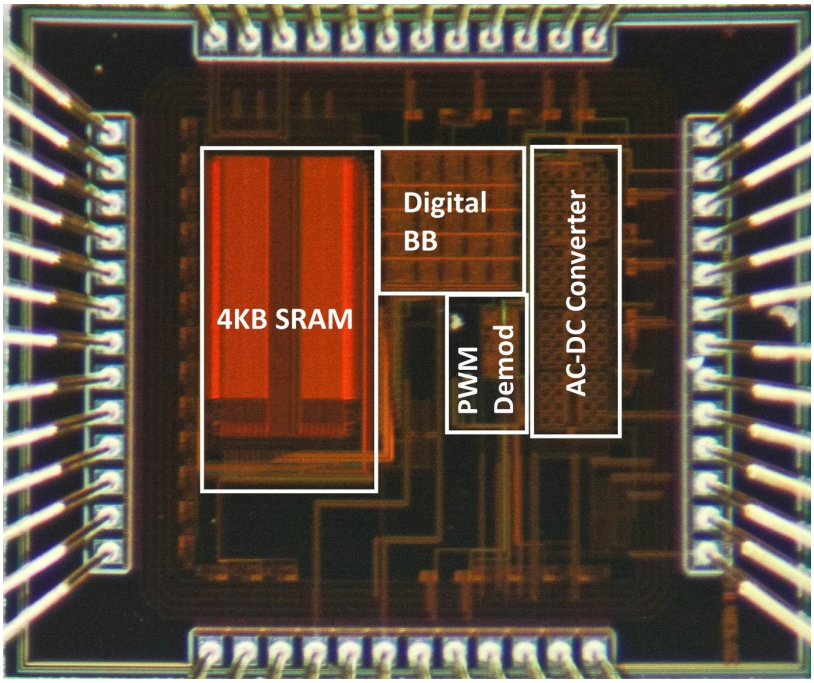


Figure 7-2: Die Photograph of Sensor Node Network Module

7.2 Test Setup

A photograph of the test setup is shown in Figure 7-3. Clinical trials for testing the system on real patients have not been performed. Instead, two pieces of fabric, one each for the base station and the sensor node, have been taped to cardboard stands and the link between them is tested. Epoxy-based conductive glue has been used to connect wires to the inductors on fabric. The other end of the wires is connected to the PCB by SMA connectors.

The chips are mounted on a 64-pin TQFP-footprint socket. The Opal Kelly FPGA kit controlled through a computer is used to program the tuning bits for the analog components on the chip, and for running an HDL implementation of the designed DLL. The PCB is connected to the FPGA board by using the expansion connectors on the latter. Level shifters are used to interface between the 3.3V and 1.8V I/O levels of the FPGA and the designed circuit respenctively. The base station PCB uses two separate supply voltages: 3.3V for the power transmitter and 1.8V for the modulators, demodulators and the clock recovery circuits. A block diagram of the test setup is shown in Figure 7-4.

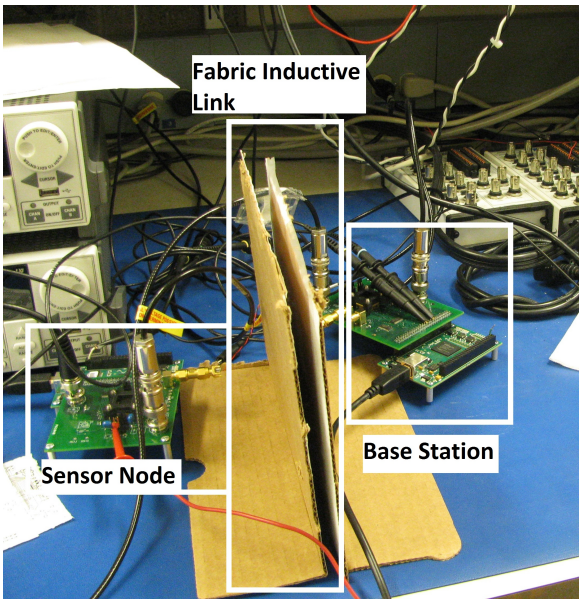


Figure 7-3: Photograph of Test Setup

7.3 Measurement Results

The analog blocks on both the base station and sensor node were tested for different packet sizes and inductive coupling coefficients. These blocks include the power transmission and rectification circuits, data modulators and demodulators at both ends and the clock recovery circuit at the base station. The digital baseband and SRAM were synthesized on the FPGA used for testing the system, as shown in Figure 7-4.

7.3.1 Power Transmitter

The system end-to-end power transfer efficiency was measured, from DC bias current drawn by base station to DC current supplied by AC-DC converter at sensor node. Efficiency plots for two different PA driving strengths are shown in Figure 7-5. The maximum attainable efficiency at 1x power is 1.2%, which agrees in order of magnitude with the theoretically predicted value in Table 4.1 for coupling coefficient $k = 1$. The generated V_{DD} for this observation was 1.5V. At low output power, the higher power transmission is more inefficient as expected. The behavior reverses as the output power is increased, which causes the output voltage to droop sharply for lower power transmission. Careful characterization of efficiency would allow the network to be at

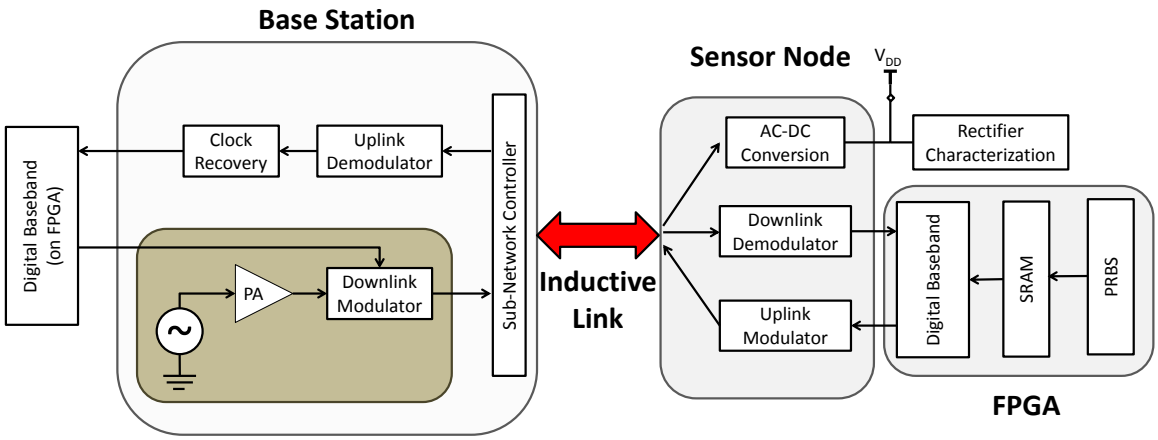


Figure 7-4: Block Diagram of Test Setup. The analog blocks on the chips were tested, while the digital logic was implemented on an FPGA.

the optimal efficiency for a given power demand by the sensor node.

7.3.2 Data Transmission

The OOK PWM envelope detection and demodulation circuitry at the sensor node consumes 1.5μW power from the 1.6V recovered V_{DD}. The impedance modulating switch has power consumption below 100nW. Figure 7-6 shows the OOK PWM data at the input of the sensor node and the demodulated output for a network configuration packet transmitted by the base station.

At the base station, the demodulator and CDR ciircuits consume 138μW power from a 1.4V supply. Figure 7-7 shows the impedance modulated data at the input of the base station and the demodulated output, for a network configuration ACK packet transmitted by the sensor node. Figure 7-8 shows the demodulated output and the synchronized clock output of the PLL for a similar packet.

7.3.3 Future Measurement Work

A complete system with multiple sensor nodes of different types needs to be implemented, measured and characterized. Additionally, the digital baseband circuits and SRAM on the base station and sensor nodes needs to be tested.

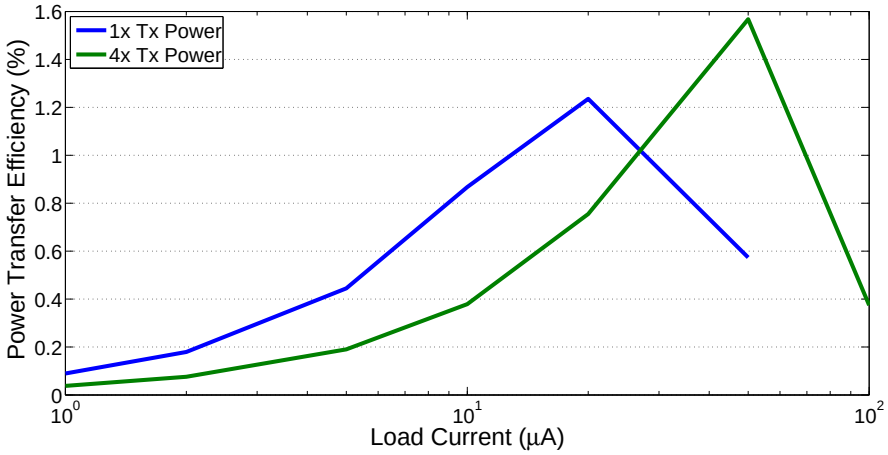


Figure 7-5: Measured End-to-End Power Transfer Efficiency Plots. Measurements were taken with 2V supply voltage for the power transmitter at the base station. The input power with 1 PA was 2.7mW, and with 4 PAs was 6.6mW. The inductors had a 5mm physical separation.

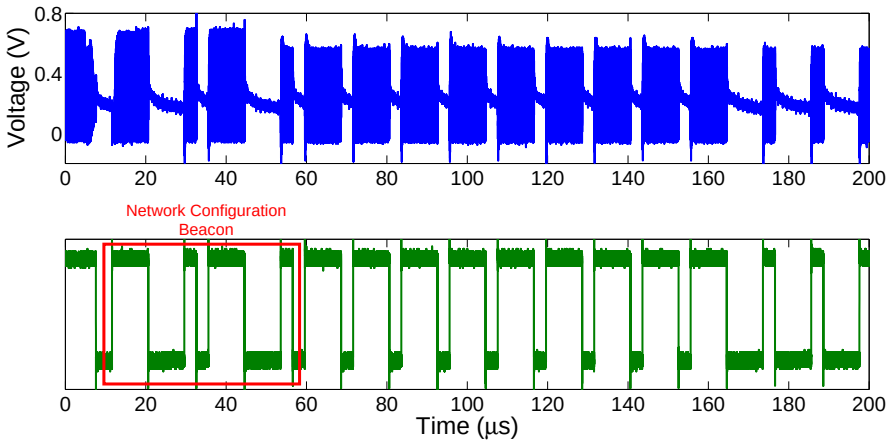


Figure 7-6: Input and Output Waveforms for Demodulator at Sensor Node with 5mm inductor separation

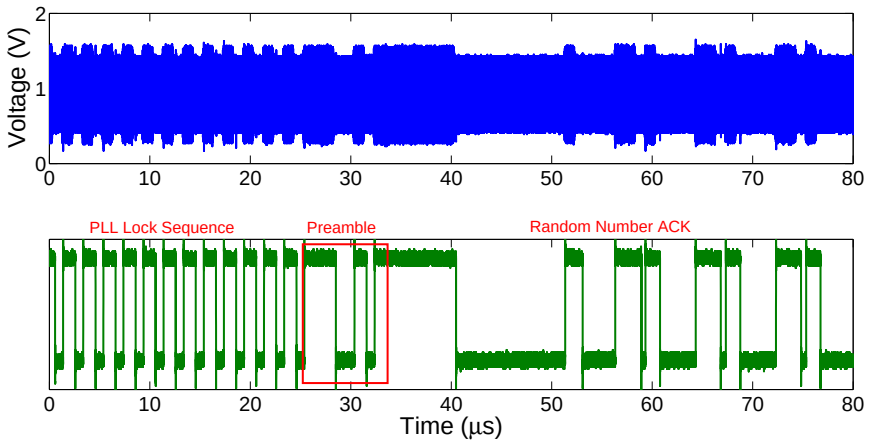


Figure 7-7: Impedance Modulated Input and Output Waveforms for Demodulator at Base Station with 5mm inductor separation

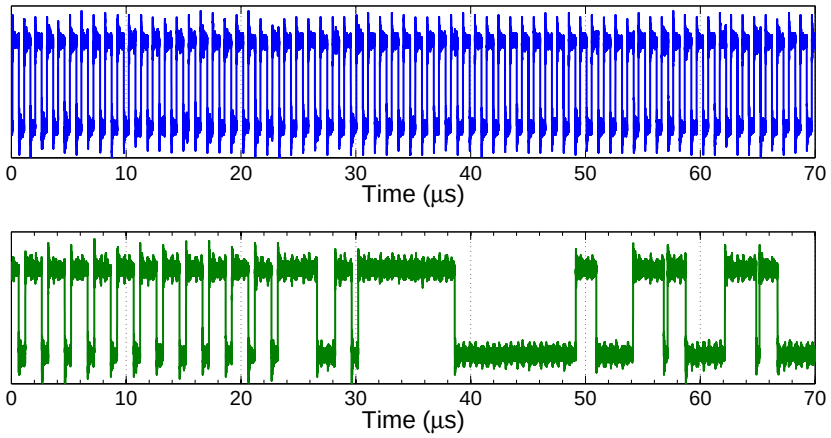


Figure 7-8: Data Input and Synchronized Output Clock for PLL at Base Station

7.4 Summary

A summary of the system performance is provided in Table 7.1

Base Station V_{DD}	2.0V (Power Transmitter) $1.4V$ (Modulator, Demodulator, CDR)
Base Station Power	2.7mW (Power Transmitter) 104μW (Demodulator) 38.3μW (CDR)
Power Transfer Efficiency	1.2% (max.)
Sensor Node V_{DD}	1.5V
Sensor Node Active Communication Power	$< 2\mu$W
Technology	180nm CMOS

Table 7.1: System Performance Summary

Chapter 8

Conclusions

This chapter summarizes the work done in the thesis and lists possible directions for future research on the topic of Fabric BANs.

8.1 Thesis Summary

This thesis presented a design of a BAN for diverse healthcare applications on conductive fabrics. Specifications were developed for the network with focus on the asymmetric energy budgets at various nodes of the network. A star topology was chosen with a network base station as the hub, and sensor nodes each talking directly only with the base station. A near-field resonant inductive coupling scheme was chosen for linking the sensors to the base station for its ability to deliver power wirelessly to sensor nodes with relatively high efficiency and minimal inconvenience to the user. A network architecture that addresses issues unique to circuits on fabrics was chosen. Techniques for reducing energy wastage by transmitting power to network locations with sensor nodes were presented.

Modulation schemes that could operate under the asymmetric budgets at the base station and sensor nodes were chosen. A OOK PWM scheme was chosen for transmitting downlink messages in order to avoid the need for carrier and clock recovery at the sensor nodes. The OOK modulation is performed on the transmitted power in order to avoid the use of a separate frequency band. Impedance modulation was

used for transmitting uplink messages. This reduces the uplink communication effort at the sensor nodes to the order of a few 10s of fJ/bit. Simple OOK modulation was chosen for the uplink, with demodulators to amplify the weak received signal at the base station and a clock recovery circuit for synchronization. The use of ASK modulation for both uplink and downlink messaging using the same carrier prevents the network from being full-duplex, which is acceptable since the network has a low access duty cycle.

A custom-DLL has been designed to minimize the energy overhead of network access and error handling. Two separate network access schemes are time-multiplexed to allow sensors with different access requirements choose the one that best suits their needs. A simple error-detection scheme has been used with an ARQ mechanism that tries to reduce the packet error rate in successive retransmissions of the same message.

The implemented base station can support 16 sensors linked to any one out of four inductors on clothing. It has a power consumption of 2.86mW, and it can supply 33.6μW maximum power to the sensors' biopotential acquisition circuits. Modulation and demodulation circuits at the sensors consume less than 2μW power when active.

8.2 Future Directions

Integrating Sensor Network Module with AFE: The design presented contained only the network communication module for the sensor node. Biopotential acquisition circuitry was to be on a separate die. In order to reduce system area and cost, the AFE of the micropower sensors need to be integrated with the network module. The network's capability to handle sensors with a wide range of power and communication requirements would allow this to be done relatively easily.

Clinical Trials: Real-life clinical testing on patients needs to be performed to get data on network performance and reliability.

Support for Implanted Devices: The network can currently only support medi-

cal devices on the body, which are usually sensors. However, a large number of medical devices are actuators, like deep-brain stimulators or cardiac pacemakers, and are implanted in the patient's body. Network architectures and access schemes need to be investigated to extend support to such implanted devices in conjunction with on-body sensors.

Standardization: Currently-existing BAN standards support far-field wireless and body-coupled communication PHYs. A effort to standardize wearable fabric BANs needs to be undertaken with active support from academia and industry in order to pave the way for commercialization and widespread use.

Appendix A

List of Abbreviations

ACK: Acknowledgement

ADC: Analog-Digital Converter

AFE: Analog Front-End

ARQ: Automatic Repeat Request

ASK: Amplitude-Shift Keying

BAN: Body Area Network

BCC: Body-Coupled Communication

CA: Contention Access

CCITT: Comité Consultatif International Téléphonique et Télégraphique (International Telegraph and Telephone Consultative Committee)

CDMA: Code-Division Multiple Access

CDR: Clock-Data Recovery

CP: Charge Pump

CRC: Cyclic Redundancy Check

CSMA: Carrier-Sense Multiple Access

DLL: Data Link Layer

ECG: Electro-cardiogram

EEG: Electro-encephalogram

EMG: Electro-myogram

FBAN: Fabric Body Area Network

FD: Frequency Detector

FDMA: Frequency-Division Multiple Access

FLL: Frequency-Locked Loop

FSK: Frequency-Shift Keying

HBC: Human Body Communication

ISM: Industrial, Scientific and Medical

LF: Loop Filter

MAC: Medium-Access Control

NRZ: Non-Return-to-Zero

OOK: On-Off Keying

OQPSK: Offset-Quadrature Phase-Shift Keying

OSI: Open Systems Interconnection

PA: Power Amplifier

PAN: Personal Area Network

PD: Phase Detector

PHY: Physical Layer

PLL: Phase-Locked Loop

PRBS: Pseudorandom Bit Sequence

PSK: Phase-Shift Keying

PWM: Pulse-Width Modulation

QoS: Quality of Service

RZ: Return-to-Zero

SoC: System-on-Chip

TDMA: Time-Division Multiple Access

TQFP: Thin Quad Flat Pack

UWB: Ultra-Wideband

VCO: Voltage-Controlled Oscillator

WBAN: Wireless Body Area Network

WSN: Wireless Sensor Network

Appendix B

Resonant Power Transfer Analysis

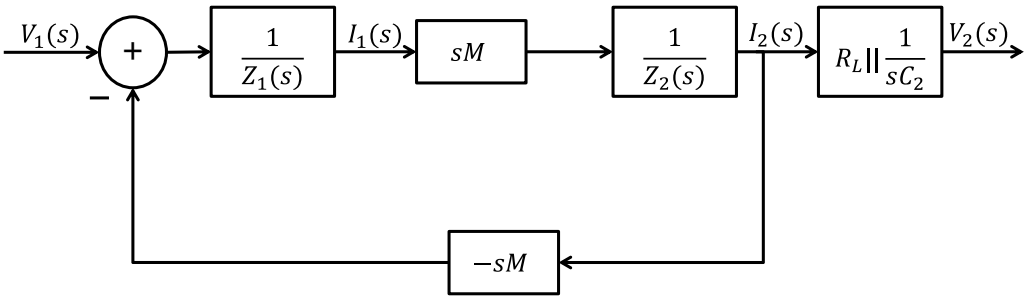


Figure B-1: Block Diagram of Resonant Inductive Power Transfer [29]

Figure B-1 shows a block diagram of the resonant inductive power transfer scheme. The coupling coefficient of the link k is defined as $k = \frac{M}{\sqrt{L_1 L_2}}$. The loop gain of the feedback system is

$$L(s) = \frac{s^2 M^2}{Z_1(s) Z_2(s)} \tag{B.1}$$

where Z_1 is the total impedance of the inductor. The current flowing into the inductor I_1 is

$$I_1(s) = \frac{V_1(s)}{Z_1(s)} . \frac{1}{1 - L(s)} . \tag{B.2}$$

The impedance seen by a voltage source V_1 across the tank $Z_{tank}(s)$ is

$$\begin{aligned} Z_{tank}(s) &= Z_1(s).\left[1 - L(s)\right] || \left(sC_1\right)^{-1} && \text{(B.3)} \\ &= Z_1(s).\left(1 - \frac{s^2M^2}{Z_1(s)Z_2(s)}\right) || \left(sC_1\right)^{-1} && \text{(B.4)} \\ &= \left(Z_1(s) - \frac{s^2M^2}{Z_2(s)}\right) || \left(sC_1\right)^{-1} && \text{(B.5)} \\ &= \left(Z_1(s) - Z_{rfl}(s)\right) || \left(sC_1\right)^{-1} && \text{(B.6)} \end{aligned}$$

where

$$Z_{rfl}(s) = \frac{s^2M^2}{Z_2(s)}. \tag{B.7}$$

$Z_{rfl}(s)$ in Equation B.7 is the reflected impedance of the secondary seen by the primary. Around the resonant frequency $\omega_0 = \left(\sqrt{L_1C_1}\right)^{-1} = \left(\sqrt{L_2C_2}\right)^{-1}$, the parallel load resistance at the secondary R_L can be approximately transformed to a series resistance using the well-known expression

$$R_{L,srs} = \frac{R_L}{Q_L^2 + 1} \tag{B.8}$$

where $Q_L = \omega_0 C_2 R_L$ is the quality factor of the load. At resonance, the reflected impedance is real and is given by

$$\begin{aligned} Z_{rfl}(j\omega_0) &= \frac{-\omega_0^2M^2}{R_2 + R_{L,srs}} && \text{(B.9)} \\ &= -\frac{k^2\omega_0^2L_1L_2}{R_2 + R_{L,srs}} && \text{(B.10)} \\ &= -k^2\omega_0L_1Q_2' && \text{(B.11)} \end{aligned}$$

where Q_2', the loaded quality factor of the secondary, is defined as

$$\begin{aligned} Q_2' &= \frac{\omega_0L_2}{R_2 + R_{L,srs}} && \text{(B.12)} \\ &= \frac{Q_2Q_L}{Q_2 + Q_L} && \text{(B.13)} \end{aligned}$$

. Under resonance, the real part of $Z_1(j\omega_0)$ is

$$Re\left[Z_1(j\omega_0)\right] = R_1\left(1 + k^2 Q_1 Q_2\prime\right) \tag{B.14}$$

Converting this resistance in series with the inductor into a parallel resistance across the tank, the power transfer efficiency of the primary is

$$\eta_1 = \frac{Q_1'^2 R_1\left(1 + k^2 Q_1 Q_2'\right)}{R_s + Q_1'^2 R_1\left(1 + k^2 Q_1 Q_2'\right)} \cdot \frac{k^2 Q_1 Q_2'}{1 + k^2 Q_1 Q_2'}. \tag{B.15}$$

Q_1' is the loaded quality factor of the primary, calculated using Equation B.14. The power transfer efficiency of the secondary is

$$\begin{aligned}
\eta_2 &= \frac{R_{L,srs}}{R_2 + R_{L,srs}} && \text{(B.16)}\\
&= \frac{\omega_0 C_2 R_{L,srs}}{\omega_0 C_2 R_2 + \omega_0 C_2 R_{L,srs}} && \text{(B.17)}\\
&= \frac{Q_L^{-1}}{Q_2^{-1} + Q_L^{-1}} && \text{(B.18)}\\
&= \frac{Q_2}{Q_2 + Q_L}. && \text{(B.19)}
\end{aligned}$$

The net power transfer efficiency of the link is the product of the two individual efficiency values.

Appendix C

Common Network Access Schemes

Contention Access (CA): Also known as the ALOHA protocol, this scheme allows nodes to transmit data whenever it is available, and allows for re-transmission in case of collision. Suitable for networks with low transmit-duty cycle nodes, which leads to lesser collision probability.

Carrier-Sense Multiple Access (CSMA): Modification of CA, wherein a node first "senses" the common network channel for a fixed amount of time for any transmission that is under progress, and starts transmitting if none is found. Reduces collision rate but increases complexity for star-topology networks.

Time-Division Multiple Access (TDMA): Each node transmits only in a fixed timeslot assigned to it. Suitable for networks with repeatable traffic patterns.

Frequency-Division Multiple Access (FDMA): Simulaneous data streams at different frequencies. Not preferred for low-power applications due to additional complexity at the transmitter and receiver.

Code-Division Multiple Access (CDMA): Simultaneous data streams modulated on orthogonal vectors ("codes"). Also not suited for low-power applications due to increased computational complexity.

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