Study of Organic Molecules and Nano-Particle/Polymer Composites for Flash Memory and Switch Applications

by

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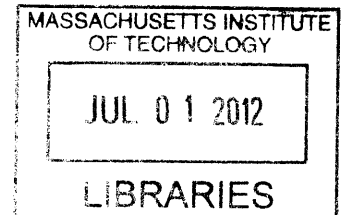
Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy in Electrical Engineering

at the

Massachusetts Institute of Technology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Abstract

Organic materials exhibit fascinating optical and electronic properties which motivate their hybridization with traditional silicon-based electronics in order to achieve novel functionalities and address scaling challenges of these devices. The application of organic molecules and nano-particle/polymer composites for flash memory and switch applications is studied in this dissertation.

Facilitating data storage on individual small molecules as the approach the limits in miniaturization for ultra-high density and low power consumption media may enable orders of magnitude increase in data storage capabilities. A floating gate consisting of a thin film of molecules would provide the advantage of a uniform set of identical nano-structured charge storage elements with high molecular area densities which can result in a several-fold higher density of charge-storage sites as compared to quantum dot (QD) memory and even SONOS devices. Additionally, the discrete charge storage in such nano-segmented floating gate designs limits the impact of any tunnel oxide defects to the charge stored in the proximity of the defect site. The charge retention properties of molecular films was investigated in this dissertation by injecting charges via a biased conductive atomic force microscopy (AFM) tip into molecules comprising the thin films. The Kelvin force microscopy (KFM) results revealed minimal changes in the spatial extent of the charge trapping over time after initial injection. Fabricated memory capacitors show a device durability over 10^5 program/erase cycles and hysteresis window of up to 12.8 V, corresponding to stored charge densities as high as 5.4×10^{13} cm^{-2}, suggesting the potential use of organic molecules in high storage capacity memory cells. Also, these results demonstrate that charge storage properties of the molecular trapping layer can be engineered by rearranging molecules and their π-orbital overlaps via addition of dopant molecules.

Finally, the design, fabrication, testing and evaluation of a MEMS switch that employs viscoelastic organic polymers doped with nano-particles as the active material is presented in this dissertation. The conductivity of the nano-composite changes 10,000-fold as it is mechanically compressed. In this demonstration the compressive squeeze is applied with electric actuation. Since squeezing initiates the switching behavior, the device is referred to as a "squitch". The squitch is essentially a new type of FET that is compatible with large area processing with printing or photolithography, on rigid or flexible substrates and can exhibit large on-to-off conduction ratio.

Thesis Supervisor: Vladimir Bulović
Title: Professor of Electrical Engineering

To my mother, a truly caring and loving soul. Her support, personal sacrifices, encouragement, and constant love have sustained me throughout my life.

To my dear father, who has been my role-model for hard work and persistence, who has been proud of my work and has been supportive throughout my life.

To Shahriyar, my dear and loving husband, who instilled in me the inspiration to set high goals and the confidence to achieve them, and who has shared the many uncertainties, challenges and sacrifices for completing this dissertation.

Acknowledgments

This work would not have been possible without the support of many talented people and organizations.

First of all, I would like to thank my research supervisor, Prof. Vladimir Bulovic for all his guidance, encouragement, support, and patience throughout the completion of this dissertation. I feel very fortunate for the opportunity to have him as my research advisor.

I'm infinitely grateful to my dissertation committee members, Prof. Jeffery H. Lang and Prof. Judy L. Hoyt for their very helpful insights, comments and suggestions. I would also like to thank Prof. Dimitri Antoniadis for his thoughtful comments.

I am thankful to my fellow lab members past and present who have taught me so much. It was a pleasure to work in such a friendly, multi-cultural working environment. Specifically, I would like to thank Dr. Pouya Hashemi for all his help and for being a good friend for me; Dr. Katherine Aidala, Dr. Timothy P. Osedach, Patrick Brown, Dr. Ivan Nausieda, Dr. Polina Anikeeva, Dr. Osama Nayfeh, Hassen Abdu, Dr. Corinne Packard, Dr. Elizabeth Young, Dr. Alexi Arango, Yasu Shirasaki, Geoffrey Supran, Dr. Trisha Andrew, Apoorva Murarka, Jill Rowehl, Dr. Annie Wang, Farnaz Niroui, Dr. Burag Yaglioglu, Dr. Matt Panzer, Gleb Akselrod and everyone else in the Laboratory of Organic and Nanostructured Electronics (ONE lab).

Additionally, I would like to acknowledge the staff at MIT Microsystems Technology Laboratories for their technical support and assistance including Vicky Diadiuk, Paul Tierney, Bernard Alamariu, Eric S. Lim, Robert Bicchieri, Donal Jamieson, Paudely Zamora, Kurt Broderick, and Dennis Ward.

I am also thankful to the staffs at Department of Material Science and Engineering of MIT specially Dr. Yong Zhang, for training me on TEM and spending long hours helping me with sample preparation and TEM imaging. I would also like to express my gratitude to Mrs. Monica Pegis. She has always ensured that all the administrative hurdles were handled in time.

I am enormously grateful to my family. I am forever indebted to my parents for their understanding, endless love, patience and support. I'm truly thankful to my brother, Navid, a passionate learner, in whose footsteps I follow as an educational leader, for his invaluable guidance and for his psychological, and intellectual support and to my dear sisters, Fahimeh, Naeemeh and Maryam who have been my emotional anchors through not only the vagaries of graduate school, but my entire life.

I would like to express my sincere and very special gratitude to my husband, Shahriyar, for his unconditional love and constant support.

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Chapter 1

Dissertation Motivation and Outline

The future of computing lies in small and low-power solutions coupled with cloud services. Smartphones are becoming personal computers, powerful enough to run simple desktop computing environments. Tablets are cannibalizing laptops. Even entire home entertainment experiences are being jammed into tiny set-top boxes and embedded into televisions. For many decades, silicon based electronics have been successfully scaled down in size and cost while at the same time achieving higher speed with higher density devices. However, these technologies have recently started to expose their lower limits and have resisted the creation of higher density products.

Organic electronics is an active area of research due to its application in the low-cost manufacture of lightweight, large-area electronic devices and solar cells [1-3]. Molecules and polymers exhibit fascinating optical and electronic properties [4-9]. Researchers have discovered that they can be tailored for specific properties and are compatible with inorganic materials - a significant finding that has encouraged their hybridization with traditional silicon based electronics in order to achieve novel functionalities.

They can be tailored for specific properties and are compatible with inorganic materials that motivate their hybridization with traditional silicon based electronics in order to achieve novel functionalities.

This dissertation is mainly focused on charge storage properties of small organic molecules for potential application in flash memories. In addition, it addresses viscoelastic organic polymers doped with nano-particles as the active element in squishable electronically-controlled switches.

1-1 Molecular charge storage elements

Conventional flash memory technology stores charges in the floating gate of individual memory cells, with the floating gate sandwiched between the gate oxide and the tunneling oxide of each cell [10, 11]. Technological advancements have led to a reduction in the lateral size (and increase in the areal density) of flash memory cells, with an associated decrease in the thickness of the tunneling oxide layer. The tunneling oxide is responsible for retaining the charge in the floating gate for more than 10 years, but reductions in the tunneling oxide thickness and presence of intrinsic defects in the oxide can lead to poor charge retention, limiting the ability for continued scaling of conventional flash memories. The number of electrons stored in the floating gate decreases with each new technology node while the defect-related charge leakage increases, with the consequence that oxide defects have an increasing impact on the cell operation as the size of memory cells is reduced [12, 13].

One technological solution that can enable continued scaling of flash memory cells is to replace the conventional polysilicon floating gate by an array of segmented charge storage elements such as quantum dots (QDs) [14-16], molecules [17-21] and dielectric traps, as has been done for the SONOS flash memory technology [16, 22 ,23] . The discrete charge storage in such a nano-segmented floating gate inhibits charge transport between the nano-segments, limiting the impact of any one tunnel oxide defect to the charge stored in the proximity of the defect site. Charge stored in the remaining segments of the nano-segmented floating gate would remain unaffected. One challenge with this approach is that the array of discrete charge-storage segments may cumulatively store a smaller number of electrons than a continuous floating gate of same dimensions. The self-charging energy of individual nano-segments could limit the number of charges stored on each to one electron. In addition, spatial density of nano-segments may have to be small to maintain sufficient spacing between the segments and inhibit charge transport between them, as otherwise charge tunneling between the segments would obviate the intended benefit of nano-structuring the floating gate to preserve the charge on individual segments. Therefore, the benefit of nano-segmenting the floating gate will be manifested only if high charge storage capability can be maintained.

Unfortunately, semiconductor nanocrystal/QDs memories may not be the ultimate solution to flash memory scaling, although it is a novel memory structure that still attracts a lot of attention now [14, 16]. It is hard to control the uniformity of the nanocrystals' size and their physical locations in the channel. It is not a surprise that nanocrystal memories exhibit large device-to-device variation. Also, in order to have a negligible lateral tunneling between the nanocrystals, the spacing between nanocrystals should be greater than 5 nm that limits the maximum stored charge density in this kind of memories.

Charge storage in dielectric traps is also vulnerable to trap density and energy variations. In comparison, a combination of the top-down lithography and the bottom-up molecule self-assembly processes can offer a uniform charge density and possible stable multilevel storage in a single memory cell [17, 24, 25]. The monodisperse nature of the molecular orbitals (MOs) can potentially reduce cell variations, whereas the distinct energy levels may enable stepwise charging for precise control of each memory state.

Although organic compounds have recently attracted growing interest for nonvolatile memory applications, many of the devices reported so far are two-terminal resistive memories, rather than reversible charge-storage elements [19-21]. Memory behavior of a series of molecular thin films embedded in metal-oxide-semiconductor (MOS) structures was investigated in this dissertation.

A floating gate consisting of a thin film of molecules would provide the advantage of a uniform set of identical nanostructured charge storage elements, with low density of states and high binding energy that results in low intermolecular interactions. The minimal overlap between the neighboring molecular electron wavefunctions contributes to organic thin film electron/hole mobilities in the range of 10^{-1} $cm^2V^{-1}s^{-1}$ to 10^{-7} $cm^2V^{-1}s^{-1}$. Compared to QDs which typically exhibit size and order variability, molecular films have the highly desirable size and morphological consistency that provides relative constancy in the electronic energy level structure of molecular films.

1-2 MEMS Switches Employing Active Metal-Polymer Nano-Composites

For decades much research has been directed towards utilizing the piezoresistive properties of polymer materials doped with conductive particles in developing a broad range of devices from tactile sensors to fuses [26-29]. These composite materials in general can be fabricated such that they act as poor conductors but exhibit an increased electrical conduction due to tunneling between particles. This property of conductive composites is employed in this disssertation to develop an electrostatically actuated squishable switch or "squitch" which functions as a gated transistor.

Some advantages of this MEMS switch are that: (1) it is an aditive technology compatible with large area processing with printing or photolithography on rigid or flexible substrates; (2) it can exhibit large on-to-off conduction ratio of 10^7:1; (3) it can exhibit voltage-controlled conduction with a gain greater than 1 decade per 60 mV - a fundamental limit for silicon-based semiconductor switches; and (4) its contacts are not subject to the usual wear associated with point-contact electromechanical switches.

This low-loss squishable MEMS switch can be used for power management of digital IC's. Lowering power consumption in digital IC's is becoming increasingly important in order to increase mobile device battery life and to decrease cooling costs for enterprise server farms. Power gating of digital logic using MEM relays may provide significant power savings over conventional MOS power gating [30].

The squitch can also be used as the integrated electronics in sensory skins for signal processing and the local amplification of sensor signals. The lightweight and flexible sensory skins are capable of recording external pressure, sound waves, liquid flow, or changes in temperature or chemical environment.

Formed as an array of integrated detectors embedded in a flexible matrix, sensory skins will enable phased-array detection for directional location of external stimuli. The squitch can be used to construct analog and digital circuitry that can then process the signals produced by the sensors. The objective is to develop environmentally responsive sensory skins that both probe

their environment and process the sensed signals, mimicking the capabilities of living skins that possess both sensory cells and a signal-processing “nervous system". ". Such skins may enable the development of devices like sensors that can measure the stresses and strains in parachute fabrics, large-scale “listening” devices that can be unobtrusive, wearable sensors of the battlefield environment for soldier protection and wearable sensors that can monitor soldier health.

1.2 Dissertation Outline

The structure and operational basics of conventional flash memories are discussed in Chapter 2.

The background physics and methods incorporated in the next chapters will be briefly described to facilitate the understanding of the rest of this dissertation. After an introduction of the general scaling requirement, charge storage on segmented floating gates as a solution for scaling limits are proposed. Finally, challenges and essential properties of the segmented floating gate are briefly discussed.

In chapter 3, new kind of memories with molecular floating gate is introduced. Charge-storage behavior in a series of molecular thin films was investigated using MOS structures with SiO_2 and Al_2O_3 as the tunneling and control oxides, respectively. It was shown that molecular floating gates can reach record-high densities of 5.4×10^{13} cm^{-2} and durability over 10^5 charging/discharging cycles.

In chapter 4, retention and diffusion of charge in tris(8-hydroxyquinoline) aluminum (Alq_3) and C_{60} molecular thin films were visualized and investigated using Kelvin force microscopy. Chapter 5 presents molecular memories with increased storage capacity. It was demonstrated that charge storage properties of the molecular trapping layer can be engineered by rearranging molecules and their π-orbital overlaps via addition of dopant molecules. Chapter 6 presents the design, fabrication, testing and evaluation of a MEMS switch that employs viscoelastic organic polymers doped with nano-particles as its active material. This switch is a new type of FET that is compatible with large area processing with printing or photolithography, on rigid or flexible substrates and can exhibit large on-to-off conduction ratio.

Finally chapter 7 summarizes and concludes the dissertation and offers suggestions for future work to further enhance the performance of the memory and switches fabricated by using organic molecules and polymers.

Chapter 2

Introduction to Flash Memory

2.1 Memory Industry and Applications

Complementary metal-oxide-semiconductor (CMOS) memories can be divided into two main categories: volatile memories that lose stored information once the power supply is switched off, and nonvolatile memories that keep stored information also when the power supply is switched off. In the past decade, memory chips with low power consumption and low cost have attracted more and more attention due to the booming market of portable electronic devices such as cellular phones and digital cameras. These applications require the memory to have ten years data retention time, so that the nonvolatile memory device has become indispensable. There are mainly four types of nonvolatile memory technology: flash memory, Ferro-electric Random Access Memory (FeRAM), Magnetic Random Access Memory (MRAM) and phase change memory. Flash memory is presently the most suitable choice for nonvolatile applications [16]. The continuous-film polysilicon-based floating-gate device has been the backbone of the nonvolatile memory (flash) market for the past decade.

The flash memory business flourished when the memory was adopted as the standard memory in cell phones, in which the memory enabled just-in-time loading of the latest program code as the last step in manufacturing, and program bugs could be fixed without taking the phone apart.

The simplicity of its device fabrication process is evident. Flash memory fabrication process is compatible with the current CMOS process and is a suitable solution for embedded memory applications.

A flash memory cell is simply a MOSFET cell, except that a poly-silicon floating gate (or Silicon Nitride charge trap layer) is sandwiched between a tunnel oxide and an inter-poly oxide to form a charge storage layer. All other nonvolatile memories require integration of new materials that are not as compatible with a conventional CMOS process. It is easier and more reliable to integrate flash memory than other nonvolatile memories with logic and analog devices in order to achieve better chip performance for wireless communication and wireless computation.

Flash memory can achieve the highest chip density since flash memory cell consists of only one transistor. A FeRAM memory cell generally consists of one transistor and one capacitor [31], while a MRAM cell needs a transistor and a magnetic tunnel junction [32]. Phase change memory was expected to be a promising nonvolatile memory; however, its memory cell consists of one resistor and a bipolar junction transistor [33]. In addition, Flash memory possesses the multi-bit per cell storage property [34]. Four distinct threshold voltage (V_T) states can be achieved in a flash memory cell by controlling the amount of charge stored in its floating gate [10, 16].

However, after years of intense growth in the Flash memory market, conventional flash memory technology appears to be reaching fundamental scaling limits [10, 12, 13]. The difficulty in scaling the tunnel oxide thickness due to leakage-current-related charge loss, reduction in gate coupling, and increase in cell-to-cell interference, necessitate modification in the design of the flash memory structures, including proposals for replacing the polysilicon floating gate by either floating traps such as silicon nitride in the SONOS technology [16, 22, 23] or floating quantum dots (QD) [14, 16]

2.2 Flash Memory Structure

To have a memory cell that can commute from one state to the other and that can store the information independently of external conditions, the storing element needs to be a device whose conductivity can be changed in a nondestructive way.

One solution is to have a transistor with a threshold voltage that can change repetitively from a high to a low state, corresponding to the two states of the memory cell, i.e., the binary values

("1" and "0") of the stored bit. Cells can be "written" into either state "1" or "0" by either "programming" or "erasing" methods. One of the two states is called "programmed," the other "erased."

The threshold voltage of a MOS transistor can be written as [10]

$$V_T = K - \bar{Q}/C_{ox} \tag{2.1}$$

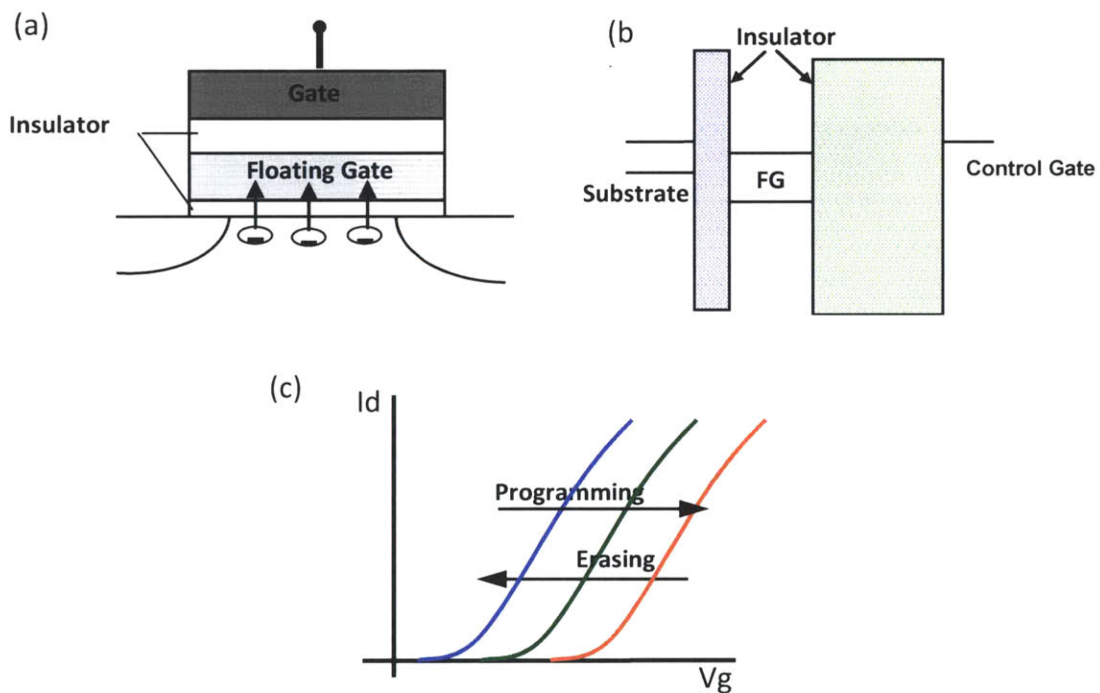


Figure 2-1: (a) Schematic cross section of conventional flash memory; (b) Flash memory energy band diagram; (c) Threshold voltage shift during programming and erasing.

where K is a constant that depends on the gate and substrate material, doping, and gate oxide thickness, $\bar{Q}$ is the charge weighted with respect to its position in the gate oxide, and C_{ox} is the gate oxide capacitance. As can be seen, the threshold voltage of the memory cell can be altered by changing the amount of charge present between the gate and the channel. There are many ways to obtain the threshold voltage shift. Two are the most common solutions used to store charge:

In a conductive material layer between the gate and the channel and completely surrounded by insulator. This is the floating gate (FG) device.

In traps that are present in the oxide, more precisely at the interface between two dielectric materials. The most commonly used interface is the silicon oxide/nitride interface. Devices obtained in this way are called metal-nitride-oxide-silicon (MNOS) cells.

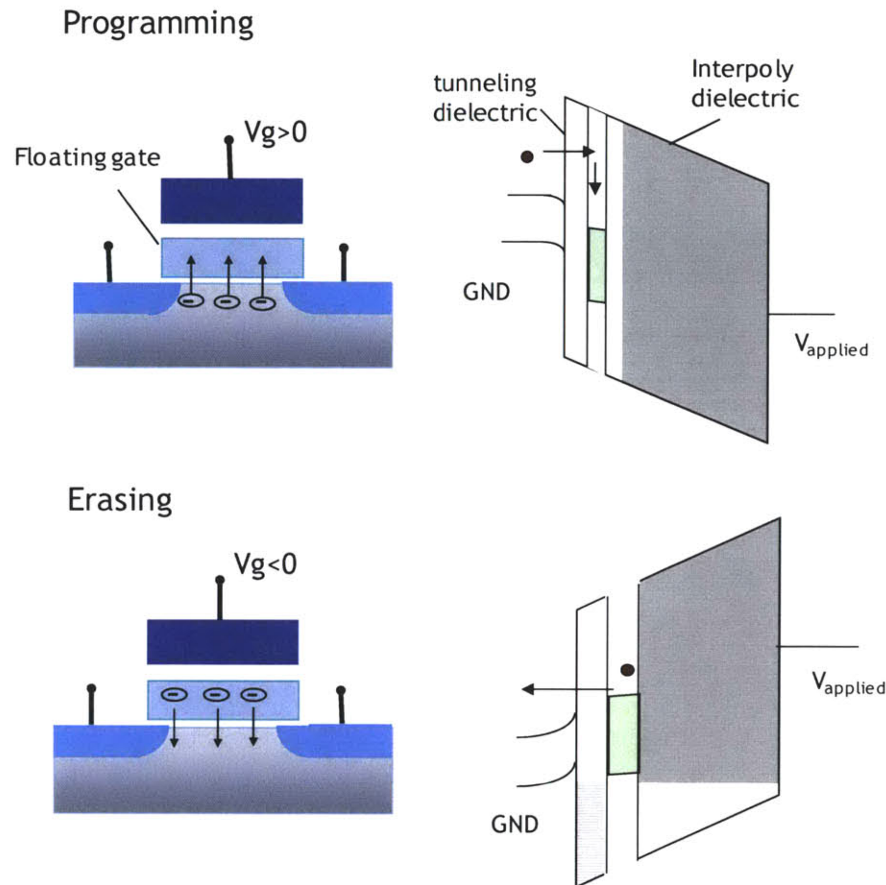


Figure 2-2: Schematic cross section and energy band diagram of conventional flash memory during programming and erasing.

The schematic cross section of a generic FG device is shown in Figure 2-1(a); the upper gate is the control gate (CG) and the lower gate, completely isolated within the gate dielectric, is the FG. The FG acts as a potential well (see Figure 2-1(b)). If a charge is forced into the well, it cannot move from there without applying an external force: the FG stores charge [1]. Usually the gate dielectric, i.e., the one between the transistor channel and the FG, is an oxide in the range of 9–10 nm and is called "tunnel oxide" since electron tunneling occurs through it. The dielectric

that separates the FG from the CG is formed by a triple layer of oxide–nitride–oxide (ONO). The ONO thickness is in the range of 15–20 nm of equivalent oxide thickness. The ONO layer as interpoly dielectric has been introduced in order to improve the tunnel oxide quality.

Stored charges on the floating-gate alter the threshold voltage of the MOSFET. The amount of charge stored on the floating gate can be controlled with biasing the terminal electrodes with voltages sufficient enough to cause tunneling of carriers in the gate-insulator from either the channel or the gate. These charges can tunnel through the gate insulator and be trapped/stored on the floating gate (programming), therefore causing a shift in the threshold voltage of the device. Appropriate biasing of the device can also be performed to cause removal of the charges that are stored on the floating gate (erasing), and to return the threshold voltage to the original uncharged state (Figure 2-2).

The data stored in a Flash cell can be determined measuring the threshold voltage of the FG MOS transistor by reading the current driven by the cell at a fixed gate bias.

2.3 Types of Flash Memory

Two major forms of Flash memory, NAND Flash and NOR Flash, have emerged as the dominant varieties of non-volatile semiconductor memories utilized in portable electronics devices. NAND Flash, which was designed with a very small cell size to enable a low cost-per-bit of stored data, has been used primarily as a high-density data storage medium for consumer devices such as digital still cameras and USB solid-state disk drives. NOR Flash has typically been used for code storage and direct execution in portable electronics devices, such as cellular phones and PDAs.

In NOR flash memory, each cell resembles a standard MOSFET, except that the cell has two gates, stacked vertically, instead of just one. Each NOR memory cell is connected to the common drain connection called a bitline and can be read from directly giving the fast read performance that is necessary for fast program execution. In order to decrease the cost of flash memory, NAND flash memory (Figure 2-3) was invented [12, 35].

In NAND flash memory, the memory cells are connected in series with 16 or 32 memory cells connected to the bitline and source line through two select transistors. [In Figure 2-3, the source

line is connected to the ground through SG(S).] Because cell contact area represents about 30% of unit cell area, this serial cell approach gives smaller cell size and lower die cost compared to NOR memory. The tradeoff is slower read performance because the read current is lower when using serial transistors. The NAND memory business flourished with the growth in popularity of digital cameras, for which NAND memory cards provided a convenient low-cost media for

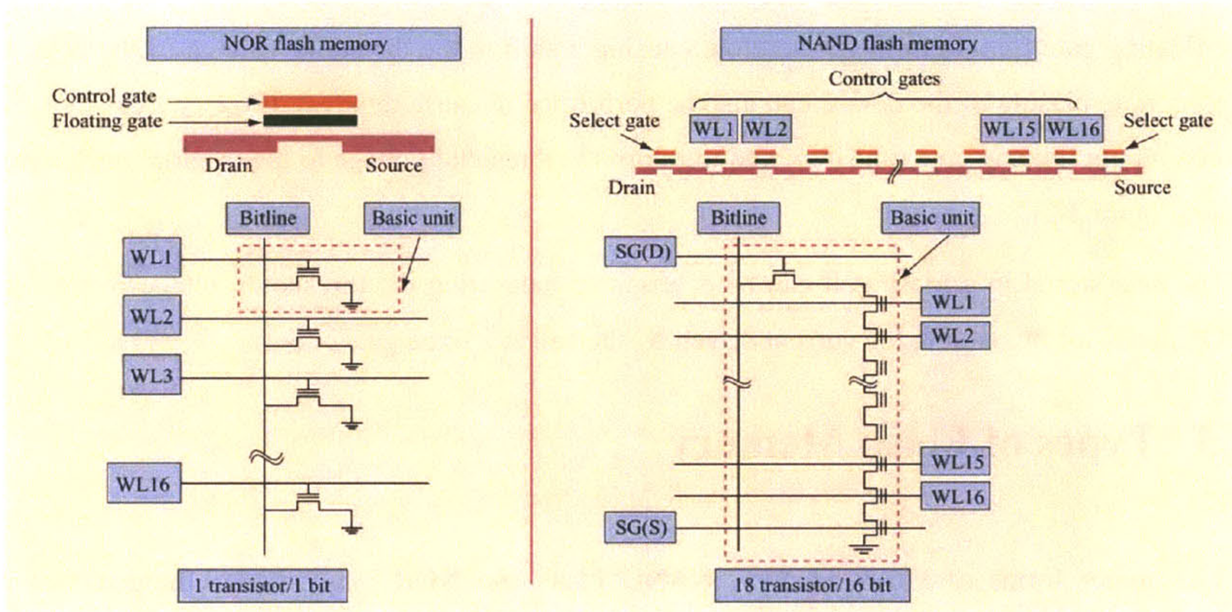


Figure 2-3: Schematic cross-sections and circuit diagrams for NOR and NAND flash memory. In NOR memory, the basic unit is one memory transistor. For NAND memory, the basic unit is 16 memory and 2 select transistors [12]. (WL: wordline; SG(D): select gate drain; SG(S): select gate source)

picture storage. The slow read speed is not an issue for such applications. This application was followed by the ubiquitous USB (Universal Serial Bus) drives and MP3 (MPEG-1 Audio Layer 3) players. An emerging new application that will drive more growth for NAND memory is solid-state disks to replace disk drives in notebook computers. The growth of flash memory over the years was driven by the relentless memory cost reduction through Moore's Law; the price for flash memory dropped from approximately $80,000 per gigabyte in 1987 for NOR flash to approximately $10 per gigabyte in 2007 for NAND flash.

2.4 Program and erase mechanisms

There are two main mechanisms by which charge carriers can charge and discharge the floating gate: Hot-Electron Injection and Fowler-Nordheim tunneling.

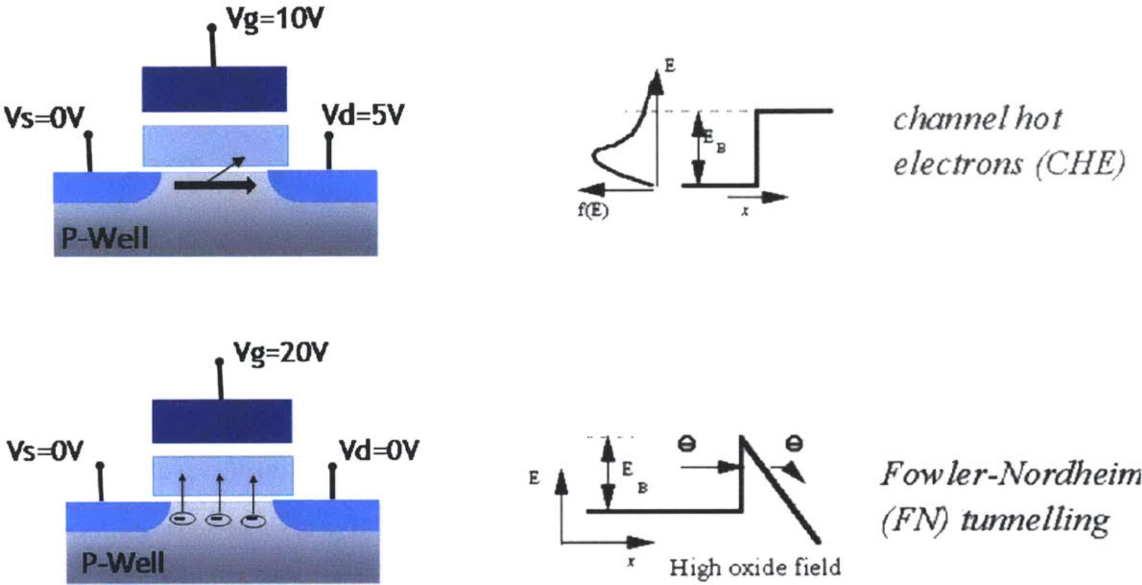


Figure 2-4: Writing mechanism in floating-gate devices [11, 36].

2.4.1 Hot-Electron Injection

Hot-Electron Injection is a phenomenon by which a charge carrier in the channel gains energy from the lateral electric field, and then crosses the oxide energy barrier into the floating gate by experiencing a vertical electric field between the control gate and substrate.

An electron traveling from the source to the drain gains energy from the lateral electric field and loses energy to the lattice vibrations (acoustic and optical phonons). At low fields, this is a dynamic equilibrium condition, which holds until the field strength reaches approximately 100 kV/cm [10, 11]. For fields exceeding this value, electrons are no longer in equilibrium with the lattice, and their energy relative to the conduction band edge begins to increase. Electrons are

"heated" by the high lateral electric field, and a small fraction of them have enough energy to surmount the barrier between oxide and silicon conduction band edges. For an electron to overcome this potential barrier, three conditions must hold.

1) Its kinetic energy has to be higher than the potential barrier.
2) It must be directed toward the barrier; and
3) The field in the oxide should be collecting it.

In general terms, the electron current density from Si to SiO_2 at a point x along the channel of a MOSFET can be analytically expressed as [11]:

$$J = q \int_0^{\infty} v_{\perp} (x, E) f_{\perp}(x, E) g(E) P(x, E) dE) \tag{2.2}$$

where $f_{\perp}(x, E)$ is the distribution of electrons that hit the interface between x and $x+dx$; g is the number of available electron states; $P(x,E)$ is the injection probability; and $v_{\perp}(x, E)$ is the electron velocity component perpendicular to the interface and directed towards it. The injected current is the combined result of a few factors: (1) the number ($f_{\perp}.g$) and velocity ($v_{\perp}$) of electrons directed towards the interface; (2) the electron energy and momentum distribution; and (3) the probability of injection from Si to SiO_2 ($P(x,E)$).

2.4.2 Fowler-Nordheim Tunneling

Fowler-Nordheim Tunneling is another mechanism for charge carriers to cross the oxide energy barrier by applying a strong electric field (in the range of 8–10 MV/cm) across a thin oxide. The concept of tunneling is rooted in quantum mechanics. Electrons can penetrate a forbidden region in order to tunnel from one classically allowed region (substrate) to another (floating gate). However, this phenomenon is probabilistic, depending on the source material, and the height and width of the oxide barrier. For this method only single external power supply is needed. The current density of electrons being shown in Figure 2-5 is transmitted through the trapezoidal potential barrier to the polysilicon gate is [37]:

$$J = \frac{2}{(2\pi)^3} \iiint dk_x dk_y\, dk_z v_x(k_x) \times D(E_x(k_x)) f_{eq}(E(k)) \tag{2.3}$$

where

$$E(k) = \frac{\hbar^2 k_x{}^2}{2m} + \frac{\hbar^2 k_y{}^2}{2m} + \frac{\hbar^2 k_z{}^2}{2m} \equiv E_x(k_x) + E_y(k_y) + E_z(k_z) \tag{2.4}$$

is the electron energy; E_x is the associated perpendicular tunneling energy;

$$D(E_x) = \exp\left(-\frac{2}{\hbar}\int_{S_1}^{S_2} dx\sqrt{2m(V(x) - E_x)}\right) \tag{2.5}$$

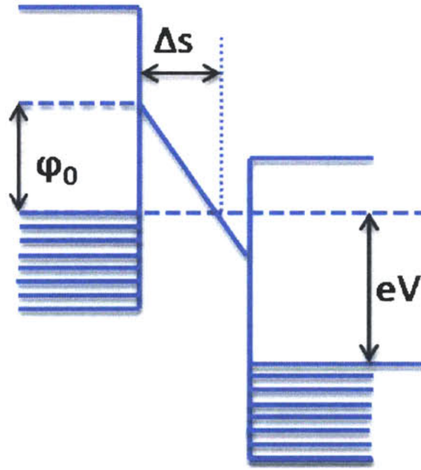


Figure 2-5: Rectangular potential barrier in insulating film between metal electrodes for V> φ_0 /e.

is the transmission probability in the WKB approximation, which depends on the perpendicular tunneling energy E_x; $v_x = \hbar^{-1} dE_x / dk_x$ - the x component of the group velocity; m - the electron mass; and $f_{eq}(E)$ - the equilibrium electron distribution function.

Approximating the Fermi–Dirac distribution with the step function leads for high oxide fields to the Fowler–Nordheim tunneling current [37]

$$J = \frac{2.2e^3F^2}{8\pi h\varphi_0}\exp\left(\frac{-8\pi}{2.96heF}\sqrt{2m}\varphi_0{}^{1.5}\right) \tag{2.6}$$

where φ_0 is the barrier height and F the oxide field. This formula has proved very successful in describing the dependence of the FN tunneling current of *cold* electrons on oxide thickness and gate voltage, in particular for the erase operation in silicon flash memory cells.

A plot of the amount of Fowler-Nordheim tunneling as a function of electric field is shown in Figure 2-6. Though the Fowler-Nordheim tunneling current can be intensified by increasing voltage or decreasing the oxide thickness, the performance and reliability needs must be balanced. The oxide cannot be made too thick as it would significantly increase the voltage and time required for charging the floating gate nor can it be made too thin as it would increase oxide defect density and ruin device reliability. In this dissertation memory behavior of organic molecules were studied using MOS structures. FN tunneling method will be used for programming and erasing the memory cells.

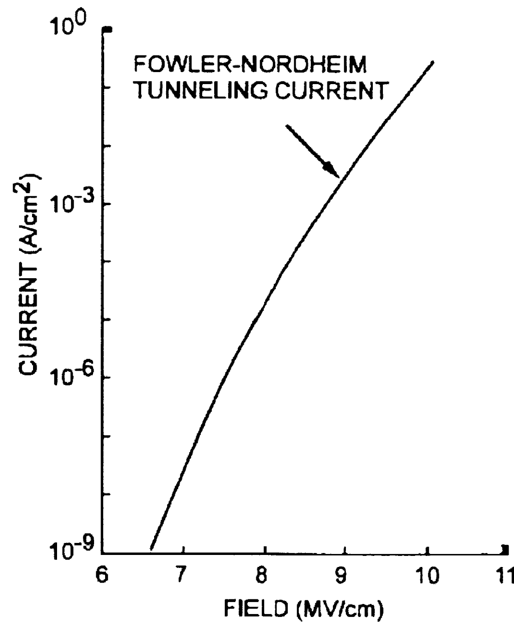


Figure 2-6: FN tunneling current as a function of electric field [10].

2.4.3 Metal Oxide Semiconductor (MOS) Capacitor

The MOS capacitor consists of an oxide film sandwiched between a P- or N-type silicon substrate and a metal plate called gate as shown in Figure 2-7.

The capacitance of the MOS structure depends on the voltage (bias) on the gate. Typically a voltage is applied to the gate while the body is grounded. The dependence is shown in Figure 2 and there are roughly three regimes of operation separated by two voltages. The regimes are described by what is happening to the semiconductor surface. These are (1) *Accumulation* in which mobile carriers of the same type as the body accumulates at the surface [electrons] (2) *Depletion* in which the surface is devoid of any mobile carriers leaving only a space charge or depletion layer, and (3) *Inversion* in which mobile carriers of the opposite type to the body [electrons] aggregate at the surface to "invert" the conductivity type. The two voltages that demarcate the three regimes are (a) Flatband Voltage (V_{FB}) which separates the accumulation regime from the depletion regime and (b) the Threshold Voltage (V_T) which demarcates the depletion regime from the inversion regime.

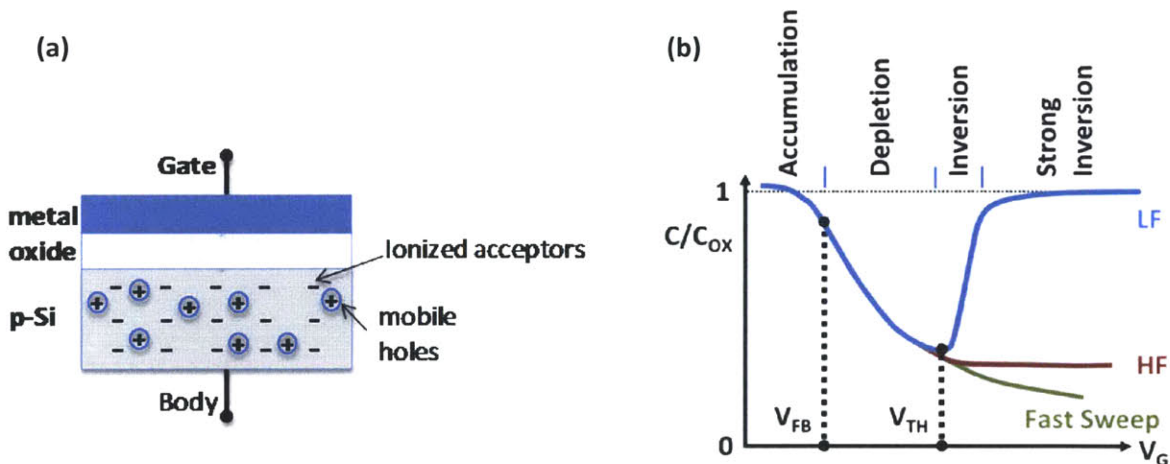


Figure 2-7: (a) The MOS capacitor structure. The substrate (body) is grounded and a voltage V_{GB} is applied to the gate; (b) Capacitance vs. gate voltage (C-V) diagram of a MOS Capacitor. The flatband voltage (V_{FB}) separates the Accumulation region from the Depletion regime. The threshold voltage (V_T) separates the depletion regime from the inversion regime [38].

2.4.3.1 Accumulation

When an external voltage V_G is applied to the silicon surface in MOS capacitor, the carrier densities change accordingly in its surface region. With large negative bias applied to the gate, holes are attracted by the negative charges to form an accumulation layer (Figure 2-8). The high concentration of these holes will form the second electrode of a parallel plate capacitor with first electrode at the gate. Since the accumulation layer is an indirect ohmic contact with the P-type substrate, the capacitance of the structure under accumulation conditions must be approximately equal to the capacitance of the oxide [38],

$$C_{ox} = \frac{\varepsilon_o \varepsilon_{ox}}{t_{ox}} \quad (2\text{-}7)$$

where ε_0 is the permittivity of the free space, ε_{ox} the relative permittivity of oxide, and t_{ox} the oxide thickness. This capacitance is always expressed per unit gate area ($F.cm^{-2}$). It does not vary with bias V_G as long as the structure is maintained in accumulation mode.

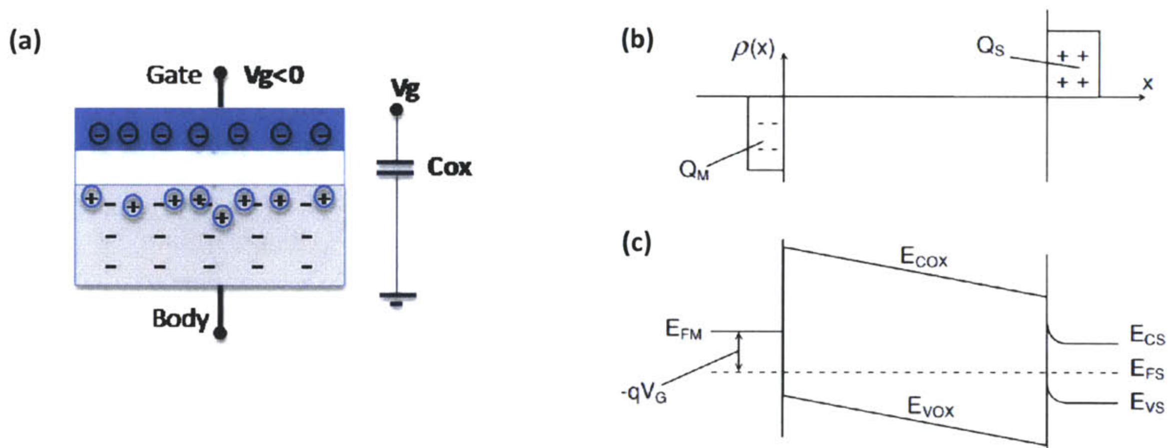


Figure 2-8: Schematic representation of P-MOS structure under bias resulting in accumulation mode, (a) biasing condition, (b) charge distribution, (c) energy band diagram [39].

2.4.3.2 Depletion

When negative charges are removed from the gate, holes leave the accumulation layer until the silicon will be neutral everywhere. This applied gate bias is called the flat band voltage. As the bias on the gate is made more positive with respect to flat band, holes are repelled and a region is formed at the surface which is depleted of carriers (Figure 2.9). Under depletion conditions, the Fermi level near the silicon surface will move to a position closer to the center of the forbidden region as illustrated in Figure 2-9.

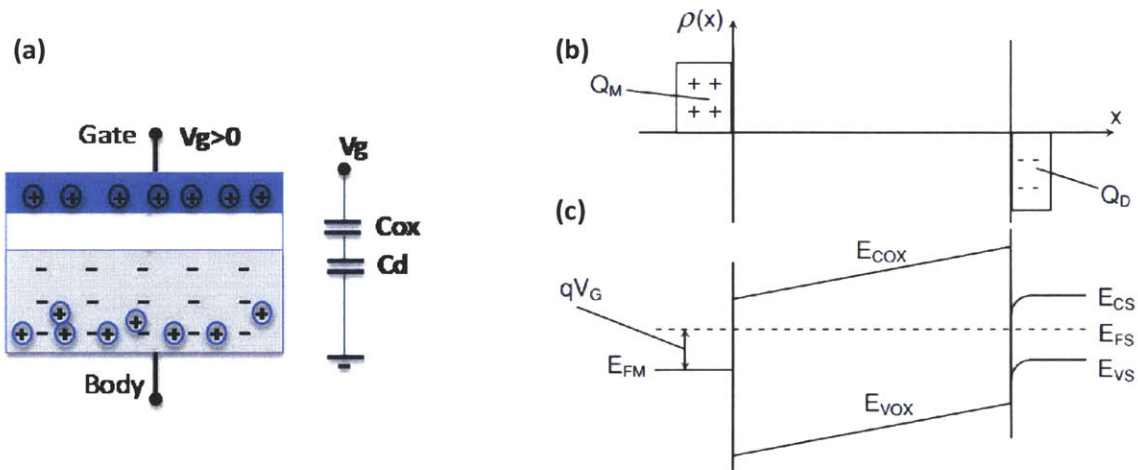


Figure 2-9: Schematic representation of P-MOS structure under bias resulting in depletion mode, (a) biasing condition, (b) charge distribution, (c) energy band diagram.

Increasing the positive voltage V_G will tend to increase the width of the surface depletion region X_D, the capacitance from the gate to the substrate associated with MOS structure will decrease, because the capacitance associated with the surface depletion region will add in series to the capacitance across the oxide. Thus the total capacitance per unit area from the gate to substrate under depletion conditions is given by [39]

$$C(V_G) = \left(\frac{1}{C_{ox}} + \frac{1}{C_S(V_G)}\right)^{-1} \tag{2-8}$$

where C_S is the silicon capacitance per unit area, is given by [39]

$$C_S(V_G) = \frac{\varepsilon_0 \varepsilon_S}{X_D} \tag{2-9}$$

and,

$$X_D = \sqrt{\frac{2\varepsilon_0 \varepsilon_S \psi_S}{qN_A}} \tag{2-10}$$

where the relation between the applied gate voltage V_G and the total band banding ψ_S can be written as [39]

$$V_G = \psi_s + \frac{\sqrt{2\varepsilon_0 \varepsilon_s q N_A \psi_S}}{C_{ox}} \tag{2-11}$$

2.4.3.3 Inversion

With increasingly applying positive voltage, the surface depletion region will continue to widen until the onset of surface inversion is observed (n-type), an inversion layer is formed, the

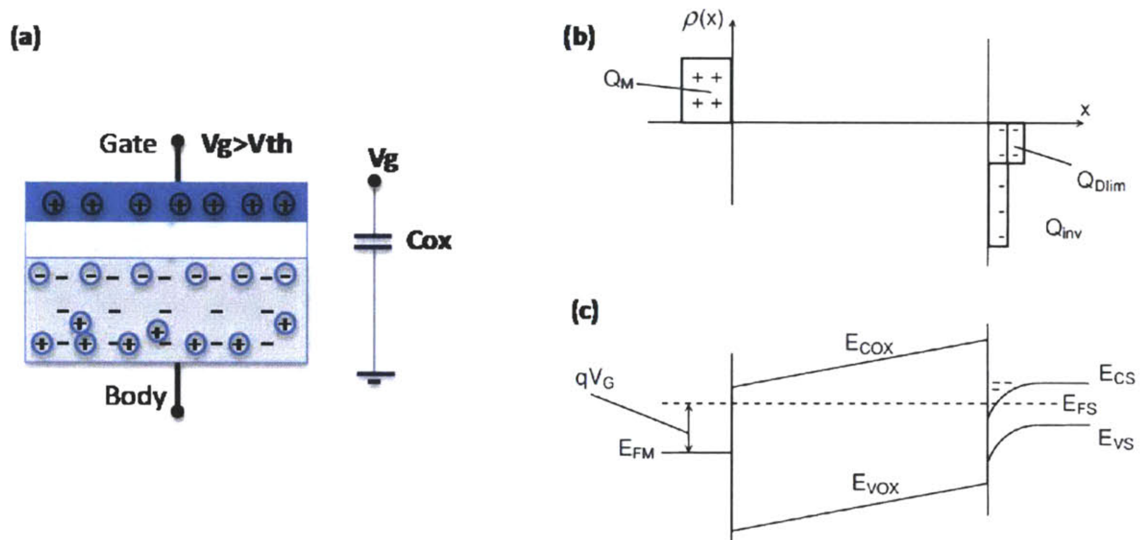


Figure 2-10: Schematic representation of P-MOS structure under bias resulting in inversion mode, (a) biasing condition, (b) charge distribution, (c) energy band diagram [39].

Fermi level near the silicon surface will now lie close to the bottom of conduction band (Figure

2-10). This inversion layer is very thin (1–10 nm) and separated from the bulk of silicon by the depletion layer.

The buildup of inversion layer is a threshold phenomenon. The threshold condition marks the equality of the concentration of minority carriers to the doping concentration.

At the onset of inversion, the depletion layer width reaches a limit, X_{DLim} as shown in Figure 2-10. Since the charge density in the inversion layer may or may not be able to follow the ac variation of the applied gate voltage, it follows that the capacitance under inversion conditions will be a function of frequency.

2.4.3.4 Low frequency Capacitance

This case, illustrated in Figure 2-7, corresponds to the thermal equilibrium in which the increase in the gate charge δQ_M is balanced by the substrate charge δQ_{inv}. It arises when the frequency of the small signal is sufficiently low (typically less than 10 Hz). The low frequency capacitance of the structure, C_{LF}, is equivalent to that of the oxide layer, just as in accumulation mode,

$$C_{LF}=C_{ox} \tag{2-12}$$

2.4.3.5 High Frequency capacitance

In the case of higher frequencies (typically above 10^5 Hz), the increase of charge in the metal side δQ_M is now balanced by the substrate charge δQ_D, since the minority carriers can no longer adjust their concentrations. The charge modulation δQ_D occurs at distance X_{DLim} of the Si–SiO_2 interface. It follows that the high frequency capacitance of the MOS structure, C_{HF}, is given,

$$\frac{1}{C_{HF}} = \frac{1}{C_{ox}} + \frac{1}{C_{Dv\,lim}} \tag{2-13}$$

where

$$C_{D\,lim} = \frac{\varepsilon_0 \varepsilon_S}{X_{D\,lim}} \tag{2-14}$$

and,

$$X_{D\,lim} = \sqrt{\frac{4\varepsilon_0 \varepsilon_S kT Ln(\frac{N_A}{n_i})}{q^2 N_A}} \tag{2-15}$$

In MOS structures, the threshold voltage V_T and the flat band voltage V_{FB} could strongly be affected by any Charges trapped in the oxide. The net result of the presence of any charge in the oxide is to induce a charge of opposite polarity in the underlying silicon. The amount of charge induced will be inversely proportional to the distance of the charge from the silicon surface.

2.5 Flash memory Reliability

Reliability of a Flash cell is attributed to its endurance and retention. Endurance (capability of maintaining the stored information after erase/program/read cycling) and retention (capability of keeping the stored information in time) are the two parameters that describe how "good" and reliable a cell is.

2.5.1 Charge Retention

As in any nonvolatile memory technology, Flash memories are specified to retain data for over ten years. This means the loss of charge stored in the FG must be as minimal as possible.

Possible causes of charge loss are:

1) defects in the tunnel oxide;
2) defects in the interpoly dielectric;
3) mobile ion contamination; and
4) detrapping of charge from insulating layers surrounding the FG.

The generation of defects in the tunnel oxide can be divided into an extrinsic and an intrinsic one. The former is due to defects in the device structure; the latter is due to the physical mechanisms that are used to program and erase the cell. The tunnel oxidation technology as well as the Flash cell architecture is a key factor for mastering a reliable Flash technology.

The best interpoly dielectric considering both intrinsic properties and process integration issues has been demonstrated to be a triple layer composed of ONO. For several generations, all Flash technologies have used ONO as their interpoly dielectric.

Electrons can be trapped in the insulating layers surrounding the floating gate during wafer processing, as a result of plasma damage, or even during the UV exposure normally used to bring the cell in a well-defined state at the end of the process. The electrons can subsequently detrap with time, especially at high temperature. This apparent charge loss disappears if the process ends with a thermal treatment able to remove the trapped charge.

The retention capability of Flash memories has to be checked by using accelerated tests that usually adopt screening electric fields and hostile environments at high temperature [36].

2.5.2 Endurance

A floating gate needs to endure over 10^5 program/erase cycles. Cycling is known to cause a fairly uniform wear-out of the cell performance, mainly due to tunnel oxide degradation that eventually limits the endurance characteristics [40].

A typical result of an endurance test on a single cell is shown in Figure 2-11. The reduction of the programmed threshold with cycling is due to trap generation in the oxide and to interface state generation at the drain side of the channel that are mechanisms specific to hot-electron degradation. The evolution of the erase threshold voltage reflects the dynamics of net fixed charge in the tunnel oxide as a function of the injected charge. The initial lowering of the erase is due to a pile-up of positive charge which enhances tunneling efficiency, while the long-term increase of the erase is due to a generation of negative traps. Cycling wear-out can be reduced by proper device engineering and by optimization of the tunnel oxide process.

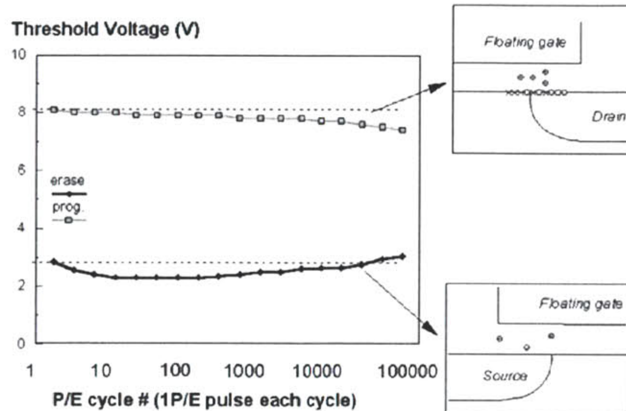


Figure 2-11: Threshold voltage window closure as a function of program/erase cycles on a single cell [36].

2.6 Future Scaling Challenges

NAND and NOR flash memories have had great success with respect to memory cell-size reduction and the corresponding product cost reduction. Looking toward the future, significant scaling challenges are expected. In most cases, even though innovations will exist to facilitate scaling, increasingly, they will involve a significant increase in complexity or the use of expensive new manufacturing tools. Thus, the scaling limit in the future may depend more on economics than on purely technical issues [12].

Flash will face tough challenges, such as much more severe floating gate interference, a lower coupling ratio and less tolerant charge loss. As word-line space drops below 30 nm the capacitance coupling among floating gates is increased as much, which shifts and widens distribution of the cell threshold voltage (V_T). The height of the floating gate must be decreased to reduce the coupling. Figure 2-13 shows the necessary height of the floating gate for suppressing a V_T shift induced by coupling below 0.2V. While low-k dielectric materials help improve the floating gate coupling, the capacity to scale it down will be increasingly limited.

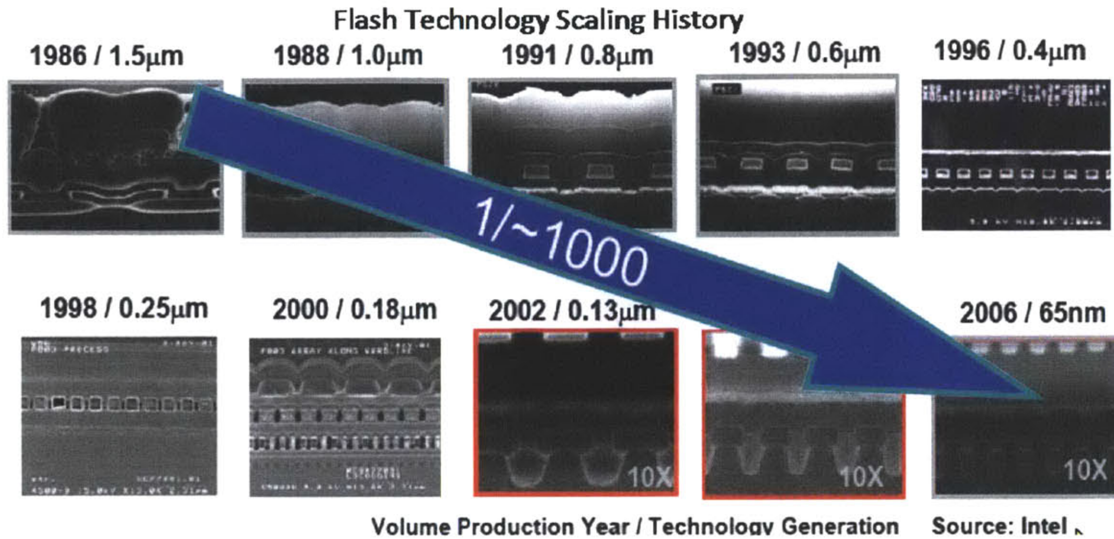


Figure 2-12: Flash memory device scaling history (source: Dr. A. Fazio, Intel Corp.).

Another structural limit at around 35nm NAND technology node is that the utilization of floating gate sidewall ONO (Oxide Nitride Oxide) capacitance will no longer be possible because the inter-poly dielectrics will be thicker than the space between floating gates. Since the sidewall's contribution to the coupling ratio from control gate to floating gate is reduced, the coupling ratio will drop drastically to below 0.4 at 35nm node as shown in Figure 2-13. To enhance the coupling ratio, inter-poly ONO dielectrics needs to be scaled down from the approximate 15 nm in use today. But its scaling looks very difficult. The development of ultra low leakage high-k dielectric materials for the NAND Flash inter-poly coupling capacitor application will be one of the most important and difficult tasks for the further scaling of NAND Flash at around and beyond 35nm node [41].

The number of electrons on the floating gate is significantly decreased due to the decrease of inter-poly ONO capacitance. It is expected that less than 100 electrons for a V_T shift of 6V will be stored following 30 nm design rule. Considering that a MLC will fail after a 5 percent loss of the charges stored in the floating gate, loss of no more than 10 electrons is allowed over a 10-year period of operation for the device [41].

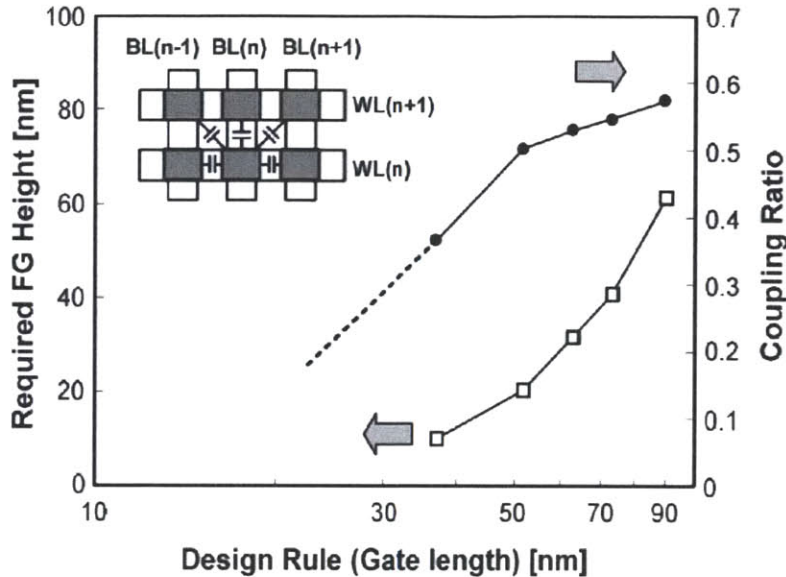


Figure 2-13: Required floating-gate height for the effective suppression of inter-poly coupling interferences and coupling ratio by design rule [41].

Broadly speaking, there are three key areas of challenges for flash memory scaling:

- Physical scaling that is primarily defined by lithography and the cell layout design;
- Electrical scaling that is primarily defined by the program/erase/read voltage requirements; and
- Reliability scaling that is primarily defined by the fundamental physics of the program, erase, and storage mechanisms.

2.6.1 Physical Cell-Scaling Challenges

In all cases, lithography is still the main factor affecting Moore's Law scaling. NAND memory, with its very regular layout consisting of straight lines and spaces, allows for the use of many optical enhancement technologies that greatly facilitate the continued use of conventional optical lithography. Consequently, NAND memory leads the industry with the tightest lithographic pitch of any silicon memory products. However, conventional lithography with i-line and immersion technology is affected by a manufacturing limit at approximately 40 nm. New techniques such as self-aligned double patterning have been reported [42] that go beyond

conventional lithography. The space between lines can be further subdivided by using spacers on two sides of the lithographic line, effectively improving the resolution. The ability to define minimum line and space is extended to nearly 20 nm given this feature, and will mostly likely not be the limiting factor for scaling. Note that this technique adds exposure and other process steps that increase the cost of pattern definition. In the case of NOR memory for the 65-nm generation, the layout of the memory cell has 45-degree angle structures around source contacts that are not conducive to optical enhancement techniques. To improve NOR scaling in two significant ways a self-aligned contact technology is being developed for the 45-nm lithographic node. First, the self-aligned contact reduces the contact area. This is a scaling limitation for NOR flash memories. Second, the new layout consists of straight lines only similar to NAND, making it easier to implement optical enhancement techniques [43].

In summary, it is possible to continue to reduce the physical size of the cell to dimensions close to 20 nm for both NOR and NAND memories. The true limiters of cell-size reduction involve electrical and reliability requirements, topics that are discussed in the following sections [12].

2.6.2 Electrical Cell-Scaling Challenges

For NOR flash memories, a primary scaling limitation for the cell is the high voltage required during the programming operations that in turn limits the minimum channel length. To achieve hot carrier channel programming, a voltage of more than 4 V is required from the drain to the source to produce electrons of sufficient energy to overcome the 3.2-eV Si-to-SiO_2 barrier height [12]. Therefore, the minimum gate length will be limited to the channel length that can withstand the required programming voltage. For NAND flash, the transistor channel is used for read only, requiring a much lower drain-to-source voltage and, therefore, a shorter channel length limit.

Three-dimensional cell structures are one way to address the gate length scaling constraint. Both above- silicon fin structures [44, 45] and below-silicon U-shaped structures [46] have been reported. These structures move the channel length constraint into the Z direction, allowing further X/Y scaling to occur, a design that permits further area scaling while maintaining the total channel length required. Recent experimental results reported for NAND, involving the

hemi-cylindrical FET (HCFET) [42], show superior transistor characteristics down to the 38-nm node.

Another significant scaling limitation involves maintaining adequate coupling of the control gate to the floating gate. A high coupling ratio is required to provide adequate control of the channel used for reads. As the cell scales in size and self-aligned techniques are used for the floating gate, maintaining control of the channel requires a thinner inter-poly dielectric between the control gate and the floating gate. One possible solution is the use of a high-k dielectric (i.e., a dielectric material with a high dielectric constant). It must be emphasized that the requirement of a high-k dielectric for the inter-polysilicon layer is different from a high-k dielectric for the transistor gate. The inter-poly dielectric has to be optimized for no leakage current under low-field charge storage, whereas a gate dielectric can have a small leakage current.

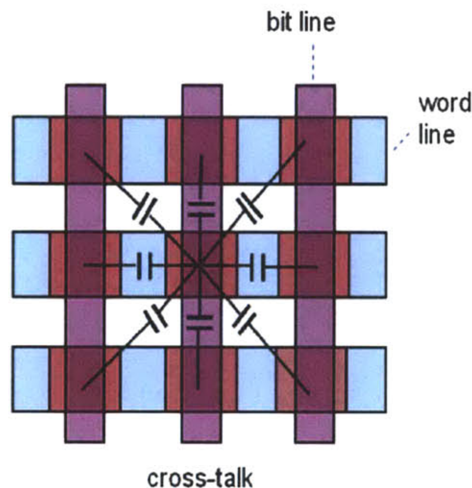


Figure 2-14: Schematic of a Flash array, showing row and column disturbs occurring when the cycled cell is programmed.

Another scaling limitation involves the coupling of two adjacent cells through the capacitance between the cells [44, 46]. As the spacing between floating gates is reduced, the floating-gate to floating-gate coupling increases. The data stored in one cell can influence the operation of an adjacent cell. Different solutions exist to address this problem, including reducing the size of the floating gate, electrical screening of the floating gate, or special read biases to compensate for

Figure 2-15: Minimization of crosstalk by replacing the floating gate with either floating traps or floating conducting islands.

the coupling. In the case of NAND memory, the most promising approach is to replace the floating gate with either floating traps or floating conducting islands that function as charge storage layers. In such cases, the capacitive coupling between adjacent cell charge storage layers is greatly reduced (Figure 2-16). However, this is not a possible solution for floating-gate NOR memory, because in order to move across the transistor channel, NOR memory relies on a conducting charge storage layer to redistribute the channel hot electron charge injected in the drain area.

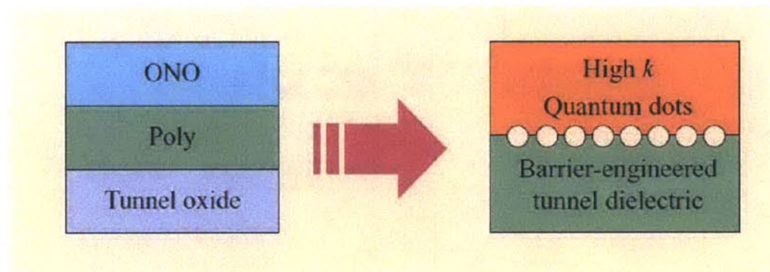


Figure 2-16: High-level depiction of floating-gate transistor improvement. The ONO dielectric in the traditional transistor (left) is replaced by a high-k insulating dielectric (right). A floating-gate (poly in the diagram) is replaced by either floating [12].

In summary, the general concept of extending scaling limit is shown in Figure 2-16. First, ONO (oxide-nitride- oxide) scaling can be extended by the use of a high-k dielectric. Second, the polycrystalline floating gate can be replaced by either floating traps or floating quantum dots. Finally, alternative materials can be explored to allow further improvement of the tunneling dielectric. Tunnel oxide of non-volatile memory (NVM) devices would be very difficult to downscale if ten-year data retention were still needed. This requirement limits further

improvement of device performance in terms of programming speed and operating voltages.

When tunnel oxide for non-volatile memory (NVM) is scaled, the direct tunneling effect becomes dominant. A simple calculation shows that the minimum thickness is around 6 nm (see section 3.2.2.3). In addition, the strain-induced leakage current increases for thinner oxides and aggravates scaling of tunnel oxide thickness. In current flash NVM devices the tunnel oxide thickness is approximately in the 7–8 nm range. When the barrier is thin, the program and erase process is more rapid at the expense of charge leakage that destroys the retention time. When the barrier is relatively thick, long charge retention times are achieved at the expense of a higher voltage and a longer period of time that are required to program and erase the floating gate. Because of this, downscaling of tunnel oxide would be very difficult if ten-year data retention were still required. Consequently, for low-power applications with Fowler- Nordheim (FN) programming, such as NAND, program and erase voltages are sustained at unacceptably high levels. A promising solution for tunnel oxide scaling is engineering the tunnel dielectric so that the retention is not compromised at low electric fields while the tunneling probability is

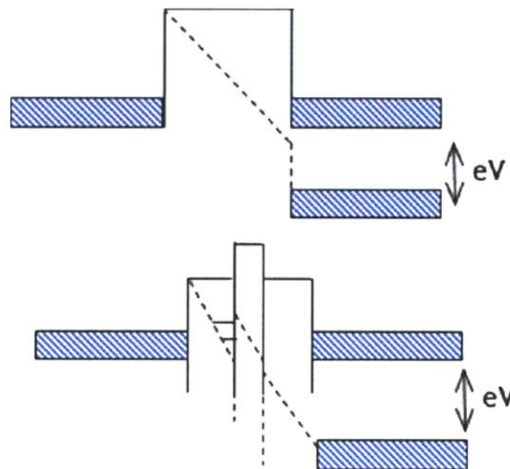


Figure 2-17: Conduction band edge diagrams of typical uniform barrier and crested symmetric barrier.

enhanced at high fields by using multiple dielectrics of different barrier. This may be made possible with the improvement in atomic-layer deposition processes and the demonstration of trap-free dielectric films. Note that in all of the above examples, new materials are involved. The introduction of new materials in semiconductor manufacturing is a key part of the innovations

that enabled Moore's Law scaling to continue for so many generations.

2.6.3 Reliability Scaling Challenges

One of the most significant innovations in both NOR and NAND flash memories is multilevel cell (MLC) technology: the storage of more than one bit in a single flash cell. This is possible for flash memory because of the analog nature of charge storage in the floating gate that allows for subdividing the amount of stored charge into small increments. When this is coupled with the superior retention characteristics of the floating gate, it is possible to accurately determine the charge state after a long period of time. The weakness of MLC arises because the separation between charge states is less for MLC technologies compared to SLC (single-level cell) technologies, resulting in a higher sensitivity to cell degradation mechanisms. To achieve stable storage, it is important to properly control the write and erase operations, using special MLC charge-placement algorithms, to reduce the damage of the tunnel dielectric by reducing the applied fields and controlling how the fields are increased or decreased with the controller rate during write and erase. A further enhancement is the use of error-management techniques, such as error correction, which can recover data or prevent errors.

As the memory cell is scaled, the cell capacitance is decreased, resulting in the decrease of charge stored [44]. For NOR flash with a larger memory cell layout, the number of stored electrons is approximately 1,000 for the 45-nm node, while for NAND flash [46], it is less than 500. In this case, for two-bit-per-cell with four-level MLC technology, the number of electrons per level is just more than 100. While the numbers of stored electrons decrease with each new lithography node, the defect charge leakage mechanisms causing charge loss remain the same.

Thus, the impact of each defect on the cell-threshold voltages is proportionally larger for each new node, manifesting as faster threshold voltage drops and an increase in error rates. One method of mitigation involves the improvement of the tunnel dielectric to make it more resistant to defect generation by the introduction of nitrogen into silicon dioxide. Another method is to replace floating gates with either floating traps such as silicon nitride or floating dots such as silicon islands or metal nanodots. With discrete charge storage, the impact of a defect is limited

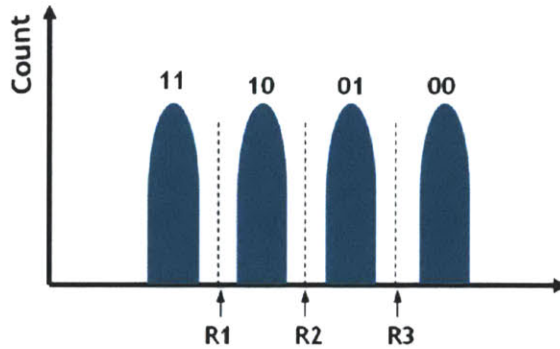


Figure 2-18: Threshold voltage distribution for 2 b/cell.

only to charge stored in its proximity and not to leaking of the conducting floating gate. However, the discrete traps or islands may store a smaller number of electrons compared to a floating gate, further exacerbating the decrease in stored electrons for each storage level. Even though this problem exists in both NOR and NAND memories, for actual products, it is a larger challenge for NOR flash memories because for NOR flash used in program execution, data errors will result in system failure, and the fast-read requirement does not give much time for error detection and corrections. For NAND flash used in secondary data storage, it is possible to implement extensive error corrections through sophisticated data controllers. With the error rate increasing with scaling, it is possible to implement in the data controllers increasing sophisticated error correction techniques that have been developed for the disk drive industry, and which have made disk drives one of the more reliable storage devices [12].

2.7 Segmented Floating Gate memories

In conventional flash memory, since the floating gate is conductive, the electrons can move freely in the conduction band and hence in case of any defect chain within the tunnel oxide, all of the trapped electrons in the floating gate can easily leak to the channel or source/drain through it.

While the discrete charge storage in nano-segmented floating gate limits the impact of any tunnel oxide defects to the charge stored in the proximity of the defect site. Charge stored in the remaining parts of the nano-segmented floating gate remains unaffected due to the low charge

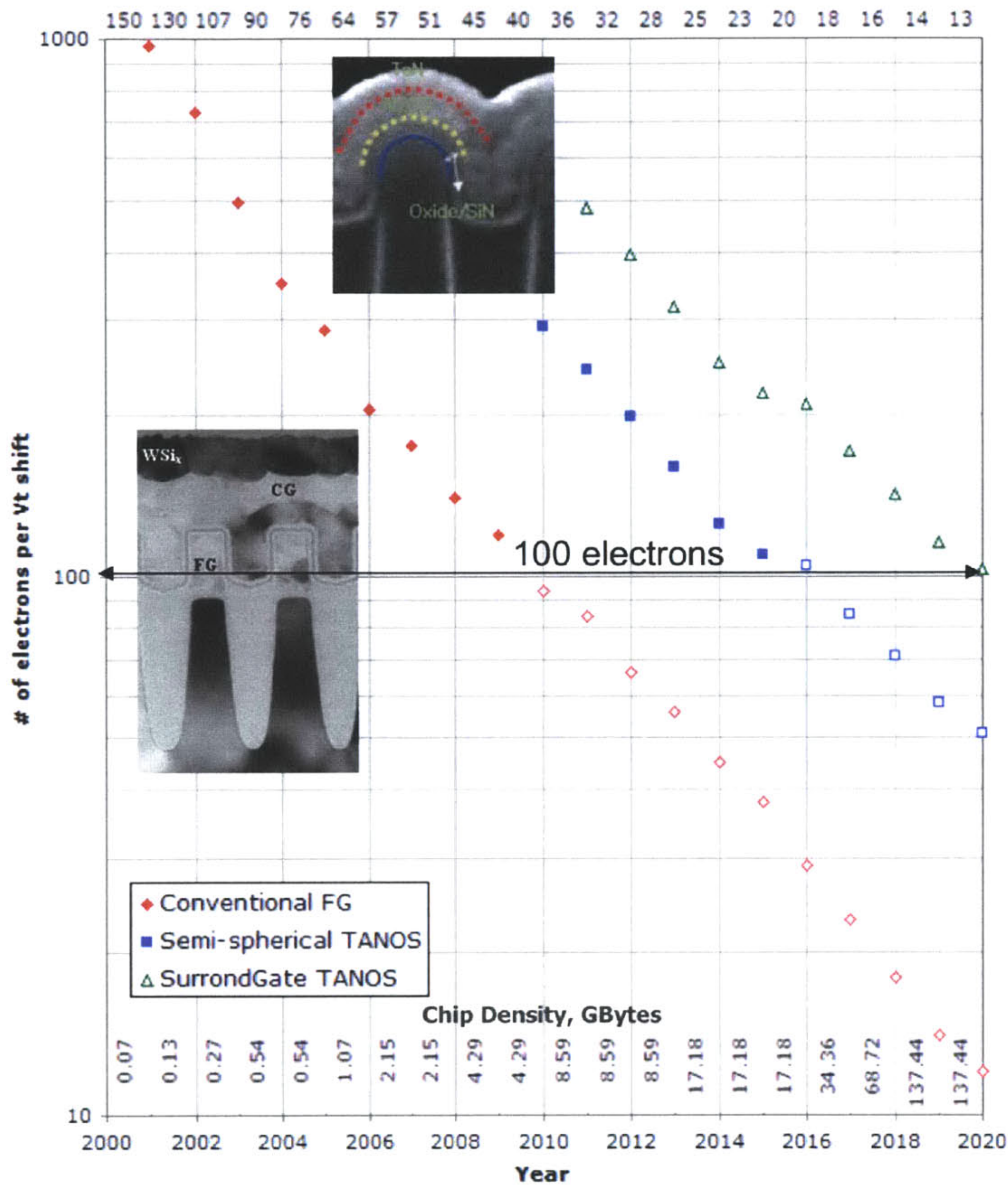


Figure 2-19: Number of Electrons Stored in a Floating Gate (source: Chung Lam, IBM).

mobility in the nano-segmented films, extending the functional retention time of the memory cells. Another scaling limitation involves the coupling of two adjacent cells through the capacitance between the cells. As the spacing between floating gates is reduced, the floating-gate to floating-gate coupling increases. The data stored in one cell can influence the operation of an

adjacent cell. Different solutions exist to address this problem, including reducing the size of the floating gate, electrical screening of the floating gate, or special read biases to compensate for the coupling. However, in the case of NAND memory, replacing the floating gate with either floating traps or floating conducting islands is the most promising approach that provides near-planar cell array with drastically reduced inter-cell coupling, thanks to the absence of floating gates. In such cases, the capacitive coupling between adjacent cell charge storage layers is greatly reduced.

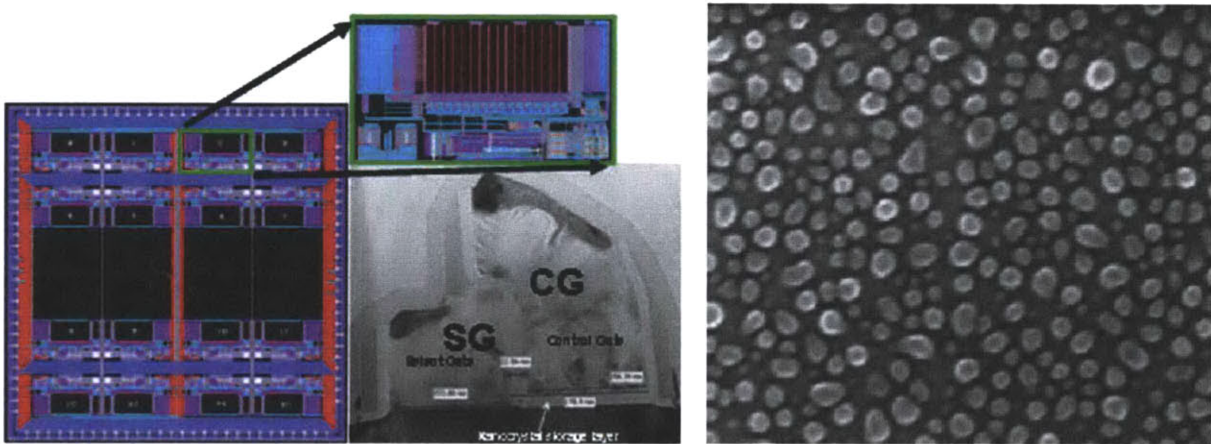


Figure2-20: Segmented floating gate with 10-15 nm in diameter nanocrystals (source:freescale).

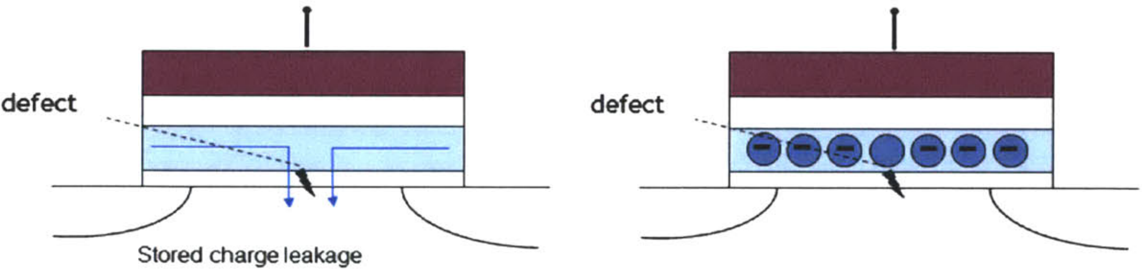


Figure 2-21: Charge loss through the oxide defects in memories with continues floating gate and segmented floating gate.

In QD memories, for example, as shown in Figure 2-22, the stored charge is distributed over multiple QD sites, so that if one of the QDs is discharged due to defects in the very thin tunneling oxide, the remaining QDs in the floating gate would retain their charge and preserve

the memory state of the cell.

The QD layer can vary in order, translation, and rotation, all of which alters the number of charge storage sites between the gate and the channel that alters the shift in threshold voltage, and that ultimately alters the accurate operation of the memory device. Morphology experiments on QD monolayers together with numerical analysis of spatial packing of monodispersed nanoscale QDs indicate that use of the QD floating gate in the 50nm technology node would require use of hexagonally packed ordered QD monolayers with a QD-to-QD center distance spacing of 4nm or less [14].

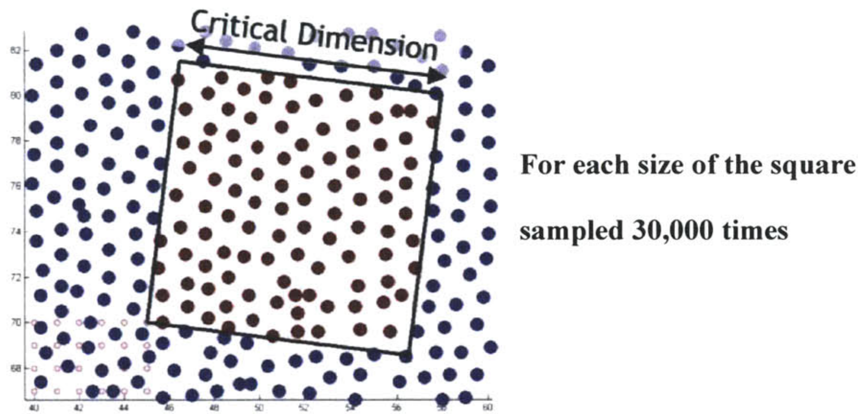


Figure 2-22: The random quantum dot array was obtained from actually spin-casting quantum dots, taking its SEM, and using our own custom software to detect their locations [14].

Technology Design Node	V=+/- 10%	V= +/- 5%
50 nm	7 nm	4 nm
39 nm	6 nm	3 nm
28 nm	4 nm	2 nm
20 nm	3 nm	1 nm

Table 2-1: QD-to-QD distance for technology design nodes [14].

Such closely spaced QDs could be susceptible to significant QD-to-QD charge tunneling, obviating the intended benefit of nanostructuring the gate electrode to preserve charge on individual QDs.

The calculated QD sizes will be difficult to achieve because today's quantum dots are at best around 1 nm in diameter [47] and still need another 1 nm for the insulating cap.

This problem would be especially severe if metallic nanoparticles are utilized, as the large electron state densities and delocalized electron wavefunctions of metallic nanoparticles would facilitate efficient exchange of charges between closely packed QDs.

One solution to these problems is to utilize alternate charge storage elements, with small carrier state densities and high charge carrier binding energies. Molecular materials that are on the order of 1nm represent idealized charge storage elements. The polycrystalline arrangement and relatively smaller intermolecular spacing creates consistent molecular packing. Add to that poor lateral conduction, and the molecular floating gate memory may provide a reliable alternative to QD-FGMs.

2.8 Summary

The structure and operation basics of the conventional flash memories were briefly discussed in this chapter. Electrical and physical cell-scaling challenges and reliability scaling challenges were reviewed.

After an introduction of the general scaling requirement, charge storage on segmented floating gates as a solution for scaling limits were discussed. Challenges and essential properties of the segmented floating gate were briefly reviewed. It was also shown that, QDs memories may not be the ultimate solution to flash memory scaling, due to variation in the order and number of QDs and also tunneling between molecules.

Chapter 3

Molecular Floating Gate Memory

Flash memory device structures with discrete charge storage are potential candidates for continuous memory scaling by maintaining a coupling ratio and reducing crosstalk in conventional floating-gate devices. The discrete charge storage in nano-segmented floating gates inhibits charge transport between the nano-segments, limiting the impact of any one tunnel oxide defect to the charge stored in the proximity of the defect site. Charge stored in the remaining segments of the nano-segmented floating gate would remain unaffected.

One challenge with this approach is that the array of discrete charge-storage segments may cumulatively store a smaller number of electrons than a continuous floating gate of same dimensions. The self-charging energy of individual nano-segments could limit the number of charges stored on each to one electron. In addition, spatial density of nano-segments might have to be small to maintain sufficient spacing between the segments and inhibit charge transport between them, as otherwise charge tunneling between the segments would obviate the intended benefit of nanostructuring the floating gate to preserve charge on individual segments. Underscoring the point, the benefit of nano-segmenting the floating gate is only manifested if high charge storage capability can be maintained [12].

The memory behavior of archetypical molecular thin films is investigated using MOS (metal-oxide-semiconductor) structures in this chapter. Fabrication and detailed characterization of these memory devices are also described.

3.1 Introduction to Organic Molecular Floating gate Memories

A good charge trap material possesses the following material properties: first, there should be deep trap states and enough trap density; second, the trapped charge should stay in the discrete trap location; and third, the conduction band energy level of this material (relative to that of silicon) should be low enough, which favors both the carrier injection into the charge trap layer and the retention time.

An easily evaporated material with favorable physical and electrical properties is preferable as a molecular material for the floating gate. For instance, a planar polycrystalline material with poor lateral mobility is desirable. Poor lateral mobility is important, as it was with a QD floating gate, so that if there is a defect in the tunneling oxide, the charge leakage is localized around that defect.

Molecular electron wavefunctions are strongly localized within the spatial extent of the molecules due to the charge binding energies that are on the order of 0.2 eV or higher [48]. A floating gate consisting of a thin film of molecules would provide the advantage of a uniform set of identical nanostructured charge storage elements with high molecular area densities (e.g. $8 \times 10^{13} cm^{-2}$ for PTCBI thin films used in this dissertation) that can results in several-fold higher density of charge-storage sites as compared to QD memory and even SONOS devices.

Additionally, the low density of free carriers in the molecular thin films and the high charge binding energy on individual molecules limit intermolecular interactions. The minimal overlap between the neighboring molecular electron wavefunctions contributes to the low organic thin film electron/hole mobilities, in the range of from 10^{-1} $cm^2V^{-1}s^{-1}$ to 10^{-7} $cm^2V^{-1}s^{-1}$ - a useful property that builds immunity of stored charge to the structural defects in the neighboring areas of the device.

Furthermore, a larger conduction band offset between the tunnel oxide and charge trap layer is desirable for mitigating trapped charge leakage into the substrate and consequently achieving longer retention time. Considering the lowest unoccupied molecular orbital (LUMO) of the of

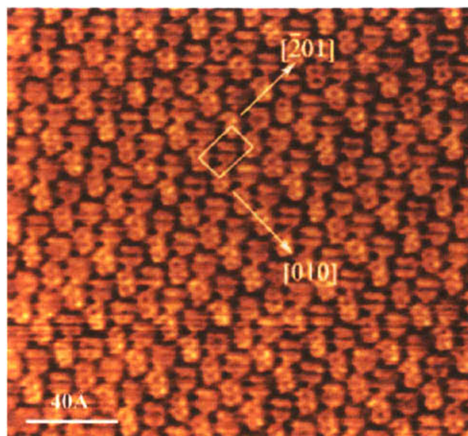


Figure 3-1: A 200 Å × 200 Å STM image of PTCDA on HOPG showing a unit cell consisting of two molecules indicating the crystallographic directions. Image taken in the constant current mode under UHV conditions, with a tip current of 200 nA and voltage of -800 mV [49].

the utilized molecules shown in Figure 3-2, they provide fairly deep trapping sites compared to polysilicon in conventional flash memories or silicon nitride in trap based memories.

Finally, molecular films have the highly desirable consistency of size and morphology that provide relative constancy in the electronic energy level structure of molecular films as compared with QDs that typically exhibit size and order variability. Although organic compounds have recently attracted growing interest for nonvolatile memory applications, many of the devices reported so far are two-terminal resistive memories, rather than reversible charge-storage elements, as described in this work.

An image of PTCDA molecules shown in Figure 3-1 was created using a Scanning Tunneling Microscope (STM), which is a technique to achieve atomic level resolution of a material.

3.2 Molecular Floating Gate Capacitors

One of the key advantages of working with organic semiconductors is that there are an almost limitless number of them. Compared to inorganic semiconductors, they are very easy to modify or design entirely from scratch.

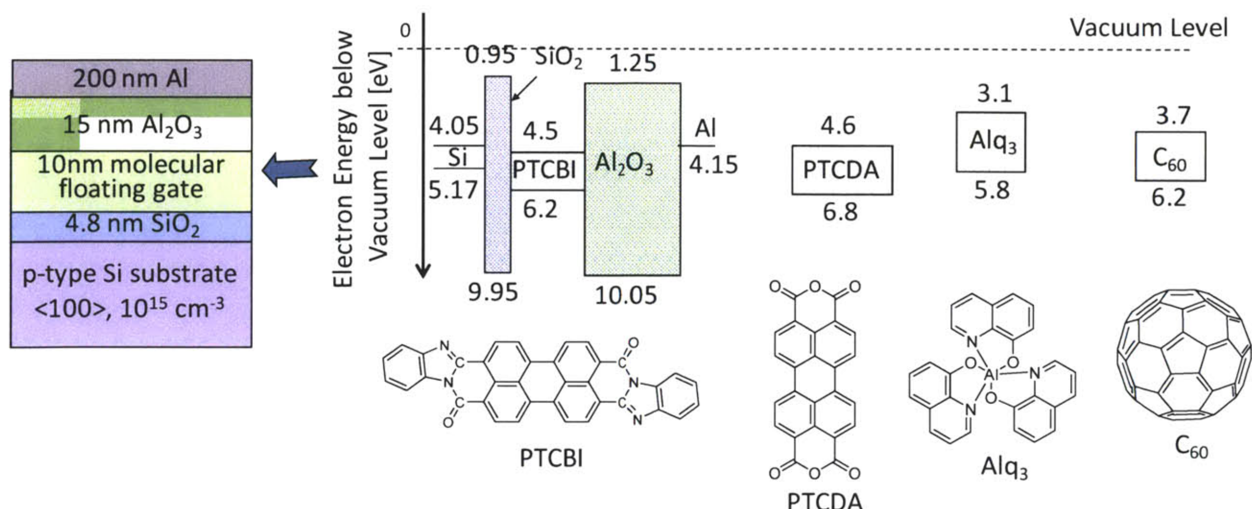


Figure 3-2: (a) The schematic cross-section of the device structure; (b) Suggested energy-band diagrams of four different organic memory devices with chemical structure of each material (energy values are in eV). The terms for organic HOMO and LUMO are analogous to valence and conductive bands used for inorganic solid state physics. According to this analogy electrons or negative charges are mobile across the LUMO level, while holes or positive charges are mobile across the HUMO level.

Charge-storage behavior has been investigated in this dissertation through the use of a series of molecular thin films embedded in metal-oxide-semiconductor (MOS) structures with SiO_2 and Al_2O_3 as the tunneling and control oxides, respectively. By comparing performance of different devices we identify the molecular thin film characteristics best suited for design of floating gate memories. Capacitive memory structures have been fabricated using archetypical molecular thin films with different charge storage energy levels and charge mobility including 3,4,9,10-perylenetetracarboxylic dianhydride (PTCDA), 3,4,9,10- perylenetetracarboxylic bis-benzimidazole (PTCBI), tris-(8-hydroxyquinoline) aluminum (Alq_3), and fullerene (C_{60}).

The charge storage, retention, and program/erase endurance characteristics were examined via the capacitance voltage (*C-V*) measurements at frequency of 100 kHz, by using Agilent 4294 impedance analyzer at room temperature. The stored charge densities were determined by measuring the shift in the flat band voltage of molecular-film-containing capacitors. Data showed that charge retention times were improved for molecular films with lower carrier mobility that for the first time confirms the stated operational benefit of the nano-segmented floating-gate structures, i.e. that lower charge mobility in the nano-segmented floating gate

inhibits stored charge loss.

3.2.1 Fabrication of MOS devices with Molecular Floating Gate

The energy band diagrams and the schematic cross-section of the capacitive floating gate structures fabricated in this dissertation are shown in Figure 3-2. The molecular-thin-film-containing capacitor was fabricated starting with a growth of a 4.8 nm thick layer of thermal SiO_2 (at 800 °C in dry O_2) on top of a cleaned p-type Si substrate.

Wafer cleaning was accomplished by immersing cassettes of wafers into cleaning baths containing SC-1 solution (1:1:5 $NH_4OH/H_2O_2/H_2O$) for striping organics, metals and particles, 50:1 H_2O/HF for removing the chemical oxide layers that are grown during the first step, and SC-2 solution (1:1:6 $HCL/H_2O_2/H_2O$) for striping alkali ions and metals. The wafers were rinsed with DI H_2O before and after the HF step and also after the last step.

The standard technique for depositing thin films of organic small molecule materials is thermal evaporation in high vacuum.

A sealed chamber capable of being pumped down to pressures of $< 1x10^{-5}$ Torr (or more commonly, $< 1x10^{-6}$ Torr), in which is located an open reservoir of material which can be heated sufficiently that the material either boils or sublimes is required to perform this kind of deposition (Figure 3-3).

At such low pressures, the mean free path of the evaporated material is generally larger than the dimensions of the chamber; and so the material simply coats every surface in line of site of the opening of the reservoir, since those surfaces (unless they are being actively heated) are generally much colder than the boiling/sublimation point of the evaporant.

Thus to deposit a film of material onto a substrate (e.g. a piece of glass or silicon), one need simply mount that substrate somewhere in the line of site of the reservoir opening, and then heat the reservoir up. Usually, one mounts shutters inside the chamber so that one can quickly hide or expose the substrate to the evaporant; in addition, one usually mounts a thickness monitor such that the rate of film deposition can be actively monitored (after appropriate calibration).

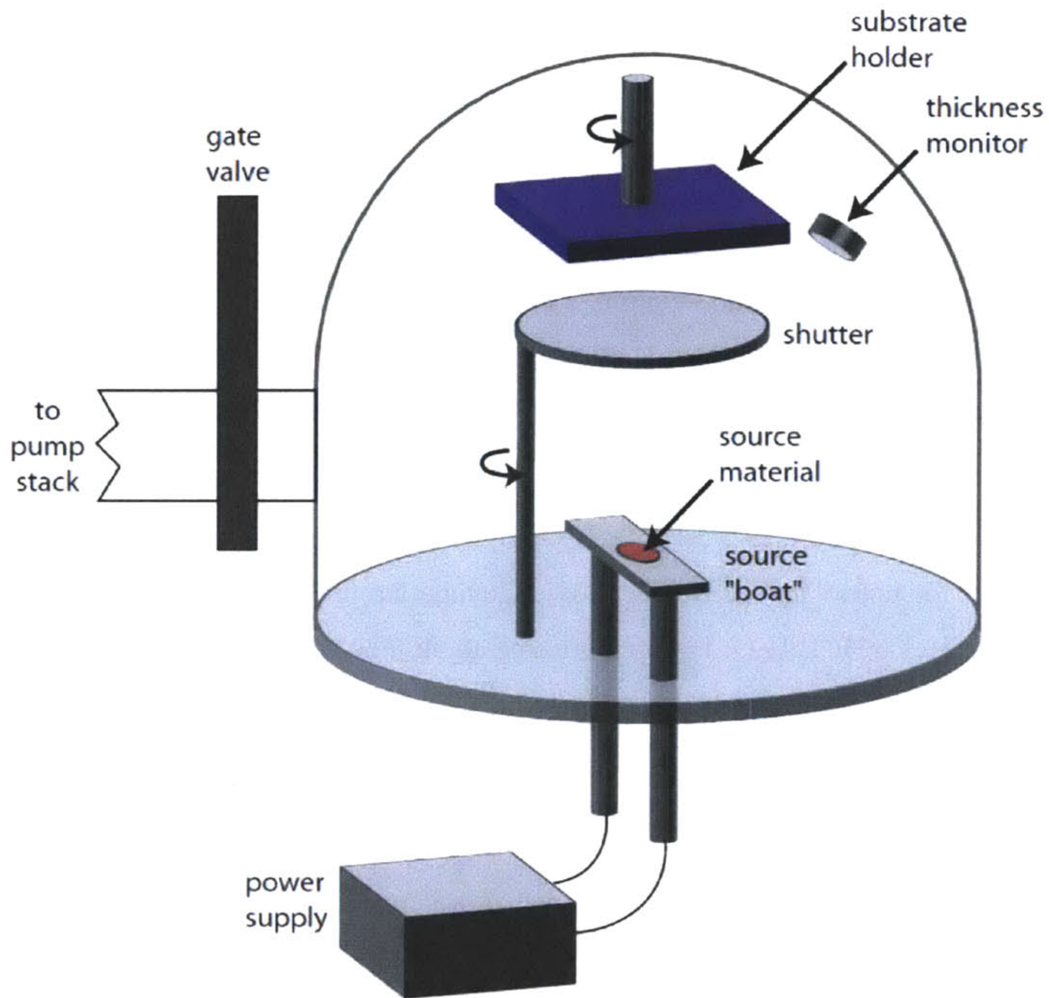


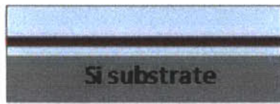
Figure 3-3: Cartoon diagram of a high vacuum thermal evaporation system [50].

The most common monitoring devices for this kind of operation are quartz crystal thickness monitors that provide a film thickness resolution of 0.01 nm. Well-controlled deposition rates are typically achievable in the range of 0.01 to 1 nm/s. This deposition technique is clearly well suited to the rapid growth of thin films in the range of 1 to 1000 nm, with thickness control as fine as 0.01 nm when combined with the aforementioned shutters that typically can be opened or closed in approximately a second.

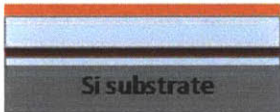
The Si Substrate is cleaned using RCA cleaning process

A layer of SiO_2 is grown at 800 °C in dry O_2 on top of the Si substrate as the tunneling dielectric

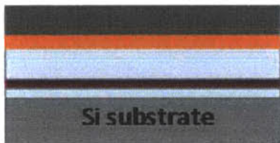
Highly purified molecular layer is thermally evaporated at the rate of (0.15 ± 0.05) nm/s at a base pressure of $<6\times10^{-7}$ torr on top of the SiO_2 layer.



A layer of Al_2O_3 capping layer is deposited by RF magnetron sputtering on top of the organic layer, followed by annealing the devices in N_2 ambient at 275°C for 2.5 hours.

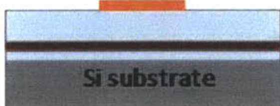


A 100-nm-thick Au film is deposited which serves as a gate electrode.



Wafers are coated with a 1-µm-thick photoresist layer.

The photoresist is prebacked, exposed and postbacked.



After wet etching the electrode, photoresist is removed using acetone/ ashing.

Figure 3-4: Fabrication process steps of memory capacitors with molecular floating gate.

A diagram of a simple thermal evaporation system is shown in Figure 3-3. The molecular material is thermally evaporated at the rate of (0.15 ± 0.05) nm/s at a base pressure of $<6\times10^{-7}$ Torr to form a 10 nm thick layer.

Prior to deposition, the organic materials were purified in three cycles using thermal gradient

sublimation in a three-foot long Pyrex tube that was heated between 450˚C and 100ºC along its length, thereby allowing for the separation of impurities of both high and low volatility from the organic material. The pressure inside the purification tube was maintained at 10^{-2} Torr.

The surface morphology of the molecular layers was observed and studied using atomic force microscopy (AFM). A representative AFM image is shown in Figure 3-5, of 30nm-thick PTCBI on 4 nm-thick thermal SiO_2 on Si substrate, revealing that PTCBI has poly crystalline morphology with an average roughness of 1.42 nm.

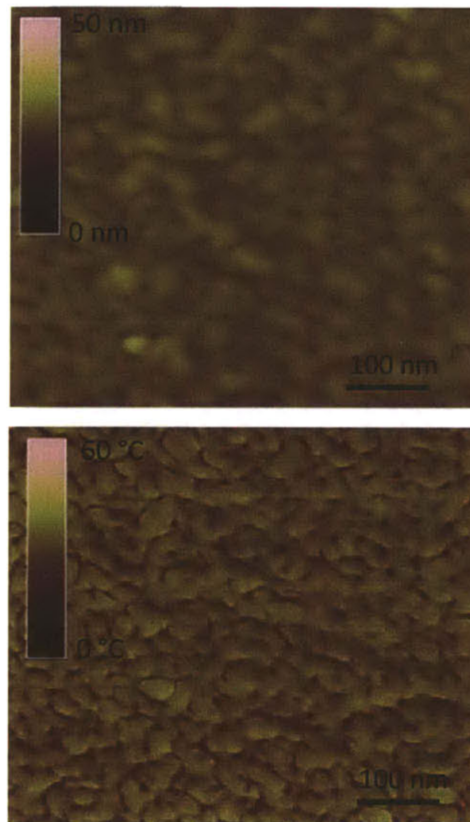


Figure 3-5: AFM (a) topographical and (b) phase images of 30nm-thick PTCBI layer.

Usually a high-*K* material is needed to replace the conventional ONO inter-poly dielectric because the planar structure cannot provide a sufficient gate coupling ratio.

A 15 nm Al_2O_3 capping layer was deposited by RF magnetron sputtering on top of the organic layer that was followed by deposition of a 300 nm thick Al film that served as a gate electrode.

The quality of the sputtered Al_2O_3 can be improved by annealing the devices in N_2 ambient.

Figure 3-6 (b) shows the capacitance and dissipation factor of the MOS capacitors with 15-nm-thick Al_2O_3 on top of the 4.8-nm thermal SiO_2 measured at 100 kHz as functions of gate bias. The devices were annealed at 250 °C and 275 °C for different timing. The dissipation factor is an indication of the structural imperfections associated with defects in an oxide film and is defined as [38]:

$$D = \frac{G}{wC} \quad (3\text{-}1)$$

where $\omega = 2\pi f$; and G is the conductance. For the ideal oxide, G=0.

There are three important sources of small-signal energy loss in the MOS capacitor: (1) changes in the interface trap level occupancy; (2) changes in the occupancy of bulk trap levels; and (3) series resistance.

The capacitors annealed for 4 hours at 250 °C show hysteresis in the *C-V* characteristics and

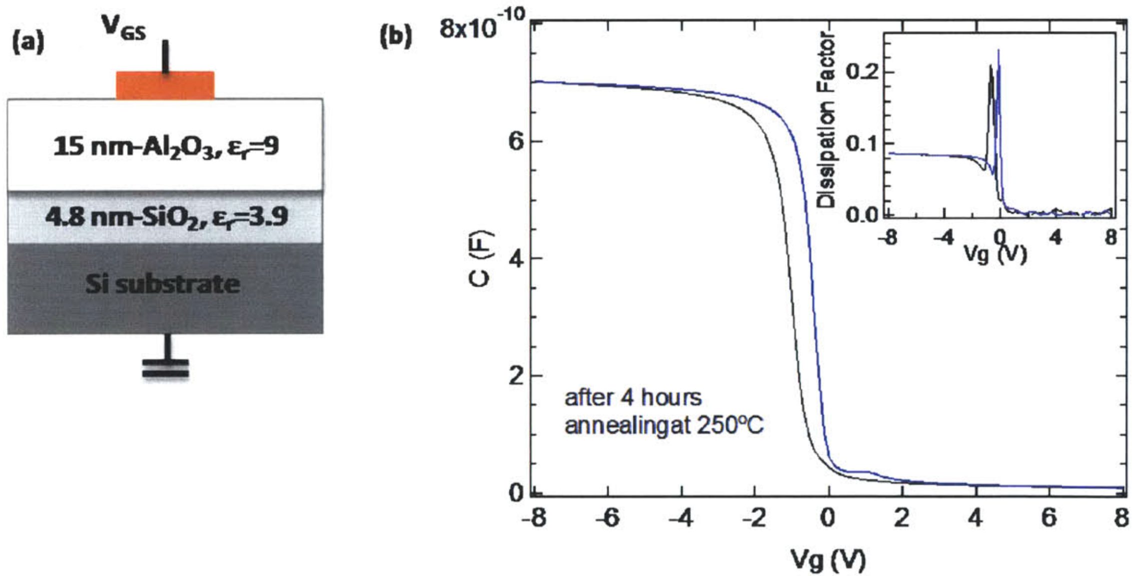


Figure 3-6: (a) Schematic cross section of the MOS capacitor with SiO2 and Al_2O_3 dielectric layers; (b) Capacitance and dissipation factor measured at 100 kHz versus gate bias. MOS capacitors were annealed at 250°C for 4 hours.

D-V characteristics show large peaks which corresponds to interface trap loss. When generation and recombination through interface trap levels dominates the loss, the equivalent parallel conductance goes through a peak as a function of gate bias in weak inversion because interface trap time constant varies inversely with majority carrier density at the silicon surface. As shown in Figure 3-7 by increasing the temperature to 275°C and annealing the device for additional 30 min the hysteresis window and trap associated peak in the *D-V* characteristics decrease showing more sensitivity of the oxide's quality to the temperature. Figure 3-8 shows the *C-V* characteristics of the control device annealed 275°C for 2 hours, which suggests that at this temperature 2 hours annealing would not be sufficient. However, the devices subjected to a 275°C post deposition annealing for 2.5 hours shows a negligible hysteresis window of 0.05 V and no peaks in the *D-V* characteristic (Figure 3-8).

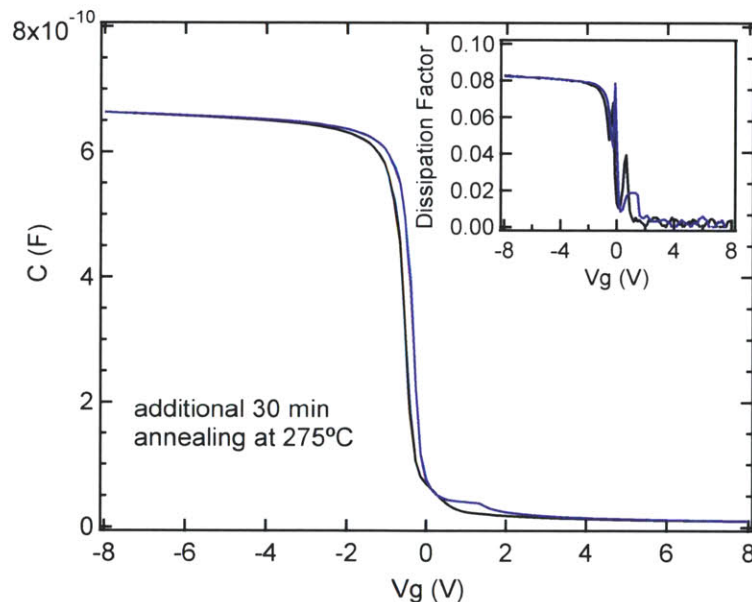


Figure 3-7: Capacitance and dissipation factor measured at 100 kHz versus gate bias. MOS capacitors were annealed at 250°C for 4 hours and then at 275 °C for 30 min.

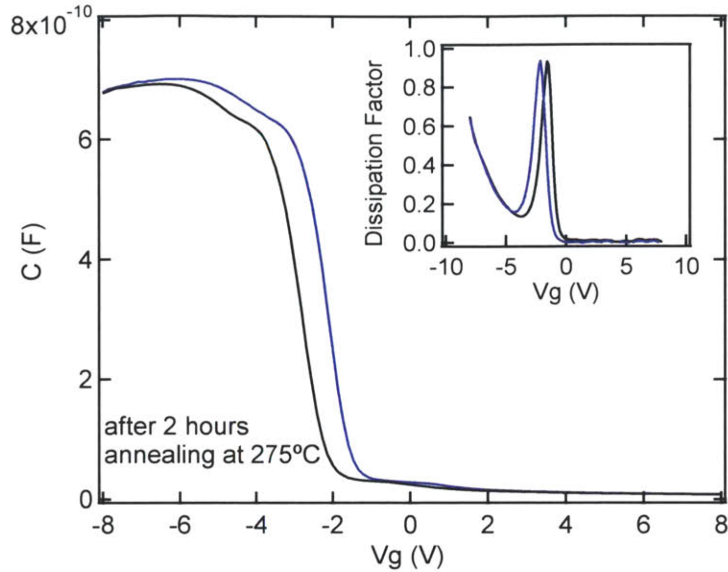


Figure 3-8: Capacitance and dissipation factor measured at 100 kHz versus gate bias. MOS capacitors were annealed at 275°C for 2 hours.

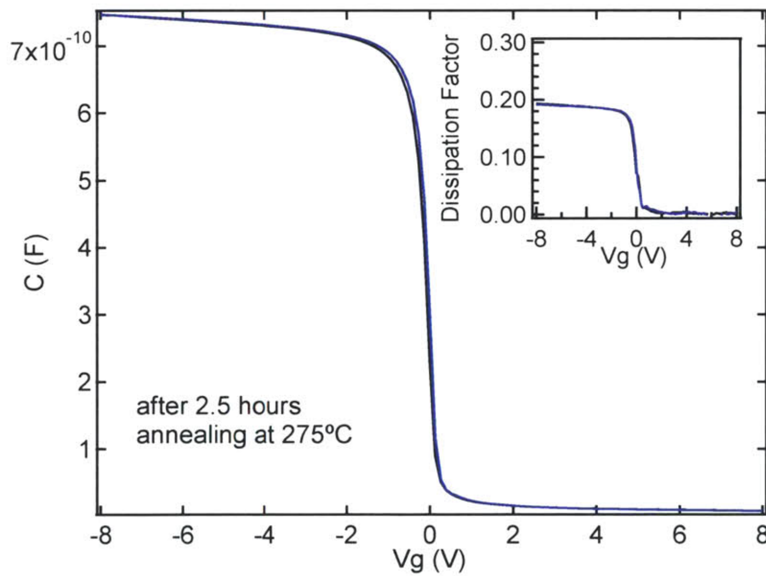


Figure 3-9: Capacitance and dissipation factor measured at 100 kHz versus gate bias. MOS capacitors were annealed at 275°C for 2.5 hours.

The effect of annealing on the organic layer was studied by measuring the photoluminescence intensity of the molecular layer sandwiched between the SiO_2 and Al_2O_3 layer before and after annealing.

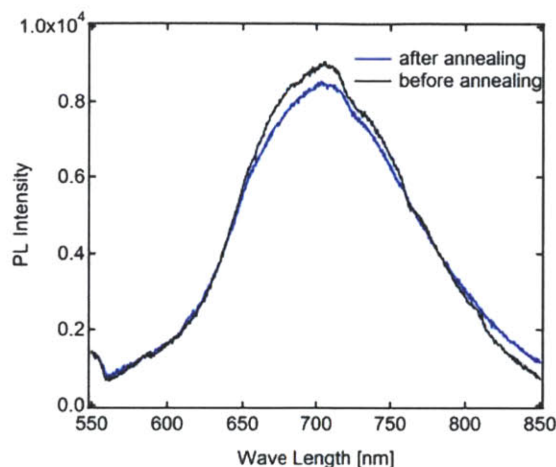


Figure 3-10: Photoluminescence spectra of PTCDA; before and after annealing.

No significant change was observed in the photoluminescence intensity of the organic thin films (that were covered by the Al_2O_3 layer) before and after the annealing in N_2 ambient at 275 °C for 2.5 hours, as shown in Figure 3-10. For the luminescence measurements, the sample was excited using a 337 nm wavelength (3.66 eV) light source with all of the measurements performed at room temperature.

3.2.2 Memory Capacitors with PTCBI, PTCDA, C_{60} Floating gate

3.2.2.1 *C-V* Characteristics

A set of memory structures were made using with a variety of molecular thin films such as the archetypical organic thin films of 3,4,9,10-perylenetetracarboxylic dianhydride (PTCDA), tris-(8-hydroxyquinoline) aluminum (Alq_3), and fullerene (C_{60}) as the floating gate.

C-V characteristics of a device with a 10 nm thick PTCDA layer as a floating gate are plotted in Figure 3-11. A clockwise hysteresis window of 2.5 V was observed for this device upon double sweeping within the range of from -10 V to 10 V, with voltage held for 20 sec at each bias. (In these measurements Si substrate was grounded, with the Al electrode biased as indicated.)

PTCDA consists of a perylene core with a delocalized π-electron system and two anhydride

endgroups. The endgroups give rise to a permanent quadrupole moment with the positive charge situated around the center of the molecule, and the negative charge around the endgroups [51]. The dimensions of PTCDA, calculated from the van der Waals radii of the constituents, corresponds to 14 Å in length and 9.2 Å in width. The crystal structure of PTCDA is monoclinic. Two polymorphic phases (α and β) of very similar lattice constants, but different inclination of the a axis, were observed [52]. In both structures, the two molecules of the unit cell are coplanar and order in a herringbone-like pattern in the (102) plane, which is the cleavage plane of the crystal. These molecular sheets are stacked and the distance between these two planes is different for the two different polymorphs. The crystal parameters of the structure are summarized in Table 3.1.

form	a (Å)	b (Å)	c (Å)	β (^{0})	D_{102} (Å)
α phase	3.74	11.96	17.34	98.8	3.22
β phase	3.87	10.77	19.3	83.5	3.25

Table 3.1: Parameters of the monoclinic unit cell of PTCDA. a, b, c, and β are the parameters of the three-dimensional bulk unit cell, and d_{102} is the inter-planar spacing for the (102)-plane. Taken from [52, 53, 54]

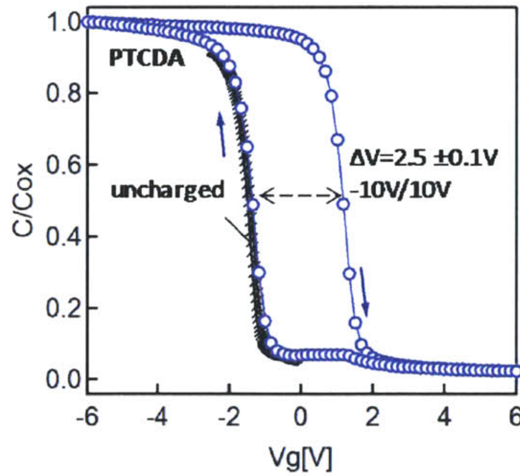


Figure 3-11: The *C-V* characteristics of memory devices with a 10nm thick layer of PTCDA.

The device containing the PTCBI floating gate layer has a clockwise hysteresis, showing a rigid shift of (3.3±0.1) V in the *C-V* characteristics. The voltage shift to the right during the

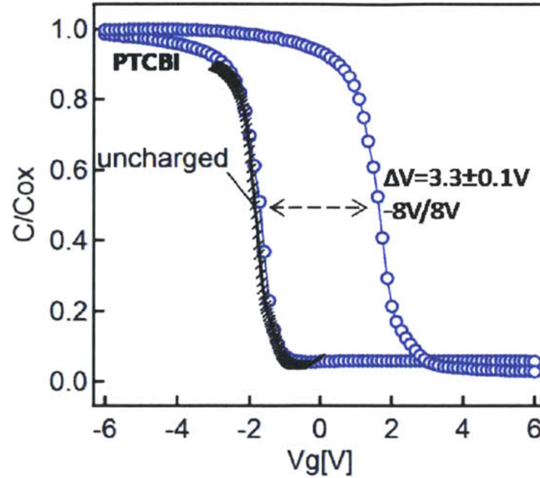


Figure 3-12: The *C-V* characteristics of memory devices with a 10nm thick layer of PTCBI.

positive sweep (from -8 V to +8 V) is indicative of electron charging on the PTCBI floating gate (Figure 3-12).

PTCBI is also a planar molecule that forms a herringbone molecular packing structure when crystallized as seen in Figure 3-13. Unit cells of ordered monolayers of PTCDA and PTCBI contain two molecules each and occupy areas of 2.07 nm^2 and 2.51 nm^2, respectively, which correspond to molecular area densities of 9.7×10^{13} cm^{-2} and 8×10^{13} cm^{-2}, respectively [55].

From the flat band voltage shift the stored charge density of 2.8×10^{12} cm^{-2} for PTCDA and 5×10^{12} cm^{-2} for PTCBI memory devices was estimated.

C_{60} memory devices showed a remarkably large hysteresis window of (6.0±0.1)V for a program/erase condition of -8 V/8 V , as shown in Figure 3-14. A voltage shift to the right during the positive sweep (-8 V to +8 V) and a voltage shift to the left during the negative sweep (+8 V to -8 V) is indicative of both electron and hole charging on the C_{60} floating gate with estimated stored electron and hole densities of 3.6×10^{12} cm-2 and 2.9×10^{12} cm^{-2}, respectively.

C-V measurements were carried out at high frequency of 100 kHz. As mentioned in chapter 2, in such a high frequency, without having electron sources (source/drain regions) to inject electrons into the channel, no inversion will be observed. However partial inversion was observed in the *C-V* of the C_{60}-containing devices that might be due to hole storage in the C_{60} molecules and electron injection from C_{60} molecules into the substrate.

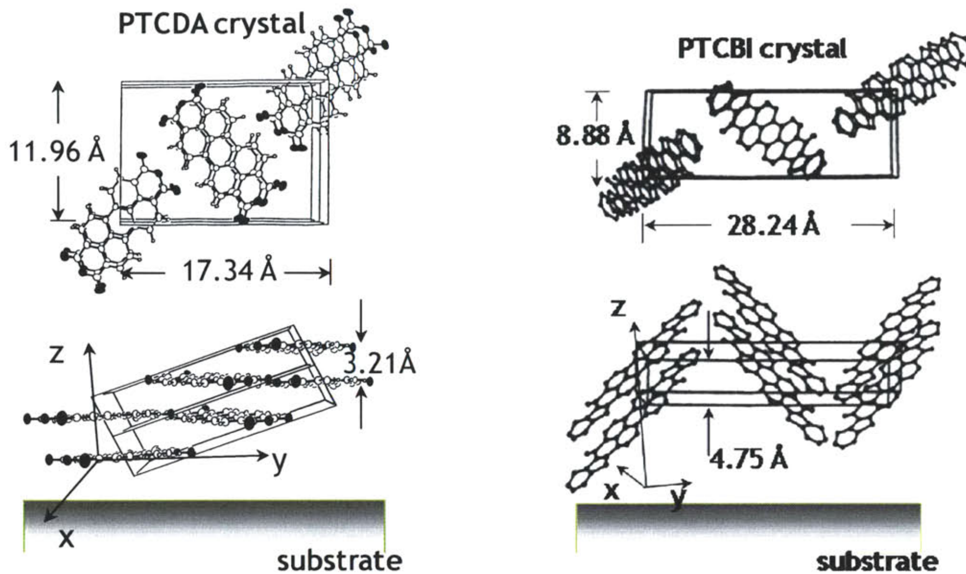


Figure 3-13: Perspective views of a PTCBI and PTCDA unit cell [48].

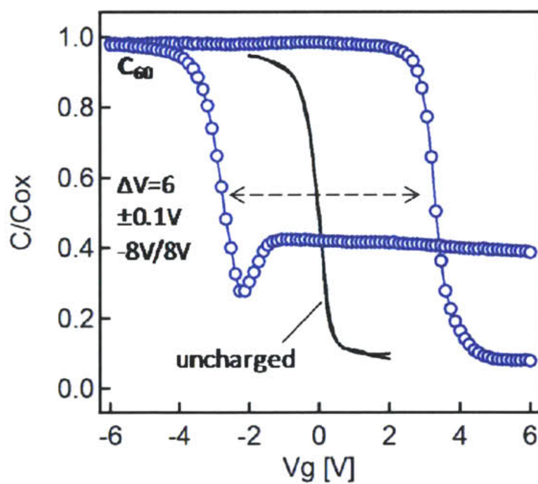


Figure 3-14: The *C-V* characteristics of memory devices with a 10 nm thick layer of C_{60}.

C_{60} has 60 orbital with different levels of degeneracy energy. In which, 30 lower orbital are filled with 60 π electrons. In this case, Hu level is completely filled by the 10 highest energy electrons, becoming the highest occupied molecular orbit (HOMO), while the next energy level, t1u, becomes the lowest unoccupied molecular orbit (LUMO). This molecular orbit can be

partially or fully filled by injecting an electron to the C_{60} molecule. They can attract up to six electrons to completely fill the LUMO [56,57].

Control devices that have no molecular layer show a minimal hysteresis of 0.05 V for program/erase conditions of +8 V/-8 V (Figure 3-15) that is consistent with charge storage in the molecular films in contrast to the molecular-film-containing capacitive memories,

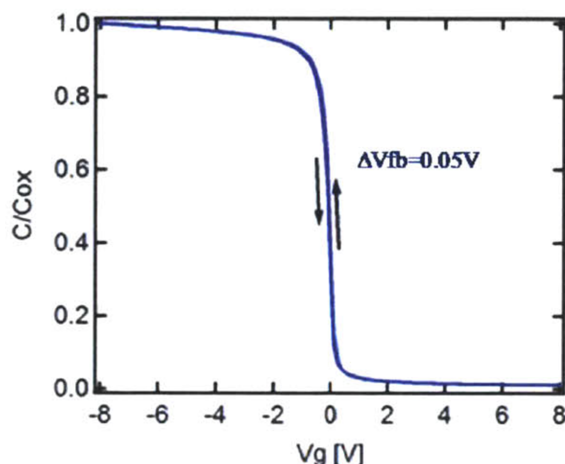


Figure 3-15: The *C-V* characteristics of a control device without organic layer measured in the -8 V/8 V sweep range.

3.2.2.2 Endurance Characteristics

After examining the observed memory effect of the molecular memory devices by measuring the *C-V* hysteresis characteristics of the devices over a range of biasing conditions, endurance measurements were performed. An endurance test is one quantifiable measure of memory device reliability. An endurance measurement was performed by repeatedly performing the program/erase operations and subsequently re-measuring the *C-V* hysteresis window after a number of cycles. For a viable nonvolatile memory technology, the device must be able to withstand $>10^5$ program/erase cycles and still maintain an adequate hysteresis window in the *C-V*

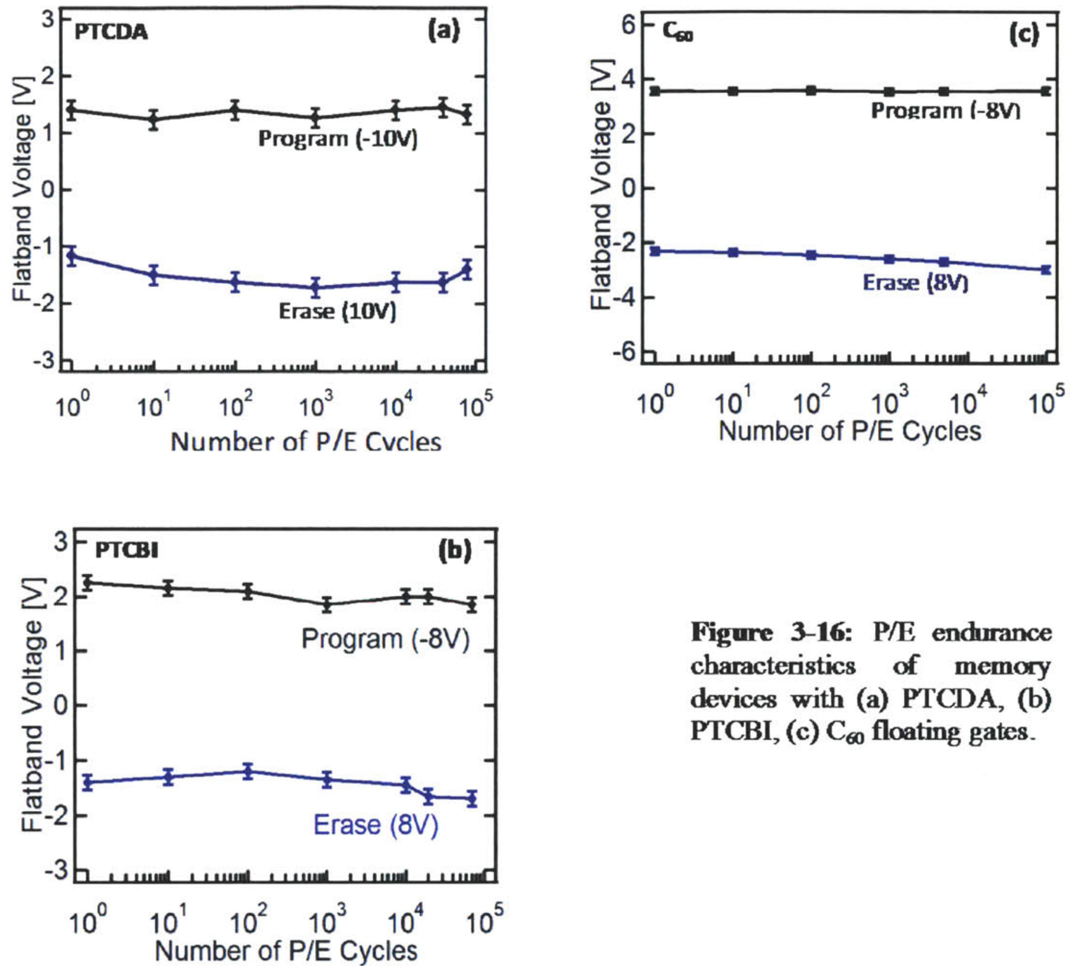


Figure 3-16: P/E endurance characteristics of memory devices with (a) PTCDA, (b) PTCBI, (c) C_{60} floating gates.

characteristics (i.e. to maintain distinct program and erase states).

The cycling endurance results for PTCDA and PTCBI memory devices are plotted in Figure 3-16 (a),(b), showing a ±10% variation in the flat band voltage after more than 10^5 programming and erasing cycles. The endurance characteristics of C_{60} samples exhibit only a slight increase in the flat band voltage shift over the same number of cycles as seen in Figure 3-16 (c).

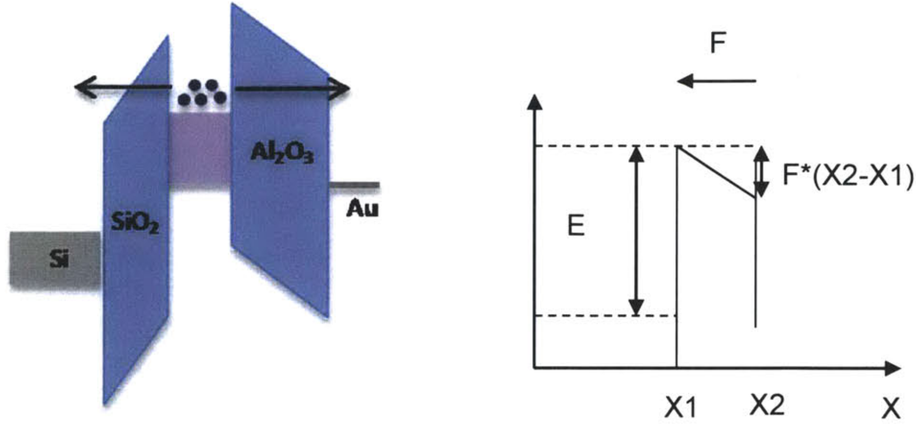


Figure 3-17: Schematic of the trapezoidal energy barrier in data retention mode.

3.2.2.3 Charge Retention Time

There are different mechanisms involved in charge loss during the retention mode. When the cell is programmed, the floating gate has a negative potential due to the stored charge. This potential induces an electric field in the oxide surrounding the floating gate itself; in thin oxides, these electric fields can be as high as some MV/cm. This electric field modifies the barrier shape, leading to increased out tunneling of the trapped charges. Furthermore, trap assisted tunneling can enhance the leakage current considerably in very thin or heavily stressed oxides. The energy barrier in charge retention mode can be approximated by trapezoidal or triangular energy barriers.

A simple trapezoidal energy barrier for which the tunneling probability can be analytically derived with the WKB method is shown in Figure 3-17 [34]:

$$T_{trap}(E) \approx \exp\left(-\frac{4(2m^*)^{1/2}}{3\hbar q}.\frac{E^{3/2}-[-qF(x_2-x_1)+E]^{3/2}}{F}\right)$$

$$T_{trap}(E) \approx \exp\left(-\frac{4(2m^*)^{1/2}}{3\hbar q}.\frac{E^{3/2}}{F}\right) \quad (3\text{-}2)$$

where F denotes the absolute value of the electric field; and E is the effective energy barrier height. The tunneling current from the floating gate to the substrate and top electrode can be computed summing the contributions of all filled states in the floating gate weighted by the corresponding tunneling probability T.

$$\frac{dQ}{dt} = q\frac{P}{m^*}Tg_1^*(E)f_1(E)(1 - f_2(E)) \tag{3-3}$$

where P/m^* is the velocity of electrons hitting the interface, $g_1(E)$ is the available electron states and $f_1(E)$ is the occupation probability in the floating gate and $(1\text{-}f_2(E))$ is the probability of finding an empty state in the region 2 which is Si substrate or top electrode in our case. The expression $q.g_1(E).f_1(E)$ indicates the amount of stored charge density which can be calculated from the flat band voltage shift in C-V characteristics of the memory devices.

The expression $(1 - f_2(E))$ was replaced for simplicity by 1 assuming there are enough empty states in the substrate and top electrode. It should be noted that m^* is the electron's effective mass that is less than the free electron rest mass (m_e) for conductive inorganic semiconductors. As is typical with organics however, this number is calculated to be about 5-20 times the free electron rest mass for electrons and holes [58]. The Simulation results of flatband voltage shift due to field-assisted charge tunneling from the floating gated are shown in Figure 3-18. For these simulations other involved charge loss mechanisms like charge loss through the oxide defects have not been considered. The normalized charge retention during time for a polysilicon floating gate programmed with the stored charge density of 1×10^{13} cm^{-2} with different tunneling oxide thicknesses of 6 nm, 3 nm, and 2.5 nm is shown in Figure 3-18 (a). In this simulation the energy barrier between the conduction band of the floating gate and the conduction band of the tunneling oxide and effective electron mass were assumed to be 3.1 eV, m_e. This simulation demonstrates that it is not possible to scale the thickness of the tunnel oxide below the 6 nm. On the other hand, using the same structure and energy levels, a molecular layer with low mobilities, and consequently low effective conduction masses allows the scaling down of the thickness of the tunnel oxide. It should be noted that in addition to direct tunneling, the oxide defects in the tunneling and top oxide have a significant role in charge loss when in retention mode.

Charge retention experiments were performed on PTDA, PTCBI and C_{60} samples. From the

charge retention results on the set of the tested molecular thin film memories we composed

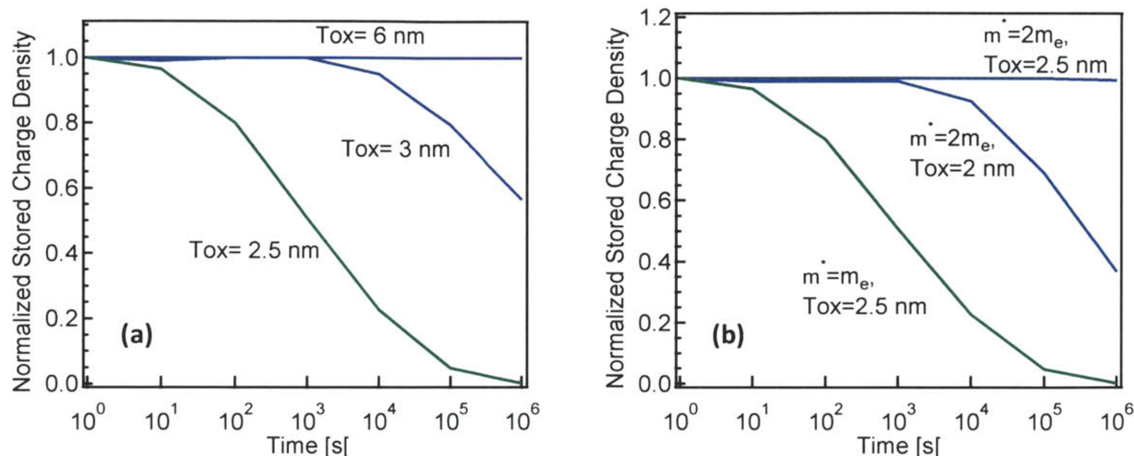


Figure 3-18: Simulation of normalized retention characteristics for (a) a memory device with polysilicon floating gate with different tunneling oxides of 6 nm, 3 nm and 2.5 nm; (b) Charge retention comparison of polysilicon flash memories with memories with higher effective mass like organic materials. The devices were assumed to be programmed with the stored charge density of 10^{13} cm^{-2} and only charge loss mechanism through direct tunneling has been considered for these simulations.

Table I, which shows the dependency of the retention time on the lateral electron mobility of the molecular layer in these memory devices.

Flatband voltage shifts at room temperature are plotted against the retention time in Figure 3-19, with all the plots normalized to the initial shift of each device. These results experimentally demonstrate that charge loss through the oxide defects can be reduced by using materials with low mobility.

The retention loss of C_{60} sample (77% charge loss in 12 min) was found to be much larger than that of the PTCDA (programmed with -10 V) and PTCBI (programmed with -8 V) samples that showed 20% charge loss after 11min and (1.5±0.2) hours, respectively, as shown in Figure 3-19.

The low retention time of C_{60} memory devices compromises their otherwise remarkable memory characteristics. It is suggested that the low retention time of C_{60}-containing memory is due to the high electron mobility (0.05 $cm^2V^{-1}s^{-1}$) of C_{60} which leads to lateral transport of electrons to the existing defects in oxide layers. In contrast, PTCDA thin films behave as one-dimensional conductors that charge transport confined to the molecular stacking direction that is typically normal to the substrate surface. Carrier mobilities range from 10^{-4} to 10^{-5} $cm^2V^{-1}s^{-1}$ in

the direction parallel to molecular planes.

Although PTCDA and PTCBI are very similar in their molecular structures; the larger interplanar stacking distance of PTCBI leads to considerably reduced π-orbital overlap and electronic anisotropy. PTCBI has a larger interplanar stacking distance of 3.45 Å as compared with 3.21 Å for PTCDA. The herringbone packing of PTCBI molecules separates the π-electron clouds on molecular neighbors that results in the low electron mobility ($\mu = 2.4\times10^{-6}$ $cm^2V^{-1}s^{-1}$) of PTCBI thin films in the direction parallel to molecular planes.

Such low charge mobility provides the same advantage as in the earlier demonstration of QDs in the floating gate memories, namely, if a defect exists in the tunneling oxide below the floating gate, charges in the floating gate are unlikely to transport laterally through the low mobility molecular film, reducing the likelihood of discharge through the oxide defect.

	PTCBI	PTCDA	C_{60}
Electron Mobility (cm^2/Vs)	2.4×10^{-6}	10^{-5}	5.1×10^{-2}
20% Charge Loss Time (s)	5.4×10^{3}	6.6×10^{2}	4

Table 3-2: 20% Charge loss time versus electron lateral mobility.

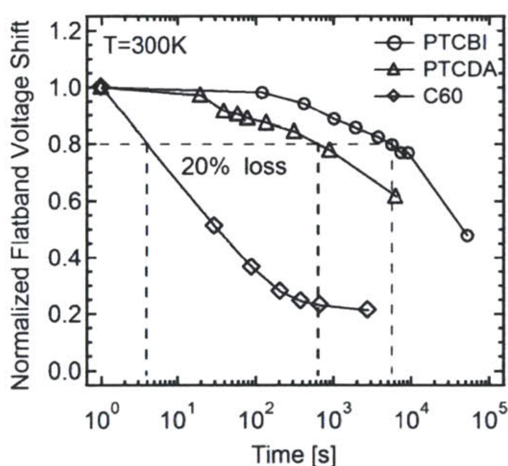


Figure 3-19: Normalized retention characteristics measured at room temperature.

Charge retention of these devices can be further improved by utilizing a higher quality dielectric film by replacing the sputtered Al_2O_3 layers with a high quality Al_2O_3 layer deposited by an atomic-layer deposition (ALD) system or by applying a bi-layer tunnel dielectric consisting of high dielectric constant oxides such as HfO_2.

3.2.3 Alq_3-Containing Memory Capacitors

Alq_3 is a stable polar organic semiconductor with average Alq_3-to-Alq_3 molecular site spacing of 0.87 nm that in a monolayer of Alq_3 corresponds to a high molecular density of 1.3×10^{14} cm^{-2} [59]. Although the spacing between Alq_3 molecules is less than one nanometer, their highly localized electron wavefunctions constrain them to act like separated charge storage nodes. Alq_3 molecules have previously been reported to exhibit negative differential resistance (NDR) and resistance switching properties; although, devices reported to date have been two-terminal resistive memories rather than reversible charge-storage elements [60,61].

The charge storage behavior of Alq_3 molecules was studied via capacitance-voltage (*C-V*) measurements of Alq_3-containing metal-oxide- semiconductor (MOS) structures with SiO_2 and Al_2O_3 as the tunneling and control oxides, respectively. The *C-V* measurements were conducted using an Agilent 4294 impedance analyzer operating at a 1MHz testing frequency.

3.2.3.1 *C-V* Characteristics

As shown in Figure 3-20 the Alq_3 device has a clockwise hysteresis window of (1.8±0.15) V for forward and backward sweep between -9 V and 9 V with voltage held for 20 s at each bias (in these measurements, Si substrate is grounded, with the Al electrode biased as indicated). As discussed in chapter 2 the charge on the floating gate screens the applied electric field that is manifested as an increase in the voltage needed to induce depletion and inversion in the Si semiconductor channel below. During the negative sweep (from +9 V to -9 V) the floating gate is discharged and the *C-V* curve shifts back to the initial state. This memory device has a negligible hysteresis in the uncharged condition as the bias is swept forward and backward between -3 V and 1 V.

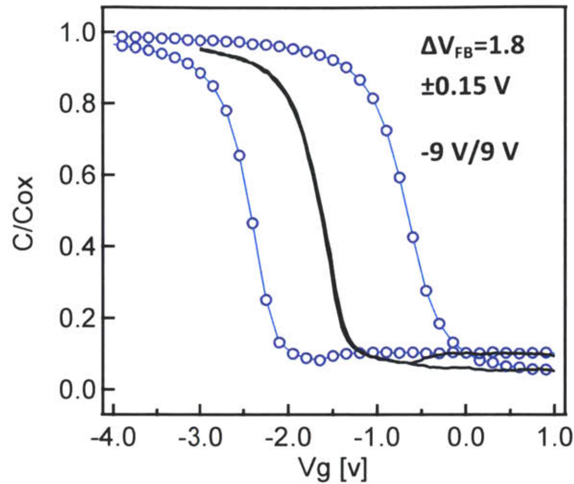


Figure 3-20: The *C-V* characteristics of memory devices with a 10nm thick layer of Alq_3[44].

3.2.3.2 Endurance Characteristics

Alq_3 devices show large change in the flat band voltage values during the program/erase cycling (Figure 3-21). The structural disorder that leads to the low charge mobility in the amorphous Alq_3 molecular thin films can explain the observed gradual change in the flat band voltage with program/erase cycling. Based on Monte Carlo calculations of Madigan and Bulović [59] the structural disorder in the amorphous thin films of polar Alq_3 molecules contributes to the

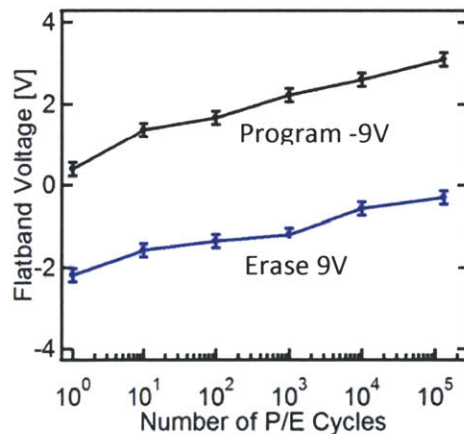


Figure 3-21: P/E endurance characteristics of memory devices with 10 nm Alq_3 floating gates.

energetic disorder in the electronic states of Alq_3 that is manifested as broadening of the distribution of the available electronic energy levels. At the low-energy tail of this distribution are the deep electronic trap states that can be difficult to discharge. The gradual increase in the density of stored electrons in these deep traps during the successive program/erase cycles can be responsible for the observed flat band voltage shift in Alq_3 films towards the positive voltage.

3.2.4 Improving the memory Characteristics of Alq_3 memories

It is evident that with a field of 7 MV/cm, the current density is about 10^{-8} A/cm^2, while with a field of 10 MV/cm it is about 10^{-1} A/cm^2 as can be seen in Figure 3-22. There is a variation of approximately seven orders of magnitude in tunnel current.

A slightly greater field range allows a difference of 12 orders of magnitude. On the other hand, the exponential dependence of tunnel current on the oxide-electric field causes some critical problems of process control because, for example, a very small variation of oxide thickness among the cells in a memory array produces a great difference in programming or erasing currents, thus spreading the threshold voltage distribution in both logical states. It is necessary to have a large electric field in the range of (8-10) MV.cm^{-1} across the tunneling oxide in order to be able to program the memory using FN tunneling.

Ellipsometry measurements of thermally deposited Alq_3 thin films yield a refractive index of n=1.67, which corresponds to relative permittivity of $\varepsilon_{rm} \approx n^2 = 2.79$.

As shown in Figure 3-22 due to the low dielectric constant of the Alq_3 layer and the thickness of this layer, 55% of the programming voltage drops across the molecular layer.

The amount of voltage drop across the tunneling oxide can be calculated from:

$$\Delta V_{TO} = \frac{\frac{d_{TO}}{\varepsilon_{TO}}}{\frac{d_{TO}}{\varepsilon_{TO}} + \frac{d_{FG}}{\varepsilon_{FG}} + \frac{d_{CO}}{\varepsilon_{CO}}} V_{GS} \tag{3-4}$$

where d_{TO}, d_{FG}, d_{CO} represent the thickness and ε_{TO}, ε_{FG}, ε_{CO} represent the relative permittivity of the tunneling oxide, molecular floating gate and control oxide (top oxide), respectively.

By having 9 V programming voltage, the electric field across the SiO_2 layer will be 3.7 $MV.cm^{-1}$ which is not sufficient for FN tunneling. Since most of the voltage drops across the organic layer, increasing the programming voltage in order to achieve a high electric field across the tunneling oxide is not possible due to degradation of the molecular floating layer.
High-K materials tend to have shallow traps. The clockwise hysteresis windows the measured *C-V* characteristics in Figure 3-20 suggesting that the charges are being injected from the gate by trap assisted tunneling through the Al_2O_3 layer.

3.2.4.1 Fabrication

This issue was addressed by reducing the thickness of the molecular layer to 3 nm. The modified memory capacitors were fabricated on top of a cleaned p-type Si substrate with a 5 nm thick layer of thermal SiO_2 (grown at 800 °C in dry O_2) that served as the tunneling oxide. The 3-nm thick Alq_3 floating gate was thermally evaporated in vacuum. A 7.6 nm thick Al_2O_3 control oxide layer was then deposited by RF magnetron sputtering on top of the organic layer. The sputtering conditions were optimized so as to minimize the possible degradation of the organic layer underneath, by monitoring changes in the mobility and current density of the bottom gate organic thin film transistors, exposed to different plasma conditions.

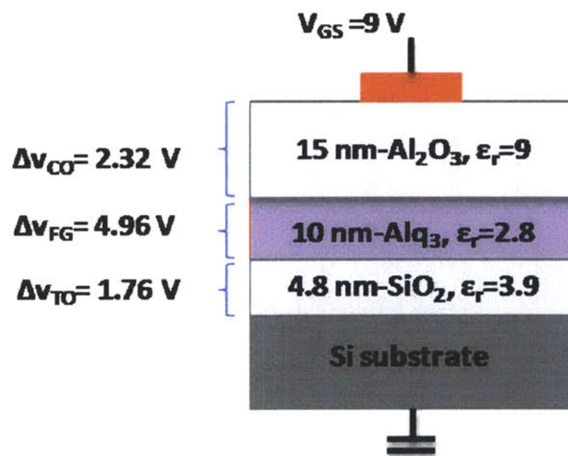


Figure 3-22: The schematic cross section of the device showing the voltage drop across the layers.

Finally, devices were annealed in a N_2 atmosphere at 275 °C for 2.5 hours, before deposition of a 100 nm thick Au film, which served as a gate electrode. Figure 3-23 shows the Cross-sectional Transmission-Electron-Microscopy (XTEM) of the device.

The amount of voltage drop across the tunneling oxide can be calculated from (3-4), which indicates that a high electric field of 12.5 $MV.cm^{-1}$ can be provided across the tunneling oxide during the programming step, all of which makes it feasible to have Fowler-Nordheim tunneling through the tunnel oxide. The oxide breaks by applying voltages higher than 16 V to these devices.

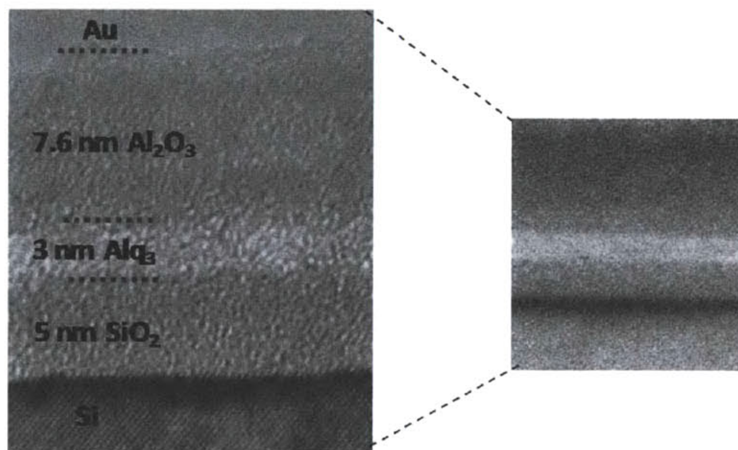


Figure 3-23: A transmission electron microscope cross-section image of the Alq_3-containing memory.

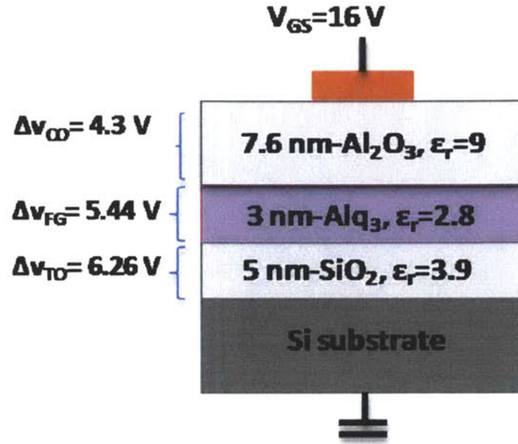


Figure 3-24: The schematic cross section of the device showing the voltage drop across the layers.

3.2.4.2 *C-V* Characteristics

The *C-V* measurements in Figure 3-25 show a remarkably large hysteresis windows of up to (7.8±0.1) V for the program/erase condition of -16 V/+13 V with voltage held at each bias for 1msec. Holes were injected through the tunneling oxide into the Alq_3 floating gate by applying negative voltages on the Au gate with respect to the Si substrate, resulting in a shifting the *C-V* curve toward negative voltages. A stored hole density of 5.4×10^{13} cm^{-2} was estimated from the amount of flatband voltage shift using the following relation:

$$n = \frac{C_{cont}\times\Delta V_{FB}}{q} \quad (3\text{-}5)$$

where n, C_{cont}, ΔV_{FB}, and q are stored charge density, capacitance of the control oxide, flatband voltage shift and the elemental charge, respectively. The calculated stored charge density is comparable with that calculated using the KFM method.

To the best of our knowledge, this storage capacity significantly exceeds any previously reported for molecular- or quantum dot-based memory devices [15,17,18].

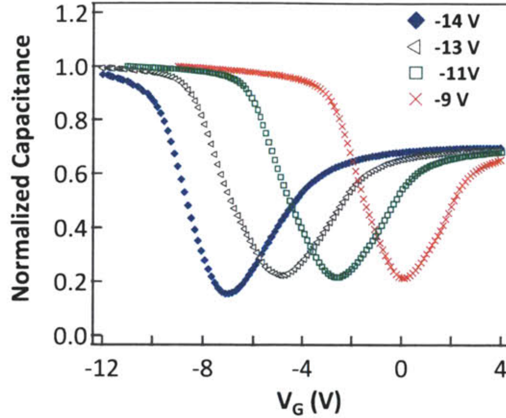


Figure 3-25: The *C-V* characteristics of memory devices comprising a 3 nm thick layer of Alq3 (program time: 50 msec).

Control devices with no molecular layer show negligible hysteresis that is consistent with charge storage in the molecular films rather than in dielectric traps of Al_2O_3 or interface traps.

The amount of flatband voltage shift as a function of the programming and erasing voltage is plotted in Figure 3-26 (b). The flatband voltage shift saturation at -14 V was observed. Above a certain voltage, gate injection through the top oxide is initiated, leading to programming saturation and charge trapping in top oxide.

By applying -14 V to the gate electrode, the bending in the conduction band of the Al_2O_3 will be comparable to the energy barrier between gate electrode and the conduction band of the Al_2O_3 considering the amount of voltage drop across the top oxide (3.7 V); and as a result there will be the forming of a triangular energy barrier with increased an possibility of electrons tunneling (FN tunneling) into the molecular floating gate.

The energy band diagram suggested in Figure 3-28 is based on having crystalline γ-phase-Al_2O_3 that is just one of several different crystal phases with a dielectric constant varying between 9 and 11. The electronic gap is dependent on the coordination of the Al sites and decreases from ~ 9.2 eV to ~ 6.8-6.9 eV, with the concentration of the four-fold coordinated ionic sites (Figure 3-29).

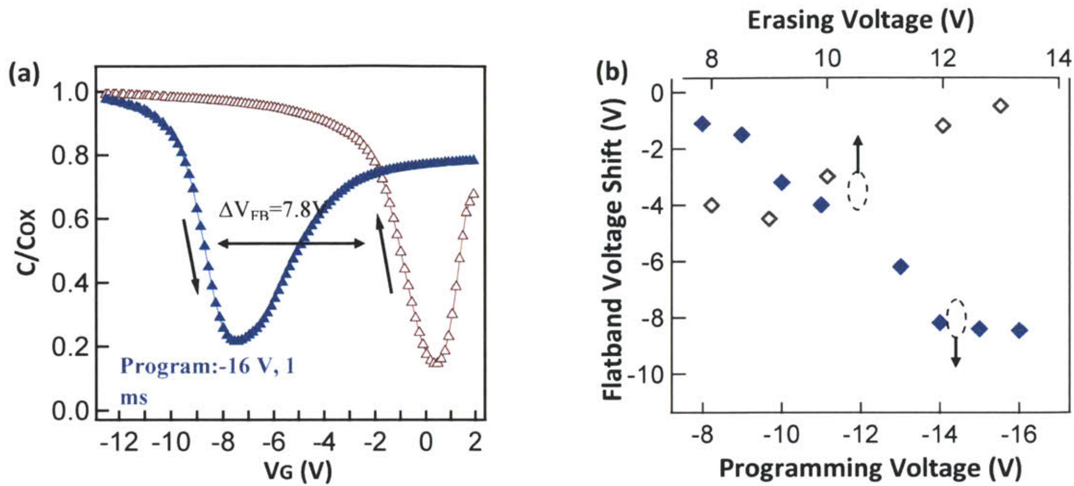


Figure 3-26: (a) the *C-V* characteristics with a charged (programmed) and discharged (erased) floating gate; (b) the flatband voltage shift as a function of programming/erasing voltage.

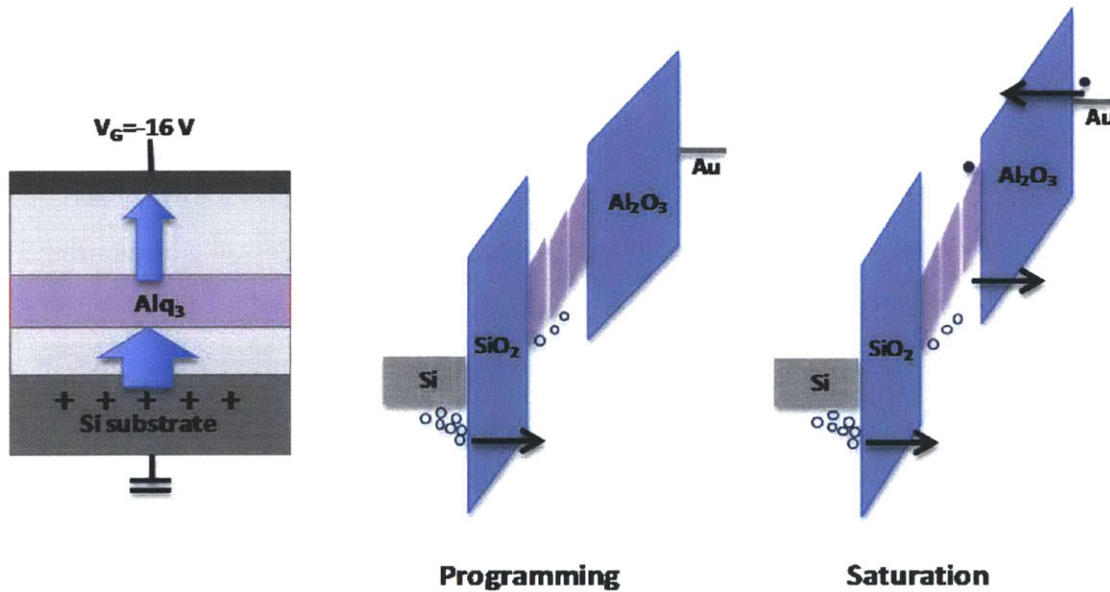


Figure 3-27: During –FN programming, out tunneling of the holes through the top oxide causes programming saturation.

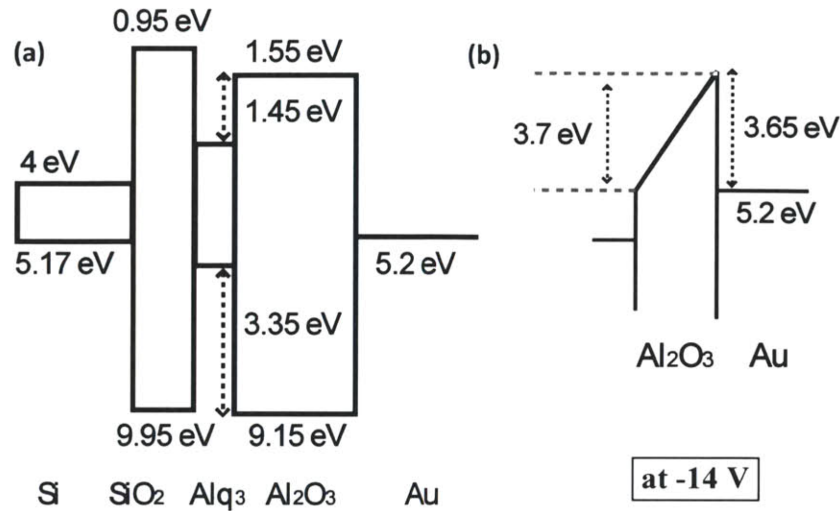


Figure 3-28: (a) Suggested energy band diagram for a memory device with 3-nm thick Alq_3 layer as the floating gate; (b) By applying larger negative bias to the top electrode, triangular energy barrier forms which causes the increased out tunneling from the floating gate and programming saturation.

The α and κ phases have the most promising properties, with a computed band gap of 9.2 and 7.7-7.5 eV, respectively and a macroscopically averaged dielectric constant of ~ 10 [62].

Unfortunately, these crystal phases require crystallization temperatures far too high (> 950°C) to be compatible with the processes typically used for the integration of flash devices.

In contrast, the γ form crystallizes at a much lower temperature (as from 350°C) and is stable upon thermal treatments as high as 1200°C. However, this phase displays a lower band gap (6.7-7.0 eV) than the other polymorphs, which set the material on the edges of the requirements for flash applications (but still within the eligible boundaries). The Al_2O_3 is likely to be γ form considering the annealing temperature of the devices that were utilized and the measured dielectric constant. As mention above γ-Al_2O_3 has lower band gap with shallow traps located at 1.6-2.0 eV and 2.6-3.6 eV below the conduction band edge that contributes to electron injection through the gate and programming saturation at -14 V.

No electron storage was observed in these memory capacitors in contrast to the previous devices showing both electron and hole storage in Alq_3 films. This can be explained by the comparatively smaller energy barrier for electrons tunneling out of the Alq_3 lowest unoccupied molecular orbital into the Si conduction band and gate electrode as compared with the tunneling barrier for holes from Alq_3 highest occupied molecular orbital into Si valence band and top

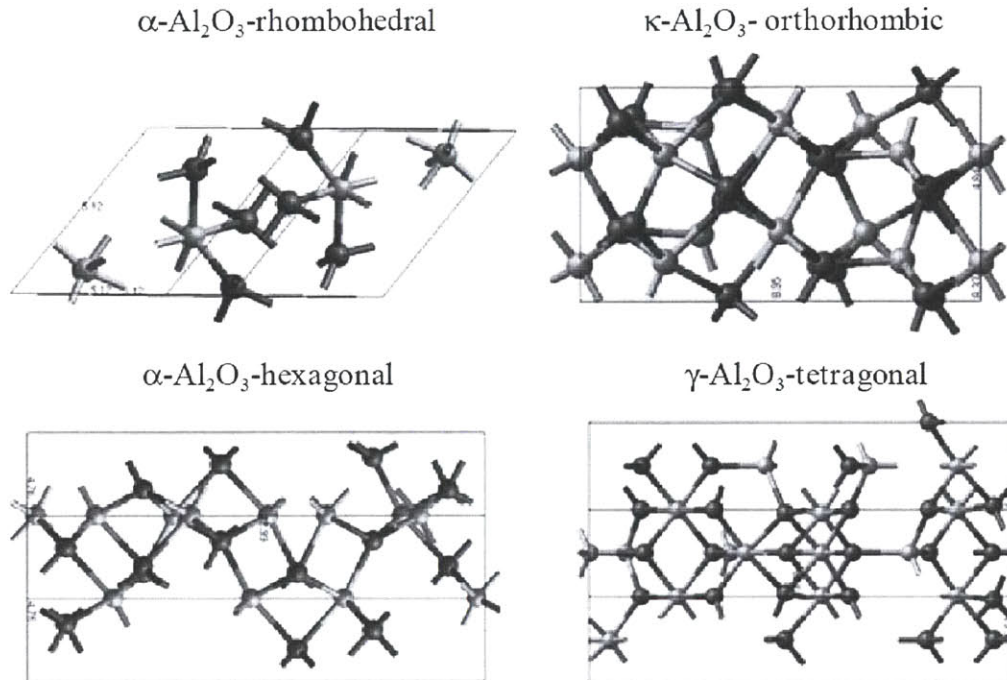


Figure 3-29: Illustration of the different symmetry associated to the crystal phases of Al_2O_3. The Al and O atoms are depicted in grey and black, respectively [62].

electrode, as drawn in Figure 3-30. By applying large positive voltage, the injected electrons into the floating gate will have enough kinetic energy above the conduction band of the control oxide to leak to the control gate. For the device discussed in the previous section however, both electron and hole injections into the floating gate were possible due to different method of charge (trap-assisted) injection and a thicker charge trap layer.

3.2.4.3 Endurance Characteristics

Program/Erase cycle tests were conducted to measure device lifetimes under operation. Even after 24 hours of continuous programming and erasing, the devices showed a large hysteresis window of 4 V. The cycling endurance of the device is plotted in Figure 3-31, showing a 20% variation in hysteresis window after 10^4 programming and erasing cycles. Such performance is sufficient for considering introduction of Alq_3 films into rewritable memory applications.

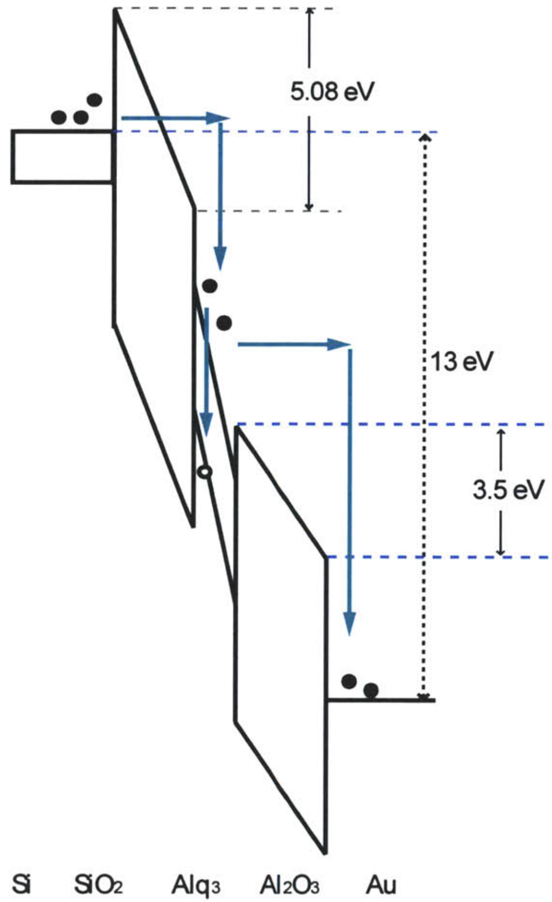


Figure 3-30: Suggested energy band diagram of the memory capacitor at +13 V applied to the gate electron.

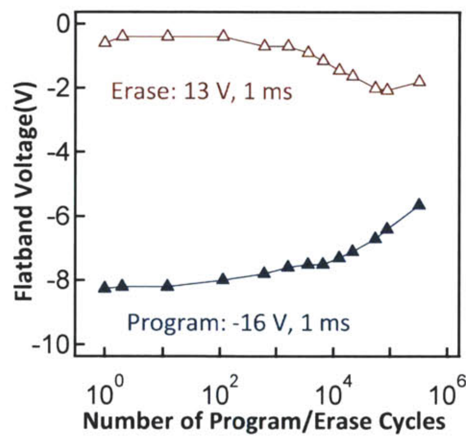


Figure 3-31: Program/Erase endurance characteristics of memory capacitors with 3 nm thick Alq_3 floating gate.

It is expected that the demonstrated endurance and memory characteristics of these devices can be further improved by replacing the sputtered Al_2O_3 layers with high quality Al_2O_3 layer deposited in an atomic-layer deposition (ALD) system.

3.3 Chapter Summary

The use of organic molecular thin film structures as nanostructured charge storage elements in a capacitive floating gate technology was demonstrated in this chapter. What was described surpassed the performance of previously demonstrated quantum dot memories, showing functional use of molecular thin films as nanometer-scale storage elements. The ultra-low electron mobility in molecular thin films and the ability to store charge on individual molecular sites inspires their hybridization with traditional silicon-based memory devices in order to achieve continued memory scaling. Charge retention properties of different molecular films were also investigated as a charge trapping layer using MOS structure. A remarkably high charge storage density of 5.4×10^{13} cm^{-2} using memory capacitors with Alq_3 molecules as the floating was demontrated. This storage capacity significantly exceeds any previously reported capacities for molecular- or quantum dot-based memory devices.

In demonstrating these devices materials were deliberated selected that are compatible with today's memory technology processing, enabling easy insertion of the demonstrated structures into today's microchips. Charge retention of these devices can be further improved by utilizing a higher quality dielectric film, by replacing the sputtered Al_2O_3 layers with a high quality Al_2O_3 layer deposited by an atomic-layer deposition system or by applying a bilayer tunnel dielectric consisting of high-dielectric-constant oxides, such as HfO_2.

Chapter 4

Detection of Charge Storage on Molecular Thin Films by Kelvin Force Microscopy

In this chapter retention and diffusion of charge in tris(8-hydroxyquinoline) aluminum (Alq_3) and Fullerene (C_{60}) molecular thin films is investigated by injecting electrons and holes via a biased conductive atomic force microscopy tip into the molecular films. After the charge injection, Kelvin force microscopy (KFM) measurements revealed minimal changes with time in the spatial extent of the trapped charge domains within Alq_3 films, even for high hole and electron densities of $> 10^{12}$ cm^{-2}. This finding is consistent with the very low mobility of charge carriers in Alq_3 thin films ($<10^{-7}$ cm^{2}V^{-1}s^{-1}), and can benefit the use of Alq_3 films as nano-segmented floating gates in flash memory cells. The spatial distribution of charges is calculated solving the Poisson equation, from which the diffusivity of charges within the molecular thin film layer is calculated. Charge storage within C_{60} molecules is also visualized using KFM. Results show faster charge diffusion within C_{60} molecules which is consistent with the relatively high mobility of C_{60}.

4.1 Tris(8-hydroxyquinoline) aluminum (Alq_3) Molecules

Tris(8-hydroxyquinoline) aluminum (Alq_3) is a stable polar organic semiconductor with average Alq_3-to-Alq_3 molecular site spacing of 0.87 nm that in a monolayer of Alq_3 corresponds to a high molecular density of 1.3×10^{14} cm^{-2} [59]. Although the spacing between Alq_3 molecules is less than one nanometer, their highly localized electron wavefunctions constrain them to act

like separated charge storage nodes.

This material is one of the very first employed in a high efficiency OLED [50], and is today one of the most widely studied organic optoelectronic materials. It is integrated into existing devices in the form of an amorphous thin film, and employed as an electron transporting material (because it transports negative polarons much more efficiently than positive polarons), and as a green light emitting layer (because it has a high photoluminscent quantum efficiency). The chemical formula of Alq_3 is shown in Figure 4-1 (a); it consists of a central aluminum atom bonded to three quinolate ligands. Alq_3 forms two geometric isomers, referred to as the meridinal (mer) and facial (fac) structures having C1 and C3 symmetries, respectively. Numerous experimental and theoretical studies have demonstrated that the mer-Alq_3 form is dominant in an amorphous solid state [63,64]. A ball and stick structure diagram of mer-Alq_3 is shown in Figure 4-1 (b) for the ground state geometry (from [65]).

Many have studied the ground state electronic structure of Alq_3, and computed the associated HOMO and LUMO molecular orbitals. (All of the ab initio calculations reported here are performed assuming classical, stationary nuclei.) Representative molecular orbital surfaces associated with (a) the HOMO and (b) the LUMO are shown in Figure 4-2. These orbitals serve to illustrate, in part, the spatial distribution of the electronic states.

The solid state of Alq_3 can be either amorphous or crystalline. Four different crystals phases have been identified to date: two composed of mer-Alq_3 (α and β), one of fac-Alq_3 (δ), and one that is polymorphic (ϵ) [66, 67, 68]. The structures of the α and β phases are shown in Figure 4-3. Though the crystal phase is not a principle concern in this dissertation, it is worth noting the densities of the purely mer-Alq_3 structures: 1.37 g/cm^3 and 1.42 g/cm^3 for the α and β phases, respectively [66]. In addition, the δ and ϵ phases have densities of 1.42 g/cm^3 and 1.38 g/cm^3, respectively. These crystals yield an average intermolecular spacing of 0.82 nm and 0.81 nm given an Alq_3 molecular weight of 459.4. The α phase crystals were formed by vacuum sublimation in a quartz tube in which the source material was heated and the crystals recondensed on the walls of the tube in a region of the furnace maintained at a lower temperature. The β phase crystals were then formed by a subsequent recrystalization in acetone [50].

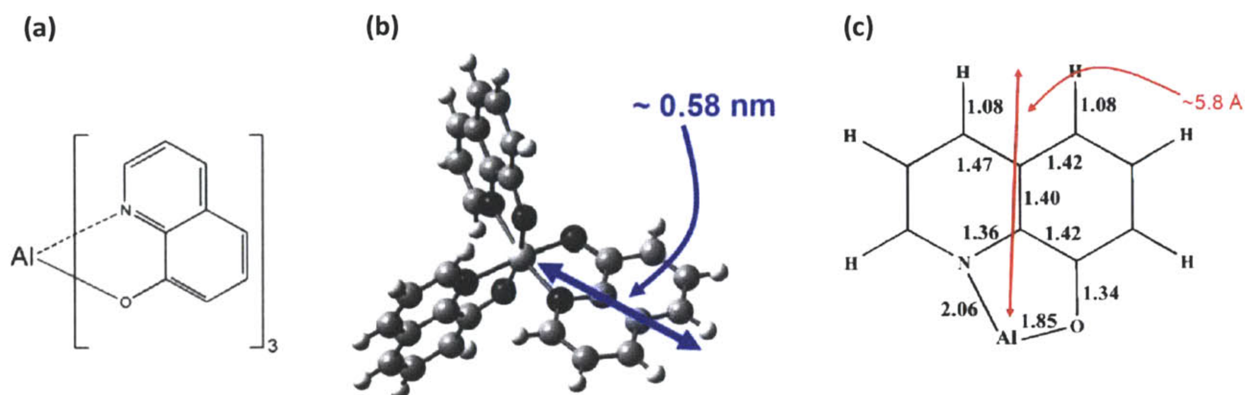


Figure 4-1:(a) The structural formula for Alq_3; (b) The ball and stick representation of the mer-Alq_3 isomer in the ground state ; (c) Diagram of the quinolate ligand of Alq_3 with bond lengths indicated [50].

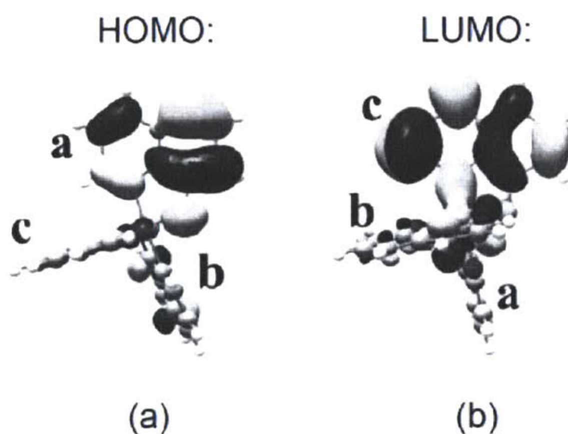


Figure 4-2: HOMO (a) and LUMO (b) of Alq_3 [65].

In contrast, when thin films of Alq_3 are deposited by thermal evaporation in the manner described in the third chapter, the material is completely amorphous. A diffraction analysis of the subsequent material showed no crystalline structure of any kind, even for material deposited at elevated substrate temperatures [66], indicating that in Alq_3, the amorphous phase is remarkably persistent in thin films.

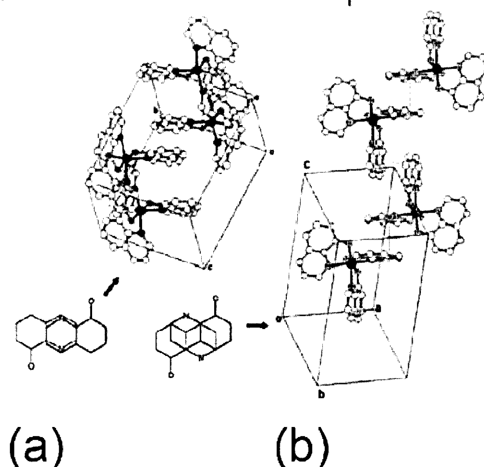


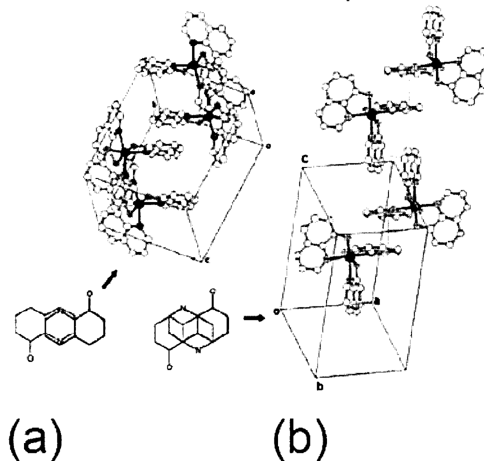
Figure 4-3: Crystal structure of (a) α and (b) β phases of Alq_3. Both phases consist entirely of the mer-isomer. These figures are reproduced from [66].

The density of the deposited Alq_3 layer was 1.16 ± 0.06 g/cm^3. This density yielded an average intermolecular spacing of 0.87 nm.

Alq_3 molecules have previously been reported to exhibit negative differential resistance (NDR) and resistance switching properties; although, devices reported to date have been two-terminal resistive memories, rather than reversible charge-storage elements [69,70].

Memory capacitors using Alq_3 molecules as the floating gate were fabricated and discussed in chapter 3, showing durability over more than 10^4 program/erase cycles and the hysteresis window of up to 7.8 V, corresponding to stored charge densities as high as 5.4×10^{13} cm^{-2}. This finding suggests the potential promising use of molecular films in high storage capacity non-volatile memory cells.

Stored charges within a film of molecules can also be detected from surface potential mapping of the sample by Kelvin force microscopy (KFM) - a scanning probe technique that uses a conductive atomic force microscopy (AFM) tip to measure the spatial extent of charges trapped at the surface of the material. KFM measures the potential of the surface by using a DC feedback voltage to null the electrostatic force between the AFM tip and sample. This force depends on the electrostatic field from the sample, giving us a relative measurement of the trapped charges.



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between the tip and the sample, allowing local static charge domains and charge carrier density to be measured.

The system detects changes in the phase response of the cantilever that are induced by the interaction of the conducting tip and the electrostatic field of the sample surface. EFM images are usually obtained by monitoring the phase change of the cantilever oscillation at the applied frequency.

The KFM probe that is typically held 30–50 nm above the sample is scanned across the surface and the potential is measured. The conducting probe and conducting substrate can be treated as a capacitor with the gap spacing serving as the spacing between probe and sample surface. A dc and ac voltage is applied to the tip (and sometimes the voltage is applied to the sample with the tip held at ground potential). This leads to an oscillating electrostatic force between tip and sample from which the surface potential can be determined.

The frequency is chosen equal or close to the cantilever resonance frequency that is typically around several 100 kHz. If a capacitance *C*, a voltage *V*, and a charge *Q* are considered, the capacitance and energy stored in the capacitor are [83]:

$$C = \frac{Q}{V}; E = \frac{1}{2}CV^2 = \frac{1}{2}\frac{Q^2}{C} \tag{4-1}$$

A voltage across the capacitor leads to an attractive force between the tip and the sample. The relationship between energy and force is [83]:

$$F = \frac{dE}{dz} = -\frac{1}{2}\frac{Q^2}{C^2}\frac{dC}{dz} = -\frac{1}{2}V^2\frac{dC}{dz} \tag{4-2}$$

for constant charge and constant voltage where *z* is the tip-to-sample spacing. The tip potential is [83]

$$V_{tip} = V_{dc} + V_{ac}\sin(\omega t) \tag{4-3}$$

Substituting into Eq. (4-2) gives

$$F = \frac{1}{2}\frac{dC}{dz}\left[(V_{dc} - V_{surf})^2 + \frac{1}{2}V_{ac}^2(1 - \cos(2\omega t)) + 2(V_{dc} - V_{surf})V_{ac}\sin(\omega t)\right]$$

(4-4)

with spectral components at DC:

$$F_{dc} = \frac{1}{2}\frac{dC}{dz}\left[(V_{dc} - V_{surf})^2 + \frac{1}{2}V_{ac}^2\right] \quad (4\text{-}5)$$

and at frequencies ω_{res} and $2\ \omega_{res}$:

$$F_{\omega} = \frac{dC}{dz}\left[(V_{surf} - V_{dc})V_{ac}\right] \quad (4\text{-}6)$$

$$F_{2\omega} = -\frac{1}{4}\frac{dC}{dz}(V_{ac})^2 \quad (4\text{-}7)$$

where V_{surf} is the surface potential. The force between the tip and surface consists of static, first harmonic, and second harmonic components. Using a lock-in amplifier, the F_{ω} component is used as the input to the feedback loop which adjusts V_{dc} to minimize F_{ω}. F_{ω}=0 when V_{dc} is equal to the surface potential V_{surf} under the cantilever. Ideally, the potential feedback loop will minimize the electrostatic forces on the cantilever resulting in an accurate measure of the surface potential.

Static charges can accumulate in few-nanometer-thick films, and KFM can be used to visualize the charge distribution with a horizontal spatial resolution of several tens of nanometers. In general, the spatial resolution is determined by the extension of the electric field from the probing tip. Since the electric field extends over a wider range than the atomic force, the atomic-scale spatial resolution is not easy to achieve in electrical measurements. In next section, charge injection using an AFM tip is discussed.

4.2.2 Contact Mode AFM

Atomic Force Microscopy (AFM) can resolve features as small as an atomic lattice, for either conductive or non-conductive samples. AFM provides high-resolution and three-dimensional

information, with little sample preparation. The technique makes it possible to image *in-situ*, in fluid, under controlled temperature and in other controlled environments. The potential of AFM extends to applications in life science, materials science, electrochemistry, polymer science, biophysics, nanotechnology, and biotechnology.

In AFM, as shown in Figure 4-4, a sharp tip at the free end of a cantilever (the "probe") is brought into contact with the sample surface. The tip interacts with the surface, causing the cantilever to bend. A laser spot is reflected from the cantilever onto a position-sensitive photodiode detector. As the cantilever bends, the laser spot position changes. The resulting signal from the detector is the Deflection, in volts.

The force interaction as the tip approaches the sample is shown in Figure 4-5. At the right side of the curve the tip and sample are separated by large distance. Tip and sample atoms first weakly attract each other as they approach. This zone of interaction is known as the "non-contact" regime. Closer still, in the "intermittent contact" regime, the repulsive van der Waals force predominates. When the distance between tip and sample is just a few angstroms, the forces balance, and the net force drops to zero. When the total force becomes positive (repulsive), the atoms are in the "contact" regime as shown in Figure 4-5.

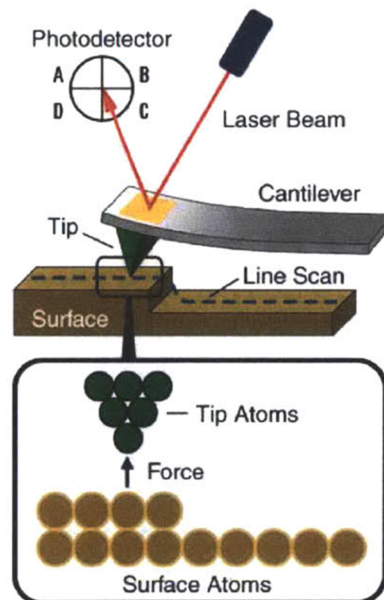


Figure 4-4: Basic AFM principles [82].

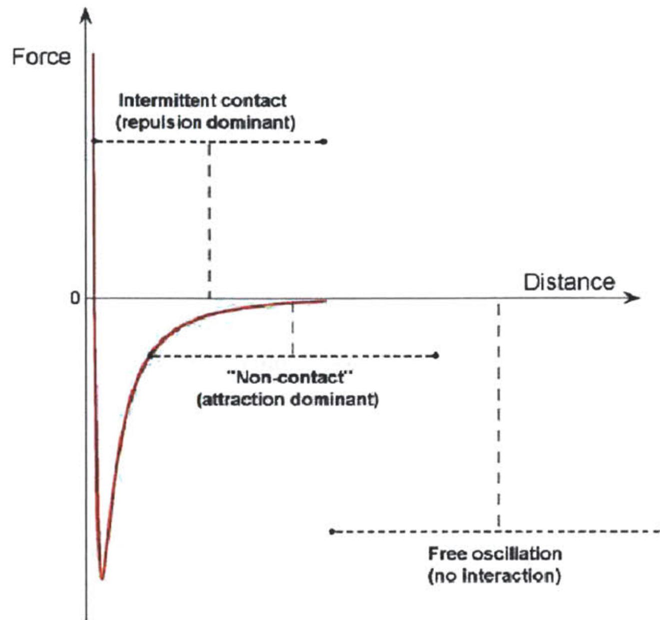


Figure 4-5: Zones of interaction as the tip approaches the sample [82].

In Contact Mode AFM, the AFM tip is attached to the end of a cantilever with a low spring constant (typically 0.001 - 5 nN/nm). The tip makes gentle contact with the sample, exerting from ~0.1-1000 nN force on the sample.

4.2.3 Intermittent Contact AFM

Intermittent Contact Mode AFM is typically referred to as AC Mode due to the alternating contact of the tip to the surface. In AC Mode, the cantilever is driven to oscillate, typically in sinusoidal motion, at or near one of its resonance frequencies. When the cantilever and the sample are close during each oscillation cycle, the tip moves through an interaction potential that includes long-range attractive and short-term repulsive components. The complex tip-sample forces cause changes in the amplitude, phase and resonance frequency of the oscillating cantilever.

Thus, topography, amplitude and phase can be collected simultaneously. The phase and amplitude images may highlight physical properties that are not readily discernible in the

topographic map. For example, fine morphological features are, in general, better distinguished in amplitude and phase images.

The force of the oscillating tip is directed almost entirely in the Z axis; thus, very little lateral force is developed and tip/sample degradation is minimized. This benefit also makes it possible to obtain clear images of soft samples.

A feedback system is employed to maintain the oscillation amplitude at a setpoint value. The difference between the amplitude and set point, called the "error signal," is used as the input to the feedback system. The output of the feedback loop is amplified and drives the Z-actuator. The map of this output signal is called the "Amplitude Image" that is typically plotted side-by-side with the topography image. The topography image is the voltage applied to the piezo required to keep the oscillation amplitude constant multiplied by the sensitivity of the piezo in nanometers/volt.

AC Mode can operate in either the intermittent contact (net repulsive) regime or the non-contact (net attractive) regime. During intermittent contact, the tip is brought close to the sample so that it lightly contacts the surface at the bottom of its travel, causing the oscillation amplitude to drop.

The tip is usually driven by a sinusoidal force, with the drive frequency typically at or near one of the cantilever's resonance frequencies (eigenfrequencies), and most often at the fundamental frequency. The cantilever oscillations are also sinusoidal if the drive amplitude is small enough to keep the cantilever motion small compared with the cantilever thickness, absent any tip-sample interactions.

AFM is an attractive surface analysis tool due to the simplicity of its use and no special requirements on sample preparation. AFM was used both for study the morphology of the layers and also for charge injection in order to visualize charge storage within molecules in this dissertation.

4.3 Direct Detection of Charge Storage within Alq_3 Molecules

It was demonstrated in this work that it is possible to store record-high charge densities per unit area in nano-segmented floating gates consisting of molecular thin films. By directly imaging the stored charge as a function of time, very low charge mobility in molecular films is demonstrated to inhibit charge diffusion between molecular sites, thus functioning as an effective nano-segmented floating gate.

The low charge mobility in molecular organic materials creates a situation that enables their hybridization with traditional silicon-based memory devices in order to achieve continued memory scaling. As shown in chapter 3, a floating gate consisting of a thin film of molecules can provide several-fold higher density of charge-storage sites than even the SONOS devices. The low density of free carriers in molecular thin films and the high charge binding energy of individual molecules limit intermolecular interactions. The minimal overlap of electron wavefunctions between neighboring molecules contributes to the low thin film electron/hole mobility typically observed in organic molecules, in the range of 10^{-4} to 10^{-9} $cm^2V^{-1}s^{-1}$. The low mobility contributes to the immunity of stored charge to structural defects present in neighboring areas of the device.

Stored charges within a film of molecules can be detected from surface potential mapping of the sample by KFM as a scanning probe technique that uses a conductive atomic force microscopy (AFM) tip to measure the spatial extent of charges trapped at the surface of the material.

4.3.1 Sample Preparation

A 5 nm thick layer of pre-purified (by thermal-gradient sublimation) Alq_3 was deposited onto 4 nm thick thermal SiO_2 grown on a highly doped n-type Si substrate (Figure 4-6) in order to study the charge storage behavior of Alq_3 films. Wafer cleaning was accomplished by immersing cassettes of wafers into cleaning baths containing SC-1 solution (1:1:5 $NH_4OH/H_2O_2/H_2O$) for

striping organics, metals and particles, 50:1 H_2O/HF for removing the chemical oxide layers that are grown during the first step, and SC-2 solution (1:1:6 HCL/H_2O_2/H_2O) for striping alkali ions and metals. The wafers were rinsed with DI H_2O before and after the HF step and also after the last step.

4 nm thick layer of thermal SiO_2 was grown at 800 °C in dry O_2 on top of a cleaned Si substrate. The organic layer was thermally evaporated in vacuum, at a rate of (0.15 ± 0.05) nm/s and base pressure of $<6\times10^{-7}$ Torr.

The morphology of the layers is crucial for the device performance. The Alq_3 surface analysis

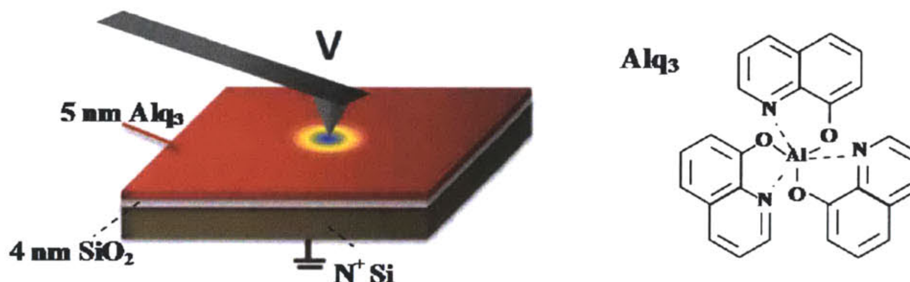


Figure 4-6: Chemical structure of tris (8-hydroxyquinoline) aluminum (Alq_3) molecules and a schematic of the Kelvin force microscopy (KFM) measurements.

with AFM is shown in Figure 4-7. The root mean square roughness of the layer is 0.10 nm, indicating that the deposited organic layer is quite smooth with amorphous structure.

4.3.2 Charge Injection

For charge storage study, electrons/holes were injected under ambient conditions by applying negative/positive bias to the AFM tip (Pt probe tip with 15nm tip radius) in contact with the organic layer while the Si substrate is grounded. During the charge injection period the tip was brought into contact with the sample surface and maintained at a specific location. Following the charging, surface potential changes were monitored by scanning the surface in the KFM mode. All charge injection and KFM imaging was performed on a Agilent 5500.

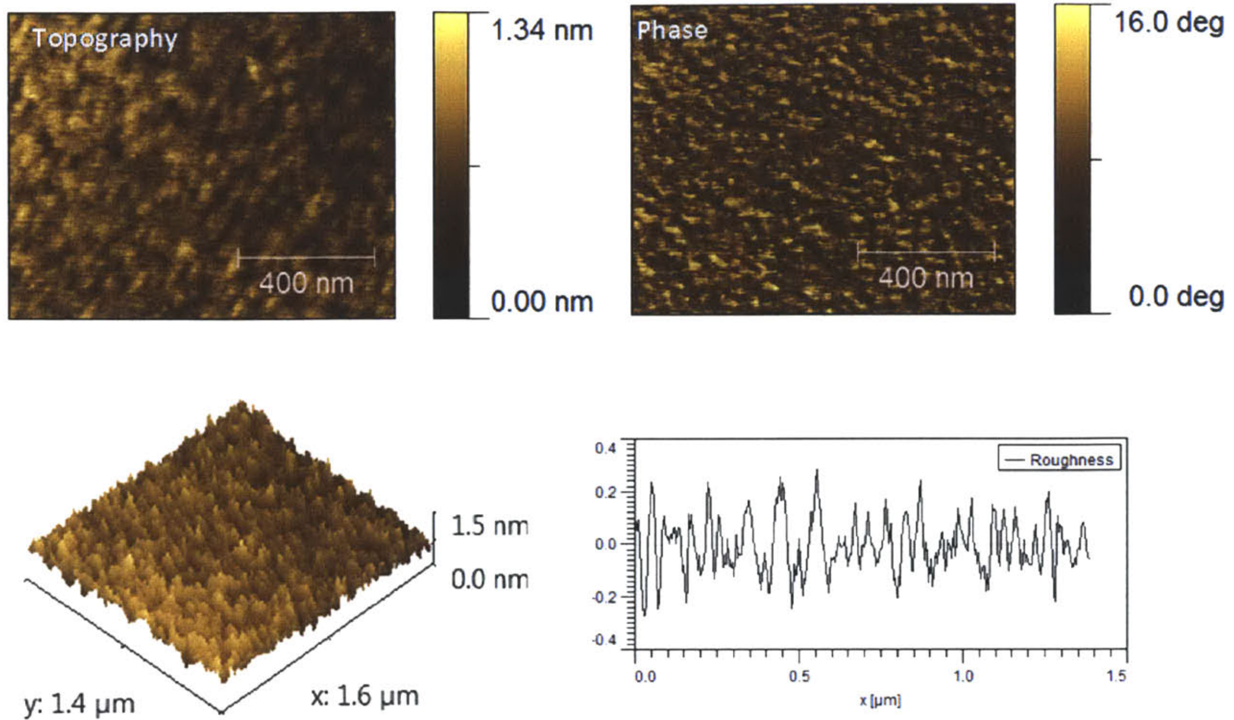


Figure 4-7: AFM topography and phase images of 5 nm-thick layer of Alq_3, deposited on top of a 4-nm thick layer of thermal SiO_2.

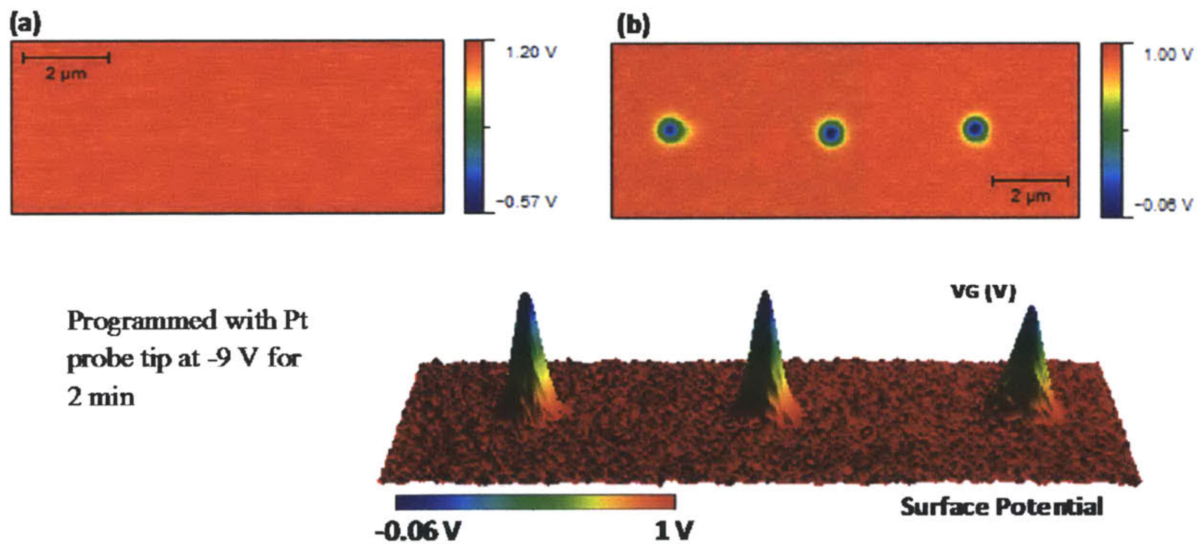


Figure 4-8: KFM image of the (a) layer before charge injection; (b) charged spots created by applying -9 V to the AFM tip in contact with the Alq_3 layer.

The surface potential of the surface before charge injection is shown in Figure 4-8 (a). The 2D

and 3D KFM image of an array of dots written by electrons injected from AFM tip biased at -9 V can be seen this figure. The KFM image of two spots on an Alq_3 film sample charged with either electrons or holes by applying -9 V and 9 V tip bias are shown in this figure.

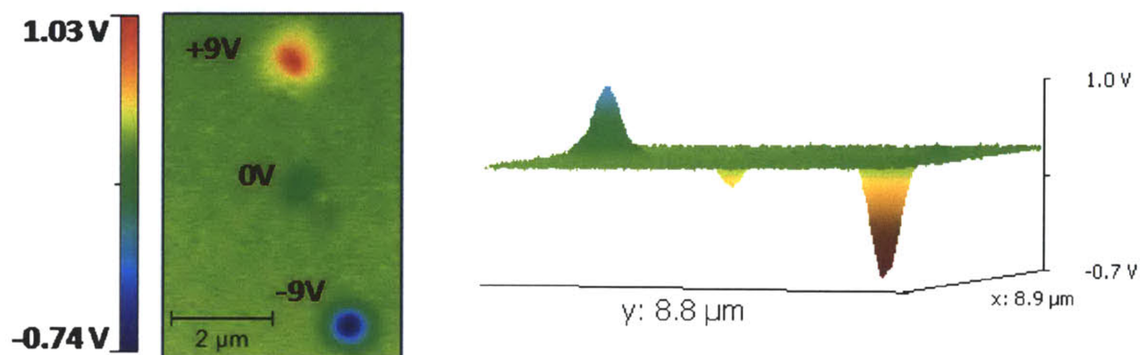


Figure 4-9: KFM image of positively and negatively charged areas written into a 5-nm-thick Alq_3 layer on top of a 6 nm-thick silicon dioxide layer on n+ silicon wafer. Color scale of the measured KFM potentials is indicated in the figure together with the programming voltage for each charged area.

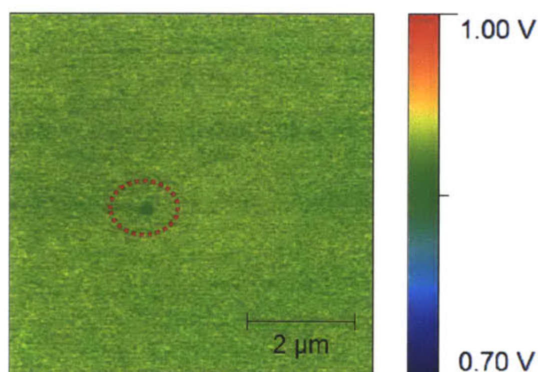


Figure 4-10: KFM image of a sample without organic layer (Si/SiO_2). The area shown with the dashed circuit shows the spot where the tip was brought in contact with the surface. -9 V bias was applied to the tip for 2 min.

By applying large charging bias to the tip, dots of both positive and negative charge can be written as shown in Figure 4-9. The area of the charge spot is larger than the contact area between the tip and the sample. This spreading is induced by the radial component of the electric field generated by the AFM tip. Differences in the KFM-recorded potential indicate surface charging. No significant change in the surface potential was observed for the reference spot formed by bringing the tip into contact with the surface and applying 0 V.

The surface potential image of a control sample with 4-nm of the thermal SiO_2, without organic layer is shown in Figure 4-10.

By Applying 9 V bias to the tip no significant change in the surface potential was observed confirming that bulk of charge retention is in the molecular floating-gate film rather than the oxide layer. The absolute value of the maximum surface potentials of charged spots versus negative tip biases, each applied for 10 seconds has been plotted in Figure 4-11. The height of the peak is a linear function of programming voltage.

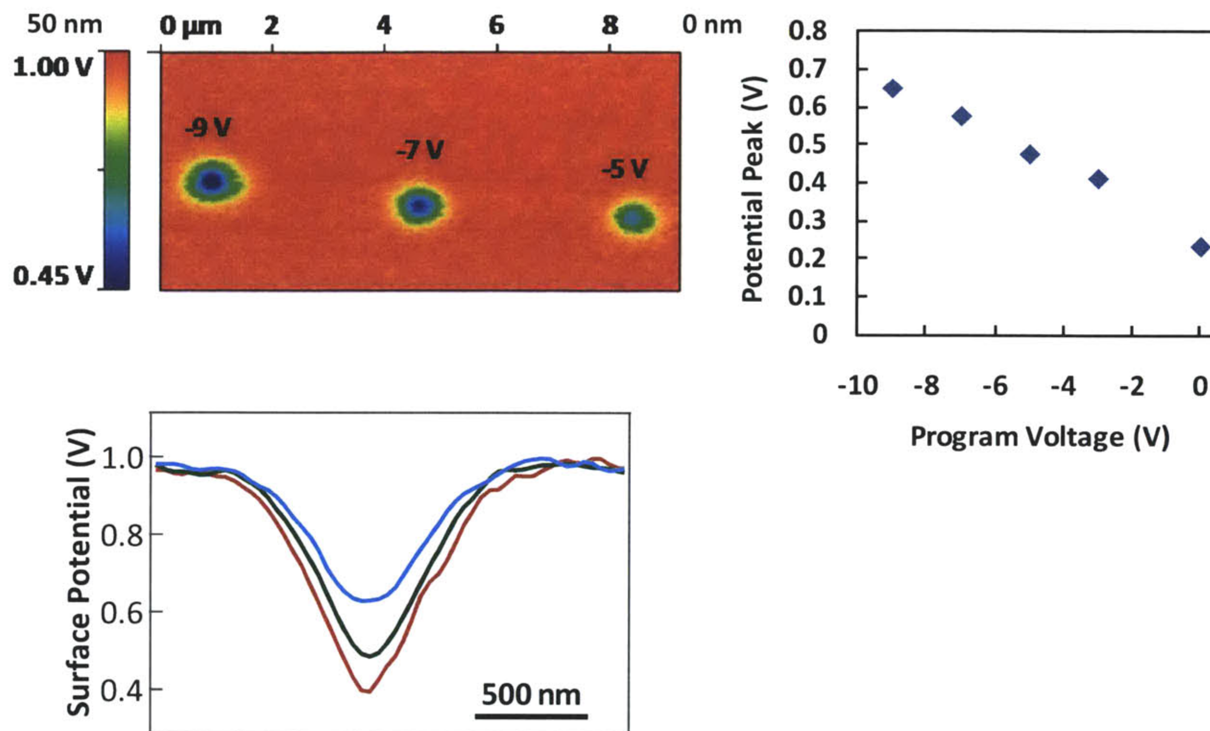


Figure 4-11: Dependence of the amount of stored charge on tip bias (a) KFM image of charged spots created by applying different tip biases (the tip was brought into contact with the surface for 10 sec) and surface potential profiles along the line crossing the center of the spots; and (b) Potential peak and charged area at half maximum of the charged spots versus injection time; -9 V was applied to the tip during charge injection. The results revealed the increased area and maximum value for longer charging times.

The amount of injected charge can also be controlled by the programming time as shown in Figure 4-12.

The potential peak and area of the charged spot as a function of injection time for -9 V tip-to-substrate voltage was plotted in Figure 4-12b, revealing the increase in both the charged area and peak potential value for longer charging times.

4.3.3 Charge Spreading within the Alq_3 Molecular Layer

Strong confinement of stored charges is necessary in order to inhibit charge migration towards existing defects in the thin oxide layers and to minimize memory window variations in floating

gate memory devices. Accordingly, low charge mobility within the floating gate is desirable. At room temperature, the hole mobility in Alq_3 has a value between 10^{-9} and 10^{-8} $cm^2V^{-1}s^{-1}$ that is at least two orders of magnitude less than electron mobility under identical preparation and measurement conditions [84]. Therefore, holes stored in a floating gate should be more localized than electrons. This is consistent with the measurement of charge diffusion in the Alq_3 film by KFM imaging the time-dependent change in the stored charge distribution.

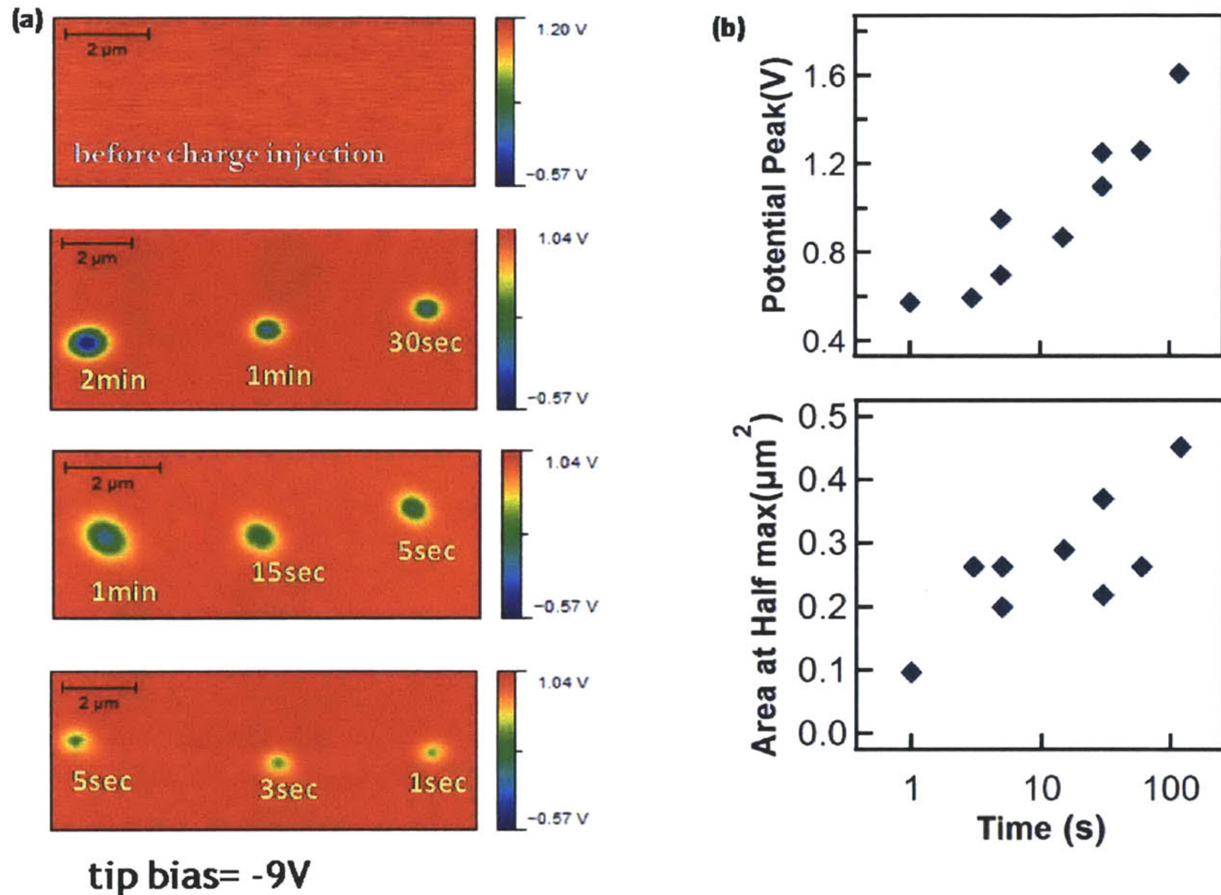


Figure 4-12: (a) KFM image of charged spots created by applying -9 V to the AFM tip in contact with the Alq_3 layer for different lengths of time; (b) KFM measurements of the peak potential and the charged area at half maximum, plotted as a function of the injection time.

Charge dots were written and monitored over time to examine the time evolution of stored charge in the system, as seen in Figure 4-13 and 4-14.

KFM imaging of the lateral spreading of charges in the Alq_3 films in Figure 4-13 shows

changes in both the maximum surface potential and in the area of the charged spots at half maximum as a function of time.

Two hours after the charge injection the spots charged with electrons show a (20±2)% decrease in the potential peak and (19±0.3)% increase in the spot size, while spots charged with holes show only (11±2)% decrease in the potential peak and (4±0.3)% increase in the spot size, as shown in Figure 14. This finding is consistent with the lower mobility of holes in Alq_3 films.

Surface potential profiles across a line passing through the maximum of the charged spots are shown as insets in Figures 4-14 (a) and (b).

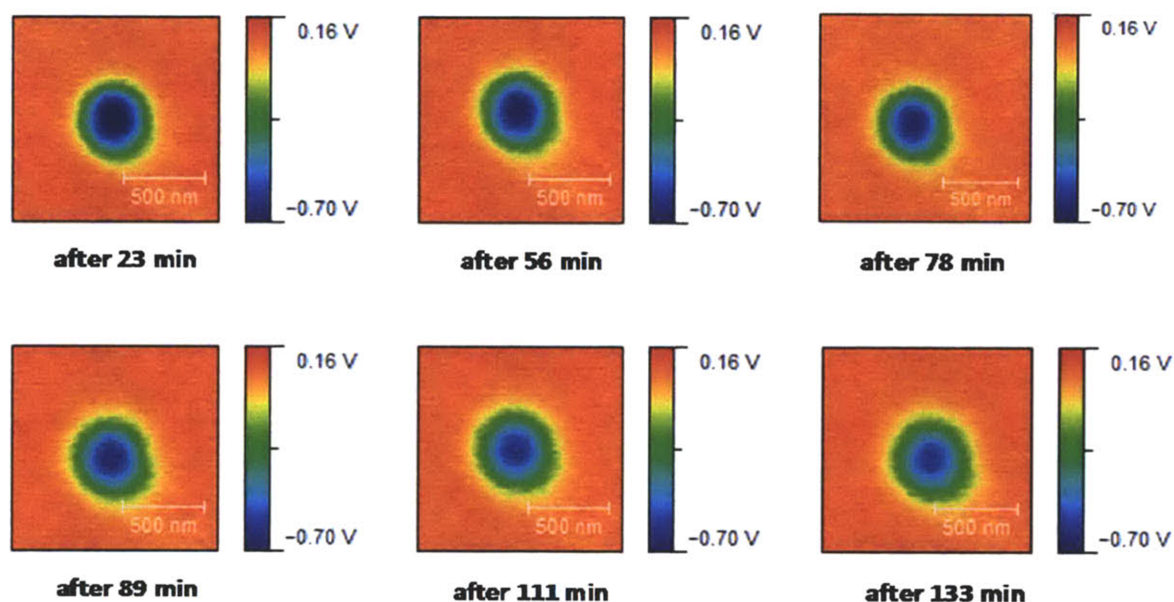


Figure 4-13: KFM images of the negatively charged spots over time illustrating the spreading and net decrease in the surface potential change and consequently the stored charges within molecules.

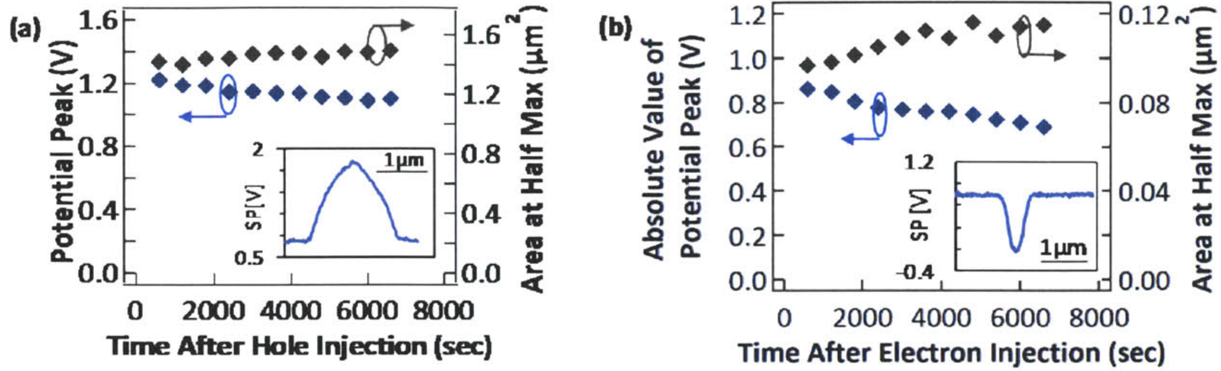


Figure 4-14: Evolution of the potential peak and area of the spot at half maximum extracted from 2D map of the measured surface potential; holes are more localized than electrons (lateral hole mobility is $5\times10^{-9}\,cm^2V^{-1}s^{-1}$).

4.3.4 Calculation of Stored Charge Density

The measured surface potential is related to the spatial distribution of charges that can be calculated by solving the Poisson equation and calculating the surface charge density on the silicon substrate, σ_{si}, using ψ_{si}, the electrical potential at the silicon surface [61].

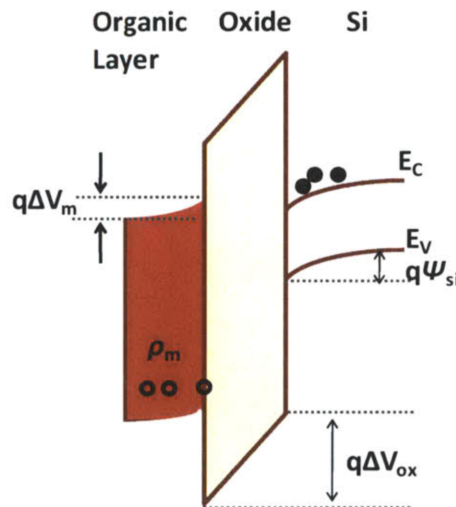


Figure 4-15: Schematic band diagram of the $Alq_3/SiO_2/n^+Si$ structure.

As shown in the schematic diagram of Figure 4-15, the measured surface potential (*SP*) can be obtained based by applying the Gauss's law as

$$SP = \psi_{si} + \Delta V_m + \Delta V_{ox} = \psi_{si} + \rho_m d_m \left(\frac{d_m}{2\varepsilon_m} + \frac{d_{ox}}{\varepsilon_{ox}}\right) \tag{4-8}$$

where d_m, d_{ox}, ε_m and ε_{ox} indicate the thickness and permittivity of the molecular and oxide layers, respectively. Ellipsometry measurements of thermally deposited Alq_3 thin films yield a refractive index of n=1.67 that corresponds with a [50, 85] relative permittivity of $\varepsilon_{rm} \approx n^2 = 2.79$. ρ_m is the trapped charge density (in units of traps.cm^{-3}) in the molecular layer. The relation between ψ_{si} and surface charge density can be obtained from the one-dimensional Poisson equation.

$$\sigma_{si}(\psi_{si}) = \mp \frac{\sqrt{2}\varepsilon_{si}}{\beta L_D} \left\{ \left[\exp(-\beta\psi_{si}) + \beta\psi_{si} - 1\right] + \frac{n_{po}}{p_{po}} \left[\exp(\beta\psi_{si}) - \beta\psi_{si} - 1\right] \right\}^{1/2} \tag{4-9}$$

where ε_{si} is the permittivity of silicon, n_{po} and p_{po} are the equilibrium densities of electrons and holes in the bulk of silicon, $\beta = q/k_B T$ (q is the electronic charge and k_B is Boltzmann's constant), and $L_D = \sqrt{\varepsilon_{si} / q p_{po} \beta}$ is the extrinsic Debye length for holes.

Assuming uniform distribution of charge across the thickness of the trapping layer and neglecting interface charges, σ_{si} is related to trapped charge density in the organic layer as

$$\sigma_{si} = \int \rho_{si} dz = -\int \rho_m dz = -\rho_m d_m \tag{4-10}$$

Hence, combining (4-9) and (4-10), ψ_{si} in (4-8) can be expressed as a function of ρ_m. By solving (1), $\rho_m d$, the surface trapped charge density can be calculated from the measured surface potential.

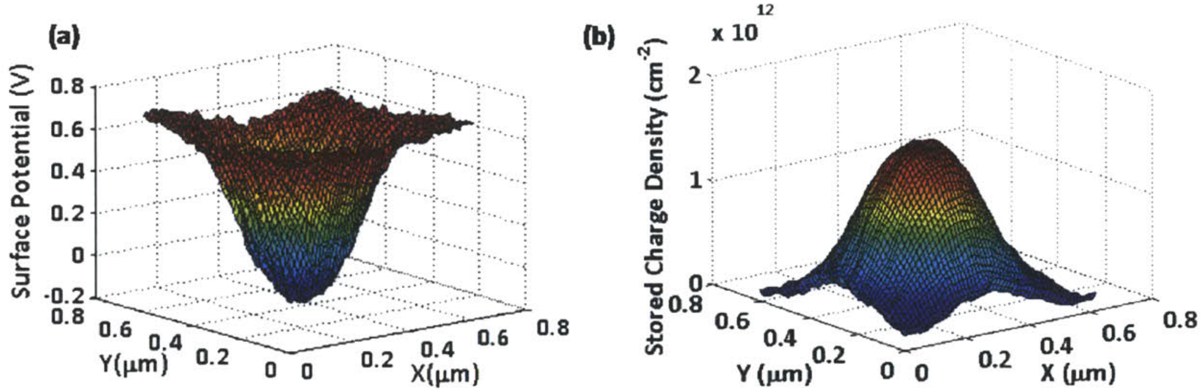


Figure 4-16: (a) Surface potential of a spot charged with electrons; (b) The calculated related spatial charge distribution by solving the relevant Poisson equation. Maximum stored charge densities of 2.7×10^{12} cm^{-2} and 1.9×10^{12} cm^{-2} were calculated for holes and electrons, respectively.

The calculated spatial distribution of stored electrons is shown in Figure 4-16. Maximum stored hole and electron densities of 2.7×10^{12} cm^{-2} and 1.9×10^{12} cm^{-2}, respectively, were calculated.

4.3.5 Evolution of Stored Charge Density

The evolution of the calculated maximum stored charge density is shown in Figure 4-17. The charge decay is well described by exponential fits with relatively long [86-90] characteristic decay times. During the first hour an exponential fit to the stored holes decay exhibited a time constant of $\tau\sim$ 9.26 h, after which the rate of decay slowed down considerably to $\tau\sim$ 388 h. The observed decay in addition to charge diffusion can be caused by charge loss through the tunnel oxide and also discharge due to environmental moisture.

Electrons showed much faster charge decay. During the first hour an exponential fit to the stored holes decay exhibits a time constant of $\tau\sim$ 5.5 h, after which the rate of decay slowed a little bit to $\tau\sim$ 6.9 h.

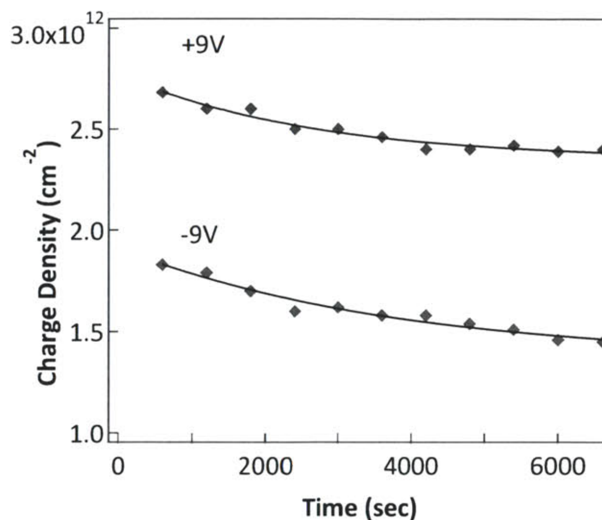


Figure 4-17: Evolution of the calculated maximum stored charge density. Symbols are experimental data and the solid lines are fitted curves.

Holes mobility is smaller than electron mobility because holes are trapped more than electrons. This is unusual for organic semiconductors because electron mobility is normally *smaller* than those of holes [91]. A number of theoretical studies have sought to explain this behavior in terms of the molecular properties of Alq_3. Holes within Alq_3 molecules experience greater energetic disorder than electrons: $\langle \Delta\varepsilon_{if} \rangle$ are 208 meV and 197 meV for holes and electrons, respectively [91]. This can be explained based on the frontier orbitals of Alq_3, shown in Figure 4-19. The HOMO is more localized than the LUMO, sitting on just one ligand rather than two.

As a result, the HOMO-HOMO interaction between two molecules will depend more sensitively on their orientation relative to each other, resulting in a wider spread of J_{if} (electronic coupling) and $\Delta\varepsilon_{if}$ for holes.

The wider distribution of $\Delta\varepsilon$ means that holes experience steeper energetic gradients than electrons do. In turn, this means that holes are trapped more often than electrons, in one of two ways. Firstly, trapping may occur on a single molecule, where $\Delta\varepsilon$ is large and positive for all possible outward hops. Having landed on one of these molecules, the hole will take a very long time to leave (the hopping rate is small).

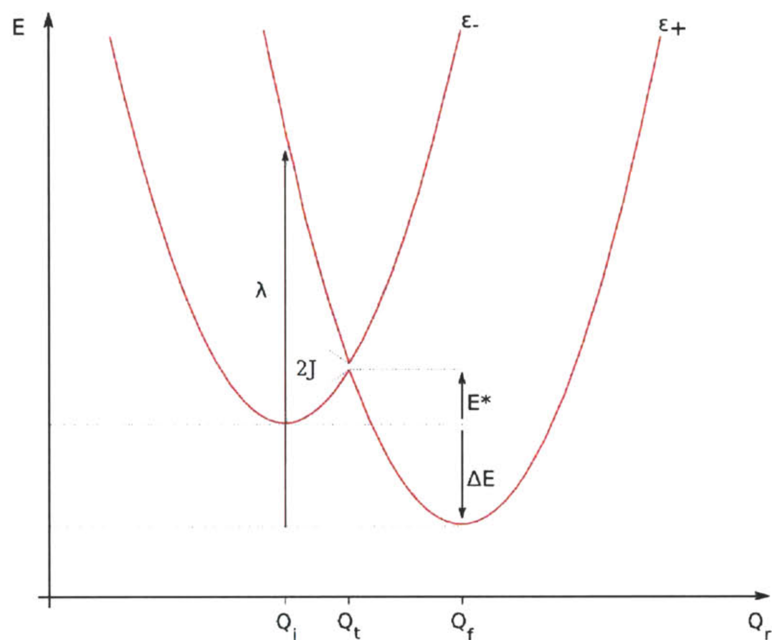


Figure 4-18: The potential energy of 2 molecules (M_1 and M_2) are shown as a function of nuclear coordinates, where the complex multi-dimensional rearrangement of M_1 and M_2 has been reduced to the one-dimensional 'reaction coordinate' Qr [91].

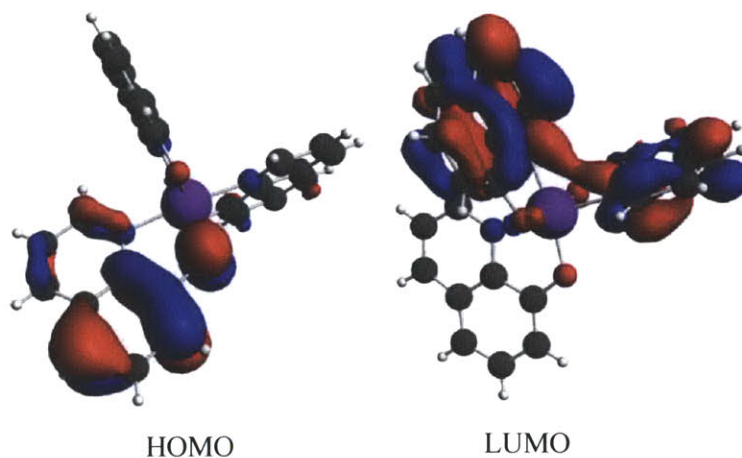


Figure 4-19: The frontier orbitals of Alq_3 [91].

Secondly, and similarly, a hole may be trapped on a small group of molecules when there are small energetic gradients between them ($\Delta\varepsilon \sim 0$), but steep, positive gradients to other molecules $\Delta\varepsilon > 0$.

In this case, the hole moves rapidly around this group of molecules, but very rarely escapes to other molecules. Holes have to hop about ten times more than electrons before they are collected because of trapping on groups of molecules.

4.3.6 Charge Diffusion within Alq_3 Molecule s

The calculated stored charge density in Figure 4-16 has an axial symmetry shape and has a Gaussian type profile.

Figure 4-20 shows the stored charge density (shown by discrete dots) well described by a Gaussian profile:

$$Q(x,y,t_0) = \beta(t_0) \,.\, e^{-\frac{((x-x_0)^2+(y-y_0)^2)}{\alpha(t_0)}} \qquad (4\text{-}11)$$

where α and β are a function of time as shown in Figure 4-21. The two-dimensional diffusion equation in Cartesian coordinates is defined as:

$$\nabla^2 P - \frac{1}{D}\frac{\partial P}{\partial t} = 0 \rightarrow \frac{\partial^2 P}{\partial x^2} + \frac{\partial^2 P}{\partial y^2} - \frac{1}{D}\frac{\partial P}{\partial t} = 0 \qquad (4\text{-}12)$$

where P is the charge density and D is the diffusion constant.

The solution to the 2D isotropic diffusion equation is:

$$P(x,y,t) = \frac{1}{\sqrt{4\pi D t}}\, exp\left(-\frac{x^2+y^2}{4Dt}\right) \qquad (4\text{-}13)$$

β is nearly linear and the diffusivity constant of $D_e \sim 3.6\times10^{-11}$ $cm^2.s^{-1}$ can be approximated from the slope of the fitted linear curve and (4-12), as shown in Figure 4-21.

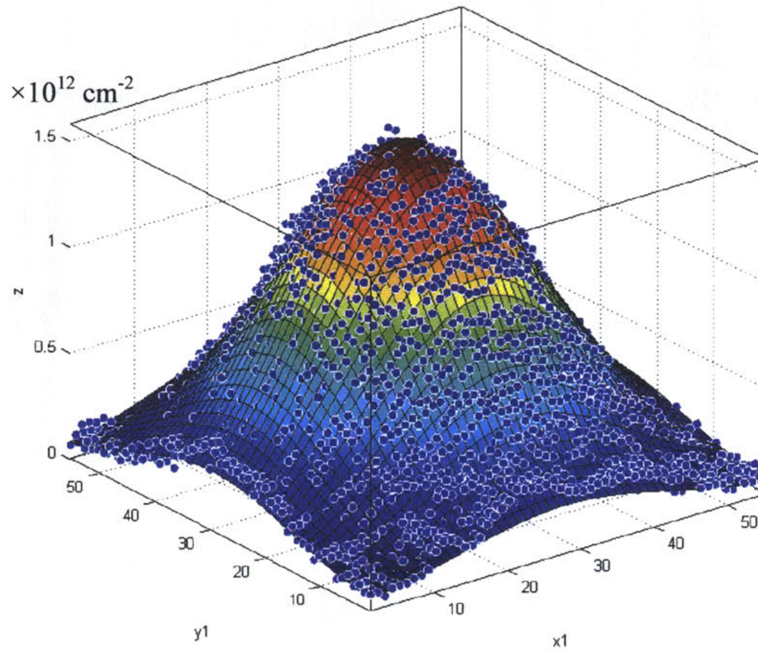


Figure 4-20: Describing the stored charge density by fitting a Gaussian profile to the calculated stored charge density from the surface potential.

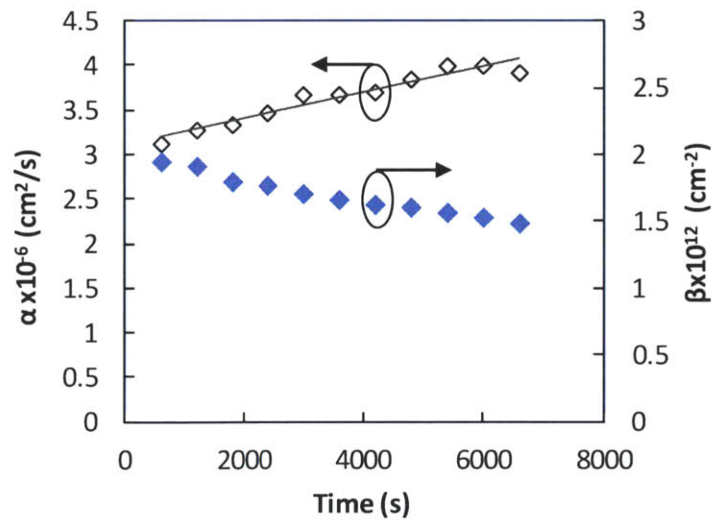


Figure 4-21: The coefficient of the Gaussian profile vs. time.

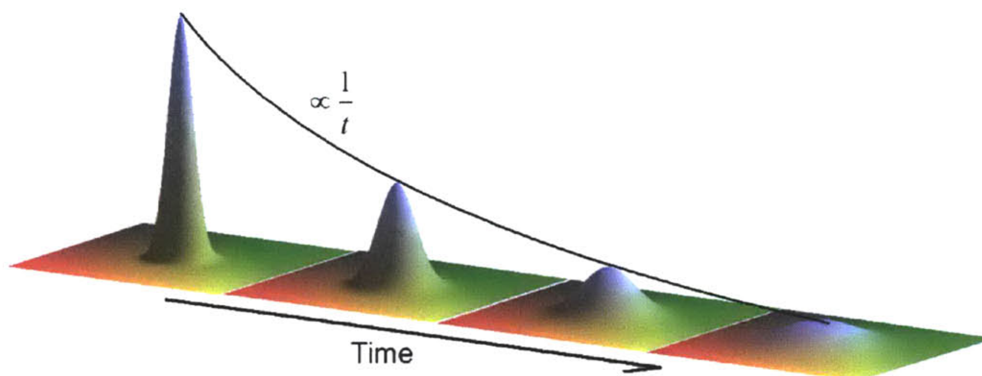


Figure 4-22: Schematic diagram of charges diffusion from their original entry point with time.

It should be noted that charge diffusion is not the only reason for charge decay. The integral of the stored charge density represents the total amount of injected charges. The decrease in the amount of the total stored charges is indicative of charge loss through tunneling into the substrate or possible discharge due to moisture.

4.4 Charge Storage on C_{60} Molecules

The name "Fullerene" is now describes all close cage forms of pure carbon having from 20 to 1,000,000 and more (nanotubes) carbon atoms. This is the largest stable single element molecule. The C_{60} molecule includes 60 carbon atoms arranged as a 3D football structure with 90 edges, 12 pentagons, and 20 hexagons. C_{60} molecules together with the other members of fullerene family represent the purest form of carbon known, not presenting any dangling bonds for interaction with the surroundings, unlike graphite and diamond, the other known forms of carbon. The diameter of the molecule, measured through the carbon nuclei, is about 7 Å [56, 57].

Each carbon atom has two single bonds (C-C) along adjacent sides of a pentagon and one double bond (C = C) between two adjacent hexagons [92] (Figure 4-24). Two different C-C bonds lengths exist in C_{60}, 1.4 Å and 1.46 Å, the length difference causes the π electrons not to be delocalized evenly over all bonds [93]. This distortion, called "Peierls distortion", corresponding to long-short-long-short alternation bonds of high and low π electron density,

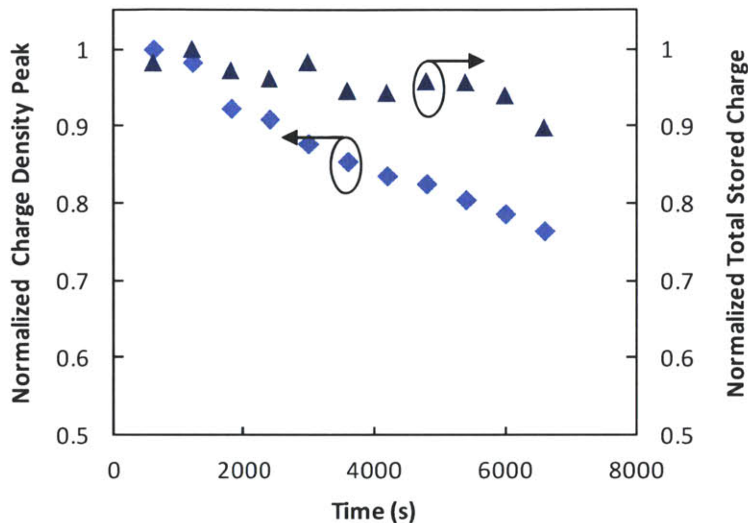


Figure 4-23: Time evolution of the maximum stored charge density and the integral of the stored charge density of the charged spots under ambient conditions.

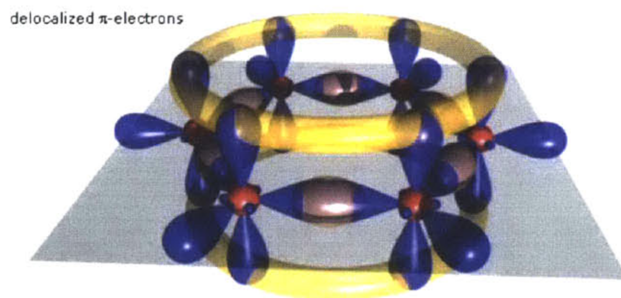


Figure 4-24: Ring of six carbon atoms creating the benzene ring. The σ (blue grey) and π bonds (yellow) are shown [57].

reduce the lattice symmetric, and cause an appearance of an energy gap at the Fermi level.

Each C_{60} atom, arranged in SP_2 form, has three σ bonds (C – C) to its neighbors, using up to total of 180 electrons. As mentioned before, these σ bonds define the structure of the molecule and have energy levels well below the Fermi level [94].

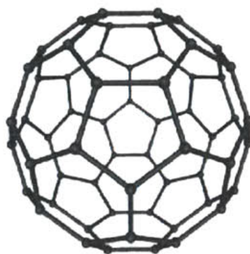


Figure 4-25: C_{60} molecule with 60 carbon atoms.

These bonds do not influence the electric properties. The remaining 60 electrons are distributed across the C_{60} molecule on the π bonds orbital. Not like 2D SP_2 structure, the π electrons in C_{60} molecule tend to spend less time inside the ball compare to the outside of the C_{60} ball. In addition, because of the non-uniform σ bonds length, the π electrons are not truly "delocalized" around the six carbon members of the hexagons ring (as in the benzene ring), but they are distributed over 30 sites of electrons orbits that stick out of the C_{60} molecule.

The C_{60} molecule has 60 orbital with different levels of degeneracy energy in which 30 lower orbital are filled with 60 π electrons. In this case, Hu level is completely filled by the 10 highest energy electrons, becoming the highest occupied molecular orbit (HOMO); while the next energy level, t1u, becomes the lowest unoccupied molecular orbit (LUMO). This molecular orbit can be partially or fully filled by injecting electrons to the C_{60} molecule; attracting up to six electrons to completely fill the LUMO.

Figure 4-26: The increase in symmetry of frontier orbitals is associated with an increase in charge mobility [91].

The symmetry of the C_{60} molecule means that $\Delta\varepsilon \sim 0$. The high symmetry of the C_{60} molecule means that the mobility is surprisingly high, even when the morphology is apparently disordered to the eye [91]. As a result, even in C_{60} film with very small crystalline grains, charge mobility is high.

4.4.1 Visualization of Charge Storage in C_{60} Molecules by KFM

4.4.1.1 Sample Preparation

In order to study the charge storage behavior of C_{60} film, a 5 nm thick layer of pre-purified (by thermal-gradient sublimation) C_{60} is deposited onto 4 nm thick thermal SiO_2 grown on a cleaned highly doped n-type Si substrate. Atomic force microscope characterization of the C_{60} layer on top of the SiO_2 layer is shown in Figure 4-27. The AFM image reveals a small root mean square roughness of less than 0.7 nm.

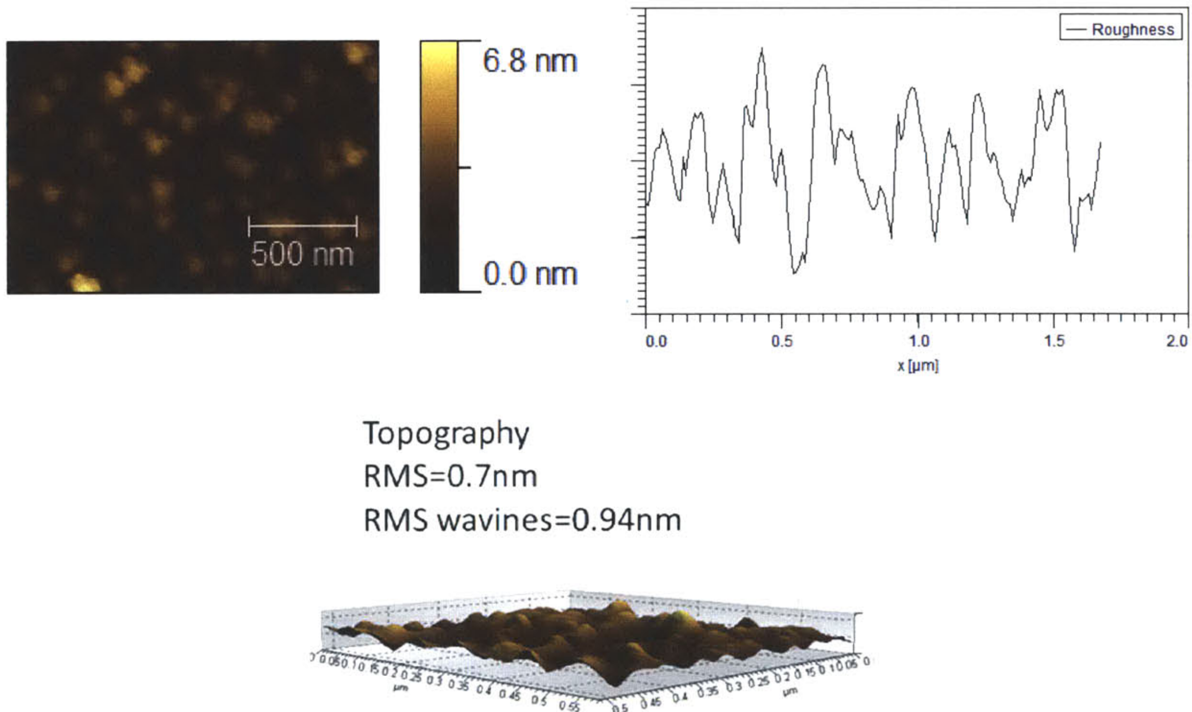


Figure 4-27: AFM topography and phase images of 5 nm-thick layer of C_{60}, deposited on top of a 4-nm thick layer of thermal SiO_2.

Scanning probe studies were performed at room temperature under ambient conditions with a gold coated tip. Sample charging was achieved using a contact mode operation by holding the tip in contact with the surface for 1 min while a bias voltage applied to the tip and the sample was grounded, causing carriers to tunnel between the tip and C_{60} layer. KFM was applied to image charged regions. (see Figure 4-28)

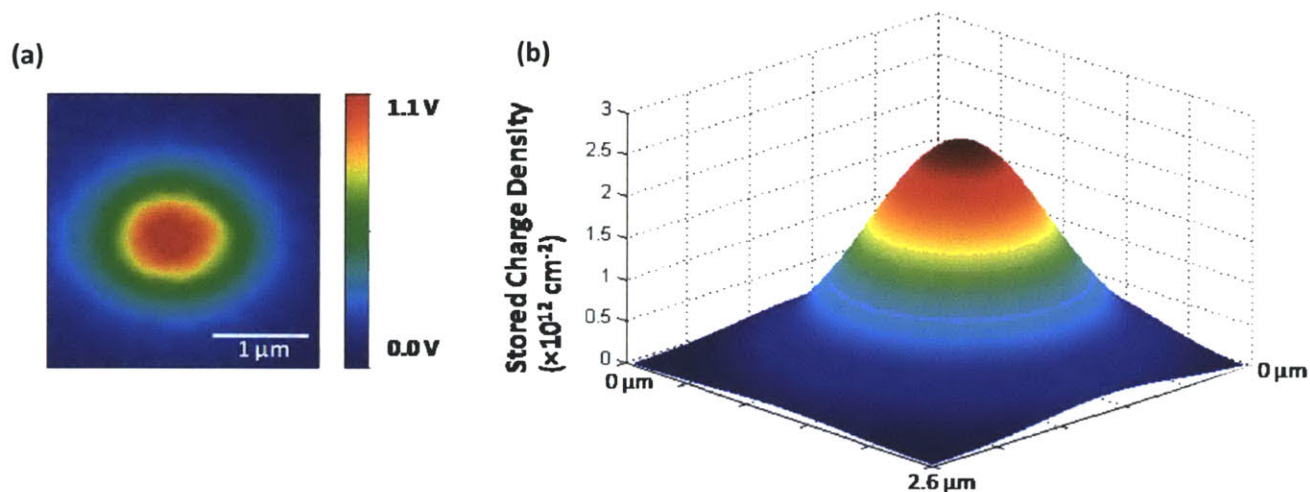


Figure 4-28: (a) The KFM image of a charged spot with holes; (b) Calculated stored charge density from the surface potential.

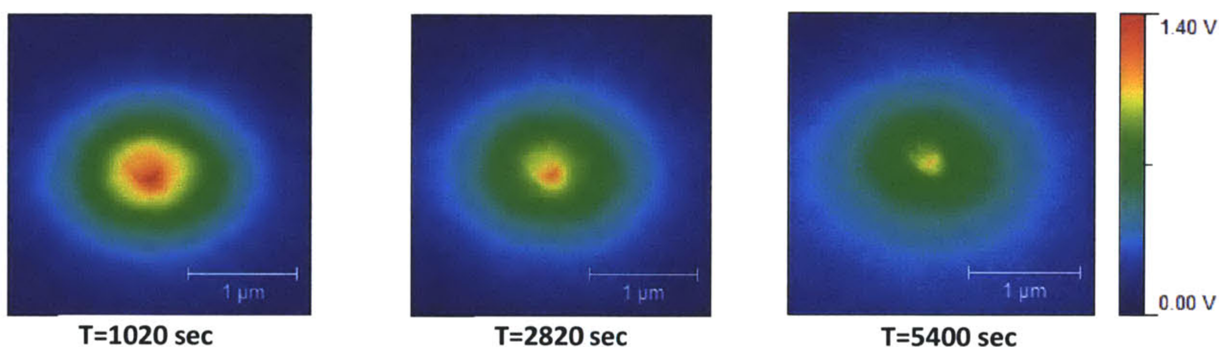


Figure 4-29: KFM images of the positively charged spots over time illustrating the spreading and net decrease in the surface potential change and consequently the stored charges within molecules.

The charge decay is well described by exponential fits with relatively short characteristic decay times of $\tau\sim$ 4 h for positively charged spots. Faster charge decay was observed for these samples due to higher mobility of C_{60} compared with KFM results for Alq_3 as expected. It

should be noted that the measurement was done in atmosphere. It is reported that C_{60} exposure to oxygen reduces the charge mobility within C_{60}.

The mobility of C_{60} molecules will be analyzed in the next chapter using FET structure investigating how it is possible to reduce the mobility within C_{60} molecules by adding dopant molecules.

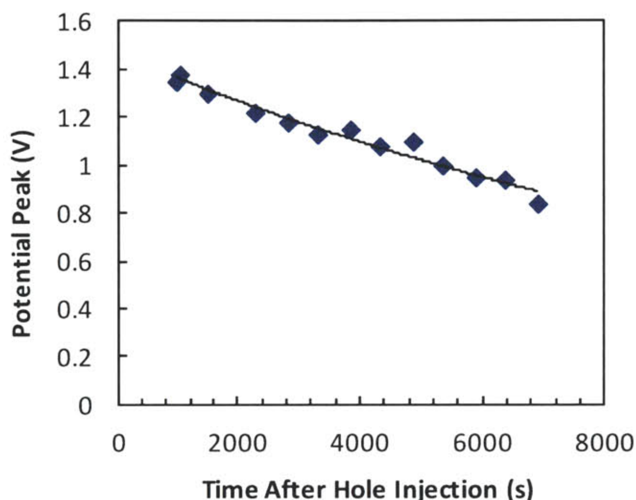


Figure 4-30: The variation of potential peak with time for a positively charged spot.

4.5 Chapter Summary

Retention and diffusion of charge in tris(8-hydroxyquinoline) aluminum (Alq_3) molecular thin film was investigated by injecting electrons and holes via a biased conductive atomic force microscopy tip into the Alq_3 film. After the charge injection, Kelvin force microscopy (KFM) measurements revealed minimal changes with time in the spatial extent of the trapped charge domains within Alq_3 film, even for high hole and electron densities of $> 10^{12}$ cm^{-2}, This finding is consistent with the very low mobility of charge carriers in Alq_3 thin film ($<10^{-7}$ $cm^2V^{-1}s^{-1}$), and can add value to the use of Alq_3 film as nano-segmented floating gates in flash memory cells. Charge storage within C_{60} molecules was visualized using KFM.

Chapter 5

Adjusting the Memory Properties of the Molecules

Data shows that charge retention is improved for molecular films with lower carrier mobility (4) confirming that in a coherent material set, inhibiting charge transport by nano-segmented floating-gate structures enhances memory retention (Figure 3-19). Among the tested materials, C_{60} containing memories showed the largest hysteresis window and better endurance. However, the high mobility and resultant low retention time of C_{60} memory devices compromises their otherwise remarkable memory characteristics.

Engineering the memory behavior of the device by mixing molecules will be this discussed in this chapter. It will be shown that by using different molecules together it is possible to increase the charge storage capacity of the molecular floating gate and to reduce their π-orbital overlap and consequently the lateral charge mobility within molecules.

5.1 Origin of Charge Transport in Organic Semiconductors

Organic semiconductors are composed of individual molecules that are weakly bound together through van der Waals forces, hydrogen bonding, and π-π interactions, typically producing relatively disordered, polycrystalline film. This is unlike classical inorganic semiconductors such as silicon in which atoms are held together with strong covalent or ionic bonds forming a highly crystalline three dimensional solid. When a large number of individual atoms are gathered together in a three dimensional lattice, the discrete atomic levels widen into bands and the

charges move freely in delocalized bands with very high mobility. In inorganic semiconductors, charge transport occurs in delocalized states that are limited by the scattering of the carriers mainly on phonons - that is, thermally induced lattice deformations. In this case, mobility is limited by phonons that scatter the carriers and is reduced as the temperature increases.

In organic materials, transport differs from the band transport of inorganic semiconductors. Charge delocalization can only occur along the conjugated backbone of a single molecule or between the π-orbitals of adjacent molecules. Currently, there is general agreement that charge transport in organic materials occurs by polaron (the deformation of the lattice around the electron or hole) hopping between localized states. In other words, charge transport is thought to rely on charge hopping from localized states and can be thought of as an electron transfer between a charged oligomer and an adjacent neutral oligomer. Hopping is assisted by phonons and hence charge mobility increases with temperature in organic semiconductors. The key parameter that defines charge transport is the charge mobility in a material. In the absence of any external potential, transport is purely diffusive.

When voltage is applied to a material sandwiched between two electrodes, charge carriers are transported across the sample under the electric field. The velocity of charges, moving through the material, is a function of the applied field and the drift mobility of the charges through the material. It should be noted that, for organic disordered systems, mobility is a function of the

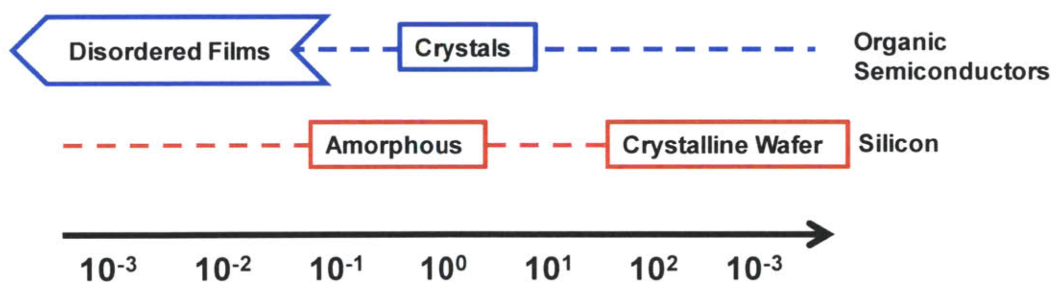


Figure 5-1: Mobility in organic/inorganic materials [91].

applied electric field. The charge mobility in organic materials greatly varies depending on the nature of charge carriers, i.e., whether they are holes or electrons, molecular structure, and morphology of the material.

Since molecular packing strongly affects mobility, the electronic interaction between two molecules still depends strongly on their relative orientation and displacement. In the case of hole transport, the orbital of relevance is the highest occupied molecular orbital (HOMO); whereas, for electron transport it is the lowest unoccupied molecular orbital (LUMO). In insulating molecules these orbitals are small and localized on just a few atoms. As a result, the spatial overlap between frontier orbitals on neighboring molecules is also small and so the likelihood of charge transfer between them vanishes.

In semiconducting molecules however, the frontier orbitals are spatially delocalized, covering much of the molecule. Delocalization arises from the strong interaction (conjugation) of partially filled orbitals on neighboring atoms, most often p-orbitals on carbon, oxygen, sulphur or nitrogen.

The spatial overlap between orbitals on neighboring molecules (or, in the case of polymers, neighboring conjugated segments) is larger than in insulators, and therefore the probability of charge transfer is greater because of delocalization.

The strength of the coupling between frontier orbitals defines not only the rate of charge transfer between molecules, but also its mechanism. When neighboring molecules are well coupled, the charge is delocalized across both molecules. Conversely, when the molecules are poorly coupled, the charge is strongly localized on a single molecule and only able to transfer to the other molecule via a thermally assisted 'hop'.

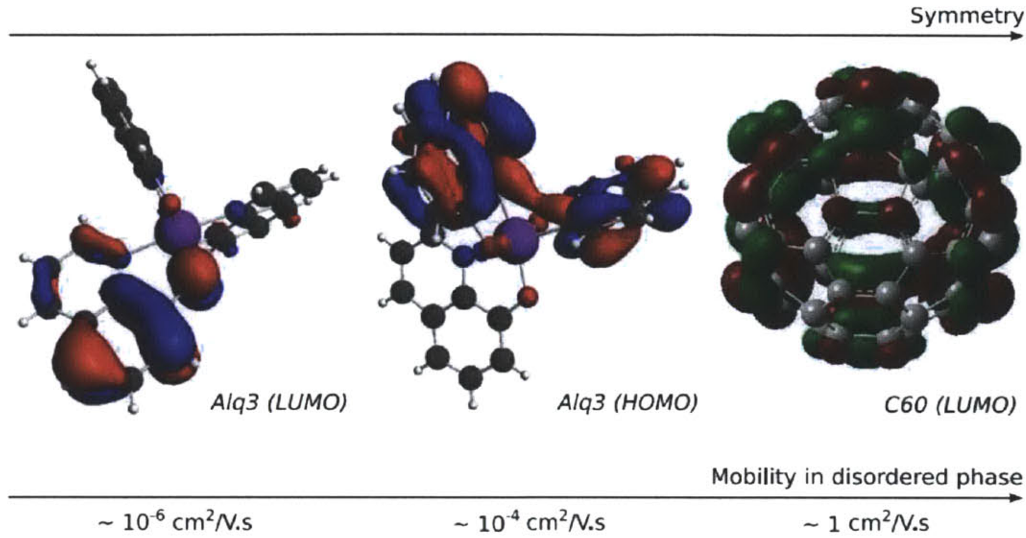


Figure 5-2: The increase in symmetry of frontier orbitals is associated with an increase in charge mobilities [91].

A charge positioned at point *i* on this lattice can hop to a neighboring point *f* with a rate Γ_{if} that is defined by the Miller-Abrahams expression [38]:

$$\Gamma_{if} = \begin{cases} \Gamma_0 \, exp(-2\gamma_{if}R_{if}) \exp\left(\frac{\varepsilon_i - \varepsilon_f}{k_B T}\right) & \varepsilon_f > \varepsilon_i \\ \Gamma_0 \, exp(-2\gamma_{if}R_{if}) & \varepsilon_f > \varepsilon_i \end{cases} \tag{5-1}$$

where Γ_0 is a frequency pre-factor; γ_{if} is a constant that describes how well sites *i* and *f* interact, R_{if} is the distance separating the center of the two molecules; the energies of the charge on site *i* and *f* are ε_i and ε_f respectively; k_B is the Boltzmann constant, and *T* is the temperature.

The higher the symmetry of the system, the better the mobility. Specifically, chapter 4 showed that electron mobility is higher than hole mobility in Alq_3 because the LUMO is less symmetric than the HOMO. Similarly, it has been demonstrated that the high symmetry of the C_{60} molecule means that the mobility is surprisingly high, even when the morphology is apparently disordered to the eye. As a result, even in C_{60} films with very small crystalline grains, charge mobilities are high.

The benefit of symmetric frontier orbitals is that they reintroduce order into disordered molecular solids. This is because the higher the symmetry of the frontier orbitals, the less the interaction between molecules depends on how they are packed.

As mentioned in chapter 2 and 3, for memory application, a charge trapping layer with poor lateral mobility is desirable. Poor lateral mobility is desirable in the sense that if there is a defect in the tunneling oxide, the charge leakage is localized around that defect.

For example, C_{60} molecules have remarkable charge storage properties however one drawback of using this material as a floating gate of the memory is its high mobility. There has been been some reports on using C_{60} molecules embedded in an organic insulator (poly-vinylphenol, PVP) or SiO_2 however, that the variation in distribution of the molecules within the insulating layer and the decrease in the density of stored charge are the primary issues of this approach. Based on studies conducted as part of this dissertation, it is possible to rearrange molecules and their π-orbital overlaps by adding dopant molecules to reduce the lateral charge mobility with an organic layer.

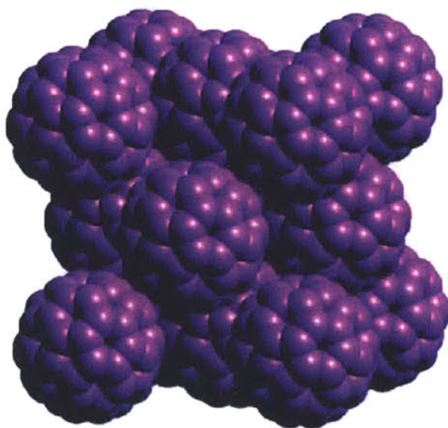


Figure 5-3: C_{60} face-centered cubic (fcc) crystall.

5.2 C_{60} and PTCBI Memory Capacitors

The schematic cross-section of C_{60} memory capacitor is shown in Figure 5-4(a). The *C-V* measurements indicate a remarkably large hysteresis window of 11.8 ± 0.1 V for P/E condition of −11 V/11 V (see Figure 5-4 (c)). A voltage shift to the right during the positive sweep (−11 V to +11 V) and a voltage shift to the left during the negative sweep (+11 to −11 V) is indicative of both electron and hole charging on the C_{60} floating gate. Endurance characteristics of C_{60} samples exhibit only a slight change in the flat-band voltage shift over 10^5 program/erase cycles (Figure 5-4 (d)).

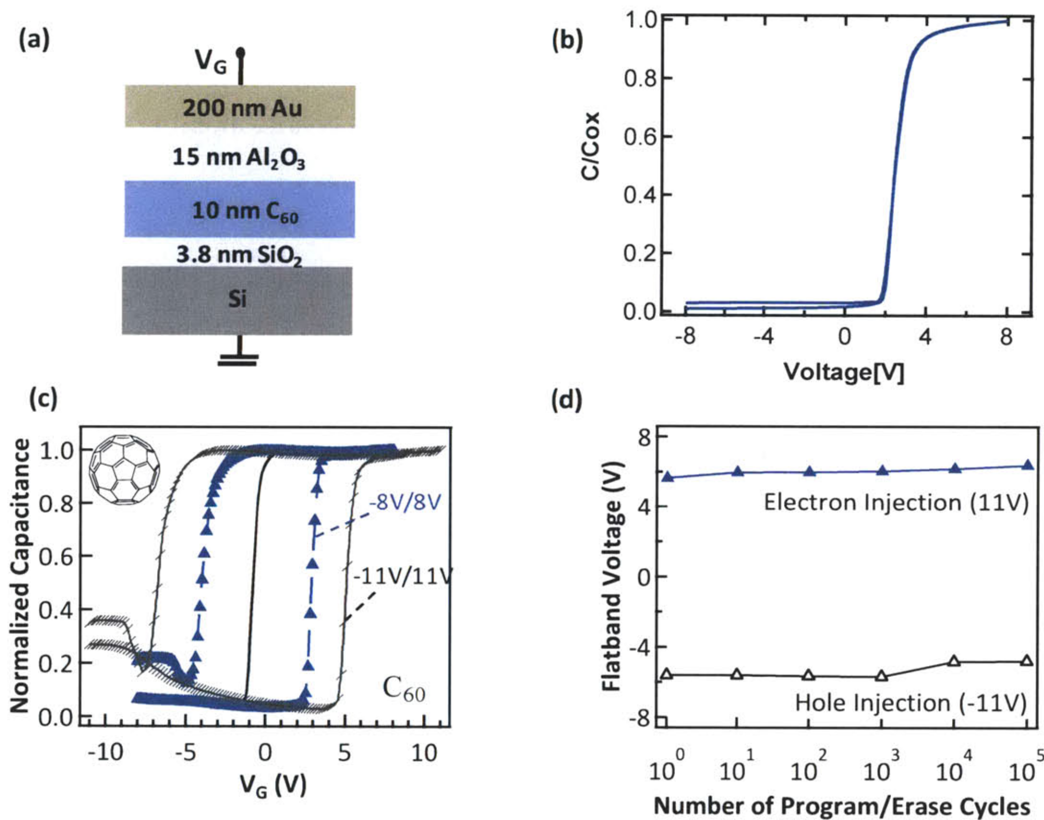


Figure 5-4: (a) Schematic cross section of C_{60} containing memory capacitor. (b) The *C-V* characteristics of the control device without organic layer; (c) The *C-V* characteristics of C_{60}-containing device, showing a large hysteresis window of 11.8 V for program /erase condition of -11 V/+11 V. (d) P/E endurance characteristic shows device durability over 10^5 program/erase cycles. The high mobility and consequently low retention time of C_{60} memory devices compromises their otherwise remarkable memory characteristics.

The control device without the organic layer exhibits to hysteresis window as shown in Figure 5-4 (b). Using the same structure, PTCBI containing memories with lower lateral mobility show comparatively smaller hysteresis window (Figure 5-5). However, the herringbone packing of PTCBI molecules separates the π-electron clouds on molecular neighbors (8, 9), which results in the low electron mobility of PTCBI thin films. Such low charge mobility provides the same advantage as the earlier demonstration of QDs in floating-gate memories, namely, if a defect exists in the tunneling oxide below the floating gate, charges in the floating gate are unlikely to transport laterally through the low-mobility molecular film, reducing the likelihood of discharge through the oxide defect. For memory applications, it is important to have a molecular layer with high storage capacity and low lateral mobility.

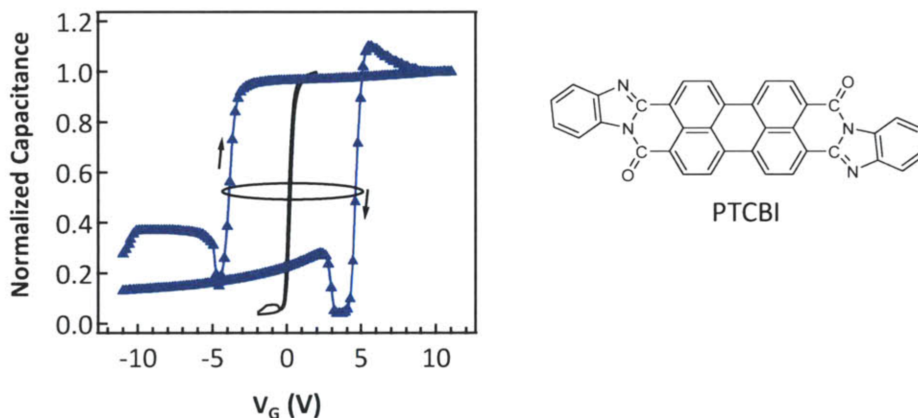


Figure 5-5: PTCBI containing memory capacitor shows hysteresis window of 8.4 V for forward and backward sweep between -11 V and 11 V.

In next sections mixed layer PTCBI:C_{60} memories are shown to have the remarkable properties of C_{60} memories while the mobility is as low as PTCBI containing memories.

5.3 Mobility measurements

There are various methods for testing the electrical properties of organic materials including time-of-flight (ToF), [68, 69] and field-effect transistor (FET) measurements [18, 67, 70-72]. In

ToF devices, charge transport is typically measured perpendicular to the substrate. Therefore, FET devices, which measure mobility parallel to the substrate, give more relevant estimations of charge mobility in materials used as the floating gate of the memory devices. It must be noted that, organic semiconductors usually form polycrystalline film, and the sample preparation can drastically affect the electrical properties.

Charge mobility μ is the ratio between the magnitudes of the average velocity of charges $\langle v \rangle$ parallel to an applied electric field F:

$$\mu = \frac{\langle v \rangle}{F} \tag{5-2}$$

Compared to inorganic semiconductors, mobility in organic semiconductors is generally very low, the highest being on the order of 1 $cm^2V^{-1}{\cdot}s^{-1}$.

The carrier mobility can be extracted from the electrical characteristics measured in a field-effect transistor (FET) configuration. The I–V (current–voltage) expressions derived for inorganic-based transistors in the linear and saturated regimes prove to be readily applicable to organic transistors (OFETs). These expressions read in the linear regime:

$$I_{SD} = \frac{W}{L}\mu C(V_G - V_T)V_{SD} \tag{5-3}$$

and in the saturated regime:

$$I_{SD} = \frac{W}{2L}\mu C(V_G - V_T)^2 \tag{5-4}$$

I_{SD} and V_{SD} are the current and voltage bias here between source and drain, respectively, V_G denotes the gate voltage, V_T is the threshold voltage at which the current starts to rise, C is the capacitance of the gate dielectric, and W and L are the width and length of the conducting channel. In FETs, the charges migrate within a very narrow channel (at most a few nanometers wide) at the interface between the organic semiconductor and the dielectric.

The molecule μ_{sat} was extracted by plotting $\sqrt{I_{DS,sat}}$ against V_G. Equation (5-4) is based on

the assumption that μ_{sat} is independent of V_G.

Transport is affected by structural defects within the organic layer at the interface, the surface topology and polarity of the dielectric, and/or the presence of traps at the interface (that depends on the chemical structure of the gate dielectric surface).

Measurement of organic materials by using bottom gate FETs are described in the next section. The charge mobility within the molecular layers was measured by forming thin film transistor structures with 10 nm thick molecular film as the semiconducting layer.

5.3.1 Fabrication of Bottom Gate Field Effect Transistors

A lateral, organic, thin film transistor (OTFT) includes gate electrode, insulating material, semiconductor organic material, and conducting source and drain electrodes. Due to the staggered shape simplicity of the bottom gate (Figure 5-6), this shape was used to fabricate the molecular lateral OTFT. All the fabrication process and measurements were done in a glove box with a nitrogen atmosphere.

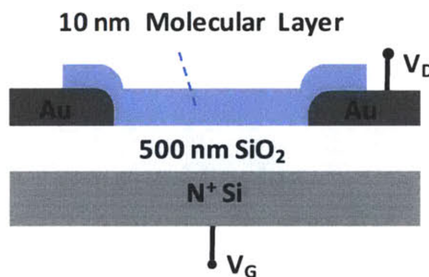


Figure 5-6: Schematic of bottom-gate OTFT for mobility measurement.

The devices were prepared on top of an N-doped silicon substrate with thermally grown silicon dioxide that was used as a gate insulator. The thickness of the silicon dioxide was 500 nm.

An interpenetrating structure mask was used to define the lateral source and drain contacts. These structure shapes allowed achievement of a high channel width (*W*) to length (*L*) ratio. The channel length for this mask was 10 μm, with W/L ratio of 1200.

The material Au was used as the drain and source electrode. The electrodes were patterned using the lift-off method. Lift-off is a common technique to pattern metal or dielectric film in the µm or sub-µm range besides wet or dry etching. The image reversal process was used for the lift-off as outlined in Figure 5-7.

After cleaning the wafer in Piranha solution, AZ 5214 resist was spun on the oxide layer and pre-baked at 90 ˚C for 30 minutes. The photoresist was then exposed to UV light in a mask aligner and exposure unit using the mask. The wafer was then post-baked on hotplate for 65 s at 110 ˚C. During the image reversal bake, the exposed resist areas were converted and became insoluble in the developer; while the resist so far unexposed remains virgin and can be exposed in the next step. After the flood exposure, the exposed area is removed from the developer.

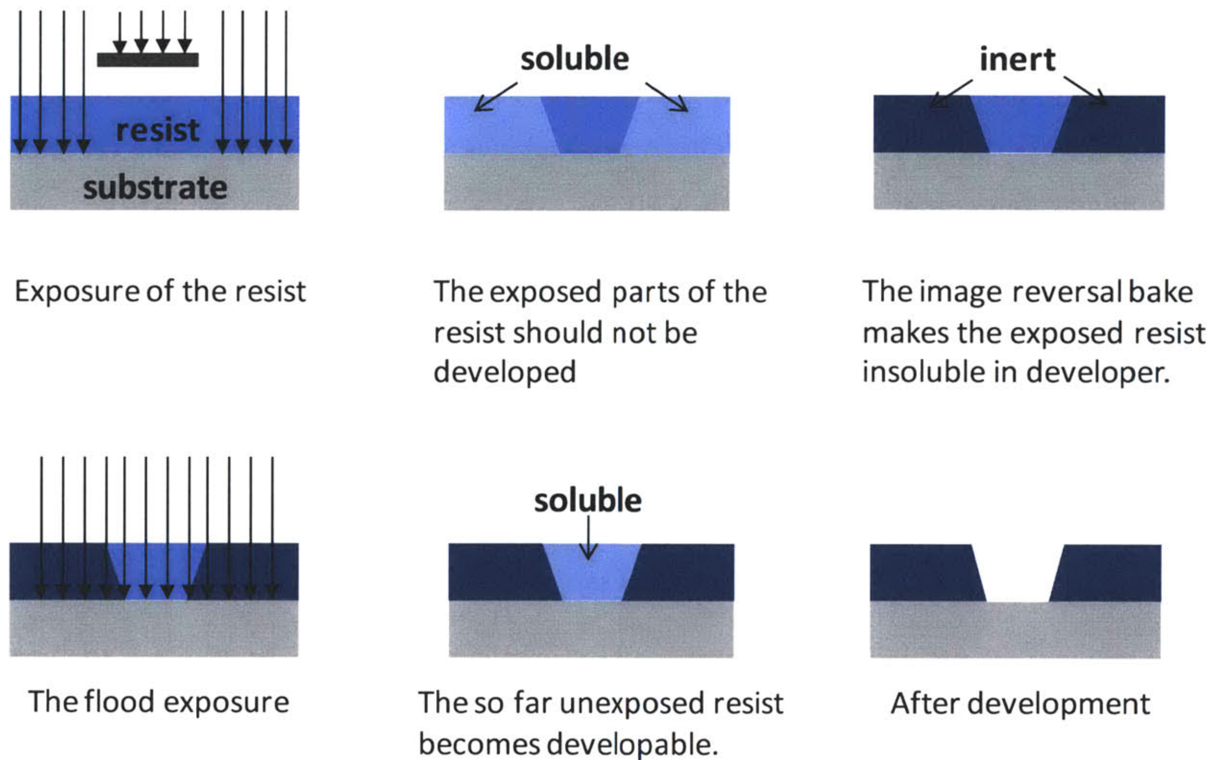


Figure 5-7: The image reversal process steps for lift-off.

After cleaning the exposed surface of the substrate in soft oxygen in order to remove resist residue, 4 nm of Cr and 40 nm of Au were deposited using an e-beam evaporator. The patterning procedure was completed by removing the resist in acetone as well as the deposited materials on

top of it. After removing the resist and cleaning the wafer (Appendix A) the samples were transferred into the glove box with a nitrogen atmosphere.

The C_{60} organic semiconductor was thermally evaporated through a shadow mask on top of the insulator layer. The samples were placed in a rotate platform with a rectangular mask inside the bell jar evaporator system (Figure 3.3).

5.3.2 PTCBI TFTs (*I-V* Characteristics and Mobility Measurement)

Quantifications of the OTFT performance were done by the current-voltage (*I-V*) characteristics of the conductance and transconductance. The threshold voltage and the mobility values were estimated from these curves. This measurement allows us exact measurement of the drain, source and gate current. The measurements were done with a semiconductor parameter analyzer (Agilent 4155B) connected to three Probe heads located inside the glove box with a nitrogen atmosphere.

All measurements were done in the dark in order to avoid photo-generation of charges.

First the output characteristic of a device with 10-nm PTCBI was measured. This was done by continuously varying the source-drain voltage ($0\ V < V_{DS} < 25\ V$) for constant gate source voltage.

This measurement was repeated for different gate-source voltage (V_{GS}= 0, 5, 10, 15, 20, 25, 30 V). The results appear in Figure 5-9. This figure shows the linear and saturation regions. The linear slope can be seen for low drain-source voltage, where the TFT is in the linear region. For higher drain-source voltage the current starts to saturate, whereas the channel current does not increase with the drain-source voltage.

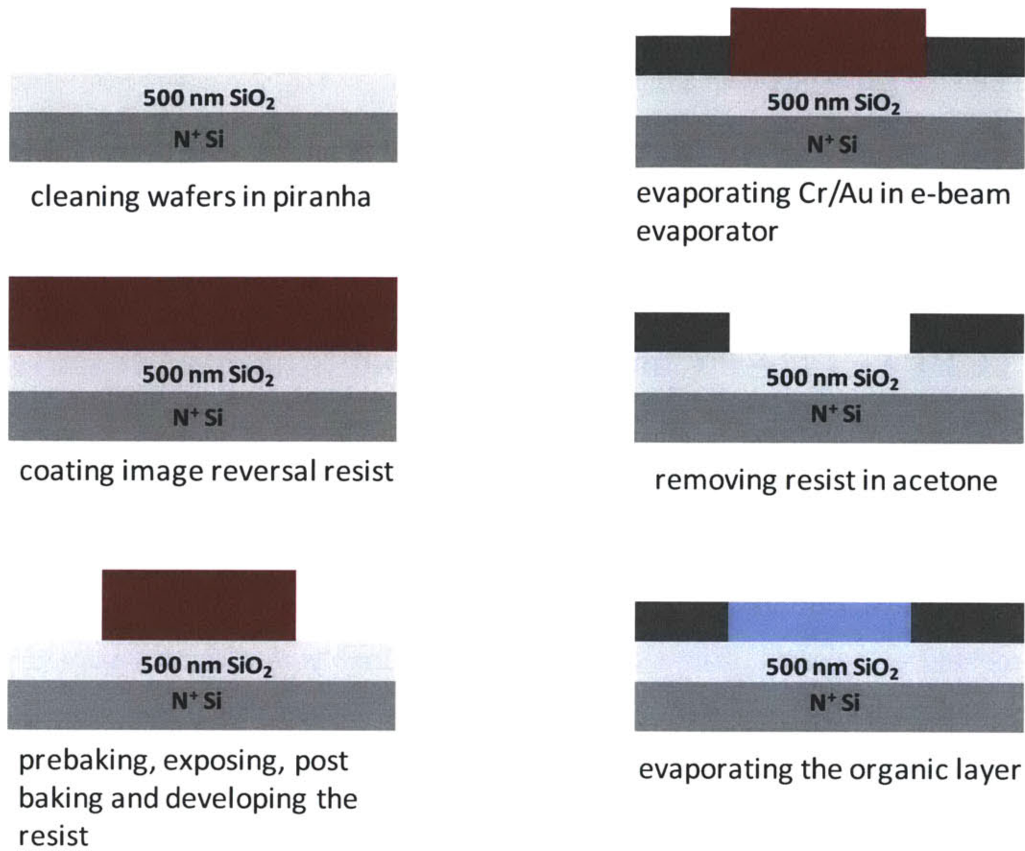


Figure 5-8: OTFT fabrication process steps for measuring lateral mobility within organic materials.

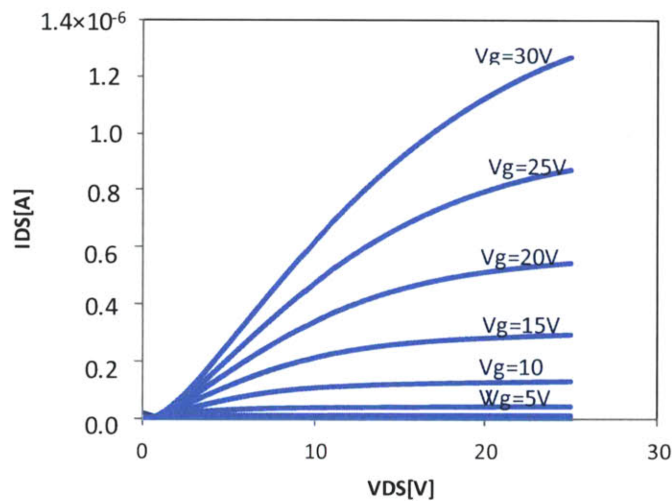


Figure 5-9: Output characteristic for PTCBI OTFT with silicon dioxide insulator and gold contacts. Drain-source voltage was swap between 0 V to 25 V while gate-source voltage was kept constant. V_{DS}=0, 5, 10, 15, 20, 25, 30 V.

The transfer characteristic for PTCBI OTFT is shown in Figure 5-10. Here the gate-source voltage is continuously changed (-30 V< V_{GS} < 30 V) while the drain-source voltage is kept at 10 V.

From the transfer characteristic, it was shown that the threshold voltage registered between -3 V to 2 V. The common method was used for OTFT threshold voltage extraction. This method includes fitting a linear curve to the square root of the channel current versus gate voltage in the range where $V_{DS} >> V_{GS}$. The linear fit is presented, according to equation (5-4), in Figure 5-11.

According to the content in Figure 5-11, the threshold voltage is equal to V_T = -2.3 V. Extraction of the threshold voltage allows the calculation of the effective OTFT mobility value using equation (5-4) for linear region. From the slope of the fitted line, the mobility in saturation can be extracted using equation 5-4. The extracted saturation mobility is 2.16×10^{-4} $cm^2V^{-1}s^{-1}$ and the linear mobility is 3.6×10^{-4} $cm^2V^{-1}s^{-1}$ respectively.

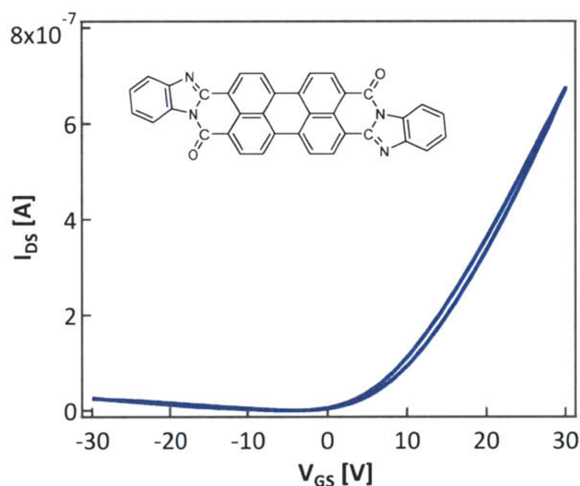


Figure 5-10: Transfer characteristic for PTCBI OTFT with silicon dioxide insulator and gold contacts. Gate-source voltage was swap between -30 V to 30 V while drain-source voltage was kept constant; V_{DS} = 10 V.

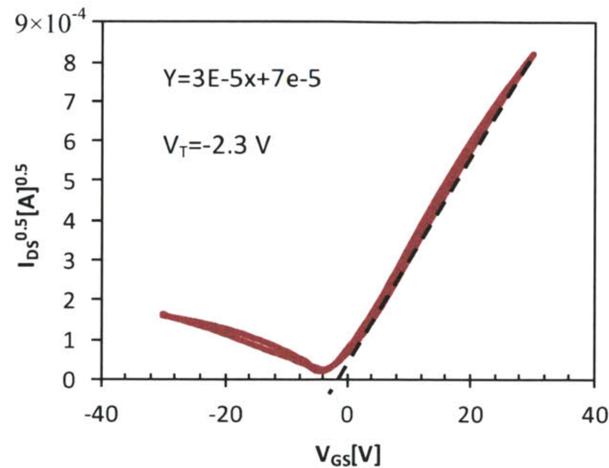


Figure 5-11: Threshold voltage for PTCBI OTFT with silicon dioxide insulator and gold contacts was defined as V_T=-2.3 V, by fitting linear curve to the square root of I_{DS} vs. V_{GS} where V_{DS} =10 V.

5.3.3 C_{60} TFTs (*I-V* Characteristics and Mobility Measurement)

The C_{60} TFTs were fabricated as described above by depositing a 10 nm C_{60} layer as the channel of the transistor. The devices were measured in the same manner as described in the previous section. The results for output and transfer measurements are shown in Figure 5-12. The output characteristic was accomplished by continuously varying the source-drain voltage (0 V $<V_{DS}<$40 V) for different constant gate-source voltages of V_{GS}=0, 5, 10, 15, 20, 25, 30, 35, and 40 V.

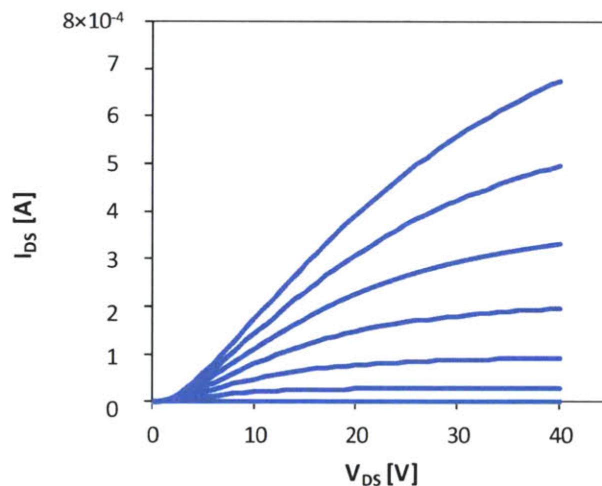


Figure 5-12: Output characteristic for C_{60} OTFT with silicon dioxide insulator and gold contacts. Drain-source voltage was swap between 0 V to 40 V while gate-source voltage was kept constant. V_{GS}=0, 5, 10, 15, 20, 25, 30, 35, 40 V.

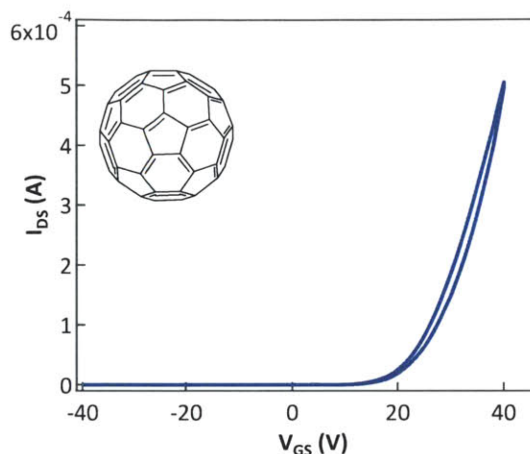


Figure 5-13: Transfer characteristic for C_{60} OTFT with silicon dioxide insulator and gold contacts. Gate-source voltage was swap between -40 V to 40 V while drain-source voltage was kept constant; V_{DS} = 40 V.

The transfer measurement was taken at the constant source-drain voltage of 40 V. In this measurement the device is operating in saturation mode (V_{DC}>>V_{GS}-V_T). The threshold voltage and saturation mobility can be calculated by fitting the linear curve to the square root of the channel current versus gate voltage in the saturation regime.

The mobility of 0.02 $cm^2V^{-1}s^{-1}$ was extracted from the slope of the fitted line. The threshold voltage is equal to V_T=15 V as seen in Figure 5-14.

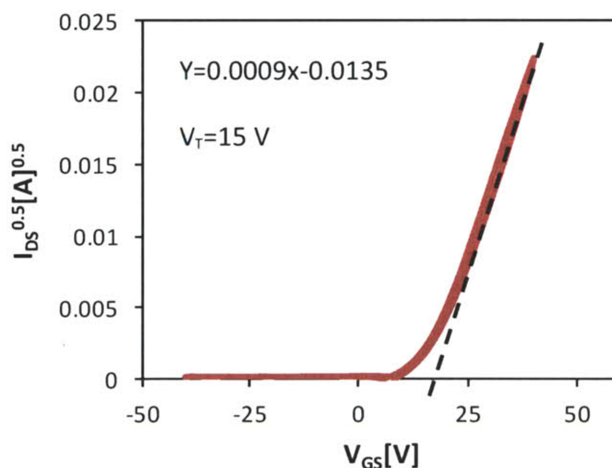


Figure 5-14: Threshold voltage for C_{60} OTFT with silicon dioxide insulator and gold contacts was defined as V_T=15 V, by fitting linear curve to the square root of I_{DS} vs. V_{GS} where V_{DS} =40 V.

5.3.4 PTCBI/C_{60} TFTs (*I-V* Characteristics and Mobility Measurement)

The effect of mixing molecules on lateral molecules is analyzed in this section. C_{60} TFTs have higher lateral mobility as discussed in section 5.3.3. However it was demonstrated that by adding PTCBI molecules to C_{60} lateral mobility decreases dramatically. The memory behavior of the mixed molecular layer will be discussed in the next section.

PTCBI/C_{60} TFTs were fabricated by co-evaporating PTCBI and C_{60} using the thermal evaporator in a ratio of 1:1. The ratio was controlled by monitoring the deposition rate of PTCBI and C_{60}. The transfer (I_D-V_{GS}) and output (I_D-V_{DS}) characteristics of PTCBI/C_{60} TFTs is shown in Figure 5-15. The threshold voltages in the range of -1 V to 2 V were calculated for PTCBI/C_{60} transistors using the same approach discussed above. The saturation mobility of 9.7×10^{-5} $cm^2V^{-1}s^{-1}$ and linear mobility of 2.4×10^{-4} $cm^2V^{-1}s^{-1}$ were calculated from the *I-V* characteristics shown in Figure 5-15. From the transistor current-voltage response, the lateral electron mobility in the range of 0.06 - 0.15 $cm^2V^{-1}s^{-1}$, 0.96-3.6 $\times$ 10^{-4} $cm^2V^{-1}s^{-1}$ and 0.96-2.4 $\times$ 10^{-4} $cm^2V^{-1}s^{-1}$ were derived in C_{60}, PTCBI and PTCBI:C_{60}, respectively. In the next section, mixed layer PTCBI:C_{60} memory is shown to have the remarkable properties of C_{60} memory while the mobility is as low as PTCBI containing memory.

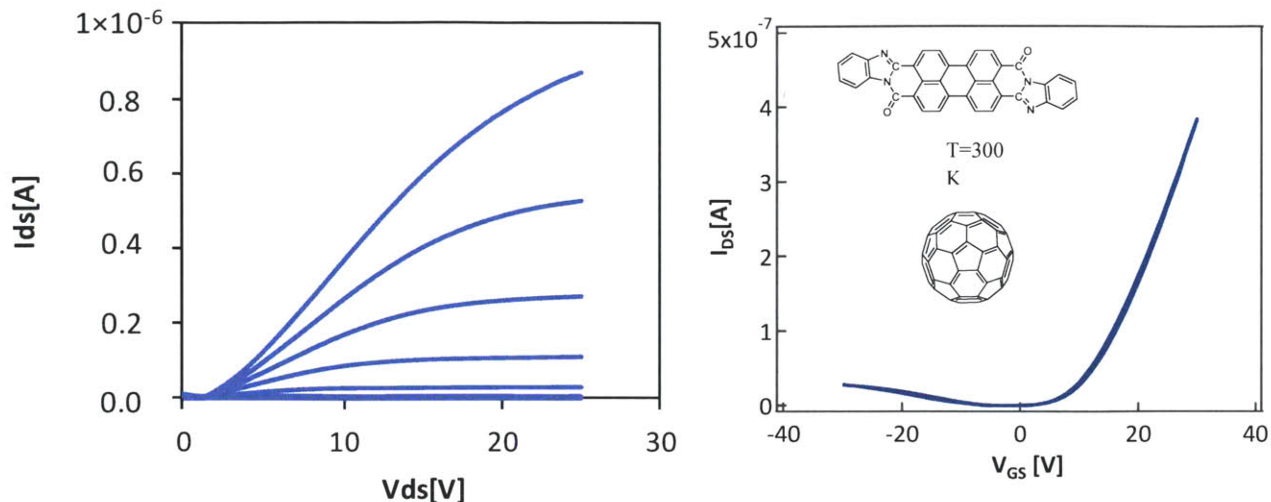


Figure 5-15: Typical (a) transfer (I_{DS} - V_{GS}) and (b) output characteristics (I_{DS} - V_{DS}) for PTCBI/C_{60} TFTs.

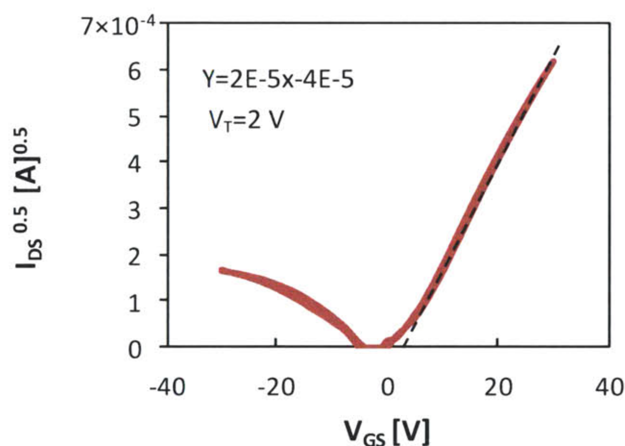


Figure 5-16: Threshold voltage for PTCBI/C_{60} OTFT with silicon dioxide insulator and gold contacts was defined as V_T= 2 V, by fitting linear curve to the square root of I_{DS} vs. V_{GS} where V_{DS}=10 V.

5.4 PTCBI/C_{60} Memory Capacitor

Memory capacitors with a 10 nm-thick mixed layer of PTBI/C_{60} were fabricated. The *C-V* measurements showed remarkably large hysteresis windows of up to 11.9 V for the program/erase condition of -11 V/+11 V with voltage held at each bias for 3 sec. The amount of flatband voltage shift as a function of programming and erasing voltage is shown in Figure 5-17

(b).

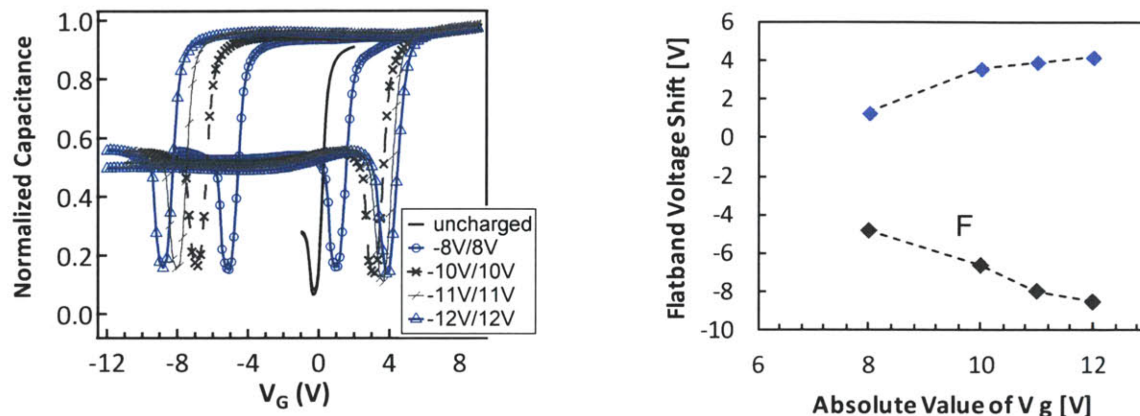


Figure 5-17: PTCBI: C_{60} containing memory shows the hysteresis window of 11.9 V for forward and backward sweep between -11 V and 11 V, while its lateral mobility has been decreased dramatically compared toC_{60}.

	C_{60}	PTCBI	PTCBI:C_{60}
Mobility ($cm^2V^{-1}s^{-1}$)	0.06-0.15	$(0.96\text{-}3.6)\times10^{-4}$	$(0.96\text{-}2.4)\times10^{-4}$
Vfb Shift (V) for -11V/11V	11.8	8.4	11.9

Table 5.1: Field effect mobility and charge storage capacity of organic thin film.

PTCBI/C_{60} memory shows a large hysteresis window comparable to C_{60} memories and at the same time has the advantage of low mobility comparable to the mobility of PTCBI thin film.

The summary of this study is presented in table I.

5.5 Conclusion

The memory properties of a set of organic materials were investigated for possible application to CMOS-compatible nonvolatile memory devices. High charge retention density and good cycling endurance was demonstrated in C_{60} structures. However, demonstrated charge retention

time dependency on the lateral mobility of organic thin films makes use of these materials challenging. C_{60} molecular thin films have higher mobility compared to other tested molecules due to symmetry and larger π-orbital overlaps between C_{60} molecules. This challenge was met by rearranging molecules and π-orbital overlaps between them in order to reduce mobility. It was demonstrated that by mixing PTCBI with C_{60} results in a mixture of two kinds of molecules with charge retention capability and reduced mobility due to reduced symmetry and overlap of electron clouds.

Chapter 6

MEMS Switches Employing Active Metal-Polymer Nanocomposites

Micro-Electromechanical Systems (MEMS) devices are starting to be used in a variety of applications. In particular, there is great demand for MEMS switches due to their low power consumption, very small size, low cost, reliable, wide tuning range, low loss digital switching, low phase noise, low insertion loss, higher isolation, better linearity and single chip packaging which are almost impossible with standard semiconductor switches [103, 104].

This chapter presents the design, fabrication, testing and evaluation of a MEMS switch that employs a metal-polymer nanocomposite as its active material. The nanocomposite is formed by doping a polymer with conducting nanoparticles. The conductivity of the nanocomposite changes 10,000-fold as it is mechanically compressed. In this demonstration the compressive squeeze is applied with electric actuation. Since squeezing initiates the switching behavior, the device is referred to as a "squitch".

6.1 Introduction

It has been known for decades that polymers doped with conducting particles such as carbon black or metal micro/nanoparticles can be piezoresistive [105-108]. These materials have found application in resettable fuses [107], and tactile and pressure sensors [109]-[111]. They are often

fabricated so as to be poor conductors that increase their conductivity under applied compressive or tensile strain; percolation pathways form to allow increased electrical conduction through tunneling between particles. When the piezoresistive behavior occurs due to tunneling, with currents that grow exponentially as the particles become closer together, large changes in conduction can occur over small strains as seen in Figure 6-1. For example, conduction change over 7 orders of magnitude has been demonstrated in response to a 15% strain [108].

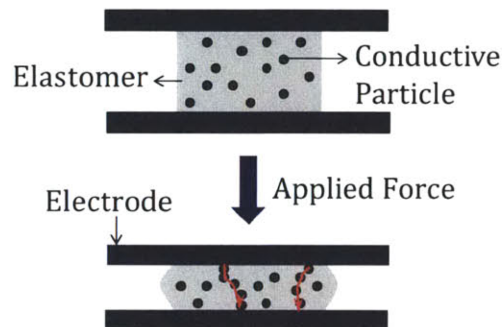


Figure 6-1: Formation of conduction paths in metal-polymer composites when compressed.

In this study, an electrically-squeezed piezoresistive nanocomposite is used to make an electrically controlled switch, or "squitch". Several advantages of the squitch are that: (1) it is an additive technology compatible with large area processing with printing or photolithography on rigid or flexible substrates; (2) it can exhibit large on-to-off conduction ratio, up to 10^7:1; (3) it can exhibit voltage-controlled conduction with a gain greater than 1 decade per 60 mV, a fundamental limit for silicon-based semiconductor switches; and (4) its contacts are not subject to the usual wear associated with point-contact electromechanical switches.

One example of a three-terminal squitch design is shown in Figure 6-2, with terminals labeled in equivalence to a field effect transistor (FET). The nanocomposite material block labeled "Squitch Material" is connected both electrically and mechanically to two metal conductors labeled "Metal Drain" and "Metal Source" in this structure. These form the primary conduction path through the squitch. As fabricated, the resistance of the nanocomposite material is very large, putting the squitch in an "off" state. As the composite is compressed in the vertical direction, it begins to conduct; and when compressed sufficiently, it conducts well, putting the

squitch in an "on" state. The "Metal Gate" controls the degree of compression and hence conduction of the composite.

By applying a positive or a negative voltage between the gate and source an electric field is established between the two. This resulting force attracts the source to the gate, thereby compressing the composite and enabling electric control of electron current from the source to the drain, as shown in Figure 6-3. Thus, the squitch is a voltage-controlled conductor in a similar manner as the FET or the bipolar-junction transistor.

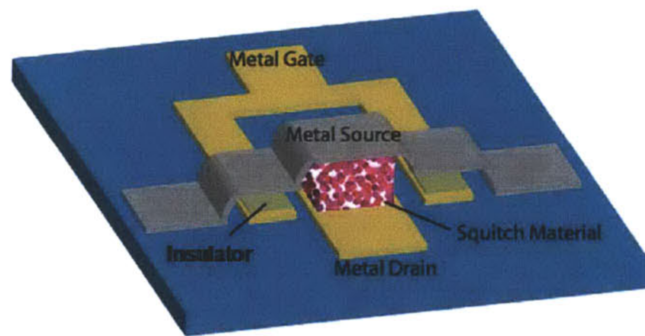


Figure 6-2: Three-terminal "Squitch" design.

The final component of the Figure 6-2 device design is the insulation layer that prevents inadvertent conduction from gate to source.

Since the conduction modulation of the nanocomposite occurs over <20% strain, the required source motion is only a fraction of the source-drain distance. Therefore the source electrode

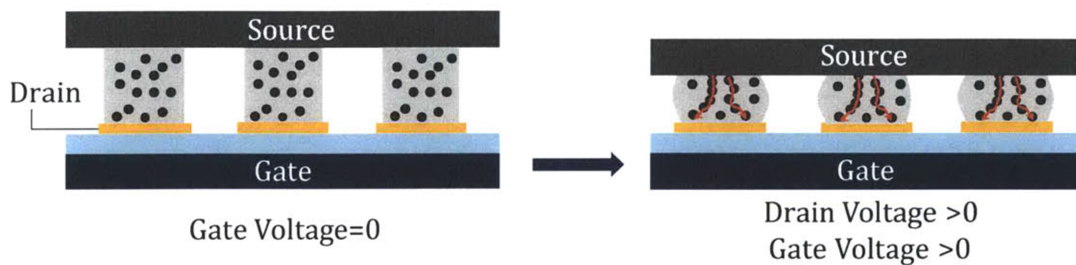


Figure 6-3: Operation mechanism of the squitch.

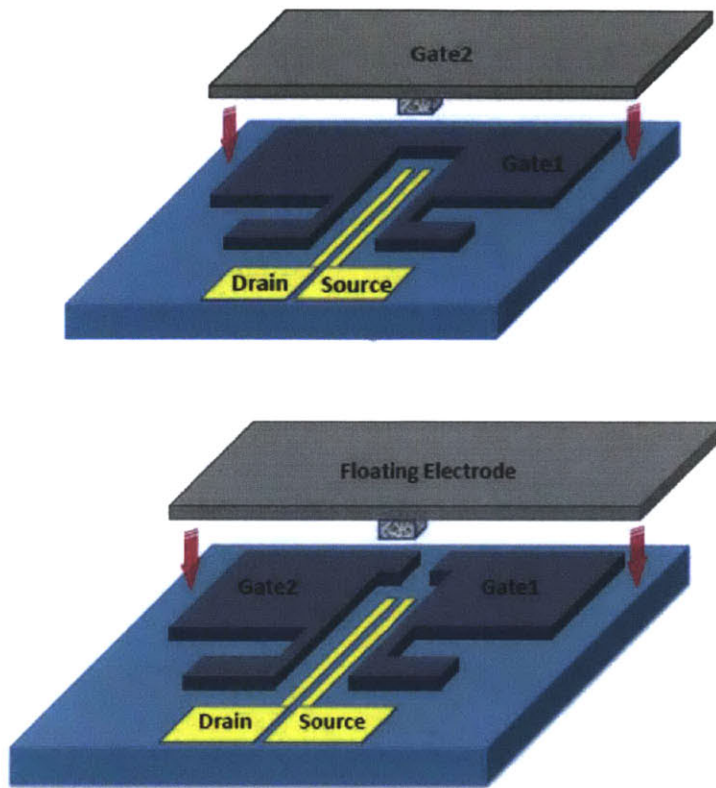


Figure 6-4: An embodiment of a two gate squitch.

may be stepped as shown in Figure 6-2, leading to greater gate-to-source electric fields and higher corresponding pressures with the same gate-source voltage.

As shown in figure 6-4 in a slightly different embodiment of the squitch switch, the metal drain contact can be split into two half contacts which become the drain and the source. In this case electron conduction occurs laterally through the elastomer composite. The top electrode that was the original source is then electrically isolated from but still mechanically connected to the composite. Its role then becomes that of a second gate. In this case, the compression of the polymer is controlled by the voltage between the two gates, while the conduction occurs between the independent source and drain.

Thus, the conduction path is separated from the control electrodes, which could offer circuit design advantages.

In implementing and fabricating the squitch components described herein, different squishable materials may be used. In this study an extremely soft elastomer, PDMS, has been used for the polymer matrix.

6.2 Elastomeric Materials

Elastomers, also known as rubbers, are amorphous polymers composed of long chains of monomers as shown in Figure 6-5. Each monomer is typically made of carbon, oxygen, and hydrogen. The individual chains are amorphously tangled with each other.

As the elastomer is strained, these tangled chains reconfigure themselves to distribute the applied stress. Chemical bonds called “cross-links” exist between the chains and help the elastomer returns to its initial state once the stress is removed. However, this process is not completely reversible as chains may change in conformation during the excitation resulting in viscoelastic effects such as creep and stress relaxation.

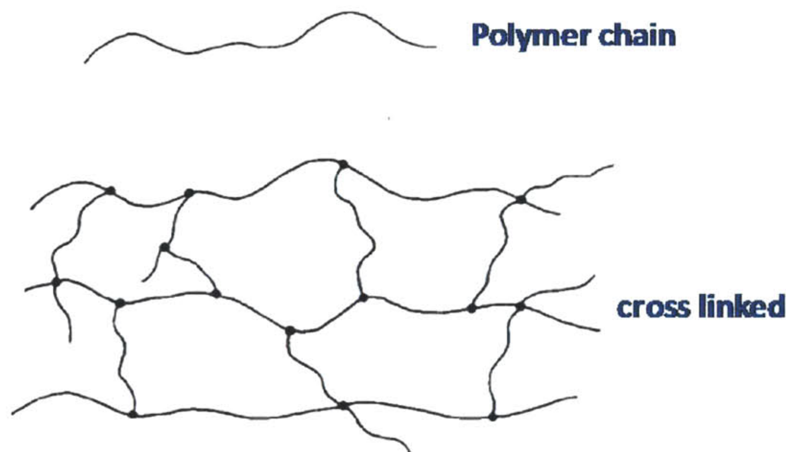


Figure 6-5: Conceptual diagram of an elastomer’s polymer chains and crosslinks.

Polydimethylsiloxane (PDMS) belongs to a group of polymeric organosilicon compounds that are commonly referred to as silicones.[1] Silicones form one subcategory of elastomers whose composition includes silicon in addition to the other elements [112-114]. They have many useful properties including electrical insulation, waterproofing, and low chemical reactivity.

PDMS is the most widely used silicon-based organic polymer, and is particularly known for its unusual rheological (or flow) properties. PDMS is optically clear and in general, is considered to be inert, non-toxic and non-flammable. It is occasionally called dimethicone and is one of several types of silicone oil (polymerized siloxane). PDMS is widely used in different fields of application, such as micro/nanofluidics, electrical insulation, micro/nanoelectromechanical (MEMS/NEMS) devices, soft lithography, quantum dots, and charge patterning in thin-film electrects [112].

The general chemical structure of a poly(siloxane) is shown in Figure 6-6. Commercial silicone kits comprised of a base and curing agent such as Ecoflex and Sylgard contain mixtures of various poly(siloxanes) and H-siloxanes as the base and a platinum catalyst and vinyl-terminated siloxanes as the curing agent.

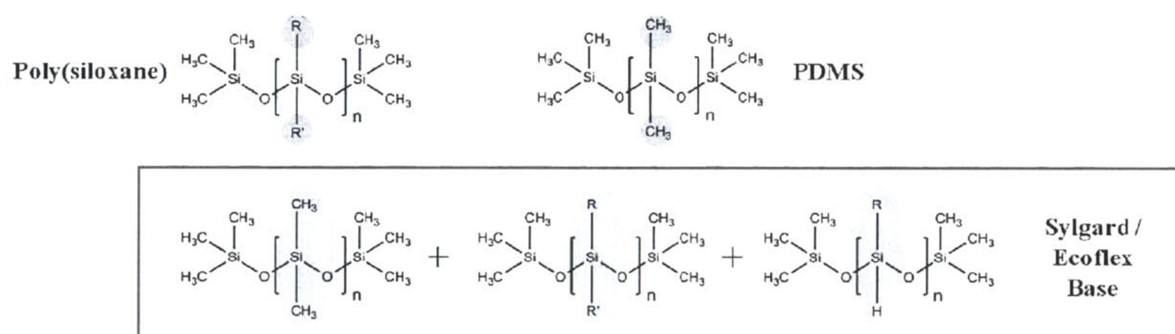


Figure 6-6: Chemical structures of various poly(siloxane)s. R = R' = long alkyl chains (e.g. C12H25, C14H28, etc.)

The base and curing agent can be mixed together in any desired ratio to yield a shape-persistent, elastomeric matrix of covalently crosslinked siloxanes (see Figure 6-7 for the crosslinking reaction). The mechanical properties of the resulting crosslinked polymer can be easily tuned by changing the ratio of base to curing agent. The Young's modulus of crosslinked siloxanes can typically be tuned between 360 – 870 kPa and the shear modulus can vary between 100 kPa to 3 MPa. In addition, softer materials can be accessed by adding long alkyl chain-containing poly(siloxane)s (R, R' = C14H29, C16H33, etc.), which act as plasticizers, to the starting base mixture [115].

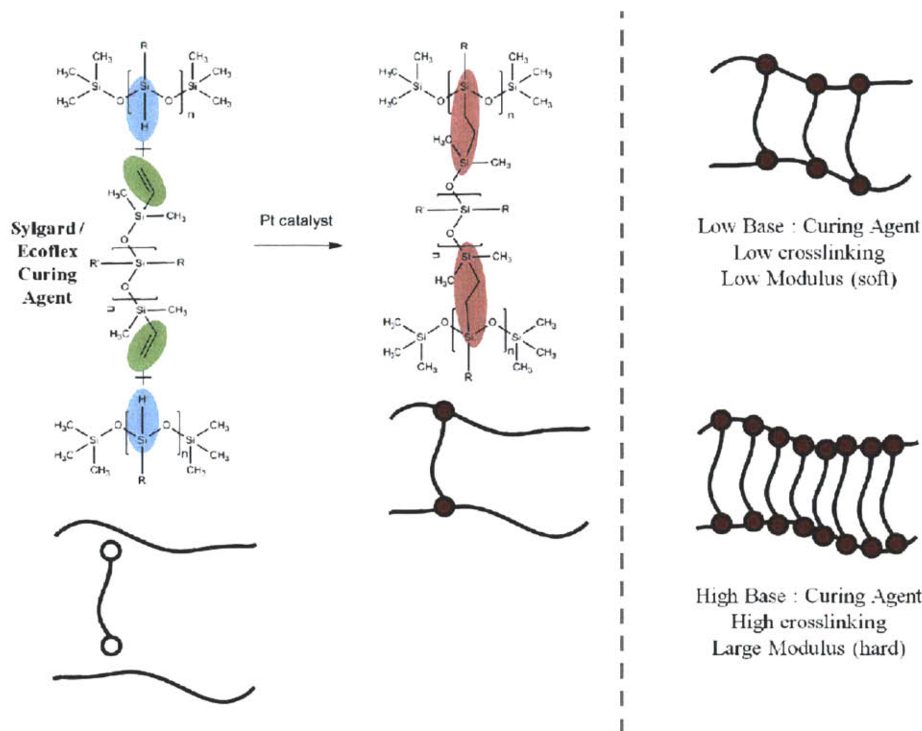


Figure 6-7: Crosslinking reaction of commercial silicone kits and tunable mechanical properties of the resulting crosslinked elastomer.

6.3 Metal-Polymer Nanocomposite

Polymer composites are a combination of a polymer matrix and micro/nano-sized fillers such as particles, fibers, platelets, or tubes. The polymer matrix can be an amorphous or crystalline thermoplastic material or a crosslinked three-dimensional polymer network. The matrix holds or binds the fillers together and protects them from damage by distributing any stress through the whole specimen. Polymer composites have received considerable attention over the last decade because of their potential to dramatically enhance properties relative to the neat polymer matrix [116–130]. Incorporation of small amounts of filler leads to an improvement in material properties, such as modulus, strength, heat resistance, flame retardant, and lowered gas permeability [117–130]. In addition, polymer composites could also yield novel functions including electrical [131–134], magnetic [135–141], and optical functions [142–145], as well as biofunctionality [146–149]. The enhancement of material properties and creation of novel

functions has been linked to the interfacial interaction between the polymer matrix and fillers as well as the formation of a network of interconnected filler particles. This network of interconnected particles can conduct heat and electrical current [118–128]. Development and tailoring of polymer composites offer the possibility to promote their use in automotive, aerospace, building, electrical, optoelectronic, and biomedical applications [147–149].

Major challenges in design and fundamental understanding of polymer composites are related to the complexity of the composite structure, dispersibility of fillers, and the relationship between dispersion and optimal properties. Uniform dispersion of nanoparticles and nanotubes against their agglomeration due to van der Waals bonding is the first step in the processing of nanocomposites.

6.4 Squitch Fabrication

6.4.1 Metal-Polymer Composite

Due to the modular nature of our nanoparticle/polymer composites, the electromechanical properties of the squitch material can be tuned independently. Three factors influence the performance of the Squitch fabricated from nanoparticle/polymer composites: (1) the nature of the polymeric matrix; (2) the identity and packing structure of the nanoparticle; and (3) the degree of nanoparticle loading in the polymeric matrix. The polymeric component needs to be elastomeric, or undergo completely reversible elastic deformations, and be stable under repeated and rapid compression-decompression cycles.

In this dissertation the composite material matrix (PDMS) was doped with conductive nickel microparticles (2-20 μm). The Ni-PDMS composite was prepared by uniformly mixing the constituents with a planetary mixer. Distribution of Ni particles inside the elastomer is seen in the back-scattered electron microscopy (BSEM) image of Figure 6-8 (a). For this BSEM measurement the composite was frozen in liquid nitrogen and then fractured. Mechanical properties of the nanocomposite can be optimized by incorporating different amounts of the curing agent into the polymer elastomer base. Thus, it is possible to engineer and reduce the Young's modulus of the composite.

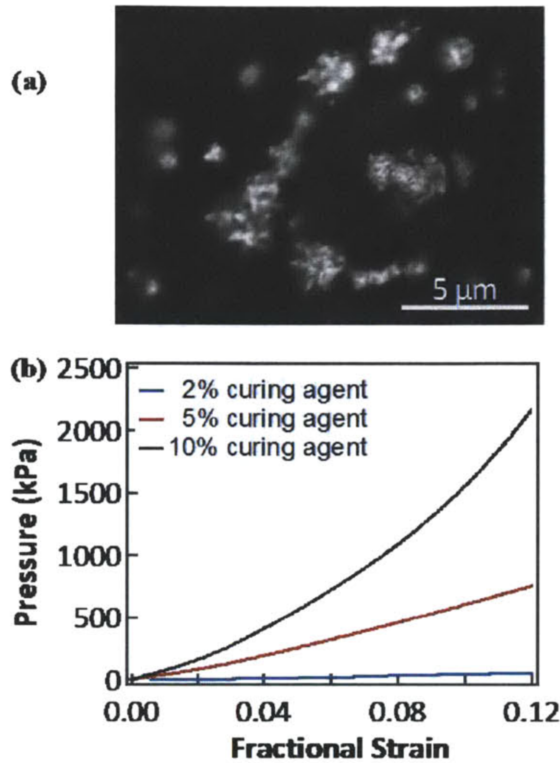


Figure 6-8: (a) BSEM image of Ni-PDMS composite where nickel particles are approximately 2.5 μm in diameter. (b) Stess-strain characteristics of the nickel-doped-PDMS composite pills with the height of 1.6mm and diameter of 4.7mm.

The stress-strain characteristics of the Ni-PDMS composite with different ratios of curing agent, 2%, 5% and 10% by weight measured using a Zwick mechanical tester is shown in Figure 6-8(b). Low cross-link densities decrease the Young's modulus of the cured elastomer, and high cross-link densities cause it to become more rigid or glassy. A softer Ni-PDMS composite allowed a desired strain to be achieved with a lower stress and hence lower actuation voltage. This increases the voltage-controlled gain of the squitch.

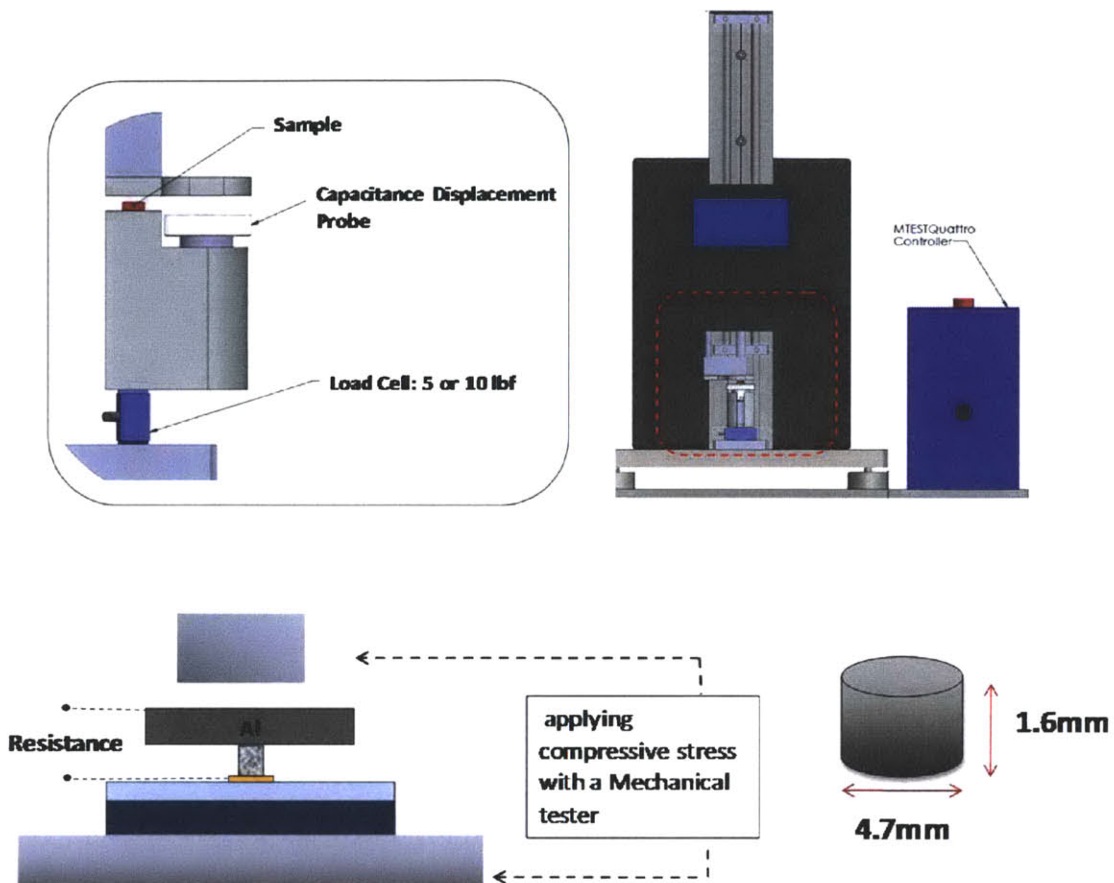


Figure 6-9: Mechanical compression testing of the nickel-doped-PDMS composite pills.

To study the electromechanical properties of the Ni-PDMS composite, a square wave of displacement is applied to a pill with the height of 1.6 mm and diameter of 4.7 mm. The resistance across the pill was measured simultaneously. By applying up to 33% strain the resistance of the pill changed by 6 orders of magnitude as shown in Figure 6-10. No significant variation in the resistance change was observed during cycling. The minimum resistance of 1 kΩ can be further decreased by improving the contact resistance.

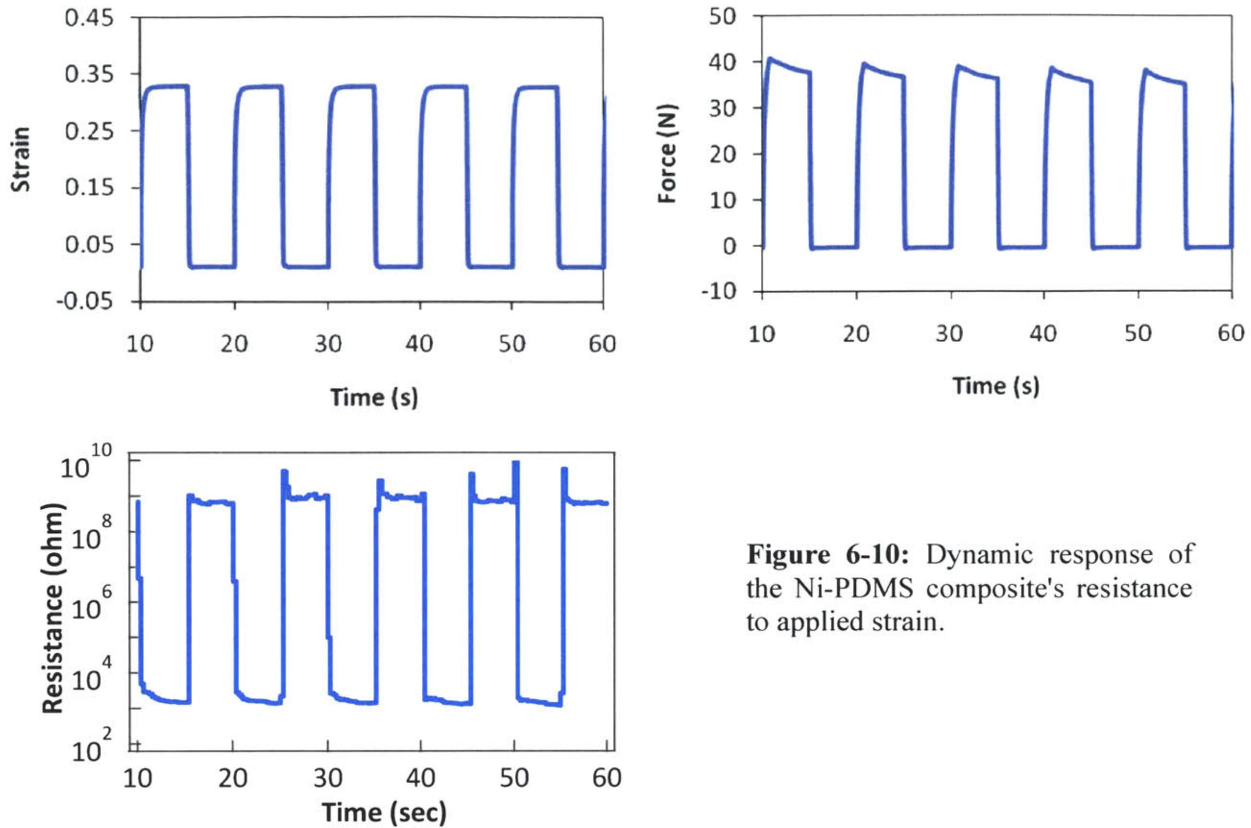
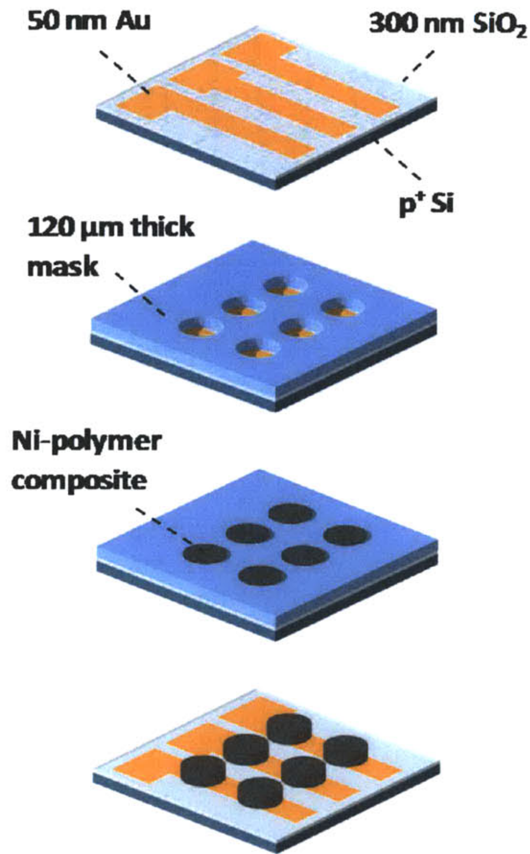


Figure 6-10: Dynamic response of the Ni-PDMS composite's resistance to applied strain.

6.4.2 Squitch Fabrication Process

The device shown in Figure 6-6 is the first-demonstration of an electrically actuated squitch. Its fabrication is outlined in Figure 6-11, and begins with a heavily doped silicon wafer on which a 300-nm-thick silicon-dioxide insulator has been grown. The wafer serves as the gate electrode. A 50-nm-thick chrome-gold drain contact was then deposited and patterned on the oxide layer. The nanocomposite was stencil-patterned by placing a 120-µm-thick stainless steel mask over the drain electrodes and filling its cavities with the mixed, uncured Ni-PDMS composite. The excess composite was removed from the mask surface using a razor blade, and the substrate was then annealed for 10 min at 100˚C. The resulting composite shape is shown in Figures 6-12. A 0.5-inch-square aluminum plate, which acts as the source electrode, was then placed on top of the nanocomposite to complete squitch fabrication. Connections to the gate and drain were made



Deposition and patterning of 50-nm-thick Cr-Au as the drain electrode on highly doped Silicon wafer with 300 nm thermal oxide.

Patterning conductive polymer on top of the drain electrode by placing a 120 µm stainless steel mask with different size openings on top the substrate.

Filling the cavities with the composite and scraping off the excess using a razor blade.

Removing mask and curing the polymer at 100 °C for 10 min

Figure 6-11: Fabrication process for the squitch.

with probes, while connection to the source was made with a thin gold wire attached to the aluminum plate. The electrically-active area of the gate and source was 0.5 inch square. The nanocomposite is a circular pillar 1 mm in diameter and 140±10 µm tall as stenciled and shown in Figure 6-12. The recess in the source plate is 90 µm, so that the initial gate-source gap is 50±10 µm.

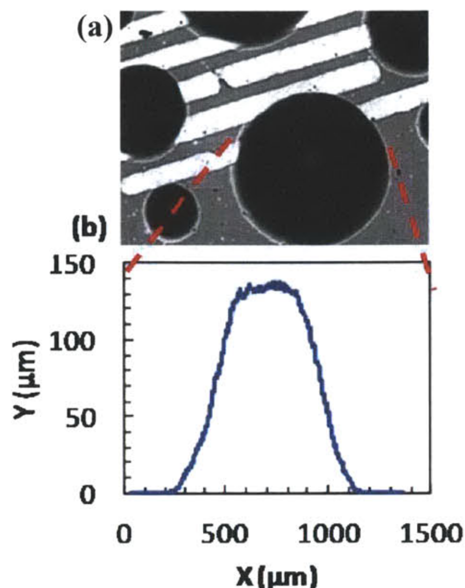


Figure 6-12: (a) Photomicrograph of patterned Ni- PDMS composite on top of Au electrodes using a 120 µm-thick chemically etched stainless steel mask with 200 µm, 500 µm and 1 mm diameter openings. The composite is prepared by mixing 1.0 g of PDMS with 1.5 g of nickel particles; (b) Surface profile of a patterned composite pillar was obtained with a profilometer.

6.5 Test Results

6.5.1 Material Tests

The mechanical properties of the nanocomposite doped with 60 wt% Ni were measured using the mechanical tester. With the source electrode in place, the squitch was compressed by the tester and the resulting force-displacement was measured as shown in the inset of Figure 6-13. Here, stress is force normalized to the area of the 1-mm-diameter pillar, and strain is displacement normalized to the 150-µm height of the pillar. Generally, the stress-strain relation of a nanocomposite pillar with fixed normalization is super-linear owing to the typical cone shape of a pillar formed by stenciling. Compressing the tip of the cone requires considerably less force than does compressing the base. On the other hand, in Figure 6-13 the relation is nearly linear, and is well approximated by a mechanical modulus of 465 kPa (corresponding to the solid curve in the inset of Figure 6-13) [150].

$$E_s = \frac{stress}{strain} = \frac{\sigma}{\varepsilon} = \frac{F / A_0}{\Delta L / L_0} \qquad (6\text{-}1)$$

where E_s is the Young's modulus (modulus of elasticity); F is the force exerted on an object under tension; A_0 is the original cross-sectional area through which the force is applied; ΔL is the amount by which the length of the object changes; and L_0 is the original length of the object.

During the mechanical testing, the drain-source conduction characteristics were also measured using an Agilent 4156C Precision Semiconductor Parameter Analyzer. The drain-to-source resistance, R_{DS}, was calculated from the measured characteristics shown in Figure 6-13. The scatter in the data at lower strains was likely caused by light-load intermittent contact during the experiment.

For large strain, R_{DS} settles to approximately 1 kΩ. This resistance is taken to be the combined nanocomposite-drain and nanocomposite-source contact resistance.

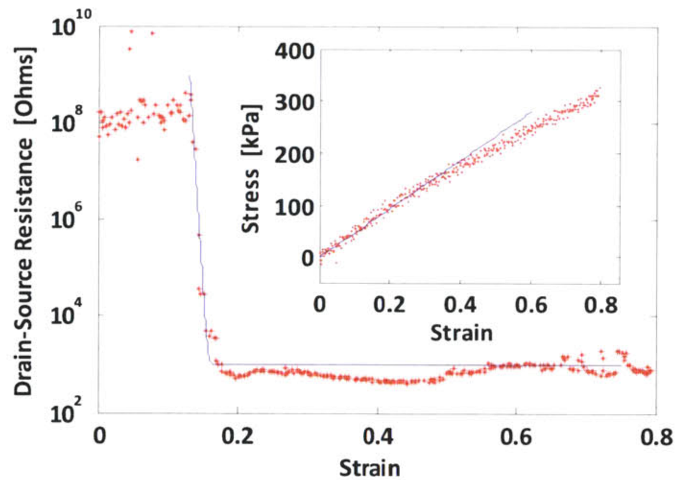


Figure 6-13: Resistance change of the Ni-PDMS composite with applied pressure. The inset shows the stress-strain characteristic of the polymer.

The apparent upper limit of resistance near 100 MΩ is the measurement limit. Very little resistance modulation occurred until a threshold was reached near 13% strain. At that point, R_{DS} fell quickly until it was limited by the contact resistance. An approximation for the dependence

of R_{DS} on strain is also shown in Figure 6-13 as a solid line. The approximation is given by

$$R_{DS} = R_S 10^{-\alpha\varepsilon} + R_C \tag{6-2}$$

where $R_S = 4.27\times10^{37}$ Ω is a resistance amplitude, α = 220 is a unitless coefficient, ε is strain, and R_C = 1 kΩ is the contact resistance.

6.5.2 Electrical Test

When tested as a squitch, the compressive force applied to the source is provided electrically by a gate-source voltage. To test the squitch as a voltage-controlled conduction device, it is first mechanically loaded with a mass near 10 g to bring the drain-source resistance nearer to the onset of conduction around 10 MΩ. This is necessary in the present macro-scale squitch due to the relatively weak electric forces available for actuation due to the large air gap. Such a mechanical assist will not be required as the squitch is made smaller. A gate-source voltage is then applied, and the drain-source conduction is measured, as shown in Figure 6-15. Figures 6-15 (a) and (b) plot the squitch *I-V* characteristics on linear and log scales, respectively, showing a 10,000-fold change in drain-source current with gate-source bias. The squitch output characteristics are of similar shape as those of conventional FETs. Figure 6-16 shows the extracted resistance of the squitch as a function of the gate-source voltage. A greater modulation would be possible with reduced contact resistance between the nanocomposite and the electrodes.

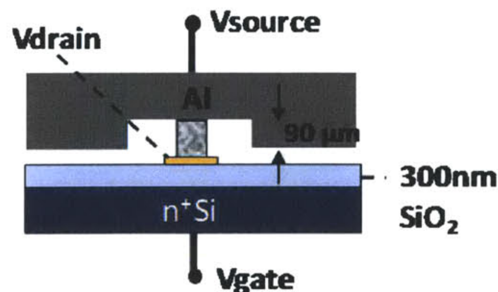


Figure 6-14: Schematic cross section of the first-demonstration squitch.

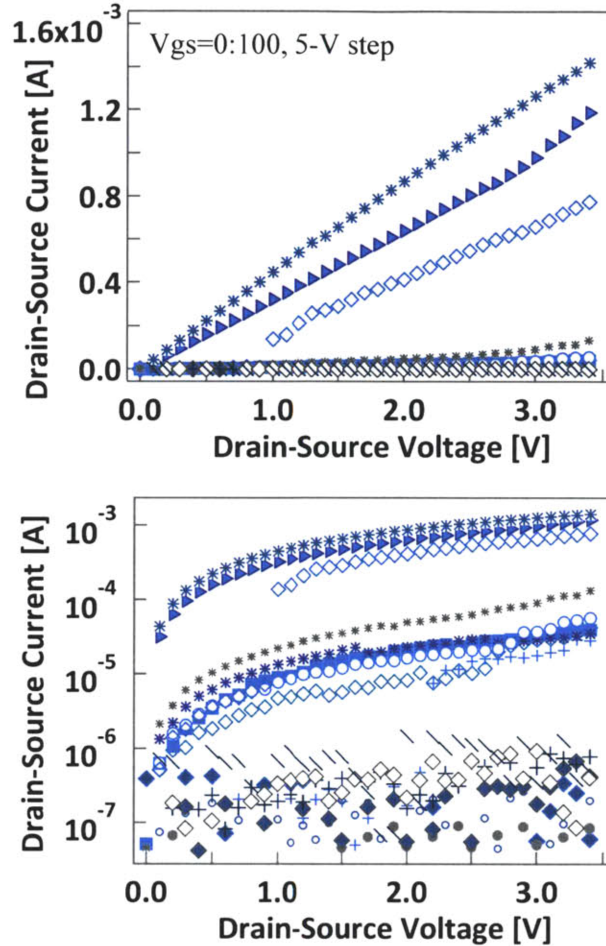


Figure 6-15: (a), (b) The squitch conduction characteristics on linear and log scales, showing 4 orders of magnitude change in the drain-source current by applying voltage to the gate terminal; the gate current during all experiments is less than 10 nA.

6.6 Modeling of the Device

The switching behavior in Figure 6-15 can be explained by using the material properties plotted in Figure 6-13. The understanding gained may then be used to extrapolate squitch performance as its dimensions are reduced. Modeling the squitch behavior, shown in Figure 6-16, begins by assuming a 4 MΩ drain-source resistance with zero applied gate-source voltage. At 4 MΩ, the resistance-strain curve fit of Figure 6-13 shows that the nanocomposite strain is 13.4%.

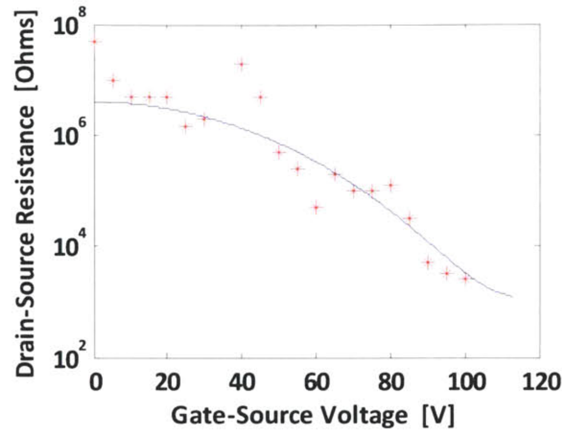


Figure 6-16: The drain-source resistance as a function of the gate-source voltage.

Then the stress-strain curve fit shown in the Figure 6-13 inset indicates that the mass applied to the source is 5.2 g. This mass is somewhat smaller than the actual 10 g mass used, likely due to tipping of the source electrode which causes part of the mass to be supported by source-substrate contact. Such tipping would not significantly affect the net electric actuation force due to the squitch geometry. Squitch behaviour was next modeled for non-zero gate-source voltages over the range of 13.4% - 16% strain. The approximation in Figure 6-13 is used to determine the total compressive load on the nanocomposite for strains in this range. This load is provided by the 5.2-g mass and the electric pressure of $0.5\varepsilon_0 E^2$ acting over the 0.5-inch-square actuation area of the gate and source. The required electric field E is thus determined as a function of strain. Given the original squitch geometry and the strain, the gap between source and gate is determined, which is then combined with E to determine the gate-source voltage required to produce the strain. Since the range of strain considered corresponds to closure of the gate-to-source gap by less than 1/3 of its zero-voltage value, pull-in is not experienced (see Appendix E). Separately, the approximation shown in Figure 6-13 is used to convert strain over the range of interest to squitch resistance. This permits drain-source resistance to be plotted against gate-source voltage using strain as a parameter. The result is shown as the solid curve in Figure 6-16. The good correspondence between the experimentally measured and theoretically predicted drain-source resistance indicates that the squitch behaves as expected.

6.7 Discussion & Conclusions

The electromechanical response of the electrically-actuated squitch measured in this study (Figure 6-16) is consistent with the material properties presented in Figures 6-13. Despite this, the squitch exhibits important irregularities that should be noted. First, the PDMS elastomer used to form the nanocomposite exhibits creep that takes time to relax. Consequently, prolonged gate-source actuation can result in conduction modulation that does not quickly return to the initial high-resistance state once the actuation is removed. Selecting a different composite with less creep may mitigate this issue. Second, after repeated cycling, the conduction characteristics of the squitch can change, often in a non-repeatable manner. This could be due to the movement of the Ni particles within the nanocomposite that can lead to coarsening and Ni agglomeration. For the most stable response it may be important to chemically bind the particles to the polymer – a procedure that was not undertaken in this dissertation. Finally, contact resistance between the nanocomposite and the drain and source contacts can be large, as seen in Figure 6-13. This limits the range of the achievable conduction modulation. By reducing the contact resistance, a range as large as 10^7:1 could be possible.

Mechanical dimensions of the squitch presented in this study are large, necessitating a significant actuation voltage to modulate conduction. It is therefore of interest to extrapolate squitch performance for smaller sized devices, and contemplate the impact of nanocomposites with a reduced mechanical modulus. Shrinking the squitch will require new fabrication techniques as well as the use of nanometer-scale metal particles or carbon fragments as dopants. At 100-V actuation shown in Figure 6-16, the electric force is approximately 7 mN while the mechanical force provided by the mass is 51 mN. To achieve fully electrical actuation then requires a voltage of approximately 285 V. However, if the squitch dimensions are scaled by a factor of 100, with the nanocomposite pillar 1.5 μm tall and 10 μm in diameter, ,and a 100-μm square gate and source, then the voltage required for full electric actuation would be reduced to 3 V.

With a softer nanocomposite further reductions in actuation voltage are possible. Additionally, improved contact resistance would lead to a greater conduction modulation. This procedure, combined with pull-in [150] would make it possible to design a squitch that exhibits conduction

modulation exceeding 1 decade per 60 mV- a fundamental limit for semiconductor switches. Another important characteristic of a squitch is its switching energy. For the experimental squitch, the required energy for switching can be calculated from [150]

$$E = \frac{1}{2} k \times (\Delta L)^2 = \frac{1}{2} \frac{E_s \times A_s}{L_0} (\Delta L)^2 \qquad (6\text{-}3)$$

where k is the spring constant; A_s is the original cross-sectional area of the Ni-PDMS pillar; ΔL is the amount by which the length of the pillar; and L_0 is the original length of it.

From 6-3, 654 nJ is required to strain the pillar to reduce its resistance to 3 kΩ. Given the steep slope observed in Figure 6-13 prior to the dominance of contact resistance, little additional energy would be required to obtain a much greater conduction modulation than is achieved in Figure 6-16. Since this energy scales as the pillar volume for a given strain, the energy required to achieve the same range of conduction modulation reduces to 0.7 pJ with the 100-fold size reduction. The switching speed of the squitch is fundamentally limited by the speed of sound [150] in the nanocomposite.

$$c = \sqrt{\frac{E_s}{\rho}} \qquad (6\text{-}4)$$

where E_s is a coefficient of stiffness (6-1); and ρ is the mass density.

With a modulus of 465 kPa and a mass density of 1600 kg/m^3, the speed of sound in the composite is estimated to be 17 m/s. Given a scaled-pillar height of 1.5 μm, the switching time would be limited to 0.18 μs. The actual switching times would be increased by the mass of the source.

In conclusion, the squitch is a voltage controlled conductor, much the same as a FET or a BJT but with a very large on-to-off conduction ratio and subthreshold swing (S) < 60 mV/dec- properties that allow for more aggressive supply voltage scaling and improvement in energy efficiency.

Chapter 7

7.1 Summary and Suggestions, Molecular Flash memories

7.1.1 Dissertation Summary

In this dissertation, the application of organic molecules and nano-particle/polymer composites for flash memory and switch applications was studied.

The field of molecular electronics has been growing for the past 30 years, particularly over the last decade. Numerous research activities are currently focused on molecule-only devices for logic and memory applications [151–154]. However, while silicon technology has a few more years before it reaches its fundamental limits [13], a hybrid Si/molecular approach might provide a smooth transition from the Si-only technology to the molecule-only technology. The hybrid approach, besides having all the advantages of the existing silicon technology, will also utilize the properties of molecules such as discrete quantum states available at low voltages, low power operation, and scalability to molecular dimensions [155]. In addition, the electronic properties of molecules combined with CMOS could give rise to novel functionalities [156].

It was demonstrated in this work that it is possible to store record-high charge densities per unit area in nano-segmented floating gates consisting of molecular thin films. Molecular materials are on the order of 1 nm in size, and their intermolecular spacing is just few angstroms. A floating gate consisting of a thin film of molecules would provide the advantage of a uniform set of identical nanostructured charge storage elements with high molecular area densities of

$\sim 10^{14}$ cm^{-2} that can results in several-fold higher density of charge-storage sites as compared to QD memory and even SONOS devices [5].

As discussed in chapter 2 significant QD-to-QD charge tunneling obviates the intended benefit of nano-structuring the gate electrode to preserve charge on individual QDs. QD-to-QD spacing limit of 5 nm restricts the maximum stored charge density in this kind of memories. As compared to QDs, which typically exhibit size and order variability, molecular films have the highly desirable consistency of size and morphology, which provide relative constancy in the electronic energy level structure of molecular films. The low density of free carriers in the molecular thin films and the high charge binding energy on individual molecules limit intermolecular interactions. The minimal overlap between the neighboring molecular electron wavefunctions contributes to the low organic thin film electron/hole mobilities, in the range of from 10^{-1} to 10^{-7} cm^{2}V^{-1}s^{-1}, which contributes to the immunity of stored charge to the structural defects in the neighboring areas of the device.

In this dissertation, capacitive memory structures were fabricated using archetypical molecular thin films with different charge storage energy levels and charge mobility including 3,4,9,10-perylenetetracarboxylic dianhydride (PTCDA), 3,4,9,10- perylenetetracarboxylic bis-benzimidazole (PTCBI), tris-(8-hydroxyquinoline) aluminum (Alq_3), and fullerene (C_{60}).

High charge retention density and good cycling endurance over 10^5 were demonstrated, which meets the industry's standard margin of endurance. It was established that the performance of the device can change dramatically based on the thickness of the layers due to the exponential dependence of the tunneling current. Modified memory devices with 3- nm thick Alq_3 floating gate layer were fabricated. It was exhibited that charge storage in tris(8-hydroxyquinoline) aluminum (Alq_3) molecular floating gates can reach record-high densities of 5.4×10^{13} cm^{-2} that are manifested as 7.8 V threshold voltage shifts in memory capacitors. This storage capacity significantly exceeds any previously reported for molecular- or quantum dot-based memory devices.

Also, charge retention dependency on the lateral mobility of organic thin films was demonstrated, suggesting the use of low mobility materials like PTCBI and Alq_3 for these kinds of memories.

Using the surface potential mapping by Kelvin force microscopy (KFM) the charge diffusion

and the corresponding carrier diffusivity in Alq_3 films was measured to be less than $D_e \sim 3.6\times10^{-11}cm^2.s^{-1}$, all together indicating that Alq_3 films could act as effective nano-segmented floating gate in nonvolatile flash memories.

Per our simulations, large effective electron mass of organic materials reduces the charge loss through the direct tunneling during retention mode which allows us to scale down the thickness of the tunneling oxide less than 6 nm which is the minimum thickness of the tunneling oxide that can be reached in conventional floating gate memories.

I was experimentally demonstrated that it is possible to engineer the memory behavior of the device by using different molecules together to increase the charge storage capacity of the molecular floating gate and to reduce their π-orbital overlap and consequently the lateral charge mobility within molecules. Among the tested materials, C_{60} containing memories showed the largest hysteresis window and better endurance. The *C-V* measurements indicated a remarkably large hysteresis window of 11.8 ± 0.1 V for P/E condition of −11 V/11 V. However, it was substantiated that the high mobility and consequently low retention time of C_{60} memory devices compromises their otherwise remarkable memory characteristics.

Using the same structure, PTCBI containing memories with lower lateral mobility showed comparatively smaller hysteresis window. The herringbone packing of PTCBI molecules separates the π-electron clouds on molecular neighbors, which results in the low electron mobility of PTCBI thin films. Such low charge mobility provides the same advantage as earlier demonstration of QDs in floating-gate memories, namely, if a defect exists in the tunneling oxide below the floating gate, charges in the floating gate are unlikely to transport laterally through the low-mobility molecular film, reducing the likelihood of discharge through the oxide defect. In this dissertation, it was demonstrated that it is possible to engineer the memory behavior of the device by using different molecules together to increase the charge storage capacity of the molecular floating gate and to reduce the lateral charge mobility within molecules.

The charge mobility was measured within the molecular layer by forming thin film transistor structures with the molecular films as the semiconducting layer. From the transistor current-voltage response, the lateral electron mobility in the range of 0.06 - 0.15 $cm^2V^{-1}s^{-1}$, 0.96-3.6 × 10^{-4} $cm^2V^{-1}s^{-1}$ and 0.96-2.4 × 10^{-4} $cm^2V^{-1}s^{-1}$ were derived in C_{60}, PTCBI and PTCBI:C_{60}, respectively. It was exhibited that mixed layer PTCBI:C_{60} memories have the remarkable

properties of C_{60} memories while the mobility is as low as PTCBI containing memories.

These results may lead to an approach toward further miniaturization of non-volatile memory by using molecules as segmented charge storage elements in the floating gate flash memory technology.

7.1.2 Possible Future Direction

Further studying and understanding the memory behavior of the organic molecules, measuring the trapping levels within the molecules and studying the dependency of charge retention versus temperature can be the next steps of this project.

A large variety of organic molecules are available which might be good candidates for memory application which should be investigated.

Retention time and programming time of these memories can be further improved by

- using multilayer of organic molecules to engineer the energy level of the floating gate
- mixing molecules and decreasing their lateral mobilities,
- using bandgap engineered bottom oxide,
- using multi-layer of nitride and high-k material for the top oxide with high-metal work function

Fabricating molecular memory transistor using gate-last process will allow us to do more accurate timing measurement. It is also believed that patterning the molecular floating gate and reducing the memory cell area will have a significant effect on increasing the charge retention time of these memory devices.

Also, it should be noted that molecules are prone to react with surrounding molecules such as oxygen and water. These reactions change the chemical structure and therefore the electronic properties of the semiconductor, usually with a detrimental effect on the performance of the device. As a result, the performance of the device declines over time.
Lifetimes can be extended by encapsulating the devices with protective membranes that slow the transmission of molecules like water.

7.2 Summary and Suggestions, Squitch

7.2.1 Dissertation Summary

The design, fabrication, testing and evaluation of a MEMS switch that employs a metal-polymer nanocomposite as its active material were presented in this dissertation. The nanocomposite was formed by doping a polymer with conducting nanoparticles. By mechanically compressing the nanocomposite, 4 orders of magnitude change in the conductivity was observed. In this demonstration the compressive squeeze was applied with electric actuation.

Since squeezing initiates the switching behavior, the device is referred to as a “squitch”.

Modifications to the type and the relative quantity of the polymer and conductive particles used and the distribution of the particles in the polymer resulted in a change in mechanical properties of the material and hence the squitch performance. Further exploring these effects will contribute to developing a composite that yields an optimal device performance.

7.2.2 Possible Future Directions

For this first squitch demonstration, the electromechanical properties of the elastomer composite material were optimized through trial and error by mixing the polymer elastomer with different amounts of curing agent and Ni particles. Much of the future should focus on perfecting the elastomer materials, retooling the fabrication sequence, and the elastomer MEMS designs to enable performance at lower operating voltages, with less power and with even more rapid transition from the “on” to the “off” state.

7.2.2.1 Device design

Figure 7-1 shows example squeezing switch drain-to-source resistances as a function of gate-to-source voltage for different gate capacitor air gaps. In this figure for a device with the area of

200 μm^2 the squisbable material thickness, gate-source electrode gap, insulator bumper-stop gap were reduced by a factor of 3 but the lateral dimensions (area) were not changed. Reduced gate capacitor air gap increases force, lowering the turn-on voltage.

Scaling the size of the device, alternative device structures, and applying new materials may optimize the performance of the device.

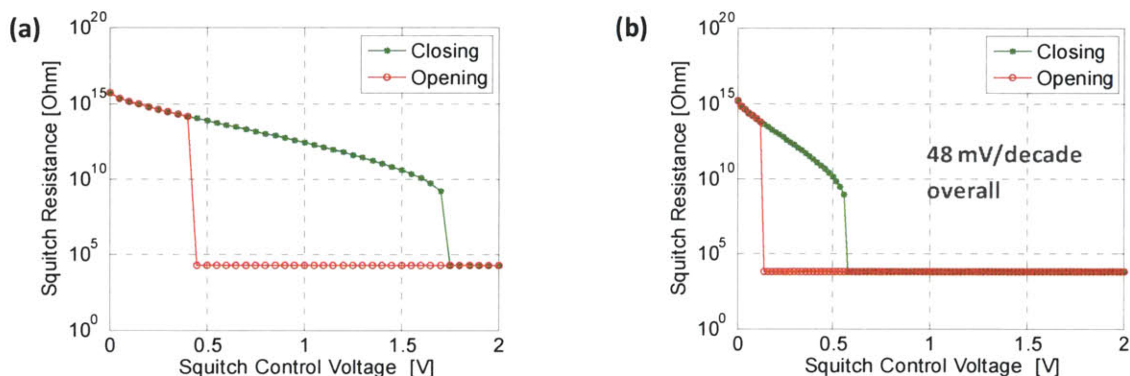


Figure 7-1: Simulation results of resistance vs. gate voltage of the 200 μm^2 devices with (a) 500 and (b) 167 nm vertical profile.

7.2.2.2 Material

It is necessary to replace macro-sized fillers used for the first demonstration with nanometer-sized fillers to scale the device. The change in particle diameter, layer thickness, or fibrous material diameter from micrometer to nanometer changes the surface area/volume ratio by three orders of magnitude. At this scale, there often is a distinct size dependence of the material properties. In addition, the properties of the composite became dominated by the properties of the interface or interphase when the interfacial area drastically increased. Also, anchoring the conductive particles to the elastomeric matrix (seen Figure 7-2) is essential to improve the electromechanical properties of the composite and reduce the performance variations during operation. Filler dispersion and metal-polymer interaction can be enhanced through use of coupling agents such as Allyltrimethoxysilane (ATS) or Vinyltrimethoxysilane (VTS) [157].

The next steps in this project will be screening and optimization of elastomer MEMS materials

and conducing atomic-scale molecular dynamics simulations for a wide range of polymer/nanoparticle blends as a function of stoichiometry, chemical functionalization, and processing conditions.

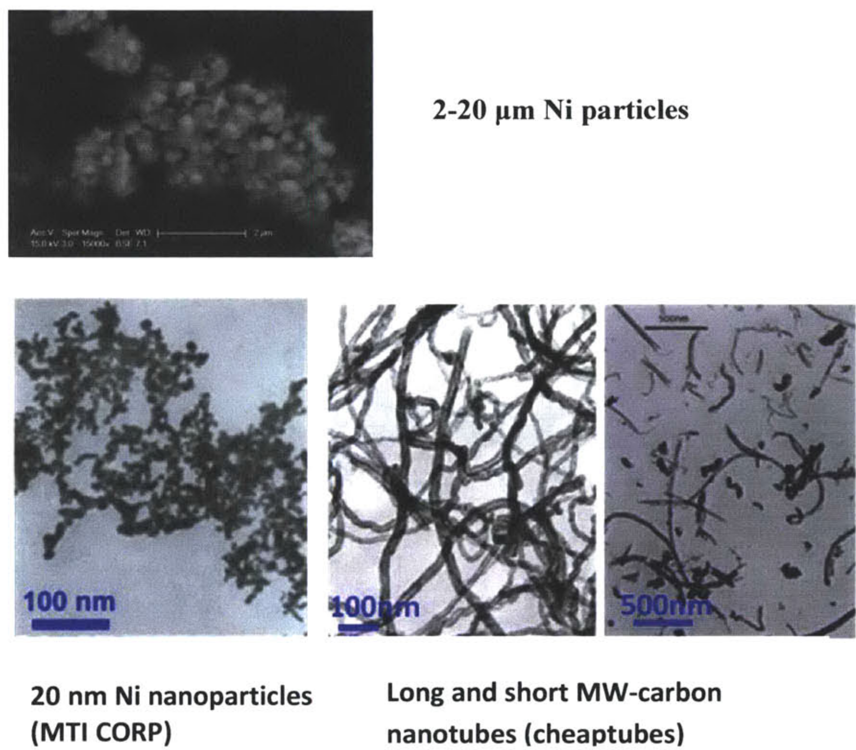


Figure 7-2: SEM image s of filler particles such as Ni nanoparticles and carbon nanotubes that can rep lace Ni microparticles currently used to provide an optimized composite for squitch application.

Since the electronic transport in these materials is strongly coupled to the formation of the percolation networks and their response to strain, the primary focus will be the prediction of morphology at the atomic-scale in these materials and their response to variations in temperature and pressure.

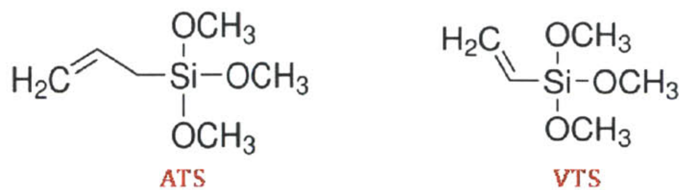


Figure 7-3: Coupling agents suitable for composite synthesis

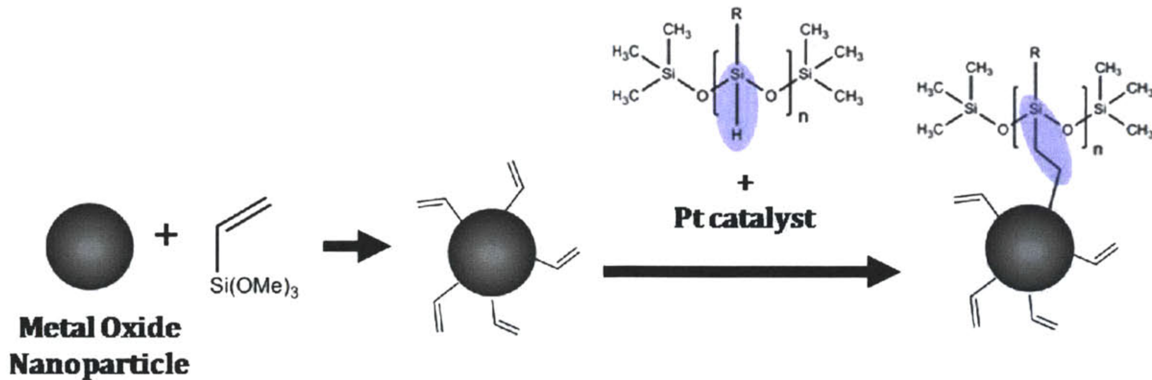


Figure 7-4: Coupling of filler particles to PDMS.

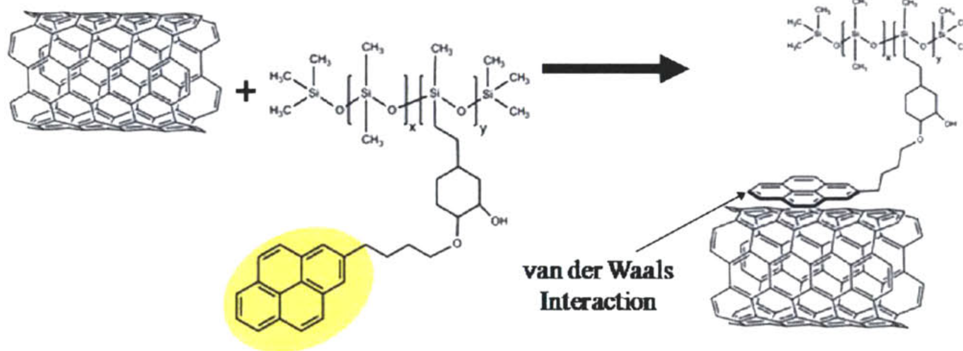


Figure 7-5: Coupling of carbon nanotubes to PDMS [158].

7.2.2.3 Patterning of PDMS-Based Conducting Composites

In order to make squitch devices in small devices, it would be necessary to develop a nanocomposite pattering method. Photoresist lift-off and nanoimpronting techniques that may be a good approach will be described briefly in this section.

7.2.2.3.1 Photoresist Lift-off Technique

The SEM images of different patterns fabricated with nano-particle/PDMS composites are shown in Figure 7-6, where it can be seen that the dimensions of the patterns can range from ten to hundreds of micrometers, indicating the capability to microfabricate conducting devices of different sizes [159]. The conductive composite patterning procedure is schematically illustrated in Figure 7-6.

First a thick layer of photoresist, such as AZ4620 is patterned on a glass substrate using a standard photolithographic technique, for the purpose of forming a mold to pattern the conductive composite. After baking, the mold is treated with a de-molding reagent, tridecafluoro-1,2,2,2-tetrahydrooctyl-1-trichlorosilane. The conducting composite is synthesized by mixing PDMS and nano-particles in different concentrations to form conductive composite gels.

The gels are then plastered on the mold. Unnecessary portions of the gel are removed from the mold surface (e.g., by using a blade) to ensure that only a clean pattern is left in the mold. After baking, the gel is cured into a solid. The photoresist is then removed by dipping the whole mold substrate into acetone, then ethanol, and subsequently washing with deionized (DI) water. After baking, only PDMS-based conducting composite is left on the substrate.

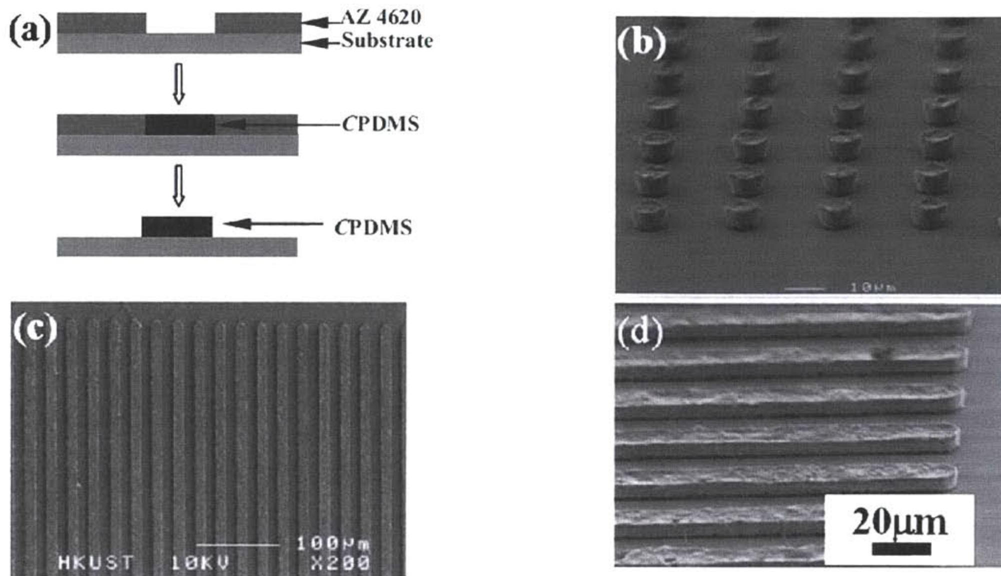


Figure 7-6: (a) Process flow chart illustrating the patterning of conductive PDMS by soft lithography. (b–d) SEM images showing the various fabricated conductive patterns [159].

7.2.2.3.1 Nanoimprinting Technique

Nanoimprinting can also be used for patterning the conductive polymer. A mold with a nanoscale relief pattern can be prepared by interference lithography.

In the simplest implementation of interferometric lithography (IL), two coherent light beams are incident on a resist-coated substrate at their point of intersection (Figure 7-7). Interference between the two beams produces a sinusoidal intensity distribution that can be used to form grating patterns in a photoresist film. The period of the grating is defined by the vacuum wavelength of the exposing light, the angle of intersection of the beams, and by the refractive index n of the medium in which the interference takes place.

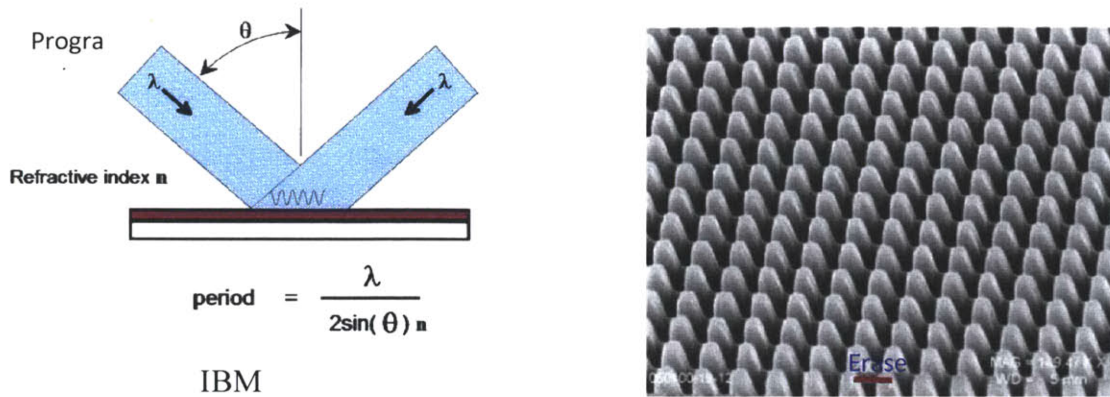


Figure 7-7: (a) Schematic diagram of interferometic lithography; (b) SEM image of 2D mask fabricated at Nanonex using interference lithography. The pattern period can be as small as 200 nm.

The SEM image of a 2D mask fabricated using interference lithography. The mask can be used to imprint nanoscale features in the polymer of interest. The mold is pressed to deform the polymer, and a replica of the mold is left in the polymer. By heating the substrate at 90 °C, the polymer is cured and after removing the mold the replica of mold left in the polymer.

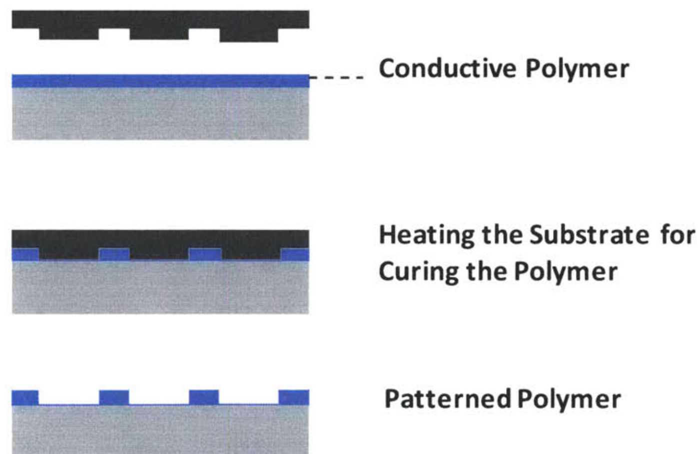


Figure 7-8: Patterning conductive polymer using nano-imprinting technique.

7.2.2.4 Future Applications of Squitch

Mechanically-actuated logic switches (that were named squeezable switches, or “squitches”)

can be used as building blocks for both analog and digital logic circuits.

This low-loss squishable MEMS switch can be used for power management of digital IC's. Lowering power consumption in digital IC's is becoming increasingly important in order to increase mobile device battery life and to decrease cooling costs for enterprise server farms. Power gating of digital logic using MEM relays might provide significant power savings over conventional MOS power gating.

The squitch can also be used as the integrated electronics in sensory skins for signal processing and the local amplification of sensor signals. The lightweight and flexible sensory skins are capable of recording external pressure, sound waves, liquid flow, or changes in temperature or chemical environment. Formed as an array of integrated detectors embedded in a flexible matrix, sensory skins will enable phased-array detection for directional location of external stimuli. The squitch can be used to construct analog and digital circuitry that can then process the signals produced by the sensors. The objective is to develop environmentally responsive sensory skins that both probe their environment and process the sensed signals, mimicking the capabilities of living skins that possess both sensory cells and a signal-processing "nervous system". Such skins could enable the development of devices like sensors of the stresses and strains in parachute fabrics, unobtrusive large-scale "listening" devices, wearable sensors of the battlefield environment for soldier protection, and wearable sensors of soldier health.

7.2.2.4.1 Digital Logic Example

This section outlines how CMOS-like logic can be implemented with a squitch. The specific example shown is an inverter. However, the design of more complex logic follows directly from the principles of CMOS logic design.

As mentioned above, a squitch can be turned on by applying either a positive or negative gate-to-source voltage, thereby developing an attractive force between these electrodes. This makes it possible to implement CMOS-like logic using two identical squitches, as distinguished from using complementary switches like the p-type and n-type FETs used in CMOS technology. This is illustrated in Figure 7-9.

Considering the simulated resistance-voltage characteristic of squitch shown in Figure 6-17, it is possible to define a lower and upper gate-to-source threshold voltage, near 0.1 V and 0.6 V,

respectively. With the application of a high input voltage magnitude, above the upper threshold,

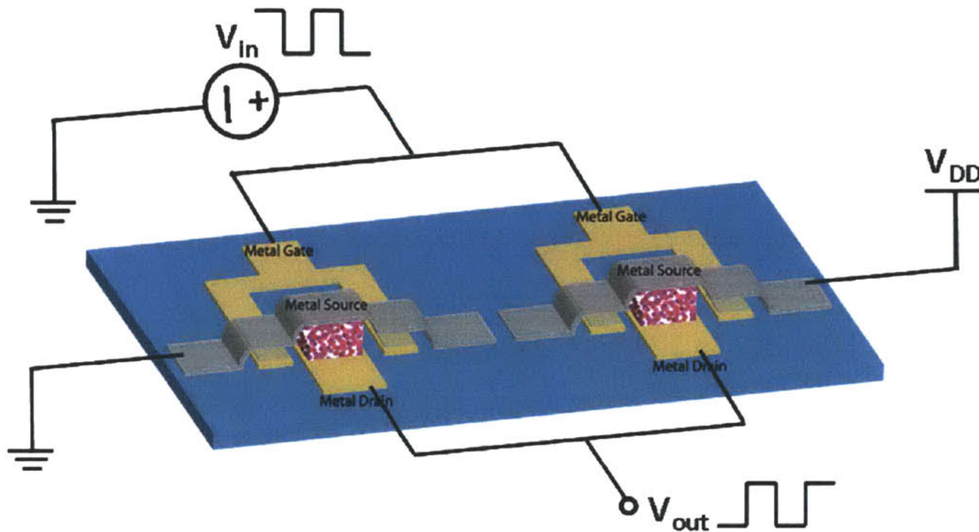


Figure 7-9: An embodiment of a digital inverter using a squitch.

the squitch will turn on; with the application of a low input voltage magnitude, below the lower threshold, the squitch will turn off. This switching characteristic, combined with the fact that the source electrode of one squitch in Figure 7-9 is grounded, while the source electrode of the other squitch is powered by the supply, causes the circuit shown in Figure 7-9 to act as a logic inverter.

Again, it is the absolute value of the gate-to-source voltage of the squitch that determines its conduction. Note that the low-side squitch turns on with a high input voltage, while the high-side squitch turns off with a high input voltage. The reverse is true for a low input voltage. Thus, similar to CMOS logic, the static power consumption of squitch-based logic will be very small since one of the two squitches is always in its off state.

7.2.2.4.2 Analog Amplifier Example

The squitch can also be used to build analog circuitry. The specific example shown here is a single-stage amplifier that mimics a common-source FET amplifier and a common-emitter BJT amplifier. However, far more complex analog circuits such as operational amplifiers, filters, multipliers, oscillators, power supplies, and others can be built as multi-stage squitch circuits

following the general principles of analog design.

In analog electronics, a common-source amplifier is one of three basic single-stage amplifier topologies, typically used as a voltage or transconductance amplifier. In this circuit the gate-to-source voltage of the transistor serves as the input, and the drain-to-source voltage serves as the output. The drain is connected to a power supply through a pull-up resistor, and the source is grounded.

Considering the simulated resistance-voltage characteristic of squitch shown in Figure 7-10, it is possible to define a lower and upper threshold voltage, near 0.1 V and 0.6 V, respectively. Below the upper threshold as a transconductance amplifier, the input voltage smoothly modulates the resistivity of the composite by creating an electric field between gate and source electrodes that compresses the composite. The output voltage across the drain-to-source electrodes of the squitch then varies in accordance with the power-supply voltage divider formed by the series connection of the squitch composite and the pull-up resistor. An implementation of such an amplifier is shown in Figure 7-10.

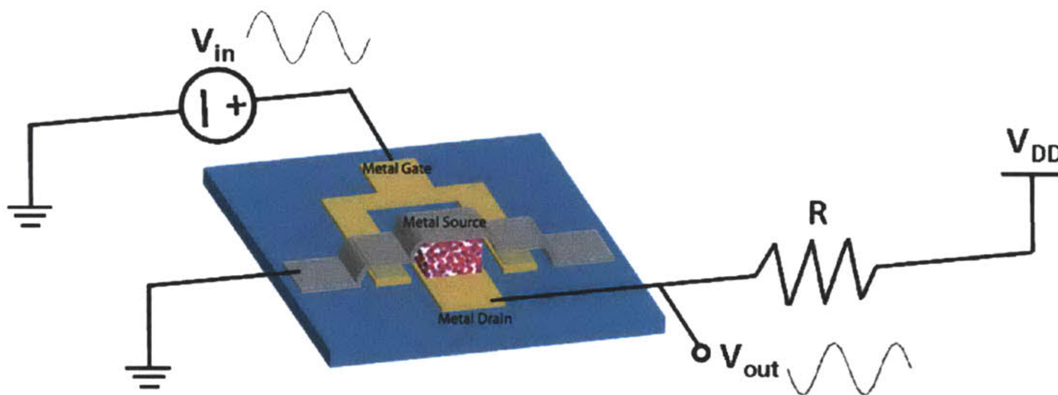


Figure 7-10: An embodiment of a common source analog amplifier.

7-3 Contributions

The main contributions of this dissertation are summarized as follows:

- Analyzing the use of molecular thin film structures as nanostructured charge storage elements in a capacitive floating gate technology as candidate materials for high storage capacity memory cells
- Process development and fabrication of molecular MOS capacitors
- Demonstrating high-density charge storage on molecular thin films
- Demonstrating durability over 10^5 charging/discharging cycles, showing the stability of organic films to repeated cycling
- Demonstrating the dependency of charge retention time on the lateral charge diffusion of organic molecules that for the first time experimentally confirms that nano-segmented floating-gate structures benefits the memory retention.
- Fabrication of memories with increased storage capacity and reduced lateral charge diffusion achieved by the addition of dopant molecules for rearranging molecules and their π-orbital overlaps.
- Visualization of charge storage within organic molecules and direct probing the time-evolution of the nano-scale distribution of trapped charges within molecules using the Kelvin force microscopy.
- Process development for molecular memory transistors using gate-last process
- Fabrication of new types of micro electro mechanical switches using nano-particle/polymer composites, with large on-to-off ratio for potential application in large area and flexible substrate electronics

Appendix A

A-1 Substrate Cleaning

1. Solvent cleaning of substrates
   - Sonicate for 5 min in de-ionized (DI) water with detergent
   - Spray with DI water
   - Sonicate for 5 min in DI water
   - Spray with DI water
   - Sonicate for 2 min in acetone I
   - Sonicate for 2 min in acetone II
   - Immerse for 2 min into boiling isopropanol I
   - Immerse for 2 min into boiling isopropanol II
   - Dry each substrate under Nitrogen (N_2) or dry air flow
2. Expose clean substrates to Oxygen plasma for 5 min. This step removes any residual organics that were not dissolved in the solvent cleaning step as well as creates a hydrophilic surface, crucial for the next step.

A-2 Purification of organic small molecules

Some organic materials contain impurities as received from the supplier. These impurities can be removed by thermal gradient sublimation. Following this procedure results in high-purity organic material suitable for device manufacture.

A turbo pump is used to maintain high vacuum inside a quartz purification tube. The tube is heated by a tube oven capable of applying a temperature gradient across the tube. High-purity material is obtained in the following way: The organic source material is heated above its sublimation temperature in Zone 1 and is deposited in Zone 2 where the temperature is kept below the sublimation temperature. Residual impurities remain in Zone 1 and volatile impurities

collect in Zone 3, which is kept at a temperature well below that of Zone 2. The high-purity organic can be collected off the sidewalls of the quartz insert tube with a clean spatula.

Appendix B

Fabrication of Memory Transistors Using Gate-Last Fabrication Process

As the next step in the fabrication of molecular memory transistors, it is necessary to design develop a CMOS compatible process. As mentioned previously, in demonstrating molecular memory devices, materials were deliberately chosen that are compatible with today's memory technology processing, enabling easy insertion of the demonstrated structures into today's microchips. These molecules are stable at temperatures as high as 400-450 °C. Due to this temperature limit, a gate-last fabrication process should be used in order to fabricate organic containing memory transistors.

The schematic cross section and fabrication process flow of gate-last molecular memory transistor is shown in Figure B-1.

The fabrication starts with RCA cleaning of 150 mm p-type Si wafers, followed by deposition of low temperature CVD oxide as the field oxide. Then, the filed oxide is selectively etched to expose the silicon surface on which the transistors will be created. Before the field oxide deposition, boron is implanted into (field implantation) in order to decrease bulk leakage. Following this step, the surface is covered with a thin layer of thermal oxide. A dummy poly-Si gate is initially formed on the Si substrate and then replaced by a metal gate. When the dummy poly-Si gate exists, source and drain regions are defined by P implantation.

After the source-drain activation, the sacrificial poly-Si layer is removed. The underlying gate dielectric is also removed.

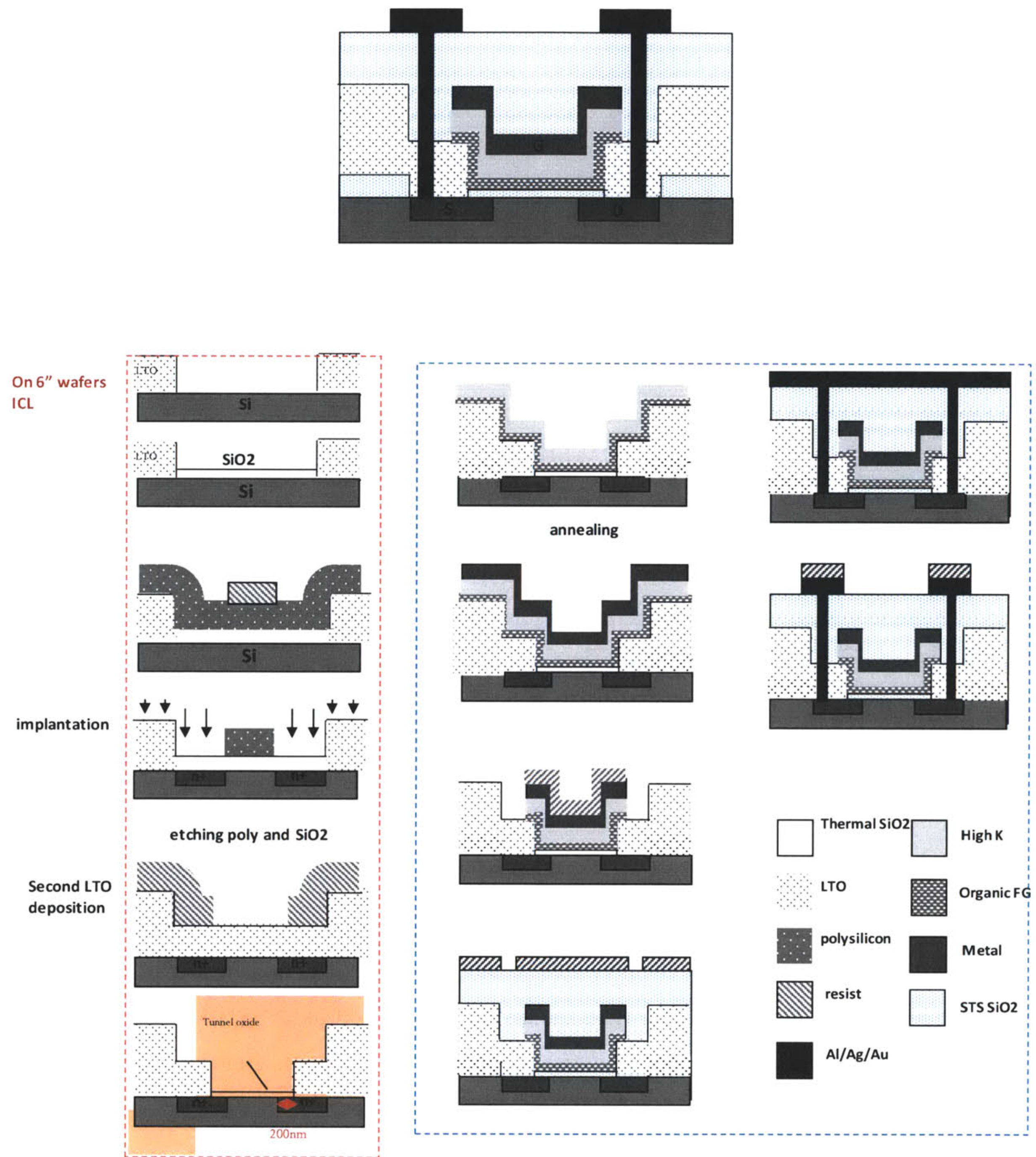


Figure B-1: The cross section of the designed molecular memory transistor and the process flow used to fabricate memory transistors.

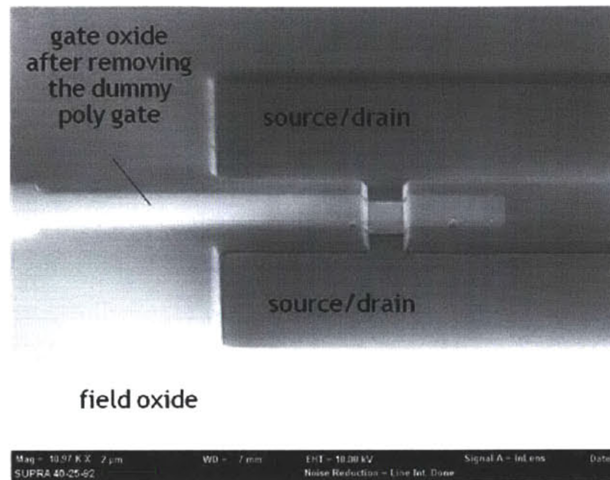


Figure B-2: SEM image of the device after removing the dummy gate; the dummy gate is used tin order to define sour-drain regions.

In order to make further alignments easier, a 100-nm thick layer of LTO is deposited followed by patterning and etching it in the channel area. In the opening left the new tunnel oxide layer is grown. These oxide steps allow continuation of fabrication in other labs with less accurate mask aligner. The metal pattern can be larger than the actual channel length; and the overlap between the gate electrode and source-drain region due to the thickness of this step will be negligible. Also there would be no need for patterning the molecular layer.

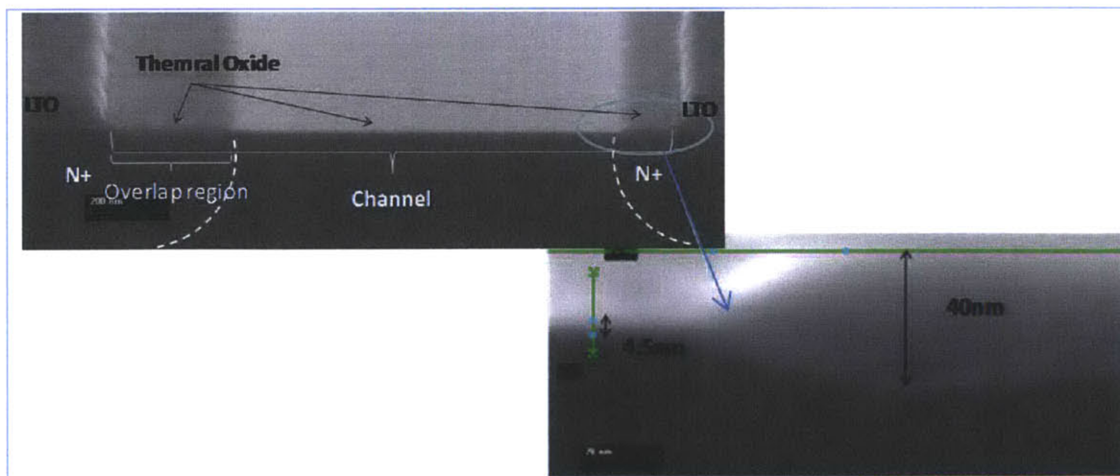


Figure B-3: SEM image of the channel region showing the thicker oxide in source and drain region.

The organic layer is just few nanometers thick and by using thermal evaporation system for deposition of this layer the amount of the material will be negligible on the side walls.

This opening is 200 nm wider (on each side) than the actual channel length that causes gate-source and drain-source overlap capacitance. The issue is minimized during thermal oxide growth. The growth rate in the dope area is higher which leads to a 40 nm-thick thermal oxide on these regions by growing 4.5 nm oxide in the channel area (See Figure B-3). By having such a thick oxide layer overlap capacitance will not be significant.

After tunnel oxide growth, the organic layer is deposited in the organic evaporator system discussed in chapter 3, followed by the deposition of the Al_2O_3 layer as the control oxide. The devices are annealed to improve the quality of the oxide (see chapter 3). After deposition and patterning the top electrode, 300-nm of encapsulating plasma-enhanced chemical vapor deposition (PECVD) oxide is deposited.

A SEM image of the device cross section is shown in Figure B-4.

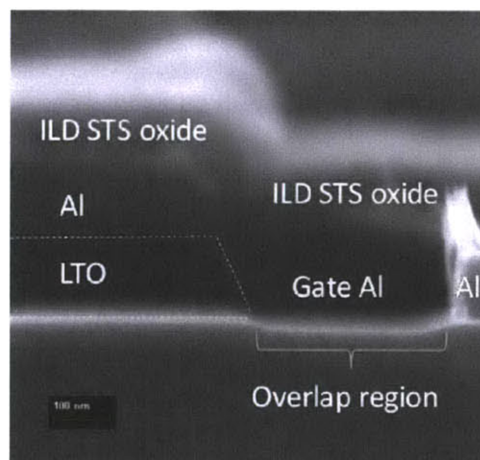


Figure B-4: SEM cross section of the transistor.

The insulating oxide layer is then patterned in order to provide contact windows for the drain and source junctions. The surface is covered with evaporated aluminum that will form the interconnects. Finally, the metal layer is patterned and etched, completing the interconnection of the MOS transistors on the surface. The devices are then annealed at 300 °C at nitrogen ambient

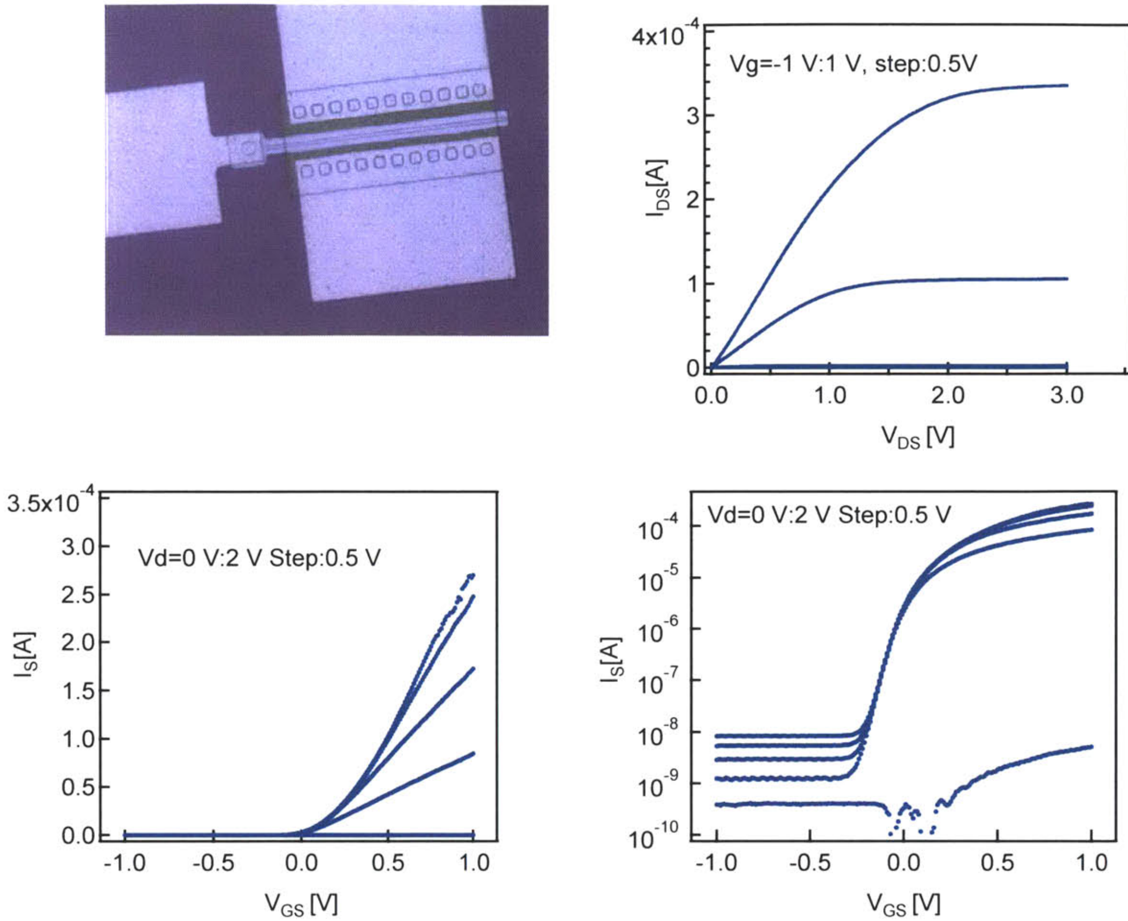


Figure B-5: (a) Microscopic image of a transistor, (b) output characteristics (I_{SD} - V_{DS}) and (c) transfer (I_{SD}- V_{GS}) for a transistor fabricated using gate-last process. The devices have not exposed to high temperature after source-drain activation.

for 30 min for improving the contact resistance. The transfer (I_{SD} - V_{GS}, in both linear and logarithmic scales) and output (I_{SD} -V_{DS}, in linear scale) characteristics of a device with channel length of 30 μm and channel width of 100 μm are shown in Figure B-5. The devices with the channel length in the range of 500 nm-100 μm were fabricated.

In this section the fabrication of the control transistors was demonstrated by describing a process that does not necessitate high temperature annealing after source-drain activation. This is a process that is compatible with using high-*k* and organic materials as the control oxide and the floating gate of the memory transistor. The investigated molecules have a thermal budget that can withstand post-metal gate annealing. The next step of this project will be the insertion of the

organic layer as the floating gate into the gate oxide and fabrication of the molecular memory transistors.

Appendix C

Studying the Effect of Annealing on Organic Molecules

The effect of annealing on PTCBI thin film was studied by monitoring the morphological change of the 30-nm-thick PTCBI layer deposited on SiO_2/Si substrate. The samples were annealed at 250 °C, 300 °C and 350 °C for 3 hours. The microscopic image of the samples after annealing is shown in Figure C-1 (a). Although PTCBI molecules form needle-like crystals by annealing, samples with a 15-nm thick Al_2O_3 capping layer have a very smooth surface, suggesting that the Al_2O_3 prevents the formation of the crystalline region.

The annealing effect on molecules has been studied using photoluminescence measurements. A significant increase in the photo-luminescence was observed by annealing the un-encapsulated PTCBI films. The photo-luminescence intensity drops due to evaporation of the PTBI for the device annealed at 400 °C. However, no significant change was observed in the photoluminescence intensity of the organic thin films (that were covered by the Al_2O_3 layer) before and after the annealing in N_2 ambient at 300 °C, 350 °C, and 400 °C for 3 hours confirming that annealing causes no degradation in organic layer, as shown in Figure B-2.

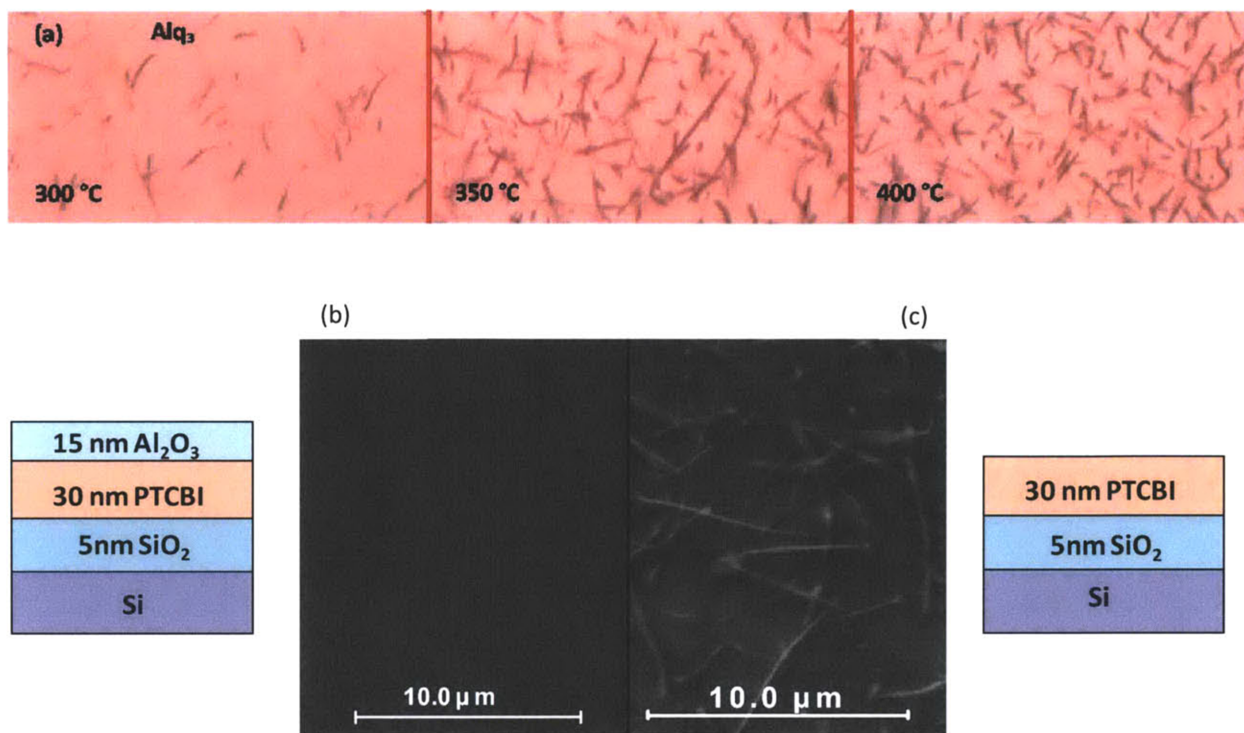


Figure C-1: (a) Microscopic images of un-encapsulated PTCBI films (30nm thick) annealed in N_2 ambient at 300 °C, 350 °C,400 °C for 3 hours; SEM images of a sample annealed at 350 °C (b) covered with Al_2O_3 layer and (c) without Al_2O_3 layer.

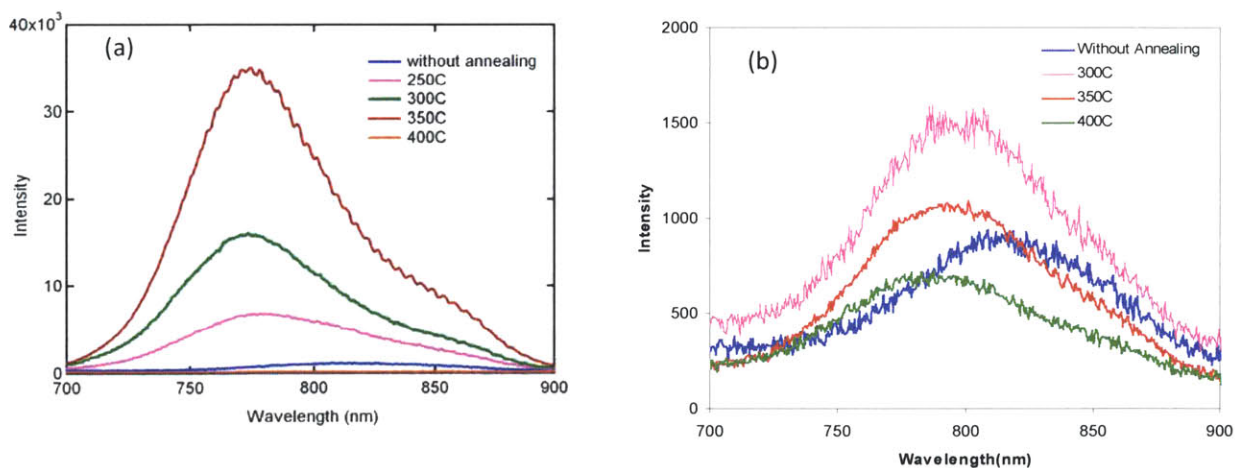


Figure C-2: Luminescence as a proxy of film stability for (a) a sample without Al_2O_3, (b) a sample cover by Al_2O_3 layer.

Appendix D

Sample Preparation for TEM Cross Section Imaging

Transmission Electron Microscopy (TEM) is a technique that uses an electron beam to image a sample. High energy electrons, incident on an ultra-thin sample allow for image resolutions that are on the order of 1 - 2 Angstroms. TEM has better spatial resolution and is capable of additional analytical measurements as compared to SEM; however it requires significantly more sample preparation.

The wealth of information available from these experiments is impressive, although working with them is more time consuming than many other common analytical tools. The sample preparation method used in this dissertation is explained here.

To protect the material surface while achieving a cross section, a sandwich of two samples was made. Sandwiching technique also allows doubling or multiplying the observable material quantity in the same object. After cutting the specimen to the desired dimensions, a thin glue film was spread over each surface to be protected. A specimen-glue-specimen sandwich was formed when the two coated surfaces are put together face to face (Figure D-2).

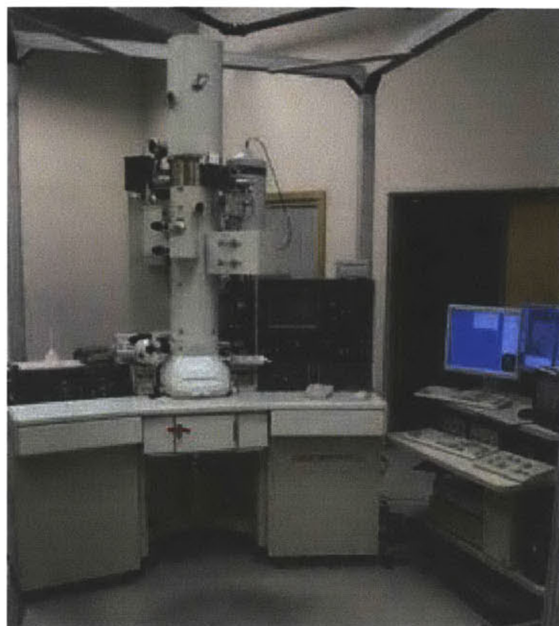


Figure D-1: JEOL 2010 FEG TEM system used in this dissertation.

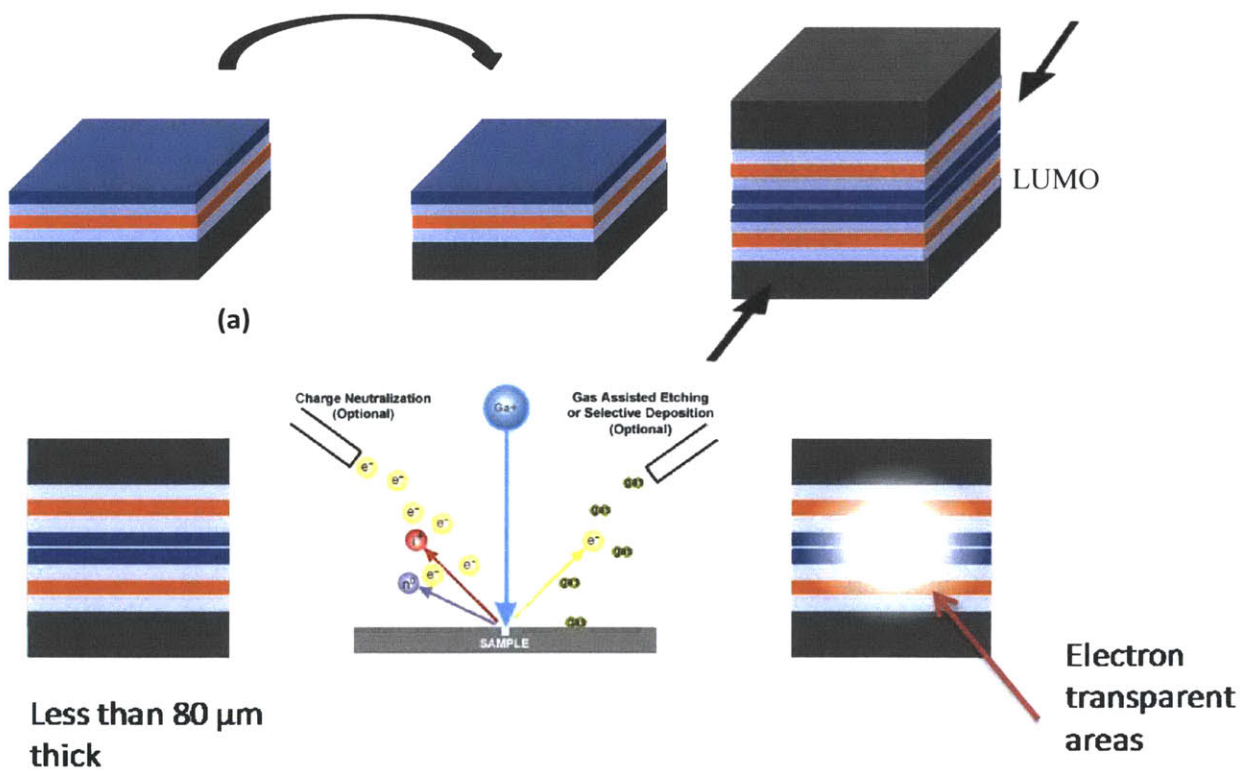


Figure D-2: Sample preparation for TEM cross section imaging.

This sandwich was introduced in a press applying a 250-300 g load in order to obtain a very thin glue film. To thin down a specimen to electron transparency, ion beam thinning was used. The thin edges of the hole produced by the ion bombardment are electronically transparent and can be used for cross section imaging. Before making a hole in the sample by ion beam, the thickness of the specimen was reduced to less than 80 μm by mechanically polishing the specimen by sand paper. The interaction of an accelerated ion beam with the specimen causes removal of its surface atoms, thus leading to relief polishing and to suppression of the possible mechanical damages introduced during the preparation.

Appendix E

Electrostatic Actuators and Pull-in

Any electric charge creates an electric field around it. In addition, any electric field applies a force to any charged particle. This principle, widely known since Maxwell's era, has not been used very much during the past decades, but MEMS has a high interest in using electrostatic actuators.

Electrostatics is the most widely used force in the design of MEMS where is also used in micro-resonators, switches, micro-mirrors, and accelerometers to name a few. Almost every kind of micro-actuator has one or more electrostatic actuation based version.

A schematic of an electrostatic actuator is shown in Figure E-1. When voltage is applied over the capacitance, electrostatic force will work to reduce the plate separation.

At small voltages, the electrostatic voltage is countered by the spring force; however, as voltage is increased the plates will eventually snap together.

Estimating this pull-in voltage V_{act} and the plate travel distance before pull-in effect is required for a successful design of the squitch (see Figure E-2). Electrostatic and mechanical forces are defined in this structure as:

$$F_{elec} = \frac{1}{2}\varepsilon_0 A_A \left(\frac{V_{act}}{Z}\right)^2 \tag{E-1}$$

$$F_{mech} = k(Z - Z_0) = \frac{E_S A_S}{D_S}(Z - Z_0) \tag{E-2}$$

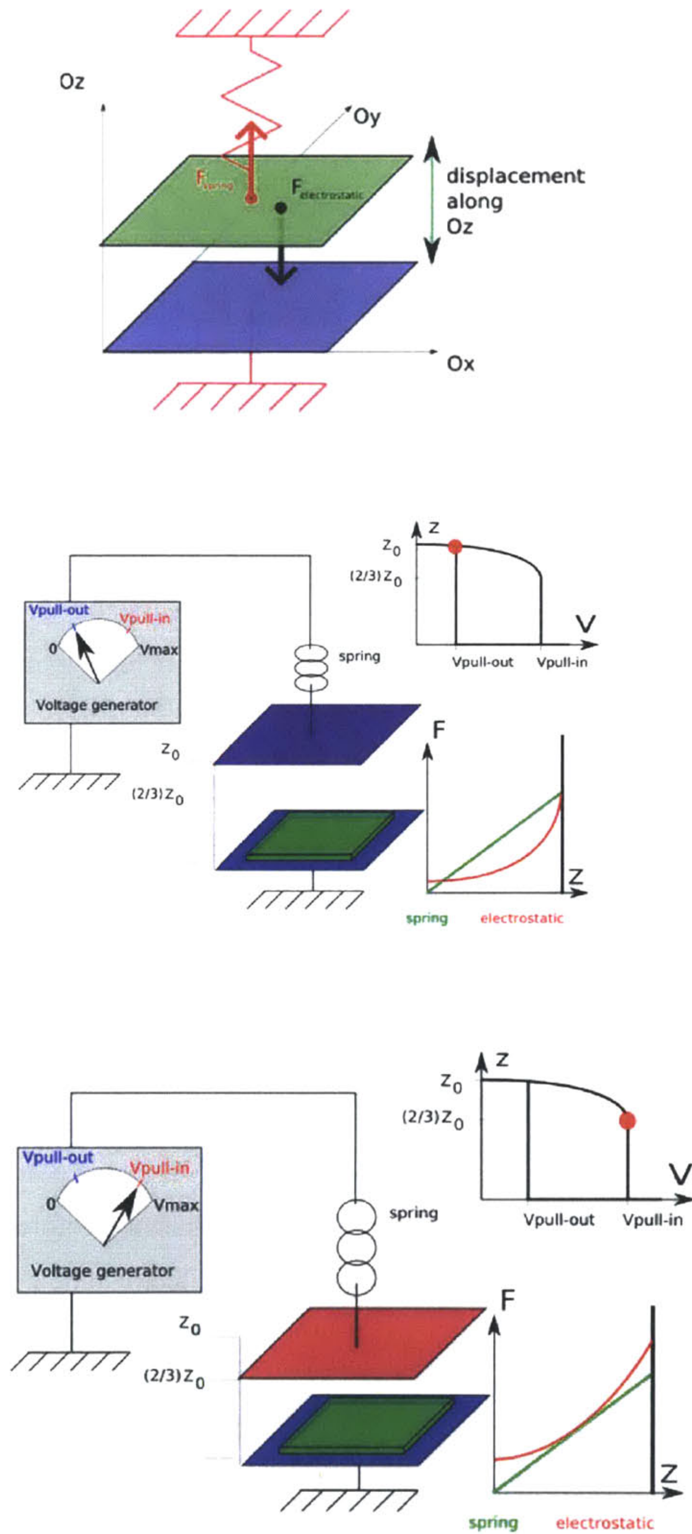


Figure E-1: Schematics and graphics showing the electrostatic actuation cycle with pull-in (from: http://matthieu.lagouge.free.fr/).

The energy calculation uses the principle that total energy of a system is a constant, so the energy accumulated by the capacitor (increasing with the plate moving to the fixed plate) is equal to the energy transferred to the spring.

Considering the position of the upper plate subjected to spring force in an upward direction and the electrostatic pull in the downward direction.

$$\delta F_{net} = \left(\frac{\varepsilon_0 A_A V^2}{(Z)^3} - k\right) \delta(Z) \tag{E-3}$$

δFnet should be negative ($k>\varepsilon_0 AV^2/z^3$) for stable equilibrium. Since equilibrium gap decreases with increasing voltage, there is a specific voltage at which stability of equilibrium is lost. The voltage is called pull-in voltage and denoted by *Vpull-in.* At pull-in, *Fnet* = 0.

$$V_{pull-in} = \sqrt{\frac{8}{27}\frac{E_S}{\varepsilon_0}\frac{A_S}{A_A}\frac{{D_A}^3}{D_S}} \tag{E-4}$$

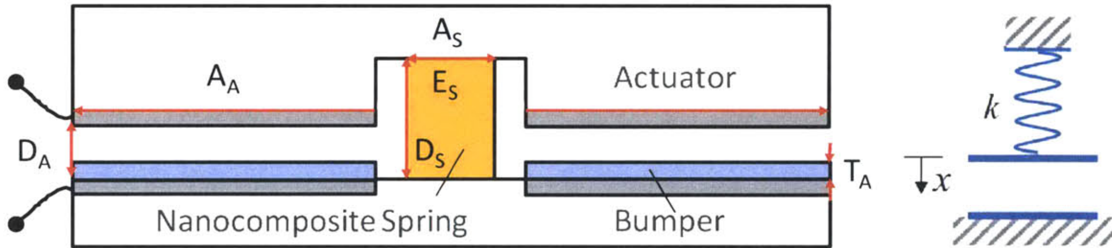


Figure E-2: Schematic cross section of the Squitch.

Switching energy can be approximated from:

$$CV^2 = \frac{8}{27} E_S A_S \frac{{D_A}^3}{D_S D_{min}} \tag{E-5}$$

Appendix F

Patents:

- "Electronically-Controlled Squishable-Composite Switch - "Squitch"", Vladimir Bulovic, Jeffrey Lang, Frank Yaul, Apoorva Murarka, Sarah Paydavosi, MIT Case No. 14594, 2010.
- "Methods for Forming Electrodes for Water Electrolysis and Other Electrochemical Techniques", U.S. Patent Application No.: 13/213,690
- "Contact-Transfer of Conductive Membranes on Silicon-Based Substrates", Vladimir Bulovic, Apoorva Murarka, Sarah Paydavosi; MIT Case No. 14993, 2011

Publications:

International Journal

1- **S. Paydavosi**, K. Aidala, P. Brown, G. J. Supran, V. Bulovic, " Direct Probing of Charge Storage on Tris(8-hydroxyquinoline) Aluminum Molecules by Kelvin Force Microscopy, a Potential Candidate For Molecular Flash Memory Devices," Nano Letters, 12, 1260-1264, 2011.

2- **S.Paydavosi**, Hassen Abdu, Geoffrey J. Supran,Vladimir Bulovic, "Molecular Floating Gate Memory," IEEE Trans. Nanotechnology, vol. 10, no. 3, May 2011.

3- Elizabeth R. Young, Ronny Costi, **Sarah Paydavosi**, Daniel G. Nocera and Vladimir Bulović, " Photo-Assisted Water Oxidation with Cobalt-Based Catalyst formed from Thin-film Cobalt Metal on Silicon Photoanodes ," Energy & Environmental Science , 4, 2058, 2011.

Publications (Refereed Conferences):

1- **S. Paydavosi**, K. Aidala, P. Brown, P. Hashemi, G. J. Supran, J. L. Hoyt, and V. Bulovic, "Molecular Flash memories," to be presented at ECS 2012, invited talk.

2- **S. Paydavosi**, K. Aidala, P. Brown, P. Hashemi, G. J. Supran, J. L. Hoyt, and V. Bulovic, "High-Density Charge Storage on Molecular Thin Films- Candidate Materials for High Storage Capacity Memory Cells," to be presented at the *IEEE International Electron Device Meeting (IEDM '11)*, Washington DC, USA, December 2011.

3- **S. Paydavosi**, F. M. Yaul, A. I. Wang, T. L. Andrew, V. Bulovic, J. H. Lang, "MEMS Switches Employing Active Metal-Polymer Nanocomposites," IEEE 25th International Conference on Micro Electro Mechanical Systems, 180-183, 2012.

4- Apoorva Murarka, **Sarah Paydavosi** and Vladimir Bulovic, "Printed MEMS Membranes on Silicon," IEEE 25th International Conference on Micro Electro Mechanical Systems, 309-312, 2012.

5- **Sarah Paydavosi**, Kathy Aidala, Patrick Brown and Vladimir Bulovic "Molecular Floating Gate Memories," *International Conference on Electroluminescence & Organic Optoelectronics* (ICEL), 2010 (oral presentation).

6- **Sarah Paydavosi,** Hassen Abdu, Vladimir Bulovic, "Organic Floating Gate Memory Devices," *MRS Conference,* spring 2009 (oral presentation).

7- **S. Paydavosi**, V. Bulovic, "A Performance Comparison of Different Molecular Organic Floating Gate Memories," to be presented at SRC TECHCON 2009, Austin, TX, USA, September 2009.

8- **Sarah Paydavosi,** Hassen Abdu, Vladimir Bulovic," Molecules as Segmented Storage Elements in Floating Gate Memories," to be presented at Organic Microelectronics & Optoelectronics Workshop V, San Francisco, July 2009.

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