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PwrSoC (integration of micro-magnetic inductors/transformers with active semiconductors) for more than Moore technologies*

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Abstract. This paper introduces the concept of power supply on chip (PwrSoC) which will enable the development of next-generation, functionally integrated, power management platforms with applications in dc-dc conversion, gate drives, isolated power transmission and ultimately, high granularity, on-chip, power management for mixed-signal, SOC chips. PwrSoC will integrate power passives with the power management IC, in a 3D stacked or monolithic form factor, thereby delivering the performance of a high-efficiency dc-dc converter within the footprint of a low-efficiency linear regulator. A central element of the PwrSoC concept is the fabrication of power micro-magnetics on silicon to deliver micro-inductors and micro-transformers. The paper details the magnetics on silicon process which combines thin film magnetic core technology with electroplated copper conductors. Measured data for micro-inductors show inductance operation up to 20 MHz, footprints down to 0.5 mm^2, efficiencies up to 93% and dc current carrying capability up to 600 mA. Measurements on micro-transformers show voltage gain of approximately – 1 dB at between 10 MHz and 30 MHz.

1 Introduction

The ongoing drive toward miniaturization of electronic products, with ever-increasing functionality and performance, from portable electronics to high-end computing, is placing significant challenges on switched-mode, power management platforms to deliver high-efficiency power at an increasing level of miniaturization and granularity. Semiconductor and microelectronics technologies have delivered significant progress through the functional integration of power switches with drivers and control electronics and through advanced system-in-package and chip scale packaging platforms. Currently, a major roadblock to further miniaturization and integration is the use of conventional, discrete magnetic and capacitor components for energy storage, filtering and isolation [1].

As a result, there is currently a very strong push in the power electronics industry to provide power supply in package (PwrSiP) platforms which address some of the above issues, with many companies having commercial offerings, mainly in the 1–5 watt dc-dc space, in the schematic form shown in Figure 1. The "holy grail" is the development of power supply on chip (PwrSoC) platform technology which functionally integrates the passives with the power management IC. Figure 2 presents a conceptual roadmap for the evolution to PwrSoC.

For a typical dc-dc buck converter, the required values of inductance and capacitance are inversely proportional to the operating frequency. Increasing the switching frequency of converters into the 10–100 MHz range offers the potential for the reduction of passive component values to the point where, with the right technology, their size becomes compatible with 3D stacking or monolithic integration with the power management IC without increasing the overall footprint significantly beyond that of the power management IC. PwrSiP offers a short- to medium-term solution with the discrete passives and the active die packaged side by side on a single substrate or lead frame. Typical examples of PwrSiP products are from Enpirion, Texas Instruments, Micrel, etc. [2,4,5]. PwrSoC traditionally would use low-profile integrated inductor on silicon with active die either monolithically built or 3-D stacked in a single chip scale package. The profile of the discrete chip inductor could still be a disadvantage for a PwrSiP solution. In contrast, the micro-inductor on silicon technology offers advantages of lower inductor profile and also a stacked or monolithic PwrSoC solution with minimum overall footprint.

As well as the above benefits of enhancing efficiency and reducing parasitic noise, the PwrSoC concept also offers the opportunity to enable semiconductor companies

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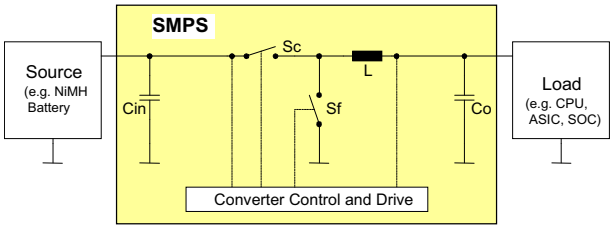

Fig. 1. Typical dc-dc switched mode power supply (buck converter).

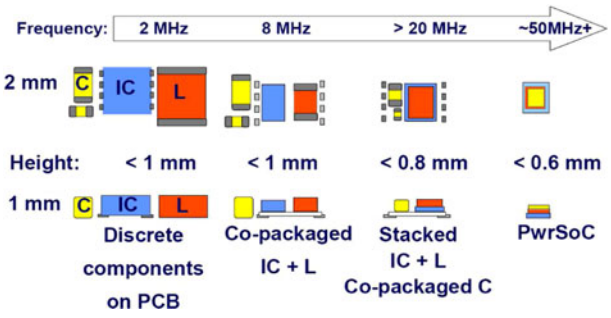

Fig. 2. Roadmap for evolution of power supply on chip technology.

to take full ownership of the power passives, thereby eliminating issues with external source of high-quality, low-cost bills of materials.

This paper presents an overview of work done by the authors, over the last 10 years, on the development of micro-magnetic power inductors and transformers on silicon to deliver the PwrSoC concept. This work is also complemented by ongoing work by a number of companies and institutes in the development of high density, trench capacitors on silicon.

2 Roadmap for dc-dc Power Converters

Increasingly, many companies, including Enpirion [2], Fuji [3], Micrel [4], National Semiconductor [5] and TI [6], have reported products using a PwrSiP platform, either with one or more passives integrated into the same package as the power management IC, in either a planar or stacked form-factor. In all the above cases, companies have developed products with enhanced integration using creative engineering solutions to deliver on the requirements of reduced footprint and reduced component count while maintaining overall height profile in the range of 1 mm.

In an attempt to understand the trends in this rapidly evolving area, this paper presents an overview of the progress of the performance of the typical dc-dc converter platforms outlined above. The accompanying figures provide plots of data for a range of dc-dc converter platforms ranging from commercial power modules [7–14] and PwrSiP products [2–6] to PwrSiP and PwrSoC research demonstrators which have been reported in the recent literature [15–31].

Figure 3 compares the power densities of the different power converters including power modules, power supply

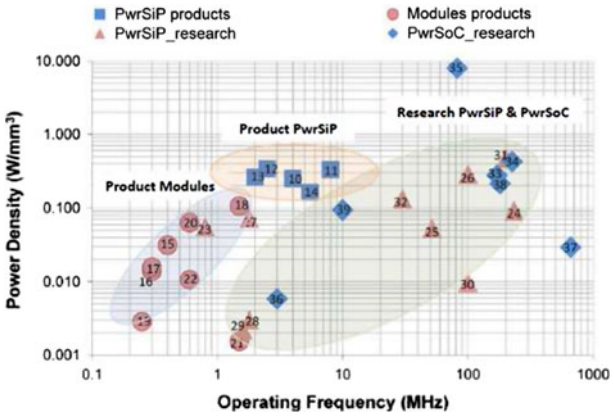

Fig. 3. Comparison of power densities of different power converters.

in package (PwrSiP) and power supply on chip (PwrSoC). The figure confirms that PwrSiP products have a higher power density than conventional power modules. This is mainly due to the higher operating frequency of PwrSiP products which allows the use of smaller value inductors, hence smaller size and lower profile. The PwrSoC converters reported in [20,21] show relatively lower power densities compared to the commercial PwrSiP products in the same range of operating frequency. This is mainly due to the fact that the commercial products use commercial ferrite chip inductors with significantly thicker magnetic material. However, as switching frequency increases, e.g., above 50 MHz, the required inductance becomes significantly less; the research demonstrators start to show comparable power density to commercial PwrSiP platforms. To date, all the inductors applied in these research demonstrators operating, at a frequency above 50 MHz, are air-core inductors, either discrete chip air-core inductors in [16,18] or on-chip, integrated, air-core inductors in [17,22,23,25,26,29–31]. In [22,23,25,26,29–31], an extra step was taken by integrating the capacitor on the same silicon as the on-chip, air-core inductor.

To complete the competitive landscape, commercial linear regulators and silicon-integrated, switched-capacitor research demonstrators of dc-dc converters have been added to Figure 4. Linear regulators are widely used as power converters due to their simplicity, low noise, good regulation and low cost [32–36]. Switched capacitor, dc-dc converters have been gaining considerable interest in recent years due to their higher efficiency compared to linear regulators but also because they don't need an output inductor, and therefore lend themselves to full integration on silicon using conventional technology, presenting a very attractive solution for PwrSoC [37–49].

As expected, Figure 4 shows that the efficiency of switched mode dc-dc products is significantly higher than those of linear regulator products and switched capacitor (SC) converters. The switched-capacitor regulators can give moderate efficiency of between 60% and 80% with high integration level, however, it has been reported that the solution still requires large silicon area even for 100 mA (i.e., 1 mm^2) [18]. So far, the demonstrated

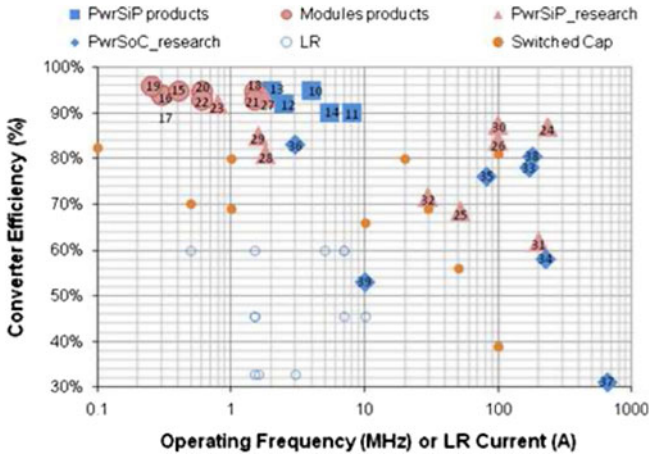

Fig. 4. Converter efficiency of POL products using commercial, packaged, on-chip inductors and switched capacitors.

current handling for SC is about 0.7 A/mm^2 [41]. Although, currently, there are no commercial SMPS products operating beyond 10 MHz, the research demonstrators have shown promising performance at very high operating frequencies, at 100 MHz or even higher. Converter efficiencies of up to 87% have been reported at operating frequencies between 100 and 233 MHz [16,18,22] using advanced CMOS processing technology. However, achieving a higher efficiency, similar to that of the majority of commercial products, operating at multi-MHz range (i.e., >93%), still remains a significant challenge.

PwrSoC is currently in research phase and is yet to demonstrate the efficiency and footprint targets required for commercial success. To realize the PwrSoC vision, the key challenges to be addressed are increased converter operating frequency, miniaturization and system integration of passive components, while maintaining efficiency. In the next section, we present the development of integrated magnetics technology at Tyndall National Institute for realizing an efficient PwrSoC solution.

3 Magnetics on silicon technology

The magnetics on silicon technology is based on a combination of electroplated, thin film, magnetic materials (NiFe permalloy core), used extensively in the magnetic disk head industry, with wafer-level, back-end-of-line (BEOL), electroplated copper conductors (windings) from the power semiconductor industry. Figures 5 and 6 show plan views and cross-sections of typical micro-inductor and micro-transformer devices based on a single-layer metal (SLM) and double-layer metal (DLM) process [50,51]. Figure 7 shows the process flows for both the SLM and DLM devices.

4 Device performance

Figures 8 and 9 present key performance data measured for micro-inductors [52,53]. Figure 8 shows that, using a NiFe core material, the micro-inductors operate at frequencies beyond 20 MHz. Figure 9 shows that the micro-inductors operate with a dc bias, with devices with a 2.5 mm^2 footprint supporting up to 600 mA. Figure 9 also shows a comparison of a micro-inductor with a commercial chip inductor operating in an 8 MHz dc-dc converter circuit. In this plot, the efficiency of the micro-inductor, which has been extracted from the overall efficiency of the converter, is shown to be only 4–6% lower than that for the commercial ceramic chip inductor [54]. The reduced efficiency can be accounted for in the resistance of the plated copper windings and the eddy current losses in the magnetic core due to its very low resistivity when compared with ferrite materials.

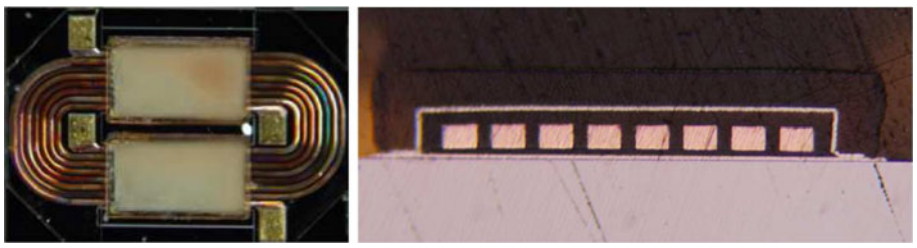

Fig. 5. Plan view and cross-section of single-layer metal (SML) micro-magnetic process – overall device footprint 3 × 2 mm.

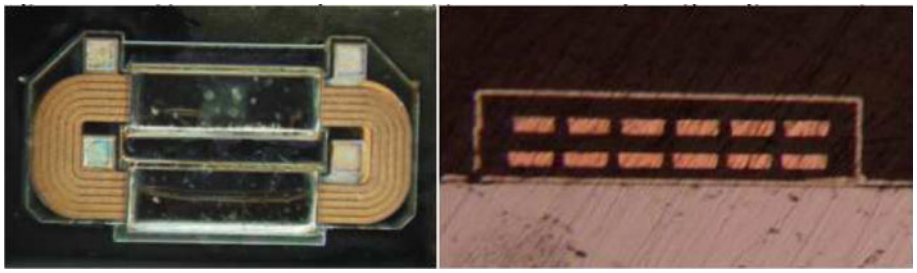

Fig. 6. Plan view and cross-section of double-layer metal (DML) micro-magnetic process – overall device footprint – 3 × 2 mm.

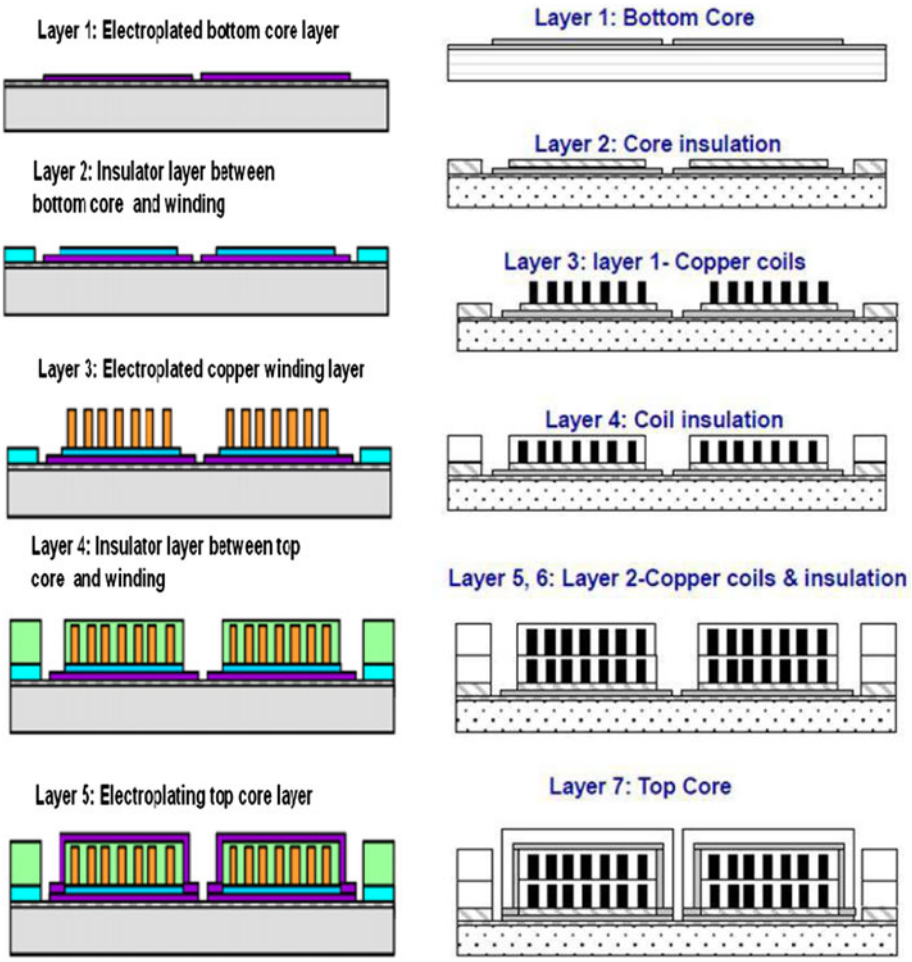

Fig. 7. Fabrication process flow for SLM and DLM micro-inductors.

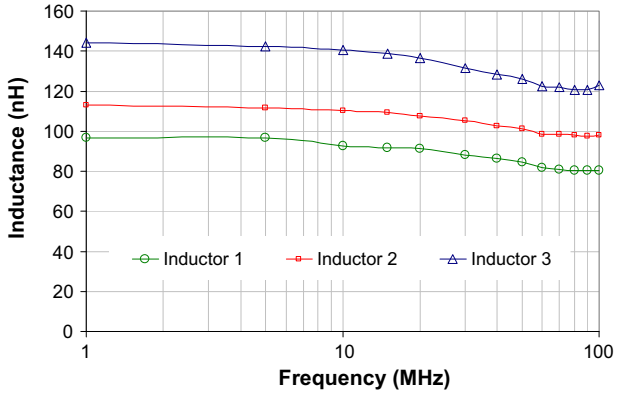

Fig. 8. Micro-inductors – measured inductance versus frequency.

Figures 10–12 plot measured and modeled data for SLM and DLM micro-transformers [55]. A plot of the measured open circuit inductance, Loc, and open circuit resistance, Roc, for both SLM and DLM micro-transformers is shown in Figure 10. The Loc values are approximately 85 nH and 210 nH at 20 MHz, for SLM and DLM, respectively. For both cases, the inductance holds up to at least 20 MHz with less than 15% drop of inductance, although inductance drop is larger than expected. The DC resistance was tested using Kelvin 4-probe method. The measured primary and secondary DC resistances for SLM device are both 0.367 Ω. Similarly, the primary and secondary DC resistances for DLM device are 1.096 Ω and 0.962 Ω, respectively. The measured resistances match well with the design values.

The measured voltage gain of the devices under a 50 Ω resistive load condition is plotted in Figure 11. Both the SLM and DLM micro-transformers exhibit the highest reported voltage gain for micro-transformers of approximately –1 dB at between 10 MHz and 30 MHz. The low voltage gain at low frequencies is due to the low magnetizing inductance. The voltage gain starts to fall off at high frequencies because the eddy current loss increases significantly. Based on validated model data, Figure 12 compares the efficiencies of different SLM and DLM micro-transformer designs with various footprint areas. DLM devices achieve higher efficiencies than SLM devices for the same footprint with DLM devices estimated for achieving efficiencies greater than 70% for a footprint of 2 mm^2.

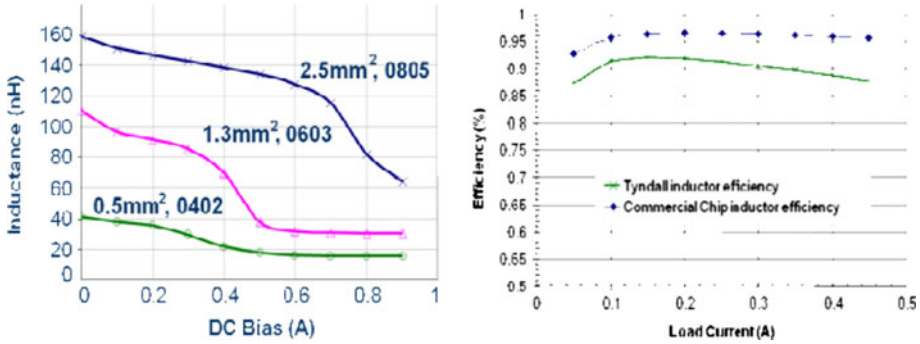

Fig. 9. Micro-inductors – measured inductance versus bias current and extracted inductor efficiency for 8 MHz buck converter circuit. Comparison with commercial wire-wound chip inductor.

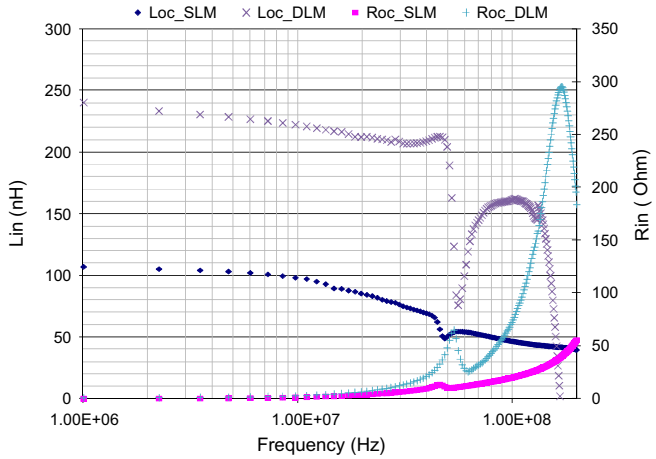

Fig. 10. Measured open circuit inductance and resistance.

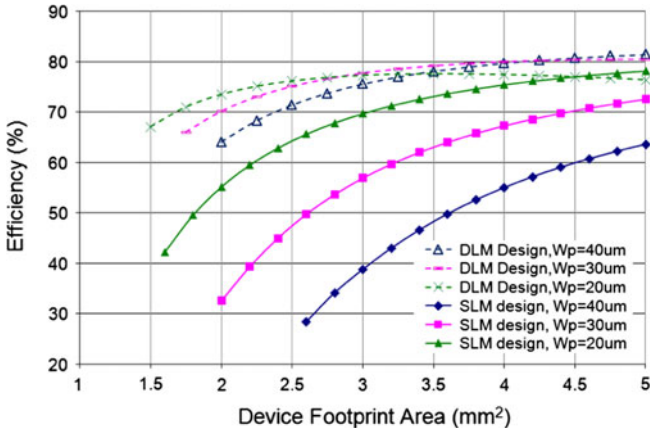

Fig. 12. Modeled efficiency of transformers using single and double layers of Cu windings.

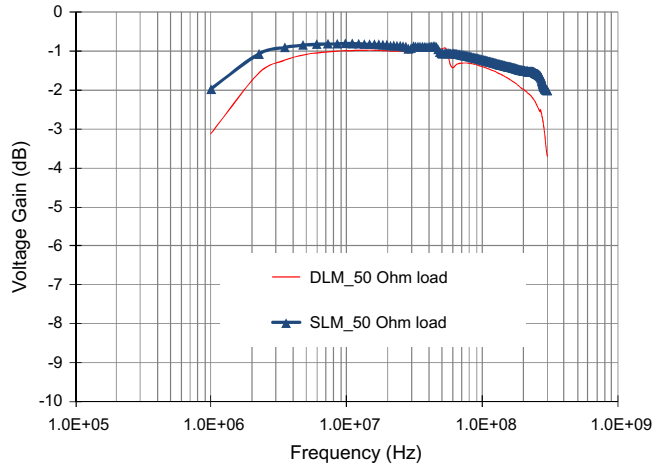

Fig. 11. Micro-transformer – measured voltage gain for SLM and DLM structures.

5 Applications

There are a very broad range of applications which can be targeted with technology. These include:

– Micro-inductors in non-isolated dc-dc converters and in gate drives. This also includes multiconverter power management ICs (PMICs) as are used extensively in smart phones, but currently relying on many discrete passives. The technology also presents an opportunity to develop a high-efficiency dc-dc converter with the footprint of low-efficiency, linear regulators.
– Micro-transformers for use in isolated converters and in isolated gate drives. This would also include instrumentation applications requiring energy transfer across an isolation barrier, currently being served by low-efficiency, integrated air-core micro-transformers [56].
– As the technology is suited to operating above 20 MHz, it may be particularly suited to operating with GaN semiconductors.
– In the case of complex SoC platforms, such as embedded microcontrollers and multicore processors, magnetics on silicon can facilitate the delivery of high granularity power management embedded on the SOC platform [27].

6 Conclusions

The paper has described a microsystems technology which combines the electroplating of thin film magnetic cores with electroplated copper conductors to fabricate micro-magnetic power inductors and transformers on silicon.

This technology platform will enable the development of next generation, functionally integrated, power management platforms with applications in dc-dc conversion, gate drives, isolated power transmission and ultimately, high granularity, on-chip, power management for mixed-signal SOC chips. While miniaturization is a key driver, other important benefits of the technology include:

- Increased efficiency and reduced noise due to minimization/elimination of interconnect parasitics.
- Reduce EMI issues due to short current loops, and system co-design optimization.
- Reduced cost through reduced BOM, PCB area and application assembly costs.

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