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Capacitance-Voltage (C-V) characterization and hard x-ray photoelectron spectroscopy (HAXPES) measurements have been used to study metal/Al_2O_3/$In_{0.53}Ga_{0.47}As$ capacitor structures with high (Ni) and low (Al) work function metals. The HAXPES measurements observe a band bending occurring prior to metal deposition, which is attributed to a combination of fixed oxide charges and interface states of donor-type. Following metal deposition, the Fermi level positions at the Al_2O_3/$In_{0.53}Ga_{0.47}As$ interface move towards the expected direction as observed from HAXPES measurements. The $In_{0.53}Ga_{0.47}As$ surface Fermi level positions determined from both the C-V analysis at zero gate bias and HAXPES measurements are in reasonable agreement. The results are consistent with the presence of electrically active interface states at the Al_2O_3/$In_{0.53}Ga_{0.47}As$ interface and suggest an interface state density increasing towards the $In_{0.53}Ga_{0.47}As$ valence band edge. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4887517]

I. INTRODUCTION

The innovation and scaling of complementary metal oxide semiconductor field effect transistors (CMOS) at the heart of integrated circuits has been on-going for the last four decades. The semiconductor and dielectric materials, which constitute the MOS transistors, are now becoming the limit to the further reduction of device dimensions required by future scaling. For instance, the scaling of the conventional Si/SiO_2 metal oxide semiconductor field effect transistor (MOSFET) has effectively come to its limit as any further reductions in the ultra thin SiO_2 layers will result in unacceptably large leakage currents via direct electron tunnelling. High mobility materials (e.g., Ge and III–V compound semiconductors) and high dielectric constant (high-*k*) gate materials (e.g., HfO_2, Al_2O_3, and ZrO_2) are being intensively investigated as alternative semiconductor channel materials and insulators for future devices with minimum dimensions below 22 nm. The high-*k* gate materials increase the physical thickness of the oxide while maintaining or increasing the oxide capacitance, thus effectively reducing the leakage current. Meanwhile the use of the high mobility channel materials has the added benefit of a high speed of switching of the MOSFET and reducing the supply voltage while maintaining the same drive current. Therefore, such high-*k*/high-mobility based MOSFETs are expected to have improved performance/power consumption ratio. To realise this potential for an improved performance/power consumption ratio it is necessary to study the high-*k*/III–V gate stack from the perspective of electrically active defect states, which include interface states, fixed charges within the high-*k* oxide and border traps near/at the high-*k*/III–V interface transition layer.[1–3] These defects affect MOSFET performance in a range of detrimental ways,[4,5] and possible methods to remove these defects from high-*k*/III–V MOS system have been extensively studied.[6–9]

Interface properties are of particular interest due to the relatively high density of electrically active interface defects present at this interface, which restricts efficient III–V surface Fermi level movement. One of the main issues associated with the accurate extraction of interface state concentrations (interface state density distribution as a function of energy in the III–V bandgap, i.e., $D_{it}(E)$) for the high-*k*/III–V MOS system is the question of how each gate voltage (V_g) is related to the corresponding surface Fermi level position (E_f) relative to the valence band edge (E_v). For a $D_{it}(E)$, which changes density exponentially with E_f-E_v, this is clearly a potential source of error and variation between research groups. Moreover, the relationship of E_f-E_v to V_g is further complicated in the case of high D_{it} and for MOS systems where the semiconductor has a low conduction band density of states, such as $In_{0.53}Ga_{0.47}As$. This combined effect results in difficulty with the accurate extraction of the oxide capacitance, which is required when relating V_g to a corresponding E_f-E_v.

As a traditional method, C-V analysis is widely used to investigate the high-*k*/III–V electrically active defects.[3,10] In this study, $In_xGa_{1-x}As$ with a 53% indium concentration, i.e., $In_{0.53}Ga_{0.47}As$, (the term "InGaAs" is used to represent $In_{0.53}Ga_{0.47}As$ in the following discussion) was chosen as the channel material due to the fact that it has a high electron mobility (14 000 cm^2/Vs at low doping levels), a suitable bandgap (~0.75 eV) for low voltage applications and the fact that it can be grown lattice matched on InP. The high-*k*/InGaAs MOS system is known to have a relatively high interface state density (D_{it}); however, the InGaAs surface Fermi level is generally not fully pinned as compared to the

high-*k*/GaAs MOS system, where the movement of GaAs surface Fermi level is strongly restricted.[11,12]

In this paper, C-V analysis was performed on MOS capacitors fabricated using both high (Ni 5.01 eV) and low (Al 4.08 eV) work function metal gates on atomic layer deposition (ALD) Al_2O_3 on InGaAs.[13] On the premise that a true high frequency C-V can be obtained, the surface potential is determined and so is the Fermi level position at the Al_2O_3/InGaAs interface. Hard x-ray photoelectron spectroscopy (HAXPES) measurements on the same MOS structures with a much thinner metal gate have also been performed. HAXPES is emerging as a technique that has the capability of providing chemical and electronic information on much larger depth scales than conventional x-ray photoelectron spectroscopy.[12,14–16] The main objective of this study is to compare the surface Fermi level positions (at room temperature) analysed by C-V characteristics at zero gate bias ($V_g = 0$ V) and HAXPES measurements without applying a gate bias, and furthermore, to investigate the Fermi level movement at the Al_2O_3/InGaAs interface and the change in potential drop across the dielectric layer, resulting from the deposition of metals with different work functions. It has recently been shown that good agreement can be obtained for E_f-E_v at $V_g = 0$ V in the SiO_2/Si MOS system[16] and strongly pinned case of the Al_2O_3/GaAs[12] MOS using a similar C-V and HAXPES comparative study. The aim of this work is to extend on the studies reported in Refs. 12 and 16 to the case of the Al_2O_3/InGaAs MOS system. These studies provide more certainty on $D_{it}(E)$ extractions and also bridge the gap between interface chemistry and electrical properties at a buried interface.

II. EXPERIMENTAL DETAILS

The samples studied in this work were heavily *n*-doped (S at $\sim 2 \times 10^{18}$ cm^{-3}) and heavily *p*-doped (Zn at $\sim 2 \times 10^{18}$ cm^{-3}) InP(100) substrates with 2 μm *n*-type (S at $\sim 4 \times 10^{17}$ cm^{-3}) and *p*-type (Zn at $\sim 4 \times 10^{17}$ cm^{-3}) InGaAs epitaxial layers, respectively, grown by metal organic vapour phase epitaxy (MOVPE). The InGaAs surfaces were initially degreased by sequentially rinsing for 1 min each in acetone, methanol, and isopropanol. Prior to the ALD of high-*k* oxide, the samples were immersed in a $(NH_4)_2S$ solution (10% in deionized H_2O) for 20 min at room temperature (~295 K), which was found to be the optimum approach to suppress the formation of InGaAs native oxides and to reduce the high-*k*/InGaAs interface state density as reported previously.[9] Samples were then introduced to the ALD chamber load lock after the removal from the 10% $(NH_4)_2S$ surface passivation solution. The transfer time from the aqueous $(NH_4)_2S$ solution to the ALD chamber was kept to a minimum (~3 min) in order to minimise the formation of InGaAs native oxides resulting from air exposure. The Al_2O_3 dielectric layer, which had a nominal thickness of 8 nm, was deposited by ALD at 300 °C using trimethylaluminum (TMA) $Al(CH_3)_3$ and H_2O as precursors.

For C-V analysis, either Al (160 nm) or Ni (70 nm)/Au (90 nm) were used as the metal gate electrodes, which were formed by electron beam evaporation and a lift-off process. The C-V measurements were recorded using a semiconductor device analyser following an open correction and performed in a probe station in a dry air, dark environment. Multi-frequency (1 kHz–1 MHz) and 1 MHz C-V measurements were carried out at both room temperature and −50 °C. The C-V characteristics measured at both temperatures at 1 MHz were compared in order to rule out the possible contribution of an interface state capacitance to the overall measured capacitance of the MOS capacitors at room temperature. The oxide capacitance and flatband capacitance used for C-V analysis are calculated using a dielectric constant value of 8.6 for Al_2O_3[17] and accurate oxide thicknesses were obtained from high-resolution cross-sectional transmission electron microscopy (HR-TEM).

For HAXPES analysis, one *n*-type and one *p*-type Al_2O_3/InGaAs sample were left without a metal gate. The other HAXPES samples were capped with either Al (5 nm) or Ni (5 nm) blanket films formed by electron beam evaporation. HAXPES measurements were carried out on the X24A beamline at the National Synchrotron Light Source (NSLS) at Brookhaven National laboratory (BNL). A double Si (111) crystal monochromator allowed for photon energy selection in the range of 2.1–5.0 keV. An electron energy analyser was operated at a pass energy of 200 eV giving an overall instrumental energy resolution of ~0.52 eV at the photon energy of 4150 eV. Samples were fixed on a grounded Al sample holder with stainless steel clips, which connected the front of the samples to the sample holder. In order to ensure correct energy calibration throughout the experiment, metallic Ni Fermi edge reference spectra were acquired immediately before and after the acquisition of the Al_2O_3 and InGaAs substrate core level peaks. The resultant error associated with this photon energy correction procedure is estimated to be no more than ±50 meV. The calculated depletion region width for the 4×10^{17} cm^{-3} doped InGaAs substrate is 51 nm and the total sampling depth of the HAXPES measurements for the metal capped samples is estimated to be ~23 nm at 4150 eV (Ref. 18) for the substrate Ga 2p and As 2p which have kinetic energies of 3033 eV and 2827 eV, respectively.[19] This means that for a 5 nm thick metal capping layer and an 8 nm Al_2O_3 layer, the sampling depth into the InGaAs is ~10 nm. Therefore, the acquired peaks directly reflect the binding energy (BE) of the core levels with respect to the Fermi level near the top of the depletion region adjacent to the dielectric interface. All core level peaks were curve fitted in order to increase the accuracy of locating the peak centre positions.

III. RESULTS AND DISCUSSION

The C-V characteristics at 1 MHz and 295 K for Al (160 nm) or Au (90 nm)/Ni (70 nm) metal gate MOS capacitors are shown in Figures 1(a) and 1(b) for Al_2O_3/*n*-InGaAs and Al_2O_3/*p*-InGaAs, respectively. If interface states can respond at these measurement conditions, the measured capacitance (C_m) will have a contribution from interface states (C_{it}), which is frequency and temperature dependent, and can be suppressed at a higher frequency and/or lower temperature.[4,5,11] This will especially affect the C-V responses

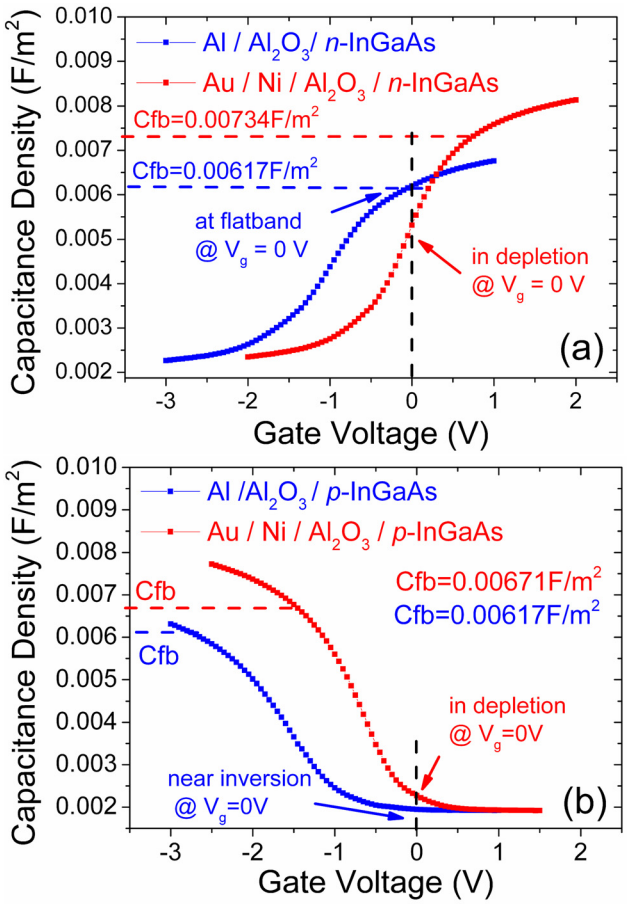

FIG. 1. C-V responses at 1 MHz and 295 K for Al gate and Au/Ni gate over (a) Al_2O_3/*n*-InGaAs and (b) Al_2O_3/*p*-InGaAs MOS capacitors.

in terms of frequency dispersion in the accumulation region at different temperatures. Therefore, a significantly lower level of accumulation frequency dispersion and a decrease in the 1 MHz C_m are expected at a lower temperature when compared to the measurements at room temperature. It is believed that a true high frequency C-V is achieved at 1 MHz and room temperature as the multi-frequency (1 kHz to 1 MHz) and 1 MHz C-V measured at room temperature have very similar characteristics when compared to the C-V measured at −50 °C (not shown) for the Al_2O_3/InGaAs MOS capacitors under investigation. Based on this observation we take the 1 MHz room temperature response to be an accurate representation of a high frequency C-V for the InGaAs structures examined in this study.

As observed in the TEM images in Figure 2, a thicker Al_2O_3 film is formed under the Al gate due to a more reactive Al/Al_2O_3 interface compared to a non-reactive Ni/Al_2O_3 interface. This is consistent with the lower oxide capacitance and thus the lower measured capacitance in accumulation for the Al gate samples as observed in Figures 1(a) and 1(b). Using the oxide thickness measured by HR-TEM in Figure 2, the oxide capacitance (C_{ox}) is calculated and used to determine the flatband capacitance (C_{fb}). Furthermore, the calculated C_{fb} can be used to determine the region of operation of the MOS capacitor, and to establish if at $V_g = 0$ V, the surface Fermi level position can be determined using the depletion capacitance. From the C-V for *n*-InGaAs in Figure 1(a), the measured capacitance for the Ni gate sample is below the calculated C_{fb} (~0.00734 F/m^2) and is thus operating in depletion at $V_g = 0$ V. The corresponding InGaAs depletion capacitance (C_s) can be calculated using the measured capacitance C_m ($C_{it} = 0$) and an oxide capacitance value of 1.27×10^{-6} F/cm^2. The C_s value can be used to calculate the surface Fermi level position with respect to valence band maximum (VBM) energy level and for Ni gate *n*-InGaAs yielding a value of ~0.71 eV above VBM. For the Al gate *n*-InGaAs sample shown in Figure 1(a), the C_m at $V_g = 0$ V approximately equals the C_{fb} value (~0.00617 F/m^2), which indicates that the sample is near the flatband condition and its surface potential is approximately

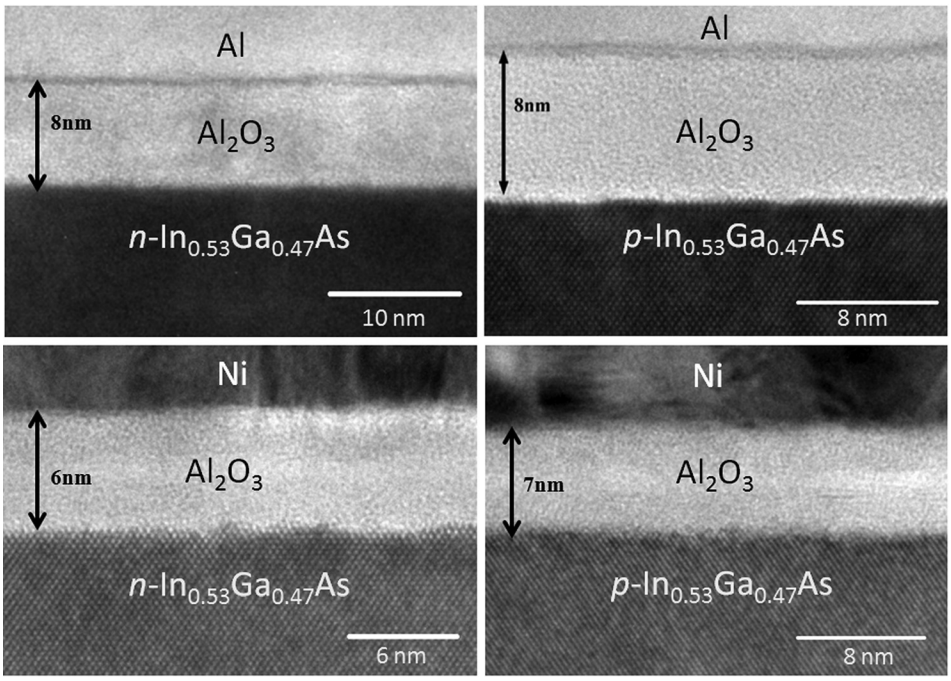

FIG. 2. Transmission electron microscopy images of the MOS capacitors under investigation. Note that there is no clear evidence of InGaAs native oxides at the Al_2O_3/InGaAs interface, which is consistent with the $(NH_4)_2S$ treatment prior to the ALD process[9] and the reported "self-cleaning" process of ALD of Al_2O_3.[29,30]

zero at $V_g = 0$ V. Thus the Fermi level position for this sample is ~0.76 eV above the VBM at the flatband condition for Al gate *n*-type InGaAs. From the C-V for Ni gate and Al gate over *p*-InGaAs shown in Figure 1(b), both samples are operating in depletion region at $V_g = 0$ V. Using the same method of surface Fermi level calculation for Ni gate over *n*-InGaAs (Figure 1(a)), the Fermi level is determined to be ~0.55 eV and ~0.73 eV above VBM with Ni and Al gates, respectively.

Figure 3 shows the HAXPES As 2p core levels acquired at 4150 eV photon energy for both *n*- and *p*-InGaAs with an Al_2O_3 dielectric layer with and without the presence of the metal gate. For the unmetallised samples, the binding energy position for the *p*-InGaAs peaks was found to be ~0.28 eV lower than the *n*-InGaAs substrate consistent with the *p*-type sample Fermi level residing closer to the VBM. The difference is however less than the expected difference of 0.68 eV, which is calculated from the difference in Fermi level position for *n*- and *p*-InGaAs for a doping level of 4×10^{17} cm^{-3},[4,5] indicating that there is band bending present at the Al_2O_3/InGaAs interface prior to metal contact.

In order to establish the absolute position of the Fermi level in the band gap with respect to the valence band edge, valence band spectra were acquired at the same photon energy for the unmetallised Al_2O_3/*n*-InGaAs sample. An extrapolation of the InGaAs valence band to a zero signal intensity yields the approximate position of the valence band edge.[20] Although more accurate methods have been recently employed,[12,21] this method is sufficient to provide an accuracy of approximately 0.1 eV in these studies. Reference spectra of the nickel metallic edge were subsequently acquired in order to establish the Fermi level position. The value of E_f-E_v is thus determined for the Al_2O_3/*n*-InGaAs sample with no metal gate. On the same sample, the As 2p spectra are recorded. These measurements provide the necessary reference for all the other samples to allow the value of E_f-E_v to be evaluated. The energy separation between the core level and the InGaAs valence band maxima is a constant; therefore, any changes in the As 2p spectra in Figure 3 are a consequence of changes in E_f-E_v. From the valence band spectra of the uncapped Al_2O_3/*n*-InGaAs sample (not shown), the Fermi level is 0.67 eV above the VBM and the equivalent measurement for the *p*-type Fermi level position is 0.39 eV above the VBM. Therefore, the Fermi level is ~0.09 eV below flatband position for *n*-InGaAs and is ~0.31 eV above flatband position (i.e., near mid-gap) for the *p*-InGaAs, indicating that the *n*-InGaAs surface is slightly depleted and the *p*-InGaAs surface is strongly depleted. Figures 4(a) and 4(b) schematically illustrates the band bending occurring for the unmetallised samples and the respective Fermi level positions (E_f) determined by HAXPES. The depletion of both the *n*- and *p*-type surface cannot be explained by one net oxide charge type. Therefore, the band bending occurring at the InGaAs surface in the absence of metal gates is attributed to a combination of fixed charge in the Al_2O_3 layer and the interface states with energy levels within the InGaAs bandgap, which deplete both the *n*-type and *p*-type surface. Based on the work by Long *et al.*[8] the fixed oxide charge in ALD deposited Al_2O_3 is comprised of negative interface fixed charge that exists near the Al_2O_3/InGaAs interface and positive fixed charge distributed through the bulk of Al_2O_3. For a relatively thin oxide of 8 nm, the net fixed oxide charge (Q_f) could be negative as discussed in Ref. 8. In addition, Refs. 8, 22, and 23 have reported the evidence that the net interface states type for Al_2O_3 on InGaAs is donor type (+/0). If this is the case, for an *n*-type sample at flatband where the E_f is close to conduction band edge and the interface state energy levels in the bandgap are occupied, the interface defects (Q_{it}) are neutral. The combination of negatively charged Q_f and neutral Q_{it} is a negative charge, which slightly depletes the *n*-type surface as shown in Figure 4(a). For a *p*-type sample at flatband where E_f is close to valence band edge, the donor-type interface defects have a net associated positive charge as their energy levels in the bandgap are empty. The positively charged interface states plus the negatively charged Q_f can result in the depletion of *p*-type surface as shown in Figure 4(b). Confirming the sign of Q_f and Q_{it} requires an Al_2O_3 thickness series as described in Ref. 8, which is beyond the scope of this work.

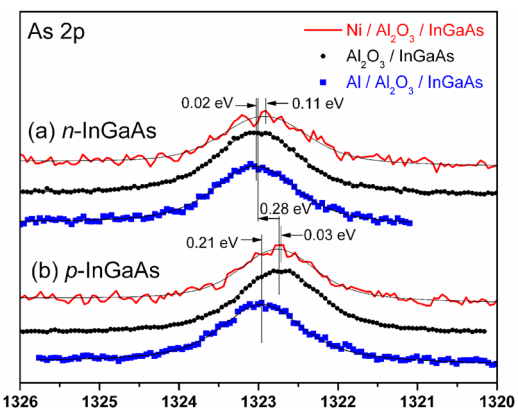

FIG. 3. Normalised and fitted As 2p core level spectra acquired at a photon energy of 4150 eV for the uncapped Al_2O_3/InGaAs (black), Ni (5 nm) capped (red), and Al (5 nm) capped Al_2O_3/InGaAs (blue) samples, showing the shifts in the core level BE after metal for (a) *n*-, and (b) *p*-InGaAs substrates. The energy separation between the *n*- and *p*-InGaAs without metal gates is 0.28 eV. The biggest BE shift occurs in the *p*-InGaAs sample with an Al gate. This is consistent with lower D_{it} distribution in the upper bandgap which allows for a more efficient Fermi level movement.

In order to determine whether the band bending displayed at the interface reflects Fermi level pinning, both high (Ni) and low (Al) work function metals of 5 nm in thickness were deposited on the dielectric. By ensuring electrical contact between the metal overlayer and the InGaAs substrate, Fermi level equalisation across the MOS structure resulting from the differences in work functions occurs. If the Fermi level at the Al_2O_3/InGaAs interface is free to move, it would be expected to align with the metal Fermi level, resulting in an increase in BE with the low work function Al contact and a reduction in BE with the high work function Ni contact for both the *n*- and *p*-InGaAs. HAXPES measurements in Figure 3 show that, for the *p*-InGaAs sample, the core level peaks shifts by 0.21 eV, and for the *n*-InGaAs sample, the peaks shifts by 0.02 eV, both to higher BE, following the deposition of Al contact. Following the deposition of Ni contact, the peak positions shift 0.11 eV for *n*-InGaAs and

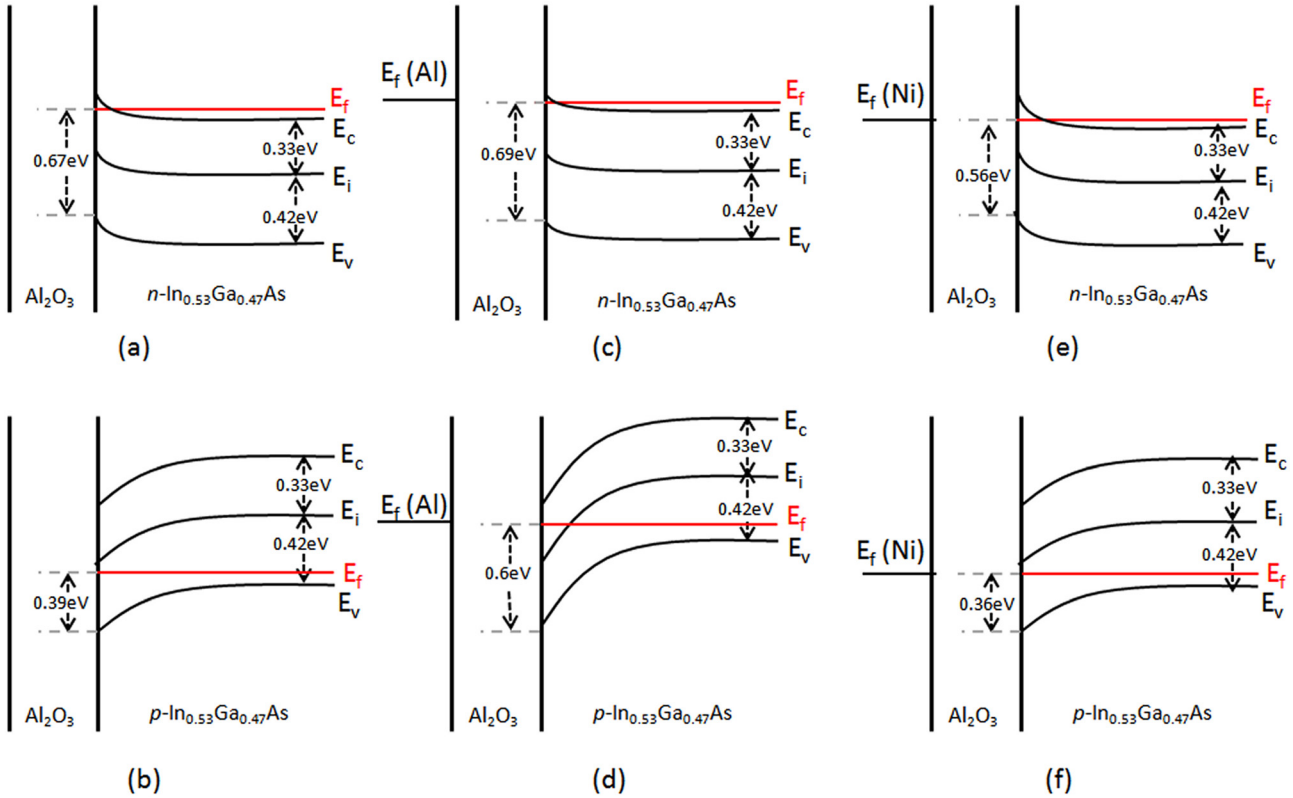

FIG. 4. Band diagrams of (a) unmetallised Al_2O_3/*n*-InGaAs, (b) unmetallised Al_2O_3/*p*-InGaAs, (c) Al_2O_3/*n*-InGaAs following Al deposition, (d) Al_2O_3/*p*-InGaAs following Al deposition, (e) Al_2O_3/*n*-InGaAs following Ni deposition, and (f) Al_2O_3/*p*-InGaAs following Ni deposition MOS capacitors. The band bending occurring in the absence of a metal contact shown in (a) and (b) is due to a combined effect of fixed oxide charges and interface states. E_f represents the Fermi level position, E_c represents the conduction band edge, E_v represents the valance band edge and E_i represents the InGaAs midgap energy level. The surface E_f-E_v values shown in this figure are determined from HAXPES.

0.03 eV for *p*-InGaAs to lower BE. It should be noted that the small shifts of 0.02 eV and 0.03 eV, measured for the Al on *n*-InGaAs and Ni on *p*-InGaAs respectively, are within the experimental error (±50 meV) of this technique; therefore, these shifts are negligible. The directions of all the BE shifts observed in the HAXPES spectra are consistent with the differences in the Fermi level positions for the InGaAs substrates and metals. The changes in InGaAs surface Fermi level when the metal contacts are present can be visualized using the schematic band diagrams and the Fermi levels presented in Figures 4(c)–4(f).

The corresponding Fermi level positions in the InGaAs bandgap following either Al or Ni deposition are calculated from the HAXPES to be 0.69 eV above VBM for the Al gate, and 0.56 eV above VBM for Ni gate, over *n*-InGaAs. Both of these Fermi level positions are in agreement with the C-V measurements at $V_g = 0$ V shown in Figure 1(a) where the sample is in the near flatband condition for the Al gate and in depletion for the Ni gate. For the HAXPES *p*-InGaAs samples, the Fermi levels are determined to be 0.6 eV above VBM with the Al gate and 0.36 eV above VBM with the Ni gate, which are consistent with the C-V measurements at $V_g = 0$ V in Figure 1(b) where both the samples are in depletion with the Al gate sample being more depleted (near inversion) than the Ni gate sample.

In the HAXPES measurements, any large degree of band bending at the Al_2O_3/InGaAs interface may lead to an error in the surface Fermi level measurement, as HAXPES has a sampling depth into the substrate of ~10 nm so the Fermi level is being measured up to 10 nm below its surface position. In order to assess the magnitude of this error in determining the Fermi level position from the HAXPES measurement, a simulation of the band bending for 4×10^{17} cm^{-3} doped *p*-InGaAs resulting from a 0.31 eV surface potential was performed by numerically solving Poisson's equation. The resulting band bending diagram (not shown) indicates that for a sampling depth into the InGaAs substrate of ~10 nm, the error in determining the VBM position is a maximum of 0.1 eV. However, due to the exponential fall off in the weighting of the photoemitted electron contribution with depth, the actual error will be less than this value. This error can thus be taken into account when comparing the results of the approximate Fermi level position of each sample in the InGaAs bandgap.

A comparison between the Fermi level positions at the Al_2O_3/InGaAs interface derived from C-V analysis at $V_g = 0$ V and the HAXPES measurements shown in Table I displays a reasonable agreement is achieved between the two techniques. The difference between the Fermi level position of Al and Ni obtained from C-V analysis are also consistent with that determined by HAXPES measurements. The difference between the C-V and HAXPES values for E_f-E_v are in the range of 0.1–0.2 eV. This is comparable to the results obtained in the case of the GaAs/Al_2O_3 MOS system,[12] but in the case of the InGaAs, this error represents a larger percentage of the energy gap.

TABLE I. Surface Fermi level positions obtained from C-V analysis at $V_g = 0$ V and HAXPES measurements for uncapped, Al gate and Ni gate Al_2O_3/InGaAs samples.

Sample	E_f–E_v (uncapped)	E_f–E_v (Al gate)	E_f–E_v (Ni gate)	ΔE_f (Al-Ni shift)
n-type (C-V)	N/a	0.76 eV	0.71 eV	0.05 eV
n-type (HAXPES)	0.57 → 0.67 eV	0.59 → 0.69 eV	0.46 → 0.56 eV	0.03 → 0.23 eV
p-type (C-V)	N/a	0.73 eV	0.55 eV	0.18 eV
p-type (HAXPES)	0.39 → 0.49 eV	0.6 → 0.7 eV	0.36 → 0.46 eV	0.14 → 0.34 eV

Further insight into the Al_2O_3/InGaAs interface properties can be obtained from the HAXPES measurements in relation to the extent of the Fermi level movements at InGaAs surface when a metal layer is deposited. Following the deposition of the Al gate, the surface Fermi level position of *n*-InGaAs moves towards the conduction band edge. For the *p*-InGaAs following Al deposition, the Fermi level moves towards conduction band edge residing slightly below the conduction band minimum. These experimental observations confirm the ability of the Fermi level in the InGaAs bandgap to move towards the conduction band edge attempting to align with the Al Fermi level (see Figure 4). The fact that the surface Fermi level does not move significantly into the low density of states InGaAs conduction band is also consistent with the reported high interface state density located within the InGaAs conduction band where the Fermi level can be strongly pinned at energies above E_c.[3,24,25] When the Ni gate is in contact, the InGaAs Fermi level movement is more restricted. The inability to move the *n*-InGaAs Fermi level to the lower bandgap and the slight Fermi level movement of only 0.03 eV towards VBM for the *p*-InGaAs suggest a peak D_{it} distribution where the density increases in the lower half of the bandgap, consistent with previous publications.[26–28]

Fermi level alignment between the metal and the InGaAs is achieved by not only the movement of InGaAs Fermi level but also a change in the potential drop across the oxide layer. The change in the oxide potential following metal deposition will result in a binding energy shift of the associated Al 1s dielectric core levels, and the total potential drop across the oxide will result in an energy broadening of the peak.[12,14,16] Note that the shift resulting from Fermi level movement in the bulk InGaAs is also present in the oxide core level, so any shift in the oxide peaks is a combination of the InGaAs Fermi level movement and the change in the potential difference across the oxide. Based on the difference in metal and InGaAs Fermi levels, the change in the Al 1 s oxide binding energies would be expected to be more apparent in the *p*-type sample than in the *n*-type with Al as the metal gate, and more apparent in the *n*-type sample than in the *p*-type with Ni as metal gate.

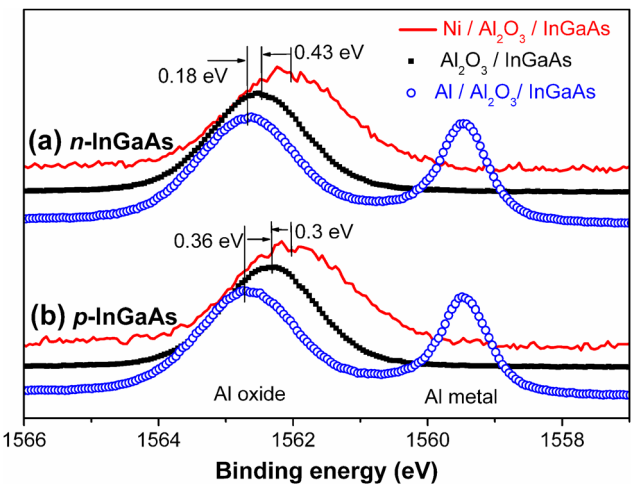

FIG. 5. Al 1s spectra showing BE shift due to the the changes in the potential across the Al_2O_3 layer caused by different work function metals and also the Fermi level movement in the InGaAs for (a) *n*-InGaAs and (b) *p*-InGaAs. The presence of a metallic Al 1s signal at ~1559.5 eV binding energy originates from the metal cap.

Figure 5 shows the changes in binding energy of the Al 1s oxide peak (at 1562 eV) for the *n*- and *p*-InGaAs substrate resulting from metal deposition. For *n*-InGaAs, the deposition of the low work function Al only results in a small increase in the Al 1s peak binding energy in the Al_2O_3 (~0.18 eV), while for the *p*-InGaAs the deposition of Al results in a more significant increase in the binding energy (~0.36 eV) reflecting the larger Fermi level difference between *p*-InGaAs and Al gate. For *n*-InGaAs, the deposition of Ni results in a decrease in the Al 1s peak binding energy (~0.43 eV), while for the *p*-InGaAs the deposition of high work function Ni results in a lower decrease in the binding energy (~0.3 eV), consistent with the larger Fermi level difference between *n*-InGaAs and Ni compared to the case of *p*-InGaAs. All of these changes are consistent with the expected shifts and polarity of the band bending in the dielectric layer caused by the low and high work function metals.

The Al 1s peak widths for the metal capped samples broaden when compared to the samples without metal gates reflecting the gradient in the potential across the dielectric layer. The change in the Al 1s binding energy of 0.18 eV measured for the Al gate on *n*-type InGaAs sample results in broadening of 0.09 eV (compared to the no metal gate sample) while a full width half maximum (FWHM) increase of 0.62 eV is measured for Ni on *n*-type InGaAs sample. This infers a larger potential drop across the Al_2O_3 layer for the Ni *n*-type compared to the Al *n*-type samples. In the case of the *p*-type sample, a negligible difference in FWHM was measured for the Al contact, but a 0.46 eV FWHM increase was found for the Ni capped sample, indicating a larger potential drop across the Al_2O_3 layer for the Ni capped *p*-type sample.

IV. CONCLUSION

In summary, C-V analysis and HAXPES measurements have been made on metal/Al_2O_3/InGaAs MOS capacitors

with both high (Ni) and low (Al) work function metal gates. The HAXPES measurements reveal the presence of band bending prior to metal deposition, resulting from a combination of fixed oxide charges and possible donor-type interface states. Following the deposition of metal, the substrate core level BE shift in the expected directions. A reasonable agreement in Fermi level positions for the InGaAs MOS structures is obtained between C-V analysis and HAXPES measurements at zero gate bias. The results point to a partially pinned Al_2O_3/InGaAs interface and suggest a higher interface state density in the lower half of the bandgap. There is a shift in binding energy of the oxide core levels following metal deposition, which is caused by the InGaAs surface Fermi level movement and a change in the potential drop across the Al_2O_3 layer, and the shifts are in the expected directions. The broadening of the oxide peak widths indicates a higher potential drop across the Al_2O_3 layer with Ni gate than that with Al gate.

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