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Multi-frequency inversion-charge pumping for charge separation and mobility analysis in high-*k*/InGaAs metal-oxide-semiconductor field-effect transistors

V. Djara, K. Cherkaoui, M. A. Negara, and P. K. Hurley[a)]
Tyndall National Institute, University College Cork, Dyke Parade, Cork, Ireland

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An alternative multi-frequency inversion-charge pumping (MFICP) technique was developed to directly separate the inversion charge density (N_{inv}) from the trapped charge density in high-*k*/InGaAs metal-oxide-semiconductor field-effect transistors (MOSFETs). This approach relies on the fitting of the frequency response of border traps, obtained from inversion-charge pumping measurements performed over a wide range of frequencies at room temperature on a single MOSFET, using a modified charge trapping model. The obtained model yielded the capture time constant and density of border traps located at energy levels aligned with the InGaAs conduction band. Moreover, the combination of MFICP and pulsed I_d-V_g measurements enabled an accurate effective mobility *vs* N_{inv} extraction and analysis. The data obtained using the MFICP approach are consistent with the most recent reports on high-*k*/InGaAs. © *2015 AIP Publishing LLC*.
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I. INTRODUCTION

InGaAs and related compound semiconductors have become serious candidates for replacing strained Si in future complementary metal-oxide-semiconductor device applications due to their remarkable electron mobility.[1] In a metal-oxide-semiconductor transistor (MOSFET), the effective mobility (μ_{eff}) is expressed as[2]

$$\mu_{eff} = \frac{L}{W}\frac{I_d}{q.N_{inv}.V_{ds}}, \tag{1}$$

where L/W is the channel length over width ratio, I_d is the drain current, q is the electron charge, N_{inv} is the inversion-charge density, and V_{ds} is the drain-to-source voltage. The "standard" μ_{eff} extraction method relies on the combination of split capacitance *vs* voltage (*C-V*) and DC drain current *vs* gate voltage (I_d-V_g) measurements to provide the parameters N_{inv} and I_d/V_{ds}, respectively. While this method enables highly accurate mobility extraction in SiO_2/Si MOSFETs, its accuracy in emerging high-*k*/InGaAs devices with a relatively high density of interface traps (D_{it}), combined with a high density of near-interface oxide traps or "border traps" (D_{bt}), is now questionable. In recent years, significant research efforts were dedicated to solving this issue. For instance, Ali *et al*. combined split *C-V* measurements performed over a range of temperature (*T*) going from 292 K to 35 K with theoretical calculations in order to extract more accurate N_{inv} and μ_{eff} values,[3] while Taoka *et al*. proposed an approach combining split *C-V* and Hall measurements to study the impact of the traps aligned with the InGaAs conduction band on μ_{eff}.[4,5] While both methods yielded important results, access to a cryogenic probe station or a Hall measurement setup (along with gated Hall structures) is not always possible. We, therefore, developed a multi-frequency inversion-charge pumping (MFICP) technique as an alternative approach to analyze the μ_{eff} in high-*k*/InGaAs MOSFETs. The MFICP technique represents an extension of the ICP approach reported by Kerber *et al*. in Ref. 6 for Si devices. Compared to the aforementioned μ_{eff} *vs* N_{inv} extraction methods for high-*k*/InGaAs MOSFETs,[3–5] the MFICP provides several advantages. Indeed, the μ_{eff} *vs* N_{inv} extraction with MFICP only requires measurements of a single MOSFET at room temperature. Moreover, the analysis of the frequency (*f*) response of border traps by MFICP not only enables a direct separation of the inversion charge and the trapped charge but also provides information about border traps located at energy levels aligned with the InGaAs conduction band.

II. EXPERIMENTAL DETAILS

A. Process flow of Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOSFETs

The InGaAs MOSFETs used in this study were fabricated using the process flow reported in Ref. 7. Briefly, the devices featured a *p*-$In_{0.53}Ga_{0.47}As$ channel with a nominal doping of $4 \times 10^{17}/cm^3$. A $(NH_4)_2S$ surface passivation was performed before the formation of a 10-nm-thick Al_2O_3 gate dielectric by atomic layer deposition.[8] The source and drain (S/D) areas were formed by ion implantation. The Pd gate and the Au/Ge/Au/Ni/Au S/D metal contacts were obtained by evaporation and lift-off. The devices received a forming gas (H_2/N_2) anneal to improve the gate stack and the S/D contact performance.[7]

B. Multi-frequency inversion-charge pumping method

The ICP/MFICP setup shown in Fig. 1(a) is similar to that reported in Ref. 6. The S/D terminals are grounded. A square pulse train of variable amplitude increasing from a

[a)]Electronic mail: paul.hurley@tyndall.ie

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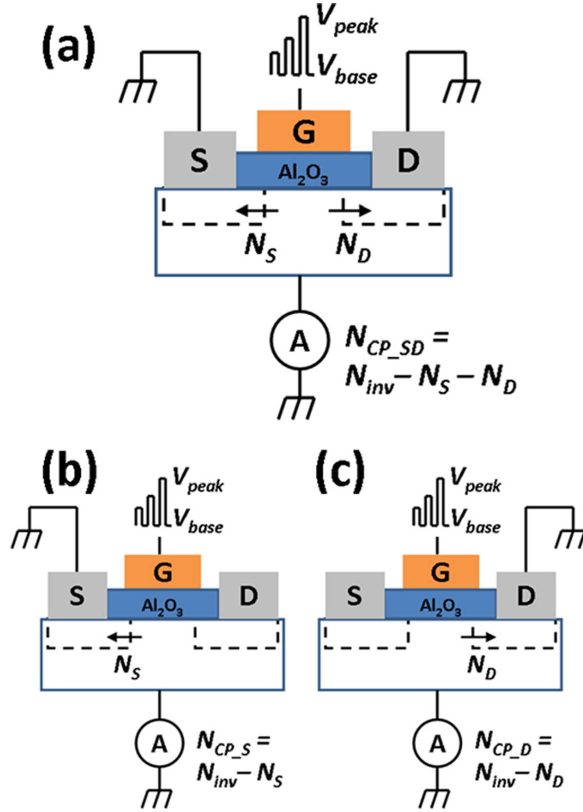

FIG. 1. Schematic representations of the ICP/MFICP setup used to extract N_{inv} in long channel length ($L > 20\,\mu$m) high-k/InGaAs MOSFETs through measurements of (a) N_{CP_SD}, (b) N_{CP_S}, and (c) N_{CP_D}.

base voltage (V_{base}), generally set to a value close to the flat-band voltage (V_{FB}), to a peak voltage (V_{peak}) is applied to the gate terminal. The total pumped charge density (N_{CP_SD}) is measured on the substrate terminal.

The geometrical and trapped charge components of N_{CP_SD} are, respectively, expressed as the first and second terms of the equation[9,10]

$$N_{CP_SD} = \alpha.C_{inv}(V_g - V_T)/q + (D_{it} + D_{bt}.\Delta t_{bt}).\Delta E, \quad (2)$$

where α is the fraction of N_{inv} recombining in the substrate, C_{inv} is the inversion capacitance, V_T is the threshold voltage, Δt_{bt} is the oxide thickness over which the border traps are probed, and ΔE is the energy interval swept by the Fermi level when V_g increases from V_{base} to V_{peak}. It is noted that, here, D_{it} refers to interface traps located at energy levels aligned with the $In_{0.53}Ga_{0.47}As$ bandgap, while D_{bt} refers to border traps located at energy levels aligned with the $In_{0.53}Ga_{0.47}As$ conduction band.

The ICP method applied to devices featuring low D_{it} and D_{bt}, such as SiO_2/Si MOSFETs, enables a direct extraction of N_{inv} by simply maximizing the geometrical component,[11] through the use of long channel ($L > 20\,\mu$m) devices in combination with fast (10 ns) pulse rise time (t_r) and fall time (t_f).[6] Under such conditions, a quantity $\alpha \cdot N_{inv}$ is forced to recombine in the substrate and contribute to N_{CP_SD}. A correction for the quantity $(1-\alpha).N_{inv}$, representing the sum of the charge density lost by diffusion to the source (N_S) and to the drain (N_D), is applied through the measurements of N_{CP_S} [Fig. 1(b)] and N_{CP_D} [Fig. 1(c)]. Following the measurements of N_{CP_SD}, N_{CP_S}, and N_{CP_D}, a corrected pumped charge density (N_{CP}) equal to N_{inv} can be obtained using the relationship:

$$N_{CP} = N_{CP_S} + N_{CP_D} - N_{CP_SD}. \quad (3)$$

However, for the case of devices featuring relatively high D_{it} and D_{bt}, such as high-k/InGaAs MOSFETs, further attention needs to be dedicated to the selection of the ICP measurement parameters in order to not only maximize the geometrical component, but also minimize the trapped charge component.

In Section III C 1, we demonstrate that V_{base} can be raised in order to maintain most of the interface traps, having energy levels located within the $In_{0.53}Ga_{0.47}As$ bandgap to be constantly occupied and, therefore, not contributing to N_{CP}. Similarly, in Section III C 2, we show that the duty cycle (D) of the pulse train applied to the gate terminal can be reduced to minimize the transient charging time (t_{charge}) of border traps, maintaining most border traps constantly unoccupied and, therefore, not contributing to N_{CP}.

In our proposed MFICP approach, where ICP measurements are performed over a wide range of f at a fixed D, a modulation of the border trap response as a function of $t_{charge} = D/f$ is observed. This enables the effective separation of the inversion charge from the trapped charge by fitting the experimental N_{CP} *vs* t_{charge} data using a charge trapping model[12] that we modified to account for N_{inv} (Section III D).

III. RESULTS AND DISCUSSION

A. Interface trap density profile

Fig. 2 shows the D_{it} *vs* V_g profile obtained on our fabricated $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSFET using the high ($f = 1$ MHz)–low ($f = 2$ kHz) frequency C-V method[13] and the full-conductance method.[14] It is noted that the D_{it} is intentionally plotted against V_g (not against energy) in order to identify the different D_{it} values for varying V_{base}. The D_{it}

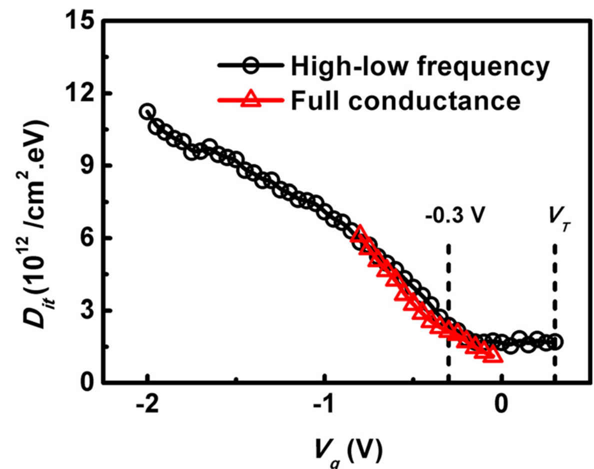

FIG. 2. D_{it} *vs* V_g profile obtained using the high ($f = 1$ MHz)-low ($f = 2$ kHz) frequency and full-conductance methods. The V_T of 0.3 V (Fig. 3) is used to locate the $In_{0.53}Ga_{0.47}As$ E_C.

vs V_g profile presents relatively high D_{it} levels ($>5.5 \times 10^{12}$/cm^2.eV) going towards the middle of the $In_{0.53}Ga_{0.47}As$ bandgap for $V_g < -0.75$ V. However, D_{it} values below 2.5×10^{12}/cm^2.eV are observed near the $In_{0.53}Ga_{0.47}As$ conduction band edge (E_C) for $V_g = -0.3$ V to $V_g = V_T = 0.3$ V (V_T is obtained by extrapolation in the linear region of the up-trace of the single triangular pulse I_d–V_g hysteresis shown in Fig. 3).

B. Evidence of border trap response

Recent studies have indicated the presence of border traps in high-*k*/InGaAs MOS structures using *C-V*,[15–19] charge pumping[20] and high-frequency transconductance[21] measurements. Evidence of the presence of border traps can also be observed in an I_d-V_g characteristic, where it is manifest as a hysteresis loop.[22] A single triangular pulse I_d-V_g hysteresis,[23] performed at $V_{ds} = 50$ mV and $t_r = t_f = 500$ ns, is shown in Fig. 3. A positive V_T shift of $\sim$200 mV is observed on the down trace, indicating electron trapping into border traps during the measurement. From Fig. 3 (inset), it is also clear that the electron trapping involves a significant I_d degradation. Indeed, the maximum I_d (at $V_g = 2.5$ V) increases from 14.5 μA in the DC I_d-V_g characteristic to 16 μA in the pulsed I_d-V_g characteristic, which represents a $\sim$10% increase. This clearly indicates that a pulsed I_d–V_g measurement is required to minimize I_d degradation due to border traps and extract an accurate μ_{eff}.

C. Inversion-charge pumping and minimization of trapped charge component

1. Base voltage and interface trap response

We found that the ICP measurement configuration where $V_{base} \approx V_{FB}$, initially developed in Ref. 6 for a SiO_2/Si interface with typical $D_{it} < 10^{11}$/cm^2.eV (Refs. 24 and 25), was not suitable for the studied Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOSFETs due to the large D_{it} level observed towards the middle of the $In_{0.53}Ga_{0.47}As$ bandgap (Fig. 2). Indeed, in this configuration, any interface trap with an energy level located within the semiconductor bandgap can contribute to N_{CP} and lead to an overestimation of N_{inv}. We, therefore, propose to raise V_{base} in order to maintain most of the interface traps constantly occupied during the ICP measurement and minimize the $D_{it}{\cdot}\Delta E$ contribution to N_{CP}. This is demonstrated in Fig. 4(a) with N_{CP} measurements obtained for V_{base} ranging from -0.9 V to -0.3 V and corrected for the charge density lost to the S/D using (3). As V_{base} is gradually raised to -0.3 V, which corresponds to the region of the D_{it} *vs* V_g profile where the D_{it} is the lowest (Fig. 2), the N_{CP} *vs* V_{peak} curves shift downwards along the *y*-axis until a point where N_{CP} starts rising at V_{peak} close to V_T. This indicates that the response of the majority of the interface traps located within the $In_{0.53}Ga_{0.47}As$ bandgap is removed at $V_{base} = -0.3$ V.

A similar approach was used in Ref. 26, where split *C-V* measurements were performed at a low *T* of 77 K in order to "freeze" the response of the interface traps located slightly below the $In_{0.53}Ga_{0.47}As$ E_C and extract a more accurate N_{inv}. We performed split *C-V* measurements over a wide range of *T* going from 440 K to 35 K [Fig. 4(b)] in order to verify this concept and demonstrate that varying V_{base} in an ICP measurement performed at $T = 292$ K had a similar impact as varying *T* in a split *C-V* measurement. From Fig. 4(b), where the N_{tot}, which is defined here as $N_{tot} = N_{inv} + (D_{it} + D_{bt}{\cdot}\Delta t_{bt}){\cdot}\Delta E$, is plotted against V_g, it is clear that the N_{tot}–V_g curves exhibit a progressive reduction in N_{tot} magnitude as *T* reduces. The similarity between the two trends observed in Figs. 4(a) and 4(b) provides evidence to support the idea that raising V_{base} reduces the N_{CP} contribution of interface states located in the upper part of the $In_{0.53}Ga_{0.47}As$ bandgap.

Having demonstrated the advantage of raising V_{base}, we also need to consider the issue associated with a higher V_{base}. Indeed, as V_{base} is raised towards V_T, the fraction $(1-\alpha)$ of N_{inv} lost to the S/D increases and the correction applied to

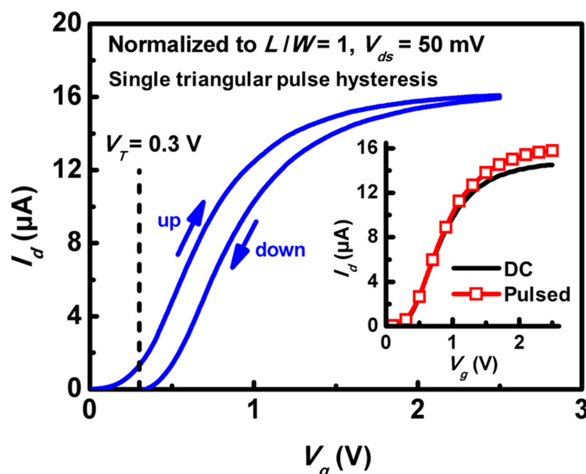

FIG. 3. Single triangular pulse I_d-V_g hysteresis and (inset) comparison of DC and pulsed I_d-V_g characteristics. The measurements were performed at $V_{ds} = 50$ mV. For the single triangular pulse I_d-V_g, $t_r = t_f = 500$ ns, while for the pulsed I_d-V_g, $t_r = t_f = 10$ ns, and $f = 1$ MHz. A V_T of 0.3 V was extracted from the up-trace of the single triangular pulse I_d-V_g by extrapolation in the linear region.

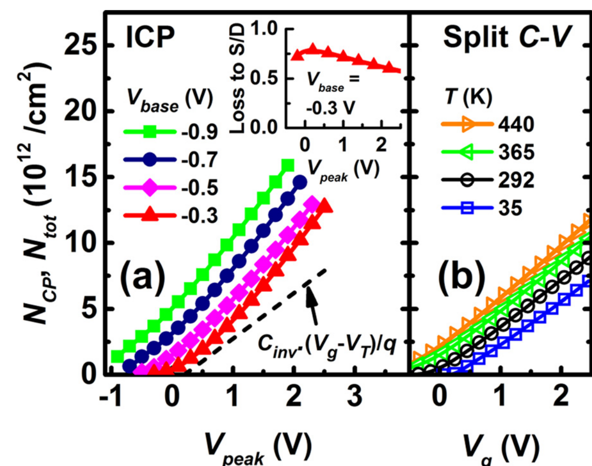

FIG. 4. (a) N_{CP} *vs* V_{peak} obtained from ICP performed on a 40-μm-channel-length device at $f = 1$ MHz and $D = 50\%$ with V_{base} ranging from -0.3 V to -0.9 V. The D_{it} contribution to N_{CP} reduces as V_{base} is raised. The curves "curl up" and deviate from the theoretical $C_{inv}.(V_g - V_t)/q$ curve. (inset) Loss to S/D $(1-\alpha)$ *vs* V_{peak} obtained for $V_{base} = -0.3$ V. (b) N_{tot} *vs* V_g obtained by split *C-V* at $f = 1$ MHz over a range of *T* going from 440 K to 35 K. The D_{it} contribution to N_{tot} reduces as *T* is reduced.

N_{CP} using (3) becomes larger. This is explained by the fact that as V_{base} increases, the barrier height of the space charge region increases, impeding the recombination of the inversion charge in the substrate and favouring its diffusion to the S/D, in agreement with Ref. 11. However, from examination of the inset of Fig. 4(a), it is evident that even with $V_{base} = -0.3$ V, the fraction α of N_{inv}, which is not lost to the S/D, is still 22% or greater. Consequently, it is possible to select V_{base} to minimise the $D_{it}{\cdot}\Delta E$ contribution (of interface traps at energy levels located within the $In_{0.53}Ga_{0.47}As$ bandgap) to N_{CP} and still extract a correct N_{inv}. However, it is important to note that the remaining $D_{it}{\cdot}\Delta E$ contribution to N_{CP} sets the lower limit for accurate N_{inv} extraction where $D_{it}{\cdot}\Delta E$ is not negligible anymore compared to N_{inv}.

Going back to Fig. 4(a) and considering a theoretical C_{inv} of 5.5×10^{-7} F/cm^2, obtained for the Pd/Al_2O_3 (10 nm)/$In_{0.53}Ga_{0.47}As$ gate stack in our previous work,[27] we can compare the measured N_{CP}–V_{peak} ($V_{base} = -0.3$ V) curve to a theoretical $C_{inv}.(V_g–V_T)/q$ curve. From this comparison, it is clear that the N_{CP}–V_{peak} curve "curls up" and significantly deviates from $C_{inv}.(V_g–V_T)/q$ as V_{peak} increases. This "curling up" can be explained by the fact that the ΔE swept by the Fermi level going from V_{base} to V_{peak} increases with V_{peak}. As a result, the $D_{bt}{\cdot}\Delta t_{bt}{\cdot}\Delta E$ contribution to N_{CP} also increases with V_{peak}, leading to the "curling up" observed in the N_{CP}–V_{peak} curves. It is noted that this assumes an increasing $D_{bt}{\cdot}\Delta t_{bt}$ with ΔE, in agreement with Refs. 4, 5, and 27.

2. Transient charging time and border trap response

To minimize the $D_{bt}{\cdot}\Delta t_{bt}{\cdot}\Delta E$ contribution to N_{CP} in our ICP measurements, we propose to reduce t_{charge} by reducing D and keeping $f = 1$ MHz. It is noted that this approach is based on the premise that, since border traps capture electrons from the inversion layer (Fig. 3), the time to charge a border trap must be larger than that required to form the inversion layer. The impact of D (t_{charge}) on N_{CP} is presented in Fig. 5, where D (t_{charge}) is gradually reduced from 50% (500 ns) to 5% (50 ns). The "curling up," attributed to the $D_{bt}{\cdot}\Delta t_{bt}{\cdot}\Delta E$ contribution, gradually reduces as D reduces. At $D = 5\%$, the N_{CP}–V_{peak} curve nearly matches the theoretical $C_{inv}.(V_g–V_T)/q$ curve and the "curling up" disappears, clearly indicating that the $D_{bt}{\cdot}\Delta t_{bt}{\cdot}\Delta E$ contribution to N_{CP} is minimized.

D. Multi-frequency inversion-charge pumping for trapped charge and inversion charge separation

Fig. 6 shows MFICP measurements performed for f increasing from 10 kHz to 2 MHz with $D = 50\%$. It is noted that N_{CP} is plotted against f on the top x-axis and against t_{charge} on the bottom x-axis (as $D = 50\%$, $t_{charge} = 0.5/f$). N_{CP} increases as f reduces and a clear N_{cp} saturation is reached for $f \lesssim 100$ kHz ($t_{charge} \gtrsim 5\ \mu$s), indicating a full border trap response in that f range. In the high f region, however, no N_{CP} saturation is observed. This suggests that some border traps still respond at $f > 2$ MHz. This result is in line with the work reported in Ref. 21, where evidence of "fast" border traps responding to $f > 1$ GHz is demonstrated. Unfortunately, the

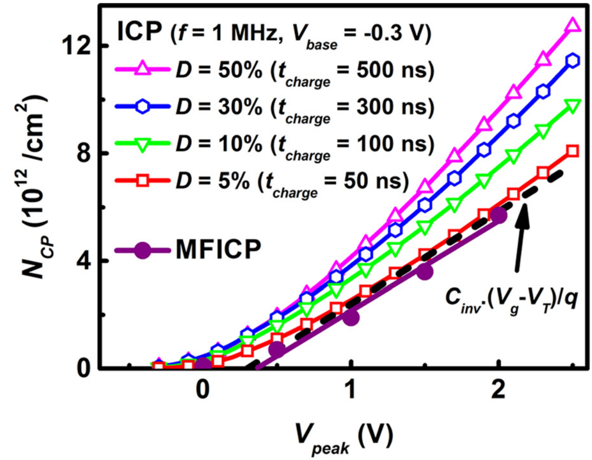

FIG. 5. N_{CP} vs V_{peak} obtained from ICP performed on a 40-μm-channel-length device at $f = 1$ MHz and $V_{base} = -0.3$ V with D (t_{charge}) varied from 50% (500 ns) to 5% (50 ns). The ICP curve at $D = 5\%$ nearly matches the theoretical $C_{inv}(V_g - V_T)/q$ curve. Note: the MFICP data obtained from Section III D are also shown to highlight the consistency between the ICP and MFICP methods.

GHz frequency range is not accessible with MFICP. Indeed, considering the model for the recombination of the electrons of the inversion layer with the holes of the p-type substrate

$$N_{inv}(t) = N_{inv}(0)\exp\left(-\frac{t}{\tau_e}\right), \tag{4}$$

and an electron lifetime (τ_e) of 30 ns for a p-$In_{0.53}Ga_{0.47}As$ doping of 4×10^{17}/cm^3,[28] we calculated that a channel with $N_{inv} = 10^{11}$/cm^2, 10^{12}/cm^2, and 10^{13}/cm^2 would be effectively depleted ($N_{inv} < 10^9$/cm^2) in approximately 130 ns, 210 ns, and 270 ns, respectively. This indicates that it is not possible to perform ICP measurements at $f > 2$ MHz and $D = 50\%$ as the transient discharge time [$t_{discharge} = (1 - D)/f$] becomes

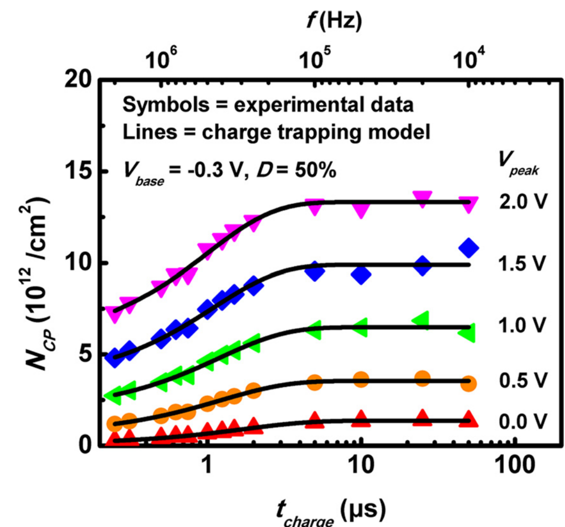

FIG. 6. N_{CP} plotted against f on the top x-axis and against $t_{charge} = 1/(2.f)$ on the bottom x-axis. The symbols show the experimental data obtained from the measurements performed on a 40-μm-channel -length device with $V_{base} = -0.3$ V and $D = 50\%$. The V_{peak} was varied from 0 V to 2 V. The lines represent the fitting of the data with the proposed charge trapping model (4).

too short to allow the full N_{inv} recombination, leading to an underestimation of N_{inv}. However, the use of a model to describe the variation of N_{CP} with f (or t_{charge}) can be employed to predict N_{inv} and extract border trap distribution parameters for each value of V_{peak}

$$N_{CP} = N_{inv} + D_{bt}.\Delta t_{bt}.\Delta E.[1-\exp(-(t_{charge}/\tau)^{\beta})], \quad (5)$$

where τ is the capture time constant, and β is the distribution factor of capture cross section (σ). This model is similar to the one reported in Ref. 12, but includes N_{inv} and assumes negligible $D_{it}{\cdot}\Delta E$ contribution to N_{CP} owing to an appropriate V_{base} selection.

The τ, β, $D_{bt}{\cdot}\Delta t_{bt}{\cdot}\Delta E$, and N_{inv} values obtained from the fitting without manual intervention of the multi-frequency N_{CP} *vs* t_{charge} data (Fig. 6) using (5) are summarized in Table I. Adjusted R^2 values ranging from 0.964 to 0.997 were obtained, indicating a good fit of the model to the experimental data. As V_{peak} increases from 0 V to 2 V, a decrease in τ from 1.7 μs to 1.0 μs is observed, consistent with an electron distribution located closer to the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface at higher V_{peak}. These τ values are consistent with the values reported in Refs. 3, 29, and 30 for traps located at energy levels aligned with the $In_{0.53}Ga_{0.47}As$ conduction band. In the charge trapping model, the distribution factor β, which represents the distribution width of σ, can range between 1.0 and 0. A β value of 1.0 corresponds to a discrete σ, while values approaching 0 indicate very wide distributions of σ. The fact that our experimental data are best fitted with $\beta = 1.0$ indicates a discrete σ. This also suggests that the border traps are located in a plane near the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface and are not distributed throughout the oxide thickness, in line with Ref. 19. Moreover, it is possible to estimate σ using

$$\sigma = 1/(N.v_{th}.\tau), \quad (6)$$

where N is the volume inversion density and v_{th} is the electron thermal velocity. For this demonstration, σ is calculated for $V_{peak} = 2$ V, corresponding to the case where the device is in strong accumulation. Using a self-consistent Poisson-Schrödinger solver, we calculated an inversion layer thickness (t_{inv}) of 14 nm for $N_{inv} = 5.7 \times 10^{12}$/cm^2 (Table I), yielding $N = N_{inv}/t_{inv} = 4.1 \times 10^{18}$/cm^3. With $N = 4.1 \times 10^{18}$/cm^3, $v_{th} = 5.5 \times 10^7$ cm/s (Ref. 15), and $\tau \sim 1.0$ μs (Table I), we obtain $\sigma \sim 5 \times 10^{-21}$ cm^2. This σ is more than four orders of magnitude smaller than the values typically reported for interface traps in the high-*k*/InGaAs system.[15,20,31] This observation is in line with Ref. 32, which brings further evidence of a charge trapping process involving tunnelling into

TABLE I. Model parameters τ, β, $D_{bt}{\cdot}\Delta t_{bt}{\cdot}\Delta E$, and N_{inv} fitted without manual intervention over a range of V_{peak} going from 0 V to 2 V. The adjusted R^2 values indicate the quality of each fit.

V_{peak} (V)	0	0.5	1	1.5	2
τ (μs)	1.7	1.2	1.2	1.1	1.0
β	1.0	1.0	1.0	1.0	1.0
$D_{bt}{\cdot}\Delta t_{bt}{\cdot}\Delta E$ (10^{12}/cm^2)	1.4	2.9	4.6	6.3	7.8
N_{inv} (10^{12}/cm^2)	0.1	0.7	1.9	3.5	5.7
Adjusted R^2	0.997	0.991	0.984	0.964	0.991

border traps. A distance (x) for the spatial location of the border traps relative to the $In_{0.53}Ga_{0.47}As$ interface can be estimated using the relationship[33]

$$x = \lambda \ln(t/\tau), \quad (7)$$

where λ is the attenuation coefficient and t is the tunnelling time. Assuming a λ value within the typical range of 9.8×10^{-9}–1.25×10^{-8} cm reported for the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface[16–18,21,30] and considering that N_{CP} saturation is reached at $t \sim 5$ μs (Fig. 6), we obtain a distance x of about 1.6–2.1 Å from the interface. This range of values is in agreement with other studies of border traps in the high-*k*/InGaAs system.[18,21,34]

It is noted that the discussion of the $D_{bt}{\cdot}\Delta t_{bt}{\cdot}\Delta E$ data relies on the energy *vs* gate bias and trap density *vs* energy profiles obtained from a previous *C-V* study that we performed on the same set of devices as that used in this study.[27] Moreover, since Δt_{bt} cannot be obtained from our ICP-based approach, a value of $\sim$2 Å is assumed from Ref. 21. This assumption is in agreement with the extracted β value of 1.0 (Table I) suggesting a discrete σ. Therefore, considering from our previous work[27] that an energy range of $\sim$0.8 eV is swept when V_g goes from $V_{base} = -0.3$ V to $V_{peak} = 2$ V and assuming $\Delta t_{bt} \sim 2$ Å (Ref. 21), a $D_{bt}{\cdot}\Delta t_{bt}{\cdot}\Delta E$ of 7.8×10^{12}/cm^2 (Table I) equates to a D_{bt} of $\sim 4.9 \times 10^{20}$/cm^3.eV. This estimated value is comparable to the peak D_{bt} value of 1.6×10^{21}/cm^3.eV reported in Ref. 21. Furthermore, the integration of our trap density *vs* energy profile across a ΔE of $E_C + 0.05$ eV to $E_C + 0.35$ eV corresponding to a V_g of 0.5 V–2 V yields a trap density of 4.4×10^{12}/cm^2. This value is in excellent agreement with the value of 4.9×10^{12}/cm^2 obtained by subtracting the $D_{bt}{\cdot}\Delta t_{bt}{\cdot}\Delta E$ values obtained using the MFICP method for $V_{peak} = 2$ V and 0.5 V (Table I).

This excellent agreement shows further evidence of the validity of our proposed MFICP technique for trapped charge and inversion charge separation. Moreover, the negligible N_{inv} value at $V_{peak} = 0$ V is consistent with a V_T of 0.3 V (Fig. 3). As V_{peak} increases from 0.5 V to 2 V, N_{inv} increases from 7.0×10^{11} to 5.7×10^{12}/cm^2. These N_{inv} values are slightly lower than those obtained using ICP with $f = 1$ MHz and $D = 5\%$ (Fig. 5), confirming the presence of "fast" border traps responding in less than 50 ns, in line with Ref. 21. Furthermore, it is important to note that the N_{inv} values obtained from MFICP are in excellent agreement with reported N_{inv} values obtained at the same gate overdrive using Hall measurements performed on similar $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSFETs featuring sulfur passivation of the $In_{0.53}Ga_{0.47}As$ interface and Al_2O_3 thicknesses of 6 nm and 8 nm.[4,5]

E. Effective mobility extraction and analysis

The effective separation of the inversion charge and the trapped charge allows for a more accurate determination of μ_{eff}. This is shown in Fig. 7(a), where the μ_{eff} values, extracted from the ICP (Fig. 5) and MFICP (Fig. 6) methods both combined with a pulsed I_d-V_g measurement [Fig. 3 (inset)], are compared. The ICP data indicate that, as D reduces from 50% to 5%, the peak μ_{eff} increases in

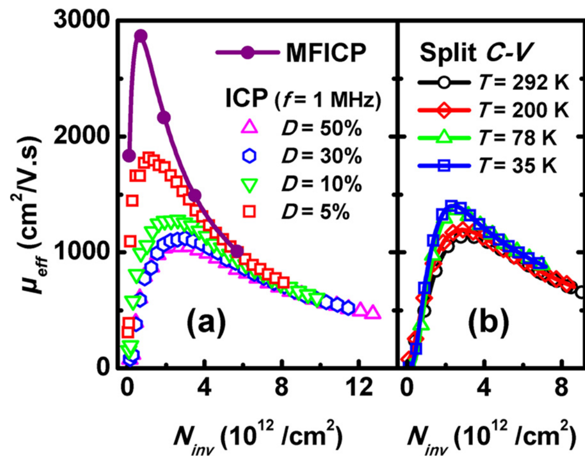

FIG. 7. (a) Comparison of μ_{eff} *vs* N_{inv} extracted using the ICP ($f = 1$ MHz, $D = 50\%$, 30%, 10%, and 5%) and MFICP methods both combined with a pulsed I_d-V_g measurement. (b) Comparison of μ_{eff} *vs* N_{inv} extracted from split *C-V* and DC I_d-V_g measurements performed at $T = 292$ K, 200 K, 78 K, and 35 K.

magnitude and its position shifts towards lower N_{inv} values. This arises from the reduction of the trapped charge component of N_{CP} with lower D, yielding a better estimation of N_{inv}. However, as MFICP enables the complete removal of the trapped charge component of N_{CP}, N_{inv} is not overestimated and a more accurate μ_{eff} *vs* N_{inv} is obtained.

The μ_{eff} obtained with MFICP reaches 2850 cm^2/V.s at $N_{inv} = 7 \times 10^{11}$/cm^2. It is noted that peak μ_{eff} values ranging from 2000 to 3000 cm^2/V.s were reported for high-*k*/$In_{0.53}Ga_{0.47}As$ devices following correction for traps aligned with the $In_{0.53}Ga_{0.47}As$ conduction band.[3,26,35–37] A strong N_{inv} dependence is observed as μ_{eff} rapidly drops from 2850 cm^2/V.s at $N_{inv} = 7 \times 10^{11}$/cm^2 to 600 cm^2/V.s at $N_{inv} = 1 \times 10^{13}$/cm^2. This suggests a μ_{eff} dominated by surface roughness, in agreement with Refs. 26, 35, 37, and 38. This is also confirmed by the lack of temperature dependence in the $N_{inv} > 5 \times 10^{12}$/cm^2 region of the μ_{eff} curve [Fig. 7(b)], extracted from split *C-V* ($f = 1$ MHz) and DC I_d–V_g measurements performed over a range of T going from 292 K to 35 K (not shown). However, while an increase in μ_{eff} is observed for $N_{inv} < 5 \times 10^{12}$/cm^2 as T reduces, consistent with Ref. 26, it is very clear that some of the trapped charge cannot be "frozen out" with low T, which confirms the presence of a temperature-independent charge trapping process involving tunnelling into border traps. Consequently, the peak μ_{eff} extracted from low-T split *C-V* remains lower than that extracted with the ICP ($D = 5\%$) and MFICP methods. This brings further evidence of the relevance of our proposed MFICP approach and highlights the limitation of the split *C-V* technique for accurate μ_{eff} *vs* N_{inv} extraction in high-*k*/InGaAs MOSFETs featuring relatively large D_{bt}.

IV. CONCLUSIONS

We successfully demonstrated the separation of the inversion charge and the trapped charge in high-*k*/InGaAs MOSFETs using our proposed MFICP technique. This approach offers the advantage of only requiring measurements performed at room temperature on a single long-channel MOSFET. The obtained values for the border trap capture time constant, capture cross section, spatial location, and density were all in line with the most recent literature values, confirming the validity of the technique. Finally, the comparison of the μ_{eff} *vs* N_{inv} extracted from the MFICP and split *C-V* techniques highlighted the limitation of the split *C-V* approach for high-*k*/InGaAs MOSFETs featuring relatively large D_{bt}.

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