EFFICIENT TV WHITE SPACE FILTER BANK TRANSCEIVER

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ABSTRACT

Future devices operating in the TV white space (TVWS) spectrum will require to access different bands at different locations and times in order to avoid interference to incumbent users, requiring agility and sufficient spectral masks to satisfy regulators. Further, with very high-speed ADCs and DACs becoming reality, the purpose of this paper is to present a transceiver front-end capable of simultaneously up- and downconverting a significant portion of the UHF band. The proposed approach takes a two-stage filter-bank conversion for implementation on state-of-the-art FPGAs. We present three different parameterisations, which are compatible with the 40 TVWS channels between 470 and 790 MHz in Europe, and compare them in terms of complexity and latency.

1. INTRODUCTION

The possibility of wireless applications utilising TV white space sets a number of requirements to potential devices, including frequency agility in order to select and change channels depending on geolocation, and the strict adherence to spectral masks which are likely to be imposed by regulators to protect incumbent users [1]. The permitted interference levels outlined in Fig. 1 cannot be met by standard orthogonal frequency division multiplexing (OFDM). Therefore, filter bank techniques that pre-date OFDM [2, 3, 4, 5] have recently seen a revival in a number of communications areas [6, 7, 8] due to their superior spectral confinement and resulting advantages in terms of synchronisation over OFDM [9, 10, 11].

Most filter bank transceivers operate in the baseband, where a number of subchannels or multiple users are allocated to well defined frequency bands. Popular structures include DFT modulated filter banks [2, 9] and derivatives [12], but also iterated halfband schemes such as [5]. Many filter bank schemes currently evolving in the context of frequency agility and cognitive radio [13, 14] are also located in the baseband. Filter banks have also been used to combine the outputs of different analogue-to-digital converters (ADCs) by means of a hybrid filter bank [15].

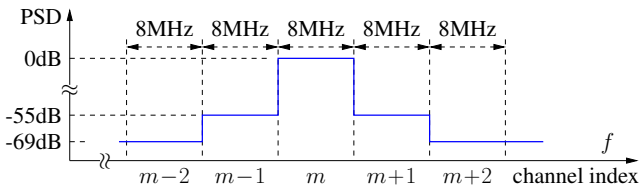

Fig. 1. Spectral mask defining PSD levels in adjacent ($m \pm 1$) and next-adjacent 8MHz TVWS channels ($m \pm 2$) [1].

With substantial progress in the area of ADCs and digital-to-analogue converters (DACs), see e.g. [16], the idea of operating a filter bank receiver up to radio frequency is appealing and could yield the frequency agility and flexibility required of future TVWS devices. Therefore, the aim of this paper is to explore a filter bank based transceiver that is capable of converting from and to RF, and explore some of its characteristics in terms of cost, latency, and selectivity.

The paper is organised as follows. Sec. 2 provides an overview over the proposed system, while Sec. 3 will be dedicated to the filter bank components of the multistage approach. Implementation issues are discussed in Sec. 4, with simulations presented in Sec. 5. Finally, conclusions are drawn in Sec. 6.

2. PROPOSED SYSTEM SETUP

The proposed transceiver system aims to downconvert all 40 channels within the TVWS spectrum from 470MHz to 790MHz. On the transmitter side, an upconverter should be capable to adhering to the strict spectral mask which regulators are expected to impose [1]. While OFDM-based standards will exhibit too poor a frequency selection to comply with this mask, filter bank multicarrier (FBMC) systems are expected to provide sufficient frequency selectivity to fulfill this specification.

The implementation of an FBMC system is numerically most efficient with a single filter bank, as it requires less coefficients and therefore lower latency than an iterated filter bank with several stages. However, targetting an FPGA implementation, there is a limit to the sampling rate that devices are currently able to achieve. If data is externally multiplexed and demultiplexed to exchange polyphase components with the FPGA, then a second limitation restricts the number of input

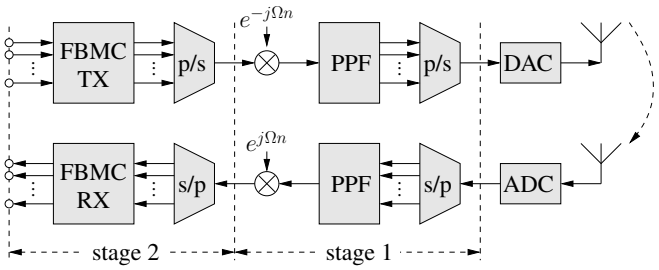

Fig. 2. Proposed multi-stage TVWS filter bank transmitter (above) and receiver (below) with a polyphase filter (PPF) in stage 1 and an FBMC modulator in stage 2.

and output streams. For this reason, a multi-stage approach is adopted. The first two stages of the proposed transceiver system are outlined in Fig. 2, which links 40 baseband TVWS to an RF signal.

Starting with the receiver in the lower branch of Fig. 2, the incoming RF signal is directly sampled at rate f_s with R_r bits resolution. In a first stage, a complex valued polyphase bandpass filter creates an analytic signal which, by appropriate modulation with a complex exponential of normalised angular frequency Ω, is shifted in frequency such that the 40 channels of the TVWS spectrum sit at DC. In a second stage, an analysis filter bank extracts the 40 TVWS channels. The filter bank is oversampled by a factor two, i.e. outputs are sampled at 16MHz in order for ease of synchronisation and further filtering in the individual channels. For test purposes, and not shown in Fig. 2, a third stage creates Nyquist systems within the individual 8MHz channels in order to measure distortion and leakage.

The transmitter is implemented with matching dual components to the receiver, combining the 40 TVWS channels by means of an oversampled synthesis bank in stage 2, and correcting the band position by modulation prior to filtering with a complex bandpass filter in stage 1. The real part of the analytic output then forms the RF signal. Not shown in Fig. 2 is preprocessing in a third stage, which creates an overall Nyquist system with stage 3 in the receiver for test and measurement purposes.

3. FILTER BANK TRANSCEIVER

This section outlines the dual operations applied in various stages of the proposed TVWS transceiver in Fig. 2.

3.1. Stage 1

Stage 1 of the filter bank receiver extracts the TVWS bands, with a centre frequency $f_c = 630$MHz, from the RF signal sampled at $f_\mathrm{s} = 1.92$GHz, with the aim of creating an analytic baseband signal with TVWS channels aligned from DC to 320MHz. This can be achieved by means of an analytic bandpass filter centred at f_c, whose bandlimitation will allow

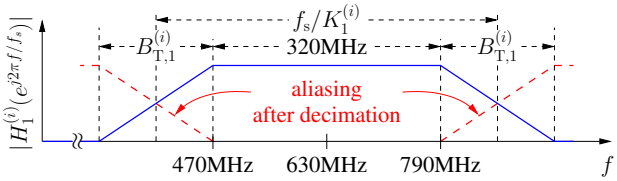

Fig. 3. Stage 1 filter with passband width of 320MHz to capture TVWS spectrum, and with transition bandwidth $B_{\mathrm{T},1}^{(i)}$.

decimation by a factor $K_1^{(i)}$, where i is an index into different possible implementations. The required filter characteristic is shown in Fig. 3, whereby aliasing is permitted in the transition band, therefore enabling a transition bandwidth $B_{\mathrm{T},1}^{(i)}$,

$$B_{\mathrm{T},1}^{(i)} = \frac{1.92\mathrm{GHz}}{K_1^{(i)}} - 320\mathrm{MHz} \quad . \tag{1}$$

Positive definiteness of (1) admits decimation ratios $K_1^{(i)} \in [1, 5]$, while sampling rates for current state-of-the-art FPGAs impose a limit to $3 \leq K_1^{(i)} \leq 5$ and hence three different implementations $i = \{1, 2, 3\}$, with $K_1^{(i)} = i + 2$.

To align the decimated TVWS spectrum with DC, a correction by the lower frequency of 470MHz after aliasing can be accomplished by selecting $\Omega = 2\pi 470\mathrm{MHz} \cdot K_1^{(i)}/f_\mathrm{s}$. An alternative implementation would first demodulate the incoming signal by a complex exponential to DC, where a real valued lowpass filter instead of the bandpass $H_1^{(i)}(e^{j\Omega})$ can be employed. After lowpass filtering, a second modulation step would then re-align the decimated TVWS spectrum with DC, although this operation could also be corrected in stage 2 by ensuring that the 8MHz TVWS channels are extracted by applying appropriate frequency offsets.

The transmitter implementation of stage 1 is a dual of the receiver, with a frequency shift by Ω followed by upsampling. Interpolation can be performed with the bandpass $H_1^{(i)}(e^{j\Omega})$, whereby the widened transition bands do not matter due to the input signal to stage 1 fulfilling tight frequency mask characteristics. The real part of the analytic signal at the bandpass output is then passed to an ADC operating at RF rate.

3.2. Stage 2

The different designs for stage 1 necessitate different filter bank approaches for stage 2. With an RF sampling rate of 1.92GHz and decimations by $K_1^{(i)}$ in stage 1, $K_2^{(i)} = \{80, 60, 48\}$ channels of 8MHz bandwidth that have to be extracted for the three designs in stage 2, respectively, as contained in Tab. 1. For each of the three designs, only 40 of the $K_2^{(i)}$ channels will be utilised. Due to their uniform ordering, a modulated filter bank is an efficient approach, which is oversampled by a factor of two to firstly ease the synchronisation efforts of individual TVWS channels in the

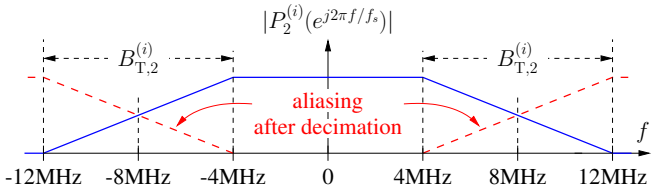

Fig. 4. Stage 2 prototype filter with 8MHz passband width and decimation to 16MHz sampling rate. The absolute bandwidths are identical for all designs, which however differ in their number of bands $K_2^{(i)}$.

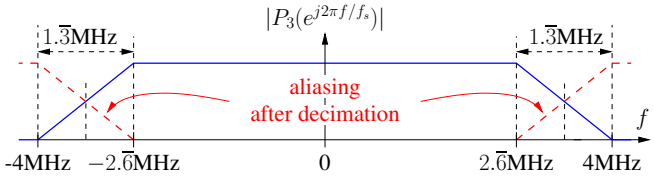

Fig. 5. Stage 3 root Nyquist(3) characteristic. Sampled at 16MHz, this filter restricts the bandwidth to $5.\overline{3}$MHz.

baseband. A second advantage of oversampling is the easing of the prototype filter characteristic, which is outlined in Fig. 4 allowing a maximum possible transition bandwidth $B_{\mathrm{T},2}^{(i)}$. This design characteristic assumes that TVWS channel signals are perfectly bandlimited to within their 8MHz channels by the Nyquist system imposed by stage 3.

We here employ a type of DFT modulated filter bank, in which, different from the standard design, the analysis filter bank in the transmitter employs a generalised IDFT and the synthesis bank in the receiver a generalised DFT, in order to align channels in ascending order from DC to 320MHz.

3.3. Stage 3

This stage represents the baseband processing, which may not necessarily be part of the filter bank transceiver system, containing synchronisation algorithms, appropriate band limitations, and the creation of an overall Nyquist system between transmitter and receiver. In order to achieve a simple test system, for convenience a Nyquist(3) system is operated in stage 3, such that the ultimate baseband signal is sampled at a rate of $16/3$MHz. The required characteristic of the root Nyquist systems employed in transmitter and receiver are shown in Fig. 5. The stopband characteristics of the combined filters in stages 2 and 3 have to satisfy the spectral mask defined in Fig. 1.

4. IMPLEMENTATION

This section elaborates on the implementation on a potential FPGA, focusing on polyphase realisations in Sec.4.1 and on word length considerations in Sec. 4.2

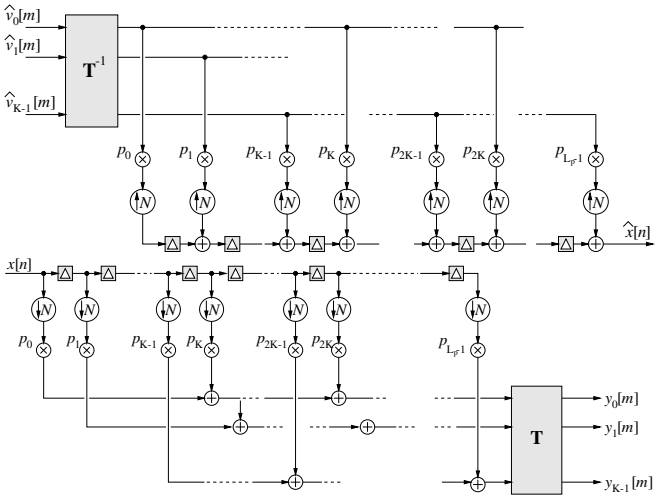

Fig. 6. Polyphase implementation of (top) transmitter and (bottom) receiver filter bank based multicarrier modulation.

4.1. Polyphase Implementations and Computational Cost

For stage 1, the receiver requires a hardware demultiplexer to feed $K_1^{(i)}$ polyphase components of the sampled RF signal into the FPGA for polyphase filtering, while in the transmitter, the output of the polyphase filter components are passed out of the FPGA implementation and will be multiplexed in hardware to form the RF signal.

The implementation in Sec. 3 assumes a complex bandpass polyphase filter, combined with a frequency shift Ω. With a filter length $L_1^{(i)}$, the complexity is $C_1^{(i,a)} = 4L_1^{(i)}/K_1^{(i)} + 4$ real valued multiply accumulates (MACs). Alternatively, the stage 1 signal could be filtered by a real valued lowpass filter, requiring a modulation at both the input and output of stage 1, leading to $C_1^{(i,b)} = 2L_1^{(i)}/(K_1^{(i)}) + 4K_1^{(i)} + 4$. The second implementation is only favoured if

$$C_1^{(i,a)} > C_1^{(i,b)} \quad \leftrightarrow \quad L_1^{(i)} > 2(K_1^{(i)})^2 \quad , \qquad (2)$$

which for values selected in Tab. 1 is unlikely to occur.

For stage 2, different implementations are possible [9]. Since circular buffers are not advantageous for FPGA implementations, we have selected polyphase implementations according to [17], which require only one tapped delay line, a set of multipliers, and the transform on which the modulated filter bank is based, e.g. an FFT, as shown in Fig. 6.

4.2. Word Length Requirements

Below, we explore word length considerations for the receiver and transmitter. In the transmitter, given the spectral mask for TVWS channels in Fig. 1, a dynamic range of -69dB [1] theoretically requires at least 12 bits word length all the way up to the DAC.

In the receiver, the succession of filtering and decimation leads to a gain in effective wordlength, whereby one extra bit is obtained for every oversampling by a factor of 4, since a reduction in bandwidth also leads to a reduction in noise power without curtailing signal power. Thus, the virtual gain in bits for the proposed filter bank transceiver is $\Delta R = \log_4 K = \frac{1}{2}\log_2 K$, where K is the reduction in bandwidth. With the overall reduction in bandwith from 1.92GHz to 8MHz, $K = \frac{1.92\text{GHz}}{8\text{MHz}} = 240$ yielding a gain in resolution by $\Delta R = 3.953$ bits.

The overall gain of $\Delta R = 3.953$ bits is divided over the different filter bank stages into $\Delta R = \Delta R_1^{(i)} + \Delta R_2^{(i)}$ as shown in Tab. 1 for the three different implementations. Thus, the coefficient quantisation for each stage has to be selected such that the greatest gain can be realised, requiring an extra resolution of at least 2 and 3 bits for stage 1 and 2 filters compared to their input signals, respectively. This enables an overall resolution of $R + \Delta R$ bits in the received baseband, where R is the wordlength of the ADC at RF.

5. SIMULATIONS AND RESULTS

This section presents some results of the filter design, shows exemplary PSDs of signals at various stages of the implementation, and summarises performance metrics such as distortion, adjacent channel leakage, and latency for the three different implementations.

5.1. Filter Characteristics and PSDs

Magnitude responses for the prototype filters in the three transceiver stages are designed as root Nyquist systems [18] and shown in Fig. 7. Responses can be seen to satisfy the stopband edges and adjacent channel attenuation of -69dB imposed by the spectral mask in Fig. 1 [1]. While the stage 3 design is common to all three implementations, stage 1 and 2 designs are only shown for $i = 1$ with $K_1^{(3)} = 5$ and $K_2^{(3)} = 48$.

The power spectral densities of simulated signals at stages 1 and 2 are shown in Fig. 8, whereby the signal at stage 1 occupies the TVWS band 470–790MHz, and the stage 2 represents a downconverted TVWS band with $K_2^{(3)} = 48$ channel, of which the first 40 TVWS channels are occupied and the remaining channels are vacated with sufficiently low leakage.

5.2. Performance

With the complexity of the stage 1 filter considered in Sec. 4.1 and polyphase filter bank requiring $2L_2^{(i)} + 4K_2^{(i)}\log_2 K_2^{(i)}$ MACs [17] at the lower rate of stage 2, the total complexity of a transmitter or receiver as shown in Fig. 2, i.e. without

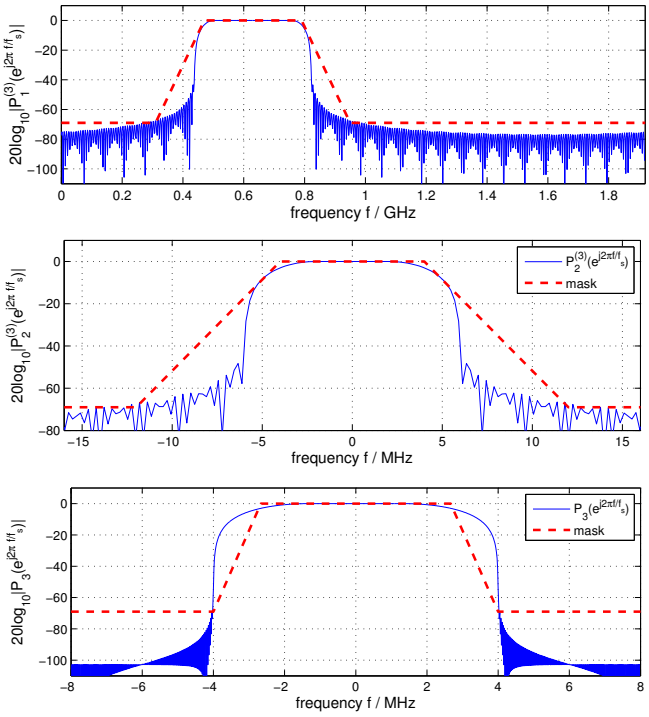

Fig. 7. Magnitude responses of (top) stage 1, (middle) 2, and (bottom) 3 prototype filters.

stage 3, is given by

$$C^{(i)} = \left(L_1^{(i)} + \frac{L_2^{(i)}}{K_2^{(i)}} + 2\log_2 K_2^{(i)} + 1 \right) \frac{4f_\text{s}}{K_1^{(i)}}, \quad (3)$$

measured in real valued MACs/s. The overall complexity in (3) is likely to be dominated by the stage 1 filter of length $L_1^{(i)}$, and is listed for the three different implementations in Tab. 1.

The latency of a filter bank transmitter or receiver, assuming linear phase prototype filters, is given by

$$\Delta^{(i)} = \frac{L_1^{(i)}}{2f_\text{s}} + \frac{L_2^{(i)} K_1^{(i)}}{2f_\text{s}} \quad . \quad (4)$$

The latency will be dominated by the lower rate stage 2 filter, with the overall transmitter or receiver delay for the three implementations shown in Tab. 1.

Testing the overall filter bank transceiver back-to-back as shown in Fig. 2, the reconstruction error between a transmitted and received $5.\overline{3}$MHz channel, as well as the leakage level into adjacent channels, is provided in Tab. 1. Due to the selection of the filter lengths $L_j^{(i)}$ for the jth stage in the ith design to comply with the overall desired spectral mask, all implementations meet the imposed requirement of at least -55dB for adjacent and -69dB for next-adjacent channels [1].

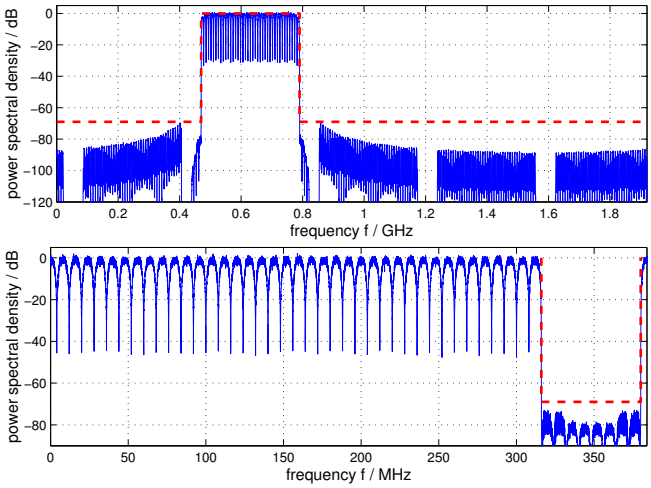

Fig. 8. Power spectral densities of (top) stage 1 and (bottom) stage 2 signals, with spectral masks indicated as dashed lines.

Design i		1	2	3
stage 1	$K_1^{(i)}$	3	4	5
	$\Delta R_1^{(i)}$	0.792	1.000	1.161
	$L_1^{(i)}$	72	128	250
stage 2	$K_2^{(i)}$	80	60	48
	$\Delta R_2^{(i)}$	3.161	2.953	2.793
	$L_2^{(i)}$	800	600	480
$C^{(i)}$ / GMAC/s		244.8	289.6	418.1
delay $\Delta^{(i)}$ / ms		16.69	9.41	6.07
reconstruction error / dB		-55.4	-55.2	-56.1
adjacent channel leakage / dB		-62.8	-62.3	-61.9
next-adj. channel leakage / dB		-71.4	-70.9	-71.2

Table 1. Bandwith reductions K_i for different receiver stages $i = 1, 2$ with associated increase in bit resolution ΔR_i, and other performance measures.

6. CONCLUSIONS

We have discussed a multi-stage filter bank transceiver design with the capability to simultaneously up- and downconvert the entire TVWS range of 40 8MHz wide channels. The designs are motivated by a hypothetical DAC/ADC operating at a sampling rate of 1.92GHz. The multistage approach is required to satisfy sampling rate and input limitations to FPGA devices, resulting in 3 designs with various trade-offs between filtering efforts in stage 1 and stage 2. A design comparison shows that a higher decimation in stage 1 has to be bought at the expense of a higher overall complexity that is dominated by the length of the stage 1 filter. In contrast, latency is dominated by the stage 2 filters, and leads to a design trade-off against complexity.

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