A magnetically isolated gate driver for high-speed voltage sharing in series-connected MOSFETs

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Keywords

«High voltage power converters», «MOSFET», «Device application», «Insulation».

Abstract

A scalable resonant gate drive circuit is described, suitable for driving series-connected MOSFETs in high-voltage, high-speed inverter applications for resistive and capacitive loads. Galvanic isolation is provided by a loop of high voltage wire, which also serves as the resonant inductor in the circuit. Fast dynamic voltage sharing is achieved by delivering equal current to each gate. A prototype is built and tested, demonstrating a 75ns switching time at 5kV using 900V MOSFETs.

Introduction

The construction of a high voltage semiconductor switch is a frequent problem in power electronics. The use of a single insulated-gate device such as a MOSFET or IGBT to block a voltage in excess of 5kV becomes uneconomical in many applications due to size and packaging constraints. As an alternative, several low-voltage devices may be connected in series. Each device supports a fraction of the overall rail voltage in the off-state. Advantageously this arrangement exhibits lower overall on-state resistance for a given silicon area compared to a single MOSFET of the same overall blocking voltage capability [1]. However the construction of a suitably isolated and reliable gate driver circuit and the enforcement of dynamic voltage balance during transient conditions make the practical implementation of this arrangement non-trivial.

Solutions for driving a series-connected MOSFET or IGBT stack as a single high-voltage switch may be split into two groups. In the first group the devices switch simultaneously, and the switching trajectory of each device is constrained within safe limits. This can be achieved using passive or active snubbers [2, 3], or by using local negative feedback and trajectory shaping to enforce dynamic balance by modification of the gate current of individual devices [4, 5, 6]. The latter technique has been reviewed extensively for IGBTs [7]. This arrangement allows the entire stack to switch as rapidly as the individual devices but requires carefully synchronized isolated gate driver circuits and floating power supplies, leading to a high component count and greater associated manufacturing costs. Snubber circuits draw a bias current from the high voltage channel, which incurs significant and unacceptable energy loss in low-power applications where fast switching is required. Isolation of the gate driver circuitry is non-trivial, and optical techniques are often used.

For circuits in the second group, the change in drain-source voltage of one device triggers the gate of the device above it, and thus the devices switch sequentially [1, 8, 9]. It is usually only necessary to drive the gate of the lowest device in the stack, greatly reducing gate driver complexity. For a low-side switch, the gate drive isolation may also be omitted in many applications. However the sequential operation leads to longer switching times, reducing the operating frequency attainable. Switching stresses in the MOSFETs are also unequal, which may result in premature failure. This is a particularly severe limitation for large chains.

To address these issues, a simple and scalable isolated resonant gate driver suitable for driving a series chain of MOSFETs is proposed. A shared transformer is used to provide isolation and deliver an equal current to each gate, resulting in an overall switching speed comparable to that of a single device. Advantageously, dynamic voltage sharing is achieved without drawing current from the high voltage current path or requiring locally referenced supplies. This circuit overcomes the two significant practical challenges in series-connected MOSFET stacks, by providing a simple and reliable isolated gate driver circuit which inherently enforces a condition of dynamic voltage balance.

Proposed Circuit

The proposed gate driver circuit is shown in Fig. 1. Q1A and Q1B comprise a portion of the high voltage MOSFET chain. The high voltage (HV) wire loop links the magnetic paths of the transformers, and introduces a parasitic inductance L_{loop}. This type of double-galvanic insulation arrangement is known in gate driver applications [10].

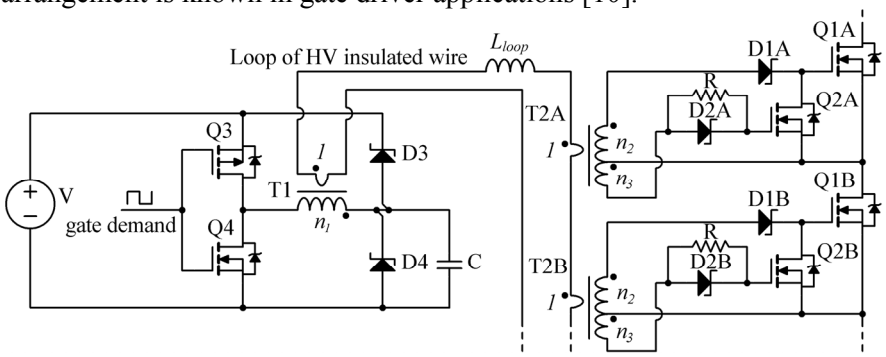

Fig. 1: Circuit diagram of proposed technique; 2 of N stages shown

The transformers T1 and T2 are wound on miniature toroidal ferrite cores, with an inner diameter sufficient to accept a single turn of suitably rated HV wire. MOSFETs Q2, Q3 and Q4 are of a low voltage and current rating, and therefore typically require less gate charge than Q1.

Turn-on Transition

At turn-on, C discharges through T1 and Q4. This induces current in the HV wire loop, causing current to be delivered to each power MOSFET gate through transformers T2 and diodes D1 (Fig. 2). An identical current is supplied to the gate of each power MOSFET. The resonant circuit reduces the energy required from the supply in comparison to a conventional voltage-source gate driver.

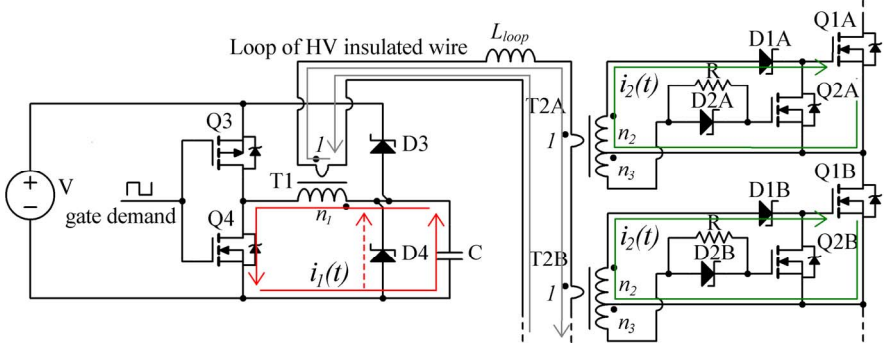

Fig. 2: Current paths during turn-on interval

The analysis of the turn-on cycle may be split into two steps, during which energy is ultimately transferred from primary capacitor C to the gates of Q1.For this purpose, the gates of power MOSFETs Q1 are modelled as ideal capacitances, C_g, and magnetising inductance is neglected.

Step 1: Discharge of primary capacitor C

During step 1, energy is transferred from the primary capacitor C to the resonant circuit formed by the parasitic loop inductance and combined gate capacitance. Neglecting forward voltage drop in Schottky diodes D1, the total gate capacitance for N stages referred to the HV wire loop, C_{loop}, may be found by combining individual referred gate capacitances in series:

$$C_{loop} = \frac{{n_2}^2 C_g}{N} \tag{1}$$

The series combination of C_{loop} and L_{loop} may be referred to the primary winding of transformer T1. In combination with the primary capacitor C, this yields a series-resonant circuit through which energy is efficiently extracted from the primary capacitor C and delivered to the resonant circuit formed by C_{loop} and L_{loop}. An equivalent circuit for step 1 referred to the primary winding of transformer T1 is illustrated in Fig. 3.

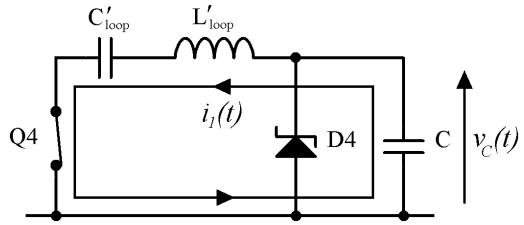

Fig. 3: Equivalent circuit for step 1 at turn-on, referred to primary side

C'_{loop} and L'_{loop} may be found from the turns ratio of T1:

$$C'_{loop} = \frac{{n_2}^2 C_g}{{n_1}^2 N} \tag{2}$$

$$L'_{loop} = {n_1}^2 L_{loop} \tag{3}$$

The primary current, $i_1(t)$, may be written:

$$L'_{loop} \frac{d^2 i_1(t)}{dt^2} + \left(\frac{1}{C'_{loop}} + \frac{1}{C}\right) i_1(t) = 0 \tag{4}$$

Initially, the voltage across C is equal to the primary rail voltage V, the voltage across the referred gate capacitances is zero and the current in the HV wire loop is zero. Solving (4) for these initial conditions yields a sinusoidal solution for primary current:

$$i_1(t) = V\sqrt{\frac{C.C'_{loop}}{C.L'_{loop}+C'_{loop}.L'_{loop}}}\sin\left(\sqrt{\frac{C+C'_{loop}}{C.C'_{loop}.L'_{loop}}}.t\right) \tag{5}$$

An expression for the voltage across C, $v_c(t)$, may be derived from (5) by integration:

$$v_c(t) = -\frac{1}{C}\int i_1(t).dt \quad ; \quad v_c(0) = V$$
$$v_c(t) = V - \frac{V.C'_{loop}}{C+C'_{loop}}\left(1 - \cos\left(\sqrt{\frac{C+C'_{loop}}{C.C'_{loop}.L'_{loop}}}.t\right)\right) \tag{6}$$

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This period ends at time T_1, when the voltage across C, $v_c(t)$, reduces to a value sufficient to cause D4 to become forward biased, V_{f4}. At this time, the energy in C will have transferred completely to the loop inductance and the combined gate capacitance of the power MOSFETs, which will subsequently continue to resonate at a lower frequency determined solely by the gate capacitance and loop inductance. Solving (6) allows an expression for T_1 to be found:

$$T_1 = \sqrt{\frac{C'_{loop}.C.L'_{loop}}{C+C'_{loop}}}\left(\pi - \cos^{-1}\left(\frac{CV+CV_{f4}+C'_{loop}V_{f4}}{C'_{loop}V}\right)\right) \quad (7)$$

The current in the HV wire loop at the end of step 1, I_{loop}, can be obtained by substituting (7) into (5), and scaling by the turns ratio of transformer T1. Similarly the voltage across the gate capacitances at the end of step 1, V_{gate1}, can be found by substituting (7) into (6).

Step 2: Energy transferred from loop inductance to gate capacitances

During the second resonant interval, the current in the HV wire loop reduces to zero. Simultaneously the power MOSFET gate voltages reach a maximum value, and are prevented from decaying by the diode D1. This completes the resonant energy transfer process. An equivalent circuit model for step 2 is shown in Fig. 4. As the final gate voltage is of interest, this equivalent circuit is referred to the secondary of T2.

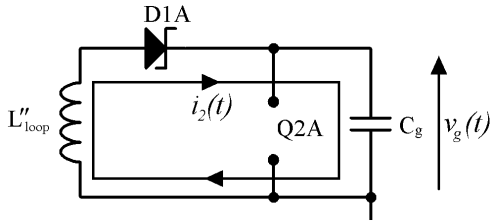

Fig. 4: Equivalent circuit for step 2 at turn-on, referred to the secondary of T2; 1 of N stages shown

The inductance L''_{loop} represents the portion of loop inductance referred to each secondary circuit, and may be found using the turns ratio of transformer T2:

$$L''_{loop} = \frac{{n_2}^2 L_{loop}}{N} \quad (8)$$

Solving the circuit in Fig. 4 and re-defining $t=0$ at the start of step 2 yields (9) and (10), which are second-order expressions describing gate current and voltage respectively. The initial conditions may be determined from the end of Step 1, i.e. solving (5) and (6) for $t=T_1$ and scaling by the turns ratio.

$$i_2(t) = \frac{I_{loop}}{n_2}\cos\left(\frac{t}{\sqrt{L''_{loop}C_g}}\right) - V_{gate1}\sqrt{\frac{C_g}{L''_{loop}}}\sin\left(\frac{t}{\sqrt{L''_{loop}C_g}}\right) \quad (9)$$

$$v_g(t) = \frac{I_{loop}}{n_2}\sqrt{\frac{L''_{loop}}{C_g}}\sin\left(\frac{t}{\sqrt{L''_{loop}C_g}}\right) + V_{gate1}\cos\left(\frac{t}{\sqrt{L''_{loop}C_g}}\right) \quad (10)$$

The duration of step 2, T_2, is found by solving (9) for $i_2(t)=0$:

$$T_2 = \sqrt{C_g L''_{loop}}\tan^{-1}\left(\frac{I_{loop}}{V_{gate1}n_2}\sqrt{\frac{L''_{loop}}{C_g}}\right) \quad (11)$$

Summing equations (7) and (11) allows the gate voltage rise-time, T_{on}, to be estimated:

$$T_{on} = T_1 + T_2 \quad (12)$$

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The final gate voltage, V_{gate2}, may be found by solving (10) for T_2. Combining the circuit equations for both stages allows analytical modelling of the whole turn-on transient. Simulation waveforms for the turn-on cycle using typical component values are illustrated in Fig. 5.

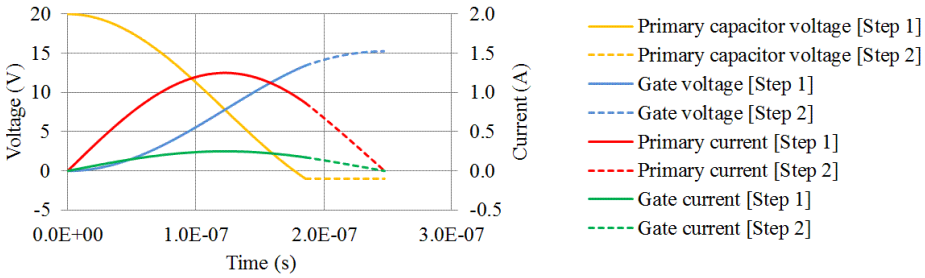

Fig. 5: Typical waveforms during the turn-on interval; N=6; C_g=3nF; V=20V; L_{loop}=50nH

Dynamic voltage balancing at turn-on due to non-linear "Miller" capacitance

In power MOSFETs, the parasitic "Miller" capacitance between the gate and the drain decreases as the drain-source voltage is increased. This effect may be exploited to achieve dynamic voltage sharing between MOSFETs if each device is driven with an identical gate current. The duration of the delay interval before the gate-source voltage has risen to the threshold voltage decreases with decreasing gate-drain ("Miller") capacitance and, therefore, with increasing drain-source voltage. Consequently, MOSFETs blocking a larger proportion of the overall voltage start to conduct first. During the following drain-source voltage transition, the rate of fall of drain-source voltage is dependent only upon the gate drive current and the instantaneous gate-drain capacitance, which is in turn dependent upon the instantaneous drain-source voltage. Devices supporting larger instantaneous drain-source voltage experience faster drain-source voltage decay, therefore equilibrium is rapidly reached where each device supports an identical fraction of overall voltage across the chain, even if the initial blocking voltages differ significantly. High-speed dynamic voltage sharing can therefore be achieved without requiring current from the high voltage path, if an equal gate current condition is enforced.

In the proposed gate driver circuit, each secondary transformer T2 has an identical turns ratio and is driven with the same loop current. T2 acts as a current transformer throughout the resonant cycle, enforcing an equal gate current profile irrespective of instantaneous gate voltage. This leads to an inherent condition of dynamic voltage balance in the power MOSFET chain during the turn-on cycle.

Turn-off transition

At turn-off, Q3 conducts. Capacitor C re-charges through the primary winding of T1, causing current to be delivered to the gates of Q2 through diodes D2. The channel of Q2 starts to conduct, rapidly turning off the stack of power MOSFETs Q1. Drain voltage is subsequently re-applied as the opposing inverter leg turns on. During this time each power MOSFET conducts an equal current, and hence the voltage across the stack is divided between the power MOSFETs in inverse proportion to their drain-source capacitances. This is only valid for resistive and capacitive inverter loads, where the reverse recovery characteristic of the intrinsic body-drain diode may be neglected.

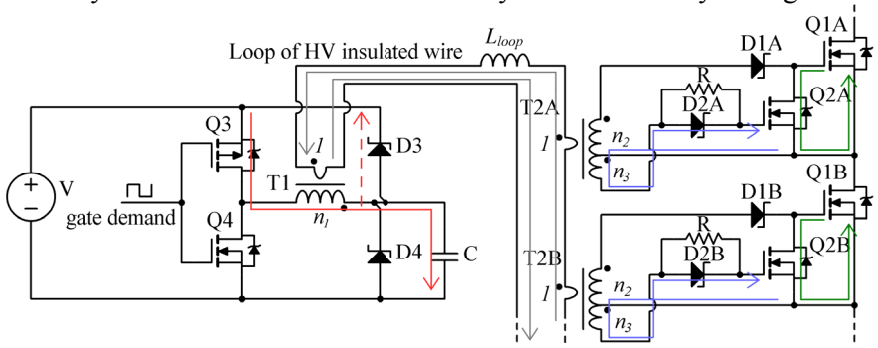

Fig. 6: Current paths during turn-off interval

During the turn-off interval, the parasitic loop inductance resonates with the primary capacitor, C, and the effective referred gate capacitances of Q2. Similar to the turn-on cycle, this may be analysed in two stages depending on whether D3 is forward biased, using second-order differential equations. The frequency of oscillation is usually higher in comparison to the turn-on transient as the gate capacitance of Q2 is typically lower than the gate capacitance of Q1.

Detailed analysis of the turn-off cycle is not necessary in determining gate drive behavior, as the power MOSFET gate voltage is actively clamped by Q2 for the duration of the turn-off resonance. For this reason the turn-off transition has no influence on component selection, other than the requirement to provide enough auxiliary turns, n_3, to successfully drive the gate of Q2. Resistor R is chosen to prolong the conduction of Q2 until after the inverter dead-time has elapsed, thus preventing dV/dt induced turn-on as voltage is re-applied. This arrangement is suitable for inverter applications with a short period of under-lap.

Design Procedure

Circuit layout considerations and loop inductance

It is generally desirable to minimize the physical size of the gate driver circuit and the parasitic inductance L_{loop}, whilst maintaining the required clearance distances to support the high off-state voltages present within the circuit. This implies minimization of the number of turns required in the transformer windings. Conveniently the series arrangement of power MOSFETs lends itself to a linear layout where the potential gradient in the off-state is evenly distributed along the length of a circuit board. This enables a relatively compact circuit layout and low loop inductance to be achieved.

The suggested design process starts by selecting suitable power MOSFETs, typically chosen to achieve the lowest overall cost for the required voltage rating. Cooling of the power MOSFETs can be challenging, as conventional earthed metal heatsinks often cannot be used whilst maintaining the required isolation strength. This situation is typically resolved by choosing MOSFETs with a lower on-state resistance than would otherwise be required for a given inverter current rating, and by potting the circuit in an insulating compound of high thermal conductivity such as epoxy resin. Potting also helps to minimize partial discharge and exclude moisture.

The size of the transformers should be considered carefully at the outset. The toroidal ferrite cores must be capable of accommodating a single turn of HV wire insulated to greater than the maximum rail voltage, in addition to several turns of thin enamelled wire for the other windings. This necessitates the use of a much larger toroid than would otherwise be required to transmit the gate energy, and the core flux density is therefore typically very low. Though this results in a higher component cost, the lower peak flux density improves gate driver efficiency for a given core material.

Once suitable MOSFETs and transformer cores have been chosen, a circuit board layout can be designed. Care should be taken to ensure the breakdown strength of the insulation medium is not exceeded at any location. Loop inductance may be estimated by approximating the HV wire as a rectangular single-turn coil, of length a, and width b metres. Formulae exist for approximating the self-inductance of this structure [11]. A typical inductance for the HV wire loop is between 100nH and 500nH, based on a typical loop area of between 5cm^2 and 25cm^2 for a 5kV inverter.

Primary capacitor selection

At turn-on, the energy in the primary capacitor C is delivered to the combined gate capacitances of the power MOSFETs. C must therefore be sized such that it is capable of storing greater than the total gate energy when charged to the primary voltage V, to account for circuit losses.

$$C > \frac{NC_g{V_{gate}}^2}{V^2} \tag{13}$$

The penalty for using a larger value of primary capacitor is increased loss at turn-off, as the primary capacitor re-charges. With the minimum value calculated from (13) as a starting point, C may be increased experimentally until the desired gate voltage is achieved on the power MOSFETs.

Designing the transformer T2

The number of secondary windings on T2 is selected to achieve a trade-off between the gate voltage rise-time and the circuit efficiency, by changing the resonant frequency of the circuit. For low values of n_2, the peak current in the primary and secondary circuits is increased and the gate voltage rise-time is reduced. The final gate voltage is determined only by the total stored energy, and is therefore largely independent of the overall transformer turns ratio.

Choosing the number of transformer windings is an iterative process. As a suggested starting point the target rise-time for the gate voltage, T_{rise}, may be specified. Assuming a similar resonant frequency during the first and second turn-on stages, the target rise-time may be equated with half the resonant period of the second time interval given by (10), i.e.:

$$\boldsymbol{T_{rise} = \pi\sqrt{L''_{loop}C_g}} \tag{14}$$

Substituting (8) into (14) and re-arranging yields a first estimate for n_2:

$$\boldsymbol{n_2 = \frac{T_{rise}}{\pi}\sqrt{\frac{N}{L_{loop}C_g}}} \tag{15}$$

Following testing, n_2 may be adjusted to vary the gate drive current in the inverter leg. This may be useful for meeting EMC requirements or improving efficiency. Dynamic voltage sharing requires that all gate drive transformers T2 have an equal number of secondary turns.

If the turn-off transformer Q2 requires an on-state voltage V_{q2}, the number of auxiliary windings, n_3, is chosen such that:

$$\boldsymbol{n_3 \geq \frac{Nn_1V_{q2}}{V}} \tag{16}$$

Designing the transformer T1

The number of primary windings, n_1, determines the ratio of the primary capacitance C and the referred lumped gate capacitance C'_{loop} (Fig. 3). It is desirable that C'_{loop} should be minimised, as this results in a lower peak current in the HV wire loop and closer matching between the resonant frequency of the two stages. However, C should not exceed C'_{loop}, to ensure that C may fully discharge during the first resonant stage. Applying this constraint leads to the inequality:

$$\boldsymbol{n_1 \leq \sqrt{\frac{n_2^2C_g}{NC}}} \tag{17}$$

Experimentation suggests that the number of primary turns is not critical, and rounding down the result of (17) to the nearest whole number has been found to produce acceptable results.

Selecting semiconductor components

Lastly, the small power semiconductor devices may be selected. This choice is informed by the peak voltages and currents in the primary and secondary circuits, which may be inferred by analytical modelling of the turn-on transient.

Design Example

A 6-stage 5kV driver was designed, using six STP2NK90Z-1 900V MOSFETs per leg. 900V devices represent the optimum trade-off between inverter voltage rating and component cost at current technology, for rated current up to 100mA. An equivalent gate capacitance of 2nF was estimated using the MOSFET datasheet parameters.

A circuit layout was chosen, based upon a clearance distance of 3mm/kV in air. TX13/7.5/5-3C90 ferrite cores were selected to accommodate the 4mm diameter of the HV wire. The wire loop measured approximately 20mm by 80mm, with an estimated loop inductance of 320nH. Choosing a target on-state gate voltage of 12V and a primary rail voltage of 20V required a minimum capacitance of 4.32nF according to (13). This was rounded to the next preferred value of 4.7nF.

Targeting a gate voltage rise-time of 500ns resulted in a secondary turns ratio of 1:25. Using equation (17) yields n_1= 5 turns. Aiming for a 5V peak gate voltage for turn-off MOSFET Q2, the minimum number of auxiliary turns n_3 was calculated to be 8 using (16).

Experimental Results

Prototype construction

The proposed gate driver circuit with the specifications given in the design example was built and tested. A simplified circuit diagram for the 5kV prototype is shown in Fig. 7. Two gate drivers were built on the same board in a half-bridge inverter leg arrangement, as shown in Fig. 8.

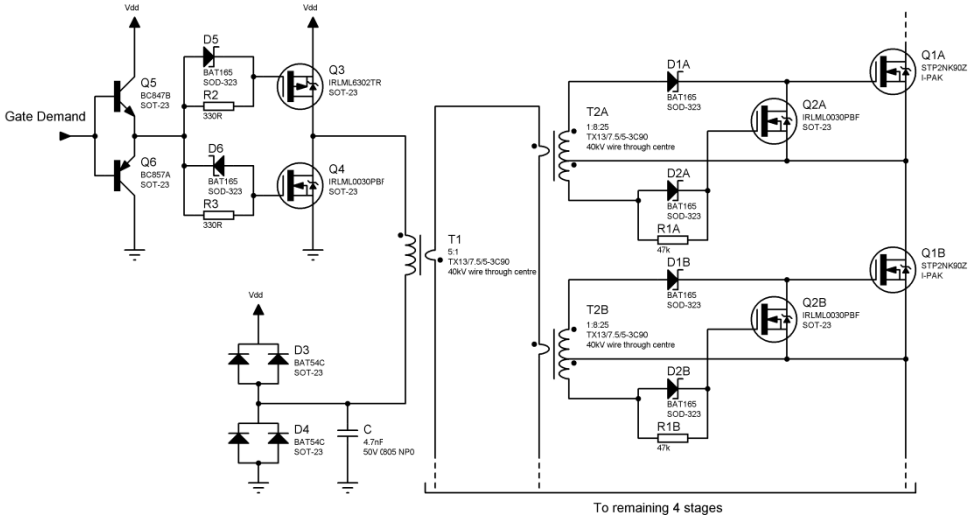

Fig. 7: Prototype circuit diagram; 2 of 6 stages shown; dead-time circuitry not shown

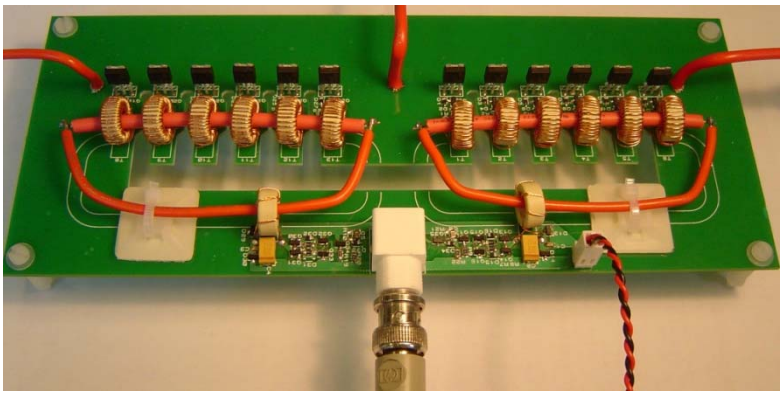

Fig. 8: 5kV Half-bridge inverter prototype

Gate driver circuit

The gate driver circuit was thoroughly tested before power was applied to the HV inverter leg. The measured waveforms were compared with those predicted by analytical modeling as shown in Fig. 9. Peak gate voltage was slightly lower than the expected 12V, at 10.5V peak. This discrepancy is attributed to loss in the resonant circuit, which is neglected in the analysis of the turn-on transient. It is noted that the resistance in the HV wire loop may cause significant voltage drop due to the relatively high current induced in the single turn. Furthermore, it has been assumed that the drain voltage of Q4 falls instantaneously whereas in the prototype this takes approximately 60ns.

The measured gate voltage rise-time is significantly less than the time predicted through analytical modeling, which is due to a higher resonant frequency. Either the effective gate input capacitance or the loop inductance, or both, are lower than approximated. This results in greater current for a shorter time to deliver the required gate charge.

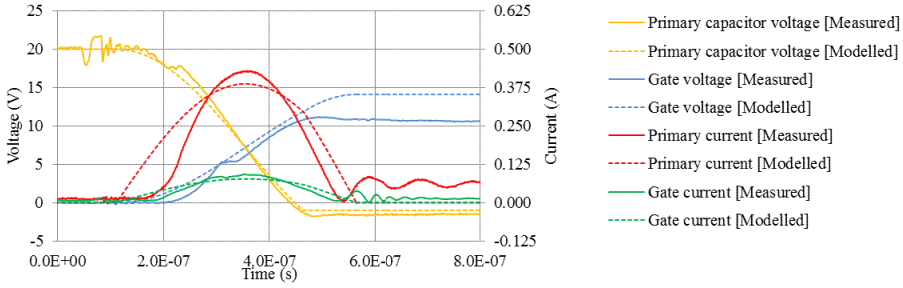

Fig. 9: Predicted and measured gate driver waveforms for 5kV prototype

Dynamic voltage balance in 5kV half-bridge inverter

Measurements of the voltage on the drain of each MOSFET show dynamic voltage balancing is possible using the proposed technique. Fig. 10 illustrates drain voltage measurements of an unloaded inverter at turn-off, taken using a high voltage AC-coupled probe. The output voltage fall-time is approximately 75ns and simultaneous switching of all devices is evident. Fig. 11 graphs the drain-source voltage of each MOSFET, inferred from Fig. 10 by subtraction. A significant error is introduced by the limitations of the measurement apparatus, though it is apparent that the MOSFETs initially supporting the highest voltage in the off-state begin to conduct first. Importantly, the voltage across these devices never rises above the initial value blocked in the off-state, preventing an avalanche condition. Devices initially supporting less voltage begin conducting up to 20ns later, and the voltage across these devices is seen to initially rise to equalise MOSFET voltage stresses.

In the steady off-state, individual MOSFETs within the inverter leg block differing voltages due to mismatch of device capacitance and off-state resistance. Though this is found not to cause device failure, some devices block a voltage greater than the 900V rating and therefore individual devices operate outside the manufacturer-specified SOA. This limitation may be avoided by the addition of external avalanche, TVS or Zener diode clamps in parallel with each device.

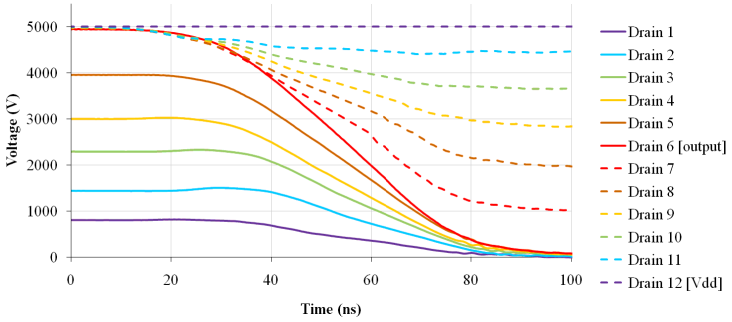

Fig. 10: Measured voltage at MOSFET drain terminals during the turn-off transient

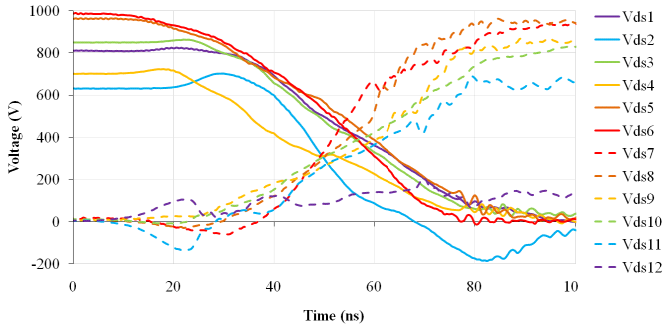

Fig. 11: Inferred MOSFET drain-source voltage during the turn-off transient

Conclusion

A novel resonant gate driver circuit is presented that uses a loop of HV wire to provide an isolated gate drive transformer. It is shown that the parasitic leakage inductance of this arrangement may be advantageously exploited as a resonant element in a gate driver circuit. A 5kV half-bridge inverter prototype that uses 900V MOSFETs has been demonstrated, for capacitive and resistive loads. Measured waveforms have provided good agreement with those predicted by theory. Individual devices exceed the SOA in the off-state due to device mismatch, though this process has been found to be non-destructive and may be avoided by adding diode clamps. Dynamic voltage balancing has been demonstrated at 5kV with a 75ns switching time, comparable to that of a single device.

References

[1] Grbovic P.: High-voltage auxiliary power supply using series-connected MOSFETs and floating self-driving technique, IEEE Transactions on Industrial Electronics Vol. 56 no 5, pp. 1446- 1455

[2] Robinson F and Hamidi V.: Series connecting devices for high-voltage power conversion, UPEC 2007, pp. 1205- 1210

[3] van Wesenbeeck M. et.al.: A multiple-switch high-voltage dc-dc converter, IEEE Transactions on Industrial Electronics Vol. 44 no 6, pp. 780- 787

[4] Baek J. et.al.: High voltage switch using series-connected IGBTs with simple auxiliary circuit, Record of the 2000 IEEE Industry Applications Conference Vol. 4, pp. 2237 –2242

[5] Abbate C. et.al.: High-voltage, high-performance switch using series-connected IGBTs, IEEE Transactions on Power Electronics, Vol. 25 no 9, pp. 2450- 2459

[6] Galluzzo, A. et.al.: Snubberless balancement of series connected insulated gate devices by a novel gate control strategy, Record of the Thirty-Second IEEE Industry Applications Conference Vol. 2, pp. 968- 974

[7] Palmer P. and A. Githiari A.: The series connection of IGBTs with active voltage sharing, IEEE Transactions on Power Electronics Vol. 12 no 4, pp. 637- 644

[8] Hess H. and R. Baker R.: Transformerless capacitive coupling of gate signals for series operation of power MOS devices, Proc. International Conference on Electric Machines and Drives 1999 pp. 673- 675

[9] Mentze E.J. et.al.: A scalable high-voltage output driver for low-voltage CMOS technologies, IEEE Transactions on Very Large Scale Integration (VLSI) Systems Vol. 14 no 12, pp. 1347- 1353

[10] Brehaut S. and Costa F.: Gate driving of high power IGBT through a double galvanic insulation transformer, 32nd Annual IEEE Conference on Industrial Electronics 2006, pp. 2505- 2510

[11] Terman F.: Radio Engineer's Handbook, McGraw-Hill, 1943