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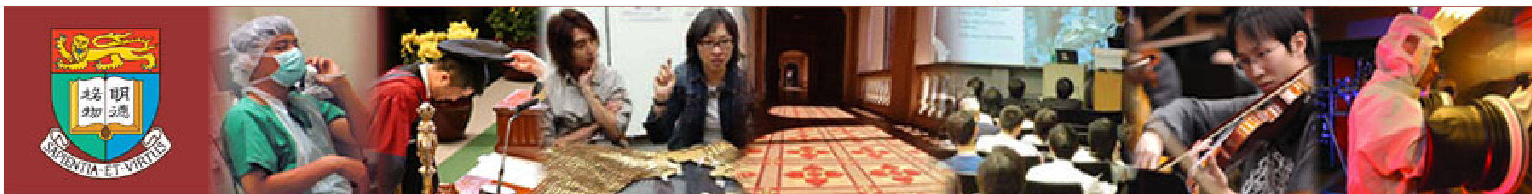

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Nb-doped Gd_2O_3 as charge-trapping layer for nonvolatile memory applications

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The charge-trapping properties of Gd_2O_3 with different Nb doping levels are investigated using an $Al/Al_2O_3/Gd_2O_3/SiO_2/Si$ structure. Compared with the memory device with pure Gd_2O_3, the one with lightly Nb-doped Gd_2O_3 shows better charge-trapping characteristics, including higher programming speed (6.5 V at +12 V programming voltage for 10 ms) and better retention property (92% retained charge at 85 °C after 10^4 s), due to its higher trapping efficiency that resulted from higher trap density and suppressed formation of a silicate interlayer at the Gd_2O_3/SiO_2 interface induced by the Nb doping. Moreover, the one with heavily Nb-doped Gd_2O_3 shows improvement in erasing behavior but worse retention and lower programming speed than the one with lightly Nb-doped Gd_2O_3. Further analysis reveals that the Nb-doping level determines the type of dominant trap in the Nb-doped Gd_2O_3, thus leading to different charge-loss mechanisms and charge-trapping characteristics. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4934183]

Floating-gate nonvolatile memories are approaching the scaling limit due to the difficulties in maintaining high gate coupling ratio and suppressing crosstalk between neighboring cells. Metal-oxide-nitride-oxide-silicon (MONOS)-type flash memories show stronger scaling ability and higher reliability than their floating-gate type counterpart because of their discrete charge-trapping nature. Si_3N_4 was the first dielectric as charge-trapping material for the MONOS devices. However, Si_3N_4 shows shortages including small conduction-band offset relative to SiO_2 and low k value ($k \sim 7$), which lead to poor retention and low operating speed. To overcome the shortages, researchers have been investigating suitable high-k dielectrics to substitute Si_3N_4. Among various high-k dielectrics, Gd_2O_3 seems to be a promising candidate with good retention property.[1,2] However, the k value of Gd_2O_3 is relatively low ($k \sim 14$).[2] In addition, Gd_2O_3 is known to easily react with the SiO_2 tunneling oxide to form undesirable low-k silicate.[3–5] This silicate interlayer is of much worse quality with more defects than the thermal SiO_2 and thus degrades the data retention. On the other hand, Nb oxide has a much higher k value ($k \sim 40$),[6] and therefore, it is an efficient way to increase the k value of Gd_2O_3 by Nb doping. Moreover, Nb oxide has good thermal stability, and therefore, Nb doping in Gd_2O_3 is expected to suppress the interfacial reaction with the SiO_2 tunneling oxide. Therefore, in this work, based on MONOS capacitors, the charge-trapping characteristics of Gd_2O_3 with different Nb doping levels are studied.

MONOS capacitors were fabricated on p-type silicon substrate. After the standard RCA (Radio Corporation of America) cleaning, a 2.5-nm SiO_2 tunneling layer (TL) was grown on the substrate by thermal dry oxidation at 900 °C. Then, Gd_2O_3 with different Nb contents was deposited on the wafer by co-sputtering Gd and Nb targets in a mixed ambient ($Ar/O_2 = 8/1$) to form the charge-trapping layer (CTL). The power of Gd was fixed at 40 W, while the power of Nb was set as 0 W, 15 W, and 30 W to make samples with various Nb contents, and denoted as the GO, LN-GO, and HN-GO samples, respectively. Following that, a 15-nm Al_2O_3 blocking layer (BL) was deposited by atomic layer deposition using $Al(CH_3)_3$ and H_2O as precursors at 300 °C. Then, all the samples received post-deposition annealing (PDA) at 900 °C in N_2 for 30 s. This PDA was used to imitate the thermal budget for activating the source and drain of memory transistors. Subsequently, Al was evaporated and patterned as electrodes. Finally, the samples received a forming-gas annealing for 20 min at 350 °C to improve the electrical contact between the electrode and the BL. The physical properties of the dielectric films were characterized by transmission electron microscopy (TEM) and secondary ion mass spectroscopy (SIMS). The electrical characteristics of the memory devices were measured by an HP4284A LCR meter and an HP4156A semiconductor parameter analyzer.

Fig. 1 shows the cross-sectional TEM images of the MONOS capacitors after going through all the processing steps. It is clear that an interlayer forms at the CTL/SiO_2

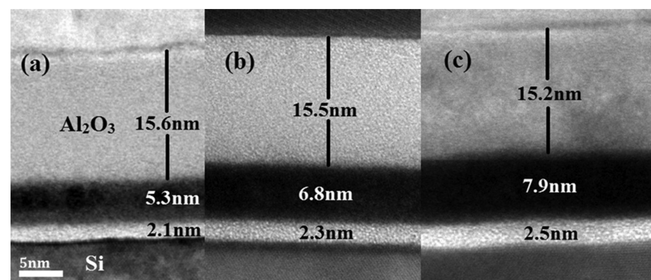

FIG. 1. Cross-sectional TEM images of (a) the GO, (b) the LN-GO, and (c) the HN-GO samples (all with the same scale).

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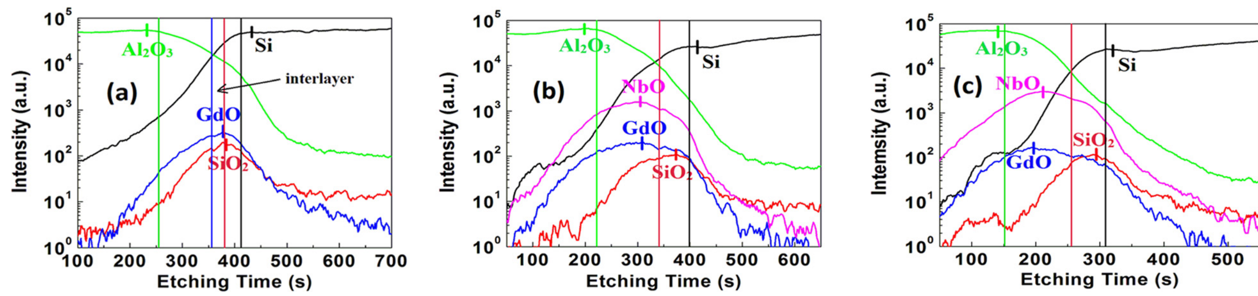

FIG. 2. SIMS depth profiles of (a) the GO, (b) the LN-GO, and (c) the HN-GO samples.

interface in the GO sample but does not form in the two Nb-containing samples. Moreover, the TL of the GO sample becomes thinner than those of the LN-GO and HN-GO ones. The above phenomena are mainly because Gd diffuses into the SiO_2 TL and forms a low-quality interlayer at the CTL/TL interface of the GO sample by chemical reaction,[3–5] which is undesirable for memory devices because the defects associated with the interlayer would degrade the data retention. The absence of the interlayer in the LN-GO and HN-GO samples indicates that Nb doping is an effective way to suppress the Gd diffusion into SiO_2 and thus contributes to an abrupt CTL/TL interface with few defects. Furthermore, there is a transition layer at the CTL/BL interface for the HN-GO sample compared with the LN-GO one. This suggests that heavy Nb doping in Gd_2O_3 increases the diffusion of Gd into the Al_2O_3 BL. These observations are consistent with the SIMS results in Fig. 2. The Nb/Gd atomic ratio for the LN-GO and HN-GO samples is determined as 4.0 and 7.0, respectively, by the Energy-dispersive X-ray Spectroscopy (EDX) method. Moreover, Metal-nitride-oxide-silicon (MNOS) devices have been prepared to obtain the band offset of Nb-doped Gd_2O_3 relative to SiO_2 by measuring their current vs applied voltage and the band offset is extracted to be 1.7 eV and 1.6 eV for the LN-GO and HN-GO samples, respectively, both larger than that of Gd_2O_3 (1.2 eV).

Fig. 2 shows the SIMS depth profile of the samples after going through all the processing steps. In Fig. 2(a), the Gd content peak nearly overlaps with the peak of SiO_2, suggesting that Gd diffuses significantly into the TL of the GO sample. In Figs. 2(b) and 2(c), the peaks of Gd and Nb are far away from the peak of SiO_2 due to the suppressed Gd diffusion by the Nb doping, indicating a high-quality CTL/TL interface with a negligible interlayer. Another interesting point is that the HN-GO sample shows a Gd peak closer to the Al_2O_3 peak in comparison with the LN-GO sample. This is consistent with the result in Fig. 1 and suggests a poor CTL/BL interface in the HN-GO sample.

Fig. 3 shows the 1-MHz C-V hysteresis characteristics of the MONOS capacitors at a sweeping voltage of $\pm$10 V. The sweep starts from the inversion region to the accumulation region, and back to the inversion region. The *k* value of the CTL for the GO, LN-GO, and HN-GO samples is calculated to be 5.4, 19.0, and 12.8, respectively. The Nb doped in Gd_2O_3 greatly increases the *k* value, but excessive Nb doping deteriorates the *k* value mainly due to higher leakage induced by Nb-related traps. The initial flatband voltage V_{FB} is -0.8 V, -0.7 V, and -0.7 V for the GO, LN-GO, and HN-GO samples, respectively. After the loop sweeping, the V_{FB} shifts from the initial value, and the final V_{FB} (open symbols in Fig. 3) is $+0.1$ V, $+1.8$ V, and -1.2 V for the GO, LN-GO, and HN-GO samples, respectively. For the GO and LN-GO samples, the reason for the positive shift is that some of the electrons stored in the CTL during the forward sweeping cannot escape during the reverse sweeping. The larger positive V_{FB} shift of the LN-GO sample indicates that light Nb doping induces electron traps in Gd_2O_3. Besides, the interlayer-free CTL/TL interface of the LN-GO sample also makes it more difficult for the trapped electrons to escape from the CTL because the high-quality interface with few defects suppresses trap-assisted electron emission. Due to the residual electrons in the CTL, the memory window of the LN-GO sample is similar to that of the GO sample. In contrast, the HN-GO sample shows a significant negative V_{FB} shift. One reason should be that the heavy Nb doping induces hole traps in addition to electron traps. It is also possible that hole traps induced by the Nb doping neutralize the electron traps at the TL/CTL interface. In order to gain deeper insight on the opposite V_{FB} shift between the LN-GO and HN-GO samples, a group of devices with the same Nb-doping level but different CTL thicknesses is also fabricated. For the LN-GO sample, the V_{FB} shift under forward sweeping increases (from $+3.7$ V to $+4.0$ V to $+4.9$ V) with increasing CTL thickness (from 3.4 nm to 6.8 nm to 13.6 nm), suggesting that the electron traps located in the CTL bulk rather than at the TL/CTL interface play the dominant role in the memory window and so light Nb doping induces electron traps. For the HN-GO sample, the negative V_{FB} shift under the reverse sweeping increases (from $+0.15$ V to -0.5 V to -1.2 V) with increasing CTL thickness (from 4.0 nm to 7.9 nm to 15.8 nm), which suggests that heavy Nb doping induces hole traps in the

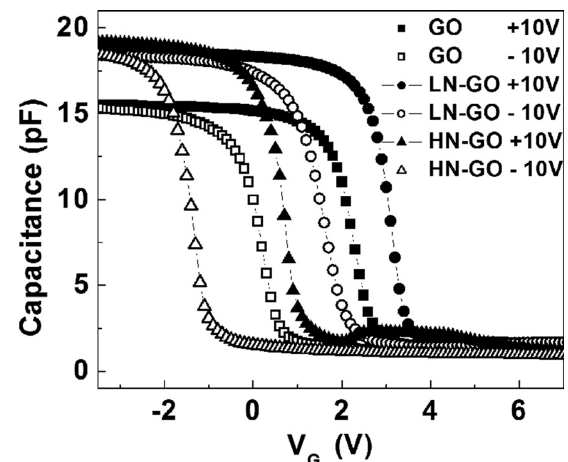

FIG. 3. C-V hysteresis curves of the MONOS samples.

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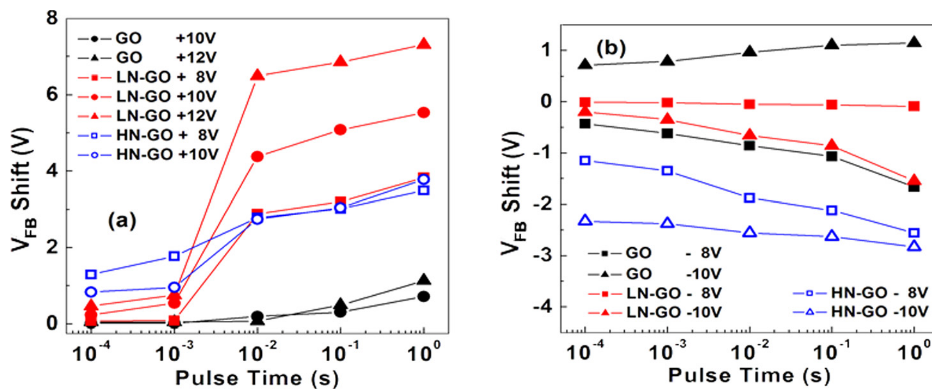

FIG. 4. (a) Program and (b) erase transient characteristics of the MONOS samples.

CTL bulk. Therefore, it can be concluded that the negative V_{FB} shift is due to numerous hole traps in the CTL, leading to recombination of electrons and holes and further hole injection during the reverse sweeping. Moreover, the HN-GO sample shows a considerable window of 2.1 V, indicating that electron traps coexist with hole traps in the CTL. The above viewpoint can be further supported by the program/erase (P/E) characteristics of the MONOS capacitors (shown in Fig. 4).

Fig. 4 shows the P/E transient characteristics of the MONOS capacitors. In Fig. 4(a), both the LN-GO and HN-GO samples display a much larger V_{FB} shift than the GO one under the same program conditions, indicating that Nb doping in Gd_2O_3 induces electron traps and thus results in higher programming speed. In addition, the V_{FB} shift of the HN-GO sample tends to saturate with increasing pulse time at a gate voltage of 10 V. However, the V_{FB} shift of the LN-GO sample increases with both gate voltage and time without a saturation phenomenon. The reason is that the dominant trap type induced by Nb doping is different for the two samples due to different Nb contents. Light Nb doping induces electron traps in the LN-GO sample while heavy Nb doping produces both electron and hole traps in the HN-GO sample. This can also be supported by the erasing characteristics of the two Nb-doped samples shown in Fig. 4(b). The HN-GO sample shows a much larger V_{FB} shift than the LN-GO one under the same erasing conditions, which is caused by the hole traps in the HN-GO sample. For the HN-GO sample, hole traps partially annihilate the effect of electron traps, and therefore the program V_{FB} shift saturates at 10 V and the erase speed is considerably higher. In contrast, for the LN-GO sample, the major traps are electron traps, and so, it has high electron-trapping efficiency and thus high programming speed, but low erasing speed due to a shortage of hole traps. The above phenomenon is consistent with the memory window shown in Fig. 3. The charge-trap density (Nt) can be estimated by the method in Refs. 7 and 8. The extracted Nt for the LN-GO sample is $1.5 \times 10^{13}\,cm^{-2}$, which is much higher than that of the GO sample ($2.3 \times 10^{12}\,cm^{-2}$) and the HN-GO sample ($9.5 \times 10^{12}\,cm^{-2}$). Another phenomenon worth mentioning in Fig. 4(b) is that the abnormal positive V_{FB} shift takes place at a gate voltage of -10 V for the GO sample but does not exist for the two Nb-doped ones. This positive V_{FB} shift during the erasing operation is a result of undesirable electron tunneling from the gate to the CTL via the BL, which is called erase saturation.[9] It indicates that the GO sample has a low-quality CTL/BL interface, which can be improved by the Nb doping, as demonstrated in Fig. 1(a).

Furthermore, in Fig. 4(a), the program transient of the LN-GO sample jumps as the pulse time increases from 1 ms to 10 ms. This is due to the bulk electron traps in the LN-GO sample. Since the electrons travel a longer distance to get into the bulk, it takes the electrons from the substrate a relatively long time to be trapped in those bulk traps during programming.

Fig. 5 shows the retention characteristics of the MONOS samples prepared at 10 V for 1 s. In Fig. 5(a), the

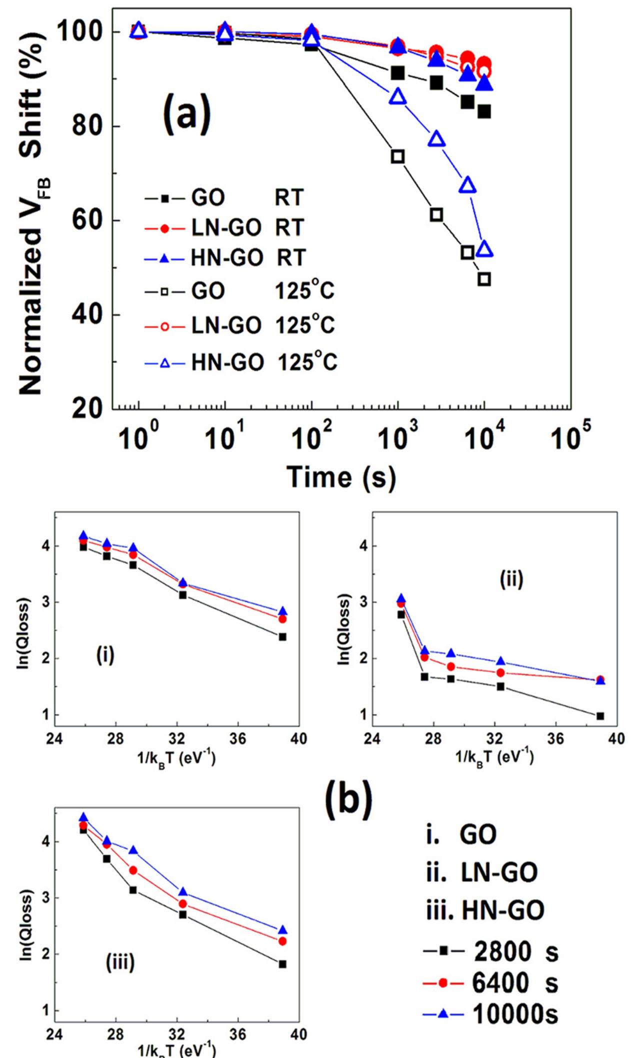

FIG. 5. (a) Retention characteristics of the GO, LN-GO, and LaNbO samples tested at 25 °C (RT) and 125 °C. (b) Arrhenius plot of the charge-loss characteristics for (i) the GO sample, (ii) the LN-GO sample, and (iii) the HN-GO sample from 25 °C to 175 °C.

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LN-GO sample shows the best retention property (93% charge remained at room temperature after 10^4 s) among the three samples. Moreover, the good retention is hardly dependent on temperature (91% charge remained even at 125 °C after 10^4 s), indicating that lightly Nb-doped Gd_2O_3 is a promising charge-trapping (CT) material for high-temperature application. The HN-GO sample also shows good retention at room temperature, but degrades severely with increasing temperature. To gain better insight on the charge loss, the Arrhenius plot, which relates the charge loss with temperature, is shown in Fig. 5(b), where the activation energy E_A for each sample is extracted. The LN-GO sample shows the smallest charge loss under all temperature conditions, implying its abrupt CTL/TL and CTL/BL interfaces. Furthermore, it is clear that the curve exhibits a gentle slope (small E_A 0.047 eV) for the low-temperature range from 25 °C to 150 °C but a steep slope (large E_A 0.62 eV) for the high-temperature range from 150 °C to 175 °C. The small E_A suggests that the trap-to-band (T-B) tunneling mechanism dominates the charge loss at low temperature and is insensitive to temperature.[1,10,11] The large E_A suggests that the indirect charge-loss process is responsible for the charge loss, in which the trapped electrons are first excited thermally to the conduction band and then leak out from the CTL.[11–13] It is worth mentioning that the charge loss of the LN-GO sample remains small until 150 °C even though the TL is only 2.4 nm. The GO sample exhibits an intermediate E_A (0.12 eV) at all temperatures, suggesting that the T-B tunneling is still the dominant process while the indirect process has stronger effects when compared with the LN-GO sample. Besides the intermediate E_A, the large charge loss at low temperature (25 °C) is another big difference for the GO sample compared with the LN-GO sample, indicating its poor CTL/TL and CTL/BL interfaces with many defects for reducing the tunneling path and barrier height. The HN-GO sample exhibits the largest E_A (0.21 eV) under all temperature conditions except for a narrow high-temperature range, suggesting that thermal charge-loss mechanism plays an important role. Since the HN-GO sample has a better CTL/TL interface than the GO one (shown in Fig. 1), the HN-GO sample should exhibit a smaller E_A than the GO sample at low temperature based on the indirect charge-loss mechanism, but the fact is just the opposite. The reason is that the dominant charge-loss mechanism for the HN-GO sample at low temperature is different from that of the other two samples. Heavy Nb doping in Gd_2O_3 induces hole traps in the CTL besides electron traps, as supported by Figs. 3 and 4. As a result, instead of the indirect charge-loss process, electron-hole recombination contributes significantly to the charge loss in the HN-GO sample. As different from the indirect charge-loss mechanism, which requires the trapped charge to be excited first to the conduction band and thus suddenly exerts a huge effect above a certain temperature [shown in Fig. 5(b) (ii) for the LH-GO sample], the effect of electron-hole recombination grows stronger with temperature without any low-temperature limit because the probability of electron-hole recombination increases with thermal vibration intensity.[14–16]

In summary, the charge-trapping properties of Gd_2O_3 with different Nb doping levels have been investigated based on a MONOS capacitor. The memory device with lightly Nb-doped Gd_2O_3 as the CTL shows better characteristics than that with pure Gd_2O_3 in terms of higher programming speed and better data retention, which result from higher electron-trap density in the CTL and a better TL/CTL interface (both induced by the Nb doping). The memory device with heavily Nb-doped Gd_2O_3 shows further improvement in erasing behavior, but a smaller memory window and worse high-temperature retention due to hole traps generated by excessive Nb doping. Therefore, Gd_2O_3 with suitable Nb doping is a promising candidate as the CTL for high-performance nonvolatile memory applications.

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[1]X. D. Huang, J. K. O. Sin, and P. T. Lai, IEEE Trans. Nanotechnol. **12**, 157 (2013).
[2]J. Kwo, M. Hong, A. R. Kortan, K. L. Queeney, Y. J. Chabal, R. L. Opila, Jr., D. A. Muller, S. N. G. Chu, B. J. Sapjeta, T. S. Lay, J. P. Mannaerts, T. Boone, H. W. Krautter, J. J. Krajewski, A. M. Sergnt, and J. M. Rosamilia, J. Appl. Phys. **89**, 3920 (2001).
[3]H. D. B. Gottlob, A. Stefani, M. Schmidt, M. C. Lemme, H. Kurz, I. Z. Mitrovic, M. Werner, W. M. Davey, S. Hall, P. R. Chalker, K. Cherkaoui, P. K. Hurley, J. Piscator, O. Engström, and S. B. Newcomb, J. Vac. Sci. Technol., B **27**, 249 (2009).
[4]S. Jayanti, X. Yang, and D. J. Lichtenwalner, Appl. Phys. Lett. **96**, 092905 (2010).
[5]D. J. Lichtenwalner, J. S. Jur, A. I. Kingon, M. P. Agustin, Y. Yang, S. Stemmer, L. V. Goncharova, T. Gustafsson, and E. Garfunkel, J. Appl. Phys. **98**, 024314 (2005).
[6]D. C. Bharti and S. W. Rhee, Thin Solid Films **548**, 195 (2013).
[7]X. D. Huang, J. K. O. Sin, and P. T. Lai, IEEE Trans. Electron Devices **58**, 4235 (2011).
[8]T. H. Kim, I. H. Park, J. D. Lee, H. C. Shin, and B. G. Park, Appl. Phys. Lett. **89**, 063508 (2006).
[9]B. D. Salvo, C. Gerardi, R. V. Schaijk, S. A. Lombardo, D. Corso, C. Plantamura, S. Serafino, G. Ammendola, M. V. Duuren, P. Goarin, W. Y. Mei, K. V. D. Jeugd, T. Baron, M. GelyGely, P. Mur, and S. Deleonibus, IEEE Trans. Device Mater. Reliab. **4**, 377 (2004).
[10]S. E. Thompson and T. Nishida, J. Appl. Phys. **70**, 6864 (1991).
[11]Y. Wang and M. H. White, Solid-State Electron. **49**, 97 (2005).
[12]A. Arreghini, N. Akil, F. Driussi, D. Esseni, L. Selmi, and M. J. van Duuren, Solid-State Electron. **52**, 1460 (2008).
[13]X. D. Huang, J. K. O. Sin, and P. T. Lai, Solid-State Electron. **79**, 285 (2013).
[14]D. J. DiMaria, D. A. Buchanan, J. H. Stathis, and Ft. E. Stahlbusha, J. Appl. Phys. **77**, 2032 (1995).
[15]M. O'Neil, J. Marohn, and G. McLendon, J. Phys. Chem. **94**, 4356 (1990).
[16]K. Vanheusden, S. P. Karna, and R. D. Pugh, Appl. Phys. Lett. **72**, 28 (1998).

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