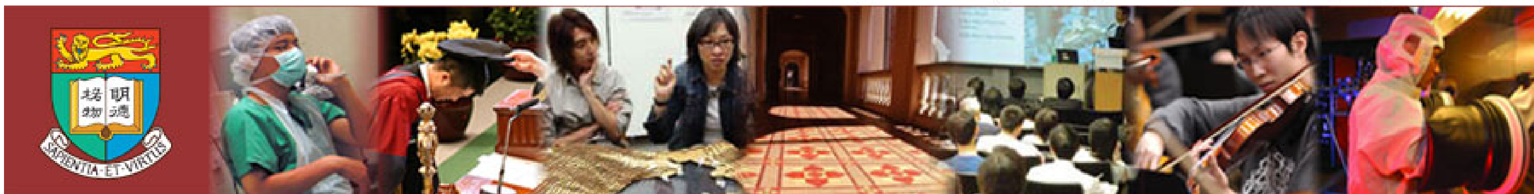
View metadata, citation and similar papers at core.ac.uk

brought to you by CORE

provided by HKU Scholars Hub



Title	**Passivation of Oxide Traps and Interface States in GaAs Metal-Oxide-Semiconductor Capacitor by LaTaON Passivation Layer and Fluorine Incorporation**
Author(s)	**LIU, L; Choi, HW; Xu, JP; Lai, PT**
Citation	**Applied Physics Letters, 2015, v. 107 n. 21, p. article no. 213501**
Issued Date	**2015**
URL	**http://hdl.handle.net/10722/231901**
Rights	**Applied Physics Letters. Copyright © American Institute of Physics.; Copyright (2015) American Institute of Physics. This article may be downloaded for personal use only. Any other use requires prior permission of the author and the American Institute of Physics. The following article appeared in (Applied Physics Letters, 2015, v. 107 n. 21, article no. 213501) and may be found at (http://dx.doi.org/10.1063/1.4936329).; This work is licensed under a Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 International License.**

APPLIED PHYSICS LETTERS 107, 213501 (2015)

Passivation of oxide traps and interface states in GaAs metal-oxide-semiconductor capacitor by LaTaON passivation layer and fluorine incorporation

L. N. Liu,[1] H. W. Choi,[1] J. P. Xu,[2] and P. T. Lai[1,a)]
[1]*Department of Electrical and Electronic Engineering, The University of Hong Kong, Pokfulam Road, Hong Kong*
[2]*School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan 430074, People's Republic of China*

(Received 2 October 2015; accepted 11 November 2015; published online 23 November 2015)

GaAs metal-oxide-semiconductor capacitor with TaYON/LaTaON gate-oxide stack and fluorine-plasma treatment is fabricated and compared with its counterparts without the LaTaON passivation interlayer or the fluorine treatment. Experimental results show that the sample exhibits better characteristics: low interface-state density ($8 \times 10^{11}\,cm^{-2}/eV$), small flatband voltage (0.69 V), good capacitance-voltage behavior, small frequency dispersion, and small gate leakage current ($6.35 \times 10^{-6}\,A/cm^2$ at $V_{fb} + 1\,V$). These should be attributed to the suppressed growth of unstable Ga and As oxides on the GaAs surface during gate-oxide annealing by the LaTaON interlayer and fluorine incorporation, and the passivating effects of fluorine atoms on the acceptor-like interface and near-interface traps. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4936329]

As one of the most promising channel materials to replace Si, III-V compound semiconductors have attracted much efforts in order to meet the requirements of higher-performance and lower-power applications in recent years.[1,2] GaAs Metal-Oxide-Semiconductor (MOS) device with high-k (dielectric constant) gate dielectric has received significant attention due to its larger bandgap and higher electron mobility than its Si counterpart.[3,4] Because of its relatively high k value (~26) and compatibility with the CMOS technology, Ta_2O_5 can be considered as a potential high-k material, especially in the DRAM.[5,6] However, it has been reported that Ta_2O_5 has relatively high leakage current and possibility of reacting with the underlying substrate at high temperature,[7,8] but doping Y to Ta_2O_5 can improve its dielectric properties by partially compensating the pre-existing oxygen vacancies in Ta_2O_5.[9] Furthermore, incorporating nitrogen in Ta_2O_5 is capable of increasing its k value and reducing its border traps.[10] Therefore, TaYON can be considered as a promising high-k gate dielectric.

However, it is well known that a large amount of defects near the valence band and the easily formed unstable native oxide of GaAs can cause Fermi-level pinning at the high-k/GaAs interface,[11] and therefore, passivating this interface is an essential factor to improve the performance of GaAs MOS devices. Various interlayers (e.g., Si, Ge, AlON, TaON) have been tried to passivate the GaAs surface, and good results have been obtained.[12,13] LaTaON has been proved to provide an excellent interface quality with Ge due to its good thermal stability and scalability,[14] and thus, it is expected to exhibit good interface performance with GaAs too. However, because of the hygroscopic nature of La-based material, LaTaON seems not suitable to be used as gate dielectric. Besides, fluorine incorporation was reported to be another good way for passivating the GaAs surface because it is capable of passivating the oxygen vacancies in high-k materials.[15] Therefore, in this work, GaAs MOS capacitor with TaYON/LaTaON gate-dielectric stack and fluorine-plasma treatment is proposed, and its electrical and interfacial characteristics are compared with those of samples without LaTaON passivation layer or fluorine-plasma treatment.

MOS capacitors were fabricated on Si-doped n-type GaAs wafers (100) with a doping concentration of 0.5–1.0 $\times 10^{18}\,cm^{-3}$. Wafers were first degreased in acetone, ethanol, and isopropanol, respectively, and then dipped in diluted HCl to remove the native oxide, followed by sulfur passivation by dipping in 8% $(NH_4)_2S$. After dried by N_2, the wafers were transferred immediately into the high vacuum chamber of sputtering system. A thin LaTaON film (~2 nm) was deposited by co-sputtering Ta and La_2O_3 targets at room temperature in $Ar/N_2 = 24/12$, followed by the deposition of TaYON gate dielectric layer (~8 nm) by co-sputtering Ta and Y_2O_3 targets also in $Ar/N_2 = 24/12$. Then, some of the samples received a fluorine-plasma treatment at a flow rate of $CHF_3/O_2 = 10/1$ for 5 min. For comparison, control samples without the passivation layer or fluorine-plasma treatment were prepared. So, the samples are divided into three groups: the sample with LaTaON passivation layer and fluorine-plasma treatment (denoted as LaTaON + F), the sample with LaTaON passivation layer but no fluorine-plasma treatment (denoted as LaTaON) and the control sample without LaTaON passivation layer or fluorine-plasma treatment. Subsequently, post-deposition annealing (PDA) was carried out at 600 °C for 60 s in N_2 for all the samples. Al electrode was then evaporated and patterned with an area of $7.85 \times 10^{-5}\,cm^2$, followed by a forming-gas (95% N_2 + 5% H_2) annealing at 300 °C for 20 min.

The capacitance-voltage (C-V) measurements were performed on MOS capacitors by HP 4284A. The gate leakage

a)Author to whom correspondence should be addressed. Electronic mail: laip@eee.hku.hk.

 © 2015 AIP Publishing LLC

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 147.8.31.43 On: Mon, 14 Nov 2016 07:56:16

current was tested by HP 4156A, and the thickness of the dielectric films (T_{ox}) was measured by ellipsometry.

The C-V curves at 1 MHz of the samples swept from inversion to accumulation and then backward are shown in Fig. 1. Compared with the control sample without passivation layer or fluorine treatment, smaller hysteresis can be found in both samples with LaTaON interlayer, especially for the one with fluorine treatment (LaTaON + F), implying that the defects in the dielectric and near/at the GaAs surface can be reduced by the LaTaON interlayer and fluorine further passivates the oxide defects. The slightly smaller accumulation capacitance (C_{ox}) for the LaTaON + F sample than the LaTaON sample should be caused by the high bonding energy between metal atom and incorporated F atom.[16] However, the smaller flat-band shift and C-V hysteresis of the LaTaON + F sample than those of the LaTaON sample indicate that the fluorine treatment can reduce the defects near/at the high-k/GaAs interface, which is beneficial to enhancing the carrier mobility (due to reduced defect-related carrier scattering), outweighing the slight loss in the k value.[17] The C-V curve of the control sample exhibits a stretch-out and C_{ox} reduction at higher gate voltage, implying poor interface quality due to the lack of passivation. Furthermore, the much smaller C_{ox} of the control sample than that of the other two samples should be attributed to the formation of a low-k native oxide (consisting of Ga-O and As-O complexes) at the GaAs surface,[18] which can be effectively suppressed by the LaTaON passivation layer, as shown by the TEM images in Fig. 2. Interface-state density near mid-gap D_{it} is extracted from the HF C-V curve by the Terman's method[19] for comparison (Fig. 1(b)). Obviously, the LaTaON + F and LaTaON samples exhibit smaller D_{it} than the control sample, with the smallest for the LaTaON + F sample ($\sim 8 \times 10^{11}\,\mathrm{cm^{-2}/eV}$), further demonstrating the passivation role of the LaTaON interlayer and F incorporation on the dangling bonds at the high-k/GaAs interface.

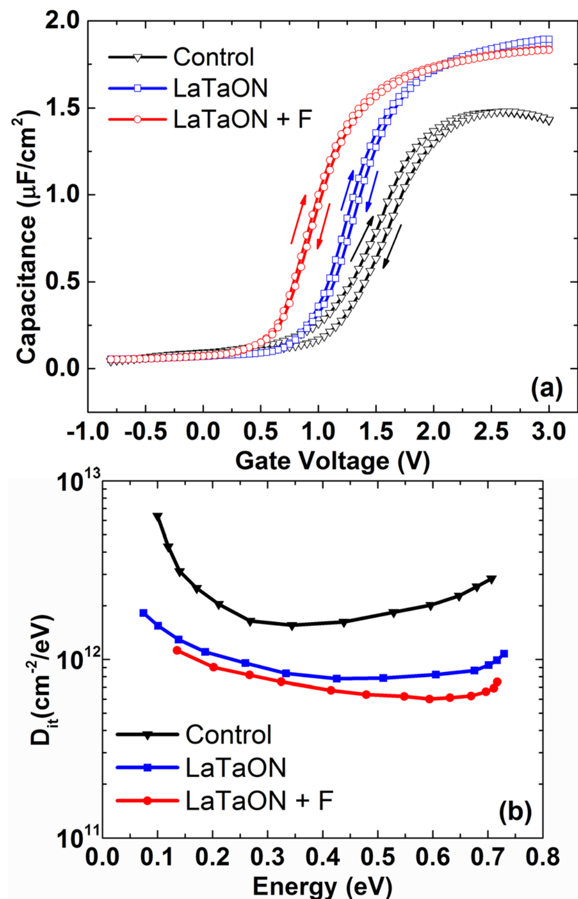


FIG. 1. (a) High-frequency C-V curve and (b) interface-state density (D_{it}) in the bandgap.

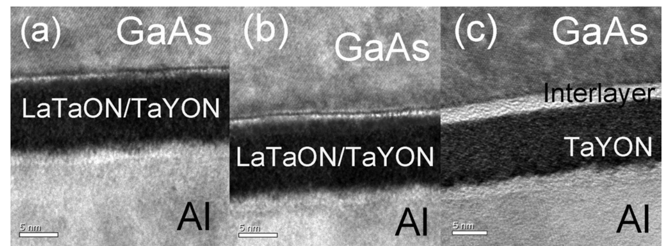


FIG. 2. The cross-sectional TEM images of the (a) LaTaON + F, (b) LaTaON, and (c) control samples.

The electrical and physical parameters of the samples extracted from their HF C-V curves are listed in Table I. The equivalent k value of the gate dielectric can be calculated as $k_{eq} = k_{SiO_2} T_{ox}/\mathrm{CET}$, where CET is the capacitance equivalent thickness equals to $k_0 k_{SiO_2}/C_{ox}$ (k_0 is the vacuum permittivity; k_{SiO_2} is the dielectric constant of SiO_2; and C_{ox} is the accumulation capacitance per unit area). Flatband voltage V_{fb} is determined from flatband capacitance, and thus, the equivalent oxide-charge density (Q_{ox}) can be obtained by $Q_{ox} = -C_{ox}(V_{fb} - \varphi_{ms})/q$, with φ_{ms} the work-function difference between Al gate and GaAs substrate, and q is the electron charge. As shown in Table I, the two samples with LaTaON passivation layer exhibit better electrical properties than the control sample. Positive V_{fb} for all the samples implies the presence of negative charges in the dielectric film. Smaller V_{fb} of the LaTaON + F sample (0.69 V) than the LaTaON sample (1.09 V) should be ascribed to the capability of fluorine incorporation in passivating the oxide traps and interface states,[20] which can be further supported by its smaller Q_{ox} ($-6.88 \times 10^{12}\,\mathrm{cm^{-2}}$) than that of the latter ($-1.17 \times 10^{13}\,\mathrm{cm^{-2}}$).

In Fig. 3, the control sample shows the largest gate leakage current density (e.g., $4.24 \times 10^{-4}\,\mathrm{A/cm^2}$ at gate voltage of V_{fb} + 1 V) and slight breakdown at gate voltages larger than 2.5 V in. This is consistent with the control sample having the most interface traps (Fig. 1(b)), which can cause trap-assisted tunneling of carriers: under a positive gate voltage, the conductive band of GaAs bends towards the Fermi level at the GaAs surface, and thus, electrons can tunnel from the

TABLE I. Electrical and physical parameters of the samples extracted from HF C-V curves.

Sample	LaTaON + F	LaTaON	Control
T_{ox} (nm)	10.3	10.6	10.9
C_{ox} (μF/cm^2)	1.84	1.87	1.48
V_{fb} (V)	0.69	1.09	1.26
Q_{ox} (cm^{-2})	-6.88×10^{12}	-1.17×10^{13}	-1.06×10^{13}
CET (nm)	1.86	1.85	2.35
k	21.5	22.5	18.1

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 147.8.31.43 On: Mon, 14 Nov 2016 07:56:16

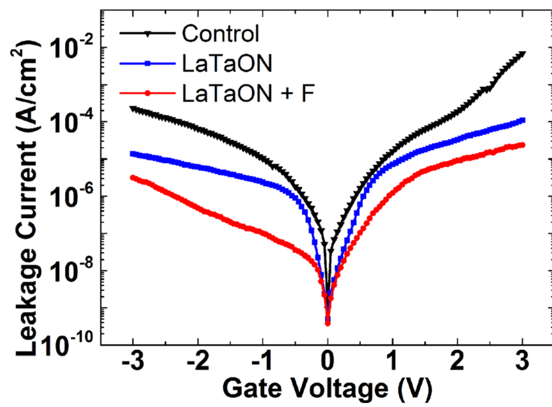


FIG. 3. Gate leakage current density vs. gate voltage (J_g-V_g) characteristics of the three samples.

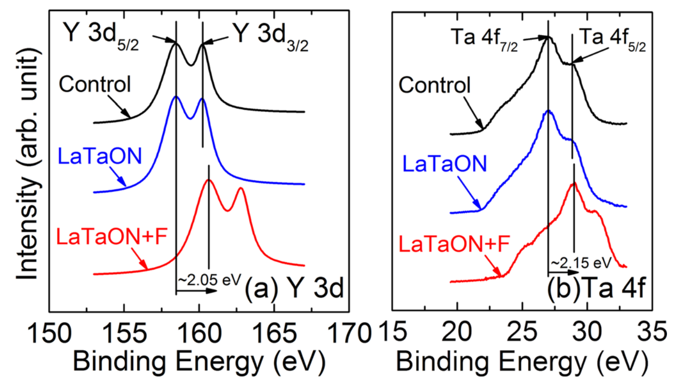


FIG. 5. (a) Y 3d and (b) Ta 4f XPS spectra at the TaYON dielectric layer of the samples.

substrate to the traps at the interface and in the dielectric and then to the gate, resulting in leakage current.[21,22] However, for the two samples with LaTaON interlayer, the leakage current density is obviously reduced, especially for the one with fluorination (6.35×10^{-6} A/cm^2 at V_{fb} + 1 V), which should be attributed to the reduced trap-assisted tunneling associated with its smallest Q_{ox} and D_{it}, as mentioned above.[23] Furthermore, C-V curves measured at 1 MHz, 100 kHz, and 50 kHz are displayed in Fig. 4. The large frequency-dependent flatband shift and the poor C-V behavior at low frequency for the control sample indicate obvious Fermi-level pinning at the high-k/GaAs interface.[24] Smaller frequency dispersion is obtained for the two samples with LaTaON passivation layer, especially for the fluorinated sample, demonstrating that slow states at/near the interface can be reduced by the LaTaON interlayer and the fluorine-plasma treatment can further improve the interface quality.

Chemical states in the dielectric layer and at/near the high-k/GaAs interface are analyzed by XPS to clarify the effects of the LaTaON passivation layer and fluorine treatment on the device's performance. Fig. 5 shows the Y 3d and Ta 4f spectra of the three samples. As compared to the LaTaON sample and control sample, the Y 3d and Ta 4f peaks of the LaTaON + F sample shift to higher energies of 2.05 eV and 2.15 eV, respectively, which should be due to the higher electronegativity of F (4.0) than that of O (3.5). Similarly, the La 3d peak in Fig. 6(a) of the LaTaON + F sample also shifts to higher energy relative to that of the LaTaON sample. The La atomic ratios of the LaTaON + F and the LaTaON samples are extracted to be 13.06% and

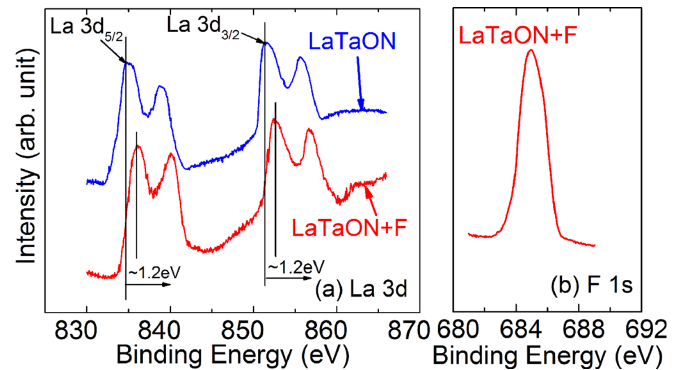


FIG. 6. (a) La 3d XPS spectrum at the LaTaON interlayer of the LaTaON + F and LaTaON samples; and (b) F 1s XPS spectrum of the LaTaON + F sample.

11.01%, respectively, possibly because the strong bonding between fluorine and metal atoms could suppresses the out-diffusion of the latter from the dielectric layer towards the substrate. The obvious F 1s peak in the F 1s spectrum of the LaTaON + F sample [Fig. 6(b)] indicates that fluorine is indeed incorporated in both the dielectric and passivation layers, resulting in effective passivation on the dangling bonds and oxide traps at/near the high-k/GaAs interface. This is why the LaTaON + F sample has the best interfacial and thus electrical properties, as shown in Table I.

Figs. 7 and 8 compare the As 3d and Ga 3d XPS spectra of the three samples. In Fig. 7, the As-Ga, As-As, As-S and As-O peaks are found at 40.9 eV, 41.7 eV, 42.6 eV, and 43.9 eV, respectively, and in Fig. 8, the Ga-As, Ga-S, Ga-O, and Ga-N peaks are located at 19.0 eV, 19.9 eV, 21.0 eV, and

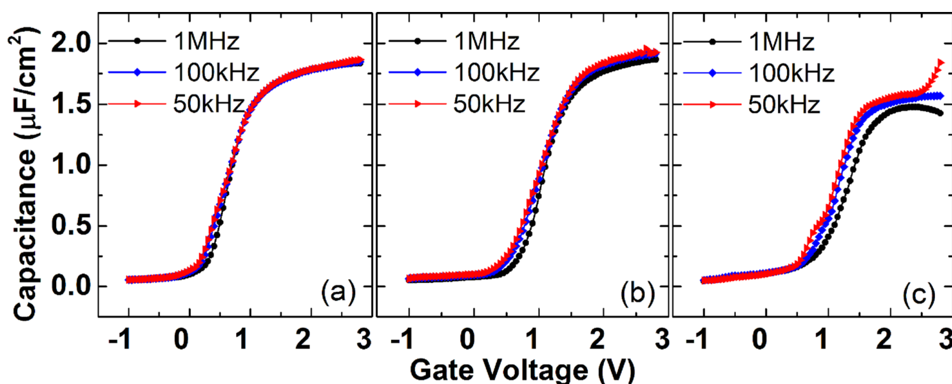


FIG. 4. Frequency dispersion of C-V curve: (a) $LaTaON_2$ + F sample, (b) LaTaON sample, and (c) control sample.

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 147.8.31.43 On: Mon, 14 Nov 2016 07:56:16

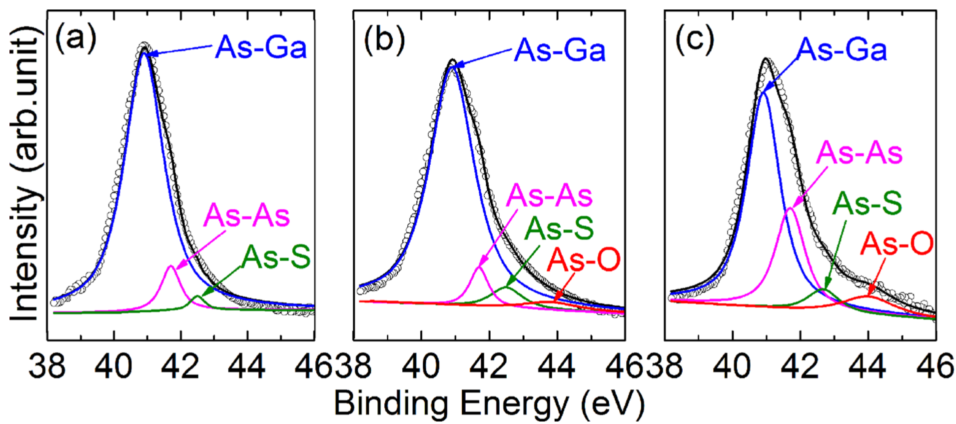


FIG. 7. As 3d XPS spectrum at/near the high-k/GaAs interface: (a) LaTaON + F sample, (b) LaTaON sample, and (c) control sample.

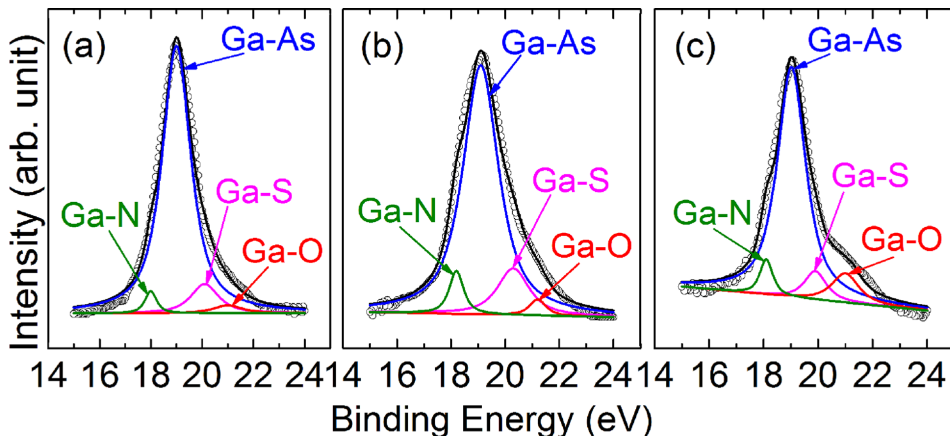


FIG. 8. Ga 3d XPS spectrum at/near the high-k/GaAs interface: (a) LaTaON + F sample, (b) LaTaON sample, and (c) control sample.

18.1 eV, respectively, according to the National Institute of Standards and Technology (NIST) XPS database. The As-S and Ga-S bonds detected in Figs. 7 and 8 imply that Ga_2S_3 and As_2S_3 have formed at the GaAs surface during the sulfur passivation, which can decrease the Ga/As-related vacancies by the reactions: $(NH_4)_2S + H_2O \rightarrow 2NH_4^+ + S^{2-} + H^+ + OH^-$ and $2GaAs + 12H^+ + 6S^{2-} \rightarrow Ga_2S_3 + As_2S_3 + 6H_2$.[25] The Ga-S bond can reduce the energy states in the band gap and suppressing the formation of native oxide on GaAs in subsequent thermal processing,[26] by only pushing the states from the lower half of the GaAs band gap to the upper half near the conduction band, but not fully eliminating them.[27] In Figs. 7 and 8, strongest As-O and Ga-O peaks are observed for the control sample, demonstrating the existence of significant amount of As/Ga-oxides at/near the interface, and thus explaining why it has the smallest C_{ox} and the lowest k value.

In addition, the intensities of As-As bond for the LaTaON + F and LaTaON samples in Figs. 7(a) and 7(b) are lower than that for the control sample in Fig. 7(c), implying that the LaTaON passivation layer can effectively reduce the weak As-O and As-As bonds. No As-O peak and weakest Ga-O peak for the LaTaON + F sample indicate that fluorine incorporation can further reduce the oxide traps and As-As dimers (contributing to the gap states), giving the best interface among the three samples.

The effects of LaTaON passivation interlayer and fluorine-plasma treatment on GaAs MOS capacitor with TaYON gate dielectric are investigated. Measured results show that samples with LaTaON interlayer have lower interface-state and oxide-charge densities, and fluorine incorporation can further reduce them, which is beneficial to enhancing the carrier mobility and thus drive current for high-speed applications. TEM and XPS indicate that the LaTaON passivation layer can effectively suppress the growth of unstable native oxides at the GaAs surface. Moreover, fluorine incorporation can suppress the out-diffusion of elements from the high-k dielectric and also reduce the oxide traps at/near the high-k/GaAs interface, thus unpinning the Femi level at the interface and giving good electrical properties to the MOS device. In summary, LaTaON interlayer combined with fluorine-plasma treatment is a promising way for passivating the traps in high-performance GaAs MOS devices.

This work was financially supported by University Development Fund (Nanotechnology Research Institute, 00600009) of the University of Hong Kong and the National Natural Science Foundation of China (Grant Nos. 61176100 and 61274112).

[1]J. J. Gu, O. Koybasi, Y. Q. Wu, and P. D. Ye, Appl. Phys. Lett. **99**, 112113 (2011).
[2]G. He, X. S. Chen, and Z. Q. Sun, Surf. Sci. Rep. **68**, 68 (2013).
[3]Y. C. Chang, C. Merckling, J. Penaud, C. Y. Lu, W. E. Wang, J. Dekoster, M. Meuris, M. Caymax, M. Heyns, J. Kwo, and M. Hong, Appl. Phys. Lett. **97**, 112901 (2010).
[4]P. Kordos, R. Kudela, R. Stoklas, K. Cico, M. Mikulics, D. Gregusova, and J. Novak, Appl. Phys. Lett. **100**, 142113 (2012).
[5]R J. Cava and J. J. Krajewski, J. Appl. Phys. **83**, 1613 (1998).
[6]D. Ma, S. Park, B. Seo, S. Choi, N. Lee, and J. Lee, J. Vac. Sci. Technol. B **23**, 80 (2005).

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 147.8.31.43 On: Mon, 14 Nov 2016 07:56:16

[7]S. Duenas, H. Castan, H. Garcia, J. Barbolla, K. Kukli, M. Ritala, and M. Leskela, Thin Solid Films **474**, 222 (2005).

[8]K. J. Hubbard and D. G. Schlom, Mater. Res. **11**, 2757 (1996).

[9]B. Majhi, C. Mahata, M. K. Bera, M. K. Hota, S. Mallik, T. Das, and C. K. Maiti, *16th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits*, Suzhou, China, 6–10 July, 2009, pp. 811–814.

[10]L. M. Lin and P. T. Lai, J. Mater. Sci-Mater. El. **19**, 894 (2008).

[11]K. Kundu, S. Roy, P. Banerji, S. Chakraborty, and T. Shripathi, J. Vac. Sci. Technol. B **29**, 031203 (2011).

[12]L. S. Wang, L. Liu, J. P. Xu, S. Y. Zhu, Y. Huang, and P. T. Lai, IEEE Trans. Electron Devices. **61**, 742 (2014).

[13]L. S. Wang, J. P. Xu, S. Y. Zhu, Y. Huang, and P. T. Lai, Appl. Phys. Lett. **103**, 092901 (2013).

[14]F. Ji, J. P. Xu, Y. Huang, L. Liu, and P. T. Lai, IEEE Trans. Electron Devices **61**, 3608 (2014).

[15]K. Tse and J. Robertson, Appl. Phys. Lett. **89**, 142914 (2006).

[16]J. Ha, K. Seo, and P. C. Mclntyre, Appl. Phys. Lett. **90**, 112911 (2007).

[17]L. N. Liu, H. W. Choi, J. P. Xu, and P. T. Lai, J. Vac. Sci. Technol. B **33**, 050601 (2015).

[18]T. Yang, Y. Xuan, D. Zemlyanov, T. Shen, Y. Q. Wu, J. M. Woodall, P. D. Ye, F. S. Aguirre-Tostado, M. Milojevic, S. McDonnell, and R. M. Wallace, Appl. Phys. Lett. **91**, 142122 (2007).

[19]L. M. Term, Solid-State Electron. **5**, 285 (1962).

[20]C. X. Li, C. H. Leung, P. T. Lai, and J. P. Xu, Solid-State Electron. **54**, 675 (2010).

[21]F. Gao, S. J. Lee, D. Z. Chi, S. Balakumar, and D. L. Kwong, Appl. Phys. Lett. **90**, 252904 (2007).

[22]M. Houssa, A. Stesmans, and M. M. Heyns, Semicond. Sci. Technol. **16**, 427 (2001).

[23]S. Kundu, T. Shripathi, and P. Banerji, Solid State Commun. **151**, 1881 (2011).

[24]K. Marten, W. Wang, K. De Deersmaecker, G. Borghs, G. Groeseneken, and H. Maes, Microelectron. Eng. **84**, 2146 (2007).

[25]M. K. Lee and C. F. Yen, Appl. Phys. A **116**, 2051 (2014).

[26]L. S. Wang, J. P. Xu, L. Liu, W. M. Tang, and P. T. Lai, Appl. Phys. Express **7**, 061201 (2014).

[27]W. Wang, C. Gong, B. Shan, R. M. Wallace, and K. Cho, Appl. Phys. Lett. **98**, 232113 (2011).

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 147.8.31.43 On: Mon, 14 Nov 2016 07:56:16