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AUTONOMOUS SUPPORT AND EFFICIENCY OPTIMIZATION OF SERIES RESONANT CONVERTER

by

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Christopher Thomas Scioscia, M.S.

University of Pittsburgh, 2017

As the electrical grid moves towards modernization and the prevalence of DC architectures, microgrids, and distributed generation increases, the interactions and performances of these DC topologies must be understood and evaluated. Focusing on microgrids, these independent electrical entities typically have distributed generation, local load, some form of energy storage, and a connection with the electrical grid. When instabilities arise on either the grid or the microgrid, the connection can be severed, allowing the microgrid to operate self-sufficiently. While the microgrid is in isolation, resource management is of primary importance as the grid is no longer electrically connected to make up deficits in power that might arise.

This research focuses on utilizing a power management algorithm to maximize the efficiency of an isolated microgrid, as to minimize the losses of the system while limited resources are available. The microgrid consists of photovoltaic generation, local load, a series resonant load converter, and energy storage. The energy storage is placed in parallel with the load converter and is interfaced via bi-directional converters to the front and back ends of the load converter. Utilizing the energy storage as a functional load or source, the operational point of the load converter can be adjusted and consequently the efficiency of the converter can be optimized.

In the work that follows, the design, control, and operation of the aforementioned system are detailed, as well as the autonomous power management logic, which governs the allocation of microgrid resources for optimization of the load converter and thus the microgrid system.

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1.0 INTRODUCTION

The electrical grid is moving towards a decentralized structure in which generation meets load directly at the local level. In the transition to the new architecture, renewable generation and DC microgrids have the potential to play a prominent role. Typically microgrids have an open line with the utility grid, allowing for transfer and sharing of power should the local load exceed local generation or vice-versa. However this is not always the case and the microgrid must be adequately designed to operate as an independent entity in the cases where the grid connection must be severed; this operation is referred to as islanded mode. While in the islanded mode, efficiency and proper utilization of the resources available are of the highest importance as there is no utility connection to make up for power margins. As more microgrids are integrated into the electrical system, the occurrence of these islanded scenarios will rise. Thus there is a need to understand and evaluate the performance of these microgrids while in islanded operation.

In addition to changing grid architectures, the penetration of photovoltaics into the market has been rapidly increasing, especially in recent years. The intermittent characteristic of PV generation necessitates energy storage to accompany these installations. Thus it is not uncommon for microgrids with renewable generation to also include battery storage as it provides redundancy, power smoothing, and a secondary source of power to the PV, which is especially critical during islanded operation.

There has already been research into the performance of PV-Energy storage coupled systems and the their ability to manage energy for varying load conditions with a grid connection [1], [2] and without [3]–[5]. Also of interest are energy storage systems that add functionality to the PV system [6], [7]. Storage systems like the Active Power Distribution Node provide active power flow control and multiple points of failure, increasing system reliability and availability [8], [9]. However studies like those just mentioned typically focus on the system level impact and interactions of the energy storage with the grid. Few studies look on the impact of energy storage in a microgrid isolated scenario and its ability to supplement the performance of an individual converter. Placing energy storage in parallel with a main converter can allow the converter to operate at a superior performance over a wide range of loads, similar to the manner in which composite converters achieve optimized efficiency over wide load range [10]–[12]. In addition to performance, power rerouting, load sharing, reliability, and operational flexibility are all important metrics.

This research focuses on addressing these metrics by using an autonomous control architecture which seeks to maximize the performance of a series resonant converter (SRC) by supplementing its power delivery with a parallel energy storage system. The islanded microgrid being studied consists of local PV generation connected to a DC bus, a high power density SRC, which provides power to the local load, and parallel battery storage interfaced via bidirectional DC-DC converters to the front and back of the high density converter; the system can be seen in Figure 1. The purpose of the parallel energy storage is threefold: it removes the single point of failure by providing two paths for power to flow, increasing system reliability, it provides a means of emergency power should local generation drop out or fail, and it provides the ability to share or source load with the main converter. By acting as a source or sink of power, the battery

storage can effectively move the operating point of the main converter. Depending on conditions outside the of the system, such as weather or power demand, the generation or load may be too great or too little, resulting in power conversion at a poor efficiency point. Using the ability of the parallel storage to alter the operational point of the main converter can result in dramatic improvement to performance, reducing losses and better utilizing the limited resources available to the microgrid.

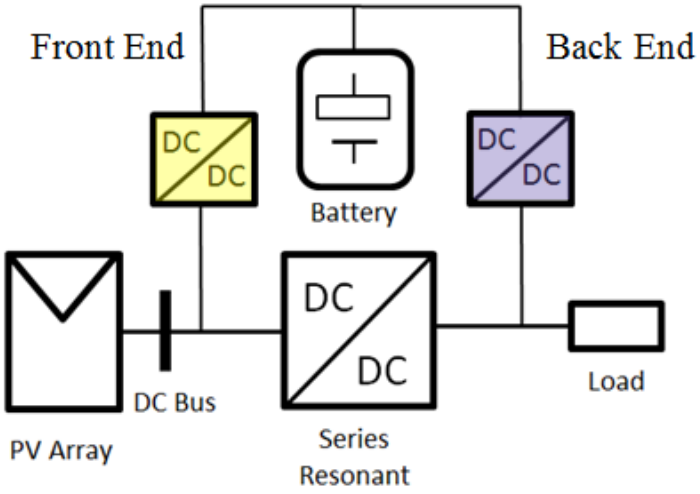


Figure 1. Isolated Microgrid under Study

This thesis consists of seven chapters which are organized as follows.

Chapter 1 provides the context for this research and summarizes a number of studies already conducted which examine the topic of microgrids, PV, and energy storage. This chapter also establishes the focus of this work and provides a high level overview of the research.

Chapter 2 focuses on the design and control of the high density series resonant converter as well as the evaluation of its performance.

In Chapter 3, the battery model and assumptions are presented in addition to the design and control of the bi-directional DC-DC battery interfacing converters.

Chapter 4 covers the photovoltaic model, design of the PV array, and control and implementation of a maximum power point tracking technique using a boost converter.

Chapter 5 examines the autonomous control logic which seeks to maximize the high density converter performance. It also looks at the logic necessary for ancillary features such as voltage sharing/load support.

In Chapter 6 a number of simulation based results are presented to evaluate the effect of the autonomous control architecture under varying operating conditions.

Finally Chapter 7 summarizes this research.

2.0 SERIES RESONANT CONVERTER

2.1 CONVERTER OVERVIEW

The series resonant converter was chosen as the main converter due to the high power density, high switching frequencies, excellent efficiency, and zero voltage switching features of this topology. The steady state analysis and operation of the series resonant converter has been thoroughly researched and is well understood [13]–[16]. The topology of the series resonant converter can be seen below in Figure 2. The converter consists of either a half or full bridge converter on the front end, followed by a resonant LC tank connected to a transformer. The transformer is optional and may or may not be included depending on step up/step down and isolation needs. The transformer connects to a rectifier and output capacitor which feeds the load resistor. Additionally, capacitors may be included across the front end power electronics to reduce switching loss. The converter regulates the output voltage by adjusting its switching frequency above or below the resonant frequency of the LC tank.

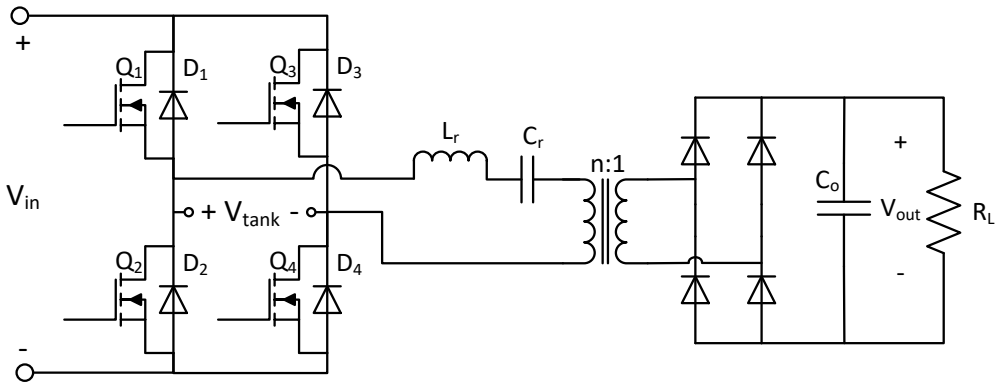


Figure 2. Series Resonant Converter

Operating above the resonant frequency is preferable for a few different reasons. It ensures that the converter always remains in a continuous mode of conductance, it allows for zero-voltage switching to occur, which is desirable when using MOSFETs as the switching device, and it allows for higher switching frequencies to be used [13]. Adjusting the switching frequency of the converter affects the impedance of the resonant tank, which in turn affects the conversion ratio of the converter and thus the regulation of the output voltage. The tank impedance is inversely related to the conversion ratio; as tank impedance increases the conversion ratio decreases and thus the output voltage decreases. For frequencies closer to resonance, the tank impedance is the lowest which results in the highest conversion ratio; this means the greatest amount of energy can be transferred from the input to the output. The opposite is true for frequencies far away from resonance; when tank impedance is high, the conversion ratio is low, and minimal energy can transfer from the input to output.

2.2 CONVERTER DESIGN

The chosen SRC converter design parameters are summarized in Table 1. For a max power rating of 3.2 kW and a desired output voltage of 80 V, then the maximum load that the converter should be able to supply is 40 Amps, which corresponds to 2 Ω of resistance. The size of the output capacitor was chosen to sufficiently large such that the output ripple was minimized to less than 1% of the output voltage under max load. For this we assume that under max load the switching frequency f is close to resonance; the equation for voltage ripple of a full bridge rectifier is shown in (1). Finally it was desired to resonate the converter at 200 kHz; the equation for the resonant frequency of a series resonant converter is shown in (2). The resonant capacitor was calculated after choosing a value for the resonant inductor.

$$V_{ripple} = \frac{I_{load}}{f * C_0} \tag{1}$$

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2}$$

Table 1. SRC Converter Parameters

System Parameter	Variable	Value
Power Rating (kW)	P_{rating}	3.2
Resonant Frequency (kHz)	f_0	200
Input Voltage Range (V)	V_{in}	90 – 150
Output Voltage (V)	V_{out}	80
Transformer Turns	n	1
Resonant Inductor (µH)	L_r	10
Resonant Capacitor (nF)	C_r	63.32
Output Capacitor (µF)	C_0	500

2.3 SRC CONTROL METHODS

There are many methods for controlling the series resonant converter, some of the most popular are frequency control, conduction angle control, current-mode control (often referred to as ASTDIC control), and optimal switching trajectory control [17]–[20]. Each means of control varies in terms of complexity, performance, stability, and range.

2.3.1 Frequency Control

Frequency control is one of the most popular methods of control due to its simplicity and reasonable performance. In this method a voltage controlled oscillator is used to determine switching period necessary to regulate the output via a voltage feedback loop. However some drawbacks of this method include a slow oscillatory response at low output voltage [20] and the existence of a dynamic double pole in the frequency response of this control method, which poses a challenge in closed loop design [17].

2.3.2 Conduction Angle Control

With conduction angle control the controller uses the zero-current crossings in the anti-parallel diodes to determine switch timings. This mode of control is non-linear and shares the same frequency response problems as that of the frequency control [17]. Though this has a low complexity level, the performance and response of this method is poor and has instability issues when operating above resonance in the continuous conduction region [20].

2.3.3 Current-mode Control (ASDTIC)

ASDTIC control rectifies the tank inductor current and compares it to a control signal. The error in the difference between these signals is integrated and this resulting output is a periodic waveform with zero crossings. These crossings determine the actuation times for the MOSFETs to properly regulate the output voltage. The complexity level of this method is noticeably higher than the previous two mentioned and requires two impedance loops instead of one [17]. Additionally there is a well-documented “static-instability” with this method in cases where the impedances of the two loops are not identical [17], [18], [20].

2.3.4 Optimal Trajectory Control

This control method compares the tank voltage and current against the desired trajectory of the tank voltage and current in a two-dimensional state plane. It uses the error in this state-plane analysis to determine transistor conduction timings. The implementation of this method is the most complex and requires the greatest computation but delivers the greatest controller performance out of the methods mentioned [17], [20].

2.4 CONTROLLER DESIGN

For this research, frequency control was chosen as the preferred control method due to balance between simplicity and performance. In this scheme, the duty cycle of the active switches is locked to 50% and the switching frequency is varied over a range above the resonant tank

frequency. In designing an appropriate controller for the SRC, small-signal transfer functions are a vital component. However due to the complex resonant switching characteristics of this converter and the existence of a dynamic double pole in the frequency domain, closed form equations have not been available as they are highly complicated and are unique to each individual design [20], [21]. However recent developments in equivalent circuit modeling have resulted in approximations of the closed form small-signal transfer functions for the series resonant converter [22]. The small-signal equations are functions of the equivalent tank impedance X_{eq}, equivalent tank resistance R_{eq}, and the equivalent tank inductance L_e, which are shown in (3), (4), and (5), where L_r refers to the resonant tank inductance, C_r refer to the resonant tank capacitance, and Ω_s refers to the switching frequency in radians/sec. The control-to-output (frequency-to-output) and the input-to-output small-signal equations derived in [22] are shown below in (6) and (7), respectively, with Ω_0 corresponding to the resonant frequency in radians/sec. By conducting bode plot analysis on these small-signal equations an adequate controller can be designed. However before this can be done, the range of SRC operating frequencies must be known as the equations cannot be solved without it. And before the range of operating frequencies can be determined, certain instabilities regarding the SRC and the frequency control method must be considered, which are discussed in the following section.

$$X_{eq} = \Omega_s L_r - \frac{1}{\Omega_s C_r} \tag{3}$$

$$R_{eq} = \frac{8}{\pi^2} R_L \tag{4}$$

$$L_e = L_r + \frac{1}{C_r \Omega_s^2} \tag{5}$$

$$G_w(s) = \frac{\hat{v}_{out}(s)}{\hat{w}_s(s)} = \frac{-\frac{V_{in}}{\Omega_s}\frac{R_{eq}}{\sqrt{R_{eq}^2 + X_{eq}^2}}\frac{\Omega_s^2 + \Omega_o^2}{\Omega_s^2 - \Omega_o^2}X_{eq}^2}{(s^2 L_e^2 + sL_e R_{eq} + X_{eq}^2)(1 + sR_L C_o) + R_{eq}(sL_e + R_{eq})} \tag{6}$$

$$G_v(s) = \frac{\hat{v}_{out}(s)}{\hat{v}_{in}(s)} = \frac{\frac{R_{eq}}{\sqrt{R_{eq}^2 + X_{eq}^2}}\left(sL_eR_{eq} + R_{eq}^2 + X_{eq}^2\right)}{(s^2L_e^2 + sL_eR_{eq} + X_{eq}^2)(1 + sR_LC_o) + R_{eq}(sL_e + R_{eq})} \tag{7}$$

2.4.1 Hybrid Control

Despite the benefits of the frequency control method, the converter still faces some issues, specifically under no load conditions. These are well documented and include loss of control at no load [17], [19] and poor efficiency at light load and no load [23]–[27], the latter of which is due to circulating tank currents and the higher switching frequencies necessary to regulate the output. One solution that addresses both issues is to use a hybrid switching scheme, with phase-shifted switching for light and no load, and frequency modulated switching (frequency control) otherwise [19], [23].

The design of a frequency based PI controller, i.e. a controller that is tuned to the control-to-output (frequency-to-output), lends itself naturally to this solution as it always outputs the expected frequency. The hybrid scheme can be implemented by limiting the switching frequency to a range between resonance f_0 and a desired limiting frequency f_{limit1}. The minimum switching frequency is referred to as f_{min} and the maximum switching frequency as f_{limit1}. For the load range that encompasses this region the converter regulates the output using switching frequency control, the value of which is determined directly by the PI controller frequency f_{PI}. As the PI frequency increases past the maximum switching frequency, the converter frequency is held constant at the chosen value of f_{limit1} and the converter regulates the output using phase shift control, now using the PI frequency to determine the value of the phase shift ϕ_{PSM}. The phase shift modulation occurs from the first limiting frequency f_{limit1} to a maximum frequency f_{limit2}; at

the boundary of the first limit f_{limit1} no phase shift occurs and at the maximum frequency f_{limit2} full phase shift occurs, at which point the converter is essentially blocking the input. The equation for determining phase shift is shown in (8) and the phase shift only applies to half of the full bridge converter, specifically on switches Q_3 and Q_4.

$$\Phi = \frac{f_{PI} - f_{limit1}}{f_{limit2} - f_{limit1}} * 180° \tag{8}$$

The frequency limits for the hybrid control scheme of the series resonant converter are detailed in Table 2 and the switching ranges and phase shift for each control scheme are shown in Table 3. Switching diagrams for four operating points from max load to light load are displayed in Figure 3. Each diagram shows the switch activation for the high side MOSFETs Q_1 and Q_3, as well as the theoretical voltage across the resonant tank V_{tank} with the corresponding switching frequency f, as well as the PI frequency f_{PI}. The four operating points are in order of decreasing load starting from top left to bottom right: max load, switching frequency/phase shifted boundary, light load, and very light load.

Table 2. Frequency Boundaries for SRC Hybrid Control

Minimum Switching Frequncy	f_{min}	202 kHz
Maximum Switching Frequency (Phase Shift Starting Frequency)	f_{limit1}	240 kHz
Full Phase Shift Frequency	f_{limit2}	260 kHz

Table 3. Frequency Ranges for SRC Hybrid Control

	SRC swithcing frequency	*Phase Shift*	*PI frequency*
Switching Frequency Control	$202\ kHz < f < 240\ kHz$	$\Phi = 0\,°$	$202\ kHz < f_{PI} < 260\ kHz$
Phase Shift Control	$f = 240\ Khz$	$\Phi = \frac{f_{PI} - f_{limit1}}{f_{limit2} - f_{limit1}} * 180°$	

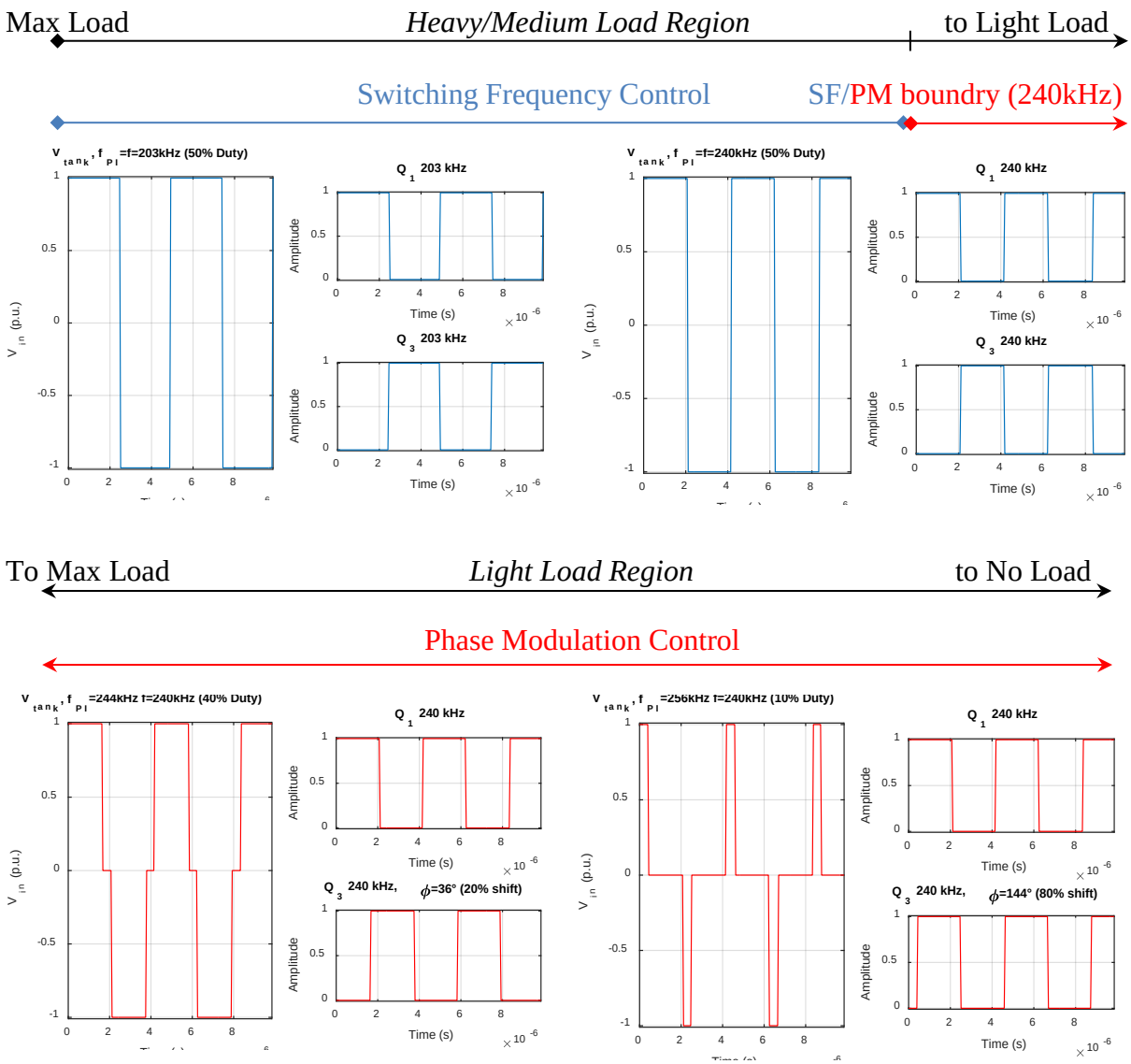


Figure 3. Switching diagram of SRC hybrid control scheme from max load (top left) to very light load (bottom right)

2.4.2 PI Controller Tuning

With the operating range of frequencies defined, bode plot analysis was conducted to tune a PI controller for regulation of the output voltage for the given converter specifications. For stable regulation it is necessary to tune the PI controller for the worst case scenario, which results in least stable conditions. Thus the small-signal frequency responses of (6) and (7) should be plotted for the two ends of operations for switching frequency modulation, which correspond to heavy load and the SF/PM boundary load. The heavy scenario corresponds to the lowest input voltage, 90 V, and smallest load resistance, 2 Ω, while the boundary scenario corresponds to some unknown combination of increased voltage and/or decreased load.

Moreover to determine the frequency response of the small-signal equations more than just the input voltage and load resistance must be known. To compute (3), (4), (5), (6), and (7) one must also know what switching frequency the converter should be operating at. Unfortunately, equations solving for the expected switching frequency of the series resonant converter do not exist or are not readily available due to complexity. However [13] provides the equations for the conversion ratio of the ideal series resonant converter in terms of the mode index, subharmonic number, normalized switching frequency, and normalized load of the converter. The mode index is an integer which satisfies the equality in (9) where F is the normalized switching frequency. For a SRC operating above resonance in the continuous conduction region this integer equals zero. The subharmonic number refers to which subharmonic mode the converter is operating in, if any, and is show in (10). For operation above resonance where the mode index is zero, the subharmonic number is one. The equation for the normalized load (11) is in terms of the transformer ratio n, the load resistance, and the characteristic impedance of the resonant tank.

$$\frac{1}{k+1} < F < \frac{1}{k}, \qquad F = \frac{f_s}{f_0} \tag{9}$$

$$\xi = k + \frac{1 + (-1)^k}{2} \tag{10}$$

$$Q = n^2 \frac{\sqrt{\frac{L}{C}}}{R_L} \tag{11}$$

With values for these converter properties the equation for conversion ratio of an ideal series resonant converter may be solved for (12); note that in this equation, $\gamma = \pi/F$ is the angular length of half the switching period and is inversely proportional to the normalized switching frequency.

$$M = \frac{\frac{Q\gamma}{2}}{\xi^4 * tan\left(\frac{\gamma}{2}\right)^2 + \left(\frac{Q\gamma}{2}\right)^2}\left((-1)^{k+1} + \sqrt{1 + \left(\xi^2 - cos\left(\frac{\gamma}{2}\right)^2\right)\frac{\xi^4\, tan\left(\frac{\gamma}{2}\right)^2 + \left(\frac{Q\gamma}{2}\right)^2}{\left(\frac{Q\gamma}{2}\right)^2 cos\left(\frac{\gamma}{2}\right)^2}}\right) \tag{12}$$

To determine the estimated switching frequency of the converter, (12) was solved iteratively in MathCAD to find the switching values that resulted in the correct conversion ratio. For the heavy load scenario (input of 90 V and a load of 2 Ω) and desired output voltage of 80 V, a conversion ratio of M = 0.88 is needed; the switching frequencies that achieves this is 206.6 kHz.

As for the boundary conditions, the voltage and load values are unknown, yet the boundary frequency is known to be 240 kHz. Once again (12) was solved iteratively to find combinations of load and voltage that resulted in the correct conversion ratio at a frequency of

240 kHz. The first combination tried was the lowest voltage and some unknown load. The input voltage was held constant at 90 V at 240 kHz and the load was varied to determine which value resulted in the correct conversion ratio of M = 0.88; the load that achieves this is 14 Ω. The next scenario that was tried was max load and some unknown voltage; the load was kept at 2 Ω at 240 kHz, which results in a conversion ratio of M = 0.325. However to regulate the output voltage to 80 V at this conversion would require an input voltage 246 V, which is beyond our SRC design parameters for the upper end voltage. For the upper voltage of 150 V, this requires a conversion ratio of M = 0.533, thus the load was increased until this constraint was satisfied resulting in a load of 3.8 Ω. The two boundary scenarios as well as the heavy load scenario are summarized in Table 4.

Table 4. Operating Cases for PI Tuning

Scenario	Input Voltage	Load	M	F_{sw}
Heavy	90 V	2 Ω	0.88	206.6 kHz
Boundary 1	90 V	14 Ω	0.88	240 kHz
Boundary 2	150 V	3.8 Ω	0.533	240 kHz

The frequency response of the control-to-output and input-to-output under heavy, boundary 1, and boundary 2 conditions are shown in Figure 4, Figure 5, and Figure 6, respectively. Observing all three graphs, it can be seen that of the two equations, the control-to-output has significantly lower magnitude, as well as a positive phase from 180º to zero. This positive phase is a result of the negative sign in the numerator of the control-to-output equation

and this must be accounted for when calculating margins by shifting the phase by -180º. Typically gain and phase margins are used to determine whether a system is stable and the measure of system stability. The gain and phase margins of the two responses are listed in Table 5. All margin values are positive indicating inherent system stability however it is desirable to have non-infinite margins for accurate control of a system. To ensure all cases have a non-infinite phase margin the case with the lowest DC gain must be satisfied, which corresponds to the control-to-output response for the first boundary scenario.

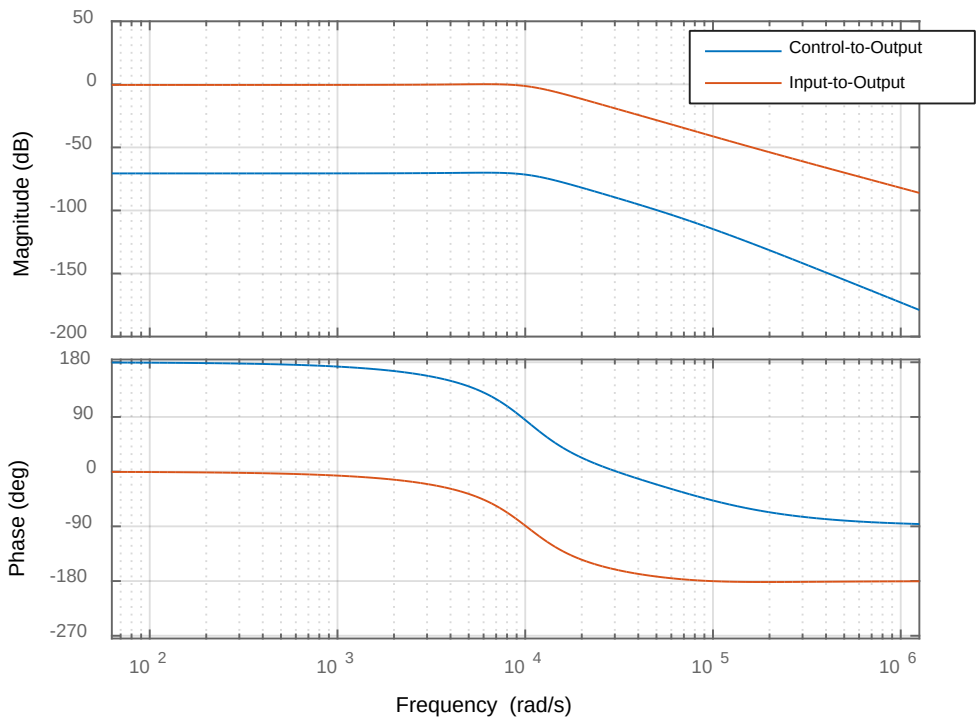


Figure 4. SRC Frequency Response under Heavy Conditions

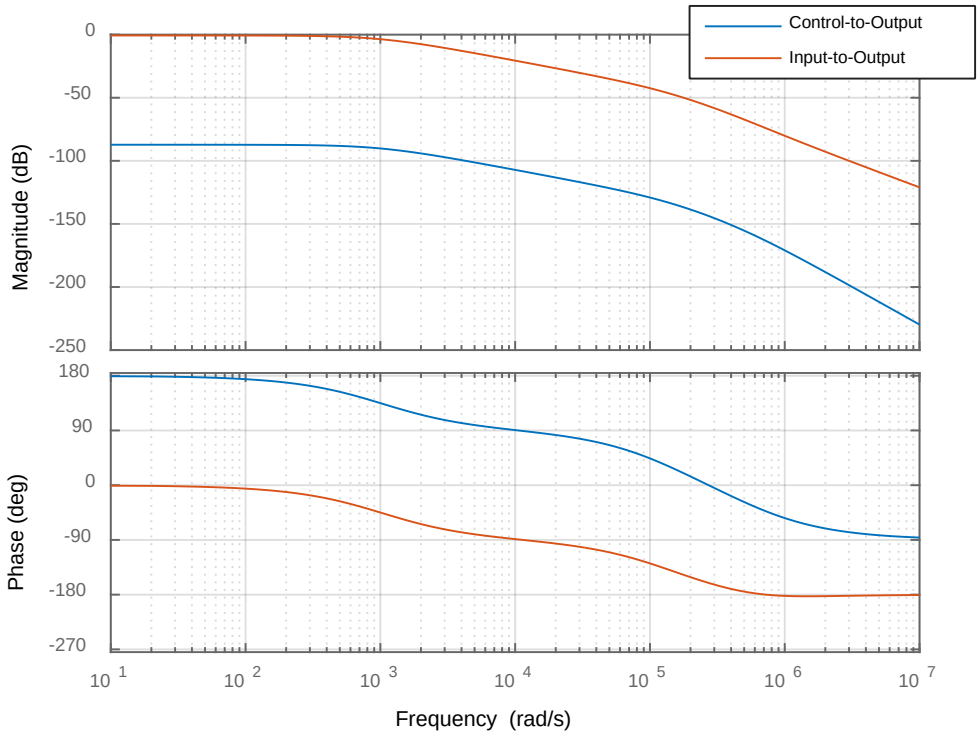


Figure 5. SRC Frequency Response under Boundary 1 Conditions

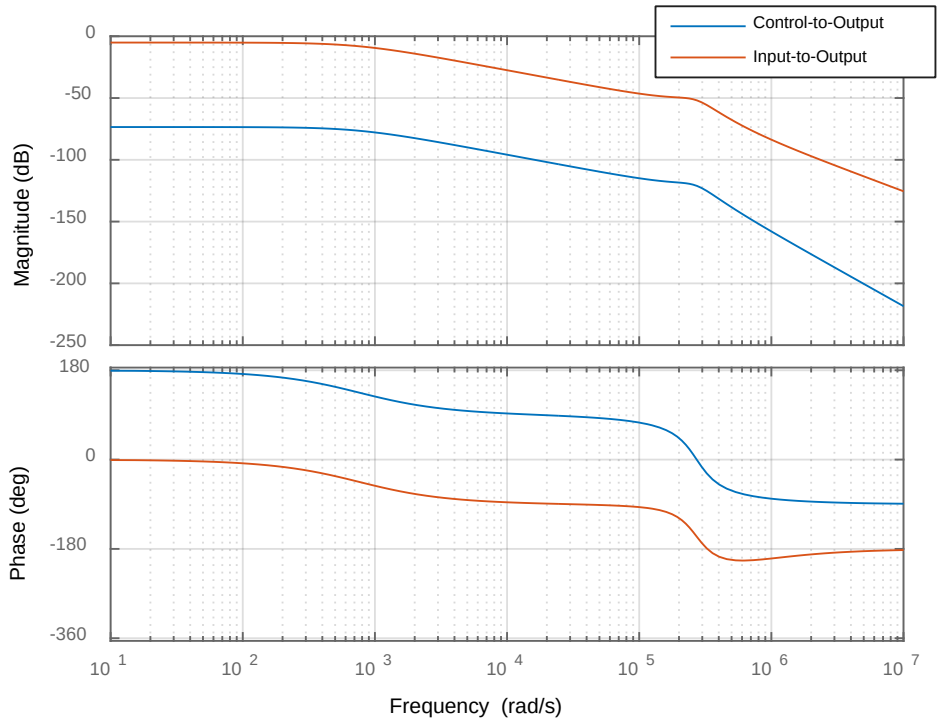


Figure 6. SRC Frequency Response under Boundary 2 Conditions

Table 5. Gain and Phase Margins for PI Operating Cases

	Gain Margin			Phase Margin		
Scenario	**Heavy**	**Bndry 1**	**Bndry 2**	**Heavy**	**Bndry 1**	**Bndry 2**
Ctrl-to-Out	92.9 dB	143.7 dB	121 dB	Inf.	Inf.	Inf.
In-to-Out	40.3 dB	74.12 dB	55.89 dB	Inf.	Inf.	Inf.

The PI controller was then tuned following the general design approach found in [28]. The transfer function for the PI controller is shown in (13). The desired phase margin ϕ_M was chosen to be 50° and the value of K_c was chosen to be -2000 such that dc gain of the control-to-output would have a positive decibel value. The proportional and integral gains were then derived via (14) and (15). In these two equations, ω_1 corresponds to the frequency at which the phase of the control-to-output equals (-180° + ϕ_M + 5°). The derived PI gain values are summarized in; note that the negative sign in the DC gain is to account for the negative sign in the numerator of the control-to-output equation. In practical terms this negative sign in the small-signal equation conveys that there is an inverse relationship between the frequency of the converter and the regulation of the output, as discussed earlier.

$$G_{PI}(s) = K_c(K_P + \frac{K_I}{s}) \tag{13}$$

$$K_P = \frac{1}{|K_c G_w(j\omega_1)|} \tag{14}$$

$$K_I = 0.1\omega_1 K_P \tag{15}$$

Table 6. SRC PI Controller Gains

DC Gain	K_C	-2000
Proportional Gain	K_P	0.0194
Integral Gain	K_I	63.147

The frequency response of the control-to-output of the new PI compensated system is shown in Figure 7 and the Nyquist diagram is shown in Figure 8. Results from the bode plot show that the new gain margin for the compensated system is 112.5 dB and the new phase margin is 89.5°. Generally, an adequately compensated system has at least 8 dB and 30° of gain and phase margin, respectively [28]. Furthermore, from the Nyquist diagram it can be seen that the system model is stable as the path begins at negative infinity, converges to zero, and ends at positive infinity, but does not encompass -1;, note that the x-axis is on the scale of 10^{-3}.

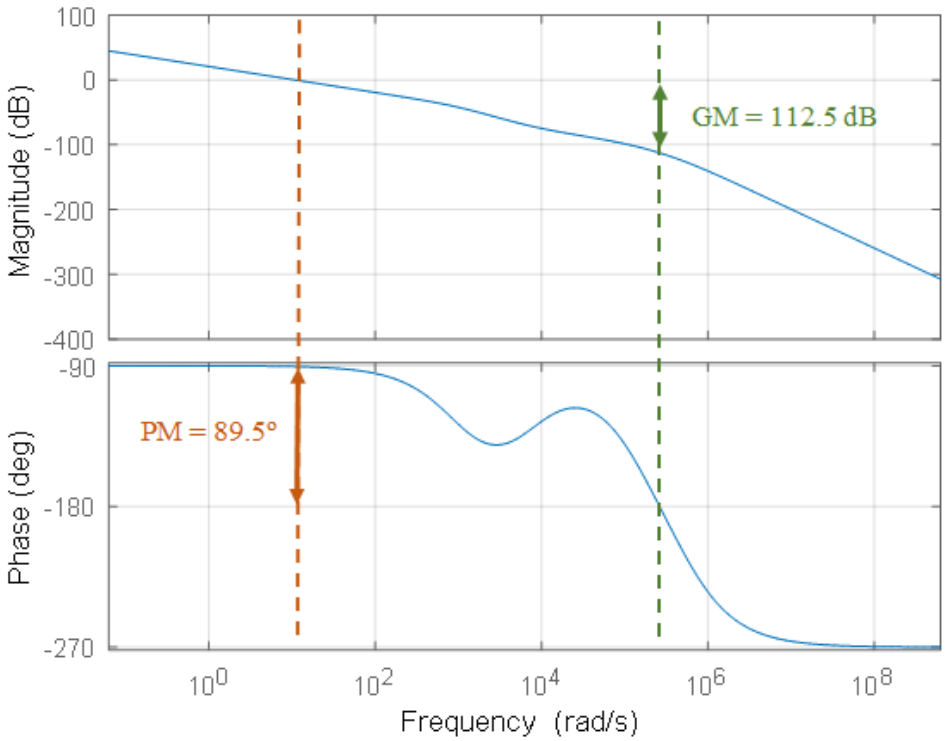


Figure 7. SRC Frequency Response of PI Compensated Control-to-Output

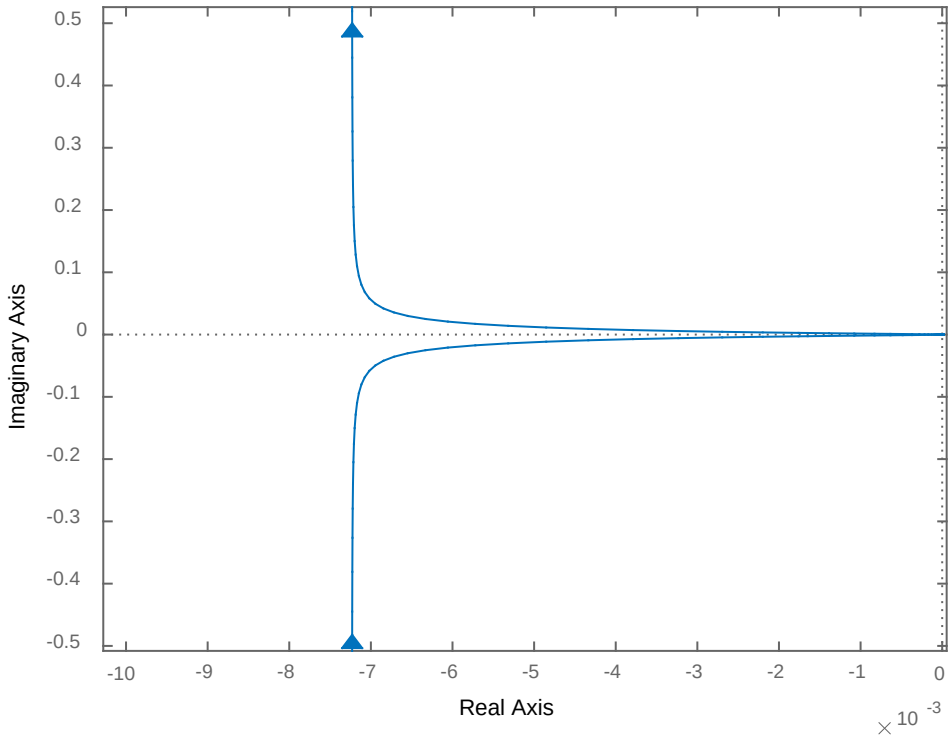


Figure 8. Nyquist Diagram of SRC PI Compensated Control-to-Output

With the PI tuned it can be expected that the controller outputs the switching frequency that the converter should operate at for a given input voltage and load resistance. For example, for increases in the output load or decreases in input voltage, the PI should lower the switching frequency towards resonance. These cases represent a scenario where the converter must move to a heavier operating point to keep the output regulated, either because a greater amount of energy is required at the load or because a lesser amount of energy is supplied to the system. For decreases in load or increases in input voltage the switching frequency should increase via the same logic.

2.4.3 Dead Time

The last topic of control regarding the SRC is the introduction of dead times. Inclusion of dead times on the switches is twofold: it allows for zero voltage switching to occur and it ensures that no two MOSFETs are ever actuated at the same time as to avoid current shoot through, which can cause severe damage to the device. In practical applications the ideal amount of dead time needed is unique to the semiconductor device capacitance [29], [30], however for simulation purposes, a dead time of 4% or less of the minimum switching period achieves the desired effect without adversely affecting the output of the converter [31]. For the SRC, a dead time of 100 ns was used, which is 2.4% of the minimum switching period of 4.167 μs, the period corresponding to max switching frequency 240 kHz.

2.5 SIMULATION AND VERIFICATION

The SRC was modeled in Ansys Simplorer to verify that the circuit operates as expected and that the PI controller correctly regulates the output voltage for steady state operation. Using (12), the frequency necessary for regulation can be predicted and compared to the simulation frequency. The cases to be verified are shown in Table 7 and include max load, the switching frequency boundary, and phase shifted light load. As before, the frequency was calculated iteratively by determining the conversion ratio M that regulates the output to 80 volts. It should be expected that the simulation frequencies deviate slightly from this as (12) is for a lossless converter, and the diodes and MOSFETs used in the simulation have slight loss resulting from a forward voltage of 0.8 V and an on resistance of 1 mΩ. Frequencies can be predicted for the first two cases, however making accurate estimation of the required phase shift is challenging, as the equation exists in the complex domain and requires knowledge of the phase shift in the resonant tank to calculate phase shift for regulation [23].

Despite this a reasonable estimate of the phase shift can be made based off the size of the load compared to the load at the phase shift boundary. From (12), for the case of a 90 V input and 14 Ω (457 W load), the estimated frequency to regulate is 240 kHz, i.e. the phase shifted load boundary. The light load case has a load resistance of 40 Ω (160 W); thus this case is equivalent to 35% of the 457 W phase shift load boundary, that is, the light load case is 35% of the load which requires no phase shift. Equivalently the light load case can be seen as 65% of the full phase shifted case, i.e. no load. Via this logic, an equation for estimated phase shift based on load is derived in (16). For the light load case, the phase shift is predicted to be around 115º. This calculation was done for an input voltage 90 V; as the simulation voltage is 150 V, it is expected that the actual phase shift is greater due to a lower conversion ratio needed for regulation.

$$\Phi_{\text{est}} = \left(1 - \frac{P_{PS_{boundary}}}{P_{lightload}}\right) * 180° \tag{16}$$

The Simplorer verification circuit can be seen in Appendix A section A.1 along with logic blocks for the hybrid control of the converter. The capacitors in parallel with the full bridge MOSFETs were included to achieve ZVS switching. Typically, device capacitance is enough to achieve this type of switching however the Simplorer semiconductor models used did not account for specific device capacitance. As per the recommendation for ZVS switching of a SRC found in [13] the value of these parallel capacitors was kept small; a capacitance of 1 nF was chosen. The circuit was simulated at a time step of 50 ns and graphs of the output capacitor voltage, PI output frequency, and phase shift are shown in Figure 9, Figure 10, and Figure 11, respectively.

Table 7. Verification Cases for Operation of SRC

Scenario	**Duration**	**V_{IN}**	**Load**	**Predicted**	
				Frequency	Phase Shift
Max Load	0 – 7.5 ms	90 V	2 Ω (3200 W)	**206.6 kHz**	0 º
SF Boundary	7.5 – 17.5 ms	90 V	13 Ω (492 W)	**236 kHz**	0 º
Light Load	17.5 – 25 ms	150 V	40 Ω (160 W)	240 kHz	**>115 º**

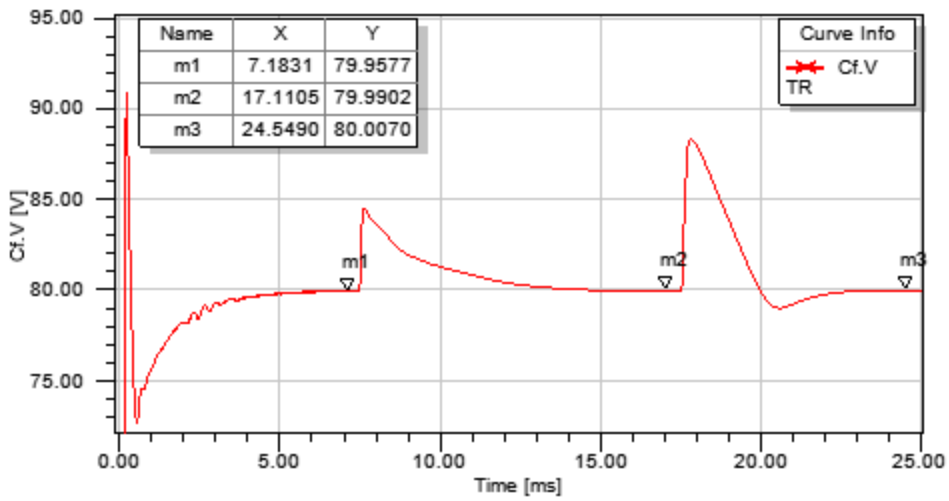


Figure 9. SRC Capacitor Output Voltage Regulated to 80 V during Verification Cases

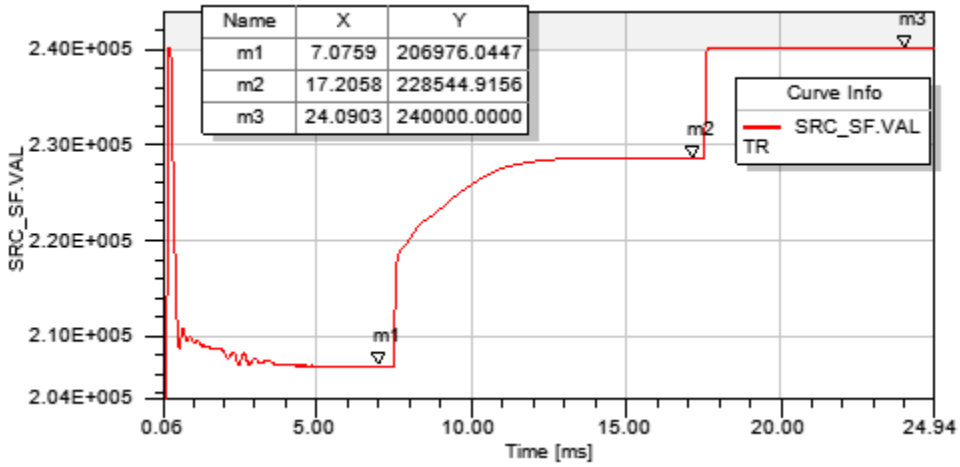


Figure 10. Output of SRC PI Frequency Controller during Verification Cases

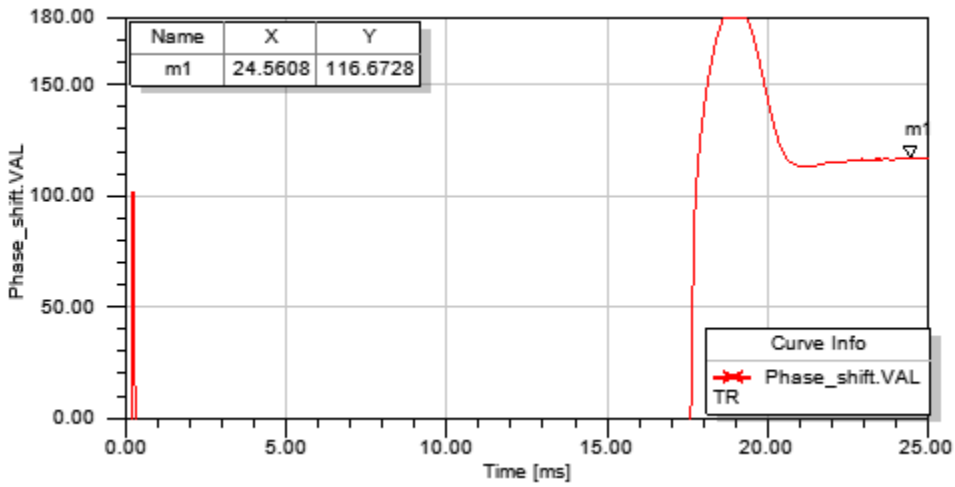


Figure 11. Measured SRC Phase Shift during Verification Cases

Figure 9 shows that the controller is able to successfully regulate the output voltage to the target of 80 V as the simulation transitions through the verification cases. Moreover, the controller is able to return to steady state target voltage quickly, within 10 ms, for large shifts in operating points. From Figure 10 it can be seen that the simulation switching frequencies are close to the predicted values: 206.9 kHz for max load and 228.5 kHz for the SF boundary. Though there is a percent difference of -3.2% for the later test case, slight deviation from the calculated ideal frequency was expected as the simulation includes some losses. Finally, Figure 11 verifies that the phase shift control is able to correctly regulate for light load conditions; the estimate phase shift had only 1.3% difference from the simulation shift of 116.6 º.

2.6 SRC PERFORMANCE EVALUATION

A case study was performed on the SRC to evaluate the performance across its load range for varying input voltage. The converter was swept over a load range from 133 W (60 Ω) to 3200 W (2 Ω) for input voltages of 90 V, 100 V, 110 V, and 150 V. Both the power into the full bridge of the SRC and out of the SRC diode bridge were averaged over 20 switching periods and the efficiency was calculated via (17) at each operating point. The resulting case study yielded the efficiency profile of the SRC shown in Figure 12.

$$\eta = \left(\frac{P_{in_{SRC}}}{P_{out_{SRC}}}\right) * 100\% \tag{17}$$

It can be seen that the converter performs sub-optimally under heavy and light loading, more so in the latter case, and that the optimal efficiency exists somewhere in the middle of the performance curve. It can also be seen that for changes in the input voltage, the general profile of the curve keeps its shape but shifts vertically, with the best efficiency curve occurring at the lowest input voltage. From these observations it can be reasoned that for a sub-optimal operating point, the SRC performance could be improved by adding or removing load to the converter, depending on the scenario. For example, the SRC supplies a load of 250 W at 150 V input for an efficiency of ~88%; if an additional load of 600 W was added to the output of the SRC, for a total load of 850 W, we should expect the operating point to shift along the 150 V curve to an

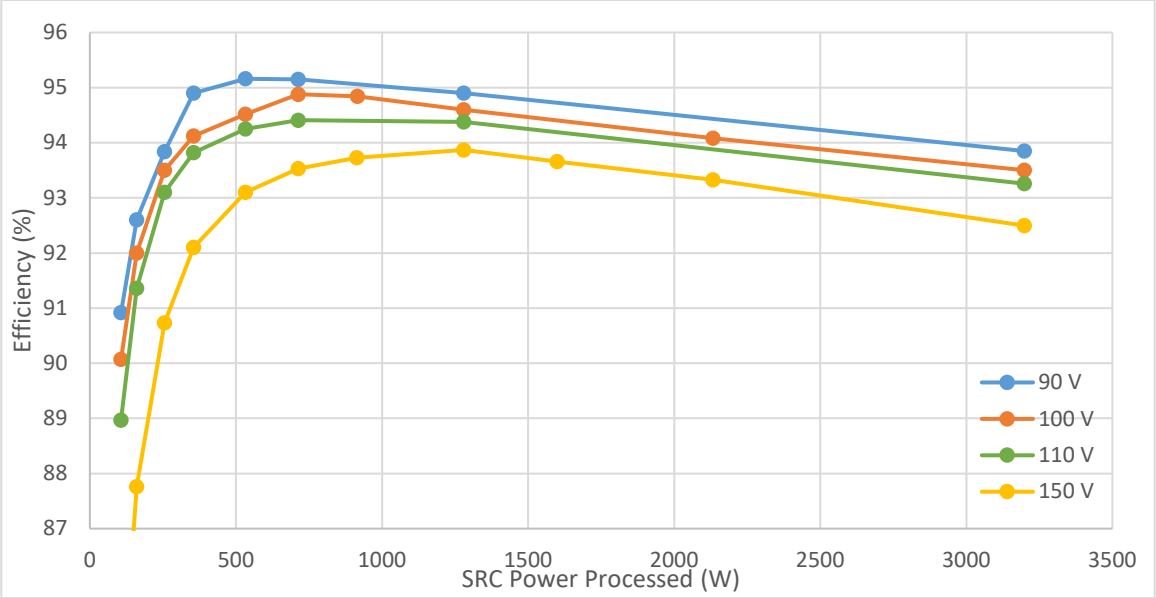


Figure 12. SRC Performance Over Load Range for Varying Input Voltage

improved efficiency of ~93.8%. Similarly, the SRC was supplies a load of 3200 W at 150 V input for an efficiency of ~92.5%; if load 2000 W of load was removed from the output, then the SRC effective load is now 1250 W at 150 V and we should expect the new efficiency improve to ~94%.

On the other hand, adding additional load to the front end of the SRC (i.e. in parallel with the SRC on the output of the source) serves to reduce input voltage, assuming a limited power source. For a non-ideal source maintaining a constant power output, an increase in the current demand results in a decrease of voltage as P = I/V must be satisfied. Thus to reduce input voltage and improve SRC performance load should only be added in parallel on the front of the SRC and only in scenarios where enough excess power exists to continue to serve the critical SRC load without issue.

Both these interactions can be taken advantage of by placing a battery in parallel with the SRC and using it as a function load, specifically by utilizing its ability to act as a current sink or current source. Transferring current between the battery and the back end of the SRC changes the effective load of the SRC, moving its operating point along a given curve. Transferring current via the battery and the front end of the SRC changes the effective input voltage to the SRC, shifting the operating point vertically between efficiency curves.

2.7 COMPONENT SIZING AND REEVALUATION

2.7.1 Power Electronics Sizing

To achieve a more accurate picture of SRC performance, semiconductor parameters needed to be included in the simulation model to reflect realistic losses. The devices under consideration are the MOSFETs in the full bridge converter and the diode bridge. Due to the high switching frequencies of this design, Silicon Carbide (SiC) based MOSFETs are a practical choice for the full bridge, while standard low loss silicone semiconductors are sufficient for the diode bridge. For this design the three essential constraints on both devices are the DC blocking voltage V_{DC}, continuous forward current I_F, and peak-pulsed forward current I_{Fpeak}. For the MOSFETs, the DC blocking voltage must be larger than the maximum input voltage of 150 V, while the two current constraints are determined by the current in the resonant tank inductor. For the diodes, the DC blocking voltage must be rated to block the voltage across the transformer, which is equivalent to the difference between the voltage across the full bridge and the voltage across the resonant tank; this value was determined through simulation. Current constraints for the diodes are the same as for the MOSFETs and correspond to the resonant inductor current.

The current flowing through the resonant inductor is derived in [32] and can be seen in (19), with the peak value occurring during maximum load. The specifics for the max load case were detailed earlier in section 2.4. The semiconductors rated value for peak-pulsed forward current must be larger than the peak resonant inductor current. As for the continuous forward current rating of the devices, this value must be larger than the average current flowing in the semiconductors, which is equal to the average of a half-sine wave with amplitude equal to peak

inductor current, see (20). A table of these design constrains and their values are shown in Table 8 for both the SiC MOSFETs and Si bridge diodes.

$$R_0 = \sqrt{\frac{L_r}{C_r}} \tag{18}$$

$$I_{L_r} = \frac{V_{in}}{R_0} * \left(\frac{\pi}{2} M * Q - \left(M - 1 + \frac{2}{\pi}\sqrt{1 - M^2}\right)\right) \tag{19}$$

$$I_{avg} = \frac{1}{\pi} I_{L_{r_{peak}}} \tag{20}$$

Table 8. Constraints for SRC Semiconductor Devices

	Variable	Constraint Values			
		MOSFET	Eqn.	**Diode**	Eqn.
Blocking Voltage	V_{DC}	150 V	-	85.8 V	Sim.
Peak Current	I_{DM}	61.46 A	(19)	61.46 A	(19)
Avg. Continuous Current	I_D	19.56 A	(20)	19.56 A	(20)

2.7.2 LC Tank Sizing

The losses resulting from the resonant tank were also of consideration. Component ratings were designed around max current and voltage seen on the inductor and capacitor, respectively. As mentioned previously, the maximum stress on these devices occurs while under heaviest load. The equation for resonant inductor current was shown previously and the maximum condition

current values are seen above. The equation for resonant capacitor voltage is also derived in [32] and can be seen in (21). Because the current and voltage in the resonant tank are AC signals, RMS values of the peak conditions are used to choose appropriately rated components. The design constraints for the resonant tank components are seen in Table 9.

$$V_{C_r} = V_{in}\left(\frac{\pi}{2}M * Q - \frac{2}{\pi}\sqrt{1 - M^2}\right) \tag{21}$$

Table 9. Constraints for SRC Tank Components

	Peak Value	**RMS Value**	**Equation**
Resonant Inductor	61.46 A	42.45 A	(19)
Resonant Capacitor	756.7 V	535 V	(21)

Relevant parameters and part numbers of the chosen SRC components are detailed in Appendix B section B.1 along with a discussion of modeling of certain losses in Ansys Simplorer.

2.7.3 SRC Performance Reevaluation

The performance case study was redone for SRC with the new loss parameters included in the simulation model. The converter was again swept over its load range from 133 W (60 Ω) to 3200 W (2 Ω) for a wider range of input voltages from 90 V to 400 V, see Figure 13 . The addition of losses altered the shape of the efficiency curve, however the general profile is still the same and the observations about current transfer with parallel energy storage via the front and back ends of

the SRC still apply. Arrows have been added to the graphs indicating the two methods of battery assisted current transfer and the effect each has on SRC performance. This graph provides key insights into the logic needed to design the assistance algorithm to correct optimize the SRC, in addition to providing a baseline to comparing performance with battery assistance.

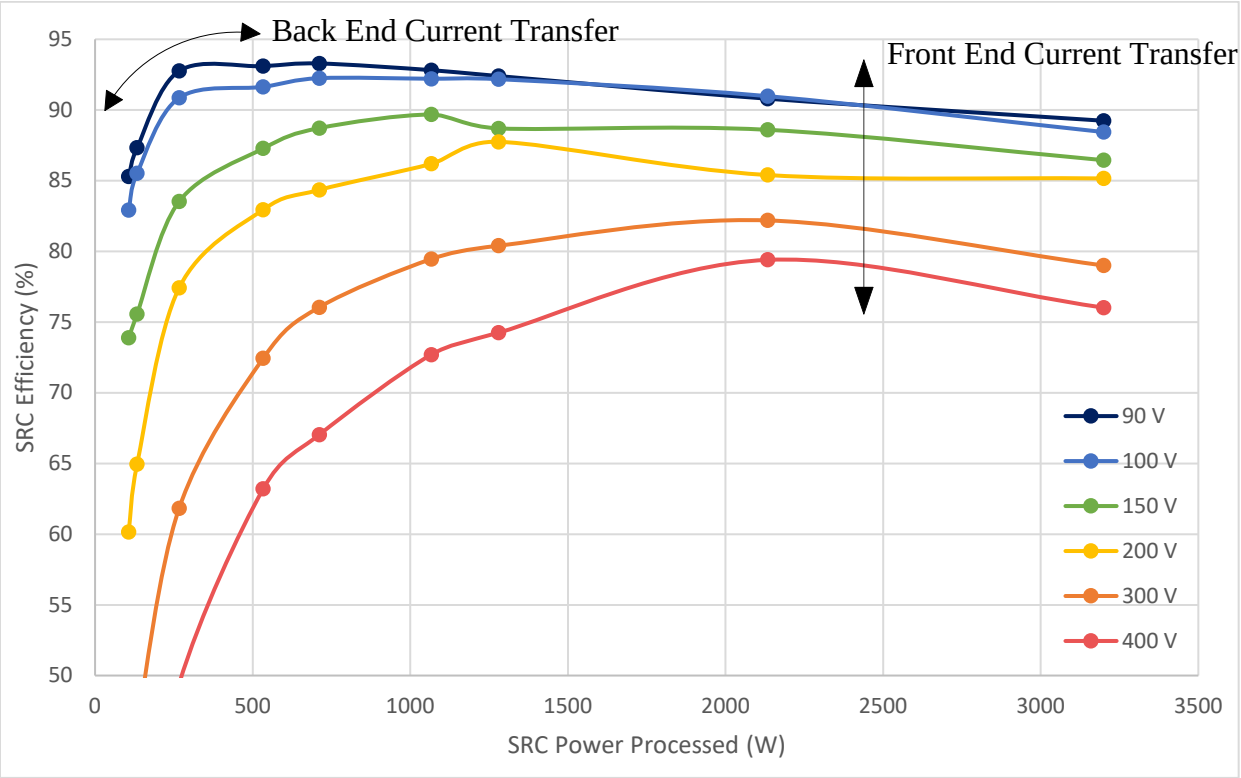


Figure 13. SRC Performance with Losses Over Load Range for Varying Input Voltage

3.0 BATTERY INTERFACING CONVERTER

3.1 BIDIRECITONAL BUCK-BOOST CONVERTER OVERVIEW

The DC/DC bidirectional buck-boost converter, also referred to as a type C chopper, was chosen as the converter to interface the SRC with the parallel battery storage. This topology is what is known as a two quadrant converter, meaning that it can transfer current in two directions depending on whether the high side or low side semiconductor is switched. In addition to bidirectionality, this topology boasts a simple circuit structure and straightforward design and control. As such, this converter is one of the most common converter designs used in conjunction with energy storage [33]–[38] and its operation is well understood [31], [38]–[40]. The circuit diagram of the bidirectional buck-boost converter can be seen in Figure 14, and it consists of a low side capacitor and inductor, half bridge converter, and high side capacitor. With regards to the larger microgrid system, the low side capacitor interfaces with the battery storage and the high side capacitor interfaces with the series resonant converter.

The converter has two modes of operation which correspond to the two directions of power transfer. In boost mode the low switch Q_L is actuated, resulting in current flow down through the low switch Q_L during the “on time” of the duty cycle, and current flow up through the high switch freewheeling diode D_H during the “off time” of the duty cycle. The net result is the transfer of power from the low side capacitor up to the high side capacitor, i.e. the battery is

discharged. In buck mode the high switch Q_H is actuated, resulting in current flow down through the high switch Q_H during the "on time" of the duty cycle, and current flow up through the low switch freewheeling diode D_L during the "off time" of the duty cycle. The net result is the transfer of power from the high side capacitor down to the low side capacitor, i.e. the battery is charged. The buck and boost modes of operation and the respective switching schemes are shown in Figure 15.

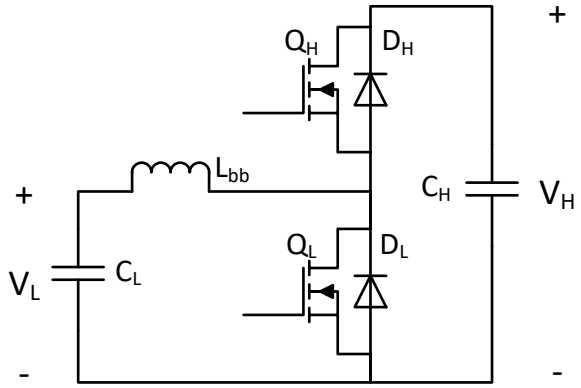
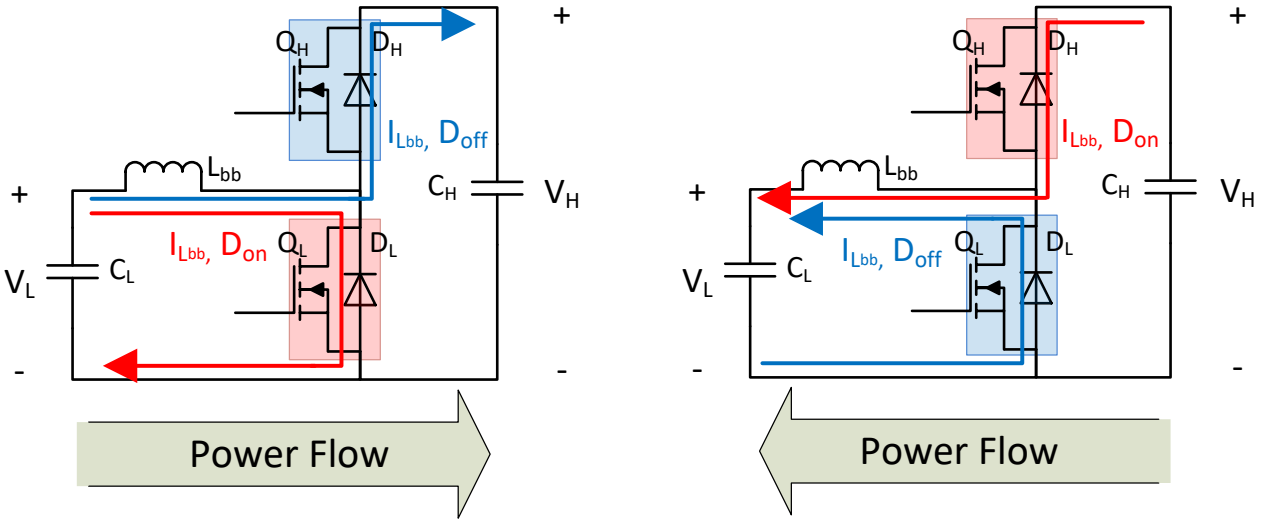


Figure 14. Bidirectional Buck-Boost Converter



a) Boost Mode Operation

b) Buck Mode Operation

Figure 15. Switching operation of Buck-Boost

3.2 BIDIRECITONAL BUCK-BOOST CONTROL METHODS

Regulation of the buck-boost converter as described above is typically done using pulse width modulation. The control is based around regulating either capacitor voltage or inductor current, however regulation requires two independent duty cycle controllers as battery charging and discharging differ from a control perspective [31], [38], [41]. For this system, the load voltage is already regulated by the SRC, thus current control of the bidirectional converters is the preferred choice. Moreover, for the purposes of injecting or absorbing power to adjust SRC performance, current control lends itself naturally to this objective as incremental adjustments to current correspond to incremental adjustments in power. Additionally [31] proposes a unified current controller which makes use of synchronous switching to regulate both charging and discharging with a single duty cycle. The relationship between duty cycle and inductor current (battery current) in this unified controller is shown in Figure 16 with the equation for the zero current duty cycle D_0 in (22).

$$D_0 = \frac{V_L}{V_H} \tag{22}$$

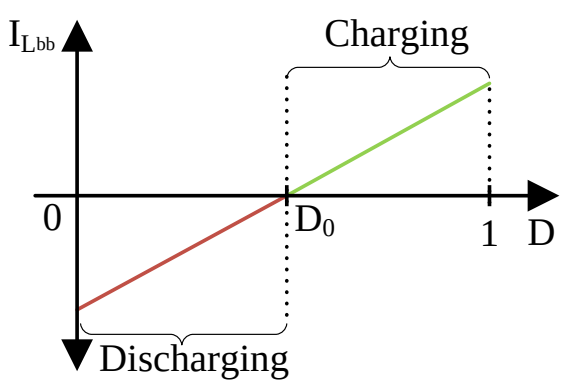


Figure 16. Duty Cycle for Two Modes of Buck-Boost Operation under Unified Scheme

3.3 BATTERY DESIGN

To adequately design a controller for the bidirectional buck-boost converter, additional information must be known about the low voltage battery storage side of the system. However modeling of a battery is quite complex as the parameters are dynamic and change with temperature, state of charge, and age [42]. This level of battery detail is outside of the scope of this research, and so a simple battery model was used, consisting of a static voltage source and static series resistance.

The chosen type of battery cell was a lithium ion cell which has a voltage range from 2.7 V to 4.2 V with a nominal voltage of 3.7 V [43]. Additionally lithium ion cells have a typical capacity ranging from 2 Ah to 2.5 Ah with a DC series resistance (DCR) between 15 mΩ and 35 mΩ [44]. It was desired to have a battery voltage of around half the regulated SRC output of 80 V, as this would place D_0 of the back end buck-boost converter close to 50% duty cycle, allowing for equal charging and discharging ranges. Motivation for this is that the back end converter must be able to shift the load by half of the max rating of 3.2 kW in order to achieve optimal efficiency for the two extreme scenarios, full load and no load, see Figure 13. Rough estimations of the required battery capacity were done to produce relevant battery parameters and are detailed below.

To achieve a battery voltage of half the output voltage, 12 cells were stacked in series to achieve a nominal voltage of 44.4 V; a voltage of 42 V was used for the battery voltage source. To supply a maximum load of 3.2 kW at 42 volts, about 76 amps of current needed to be supplied. Assuming 2 Ah rated lithium ion cells, 38 cells were stacked in parallel to satisfy the current demand. Assuming a DCR of 35 mΩ per cell, the equivalent series resistance of the 12 by 38 cell battery was 11.05 mΩ; a resistance of 11 mΩ was used for the battery series

resistance. With the battery parameters established the bidirectional buck-boost converter can be designed.

3.4 BIDIRECITONAL BUCK-BOOST CONVERTER DESIGN

The design of the front and back bidirectional converters is very similar, with the only difference being the rated power and voltage of the converters. As mentioned before the back end converter should be rated for at least half the max load of 3.2 kW. For the front converter it is desired to have the converter rated for the full power of the max load to provide voltage support on the DC bus in the case of complete PV shading. Finally it is desired to have both converters operate in the continuous conduction mode (CCM) region.

For CCM design, the first step is to determine an inductance that guarantee continuous current in the inductor for both buck and boost mode operation. Equations for minimum inductance are provided in [40] and are shown in (23) and (24) for buck and boost operation, respectively. In these equations P refers to the power processed by the converter, f_s refers to the converter switching frequency, and η refers to the converter efficiency, which was assumed to have a value of 0.95. The minimum inductance required for CCM is the largest of the buck and boost inductor values. It is important to note that CCM operation is not realistic for the no load power case, because as power decreases to zero the required inductance converges to infinity. Therefore a minimum power case must be chosen.

$$L_{buck} = \frac{V_L^2\left(1 - \frac{V_L}{V_H} * \frac{1}{\eta}\right)}{2 * f_s * P} \tag{23}$$

$$L_{boost} = \frac{2}{27}\frac{V_H^2}{f_s * P} \tag{24}$$

A secondary design choice was to make use of multiple phases in the buck-boost converter design, the addition of which serves to reduce total current ripple, reduce the power demand and stress on each of the individual phase, and improve efficiency at the cost of additional power electronics and passive components [45], [46]. Additionally the inclusion of multiple phases necessitates larger per phase inductance as the equivalent inductance must still exceed the critical inductance for CCM and inductances in parallel reduce equivalent inductance. The duty cycle control of the converter is minimally affected, the only difference being that each of phase control signals must be offset by a degree phase shift, the size of which depends upon the number of branches. The equation for the phase shift for each control signal is shown in (25), where N is the number of converter phases.

$$\varphi_{BB_N} = \frac{180°}{N} \tag{25}$$

3.4.1 Back End Battery Converter

The minimum power case for the back end bidirectional converter was assumed to be 210 W, which corresponds to 5 amps of battery current at the battery voltage of 42 V. The high side of the converter interfaces with the SRC load, which is regulated to 80 V. For the switching frequency of the converter it was desired to switch at a frequency with no multiples within the range of the resonant converter frequencies as to avoid interference with one another. The converter parameters for the back buck-boost converter are detailed in. The inductance was calculated for both buck (23) and boost (24) operation under maximum and minimum power. The inductances for the four cases were calculated and are summarized in Table 11. The

minimum inductance necessary for CCM occurs for the minimum power load case during buck operation and is 30.3 μH.

Table 10. Back Buck-Boost Converter Parameters

System Parameter	Variable	Value
Minimum Power (W)	P_{min}	210
Maximum Power (W)	P_{max}	2000
Minimum Current (A)	I_{min}	5
Maximum Current (A)	I_{max}	47.6
Battery Voltage (V)	V_L	42
Battery Capacitance (μF)	C_L	175
SRC Load Voltage (V)	V_H	80
Efficiency	η	0.95
Switching Frequency (kHz)	f_s	62

Table 11. Critical Inductance for Back Buck-Boost Converter

Mode of Operation	Variable	High Side Voltage	Min Power: P = 200 W	Max Power: P = 2000 W
Buck Mode	L_{buck}	V_H = 80 V	**30.30 μH**	3.18 μH
Boost Mode	L_{boost}	V_H = 80 V	19.11 μH	3.82 μH
Minimum Inductance for CCM			**30.3 μH**	

The number of parallel converter phases was chosen to be two, which means that the per phase inductance must be twice the minimum inductance for CCM, or 60.6 μH. Additionally each phase must be rated to carry up to 23.8 A of current to meet the full 47.6 A rating of the converter. Finally from (25) the control signals must be offset by a phase shift of 90º. The circuit diagram of the two phase back end buck-boost converter and low side battery is seen in Figure 17. The per phase inductance used in simulation was 68 μH with an inductive DC resistance of

2.8 mΩ. Relevant parameters and part numbers of the inductor and power electronics chosen for the back buck-boost converter are detailed in Appendix B section B.2 along with a discussion of modeling of certain losses in Ansys Simplorer.

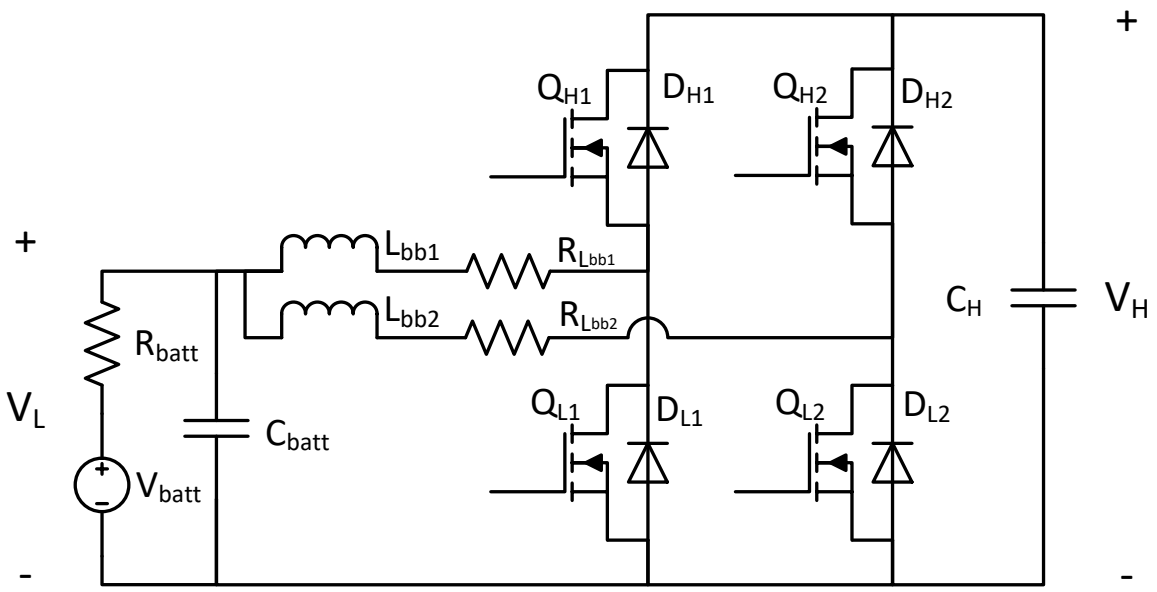


Figure 17. Back End Two Phase Bi-directional Buck-Boost Converter and Battery

3.4.2 Front End Battery Converter

The minimum power case for the front end bidirectional converter was again assumed to be 210 W, which corresponds to 5 amps of battery current. The high side of the converter interfaces with the front of the SRC converter, which is connected to the output of the PV array, with a voltage range from 90 V to 150 V. As with the back buck-boost converter the switching frequency was

chosen so that it is not a multiple of the SRC converter frequency range. The converter parameters for the front buck-boost converter are detailed in Table 12. The inductance was calculated for both buck (23) and boost (24) operation under maximum and minimum power for both the maximum and minimum high side voltages. The inductances for the six cases were calculated and are summarized in Table 13.

Of the six cases the largest inductance value is 47 μH and occurs for the minimum power load case during buck operation with the high side voltage at its max. However this value is not necessarily the critical inductance as the operating conditions are somewhat contradictory, specifically with regards to the maximum voltage and minimum power. If the high side voltage is at its maximum this indicates that there is excess power from the PV array. In the case of excess power from the array it is expected that the front buck-boost converter charges the battery as to reduce the input voltage to improve SRC efficiency. Therefore it is likely that the front buck-boost converter process more power than the minimum power assumed, hence this case can be thrown out.

The next largest inductance value is 35.27 μH and occurs for the minimum power load case during boost operation with the high side voltage at its max. However this value is also not representative of the critical inductance as the boost operation of the converter under these conditions is directly contradictory to the control objective of maximizing the SRC efficiency. Optimal efficiency for the SRC occurs at the lowest input voltage to the converter, so to discharge the battery while the input voltage is at its highest would only serve to further increase the voltage, hence this case can be thrown out as well. The minimum inductance necessary for CCM occurs for the minimum power load case at minimum input voltage during buck operation and is 33.91 μH.

Table 12. Front Buck-Boost Converter Parameters

System Parameter	Variable	Value
Minimum Power (W)	P_{min}	210
Maximum Power (W)	P_{max}	3800
Minimum Current (A)	I_{min}	5
Maximum Current (A)	I_{max}	90.5
Battery Voltage (V)	V_L	42
Battery Capacitance (µF)	C_L	175
PV Min Voltage (V)	V_{Hmin}	90
PV Max Voltage (V)	V_{Hmax}	150
Efficiency	η	0.95
Switching Frequency (kHz)	f_s	63

Table 13. Critical Inductance for Front Buck-Boost Converter

Mode of Operation	Variable	High Side Voltage	Min Power: P = 200 W	Max Power: P = 3800 W
Buck Mode	L_{buck}	V_{Hmin} = 90 V	**33.91 µH**	1.87 µH
		V_{Hmax} = 150 V	~~47.01 µH~~	2.59 µH
Boost Mode	L_{boost}	V_{Hmin} = 90 V	21.16 µH	2.51 µH
		V_{Hmax} = 150 V	~~35.27 µH~~	6.96 µH
Minimum Inductance for CCM			**33.91 µH**	

The number of parallel converter phases was again chosen to be two, which means that the per phase inductance must be twice the minimum inductance for CCM, or 67.82 µH. Additionally each phase must be rated to carry up to 45.25 A of current to meet the full 90.5 A rating of the converter. As before the control signals of the two phase converter must be offset by a phase shift of 90º. The circuit diagram of the two phase front end buck-boost converter is identical to the back end converter seen in Figure 17. The per phase inductance used in simulation was 92 µH with a inductive DC resistance of 7.5 mΩ. Relevant parameters and part numbers of the inductor and power electronics chosen for the front buck-boost converter are detailed in Appendix B section B.3.

3.5 CONTROLLER DESIGN

With the parameters of the converters established and the low side battery parameters known, the controllers for the two converters may be addressed. For control of a battery load converter the PI controller may be tuned around two different equations: the control-to-inductor current transfer function or the control-to-battery current transfer function [31]. For the functionality of this system, it is necessary to independently control the current flowing in each of the two battery load converters. Thus the control-to-battery current equation is not viable because this value is the combined current of both converters and as such, does not result in independent converter control. Therefore the control-to-inductor current equation is used to design the PI controller. The small signal equation relating inductor current to duty cycle for a battery load converter is provided in [31] and shown in (26).

$$G_{id}(s) = \frac{\hat{\imath}_{L_{bb}}}{\hat{d}} = \frac{V_H}{L_{bb} * s + R_{L_{bb}} + R_{batt}} \tag{26}$$

This equation describes the battery load converter as a first order system and a function of the high side voltage, inductance, DC inductive resistance, and battery resistance. It is important to note that the inductance refers to the equivalent inductance of the converter. For a two phase converter, the equivalent inductance is half of the per phase inductance.

Although using the inductor current as the control variable has the advantage of independent converter control, the current ripple in the inductor necessitates the use of a low pass filter to produce a clean current signal [31]. A first order low pass filter is used to reduce signal noise and the general form of this is seen in (27). In this equation, f_c refers to the cutoff frequency of the filter, the value of which should be lower than the switching frequency of the converter; a frequency of 15 kHz was chosen for the cutoff. The complete equation that should

be used to tune the PI controller is then the combination of the filter and control-to-inductor current equations (28). As with the SRC PI design, bode plot analysis is used to tune controller gains (13)-(15) following the general design approach found in [28], which was previously summarized in section 2.4.1. Again the PI controller is designed around the worst case operating scenario, which corresponds to the operating conditions yielding the largest DC gain. From (28) it is seen that the DC gain is largest when the high side voltage is at its maximum; all other parameters in the equation are static.

$$F(s) = \frac{1}{1 + \frac{s}{2\pi f_c}} \tag{27}$$

$$G_{idF}(s) = \frac{1}{1 + \frac{s}{2\pi f_c}} * \frac{V_H}{L_{bb} * s + R_{L_{bb}} + R_{batt}} \tag{28}$$

3.5.1 Back End Converter PI Design

The frequency response of the filtered control-to-inductor current is shown in Figure 18 for the worst case high side voltage of 80 V. The gain margin for the uncompensated system is infinite as the phase approaches but does not cross 180º, the phase margin is 11.5º, and the DC gain of the response is 75.3 dB. For stable PI design it is desired to reduce the value of the DC gain and increase the phase margin to be greater than 30 º. The value of K_c was chosen to be 0.005 as to reduce the DC gain to below 30 dB and the desired phase margin ϕ_M was chosen to be 70°. The proportional and integral gains were derived via (14) and (15) and the values are summarized in Table 14.

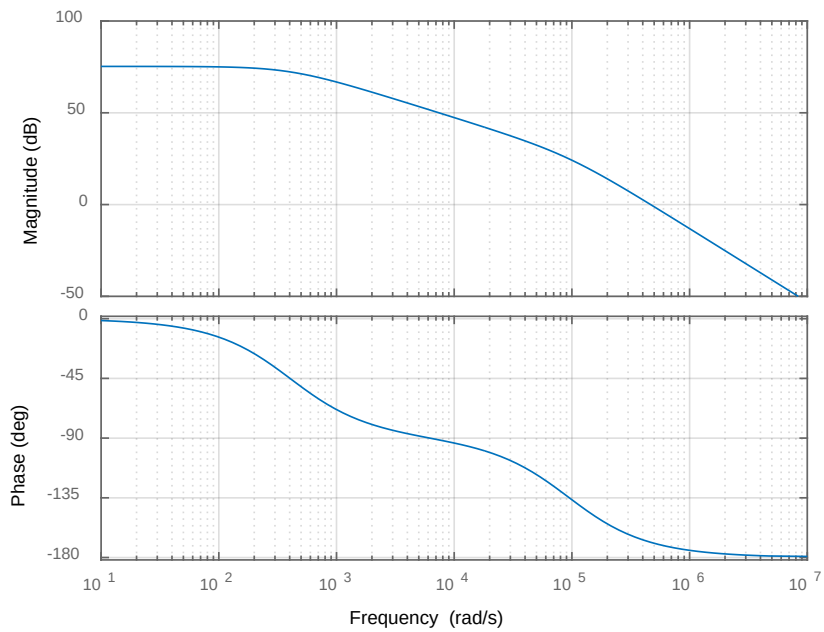


Figure 18. Back Converter Frequency Response of Filtered Control-to-Inductor Current

Table 14. Back Converter PI Gains

DC Gain	K_C	0.005
Proportional Gain	K_P	0.1343
Integral Gain	K_I	358.23

The frequency response of the PI compensated filtered control-to-inductor current equation is shown in Figure 19 and the Nyquist diagram of the system is shown in Figure 20. The gain margin of the compensated system remains infinite, while the new phase margin is 49.7º. The Nyquist diagram confirms stability in that the trace travels from negative infinity to positive infinity, but does not encompass -1.

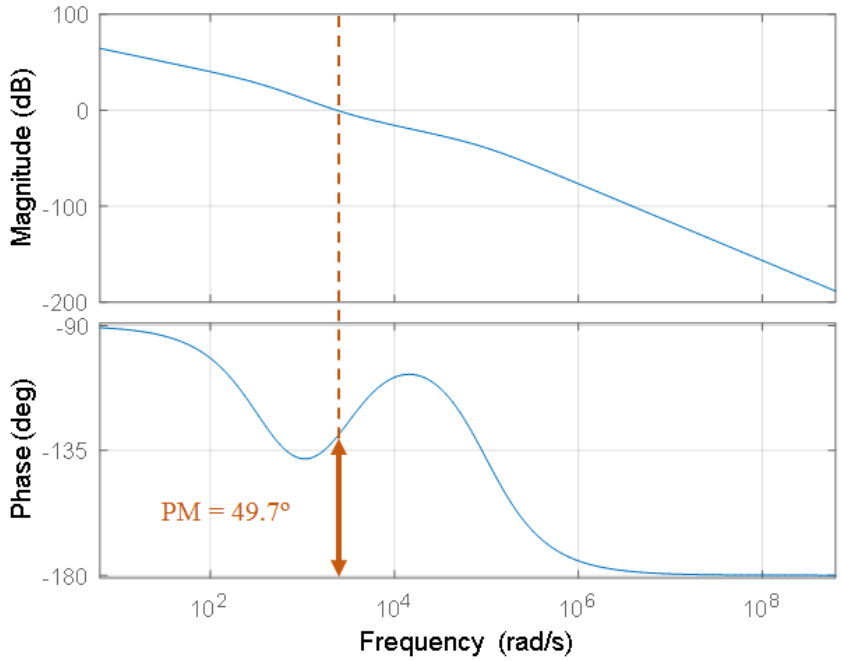


Figure 19. Back Converter Frequency Response of PI Compensated System

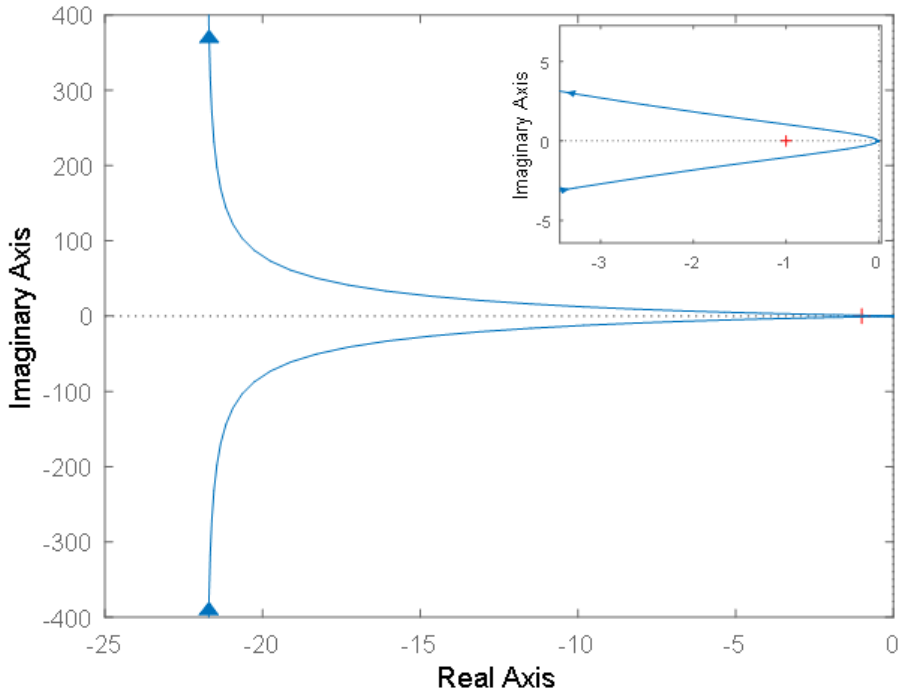


Figure 20. Back Converter Nyquist Diagram of PI Compensated System

3.5.2 Front End Converter PI Design

The front side converter operates for a high side voltage ranging from 90 V to 150 V; hence the worst case scenario occurs for an input voltage of 150 V. The frequency response of the filtered control-to-inductor current is shown in Figure 21. For the uncompensated system, the gain margin is infinite, the phase margin is 9.7 º, and the DC gain of the response is 80.7 dB. The value of K_c was chosen to be 0.002 to reduce the DC gain below 30 dB and the desired phase margin ϕ_M was again chosen to be 70°. PI gains were calculated via (14) and (15) and are summarized in Table 15.

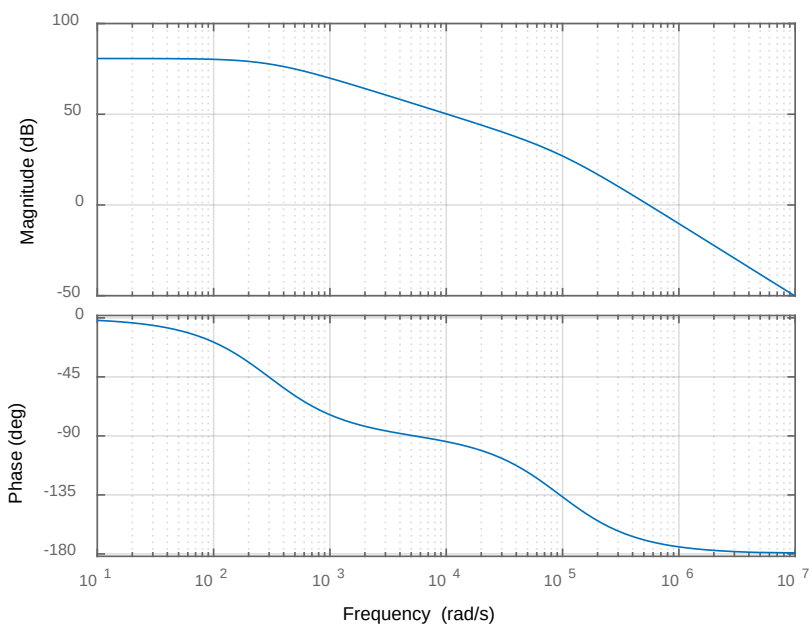


Figure 21. Front Converter Frequency Response of Filtered Control-to-Inductor Current

Table 15. Front Converter PI Gains

DC Gain	K_C	0.002
Proportional Gain	K_P	0.0802
Integral Gain	K_I	211.61

The frequency response and Nyquist diagram of the PI compensated filtered control-to-inductor current equation are shown in Figure 22 and Figure 23, respectively. The gain margin of the compensated system still has infinite value and the new phase margin is 37.8º. The Nyquist diagram again confirms stability showing a negative to positive infinite trace that does not encircle -1.

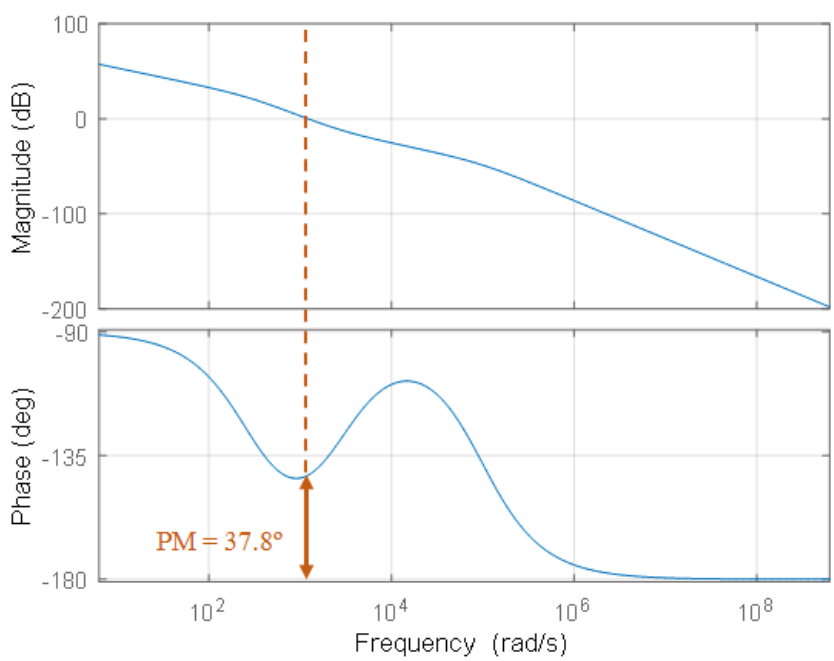


Figure 22. Front Converter Frequency Response of PI Compensated System

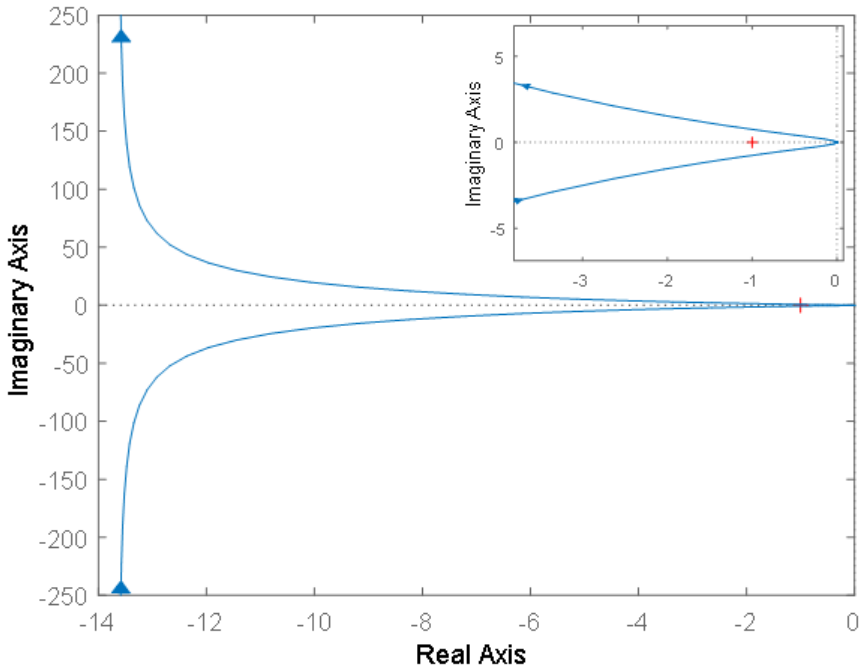


Figure 23. Front Converter Nyquist Diagram of PI Compensated System

3.5.3 Dead Time

Dead time was added to the PWM control signals for both front and back converters to mitigate current shoot through in the semiconductor devices. As before, it is desired to have a dead time of 4% or less of the minimum switching period to maintain expected converter operation. A dead time of 0.5 μs was implemented, which satisfies the desired criterion for the front and back converters.

3.6 SIMULATION AND VERIFICAITON

The front and back two phase buck-boost converters were modeled in Ansys Simplorer to verify circuit operation and correct PI regulation of the battery current during steady state operation. As the converter designs are very similar to each other, only results from the back converter are used to validate the design approach. The verification cases are shown in Table 16 and consist of minimum discharge current for CCM, maximum discharge, and maximum charge scenarios. Duty cycle from the simulation is compared to analytical duty cycle to verify the design. From [31] the equation for the duty cycle of a bidirectional buck-boost converter operating as a battery load converter is shown in (29); note that because the converter has two phases the DC resistance of the inductor must be accounted for twice.

$$D_{expected} = \frac{V_L + I_{L_{BB}}\left(2R_{L_{BB}} + R_{batt}\right)}{V_H} \tag{29}$$

Table 16. Verification Cases for Operation of Back End Converter

Case	Scenario	Duration	I_{ref}	$D_{expected}$
1	Minimum CCM Discharge	0 – 7.5 ms	5 A	0.526
2	Maximum Discharge	7.5 – 15 ms	48 A	0.535
3	Maximum Charge	15 – 22.5 ms	-48 A	0.515

The simulation circuit can be seen in Appendix A section A.2 along with the PI and logic blocks for the operation of the two converters. The low pass filter with the 15 kHz cutoff frequency was implemented as a digital filter on the current signal from the inductance. The back

end converter was simulated at a time step of 50 ns and two simulations were conducted. The first simulation of the tests cases included no dead time in the control and used ideal switches; motivation for this was to have a direct comparison of the simulation to the analytical duty cycles, as dead time and power electronic losses affect this value and are not accounted for in (29). The second simulation included both of the aforementioned parameters. The duty cycles for the idealized simulation and non-idealized simulation, see Figure 24, are summarized in Table 17. Additionally, plots of the per phase inductor current and total inductor current from the non-idealized simulation are shown in Figure 25 and Figure 26, respectively.

Table 17. Verification Simulation Results for Back End Converter

Scenario	**Analytical**	**Idealized Sim**	**Non-Idealized Sim**
	$\mathbf{D_{expected}}$	$\mathbf{D_{idealized}}$	**D**
Minimum CCM Discharge	0.526	0.5259	0.5512
Maximum Discharge	0.535	0.5331	0.5779
Maximum Charge	0.515	0.5168	0.47

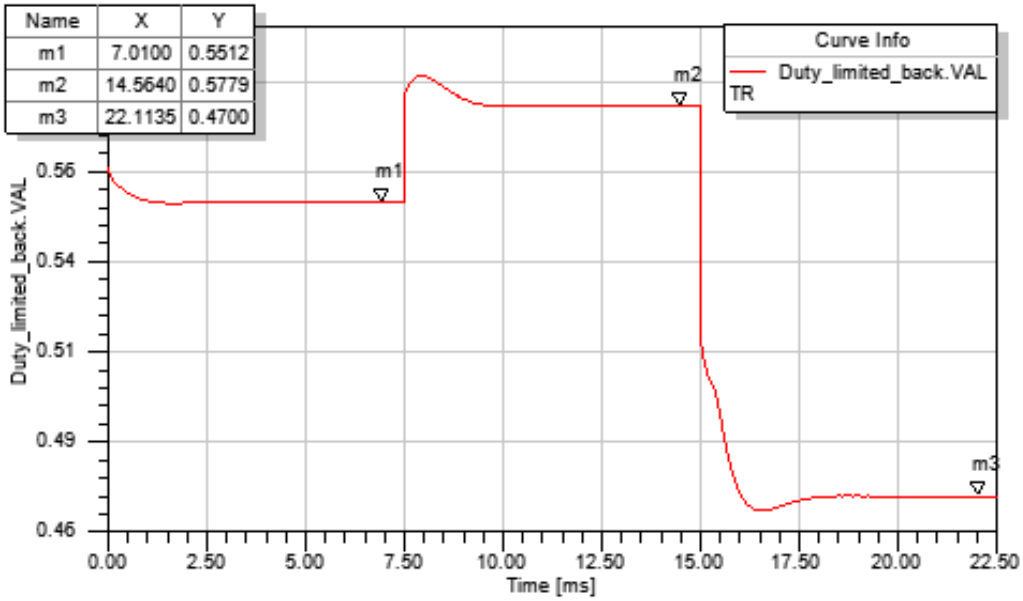


Figure 24. Simulated Non-Idealized Duty Cycle of Back Battery Converter

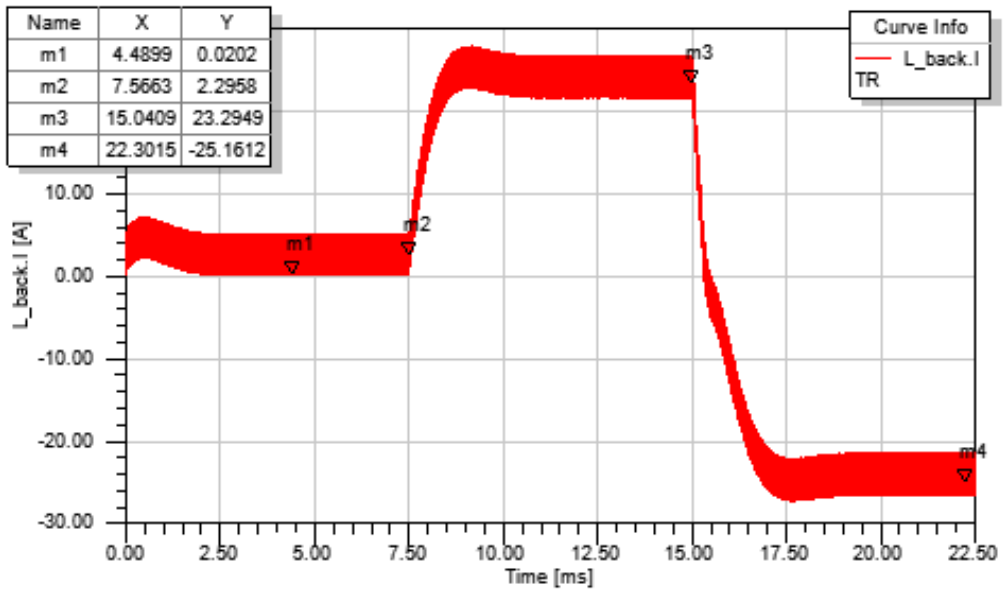


Figure 25. Simulated Non-Idealized Per Phase Inductor Current of Back Battery Converter

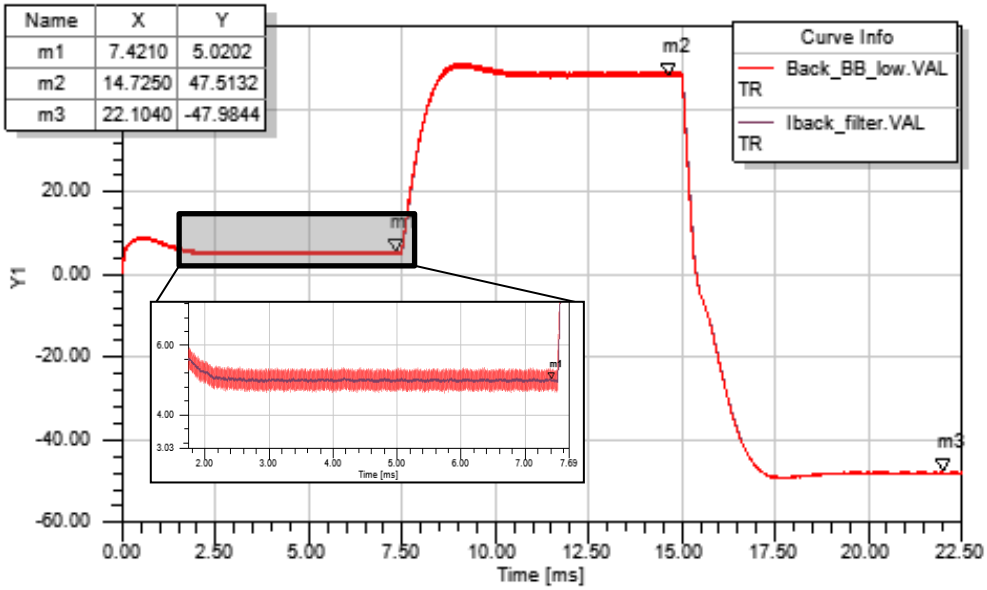


Figure 26. Simulated Non-Idealized Total Inductor Current of Back Battery Converter (red) and Filtered Inductor Current Signal (purple)

Overall there is excellent agreement between the idealized simulated duty cycle and the expected analytical duty cycle. Moreover there is good agreement between the non-idealized simulation duty cycle, though deviations were anticipated as a result of signal dead time and semiconductor losses. From Figure 25 it can be seen that the current in the individual phase is about half of the target current, with values of 2.3 A, 23.3 A, and -25.4, for each of the three cases; the result is expected as current should be split equally between the two phases. Additionally it is seen that CCM operation is satisfied for the first case, with a minimum current in the inductor of 0.02 A. Total inductor current in Figure 26 indicates that the PI controller is correctly regulating current for each case with values of 5.02 A, 47.5 A, and -47.9 A. In the zoomed in section it is seen that the low pass filter signal (purple) adequately filters the current ripple to produce an averaged current signal for the controller. In conclusion, these verification

results indicate that the converters are operating as designed, that the system is stable, and that regulation of the battery current is achieved.

4.0 PHOTOVOLTAIC ARRAY

Photovoltaic generation is used as the primary source of power in this system and with a PV source comes several key characteristics. Firstly its generation is not constant; it is prone to swings in output power as a result of changes in the solar irradiance that the PV array receives. To make up for the intermittency of the power generation, energy storage typically accompanies PV arrays. In addition to variable power, the PV cell is a non-ideal current source and must be interfaced with a converter. As a result, the voltage on the output of the PV converter depends on the amount of load it must supply as well as the maximum power available from the array for the given operating conditions. Finally, the output of the PV array is affected by the temperature of the PV cells, with decreasing output for increasing temperatures. However for the purposes of this research temperature dynamics of the PV array will be ignored as it greatly increases the complexity of the model and is not necessary for the evaluation of this work. Hence the temperature is assumed to have a constant value of 25º C, which is the nominal temperature that PV cells are rated and tested at. The overall design of the PV array includes the circuit model used for the PV cell, parameter values of the PV array, a PV interfacing boost converter, and the implementation of a maximum power point tracking (MPPT) technique as the control for the output of the PV array.

4.1 PV MODEL

The solar array was designed using the single diode model of a PV panel, which consists of a controlled current source, parallel diode, parallel resistance, and series resistance; the circuit diagram for this model is shown in Figure 27. The current source corresponds to the ideal PV current, I_{pv}, and its value is dependent on the amount of irradiance the PV panel receives. From [47] the relationship between ideal PV current, irradiance, and temperature is shown in (30). Note that the second term in the parenthesis accounts for temperature effects and because the nominal temperature is assumed for operation this term is eliminated. Hence the equation is reduced to the ratio of the irradiance, G, to the nominal irradiance, G_n (which has a value of 1000 W/m^2), multiplied by the light generated current, $I_{pv,n}$, which is a parameter unique to the PV panel. The series and parallel resistances are also unique to the PV panel model and have static values. Lastly, the parallel diode is characterized by its thermal voltage, V_T, and nominal saturation current, $I_{0,n}$, the equations of which are shown in (31) and (32), respectively [47].

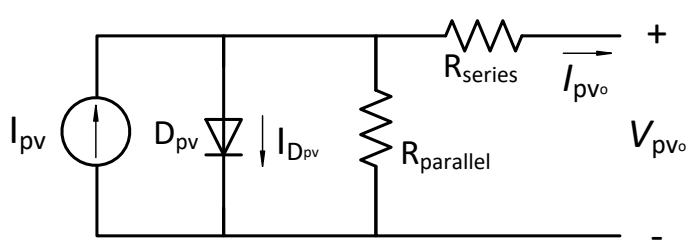


Figure 27. Single Diode Model of a PV Cell

$$I_{pv} = \left(I_{pv,n} + K_I(T - T_n)\right)\frac{G}{G_n} = I_{pv,n}\frac{G}{G_n} \tag{30}$$

$$V_T = a * N_{cells} * \frac{kT}{q} \tag{31}$$

Where a = diode ideality factor, which ranges from ~1 to 2

N_{cells} = number of cells per PV panel

k = Boltzman constant, $1.38065 \cdot 10^{-23}$ $J \cdot K^{-1}$

T = cell temperature, assumed to be a constant 298.15° K

q = electron charge, $1.60217646 \cdot 10^{-19}$ C

$$I_{0,n} = \frac{I_{sc,n}}{e^{\frac{V_{oc,n}}{V_T}} - 1} \tag{32}$$

Where $I_{sc,n}$ = nominal short circuit current diode ideality

$V_{oc,n}$ = nominal open circuit voltage

Matlab/Simulink has a database of manufactured PV panels which provides the unique parameters needed to calculate the values of the single diode model. The PV panel chosen was the Canadian Solar CS6P-260M model and the panel data for nominal irradiance (G_n = 1000 W/m^2) is summarized in Table 18. For this system it was desired to have a PV array with a total power rating of 4 kW. This was achieved by using eight parallel strings with two series connected CS6P-250M panels per string, for a total of 16 panels and a maximum power rating of 4.16 kW.

Table 18. Canadian Solar CS6P-260M Panel Characteristics

Parameter	Variable	Value
Maximum Power (W)	P_{max}	260.34
Cells per panel	N_{cells}	60
Open Circuit Voltage (V)	$V_{oc,n}$	37.8
Short Circuit Current (A)	$I_{sc,n}$	8.99
Voltage at max power (V)	V_{mp}	30.7
Current at max power (A)	I_{mp}	8.48
Light-Generated current (A)	$I_{pv,n}$	9.0105
Diode ideality factor	a	0.98994
Parallel Resistance (Ω)	$R_{parallel}$	411.9585
Series Resistance (Ω)	R_{series}	0.30227

The single diode model parameters were calculated for the 16 panel array and the circuit was built in Simplorer so that the PV model could be evaluated for accuracy. A resistor was attached to the output of the circuit and its resistance was swept from zero to a very large resistance (~100 Ω), simulating short circuit to open circuit conditions, to generate PV and IV curves for the array. The sweep was performed multiple times for irradiance ranging from 100 W/m^2 to 1000 W/m^2; the IV curve for the array is shown in Figure 28. Looking at the upper most orange line, which corresponds to nominal irradiance of 1000 W/m^2, the open circuit voltage is measured to be 76.25 V, which is the expected value. Because the array is made up of two series connected panels, the open circuit voltage of the array should be about twice the open circuit voltage of a single panel, or 75.6 V. Again looking at the upper most orange line, the short circuit current is measured to be 71.97 A. As the array is made up of eight parallel strings, the expected short circuit current of the array is eight times the short circuit current of a single panel, which is 71.92 A.

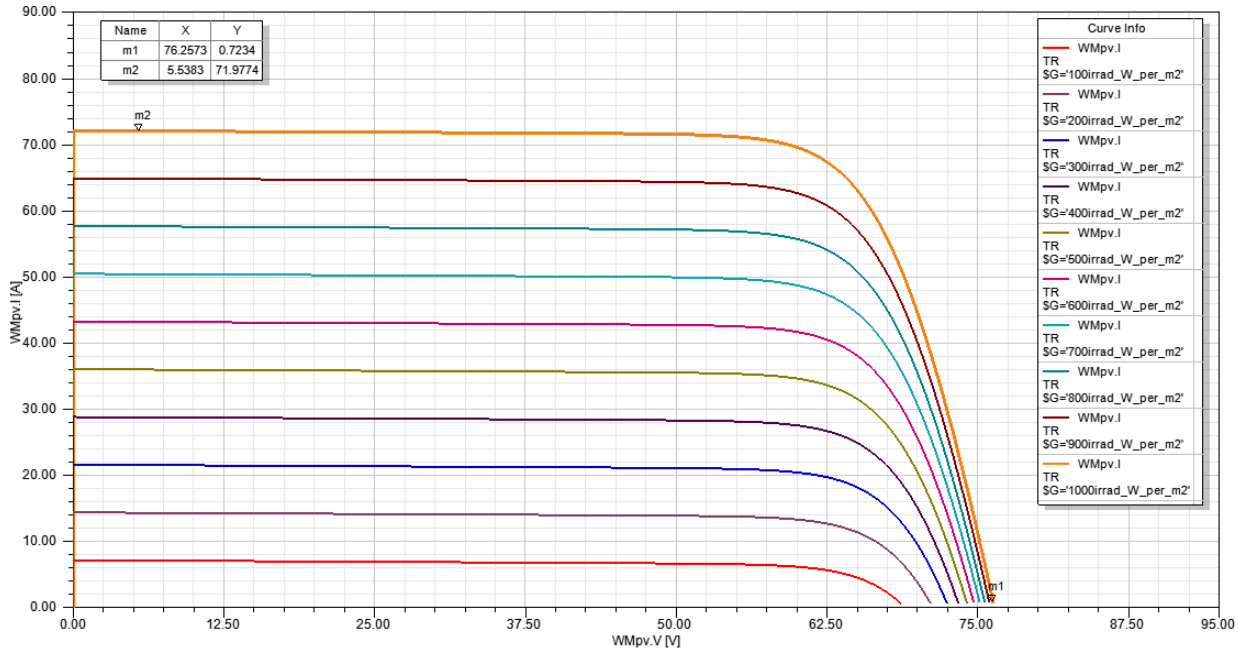


Figure 28. IV Curve of 4.16 kW PV Array for Varying Irradiance

The PV curve for the array is shown in Figure 29. The curves of interest are the top orange curve, middle green curve, and bottom red curve, which correspond to irradiances of 1000 W/m^2 (full power), 500 W/m^2 (half power), and 100 W/m^2 (1/10th power), respectively. The measured maximum power of the top curve is 4.2 kW and corresponds to the full 4.16 kW rating of the array. The max power of the green curve should be about 2.08 kW and is measured at 2.09 kW. Finally the max power of the red curve is expected to be 0.416 kW and is measured to be 0.373 kW.

Both the PV and IV curves of the array show measured values that are close to the expected values and confirm accurate modeling of the PV panel and equivalent PV array. The Simplorer simulation of the single diode model of the PV array and associated math blocks for calculating PV parameters are seen in Appendix A section A.3.

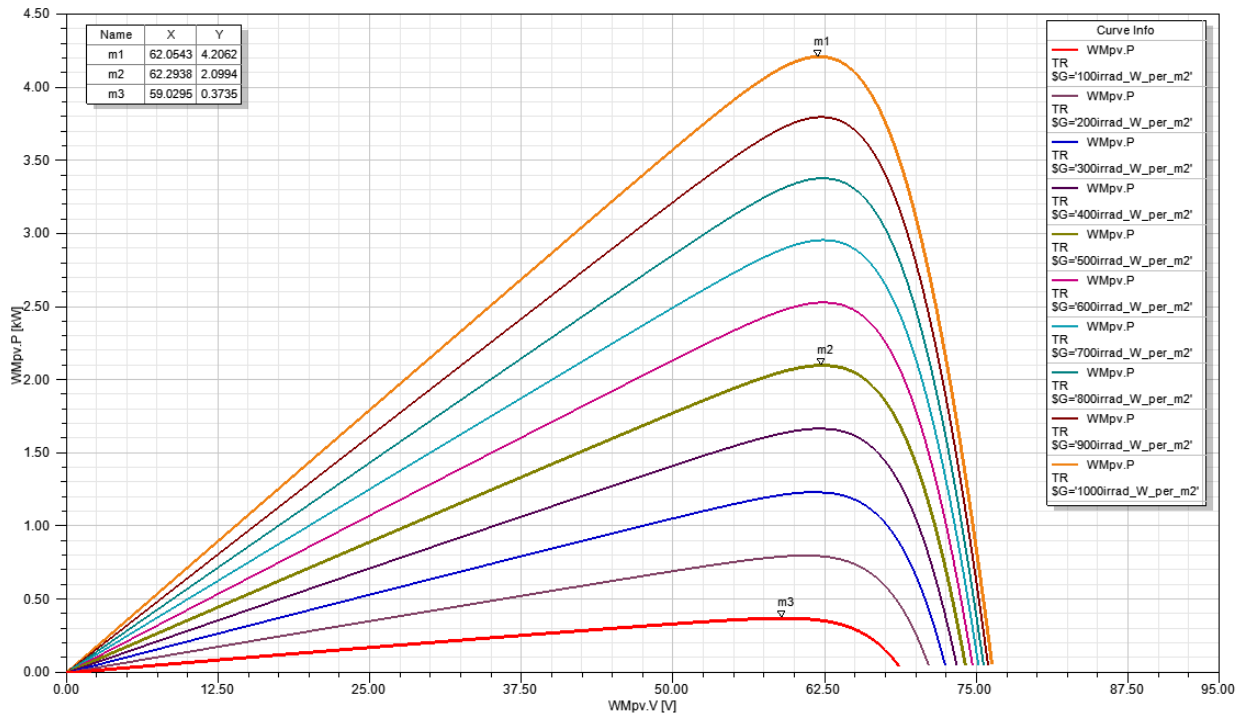


Figure 29. PV Curve of 4.16 kW PV Array for Varying Irradiance

4.2 MAXIMUM POWER POINT TRACKING

To guarantee that the PV array always produces as much power as possible, an algorithm that tracks the maximum power point (MPP) is needed to compensate for changes in operating conditions and the equivalent impedance that the array sees. A variety of power tracking algorithms exists with differing degrees of complexity [48]. One of the most commonly implemented techniques is called the Perturb and Observe (P&O) technique, which is categorized as a hill climbing method. In this method, the algorithm takes the difference between two perturbed power points and compares the resulting slopes of the voltage and current to

determine where on the PV curve the array and array converter are operating at. The changes in power are a result from perturbations in the duty cycle of the array converter. Benefits of this method include simplicity in the algorithm and implementation; however this comes at the cost of accuracy and convergence speed as the algorithm tends to bounce around values very near the maximum power point. The specifics of the algorithm operation are described below and a flow chart of the algorithm is seen in Figure 30.

The algorithm initializes and measures the current and voltage out of the array to compute the PV power output. Delaying the measurements and perturbing the array converter, the algorithm calculates the difference between the power and the voltage during for the time delay. The signs of the power and voltage differences correspond to where on the PV curve the array and array converter are at. For example if the difference in power is positive this means that the converter could be on the left side of the “hill” moving forwards towards the MPP, or on the right side of the “hill” moving backwards to the MPPT. If the voltage difference is positive the former case is true, if the difference is negative the latter case is true. Depending on the outcome of the voltage and power calculations, the algorithm perturbs the duty cycle of the converter either positively or negatively to appropriately move the array towards the maximum power point.

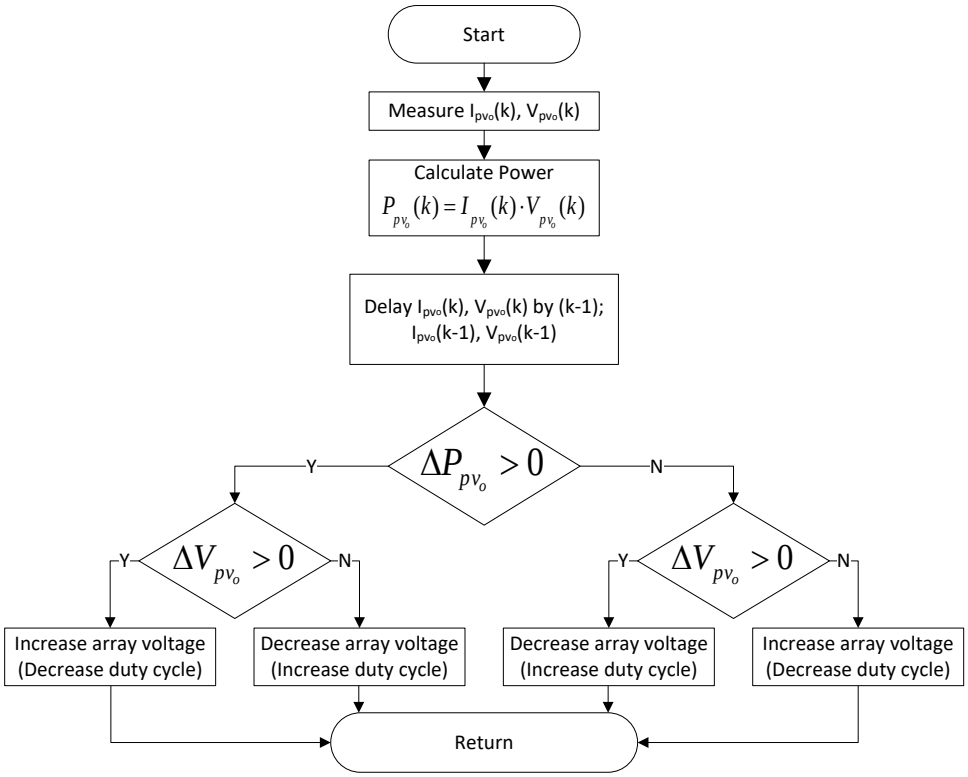


Figure 30. P&O Maximum Power Point Algorithm

4.3 PV ARRAY BOOST CONVERTER

A boost converter was chosen as the PV interfacing converter and connects the output of the PV array to the front end of the SRC. The parameters of the boost converter are summarized in Table 19. The converter is controlled via the P&O algorithm, with incremental adjustments of 0.01 to the duty cycle for each routine of the algorithm. The boost converter and P&O MPPT algorithm were implemented into the PV array Simplorer model to verify max power operation; the circuit and logic are seen in Appendix A section A.4.

The MPPT algorithm was tested for a load resistance of 30 Ω and a nominal irradiance of 1000 W/m^2. Figure 31 shows the array voltage and power as well as the output voltage of the boost converter. For maximum power output array reaches a final voltage and power of 61.84 V and 4.2 kW. Comparing this result with the array sweep simulation in Figure 29, there is excellent agreement with the 1000 W/m^2 (orange curve) maximum power point, which occurs at 62.05 V for 4.2 kW. The duty cycle for maximum power is 0.8283 in Figure 32 and it is seen that the algorithm converges to this value from a starting duty cycle of zero within 200 ms and with minimal ripple in steady state.

Table 19. PV Boost Converter Parameters

Parameter	Variable	Value
Input Capacitance (µF)	C_{boost_in}	250
Inductance (µH)	L_{boost}	50
Output Capacitance (µF)	C_{boost_out}	500
Switching Frequency (kHz)	F_{sw_boost}	88

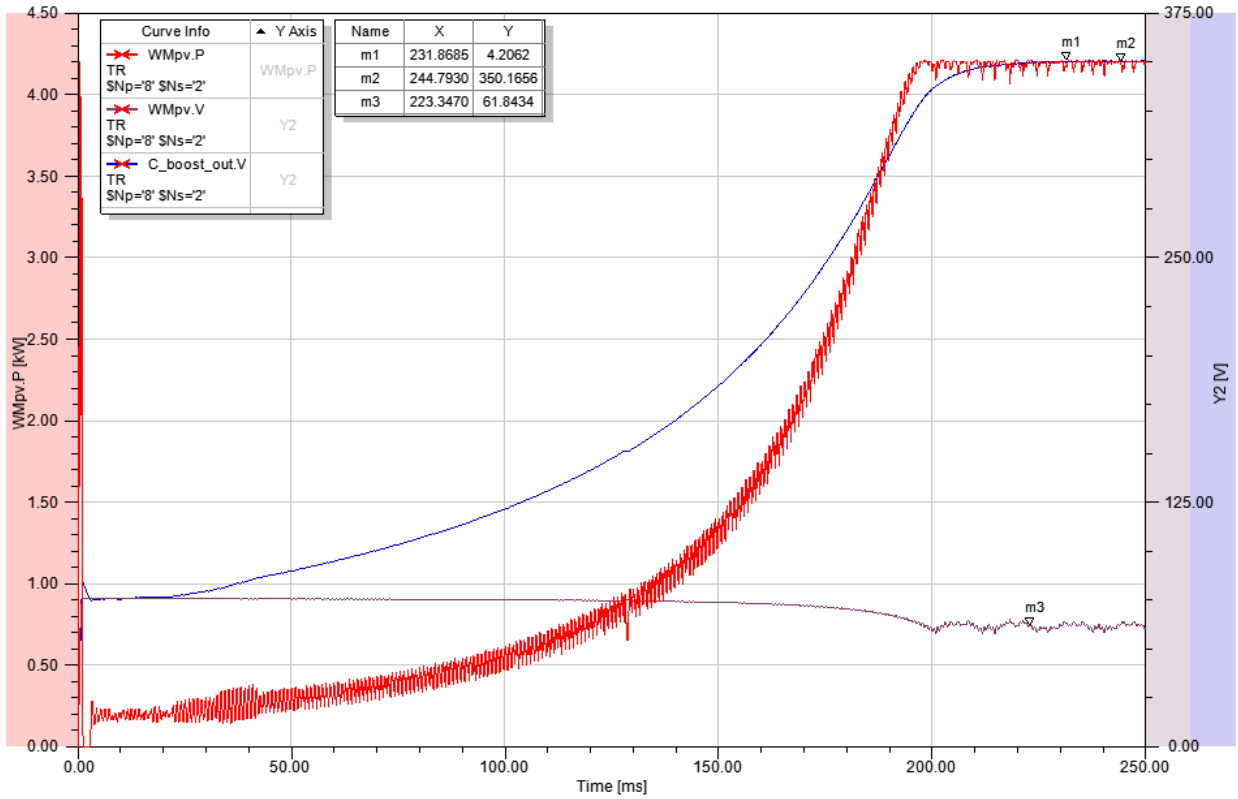


Figure 31. Array Power (Red), Array Voltage (Purple), and Boost Output Voltage (Blue) for MPP Verification

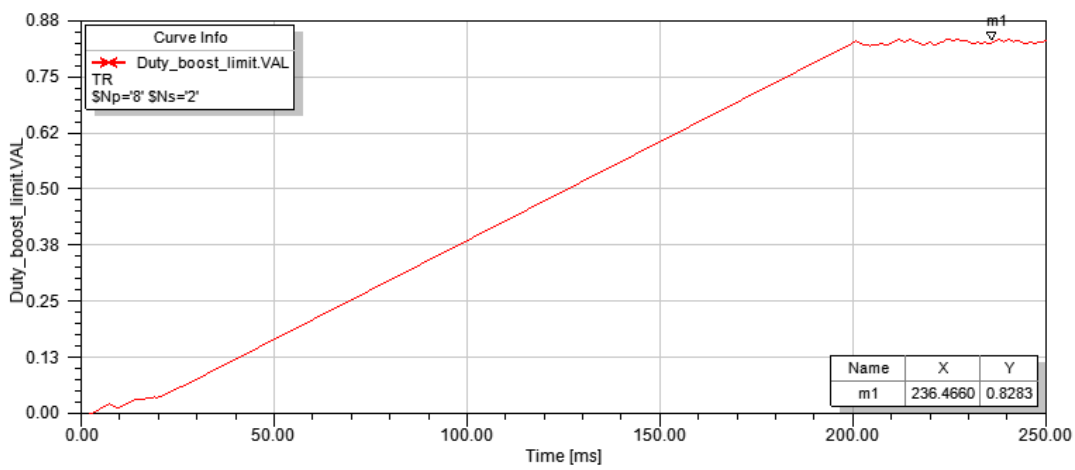


Figure 32. Boost Converter Duty Cycle for MPP Verification

5.0 ASSISTANCE LOGIC

The goal of the assistance algorithm and accompanying logic is to optimize the efficiency of the SRC, which improves overall system efficiency, while providing voltage support capabilities when required. As mentioned before, the efficiency of the SRC can be improved by using the battery as a functional load and either injecting or absorbing current via the front and back battery interfacing converter. The algorithm maximizes performance by perturbing the amount of current flowing to or from the battery and observing the effect this has on SRC efficiency. Using this information the algorithm determines whether an increase or a decrease in assistance will further improve performance and takes the appropriate action. From a system wide perspective this layer of logic is the slowest as it responds to changes in operating conditions, such as irradiance, as well as changes in SRC efficiency, both of which have slow dynamics compared to the rest of the system. Overall the control layers of the system can be categorized into three tiers, based on their switching speeds and functional objectives; the three layers are summarized in Table 20. In practical application the tertiary control may have to be slower than 40 Hz to meet current ramp rate constraints associated with the battery, however for this research the speed is sufficient. In depth discussion of the front and back algorithm assistance logic as well as the performance impacts of current transfer via the front and back converters are detailed below.

Table 20. System Control Layers

Level	Controller	Frequency	Objective
Primary	SRC Control	200-240 kHz	Tight regulation of the load voltage
Secondary	Battery Converter Control	62-63 kHz	Current transfer to and from battery
Tertiary	Algorithm Control	40 Hz	Optimization of efficiency; voltage support

5.1 FRONT ASSISTANCE LOGIC

As discussed in the SRC performance section, current transfer via the front end converter results in changes to the input voltage of the SRC. This is a result of the non-ideal source, as increased load on the PV array yields a lower output voltage from the array converter and thus a lower voltage into the SRC converter. From the profile of the performance curves in Figure 13, maximization of the SRC efficiency is then achieved by reducing the input voltage as much as possible. This is equivalently realized by using the battery as a functional load and charging the battery off of the front end. There are some limiting factors with this operation however, firstly the battery can only be charged if excess power from the PV array exists. Secondly it is paramount that the front end does not charge the battery to the extent that there is not sufficient power for the critical SRC load.

With these considerations in mind the algorithm logic for the front end was developed and can be seen in Figure 33. The algorithm works by recording the efficiency of the SRC and

the last known current reference set point from the front PI controller. Then the algorithm perturbs the reference current set point and compares the difference in the signs of the efficiency and current set point to determine if an improvement was made and whether perturbations in the same direction should be continued. To illustrate the operation of this logic, two examples, representing the two outside branches of the algorithm, are depicted on SRC performance curves in Figure 34.

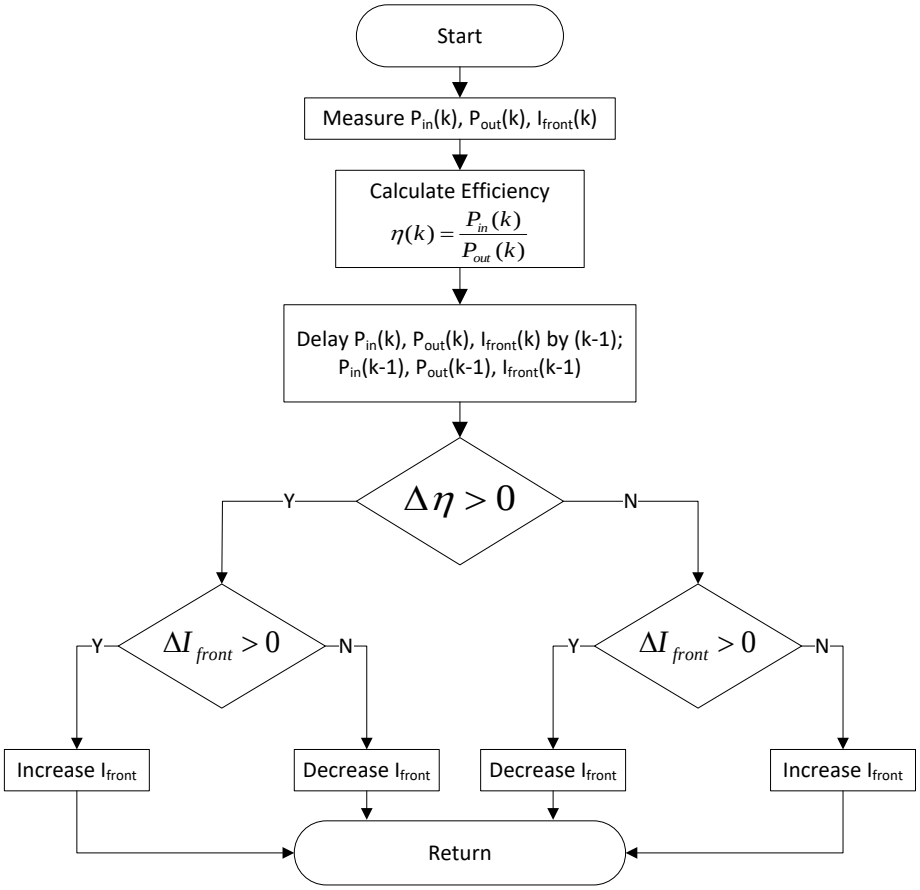


Figure 33. Front Assistance Algorithm Logic

The scenario on the right side of Figure 34, which corresponds to the left most branch of the front algorithm, shows an example where the SRC load is around 2100 W and PV array produces excess power. The algorithm perturbs the current set point to a higher value, increasing battery load (reducing input voltage) and consequently improving efficiency. As efficiency improved with a higher current set point, the algorithm would continue to increase current for the next perturbation. Note that positive current corresponds to charging the battery, adding additional battery load. The scenario on the left side of the graph, corresponding to the right most branch of the algorithm, depicts a scenario where the load is around 700 W with excess array power available. The algorithm decreases the current set point, reducing battery load, increasing front end voltage and thus reducing SRC efficiency. As the result of this perturbation was not desirable, in the next cycle the algorithm would reverse its direction and increase the set point to reduce voltage and improve efficiency.

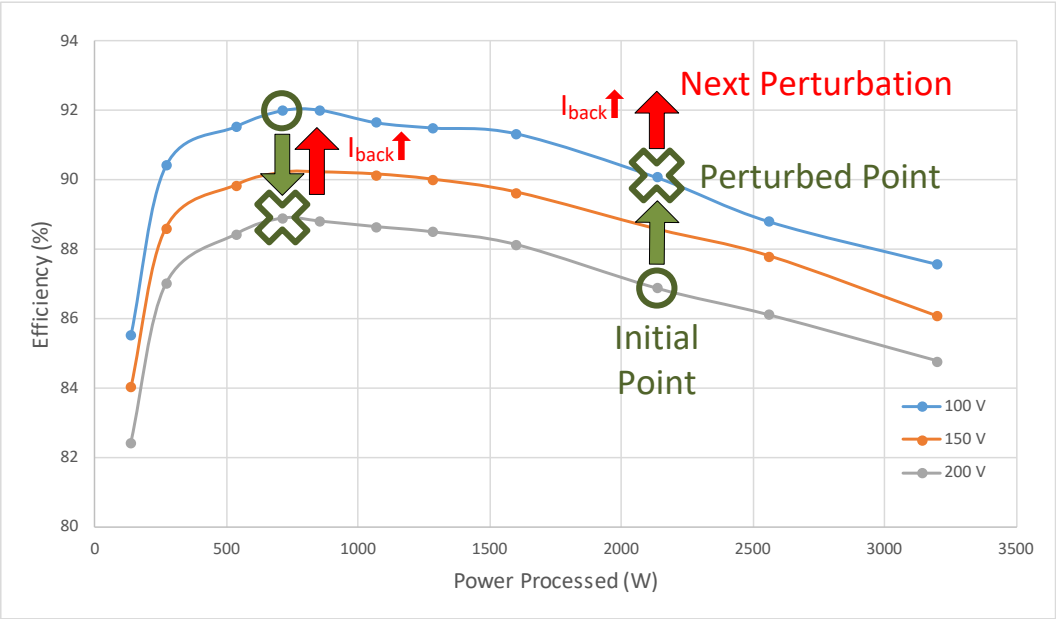


Figure 34. Example Operation of Front Assist Algorithm

The two inside branches of the algorithm represent scenarios that are not easily depicted on the performance curve. These correspond to scenario where the input voltage is decreased however efficiency is not improved and vice versa. For the scenarios in Figure 34, the example perturbations result in changes of +/- 50 V to the input voltage, however in actuality the simulation perturbations are significantly smaller and may not always result in the expected efficiency improvements for decreasing voltage. One such operating point can be seen in Figure 13; for an SRC load of 2100 W the efficiency is higher for the 100 V input than the 90 V input. Generally, however, it is expected that charging the battery off of the front end (reducing input voltage) improves the SRC efficiency.

5.2 BACK ASSISTANCE LOGIC

Current transfer with the battery via the back end converter impacts the SRC performance by adjusting the effective load seen by the SRC. From Figure 13 the maximum efficiency exists somewhere in the middle of the hill shaped profile, with the specific optimal load point dependent on the input voltage to the SRC. To move the SRC operating point towards the high performing middle region of the load profile, the battery is used as a functional load (for light SRC load) or as a source (for heavy SRC load) to adjust the effective load the SRC sees.

As with the front end operation there are limiting factors that must be considered, namely that use of the battery as a load can only be done when excess power is available from the PV array. Additionally the battery load should not exceed the power demands of the source such that the main SRC load is not sufficiently powered. A final consideration that is unique to the back end is that, in additional to shifting the effective load of the SRC, the battery can also affect the

input voltage to the SRC, depending on whether the input source to the system is strong or weak. For a strong input source the additional loading or sourcing of the battery should not affect input voltage to the SRC, resulting in only a shift of the operating point along its performance curve for the given input voltage. However for a weak (non-ideal) source, the impact of the battery will not only shift the effective load of the SRC but the input voltage to the SRC as well, similar to the manner in which the front end affects voltage.

Keeping these factors in mind, the algorithm logic for the back end was developed and is seen in Figure 35. The algorithm's operation is as follows: it records the efficiency and the power out of the SRC and then perturbs the current reference set point of the PI controller for the back end converter, calculating the change in sign of the output power and efficiency. Results of the sign changes dictate which direction to move the effective load of the SRC for optimal performance. Scenarios for the operation of the back end algorithm for both strong and weak sources are detailed below.

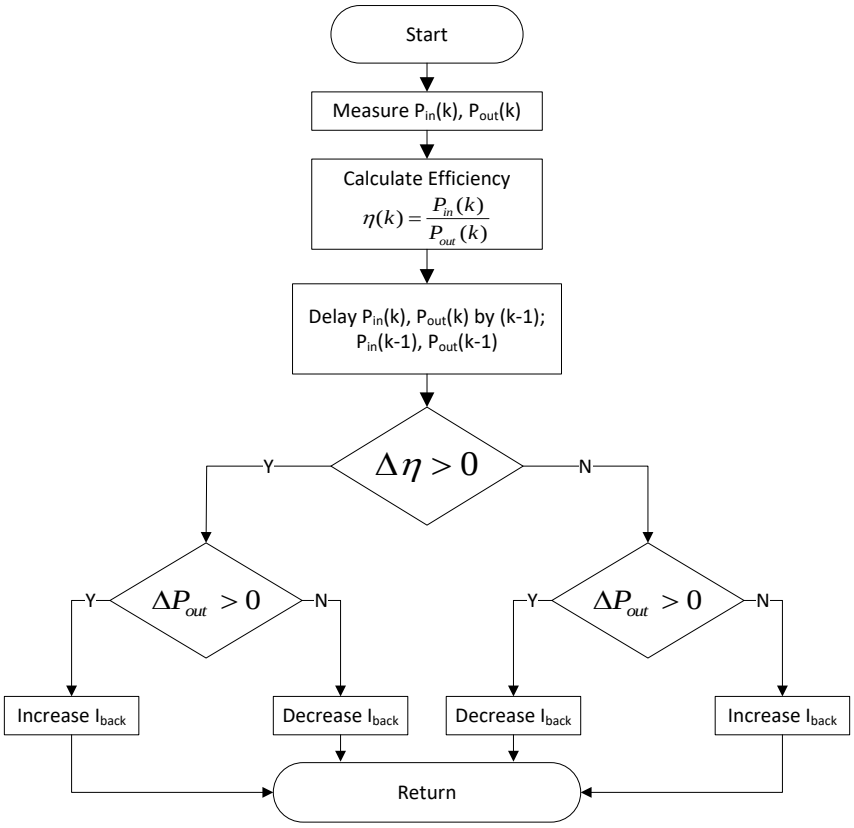


Figure 35. Back Assistance Algorithm Logic

5.2.1 Strong (Ideal) Source

The four possible outcomes for the back end algorithm are illustrated on the SRC performance curve in Figure 36. Examining the scenario on the right most side, which corresponds to the left most branch of the algorithm, it is seen that the converter operates under heavy load, supplying 3200 W. The algorithm discharges battery current to the load, reducing the effective load of the SRC and improving performance. For the next perturbation the algorithm

discharges additional current to the load to further improve efficiency. Note that negative current corresponds to discharging the battery.

The scenario on the left most side shows the SRC operating under a light 250 W load and corresponds to the right most branch of the algorithm. The algorithm charges the battery to increase the load that the SRC sees which improves performance. For the next perturbation the algorithm continues to charge the battery, adding additional battery load and moving the SRC closer to the optimal operating point.

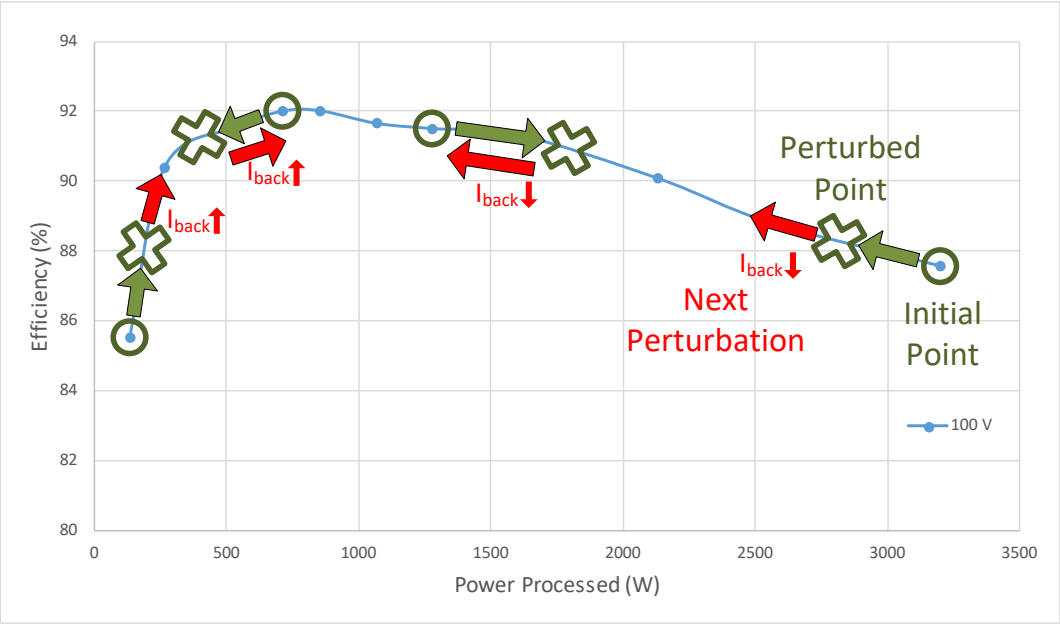


Figure 36. Example Operation of the Back Assist Algorithm with a Strong Source

The two middle scenarios on the curve correspond to the middle branches of the back end algorithm. These represent scenarios where the algorithm perturbs the current set point such that the SRC moves away from the optimal performance point, either by reducing the battery load

under light load conditions or by reducing the battery source under heavy load conditions. In both cases the algorithm recognizes the undesired result and reverses its perturbation direction to bring the SRC back towards the peak of the performance curve. From these examples, two performance trends are observed: firstly, that for light load adding additional load by charging the battery improves SRC performance and secondly, that for heavy load reducing the effective load of the SRC by discharging the battery (sourcing current) improves SRC performance.

5.2.2 Weak (Non-ideal) Source

The performance of the SRC with the back end algorithm for a weak non-ideal source, which is the source used in this research, is shown in Figure 37. Now when shifting the effective load of the SRC the effective load that the PV array sees also shifts ,resulting in changes to the input voltage to the SRC. For the light load scenario (left side of the plot), the operation of the algorithm is unchanged, as adding additional battery serves to increase the effective SRC load and increase the effective load of the PV array, which reduces the array converter output voltage (SRC input voltage). The resulting efficiency improvement is twofold as the SRC benefits from both the increased load as well as the lower input voltage.

However for the heavy loading scenario the non-ideal source creates some contradicting dynamics. From a SRC load perspective it is desired to reduce the effective load of the converter to shift the SRC towards the middle of the performance curve to operate at peak efficiency. Yet sourcing battery current to the back end of the SRC means less current is needed from the PV array, which results in an elevated output voltage front array converter. Thus the benefits of the load shift may be overshadowed by the negative impacts of the voltage shift, resulting in a negative net decrease in efficiency. Such a scenario is illustrated on the right hand side of Figure

37. After perturbing the back end current to reduce SRC effective load, the algorithm sees a decrease in efficiency and so it reverses its direction for the next perturbation; this result is undesirable as the shift is not towards the peak SRC efficiency. One way to overcome these opposing interactions is use both the front and back algorithms simultaneously when confronted with a heavy loading situation, which is discussed in the following section.

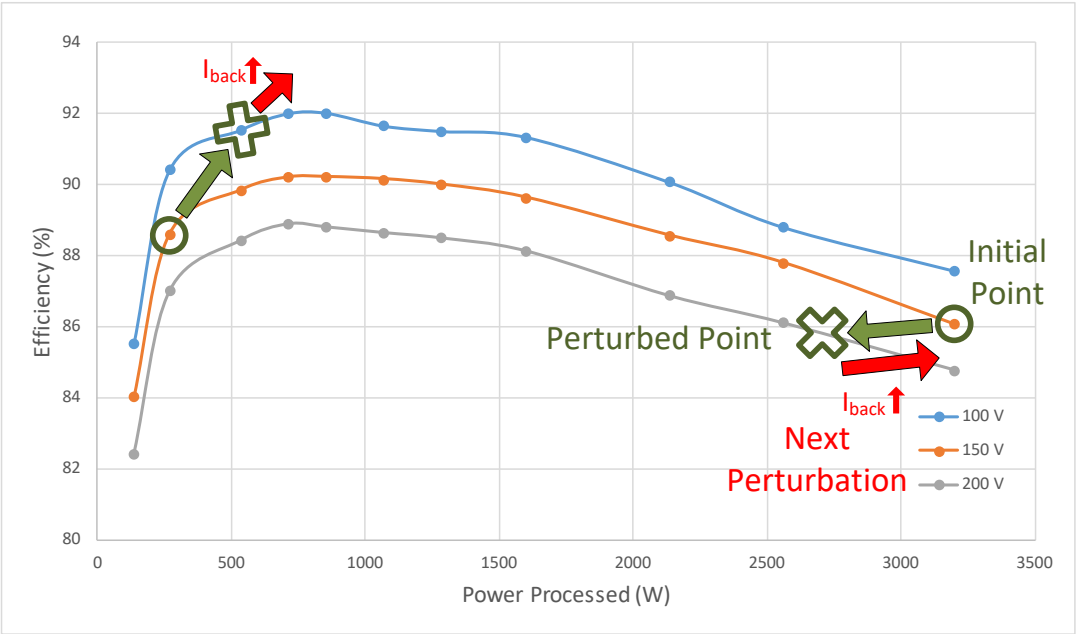


Figure 37. Example Operation of the Back Assist Algorithm with a Weak Source

5.3 DUAL ASSISTANCE

Using the two algorithms in a simultaneous manner allows for the front end algorithm to offset the negative dynamics resulting from the back end algorithm under heavy loading, namely the elevated input voltage. By adding battery load (charging the battery) on the front end that is greater or equal to the battery current discharged to the back end, the net result is that the SRC effective load is shifted as desired, the SRC efficiency improves, and the battery is charged.

For example in Figure 38, if the SRC is feeding 3200 W of load and the array generates a total of 3700 W for an SRC input voltage of 150 V, there is a net excess power of 500 W and the SRC operates under heavy load. In this case the back end algorithm reduces the effective load of the SRC by discharging 2000 W (the max power rating of the back converter) to the load, shifting the operating point to the middle of the profile, while the front algorithm accordingly charges the battery with 2500 W, offsetting the back end discharge and absorbing the excess power generated from the PV array. The battery receives an effective charge of 500 W and the input voltage to the SRC should be at or lower than the initial operating voltage, as the excess PV power is now being absorbed by the battery, suggesting an improved operating point within the boxed region.

The combined front and back assistance algorithms can be seen in Figure 39, where yellow corresponds to the front algorithm and purple corresponds to the back. Simultaneous assistance occurs only under heavy load for the reasons mentioned above, while sequential assistance occurs for light load, with the back algorithm operating first. With sequential assistance once the back algorithm has determined the optimal load for the given operating conditions, the front algorithm can initialize and absorb remaining power if any exists. In the case where there is no remaining power available for the front end or not enough power to meet

the optimal load in the first place, then only the back algorithm operates, bringing the SRC as close to optimal load as possible. The dual assistance logic modeled in Simplorer is shown in Appendix A section A.5.

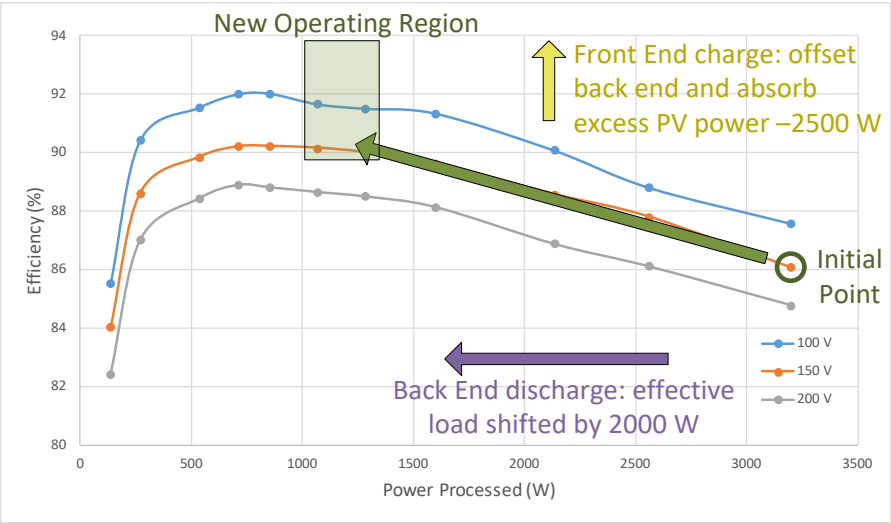


Figure 38. Example Operation of Dual Assistance for Heavy Loading and a Weak Source

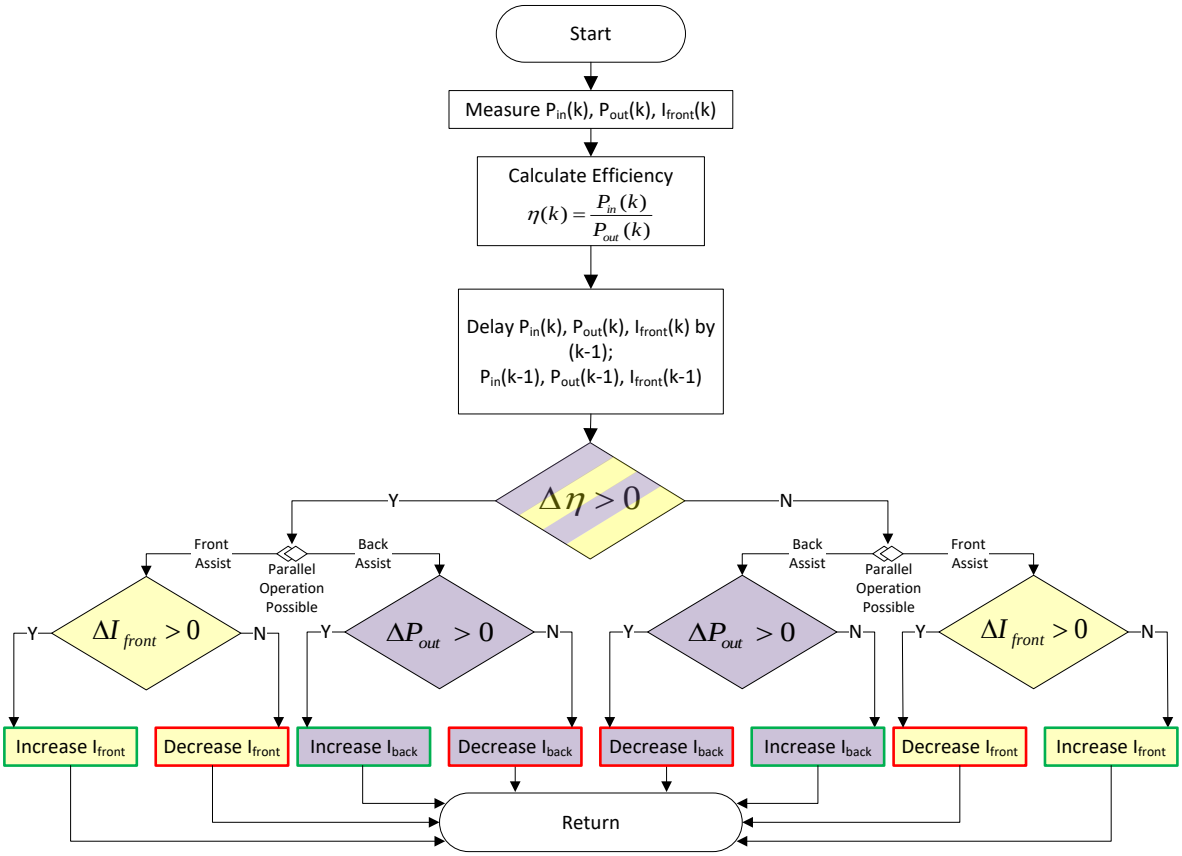


Figure 39. Dual Assistance Algorithm Logic

5.4 SUPPLEMENTARY ALGORITHM FEATURES

In addition to the assistance algorithm, supplementary logic was developed to provide ancillary features, such as peak efficiency identification and voltage support. The peak efficiency logic serves to identify when the algorithm has achieved optimal performance or the best possible performance for the given operating conditions. Once max efficiency is identified the logic reduces the perturbation step size to allow the algorithm to more precisely hone in on the peak

efficiency. The voltage support logic provides the means to switch the algorithm from peak efficiency mode to voltage support mode, in which the battery discharges current to maintain either the critical load voltage or the front end voltage, in the case of PV drop out or converter failure.

5.4.1 Efficiency Peak Identification

The peak efficiency identification (EPI) logic has two different tests, one longer term and one shorter term, which it conducts to determine if optimal efficiency is reached. The longer term check measures the efficiency every 4th tertiary cycle and compares the absolute value of the difference in efficiency. If this value is greater than the user defined threshold then the logic trips, which restarts the EPI logic. Essentially this check verifies that the longer term efficiency does not differ significantly from the efficiency range that the SRC was in four cycles ago. If this logic passes then it suggests that the SRC is in the peak efficiency range.

The shorter term check compares the efficiency difference for each tertiary cycle against the user defined threshold. If the difference in efficiency exceeds this threshold then the EPI logic trips and restarts. However if the difference in efficiency does not exceed the threshold for four consecutive tertiary cycles, then the short term logic passes. Essentially this test checks that the SRC efficiency does not increase too rapidly, as significant jumps in SRC efficiency occur when the converter is in sub-optimal performance, far from peak efficiency. As optimal efficiency is approached, the change in SRC efficiency between cycles reduces significantly. For the EPI logic to pass, both the long term and short term checks must be satisfied, in which case the perturbation sizes of the front and back algorithms are reduced and the EPI logic restarts. EPI logic continues reducing perturbation step size down to a user defined minimum.

An example illustrating the EPI and perturbation step size reduction can be seen in Figure 40 and the user defined parameters for efficiency thresholds and step size reductions are listed in Table 21. In the example scenario, the SRC powers light load and additional battery load is added via the back end converter to improve performance. Both the long term and short term efficiency phenomena discussed earlier are visible in the bottom plot, with large efficiency changes for operation far from peak performance and reduced efficiency changes as the optimal value is approached. Also of note: as the algorithm hovers around the optimal performance point the dips in efficiency reflect the overshoot and undershoot of the back end current as the algorithm attempts to converge to the optimal current value. While the algorithm oscillates around the desired current value, both the long and short term EPI tests pass and the current step size is reduced, decreasing the overshoot and undershoot of the algorithm. A second EPI pass soon follows and the SRC efficiency has essentially converged to the optimal value for this scenario. The EPI logic modeled in Simplorer can be seen in Appendix A section A.6.

Table 21. Example Efficiency and Perturbation Thresholds for EPI Operation

	Initial	**During EPI reduction**	**Final**
Efficiency Threshold	0.05 %	$\frac{0.05}{X}$ %	0.0025 %
Perturbation Step Size	1 A	$\frac{1}{X}$ A	0.25 A
Perturbation Factor	1	X For values from 1 to 4, incrementing for each successful EPI pass	4

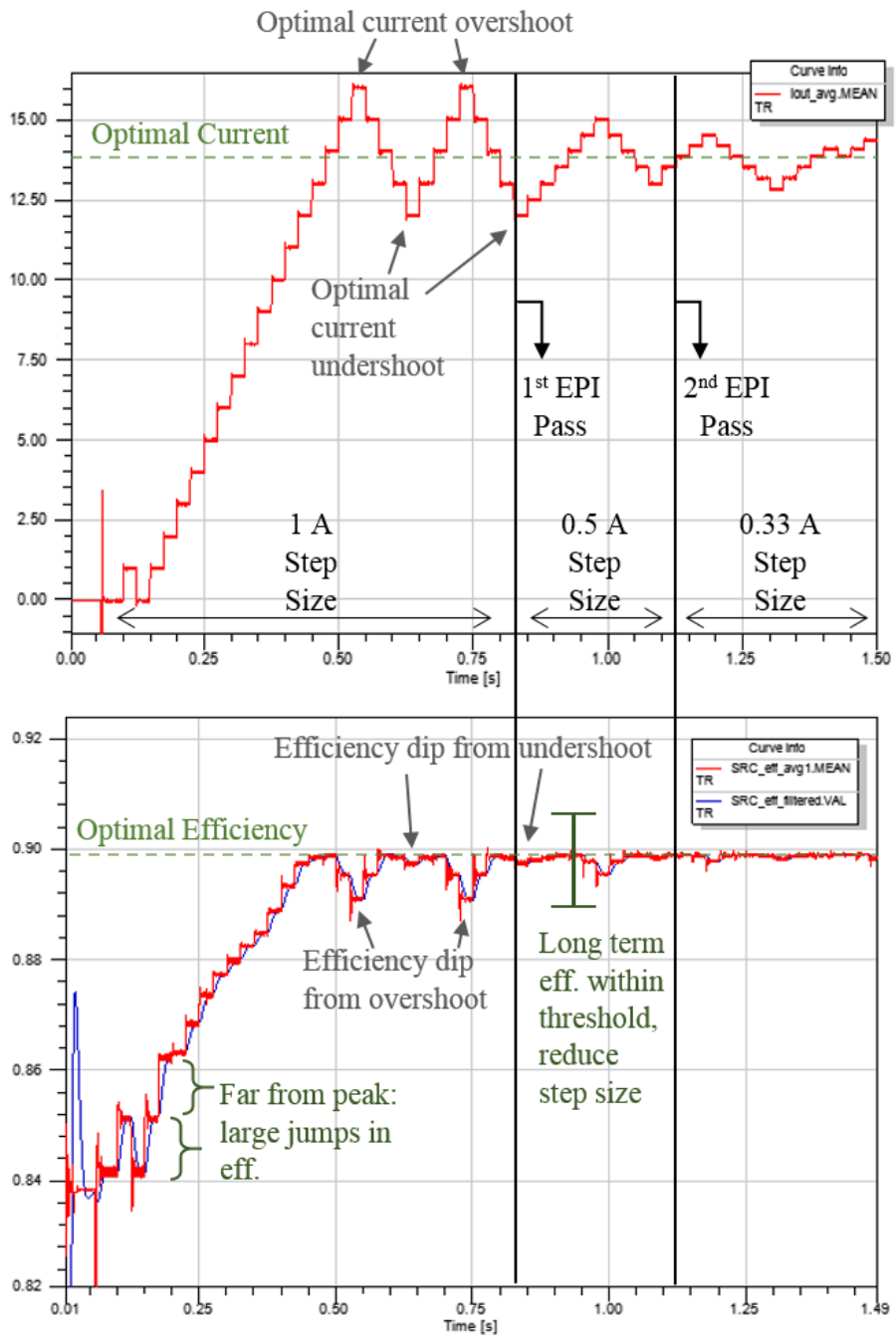


Figure 40. Example of EPI Operation Showing Back End Current (top) and SRC Efficiency (bottom)

5.4.2 Voltage Support

The voltage support feature is implemented using cutoff thresholds to identify when the voltage collapses, either as a result of PV drop out or converter failure. The front and back voltage thresholds will differ depending on system design and nominal operating parameters. For the back end of this system it is desired to maintain the load voltage at 80 VDC, so the lowest allowable voltage was set to be 77.5 V, which corresponds to 97% of the target voltage. For the front end of this system, the lowest acceptable front end voltage is determined by the conversion ratio of the SRC converter. For an ideal SRC the maximum conversion ratio is 1, thus to maintain the target load voltage of 80 V, the front end voltage must also be at least 80 V. However realistically there are losses in conversion process so the practical conversion ratio is <1, with the exact ratio dependent on the amount of SRC losses for the given operating conditions. For a reasonable safety margin it is assumed the converter achieves at least 85% efficiency, thus a margin of 1.15 should be factored into the ideal front end voltage limit of 80 V, for a lowest cut off limit of ~92 V. In a situation where either the front or back end trips the voltage cutoff, the algorithm automatically switches to voltage support mode and discharges battery current to whichever end has collapsed. The algorithm increments the magnitude of discharged current for each tertiary cycle until voltage is restored to a level above the violated voltage cutoff.

6.0 RESULTS

With all individual converter operation verified and the assistance logic developed, the entire system was built in Simplorer to verify the effectiveness of the assistance algorithm in an isolated system setting; the modeled system can be seen in Appendix A section A.7. Three test cases were conducted to verify the ability of the algorithm to optimize SRC performance and are as follows:

(1) Light Load: presents a scenario where the SRC powers light load and the PV array generates excess power. This tests the ability of the algorithm to optimize the SRC performance utilizing the back end converter.

(2) Heavy Load: presents a scenario where the SRC powers heavy load and the PV array generates excess power. This tests the ability of the algorithm to operate both the front and back algorithms simultaneously to successfully optimize SRC performance.

(3) PV Dropout: presents a scenario where the SRC powers light load and the PV array generates excess power. As the algorithm attempts to optimize SRC performance, solar irradiance drops significantly, simulating cloud coverage, which results in a deficit of generated power and a loss of load voltage. This tests the ability of the algorithm to transition from optimization mode to voltage support mode.

For all simulations a time step of 50 ns was used. The Nyquist Sampling Theorem states that the minimum sampling frequency must be twice that of the fastest frequency of the signals

to be measured. The fastest frequency is 240 kHz which corresponds to the maximum switching frequency of the SRC; thus the minimum time step allowable is 2.08 μs. However a greater fidelity was desired to accurately measure SRC efficiency. It was chosen to have 100 data points for each period of the 200 kHz resonant frequency, which corresponds to a time step of 50 ns.

6.1 LIGHT LOAD TEST CASE

Initially the PV array receives irradiance of 400 W/m^2 for an output of ~1.66 kW and the SRC powers 256 W of load, resulting in 1410 W of excess power generated. The excess power contributes to a large front input voltage which results sub-optimal performance and poor SRC efficiency. The assistance algorithm initializes at 200 ms; as this is a light load scenario the assistance initializes sequentially starting with the back end first. The algorithm tracks SRC efficiency and optimizes performance by charging the battery off the back end as to increase the effective load of the SRC and reduce input voltage. The algorithm achieves optimized performance by 1150 ms.

The PV array output power and PV converter output voltage (SRC input voltage) are shown in Figure 41 in red and navy blue, respectively. Marker 1 (m1) shows the 1.66 kW PV array output for the given irradiance. Note that the variations in the measured power from 50 ms to about 400 ms are a result of the elevated input voltage. When the P&O algorithm perturbs the duty cycle of the array converter, it is perturbing the conversion ratio of converter. Because a large conversion ratio is required of the boost converter during this time period, the small changes to the conversion ratio have an amplified impact on the PV array voltage, which directly affects the operating point of the PV array and consequently the PV array output power. Marker

2 (m2) shows that the final input voltage into the SRC is 118 V. Note that the excess generated power and elevated input voltage at start up are a result of the SRC and PV array initializing for the given conditions, moreover the assistance algorithm cannot initialize during the steep start up transients present in the first 150 ms of simulation.

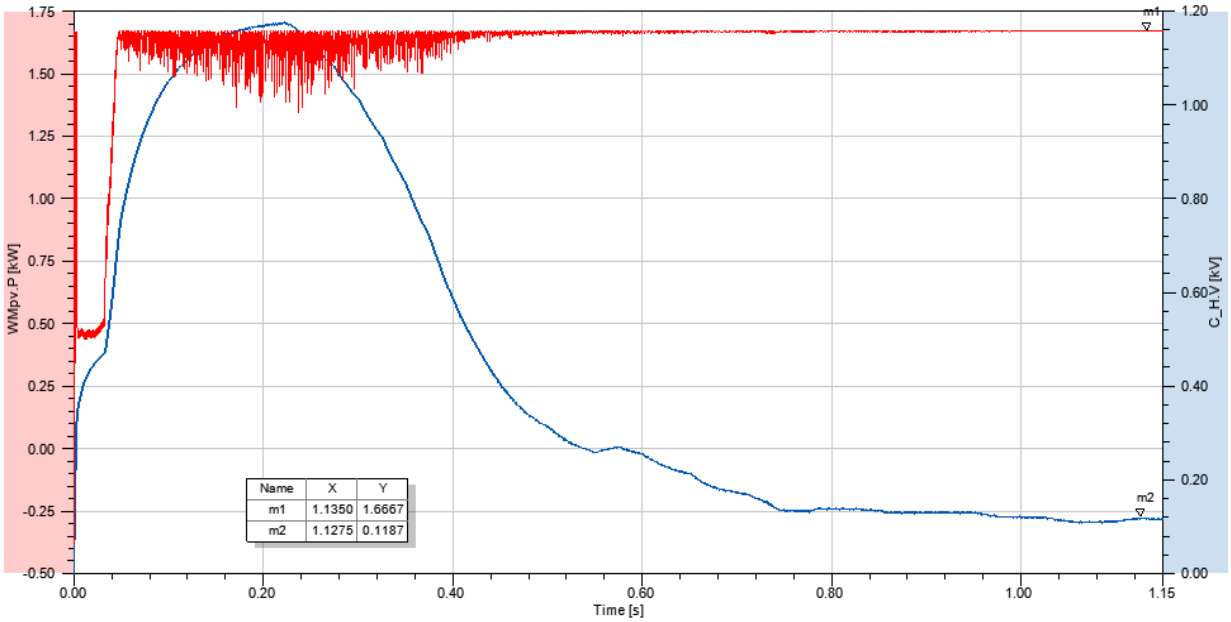


Figure 41. PV Array Output Power (red) and PV Converter Output Voltage (navy) during Light Load Test

The load voltage and SRC efficiency are shown in Figure 42, in orange and light blue, respectively. From the graph it can be seen that the voltage is tightly maintained at 80 V for the duration of the simulation. As for the efficiency, it initially starts around ~16% when the algorithm initializes, with the poor performance resulting from the elevated input voltage.

However with back assistance, the algorithm reaches a peak efficiency of 90.17% for the given system conditions.

Figure 43 shows the amount power transferred from the back end of the SRC to the battery via the back end converter. For the final SRC efficiency of 90.17% an additional 1236 W of battery load was added to the back end of the SRC, which corresponds to about 28 A of battery current charged. The result is a total effective SRC load of 1492 W.

Figure 44 shows the total system efficiency during the light load test, which considers SRC efficiency as well as the efficiency of both the front and back end converters. Final peak system efficiency corresponds to the peak SRC efficiency and has a value of 87.22%. It can be seen that system efficiency generally follows the SRC efficiency as this converter processes the bulk of the load and thus the bulk of the losses. As the SRC process the bulk of the load it follows that optimization of this converter should result in an optimized system. Note that for the system efficiency drops to 0% from 250 ms to 500 ms and this is a delayed result of the back end converter initializing with the algorithm at 200 ms.

Finally, Figure 45 shows the performance profile of the SRC and the shift in efficiency from start to finish for the Light Load Test. For a final effective SRC load of 1492 W and an input voltage of 120 V, we should expect the SRC to be operating around 89-91% efficiency, which has excellent agreement with the simulation results.

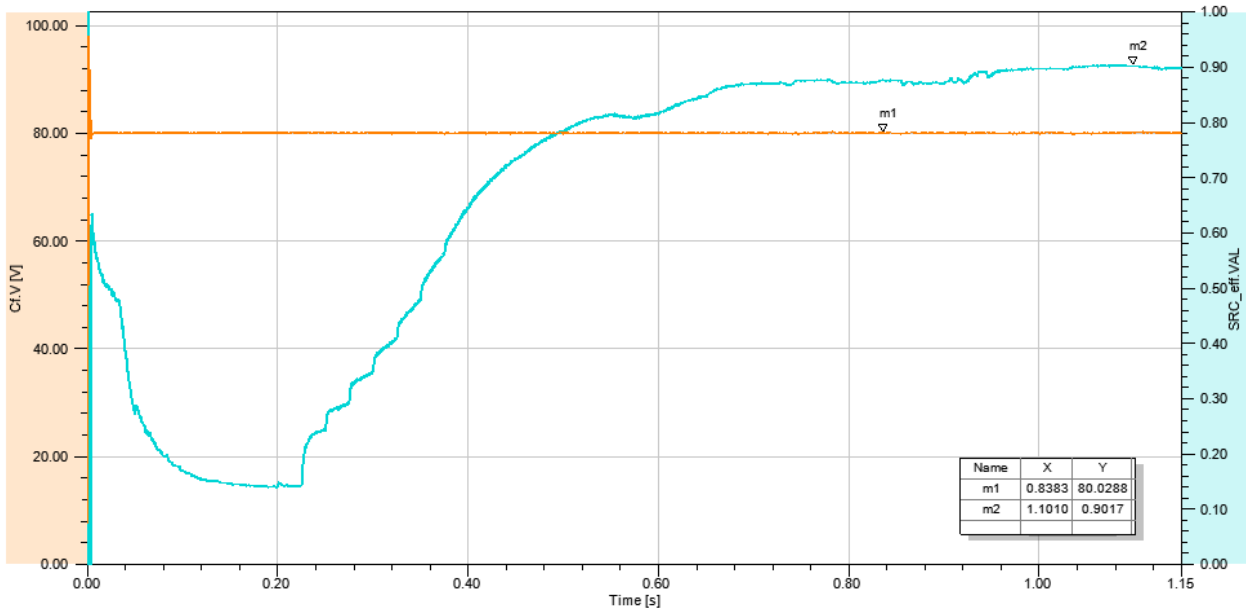


Figure 42. Load Voltage (orange) and SRC Efficiency (light blue) during Light Load Test

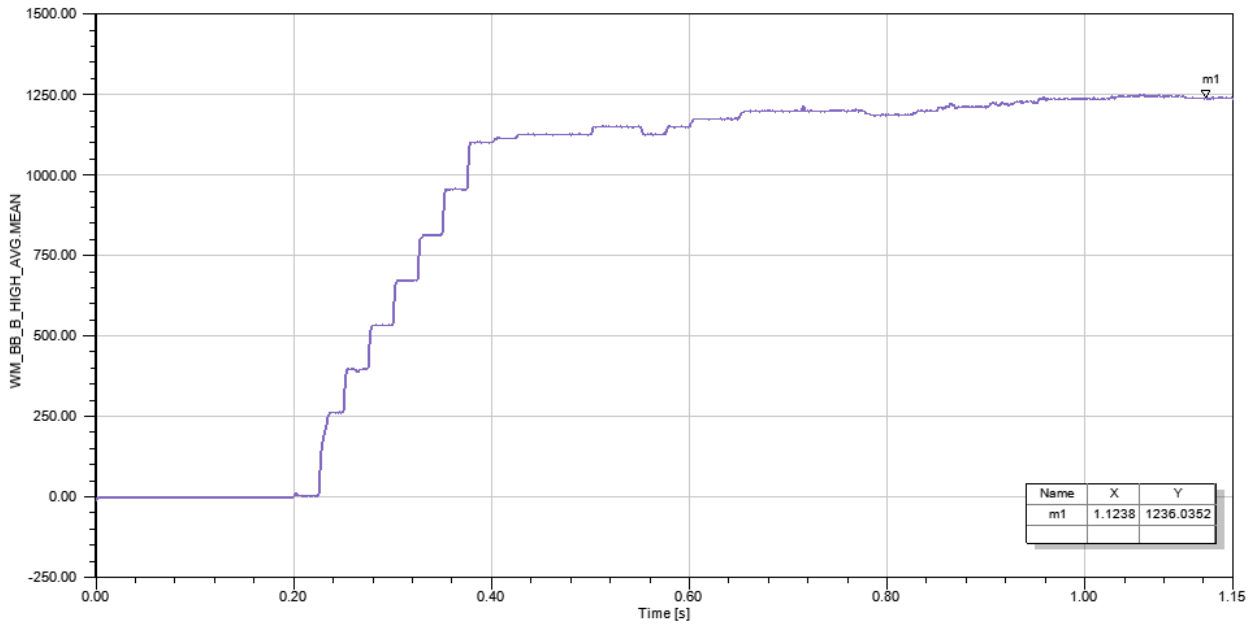


Figure 43. Back End Converter Power Processed during Light Load Test

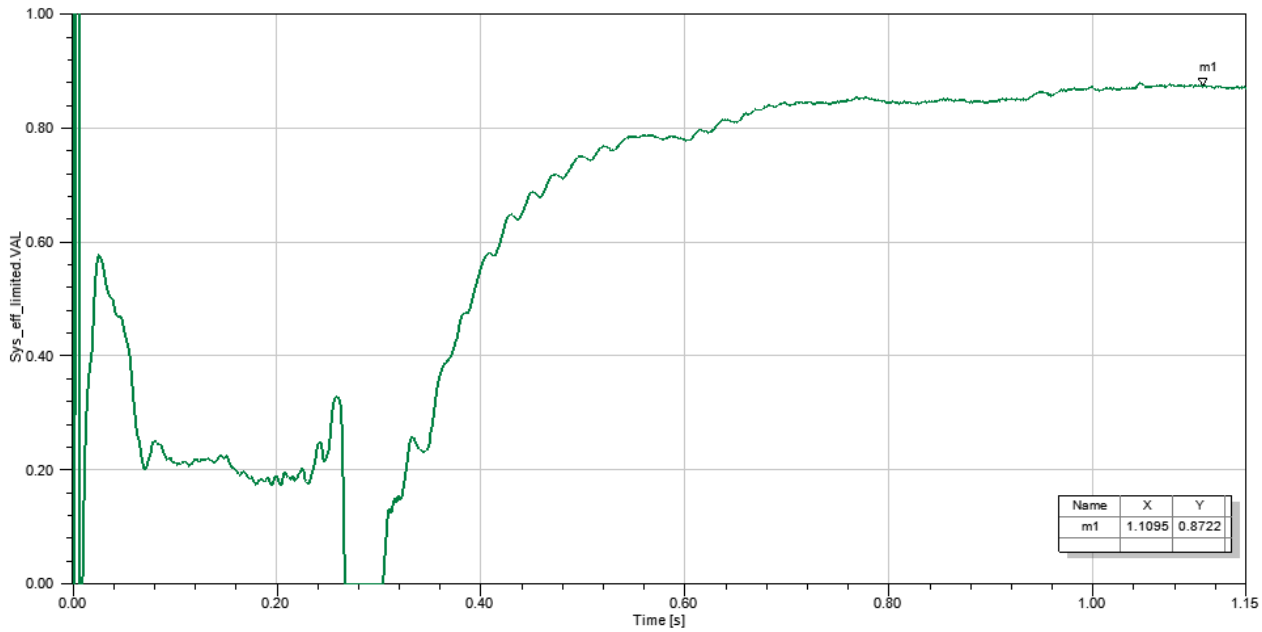


Figure 44. System Efficiency during Light Load Test

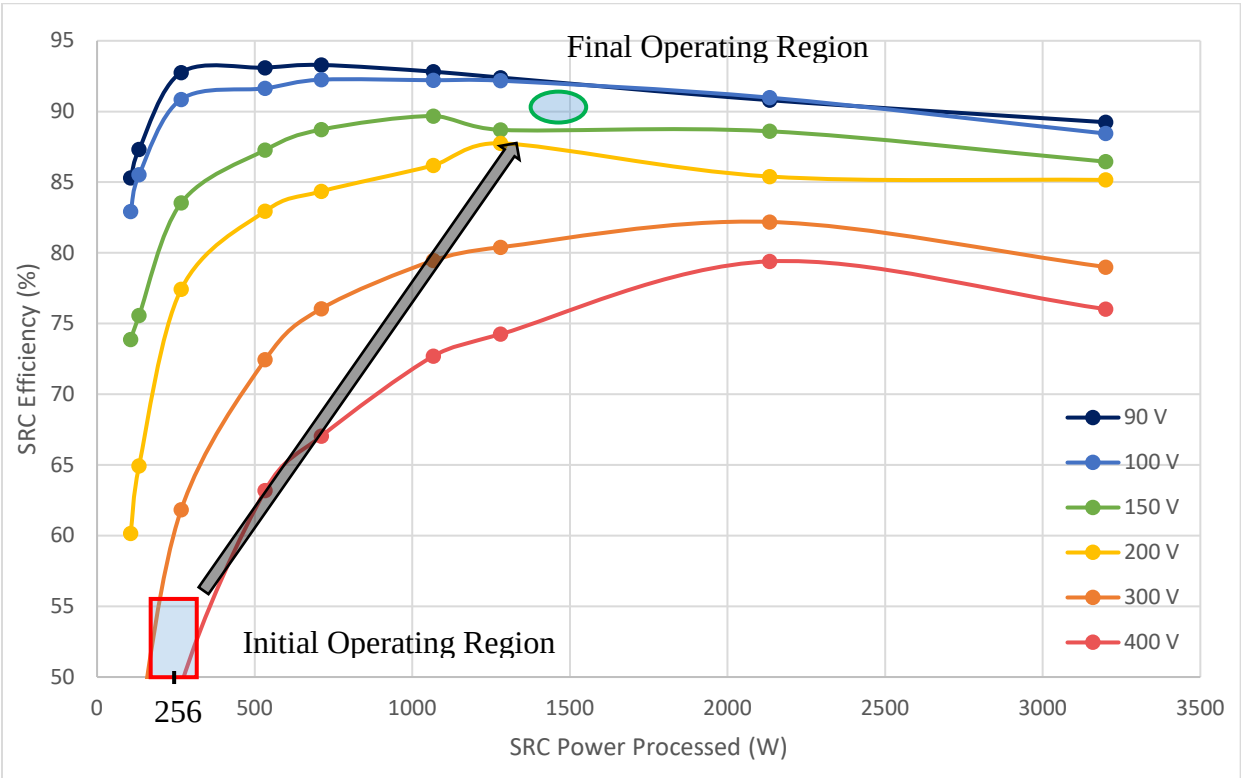


Figure 45. SRC Performance Profile for Light Load Test

6.2 HEAVY LOAD TEST CASE

Initially the PV array receives full irradiance of 1000 W/m^2 for an output of ~4200 kW and the SRC powers 2133 W of load, resulting in 2100 W of excess power generated. Assistance begins at 200 ms with both the front and back end operating simultaneously: charging the battery via the front end and discharging current to the load via the back end. Note that the front end charges at a rate quicker than the back end discharges such that the net transfer of current results in the battery charging. The algorithm achieves optimized performance by 1700 ms.

The PV array output power and PV converter output voltage (SRC input voltage) are shown in Figure 46 in red and navy blue, respectively. Marker 1 (m1) shows the 4.2 kW PV array output for the given irradiance. Marker 2 (m2) shows that the final input voltage into the SRC is 86 V.

The load voltage and SRC efficiency are shown in Figure 47, in orange and light blue, respectively. As with the light load test, the load voltage is maintained at the target 80 V for the duration of the simulation. Efficiency is 44% when the algorithm initializes, and the efficiency continues to decrease for a period until 400 ms. At this point the charging contribution of the front end converter surpasses the discharging contribution of the back end converter, resulting in a net charge to the battery and a reduction of input SRC input voltage, consequently improving efficiency. With dual assistance the algorithm reaches a peak efficiency of 92.85% for the given system conditions.

Figure 48 shows the power transferred via the front and back end converters between the battery and the SRC, in yellow and purple respectively. Recall that positive values correspond to battery charging and negative values correspond to battery discharging. For the final SRC efficiency of 92.85%, the front end converter charges the battery with 2978 W and the back end

converter discharges 1050 W from the battery to the load. Hence the net power is positive and the battery is charged with a total of 1928 W. Additionally the 1050 W of discharged power reduces the effective SRC load from 2133 W to 1083 W.

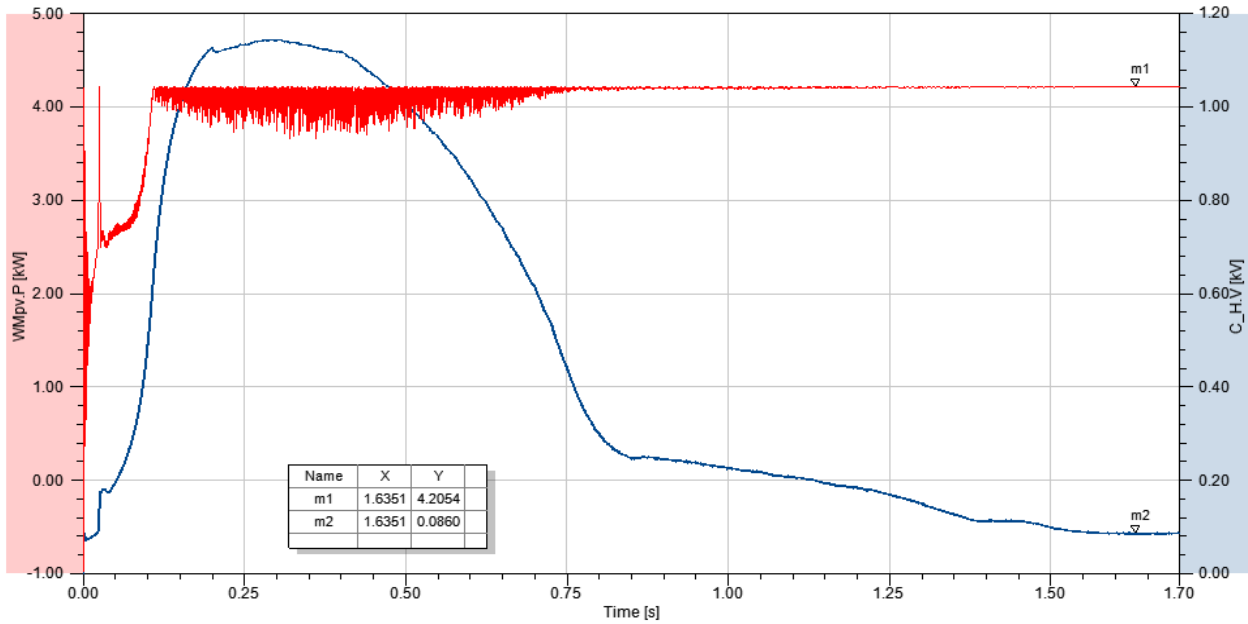


Figure 46. PV Array Output Power (red) and PV Converter Output Voltage (navy) during Heavy Load Test

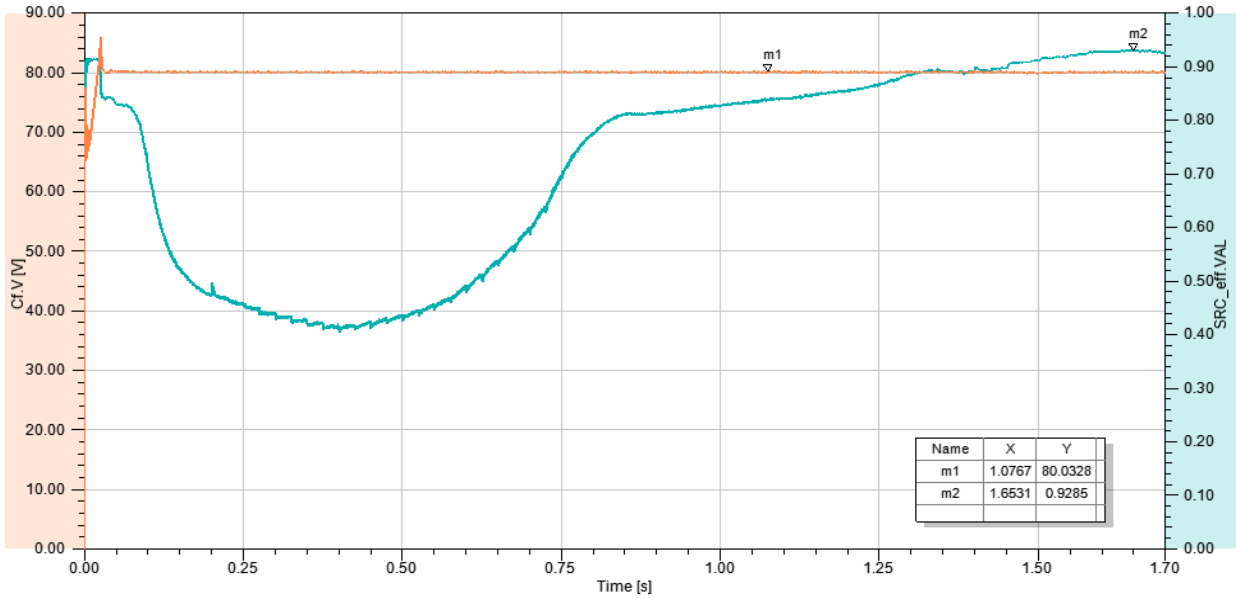


Figure 47. Load Voltage (orange) and SRC Efficiency (light blue) during Heavy Load Test

Figure 49 shows the measured current in to the battery and confirms that the battery receives a net charge. Of note is that the current that the battery receives has a significant amount of ripple during the tracking period of the algorithm as both converters are moving their respective operating points every 25 ms. This ripple could prove troublesome in practical application, however the current ripple reduces significantly once the algorithm has converged to the optimal current transfer values. For optimal SRC efficiency the battery is charged with a total of 38.25 A.

Figure 50 shows the total system efficiency during the heavy load test, with a final peak system efficiency of 93.9 %. This value exceeds SRC efficiency and is due to the large amount of power processed by the front converter, which operates with efficiency between 93% and 96%. Again with the system efficiency we see a significant drop around 250 ms which is characteristic of the front and back converter initialization.

The SRC performance profile is shown in Figure 51 and illustrates the improvement to SRC efficiency with the operation of the assistance algorithm. For a final effective SRC load of 1050 W at an input voltage of 86 V the expected efficiency is 93-94%, very near the optimized SRC efficiency of 92.85%.

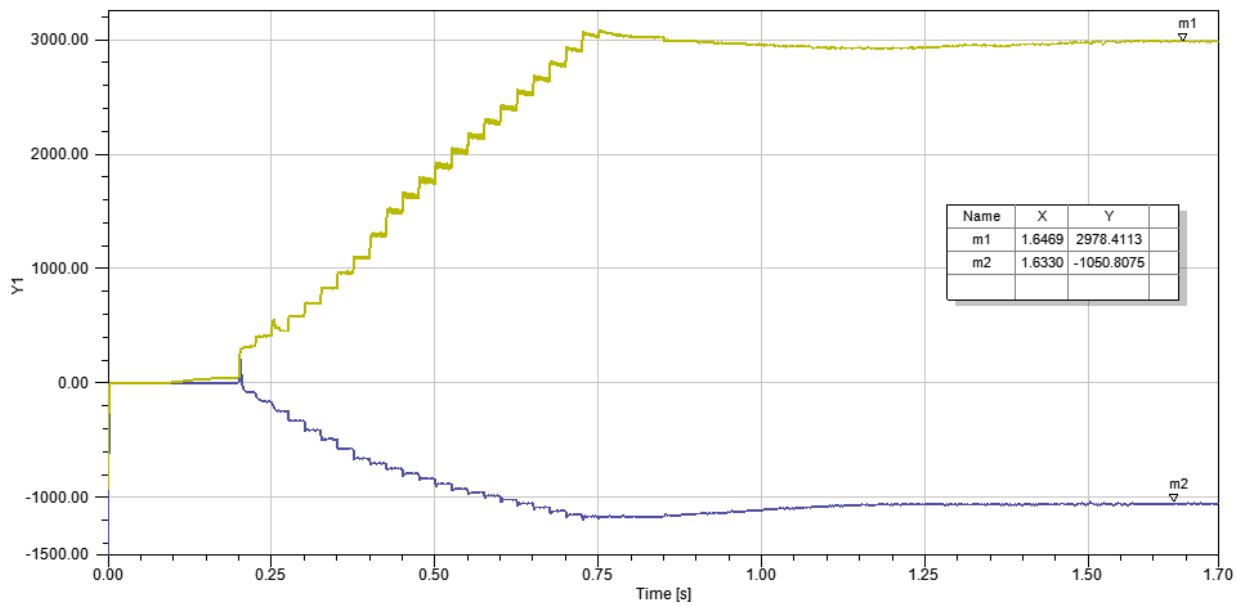


Figure 48. Front End Converter (yellow) and Back End Converter (purple) Power Processed during Heavy Load Test

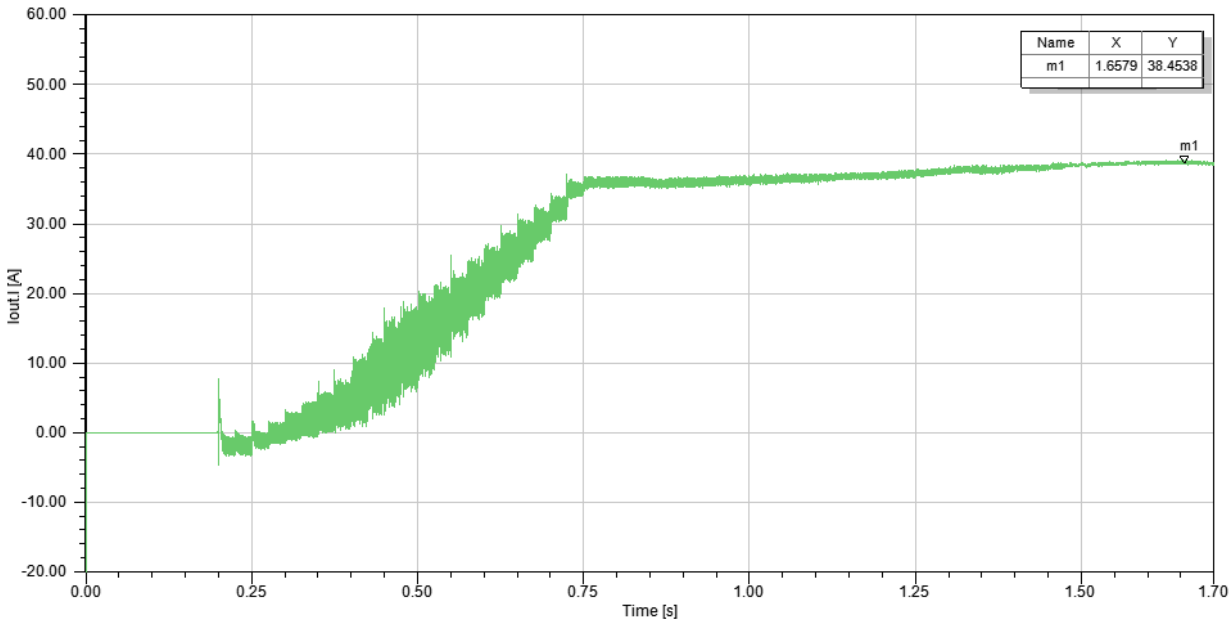


Figure 49. Battery Current during Heavy Load Test

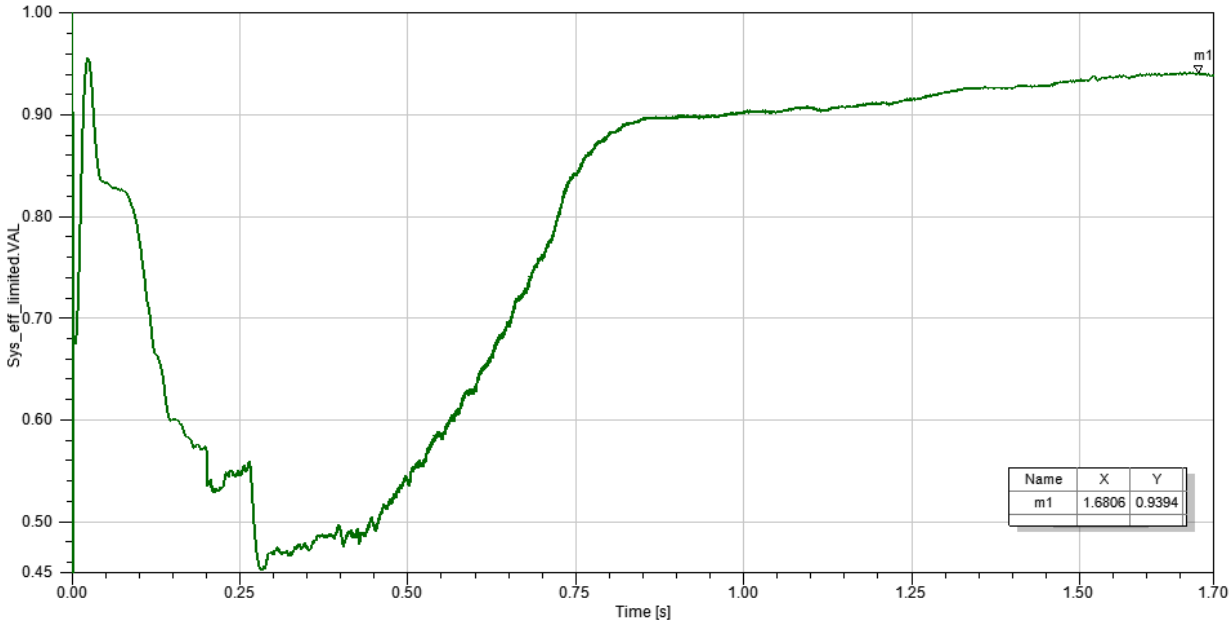


Figure 50. System Efficiency during Heavy Load Test

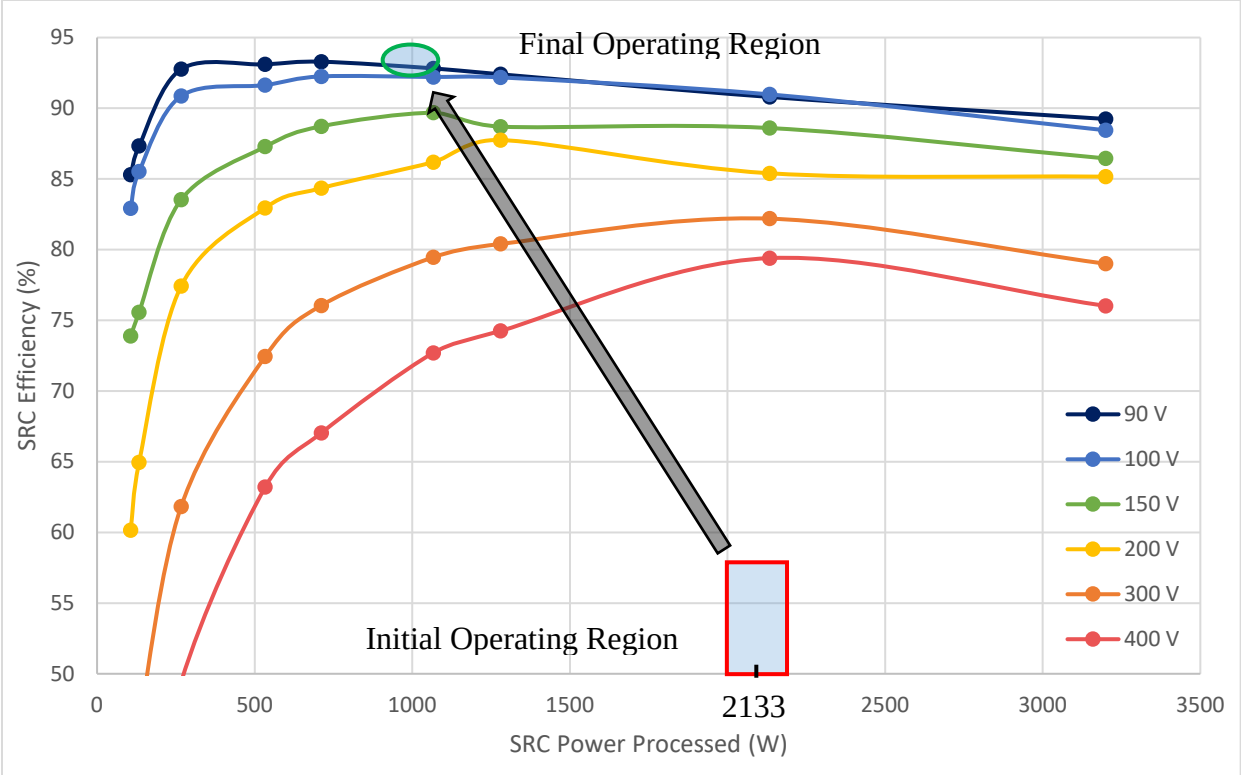


Figure 51. SRC Performance Profile for Heavy Load Test

6.3 PV DROPOUT TEST CASE

Initially the PV array receives an irradiance of 375 W/m^2 for an output of ~1550 kW and the SRC powers 256 W of load, resulting in 1294 W of excess generated power. Starting at 200 ms the algorithm initializes, starting with the back end first as this is a light load scenario. The algorithm begins tracking SRC efficiency and attempts to optimize performance by charging the battery off the back end as to increase the effective load of the SRC.

Before reaching peak efficiency, heavy shading occurs at 500 ms and the irradiance that the array receives is reduced to 40 W/m^2 for an output of ~160 W. The significant shift in irradiance causes the PV array to dropout as the array converter attempts to find the new MPP. The algorithm senses the drop in load voltage beneath the critical threshold of 77.5 V and changes its focus to voltage support of the load, disregarding converter efficiency and discharging battery current to the load.

By 800 ms the array converter has stabilized to its new MPP of 160 W. Hence for supplying a 256 W load there is a net generation deficit of 96 W. With the PV re-stabilized and generating steady power once again, the back algorithm recognizes that it is supplying more current to the load than necessary and, around 900 ms, begins reducing its contribution to improve converter efficiency, all while ensuring load voltage is maintained above 77.5 V. By 1200 ms the back end converter has reduced its contribution such that it only supplies the net power deficit while maintaining the load voltage to +/- 3% of the target voltage.

The PV array output power and PV converter output voltage (SRC input voltage) are shown in Figure 52 in red and navy blue, respectively. Markers 1 (m1) and 2 (m2) show the two output power levels of the array, 1548 W and 158 W, for the two respective levels of irradiance. Marker 3 (m3) shows the final voltage into the SRC of 81.1 V.

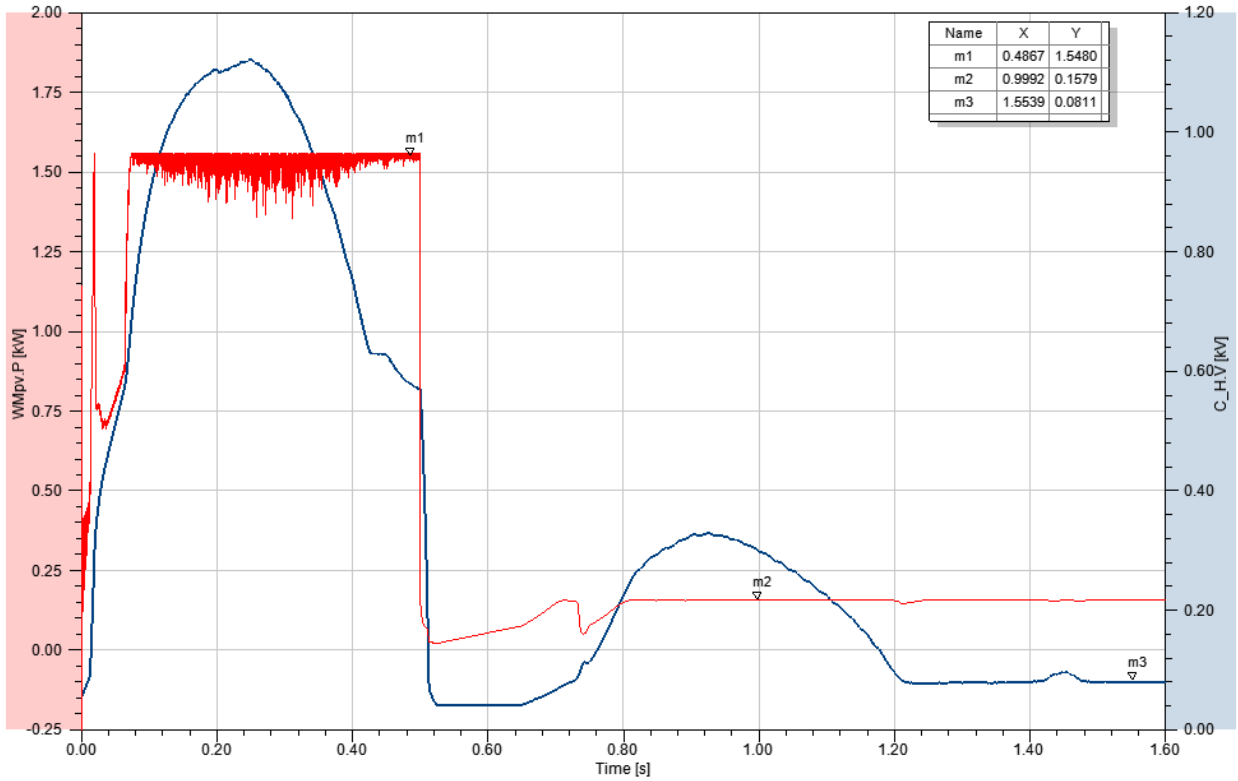


Figure 52. PV Array Output Power (red) and PV Converter Output Voltage (navy) during PV Dropout Test

The load voltage and SRC efficiency are shown in Figure 53, in orange and light blue; note that shaded regions distinguish transitional periods of the simulation. An important thing to note is that when the load voltage critically drops out, it is clamped by the battery voltage, because current flows freely from the battery to the load for any load voltages lower than 42 V battery voltage. Additionally while the PV converter readjusts to the new MPP, the SRC powers the minority of the load with the power available from the PV array while the bulk of the load is handled by the battery. Although the battery does not regulate load voltage, the SRC uses the small power it receives from the PV array to handle the tight voltage regulation of the load. Load

voltage is maintained at 80 V until the heavy shading occurs at 500 ms and voltage regulation is regained at 750 ms once the PV begins to re-stabilizes. Final load voltage is maintained above 77.5 V after the back end reduces its current contribution. Final efficiency after reduced contribution is 94%; this excellent efficiency is achieved because the input voltage to the SRC is lower than nominal as a result of the power deficit.

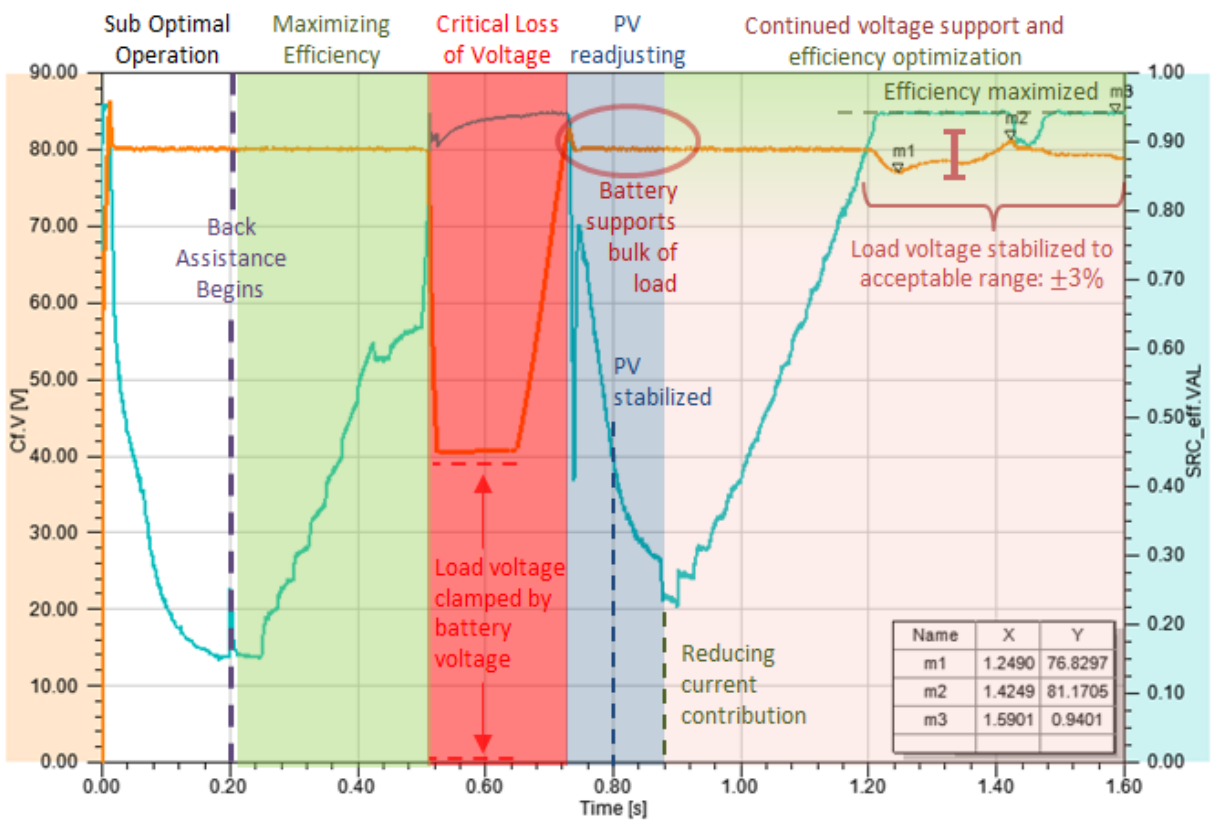


Figure 53. SRC Efficiency (light blue) and Load Voltage (orange) during PV Dropout Test

The power processed by the back end converter can be seen in Figure 54. It can be seen that starting at 700 ms it discharges 208 W to the load, recalling that negative power corresponds to battery discharge. This power in addition to the 157 W received from the array is more than

enough to power the 256 W load, which results in excess power generated and thus elevated input voltage and corresponds to the dip in efficiency from 750 ms to 1000 ms in Figure 53. After the algorithm reduces its current contribution, the back end converter supplies only 103 W to the load, which in addition to the PV array totals 260 W for the 256 W load. The effective load of the SRC is 157 W.

Finally the totally system efficiency is displayed in Figure 55. Note that when the PV drops out the efficiency takes non meaningful values as SRC does not power the load and the battery discharges freely to the load. Final system efficiency is 91.4% for this test case, which is slightly lower than final SRC efficiency as a result of losses in the back end converter.

Figure 56 displays performance profile of the SRC and the shift in efficiency resulting from the assistance algorithm in the PV drop out test case. For the final SRC load of 157 W and an input voltage of 81.V the expected efficiency is 92-94%, which shows good agreement with the optimized SRC efficiency of 94%.

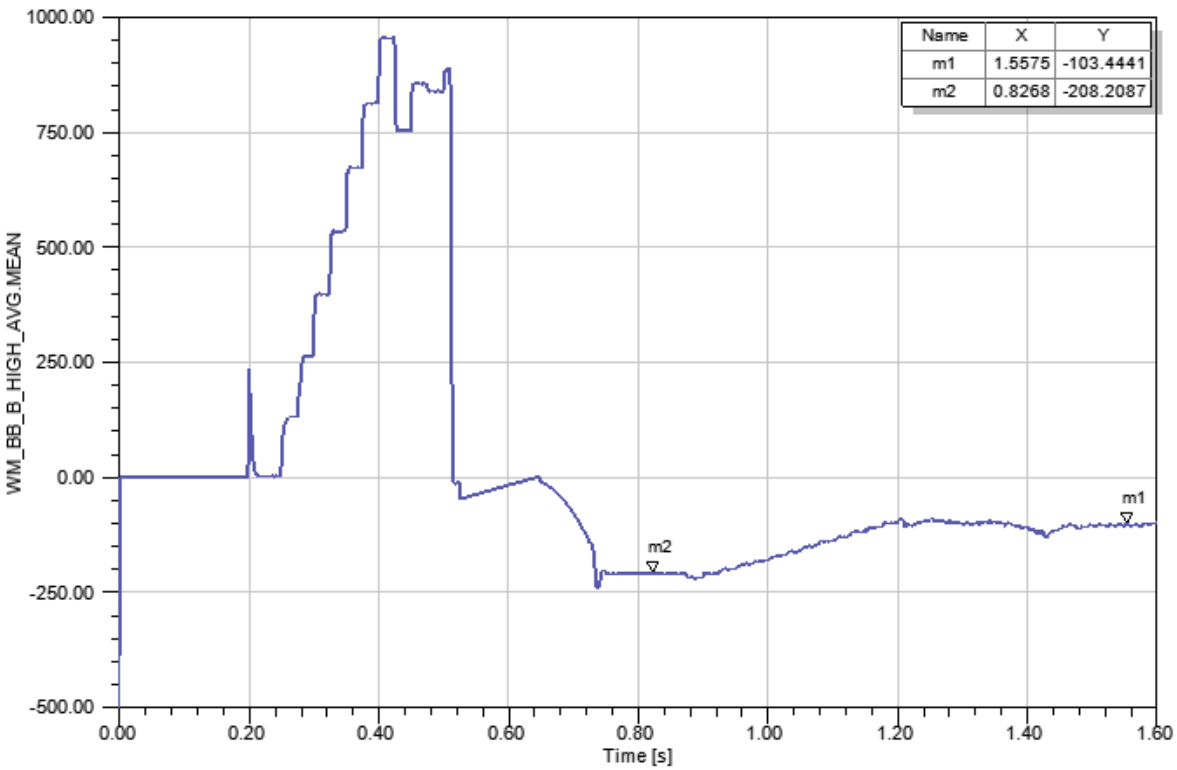


Figure 54. Back End Converter Power Processed during PV Dropout Test

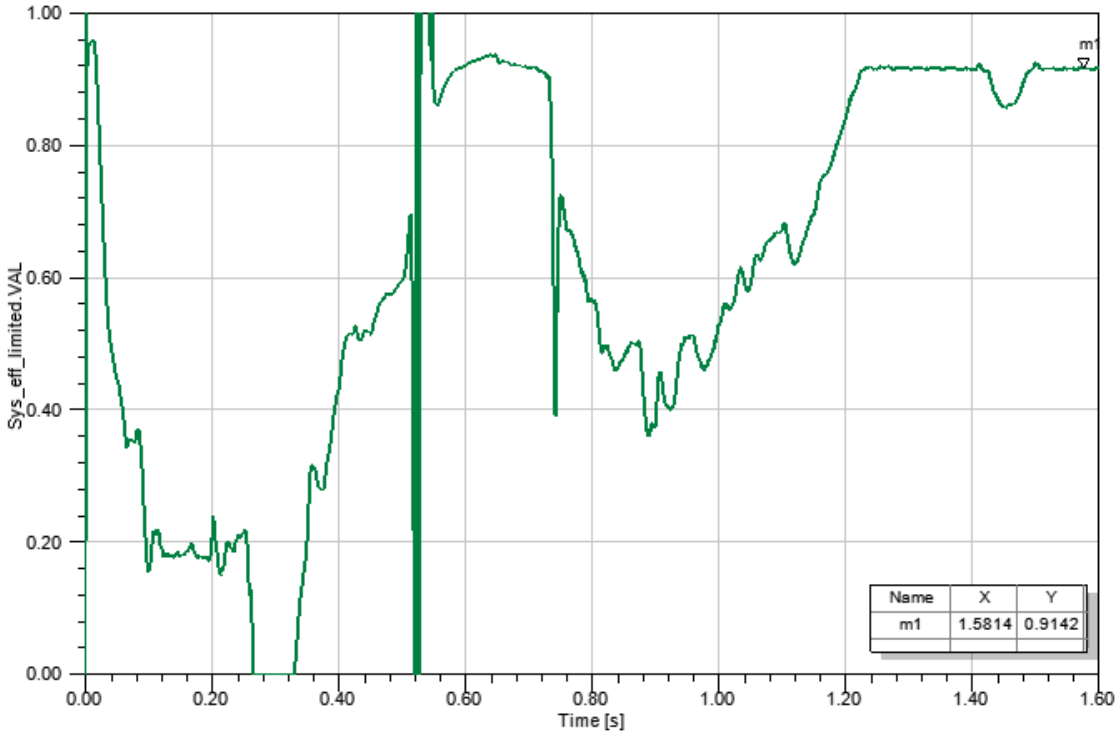


Figure 55. System Efficiency during PV Dropout Test

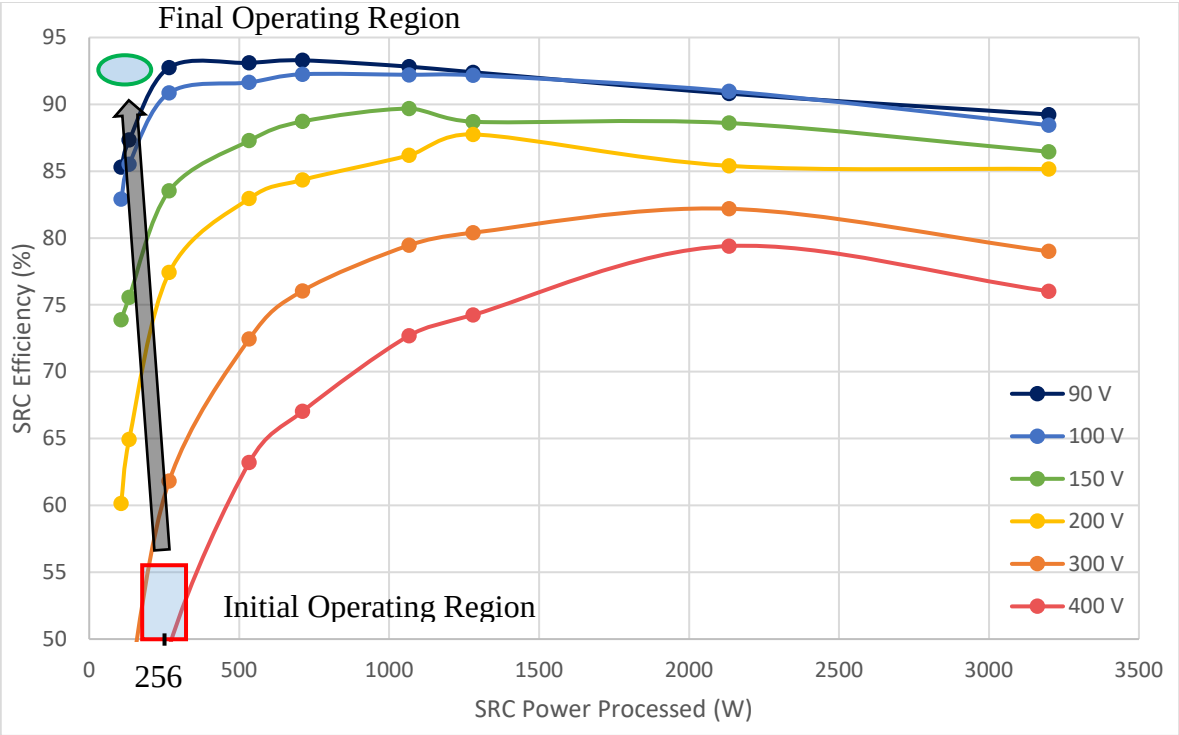


Figure 56. SRC Performance Profile for PV Dropout Test

7.0 CONCLUSION

As the electrical grid modernizes and the penetration of microgrids increases, the impacts of these independent electrical entities must be addressed. With the rising number of microgrids, isolation scenarios will become more frequent; during the duration of these scenarios proper resource management is vital to ensure power delivery to critical loads. This research has shown the effectiveness of a power management algorithm at utilizing the resources of local generation in conjunction with parallel energy storage to optimize the performance of an isolated system. The algorithm operates on the principle that the operational point of a converter of interest can be adjusted as desired, utilizing the parallel energy storage as a functional load or source. Moreover the parallel architecture lends its self naturally to multiple functionalities such as power rerouting, voltage support, and load sharing. These traits are highly desirable in isolated electrical settings and have applications in the utility, naval, and aerospace industries.

APPENDIX A

SIMULATION CIRCUIT DIAGRAMS

A.1 SRC VERIFICATION

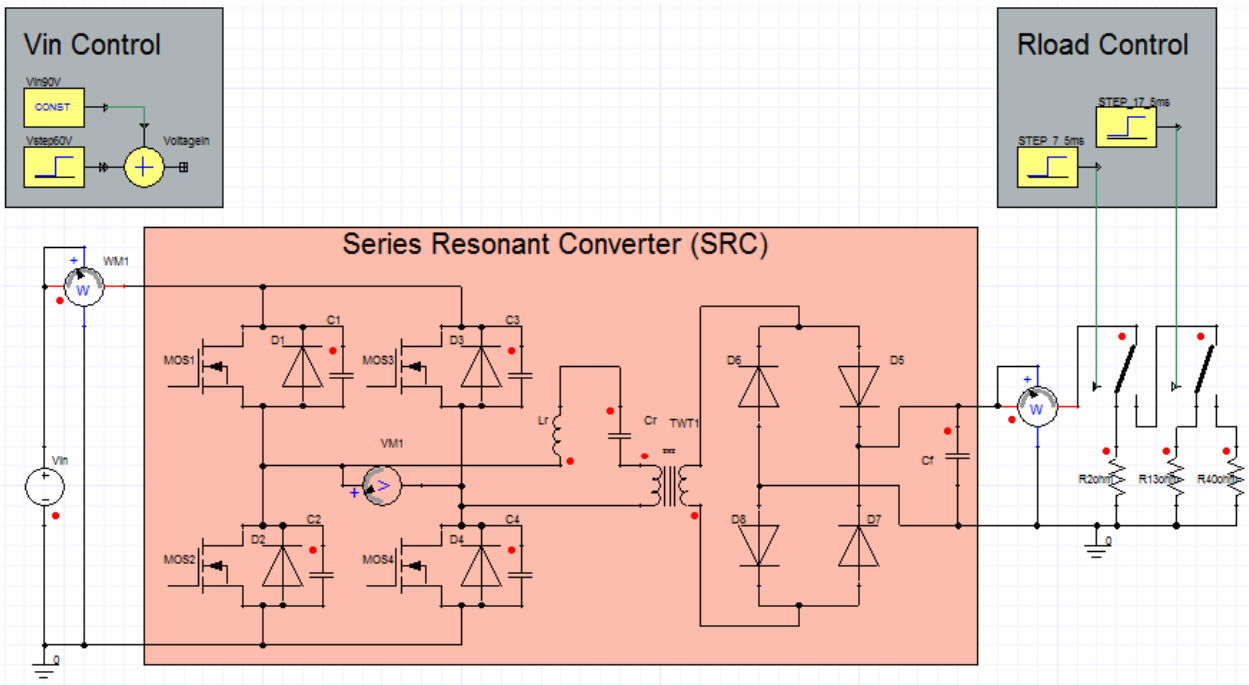


Figure 57. SRC Verification Circuit

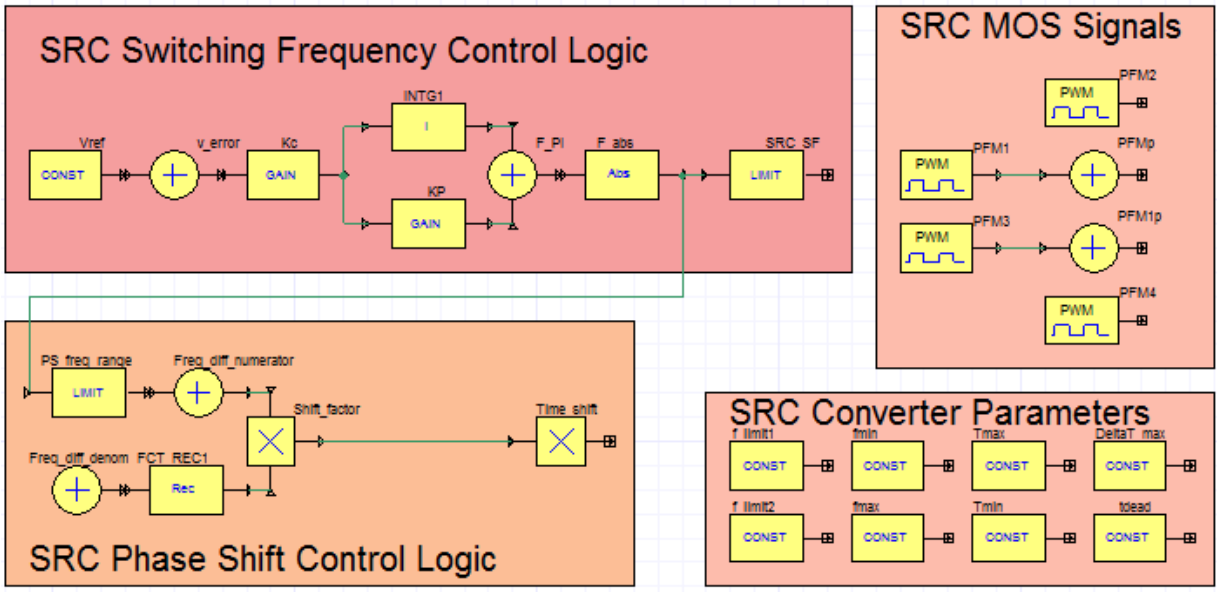


Figure 58. SRC Frequency and Phase Shift Control Logic

A.2 BUCK-BOOST CONVERTER VERIFICATION

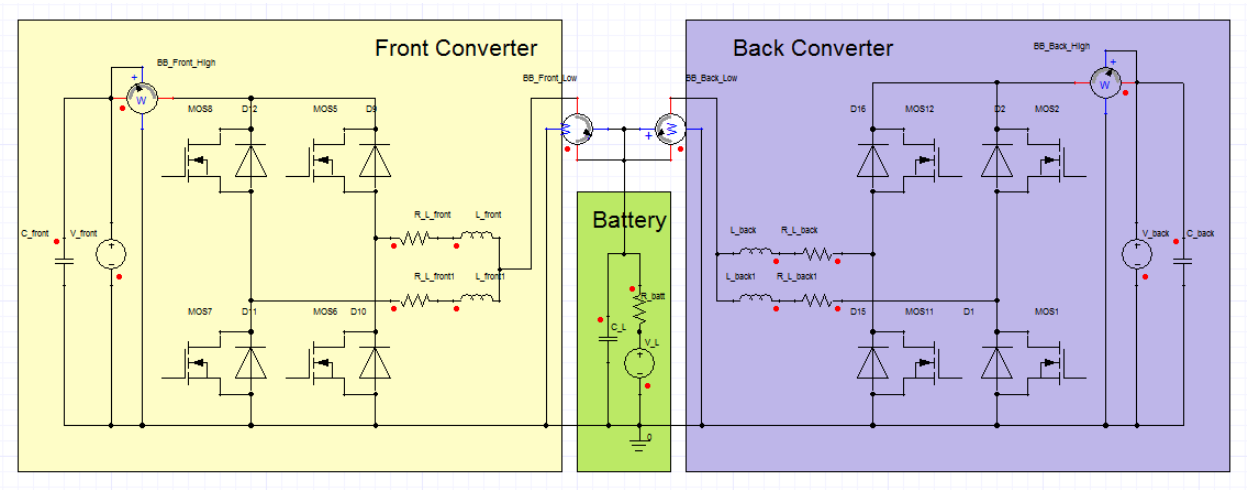


Figure 59. Front and Back Bidirectional Converter and Battery Verification Circuit

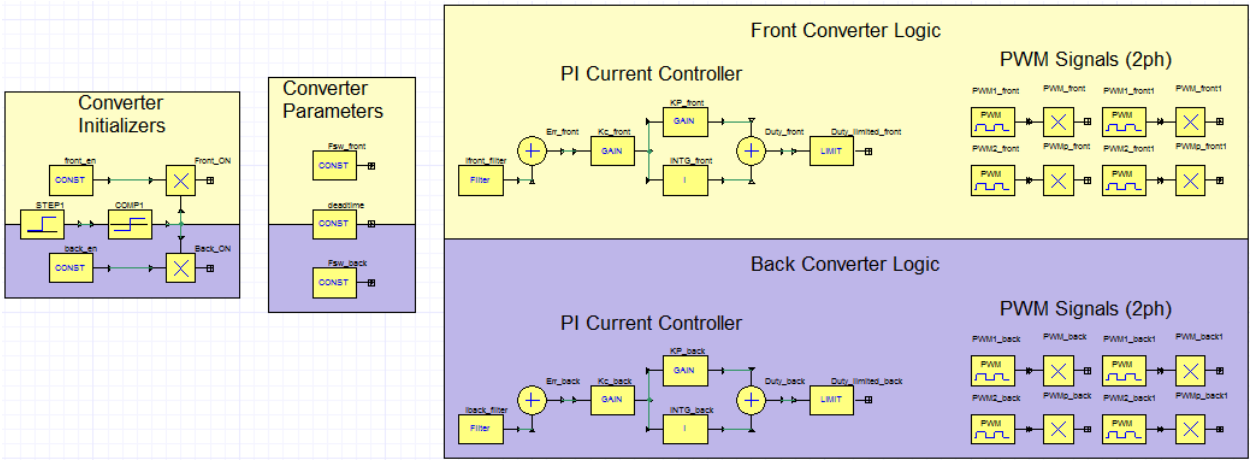


Figure 60. Front and Back Bidirectional Converter Control Logic

A.3 PV ARRAY SWEEP VERIFICATION

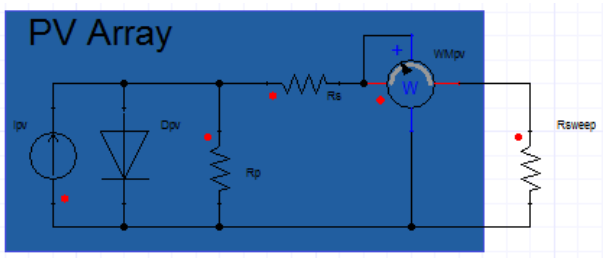


Figure 61. PV Array Sweep Verification Circuit

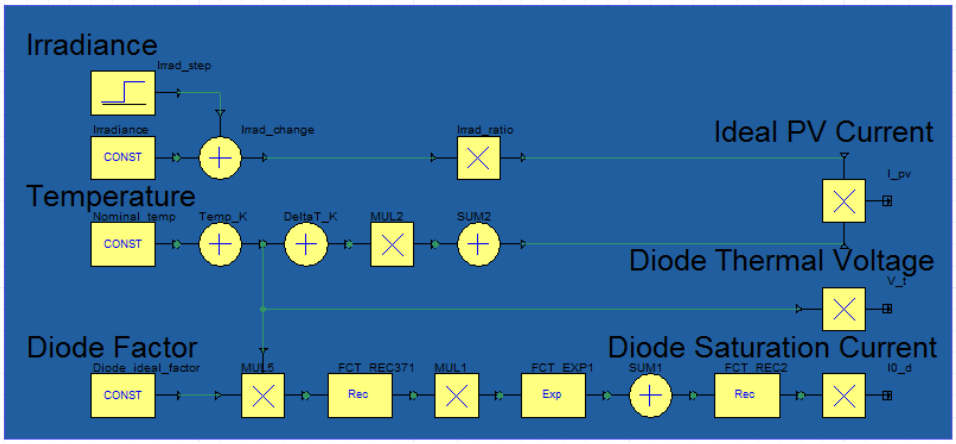


Figure 62. PV Array Parameter Calculations

A.4 MPPT VERIFICATION

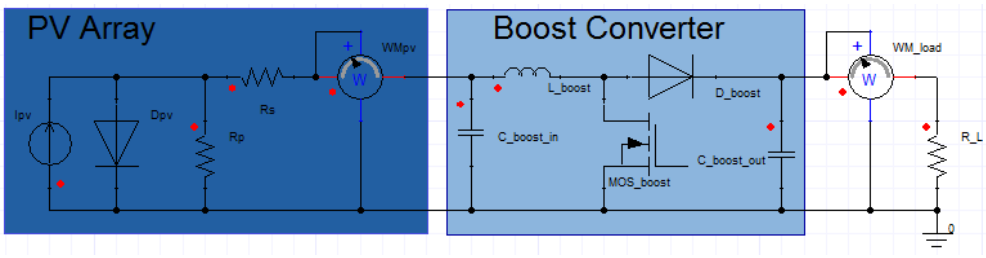


Figure 63. PV Array and Array Converter Verification Circuit

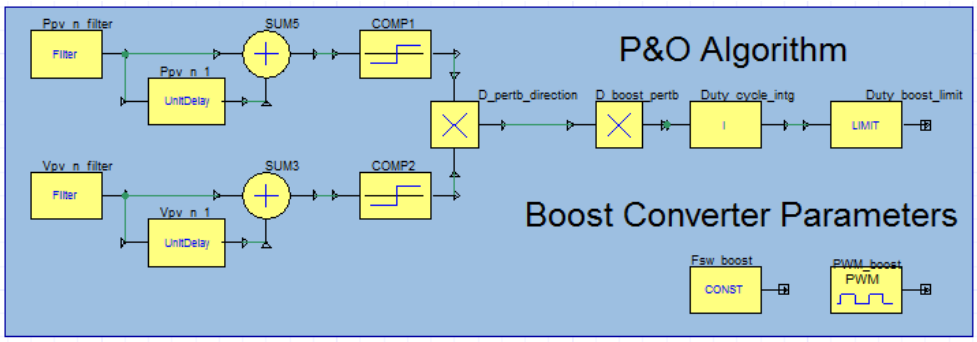


Figure 64. P&O MPPT Logic

A.5 DUAL ASSISTANCE

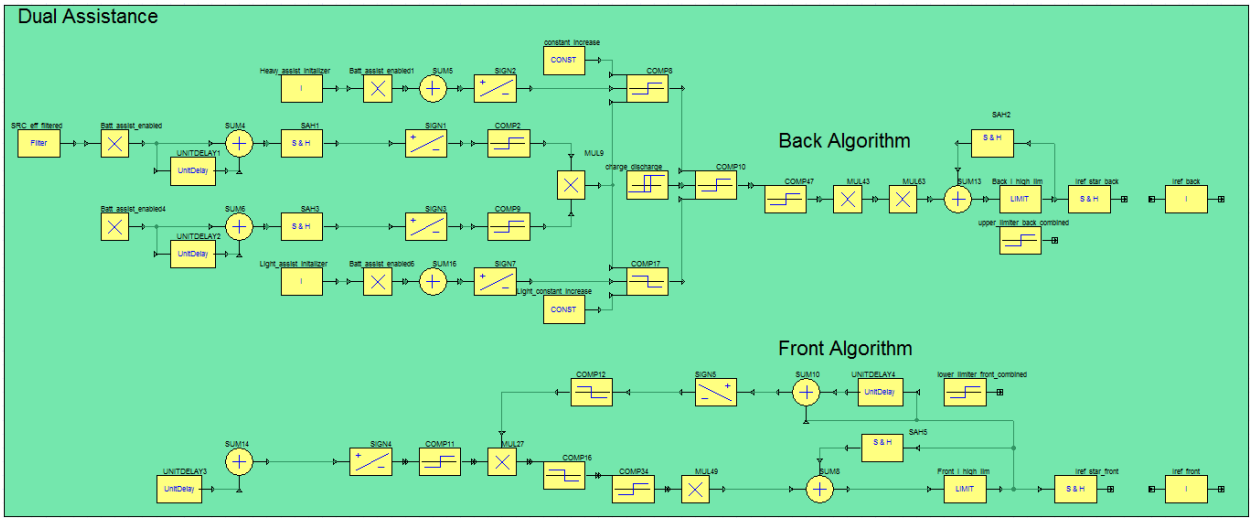


Figure 65. Front and Back Assistance Algorithm

A.6 EFFICIENCY PEAK IDENTIFICATION

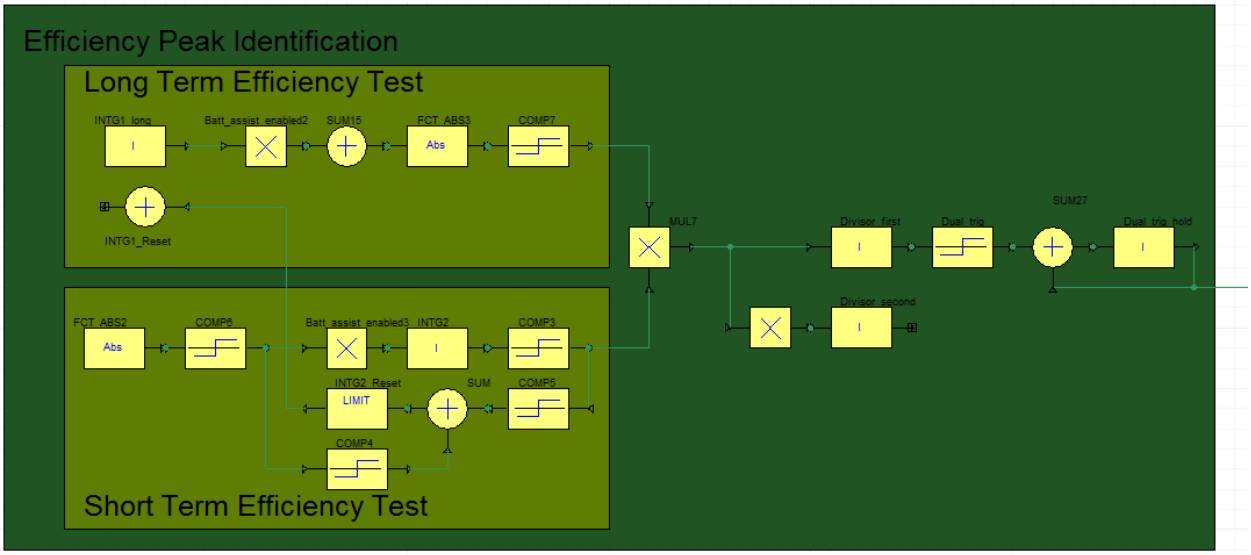


Figure 66. Efficiency Peak Identification Logic

A.7 SYSTEM MODEL

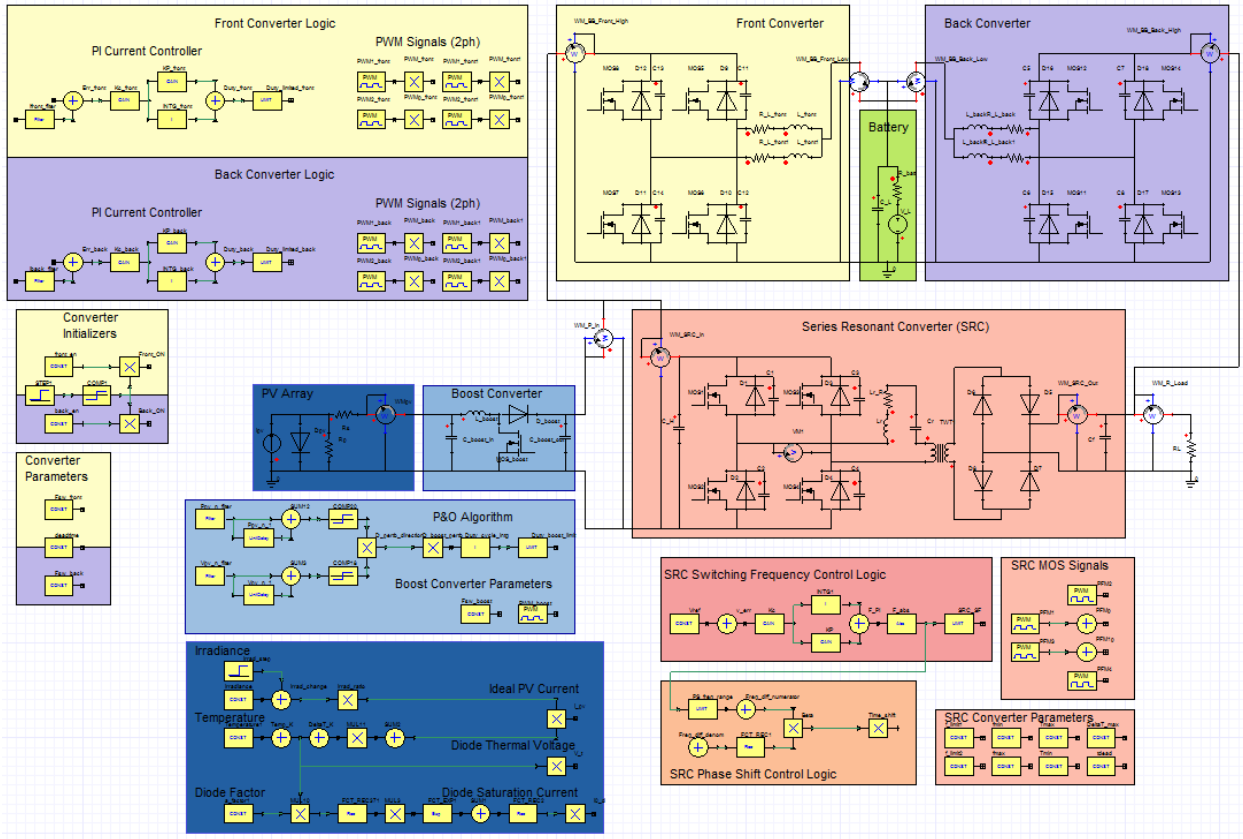


Figure 67. Isolated Microgrid System Model

APPENDIX B

MODELED COMPONENTS

B.1 SRC COMPONENTS

B.1.1 Semiconductor Devices

Table 22. Infineon FF11mR12W1M1_B11 Half-Bridge SiC MOSFET Module

Parameter	Symbol	Value
DC Blocking Voltage	V_{DC}	1200 V
Continuous Current	I_D	20 A
Surge Current	I_{DM}	142 A
On Resistance	$R_{DS,ON}$	11 mΩ
Forward Voltage	V_F	1.5 V
Calculated Diode On Resistance	_	75 mΩ

Table 23. ON Semiconductor MBR20H150CTG Power Recftifier Si Diode

Parameter	Symbol	Value
DC Blocking Voltage	V_{DC}	150 V
Continuous Current	I_F	20 A
Surge Current	$I_{F,max}$	180 A
Forward Voltage	V_F	0.72 V
Calculated Diode On Resistance	_	36 mΩ

This SiC MOSFET more than satisfies the rated maximum 150 V DC input voltage; the significant amount of voltage headroom was included to account for voltage swells resulting from transient operation periods of the algorithm. The average 19.56 A and peak 61.46 A currents are also satisfied with this device. As for the power rectifier diode the maximum 85.8 V DC voltage and the average 19.56 A and peak 61.46 currents are all satisfied.

Losses under consideration for this research are conduction losses in the FET devices and diode conduction losses in both the bridge diodes and freewheeling FET diodes; switching losses are outside the scope of this paper. Conduction losses are a direct result of the on resistance of the FET devices, while diode conduction losses are a result of both the forward voltage drop across the diode as well as the forward power dissipation through the device. Both the on-resistance and forward voltage drops of the diodes can be directly input into Simplorer, however the amount of forward power dissipation is a function of the amount of forward current flowing through the device. However, the system level diode models used in Simplorer only account for forward voltage loss and resistance loss. Thus to capture forward power dissipation under both

the heaviest and lightest load conditions, half the maximum load current was used as the baseline to calculate an appropriate static on resistance, see (33). For the FET freewheeling diodes and the half bridge diodes the average max load current is 20 A and 40 A, respectively.

$$R_{DS,ON_{calculated}} = \frac{1}{2}\frac{V_F}{I_{avg_{maxload}}} \tag{33}$$

B.1.2 LC Tank Components

Main losses of concern in the resonant tank are the DC resistance losses in the inductor and the equivalent series resistance (ESR) losses in the capacitor. The tank inductor was modeled after the HF467-130M-80AV high frequency high current toroidal power inductor manufactured by CWS. The inductor model has a range of inductance from 9 – 13 uH, a max current capacity of 80 A with a DC resistance e of 2 mΩ. The tank capacitor was modeled after the high frequency polypropylene film capacitor MPK385 series, specifically the MKP385362250JKM2T0, manufactured by Vishay BC Components. The capacitor model has a range of values from 0.47 to 82000 nF, a max voltage rating of 900 VAC, and a negligible ESR. Both of these components satisfy maximum voltages and currents expected in the resonant tank.

B.2 BACK BIDIRECTIONAL CONVERTER COMPONENTS

B.2.1 Semiconductor Devices

Table 24. International Rectifier AUIRFR4615 HEXFET Si Power MOSFET

Parameter	Symbol	Value
DC Blocking Voltage	V_{DC}	150 V
Continuous Current	I_D	33 A
Surge Current	I_{DM}	140 A
On Resistance	$R_{DS,ON}$	34 mΩ
Forward Voltage	V_F	1.3 V
Calculated Diode On Resistance	_	27.3 mΩ

The Si MOSFET ratings satisfy both the maximum 80 V DC high side voltage as well as the maximum per phase 23.8 A current during maximum power conditions. As with the SRC power electronics the losses under consideration are restricted to the main body conduction losses and diode conduction losses in the FET device. On resistance and forward voltage drop of the diode were directly input into Simplorer, while the power dissipation in the diode was calculated with (33) using a per phase average maximum current of 23.8 A.

B.2.2 Buck-Boost Inductor

Main loss in the inductor is the DC resistance losses. The inductor was modeled after the AGP4233-683ME Power Inductor manufactured by Coilcraft. This component has an inductance of 68 μH and a RMS current rating of 24 A which satisfies both the minimum CCM inductance and full power per phase current requirements of the back end buck-boost converter. It has a nominal DC resistance of 2.8 mΩ.

B.3 FRONT BIDIRECTIONAL CONVERTER COMPONENTS

B.3.1 Semiconductor Devices

Table 25. Infineon IPZ60R040C7 CoolMOS C7 Si MOSFET

Parameter	Symbol	Value
DC Blocking Voltage	V_{DC}	650 V
Continuous Current	I_D	73 A
Surge Current	I_{DM}	211 A
On Resistance	$R_{DS,ON}$	40 mΩ
Forward Voltage	V_F	0.9 V
Calculated Diode On Resistance	_	39.7 mΩ

The CoolMOS Si MOSFET more than satisfies the maximum 150 V DC high side voltage. As with the SRC power electronics the extra voltage rating is allocated to handle voltage swells

resulting from transient periods of operation. The maximum per phase 45.25 A current during maximum power conditions is also adequately satisfied.

Again the losses under consideration are restricted to the main body conduction losses and diode conduction losses in the FET device. On resistance and forward voltage drop of the diode were directly input into Simplorer, while the power dissipation in the diode was calculated with (33) using a per phase average maximum current of 45.25 A.

B.3.2 Buck-Boost Inductor

The inductor was modeled after the IHV-45-92 high current inductors manufactured by Vishay. This component has an inductance of 92 μH and a RMS current rating of 45 A which satisfies both the minimum CCM inductance and full power per phase current requirements of the front end buck-boost converter. It has a nominal DC resistance of 7.5 mΩ.

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