Ultra-Low Power, Low-Voltage Transmitter at ISM Band for Short Range Transceivers

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by

Ramy RADY

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in
Electronics and Computer Engineering

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science in Electronics and Computer Engineering.

APPROVED BY:

Assist.Prof. Dr. Hakan Doğan .....
(Thesis Advisor)

Assist.Prof. Dr. Mehmet Kemal Özdemir .....

Associate Prof. Dr. Şenol Mutlu .....

This is to confirm that this thesis complies with all the standards set by the Graduate School of Natural and Applied Sciences of İstanbul Şehir University:

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I, Ramy RADY, declare that this thesis titled, 'Ultra-Low Power, Low-Voltage Transmitter at ISM Band for Short Range Transceivers ' and the work presented in it are my own. I confirm that:

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Signed: Ramy Rady

Date: 28 APRIL 2017

“ Genius is one percent inspiration and ninety-nine percent perspiration. ”

-Thomas Edison

“ The important thing is not to stop questioning. Curiosity has its own reason for existing.”

-Albert Einstein

“ He who is not courageous enough to take risks will accomplish nothing in life.
I hated every minute of training, but I said, ’Don’t quit. Suffer now and live the rest of your life as a champion.”

-Muhammad Ali

Ultra-Low Power, Low-Voltage Transmitter at ISM Band for Short Range Transceivers

Ramy Rady

Abstract

The increasing demand for technology to be used in every aspect of our lives has led the way to many new applications and communication standards. WSN and BAN are some of the new examples that utilize electronic circuit design in the form of very small sensors to perform their applications. They consist of small sensor nodes and have applications ranging from entertainment to medicine. Requirements such as decreasing the area and the power consumption help to have longer-lasting batteries and smaller devices. The standard paves the way for the devices from different vendors to communicate with each other, and that motivates us to make designs as compatible with the standard as it can be. In this thesis, an ultra-low power high efficient transmitter with a small area working at 2.4 GHz have been designed for BAN applications. A study on the system-view perspective is important in optimizing the area and power since the transmitter architecture can change the circuit design. From a circuit design perspective, seeking to decrease power consumption means thinking of new techniques to implement the same function or a new system. Inspired by new trends, this research presents a design solution to the previously mentioned problem and hopefully, after fabrication, the measured results will match the simulated results to prove the validity of the design.

Keywords: Electronic and Communication Engineering, Integrated Circuits, Radio Frequency, ISM BAND, Low-Power Low-Voltage Circuits, UMC 65nm, Short Range Communications, BAN, WSN, Power Amplifier

Kısa Menzilli Alıcı-Vericiler için ISM Bandı'ndaki Ultra Düşük Güç Düşük Gerilim Verici

Ramy Rady

Öz

Teknolojinin hayatımızın her alanında artan kullanımı, birçok yeni uygulama ve iletişim standardının ortaya çıkmasına yol açmıştır. Şuan üzerinde en çok çalışılan konulardan birisi kabloya dayalı mevcut iletişim sistemlerinin kablosuz sistemlerle, nesnelerin interneti (IOT) gibi birçok alanda değiştirilmesidir. WSN ve BAN, elektronik devrelerin küçük bir sensör şeklinde dizayn edilerek kullanıldığı örneklerdir. Bu devreler ufak sensör düğümlerinde oluşmakta ve eğlenceden tıbbi uygulamalara kadar birçok alanda kullanım imkanı sunmaktadır. Bu eğilim, araştırmaların alıcı-verici sistemlerin yeni koşul ve gereksinimlerde daha iyi performance gösterecek şekilde optimize edilmesine odaklanmıştır. Devre alanını küçültülmesi ve güç tüketiminin azaltılması gibi yeni gereksinimler, daha uzun ömürlü piller ve daha küçük boyutta cihazlara sahip olmamıza olanak sağlamaktadır. CMOS teknolojisi, devre alanını optimize eldilmesine transistör boyutundaki küçülmeyle yardım etmektedir. Kablosuz alıcı -vericiler kapsamlı olarak çalışılmış ve olgunlaştırılmıştır fakat yeni gereksinimlerle birlikte farklı optimizasyon teknikleri daha iyi sonuç verebilir. Analog devre tasarımının karakteri gereğince bir problem için onlarca çözüm vardır ve bunların herbirisi farklı özelliklerde ve uygulamalarda daha iyi performance göstermektediler. Yani bir problem için tek bir çözüm yoktur. Standartlar farklı tedarikçilere ait cihazların birbirleriyle iletişim kurabilmesine olanak sağlar, bu yüzden tasarımımı bu standartlara olabildiğince uyumlu yapabilmek en büyük motivasyonumdu. Sistem perspektifi devrenin alan ve güç tüketimini optimize etmek için önemlidir çünkü verici mimarisi devre tasarımını değiştirebilmektedir. Devre tasarımı perspektifinden bakıldığında güç tüketimini azaltmaya çalışmak yeni tekniklerle aynı işlevi görebilecek bir devre oluşturmak yada yeni bir sistem oluşturmak demektir. Yeni trendlerden esinlenerek bu çalışmada, endüstri ve araştırmalara katkı sağlamak amacıyla bir ürün hazırlamaya çalışacağım.

Anahtar Sözcükler: Elektronik ve iletişim mühendisliği, Entegre Devreler, Radyo Frekansı, ISM BAND, Düşük Güç Düşük Gerilim Devreleri, UMC 65nm, Kısa Menzilli İletişim, BAN, WSN, Güç Amplifikatörü

To my family in Egypt that always support me, To my father's soul and to my best Friends....

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Abbreviations

MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
CMOS	**C**omplementary **M**etal **O**oxide **S**emiconductor
MEMS	**M**icro **E**lectro **M**echanical **S**ystems
OOK	**O**n- **O**ff **K**eying
BPSK	**B**inary **P**hase- **S**hift **K**eying
DBPSK	**D**ifferential **B**inary **P**hase- **S**hift **K**eying
BFSK	**B**inary **F**requency- **S**hift **K**eying
OOK	**O**n- **O**ff **K**eying
MSK	**M**inimum **S**hift **K**eying
FSK	**F**requency **S**hift **K**eying
CPFSK	**C**ontinous **P**hase **F**requency **S**hift **K**eying
PSK	**P**hase **S**hift **K**eying
ASK	**A**mplitude **S**hift **K**eying
GMSK	**G**aussian **M**inimum **S**hift **K**eying
PAN	**P**ersonal **A**rea **N**etwork
BAN	**B**ody **A**rea **N**etwork
WSN	**W**ireless **S**ensor **N**etwork
PA	**P**ower **A**mplifier
ISM	**I**ndustrial **S**cientific **M**edical
FCC	**F**ederal **C**ommunication **C**ommission
ESD	**ES**lectro-static **D**ischarge
QFN	**Q**uad **F**lat **N**o-lead
RF	**R**adio **F**requency
TRX	**T**ransceiver
T/R	**T**ransmitter/ Receiver

TX	**T**ransmitter
RX	**R**eceiver
OPAMP	**OP**erational **AMP**lifier
FBAR	Thin **F**ilm **B**ulk Wave **A**coustic **R**esonator
IC	**I**ntegrated **C**iruit
DC	**D**irect **C**urrent
AC	**A**lternating **C**urrent
PLL	**P**hase **L**ocked **L**oop
XO	Crystal **O**scillator
PA	**P**ower **A**mplifier
SAW	**S**urface **A**coustic **W**ave resonators
HBC	**H**uman **B**ody **C**ommunication
UWB	**U**ltra **W**ide **B**and
NB	**N**arrow **B**and
EVM	**E**rror **V**ector **M**agnitude
SRD	**S**hort **R**ange **D**evices
PSRR	**P**ower **S**upply **R**ejection **R**atio
ACP	**A**djacent **C**hannel **P**ower
WLAN	**W**ireless **L**ocal **A**rea **N**etwork
ACPR	**A**djacent **C**hannel **P**ower **R**ejection
SRRC	**S**quare- **R**oot **R**aised **C**osine
SPDT	**S**ingle- **P**ole **D**ouble -**T**throw
PHY	**PH**ysical **L**ayers
TDD	**T**ime **D**ivision **D**uplexing
DAC	**D**igital to **A**nalog **C**onverter
IOT	**I**nternet **O**f **T**hings
FDD	**F**requency **D**ivision **D**uplexing
FOM	**F**igure **o**f **M**erit
MIM	**M**etal **I**nsulator **M**etal
MOM	**M**etal **O**xide **M**etal
DCO	**D**igitally **C**ontrolled **O**scillator
PSD	**P**ower **S**pectral **D**ensity
EEG	Electroencephalogram

ECG	Electrocardiogram
BLE	**B**luetooth **L**ow **E**nergy
BW	**B**and **W**idth
mBVD	**mB**odified- **B**utterworth **V**an **D**yke
ITN	**I**mpedance **T**ransformation **N**etwork

Chapter 1

Introduction

1.1 Background and Motivation

Wireless data transmission and reception are required everywhere for various applications. Cell phones are the most famous example utilizing wireless signals but there is plenty of other applications. For instance, wireless local area network (WLAN) such as WIFI technology is based on wireless data transmission. A critical example would be a sensor implemented inside a human body that needs to send data to a nearest receiver which cannot use wired transmission. CMOS technology is very mature and available for bulk fabrication, which motivates the production of many chips at a reasonable price for the end-consumer. CMOS fabrication continually decreases the feature size and scales down supply voltage. That trend motivates researchers to develop efficient low voltage circuits with small sizes. In this thesis, we present a new solution in the realm of the low-voltage weak-inversion short-distance wireless transmitter. The new solution is the high efficient ultra-low power transmitter at 2.4 GHz frequency with a small cost and size. A prototype has been designed, simulated, taped-out and will be measured upon arrival to truly prove the validity of the design.

1.2 Communication Concepts

The design of a complete Radio Frequency (RF) Transceiver (TRX) requires a good background in communication concepts such as modulations, multiple access techniques

and wireless standards. This section quickly reviews those concepts with a focus on topics that are important to short-distance applications. Reference [8] provides more details about the communication concepts and wireless standard, and here we present a summary that is more concerned with low-power applications.

1.2.1 Digital Modulation

The digital modulation is implemented by digitizing the baseband signal and using it to modulate the carrier. The most basic forms are "amplitude shift keying"(ASK), "phase shift keying"(PSK), and "frequency shift keying"(FSK). The binary forms of these keying techniques are On-off keying (OOK), Binary phase shift keying (BPSK) and Binary Frequency shift keying (BFSK).

- **OOK**: The presence or the absence of the carrier for a bit period to represent binary one or zero.
- **BPSK**: Binary-phase modulation of the carrier, either pass the carrier or invert its phase. Differential PSK is done by making additional 90-degree phase shift than the normal phase of signals.
- **BFSK**: The modulation is done through discrete frequency changes of the carrier resulting in two discrete frequencies. The minimum bandwidth version with a modulation index of half is called **MSK**.

Pulse shaping: It is usually applied on the baseband pulse in order to decrease the bandwidth of the modulated signal. The most common types are:

- Gaussian filter pulse shaping: It is used with MSK, for example, and the result is GMSK
- Square-root raised cosine (SRRC) pulse shaping:It is used with the D-PSK

The modulation accuracy: The transmission modulation accuracy for PSK is measured by Error Vector Magnitude (EVM), which is the difference between the actual and theoretical symbol location on the constellation diagram.

For GMSK, the accuracy is measured by frequency tolerance and zero crossing error of the eye diagram.

The frequency deviation tolerance (δf) is measured as a percentage of the maximum frequency deviation Δf.

The Zero crossing error (Δ X_0) is the time difference between the ideal symbol period T_s and the measured crossing time [1].

1.2.2 Unwanted Power Limitations

Unwanted power limitations is an important topic, especially for power amplifiers and transmitters.

The unwanted output power is restricted by many factors such as :

Adjacent and Alternate Channel Power:

It puts a limitation to the unwanted emission of a transmitter. Usually, it is defined as the ratio of the power integrated over the channel bandwidth in the adjacent/alternate channel to the total desired transmission power and is usually given in the standard.

Transmission Mask: It gives the transmit spectral mask for each frequency band, and it shows the drop required for a channel bandwidth. Also, the transmit power-on and power-down ramps are given as a percentage of maximum power.

Wireless Device Regulation: The Industrial, Scientific and Medical frequency band (ISM-band) as called in the USA and Short-Range Devices (SRD) in Europe is a license free band that is regulated. Organizations that regulate the frequency spectrum usage, such as Federal Communication Commission in the USA (FCC), put limitations on the operating frequency, output power, spurious emissions, modulation methods and transmit duty cycle for the wireless devices. For example, it gives the maximum electrical field strength for each band, the corresponding effective radiated power and the restricted operating frequencies.

1.2.3 Multiple Access Techniques

The duplexing problem i.e. two-way communication by the TRX is discussed here.

Frequency division duplexing (FDD): It is done by using two different frequency bands for TX and RX with simultaneous transmission and reception but it needs a band pass filters.
Time division duplexing (TDD): It is done by making TX and RX paths do not work together simultaneously. TDD needs a transmit/receive switch with a low-insertion loss that follows the antenna.

TDD is preferred for the radios that are designed for low power applications due to the elimination of the filters which are more costly than a switch.

1.3 Transmitter System Level Specifications

This section provides a brief overview of the system level specifications of the wireless RF transceivers (TRX) that are necessary for short distance applications. The transmitter architecture should be selected based on performance requirements, size, cost, integrated circuit (IC) technology, and power consumption. The important parameters for the transmitter are the output power (especially the maximum output power), power consumption, size, modulation data rate and EVM. The unwanted emission of a transmitter such as Adjacent Channel Power (ACP) and in-band and out-of-band noise/spurious emissions should be defined.

1.3.1 Low Power Wireless Standards

We need the standards so that the devices that are designed by different vendors are able to exchange data. There are many wireless technologies in the world such as Bluetooth Low Energy (BLE), ZigBee, IPv6 over low power Wireless Personal Area Networks (6LoWPAN), Sub 1-GHZ Transceiver, and Body Area Network. These low power standards can be used in the design of the transceiver for applications such as the Internet of Things (IOT), wireless sensors, body and health monitoring, and gym equipment. Two examples of the applications that require integrated radio design are wearable healthcare or fitness monitors and Internet of Things devices. Reducing the size and the power consumption can help reduce battery size and reduce the final device size. The power consumption of the radio TRX is usually one of the largest contributors to the power budget of the whole system [9].

Wireless sensor Network(WSN):

The WSN consists of many small sensors that sense and send data to the base station. Those sensors consist of integrated circuits that perform many functions for medical, environmental and vehicular applications. Vehicular sensors are used in parking, braking and accidental collision systems. Environmental sensors can be used in nature for forest fires, animal tracking, food tracking and in many other ways. Medical sensors are being used to sense the vital signs of the patient such as ECG, EEG, O2 state, etc. Wireless transceiver modules have started to become integrated within these sensors allowing them to send the detected data into the base station. These operations, especially medical applications, should be done with a low power consumption. Without wireless modules, a multitude of wires will be needed to do a certain operation, and it can become impossible for devices to send data. Usually, we use multiple sensors to do any function so for ultra-low power transmitter it is critically important to increase the power efficiency and to decrease the size of the design.

Body Area Network(BAN):

Wireless body area network is a multiple-body sensor made up of implementable or wearable sensors communicating with a body central unit around the human body. The wireless body central unit can be a cell phone which has an abundance of power. Since the sensors usually suffer from lack of power, the design of high efficiency transmitter is very critical. The IEEE 802.15.6 standard for Wireless Body Area Network [1] specifies many features that are required in the design of a standardized product. For the radios, it defines three physical layers(PHY) types: Narrow Band (NB), Ultra-Wide Band (UWB) and Human Body Communication (HBC). For this thesis,a NB transmitter is designed, due to the availability of free unlicensed band to use. For NB PHY there are different frequency bands as stated in the next table.

The last two bands are

2.36-2.4 GHZ: It is a new band for BAN where there is less interference. A product can support at least one channel.
2.4-2.4835 GHZ : It is the ISM band that is available and unregulated, so many channels should be supported to avoid most of the interference.

TABLE 1.1: BAN Narrowband Channels Specifications

Freq. (MHZ)	BW(MHZ)	N channels	P_TX(dBm)	Center Freq.(MHZ)
402-450	0.3	10	Max -40. min -16	402.15
420-450	0.5	12	-10	420.30
863-870	0.4	14	-10	863.20
902-928	0.5	48	-10	903.20
950-956	0.4	12	-10	951.0
2360-2400	1	39	-10	2361
2400-2483.5	1	79	-10	2402

Using the standard [1], the other specifications of the narrowband PHY that are required to design the radios can be extracted.

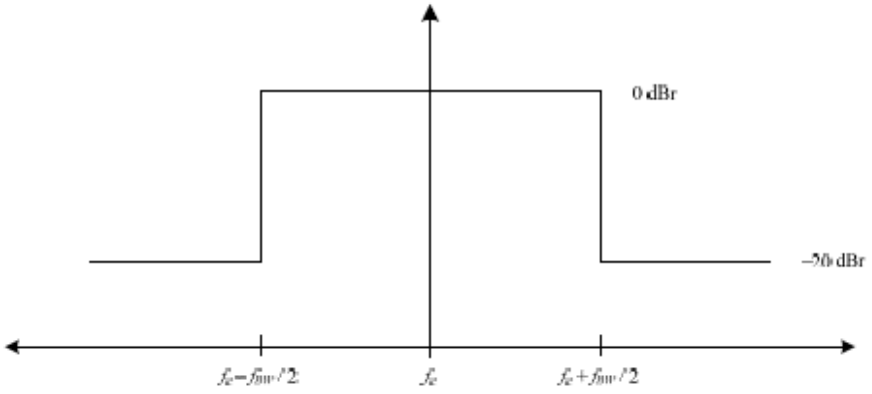

FIGURE 1.1: The Transmit power spectral density for all the frequency bands [1]

-**Power Spectral Density (PSD) MASK**: less than -20 dBr (dB relative to max power) For $||f - fc|| > fbw/2$

as shown in Figure 1.1

-**Center Freq. Tolerance** within ± 20 PPm.

-**Transmitter EVM**:

-$\frac{\pi}{2}$ DBPSK : EVM = -11 dB

-GMSK : 120% $> \delta$ f $>$ 80 % , Δ $X_0 < \pm$ (1/8)T_S

-**ACPR**: For our frequency band of interests it should be -26 dB

1.4 Low-Power Wireless Transceiver systems

Efficient high output power transmitters may not be able to work with the same efficiency at low output powers [10]. Each system may have its own optimized solution in power,

area, linearity which does not translate to the others as the standard is not the same.

For low output powers, unlike the high output counterparts, the efficiency is very critical for all the blocks, not only the power amplifier, as the power consumption of the power amplifier now tends to be nearly equal to the power consumption of any other block.

1.4.1 Survey of the previous work

A good survey of the available transmitters and carrier generation techniques is provided in reference [10]. The low-power transceiver can be done for WSN, BAN or other low-power standards. Furthermore, it can support a high data rate or a low data rate modulation schemes, which affects the spectral efficiency. The power consumption is highly related to the frequency of operation. Low-frequency transmitters can consume low power, but when they are implemented at high-frequency the power tends to increase.

Carrier Synthesis for High-Frequency Ultra-low Power Transceiver:

The most common methods are as follows:

1. **Phase Locked Loop (PLL)**: It is very common for most of the available transceiver to use a synthesizer because of its robust performance, frequency stability and ability to cover many channels. The main drawback is that it will consume high power [11].

2. **Free Running Digitally Controlled Oscillators (DCO)**: It is simple to design with very low power consumption [12]. The main problem is that the phase and the frequency are not precisely set, and as a result, it can only support OOK, FSK as non-coherent modulation schemes. One of the calibration techniques that are used to enhance frequency accuracy is base station calibration [13] which uses the injection locked loop and implements FSK; however, a receiver is needed.

3. **High-Quality Resonator (Crystal Oscillator)**:

   Due to their high quality, they provide stable frequency and phase, as is the case in the PLL. They can be used to make a BPSK modulation.

   - Crystal-Based Injection Locking:

     The idea is introduced in [14] and designed for high-frequency in [15] which

shows low power consumption and data rate. It consists of both low-frequency and high frequency parts. Due to the availability of low-frequency part, high data rate can be supported.

- RF Crystal Oscillator:

  The new advancement in the Micro-Electro-Mechanical systems (MEMS) resonators enables the design of an RF crystal oscillators that will have stability properties similar to low-frequency ones due to the High-Q factor they have. For example, Film Bulk Acoustic Wave Resonators (FBARs) or Surface Acoustic Wave Resonators (SAW) are RF high-Q resonators. The problems they may have are the limited tunability and the possibility of parasitic oscillation due to the bonding wire inductance. A solution for the tunability problem is shown in reference [6], where multiple resonators are used to achieve channel selection.

Transmitter and Modulation Scheme:

Simple modulation schemes such as OOK, BFSK and MSK are straight forward to implement and they require less complex circuit which means lower power consumption (They are energy efficient). They also do not need a linear PA or a very stable frequency generation method [10]. The only disadvantage for those modulation schemes is the spectral efficiency, which translates to less data rate regarding other modulation schemes. Other modulation schemes may have more spectral efficiency but they need a linear PA, a frequency stable reference (which translates to a higher power consumption) and they have long start-up time.

1.4.2 The Designed Transmitter System

As shown in Figure 1.2 the schematic is a direct modulation transmitter, utilizing FBAR crystal oscillator to generate the carrier, also MSK or FSK can be implemented inside the oscillator. Then the signal is either buffered to the PA or modulated and buffered to isolate the PA from the crystal oscillator. The modulations that are supported are OOK, and BPSK and they are done as part of the buffer. MSK modulation is also supported and it is implemented as part of the crystal oscillator. The antenna is shared with the RX as the system is a half-duplex system so we need a switch to connect one path at

a time i.e. TDD is used. The effect of the receiver on the transmitter is apparent as it will load the oscillator and the antenna switch. Also, receiver-transmitter coexistence i.e. sharing the same chip, will make it more probable to have a leakage or common supply/ground drops. The power management will affect the start up time of the whole transmitter and the final phase noise at the output. If the power management uses a varying time signal (when using a switched capacitor as supply), then the power supply rejection ratio (PSRR) may be crucial, as supply noise may affect the throughput.

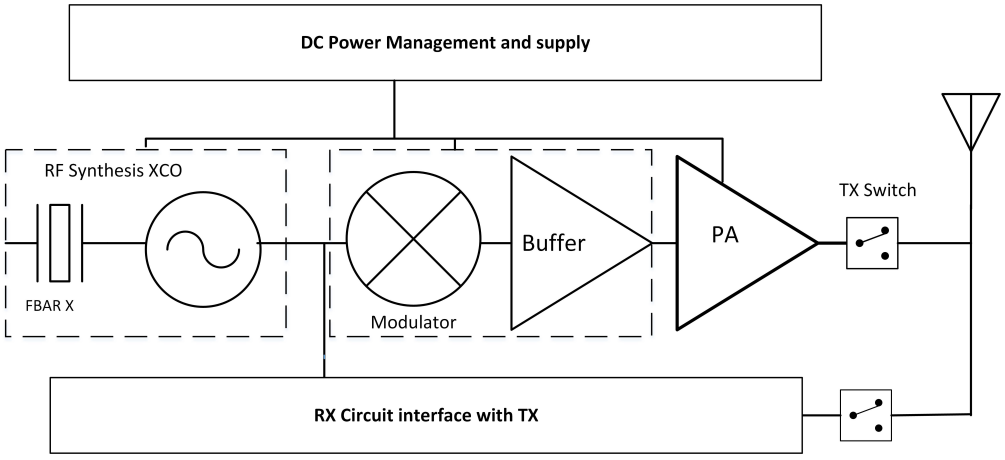

FIGURE 1.2: The Transmitter with the Rest of the Chip

1.5 Ultra-Low Power Transmitters Performance Metrics

The most important performance metrics for an ultra-low power transmitter are the output power and the efficiency.

The Efficiency:

The efficiency is indication of the amount of DC power that has been converted into RF power radiated by the antenna.

Drain Efficiency: It is the efficiency at the drain of the PA, without including the loss from the drain to the antenna.
PA Efficiency: It is the overall PA efficiency including all the biasing and transmit switch losses from the input to the antenna.
Global Efficiency: It is the overall PA and pre-driver efficiency by dividing the output power over their overall power consumption.

Total TX Efficiency: It is the efficiency that includes the crystal oscillator power consumption and the consumption of the rest of the digital circuitry supporting the transmitter.

1.6 Thesis Contribution and Outline

In this thesis, we show the design of an ultra-low power transmitter with higher efficiency, lower cost and smaller area than some in the literature, to our knowledge. All the circuits are working in the weak inversion region which results in an increase in transmitter efficiency. A fully integrated transmitter helps to decrease the cost and the area of the chip as the off-chip components are the main limitation for the reduction. Here, we present a new way to design the integrated T/R switch, which saves area and cost, as it will decrease the number of components that are not on the chip. Also, the design of the power amplifier is optimized by decreasing the supply voltage. The driver design is optimized for low power consumption by decreasing the short circuit current. The oscillator is optimized by using inverter stage with bulk biasing. Finally, the transmitter is tested with the receiver to show the final impact on the efficiency.

Chapter 2

Circuit Design for The Transmitter

This chapter is focused more on the circuit design of each block of the transmitter and emphasizes all the different options and trade-offs that concern low-power short range standards. First, we review the general considerations for low-power designs and then about each block separately. We then focus on the methodology for each block and other design parameters that are relatively important, especially small area.

2.1 Technology Characterization and Modeling for Low-Power Designs

The design starts by characterizing the technology based on the required operating conditions. The used technology is UMC65nm low leakage with RF options because of its availability and high-speed performance. We present an overview of the components focusing on the most used ones. Also, the performance around the required operating point for low-power is shown.

2.1.1 Passive Components modeling

Passive components are the elements that do not provide any gain but are crucial for circuit performance. Integrated passive components are designed different than discrete passive components. They are designed using silicon substrate and CMOS technology, so they should be modeled different than discrete passives.

Resistors :

For RF applications, we usually try to avoid using the resistor on the RF signal path to the output, or for amplifier or impedance transformation network, as it will cause a loss in signal amplitude. Instead, we try to use a transistor or an inductor at the cost of increased area. Resistors are used for biasing purposes, in analog-mixed circuits (DAC) and in low-current reference. The transmitter design utilizes RF and non-RF resistors and usually, it needs large values of resistors. To achieve high resistance, it is preferred to use high resistance with NWELL option or a non-slicide poly (which needs an extra mask) because of their high resistance density.

Capacitors :

The capacitor will be used for RF design, biasing (AC coupling) and supply DC filtering (AC decoupling) purposes. The existing types are : Metal Insulator Metal (MIM), Metal Oxide Metal (MOM), MOSFET (NCAP, PCAP). For RF design (RF signal path), the capacitor should have a low parasitic resistance, a high quality factor, and a low bottom-plate capacitance to minimize the degradation of the RF signal. MIM capacitors are used due to their superior quality factor with respect to others. MIM capacitors do not have a large area but it needs an extra mask. For DC decoupling (biasing), MIM capacitors will be used. For supply DC filtering purposes, a very high capacitor is needed. Usually, capacitor area depends on the capacitance value, so to optimize the area, we should choose a capacitor with a high capacitance density, i.e. capacitance per area, an example is NCAP.

Inductor :

Inductors are a very important circuit components for RF design. They have been studied and modeled in a lot of previous literature. Spiral inductors are the most common types. Although they are large in area, their impact on the improvement of the performance makes them an invaluable component in RF design. The inductors that are available on IC design have a limited quality factor which means that they introduce more loss than off-chip inductors.

Layout Wires Parasitic Modeling:

The parasitic effects on the circuit, due to metal wires can be modeled by resistors and capacitors in a π network [16]. The layout effects on the inductor need to be modeled,

especially for RF application. The highest metal line (Metal 8 in our case) has the lowest resistance, which improves performance of the circuit. As shown in Figure 2.1 the inductor is assumed to be ideal and only the wire parasitics are modeled. The structure resembles the π impedance transformation network and will affect the self-resonance of the inductor. The parasitic resistance will decrease the quality factor of the inductor. All these effects should lead us to connect the inductor using very short wires and to place it close to the circuitry.

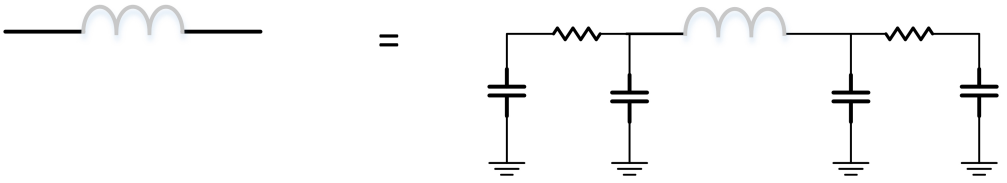

FIGURE 2.1: Parasitic of Metal Line on the Lumped Inductor on The Chip

2.1.2 Active Components Modeling

The NMOS and PMOS transistors usually differ in each new technology and have different versions within the technology. The transistors are responsible for providing gain in voltage, current or power. For nanometer technology, the short channel effects dominate the performance of the transistors and the current-voltage square law is not valid anymore. The MOSFET can be biased in one of the following operating regions: strong inversion, moderate inversion, and weak inversion (sub-threshold). At each of these regions, the transistor behaves differently and should have a different circuit equivalent model. For short channel and weak inversion operation, it is better to use a simulation-based approach to design circuits rather than using hand-calculation.

2.1.3 MOS Transistor Sub-threshold Modeling

Several methods to model the transistor behaviors in sub-threshold exists. Charge-based model and (gm/ID) can be used interchangeably. Meanwhile, using the curves that are generated from the simulator can give very accurate results [17], [18].

2.1.4 MOS Transistor Simulation-Based Modeling

This section provides the characterization of the active element, the MOS transistor. The characteristics depend on the operating frequency and the level of inversion, i.e. the operating point. This section also gives an idea about the capabilities of the technology such as the maximum operating frequency, the amount of inversion and widths that are needed to achieve the required gain.

As an example of technology characterization, NMOS for RF applications is chosen with the following parameters (W=2 μm, L=60 nm, VDS=0.35-V, lowest vth). The Figures (2.2, 2.3, 2.4, 2.5, and 2.6) explore various inversion regions determined by overdrive voltage V_{OV} and provide the transistor parameters at those regions. This technique provides the actual values necessary to design the transistors in a more accurate way than an equation, therefore it helps the designer to find the optimum solution without many iterations. V_{OV} is given by equation 2.1.

$$V_{OV} = V_{GS} - V_t \tag{2.1}$$

where V_{GS} is the gate to source voltage, V_t is the threshold voltage. Equation 2.2 defines the Quasi-static model equation of the technology and gives the minimum F_T [18].

$$F_T > 10F_{Operation} \tag{2.2}$$

where F_T is the transit frequency of the transistor and $F_{Operation}$ is the operating frequency of the transistor. When $f_{operation}$ equals 2.4 GHz, the minimum F_T value is 24 GHz and from Figure 2.2. the minimum V_{OV}=-65 mV These curves give an indication of the maximum frequency for the transistor at different values of V_{OV} i.e different levels of inversion.

From Figure 2.3 we can see that the operating gm/ID is 17. Increasing Vov more than -65 mV, decreases gm/ID value which means that the power efficiency is lower.

Using Figures (2.3 and 2.5) the value of the current of the transistor and the width can be decided on.

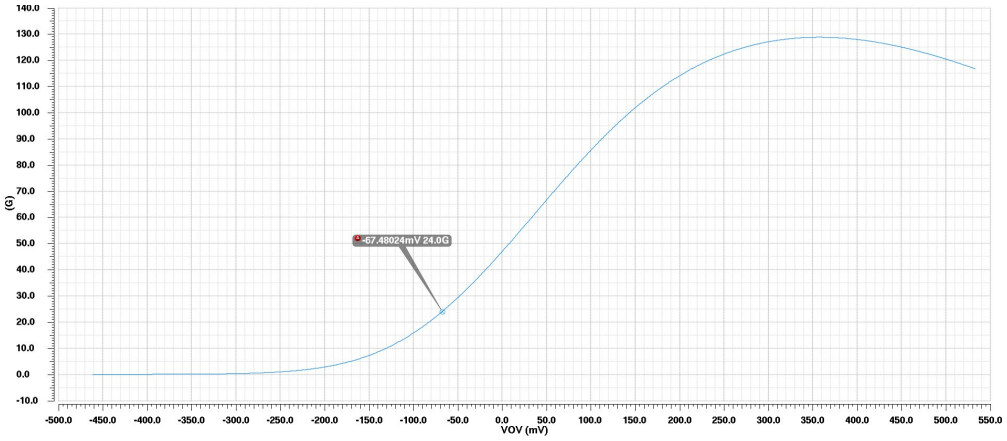

FIGURE 2.2: Transit frequency vs. Overdrive Voltage

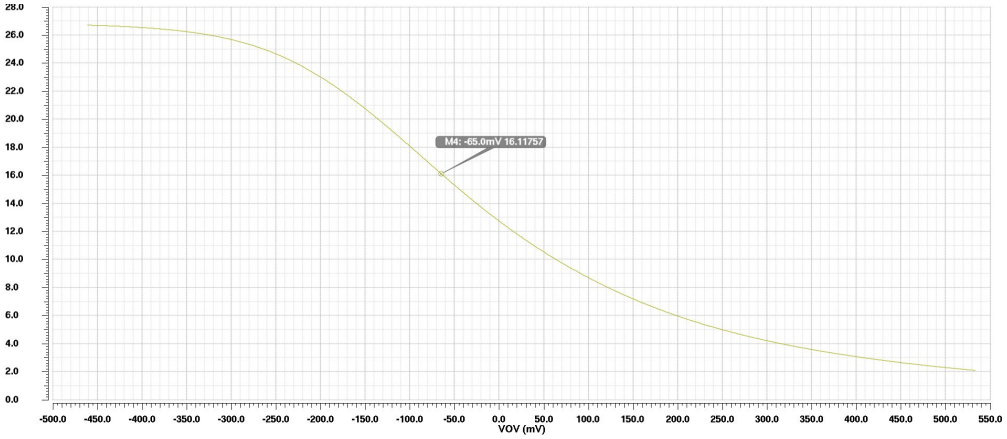

FIGURE 2.3: (gm/ID) vs. Overdrive Voltage

Figure 2.6 shows the value of gm/gds, knowing gm then gds can be calculated which is the output conductance. The output resistance (rout) is the inverse of the output conductance. Ideally, rout is infinite for ideal transistor, so having a finite value represents a non-ideality in the transistor performance i.e. signal loss.

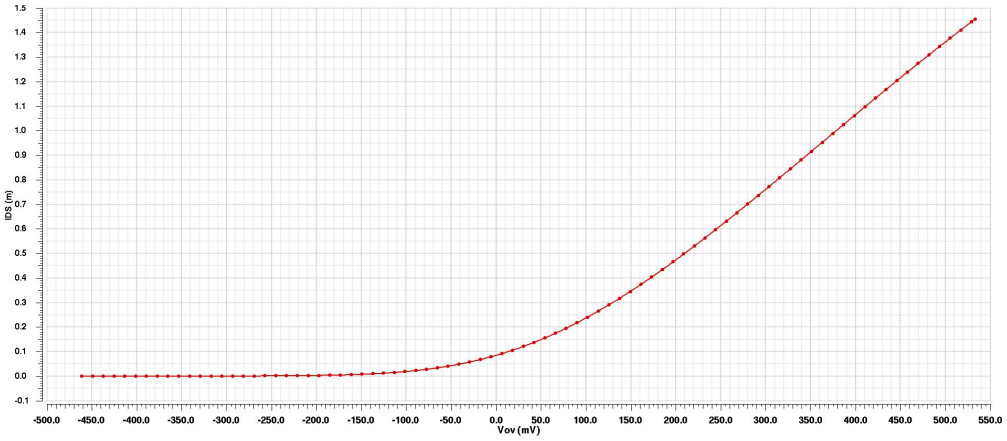

FIGURE 2.4: Transistor Current vs. Overdrive Voltage

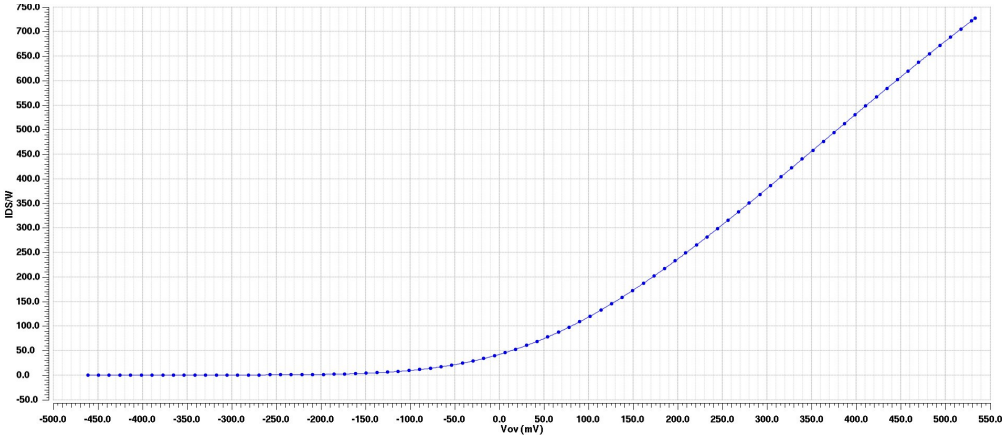

FIGURE 2.5: Transistor Current Density vs. Overdrive Voltage

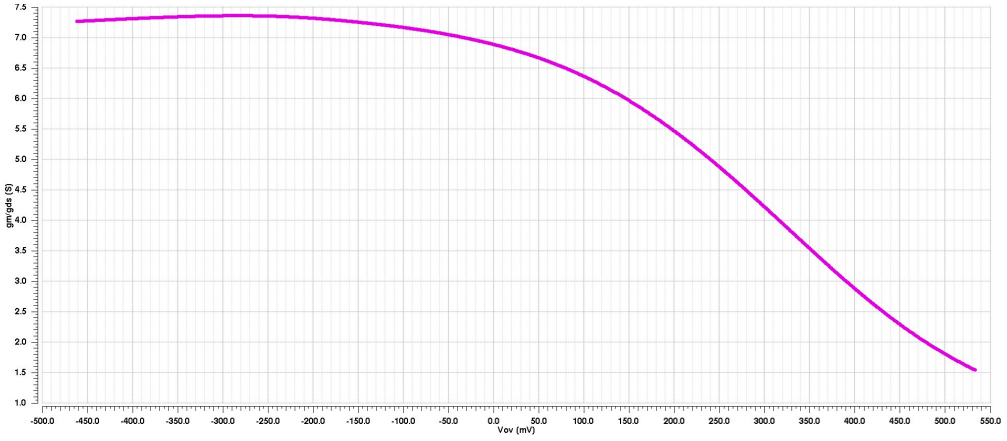

FIGURE 2.6: Transistor's trans-conductance over output conductance vs. overdrive voltage

2.2 Low-Voltage Low-Power Analog and RF Design Principles

For low-power designs, it is preferred to operate the transistor in weak inversion (sub-threshold) region, however to get the same gain a large device size is needed. This section provides a quick overview of the techniques that are used to decrease the power consumption of the designed circuits.

2.2.1 Separate Gate Biasing of The Inverter

The current-reuse architecture as shown in Figure 2.7 has more gm i.e. more gain than a single transistor, so it consumes less power. A decoupling capacitor and bias through a large resistance are used to increase the gate voltage. Due to large RC time constant in this network, settling time of the bias network is quite high. Therefore, the values need to be chosen to meet worst case settling requirements.

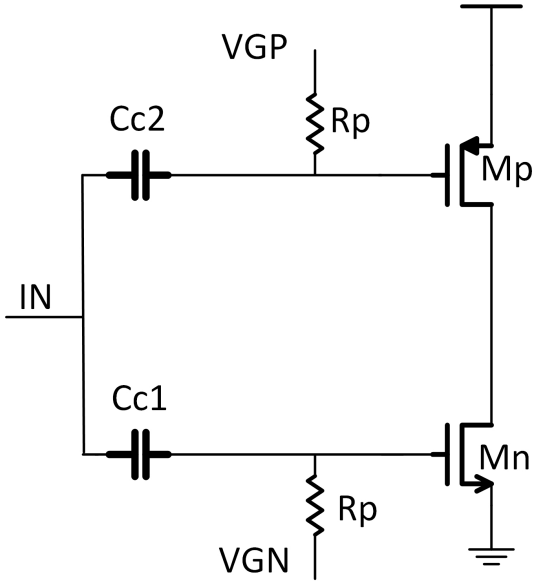

FIGURE 2.7: Current-Reuse Amplifier with Different Gate Biasing

2.2.2 Body Biasing

For low supply voltages, the transistor width should be very large to have large gm and hence gain. Reducing threshold voltage means that less width is required to get the same gain with the same V_{GS} voltage. Body biasing is done to control the threshold voltage.

The threshold voltage is reduced when V_{SB} is positive and decreased. The relation is given as in equation 2.3 [19], where V_{t0} is the value of V_t when V_{SB} is zero, γ is the body effect coefficient for a given technology. For the PMOS transistor with a positive V_{BS} it can be rewritten as equation 2.4 [19].

$$V_t = V_{t0} + \gamma(\sqrt{\phi_0 + V_{SB}} - \sqrt{\phi_0}) \tag{2.3}$$

$$V_t = V_{t0} - \gamma(\sqrt{\phi_0} - \sqrt{\phi_0 - V_{BS}}) \tag{2.4}$$

The threshold is reduced, when V_{BS} is positive and increased.

2.3 Low-Voltage Analog Mixed Biasing Circuit Designs

RF circuits usually need some supporting low-frequency circuits such as DC biasing generation to make it operate properly. A Digital to Analog Converter (DAC) and Operational Amplifier (OPAMP) are used to set the DC operating point of the transistor.

2.3.1 DAC

Setting the DC bias point for the transistor can alter the performance tremendously. Using a DAC for biasing and the ability to reconfigure makes it possible to change the values as needed. The designed DAC as shown in Figure 2.8 trades off minimum area with minimum step size. The resistive ladder DAC topology is chosen. Implementing the resistors by transistors decreases the area but also decreases the matching accuracy. The poly resistors are chosen to implement the ladder, NMOS and PMOS transistors are used to implement the switches. The digital bits for the DAC are set only at the start so high-speed writing capability is not needed. The Biasing DACs digital inputs are generated from the I2C interface. The DAC occupies an area of $(48.5 \times 35)\ \mu m^2$.

For low-power applications with 0.7-V or 0.5-V as supply voltage, since the current is needed to be few μA, total resistance in the DAC becomes in $M.\Omega$ range. Biasing many different nodes with a DAC requires custom design for each DAC so values of the resistors from R0 to R15 are set to generate the required voltages for each DAC. The resolution

of the DACs are 31.25 mV for 0.5-V supply and 43.75 mv for 0.7-V supply which is acceptable for our application.

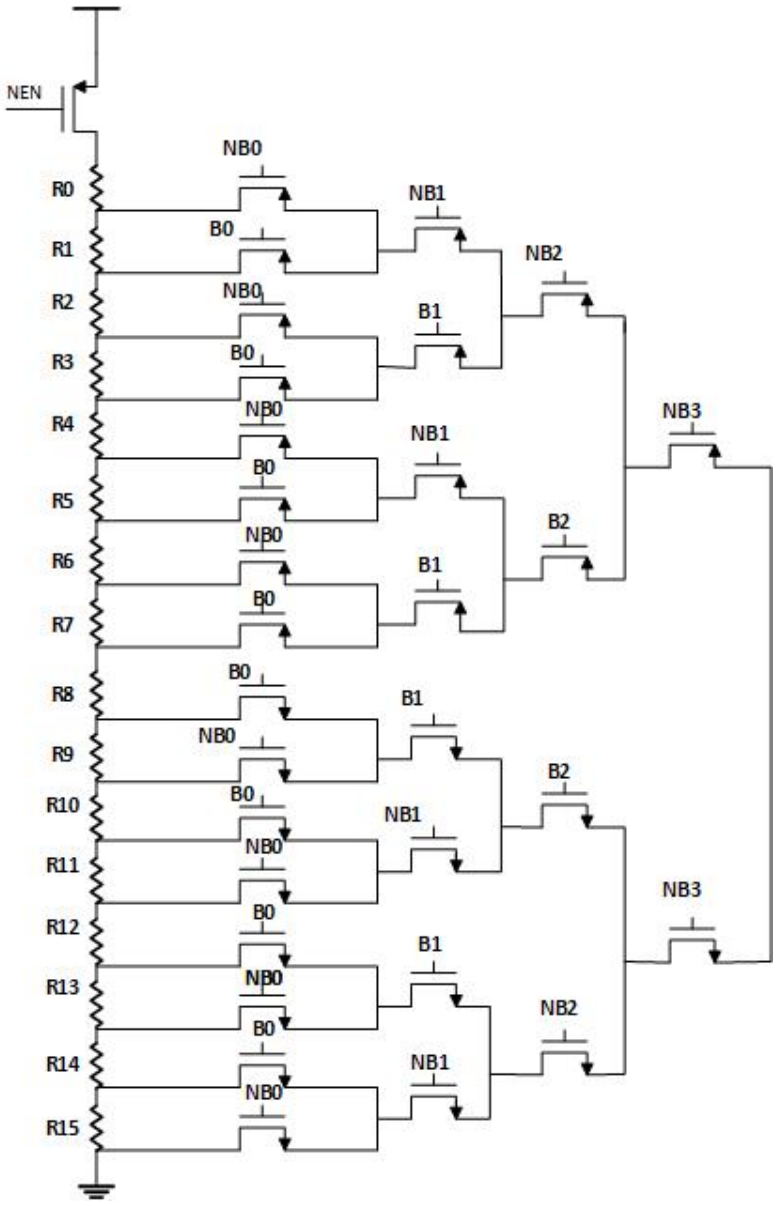

FIGURE 2.8: Circuit of 4-bits Resistive ladder DAC

2.3.2 Operational Amplifier Design

A voltage buffer is needed as part of the gate biasing in order to decrease charge re-distribution and leakage from the RF to the biasing point. The buffer is implemented by an Operational Amplifier (OPAMP). The opamp is shown in Figure 2.9 and needs to consume very low power as its power consumption is part of the transmitter power consumption, which affects the efficiency. The opamp operates in sub-threshold, which

requires larger width to increase the gain but this increases the parasitic capacitance. Supporting circuits such as a current mirror and reference are designed and shown in Figure 2.10 and 2.11, performance results are given as follows.

Phase Margin=65.7 Deg at freq=123 KHz and the Gain Margin is 40 dB at freq=1.9 MHz

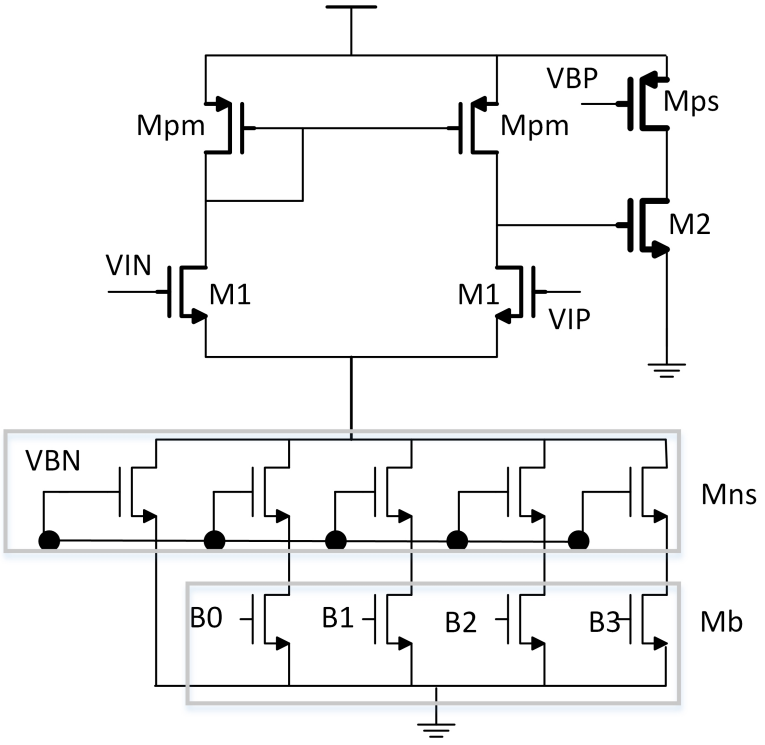

FIGURE 2.9: Low power Opamp with programmable current source

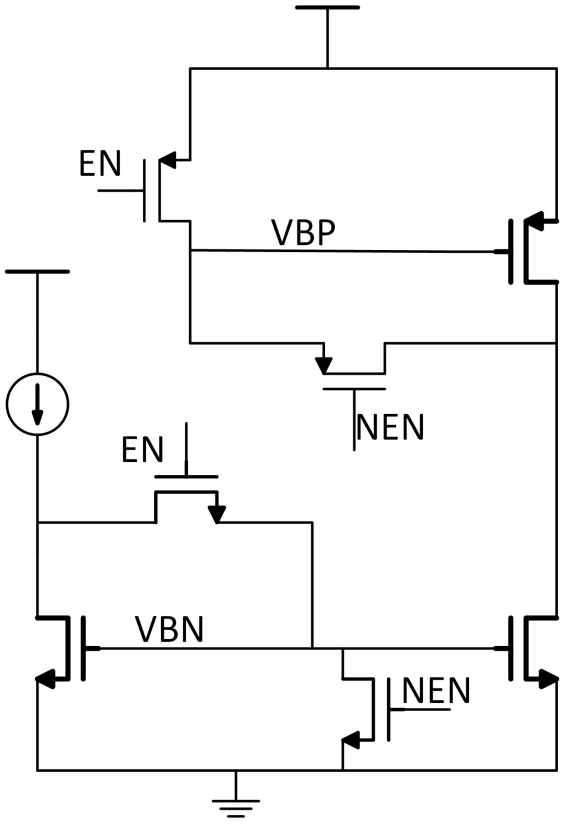

FIGURE 2.10: current mirror with Enables

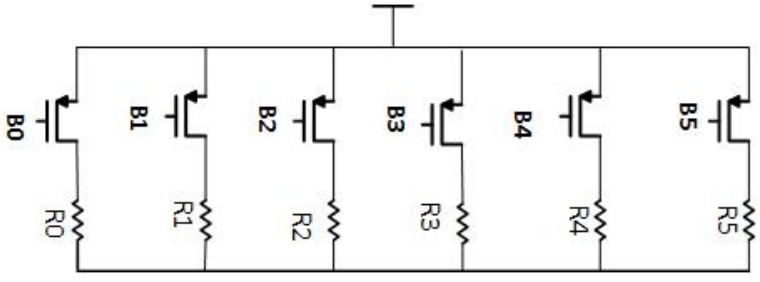

FIGURE 2.11: Resistor-Based low-Current Reference

2.4 Crystal Oscillator

This section describes the design of the Crystal Oscillator(XO) utilizing MEMS crystal and a CMOS circuit. This crystal drives the Pre-Drivers of the PA and the receiver, hence their loading capacitance should be considered. Usually, crystal oscillators have a very high-quality factor which means they have a high Figure of Merit (FOM) and good phase noise performance. The bonding wires introduce an inductance and a capacitance effect (Appendix A) on the crystal which may give rise to parasitic oscillations. Reducing the power consumption of the crystal oscillator while taking care of the parasitic oscillation modes is the main challenge of the design. The efficiency of the PA increases as its input swing increases. Therefore, to have the maximum transmitter efficiency, it is required that all the nodes including the output of the oscillator have the maximum possible RF signal amplitude to avoid the need for any extra gain stages.

2.4.1 The MEMS Crystal

The Film Bulk Acoustic Resonator (FBAR) is a MEMS-Based crystal and it is modeled as in [20] which is called the Modified-Butterworth Van Dyke (mBVD) model and is shown in Figure 2.12. The model of the crystal is similar to the model of the crystal quartz oscillators.

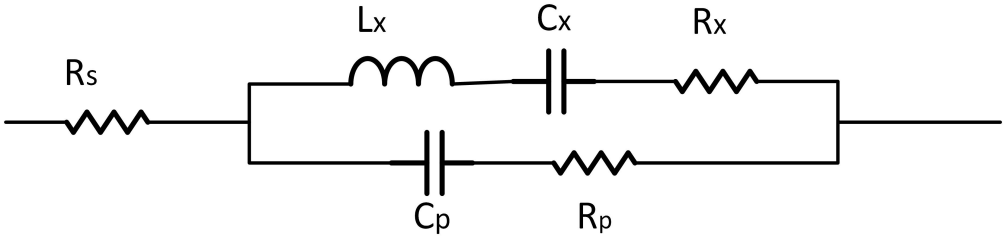

FIGURE 2.12: Equivalent Circuit model of the FBAR MEMS Resonator

TABLE 2.1: FBAR mBVD Model Parameters

R_x (Ω)	R_p (Ω)	R_s (Ω)	C_x (fF)	C_p (pF)	L_x (μ H)
1.424	0.100	0.814	33.43	1.210	0.1235

2.4.2 Crystal Oscillator Topologies

There are many techniques to generate negative resistance, which have been developed and have matured for years. Here we present a quick survey of the different implementations with a specific focus on low power applications. The single transistor crystal oscillator is shown in Figure 2.13. It can be classified into Pierce, Colpitts and Santos according to the position of the common point.

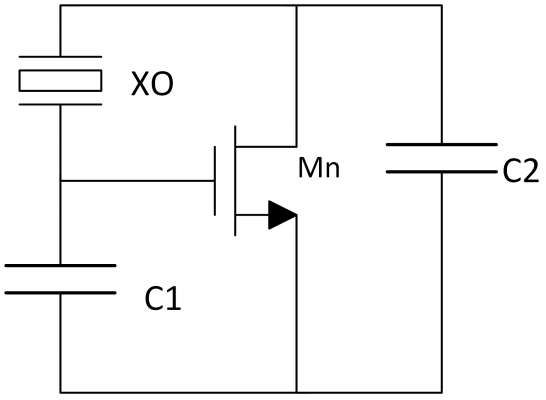

FIGURE 2.13: Basic Three-Point Crystal Oscillator

According to [21], supply and substrate noise on the analog and RF circuits are increased in an IC with digital circuits. Therefore, it is advantageous to use a differential topology. As shown in Figure 2.13, making the gate or the drain the common terminal will produce **Single Ended Colpitts** and **Single Ended Santos**. Both have one terminal of crystal to ground so it will face more substrate noise. Therefore, it is preferred to use a topology where the crystal is not used as a single common terminal to ground or supply, such as, the Pierce XO.

Single Ended Pierce

It is a commonly used XO topology due to its simplicity in design and good performance regarding power consumption and phase noise. The implementation is similar to Figure 2.13 except for the addition of a PMOS current source and a feedback resistance that are used for biasing. The crystal is connected between the gate and the drain of the transistors, and it does not share any connection to supply or ground. Thus, phase noise performance is better than the other single ended architectures. Low-voltage and low-power implementation have been reported in [22] which consumes 300 μW from a 1V supply. The forward-biased bulk technique is used for the Pierce in [23] to decrease the power consumption by 41 % and it can work with very low supply voltages. The major

disadvantage of this type is the very low swing it provides, so another stage with high gain should be provided to increase the swing amplitude. To implement a high-frequency amplifier, a current consumption in the order of 100 μ W may be needed, which degrades the overall transmitter efficiency.

Differential Colpitts Crystal Oscillator

One advantage of using a differential crystal oscillator is the ability to generate accurate BPSK modulation or drive a differential power amplifier. The differential Colpitts crystal oscillator is shown in Figure 2.14. This circuit was designed based on the differential colpitts VCO that is shown in [24] and the adaptation for crystal oscillators that were done by [2]. It works with low supply and consumes a minimum current, but the swing

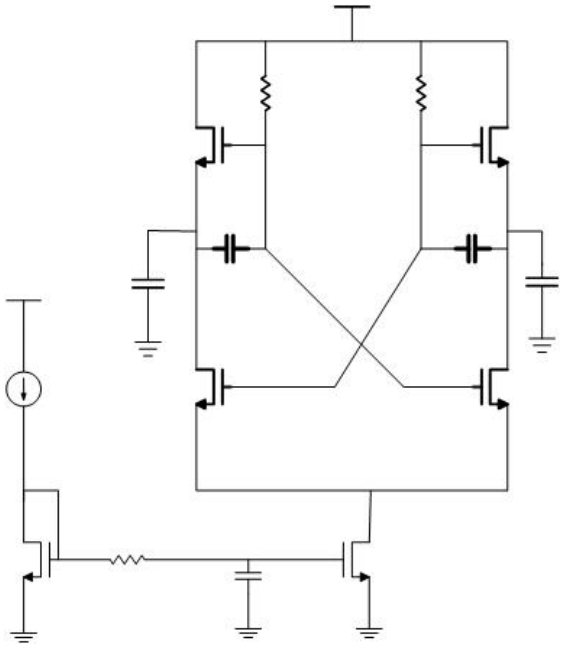

FIGURE 2.14: Differential Colpitts crystal oscillator [2]

is less than peak to peak.

Differential Cross-Coupled Crystal Oscillator

The traditional cross-coupled VCO as shown in Figure 2.15 works as follows. It consists of a cross-coupled pair of transistors or back-to-back inverters with an LC tank resonator. The cross-coupled pair represents a wide band (0 Hz up to high frequencies) negative resistance inversely proportional to gm, hence the current. The parallel tank resonates at

one frequency. The inductor is a short circuit at DC frequency providing a bias current path.

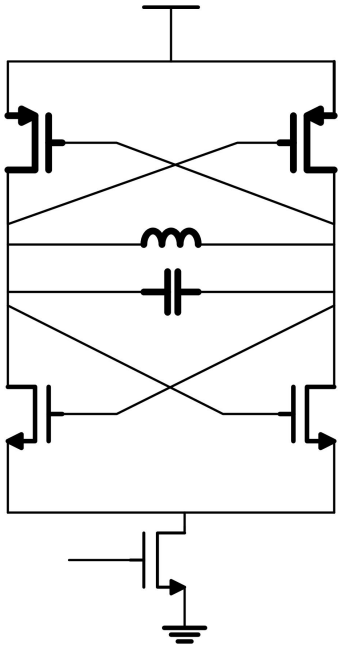

FIGURE 2.15: Differential Crystal Cross-Coupled VCO

Implementing differential crystal oscillator using a cross-coupled pair faces some troubles as the XO represents high impedance at DC. Unlike inductors, the DC high impedance causes it to be unstable and latches up similar to a comparator. Also, a DC current bias is needed to control the common-mode point without de-tuning the resonator. The original implementation is based on [25] which used capacitors and current source to solve the previous mentioned issues . This thesis [3] provides another implementation of the differential oscillator, which is shown in Figure 2.16. The drawback of the previous circuit is the reduced swing due to the current source.

Inverter-Based XO

Figure 2.17 shows the implementation of this circuit which uses a NMOS and a PMOS transistors as gain elements instead of using a PMOS as a current source in the single transistor pierce oscillator. Hence, it is more preferred than single transistor Pierce for low power applications, as it has higher gm as shown in Equation 2.5 .

$$gm_{eff} = gm_n + gm_p \tag{2.5}$$

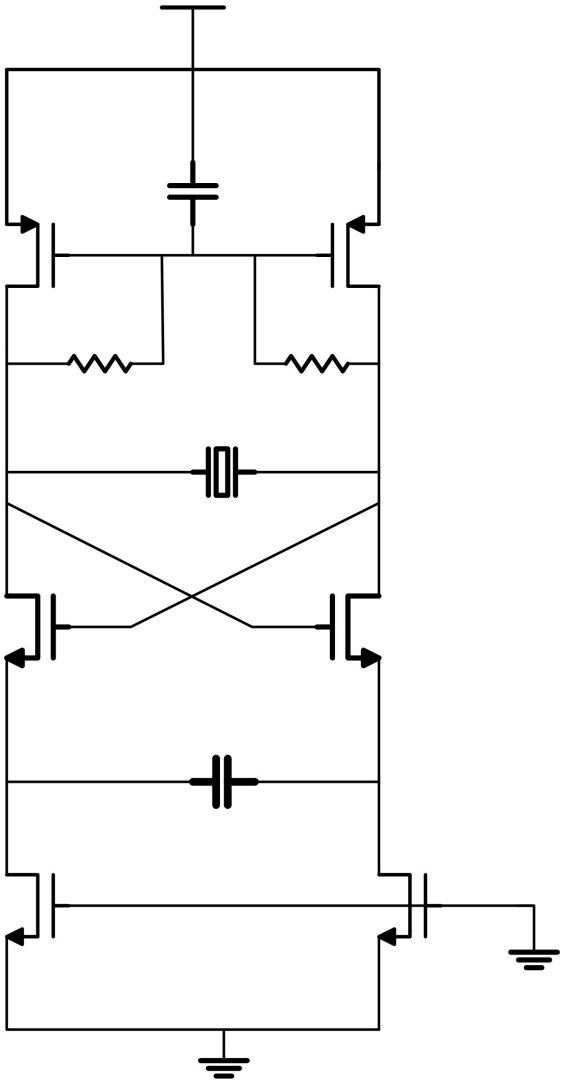

FIGURE 2.16: Differential Crystal Cross-Coupled Crystal Oscillator[3]

Decreasing the minimum required gm for the oscillation to sustain, decreases the current consumption which is the main specification for our applications. The resistance is needed to self bias the gate at mid-supply voltage, and the final swing amplitude at the drain is peak to peak voltage. This rail to rail oscillation comes due to the absence of current source to control the current.

2.4.3 Design of The CMOS Crystal Oscillator

The design of high-frequency oscillators is generally more sophisticated than their lower frequency counterparts, as they are more susceptible to parasitic elements, which makes it harder to well define the frequency of oscillation [26]. Conventional methods such as feedback analysis are necessary but not always sufficient. However, the root locus analysis

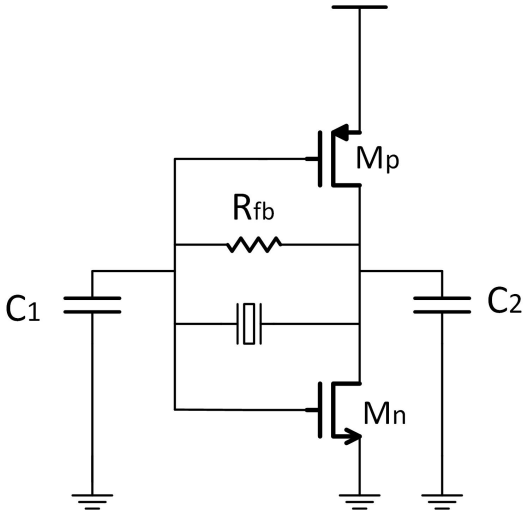

FIGURE 2.17: The Inverter-Based XO

will provide more accurate results. The design of the inverter-based XO as shown in Figure 2.17 starts by calculating the desired oscillation frequency and the corresponding loading capacitors. Figure 2.18 shows the equivalent circuit of the inverter-based XO after using the crystal model and neglecting the series resistance loss Rs. The analysis can be done similar to [6] with only slight difference in the final value of circuit parameters.

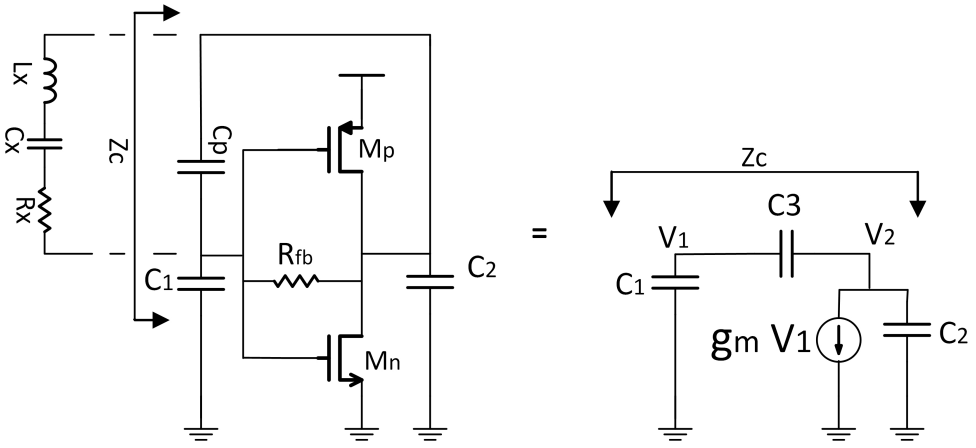

FIGURE 2.18: Analysis of the Inverter-Based XO

The oscillation frequency relationship to the circuit parameters is given by the equations 2.6 & 2.7 as given in references [27] & [6].

$$\omega_{osc} \approx \omega_s \sqrt{1 + \frac{C_x}{C_{circuit}}} [27] \tag{2.6}$$

$$C_{circuit} = \frac{(gmC_3)^2 + \omega^2(C_1C_2 + C_1C_3 + C_2C_3)^2}{gm^2C_3 + \omega^2(C_1C_2 + C_1C_3 + C_2C_3)(C_1C_2)} [6] \tag{2.7}$$

Where C_1 and C_2 represent the drain and the gate capacitance of the crystal respectively as shown in Figure 2.17, C_3 is the parasitic capacitance between the drain and the gate, $C_{circuit}$ is the equivalent capacitance of the circuit, ω_{osc} is the final oscillation frequency, ω_s is the series resonant frequency of the resonator, C_x and R_X are the capacitance and the resistance of the series resonant branch of the FBAR crystal. t_{osc} is the period of oscillation and Q is the quality factor of the resonance in the resonator.

The equations 2.8 and 2.9 give the critical value of the transconductance required to ensure that oscillations take place. Another design parameter is the optimal transconductance which is given by the equation 2.10.

$$gm_{crit} = \frac{C_1C_2}{2C_3^2R_X} - \sqrt{(\frac{C_1C_2}{2C_3R_X})^2 - (\frac{\omega^2(C_1C_2 + C_3C_2 + C_3C_1)^2}{C_3}}[27] \tag{2.8}$$

If $C_1 = C_2 = C$ then equation 2.8 is reduced to:

$$gm_{crit} = \frac{C^2}{2C_3^2R_X} - \sqrt{(\frac{C^2}{2C_3R_X})^2 - (\frac{\omega^2(C^2 + 2C_3C)^2}{C_3^2}}) \tag{2.9}$$

$$gm_{opt} = \omega \times (C_1 + C_2 + \frac{C_1 \times C_2}{C_3}) \tag{2.10}$$

The optimal transconductance is generally larger than critical transconductance, so for low power application and as the current reduces more with lower transconductance values, the operation around critical transconductance is preferred.

Equation 2.11 indicates that the startup time of the crystal oscillator is a function of the current consumed by the crystal in the form of $R_{circuit}$. Increasing the current consumption will decrease the startup time.

$$t_{startup} \propto \frac{L_x}{-(R_{circuit} + R_X)} = t_{osc} \times Q \times \frac{R_x}{-(R_{circuit} + R_X)}[6] \tag{2.11}$$

The forward bulk biasing is used to reduce the power consumption that is required for certain gm_{crit} as in [23]. A unit crystal inverter with bulk biasing is shown in Figure 2.19. The bulks of the NMOS and PMOS transistors are biased separately from two different 4-bit DACs.

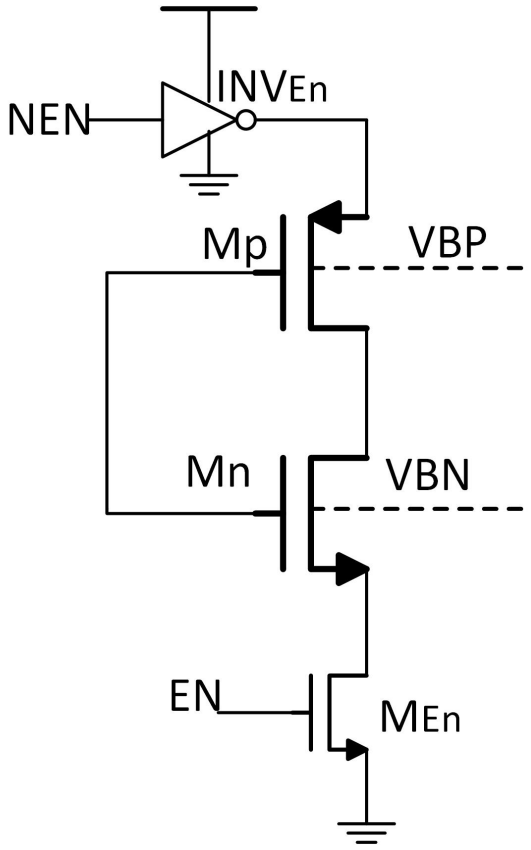

FIGURE 2.19: A Unit Crystal Inverter of the XO

Three units as shown in Figure 2.20 are used to control the gm and give exactly the minimum required gain to oscillate at any corner or supply voltage between 0.7-0.5 V. The inverters are connected in parallel and all three share the same DACs that bias the bulk i.e. sharing the bulk of PMOS and NMOS. Each one of them uses a different enable control signal. The drain of the oscillator drives the loading capacitor of the pre-driver of the PA, BPSK modulator and the mixer driver. The gate of the MOSFET is connected to the circuit capacitors C_1 as shown in Figure 2.20. C_1 can be divided into oscillation tuning capacitors (C_{1a} and C_{1b}) and the MSK capacitor bank. The oscillation tuning capacitors are used to make sure the gain required for the parasitic oscillations to dominate is much higher than the gain for the desired oscillation. Hence, the parasitic oscillations is damped and the required mode sustains and dominates the output.

Parasitic Oscillation: The package, bonding wires and RF PAD parasitics can affect the oscillator and can initiate a parasitic oscillation mode. High frequency oscillators, may suffer from multimode oscillations, specially due to the parasitics effect on circuit. The root locus analysis of feedback circuits is used to make sure that the desired oscillation mode is the dominant one from all other parasitic modes. The problem of parasitic

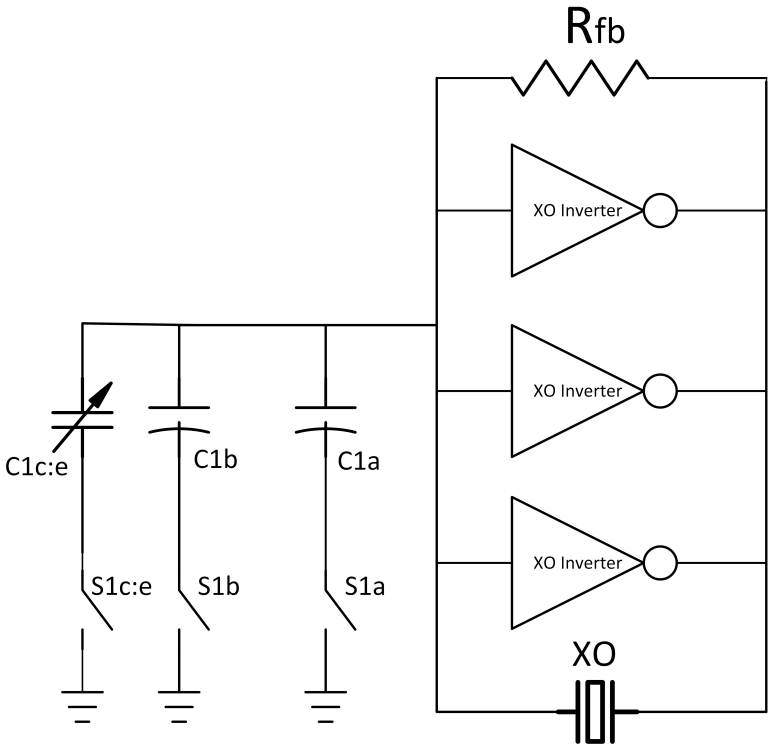

FIGURE 2.20: The complete Crystal oscillator

oscillations is discussed more in Appendix B. This appendix provides all the effects on the crystal after the addition of the parasitic components. Also, during spectre simulation an estimation of the parasitic losses as given in Appendix A is used to simulate their effect on the oscillator.

MSK Modulation

In traditional FSK we use signals of two different frequencies f_L and f_H to transmit a message m=0 or m=1 over a time of T_b seconds. Continuous phase frequency shift keying (CPFSK) is a version of FSK where there is an integer number of periods of the signals inside each T_b period. This can be done by choosing f_L and f_H to be an integer multiple of the inverse of T_b. When the difference between the two frequencies f_L and f_H is the smallest possible difference that keep the orthogonality of the two message, representing signals over one bit interval the modulation is called MSK. For MSK modulation, the frequency relationship to the bit period can be written as Equations 2.12, 2.13 and 2.14.

$$F_L = \frac{F_{center}}{2} - \frac{1}{4 \times T_b} \tag{2.12}$$

$$F_H = \frac{F_{center}}{2} + \frac{1}{4 \times T_b} \tag{2.13}$$

$$F_H - F_L = \frac{1}{4 \times T_b} \tag{2.14}$$

Where F_L is the lower frequency of the MSK, F_H is the highest frequency of the MSK and F_{center} is the center frequency of the oscillation.

For BAN applications, data rates as high as 1 Mb/s are needed, so the frequency separation between F_L and F_H is 500 KHz. Changing the frequency can be mainly done by adding and removing a capacitor from the loading capacitors of the oscillator. A high quality capacitor bank is designed to tune the center frequency by the required amount for the modulation. The bank of capacitors should be designed with a high-quality factor in order not to decrease the quality factor of the FBAR and thus increasing the power consumption.

The MSK capacitors are implemented as shown in Figure 2.20 and they consist of three different capacitors.

2.5 Pre-Driver

Driving the PA transistors directly from the LO generator, reduces the power consumption overhead of the driver. However, the gate to drain capacitance (C_{gd}) of the power amplifier will need to be isolated from the LO generator to prevent kickback noise and also to enhance system stability. Therefore, an intermediate stage needs to be used between the power amplifier and the LO generator. Three paths are needed to implement OOK/MSK and BPSK modulators. The main single path is used for OOK/MSK modulation and the other two paths are needed for the BPSK modulation.

Driving the PA gate capacitance (C_{gs}), which is equal to 300 fF due to the large size of the PA, by an inverter chain as a buffer as shown in Figure 2.22(a) consumes a lot of power as calculated by equation 2.15.

$$P = C_l * V_{DD}^2 * f \tag{2.15}$$

With 0.5-V working at 2.4 GHz and driving 300 fF, the power consumption is 180 uW, which is a large number compared to the transmitted output power.

The NMOS-based circuit is shown in Figure 2.21 and it uses an inductor Lt to tune the gate capacitance of the PA at the cost of consuming a static current. Figure 2.22 (b) shows the inverter-based driver called resonant load driver, which was proposed by [28]. It has a peak-to-peak amplitude and a small static power consumption, which is only to compensate the inductor loss [6]. Its power consumption is given by the equation 2.16.

$$P = V_{DD} I_{ShortCircuit} + \frac{V_{DD}^2}{8 R_{p,ind}} \tag{2.16}$$

The Core Circuit: It is the current-reuse amplifier shown in Figure 2.7. It has more gm than the single NMOS transistor amplifier, which means it consumes less power to get the same gain, but with larger parasitic capacitance. The gate biasing is done to decrease the required width to get the required gm i.e. less parasitic capacitance and also less power consumption. Operating from a 0.5-V in the weak inversion region makes the gate biasing necessary to overcome the threshold voltage with an acceptable width. The inductor value is set to tune the total capacitance at the input of the PA including the parasitic capacitance.

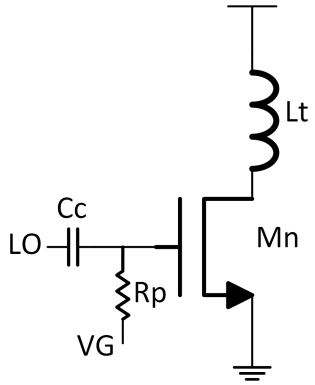

FIGURE 2.21: The NMOS-Based Pre-Driver of the PA

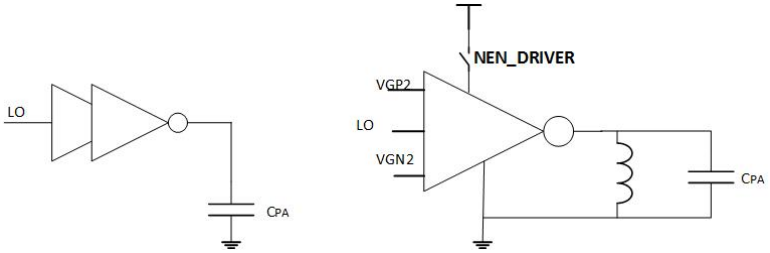

FIGURE 2.22: (a) Inverter Chain (b) Inductor-Based Driver

2.6 OOK Modulator

The simplest OOK modulator is a switch in the path of the RF signal. Placing the switch after the crystal oscillator, a degradation in the amplitude of the RF signal will be introduced, which can be reduced by using a high-supply voltage. This is not suitable for our application. Another technique is to decrease the gain of the RF stages, which are pre-driver and the PA by controlling the gate biasing. Also, supply-enable transistors may help to implement this function. A combination of both of them is used to achieve the required function of fast 1MHz switching and a small off-mode voltage swing level. Figure 2.23 shows the path of the OOK modulated signal from crystal to the output.

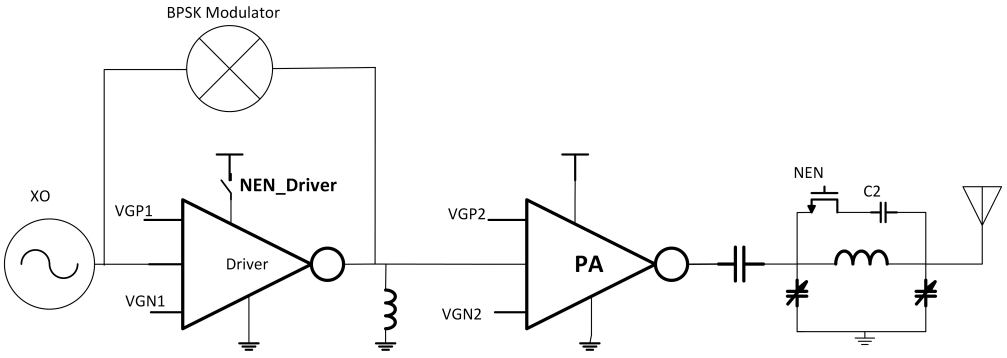

FIGURE 2.23: The Path That Implements OOK Modulation in the Tx

The gate biasing of the PA changes on two cases only as shown in Figure 2.24. In the first case, the transmitter is working and either sending the carrier, modulating it with BPSK or MSK. In the second case, the transmitter is working and OOK modulation is used: in this case, the PA should be on or off during the modulation bits one or zero. The biasing variations can be done by using simple switches, but when the capacitance is large and switching speed is fast we need to stop the charge leakage. Charge leakage and redistribution happens in the DC biasing circuits, so an opamp is used to isolate gate biasing DAC from the biased node. The capacitor at the output of the OPAMP is used to filter the DC voltage at the output.

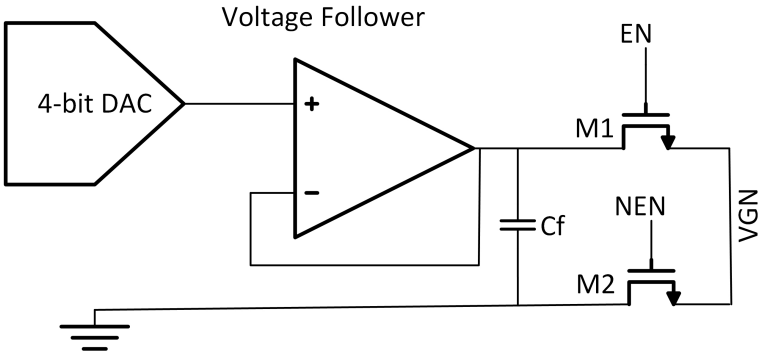

FIGURE 2.24: The NMOS Gate Bias Generation Implemented by Switches and a DAC

2.7 BPSK Modulator

The BPSK modulator is shown in Figure 2.25 and it is implemented by making two paths with 180 degrees phase difference by adding an inverter to a single path. The second path will need a delay-equalizer to the inverter delay which can be implemented by either a transmission gate or a capacitive load, but a transmission gate is chosen here. The load of the transmission gate and the inverter i.e. the second inverter is the same for both. Hence, they both need to have equal ON-resistance to have equal total delay.

The main circuit is the current-reuse amplifier which is similar to Figure 2.26 to overcome threshold voltage at low supply operation. The supply and the ground enables are shared to reduce the overall area. Also, some of the DACs are reused to decrease the total transmitter area. The input is shared and it is driven from the LO Driver which is a driver used after the LO to drive the BPSK modulator and is shown in Figure 2.26. The

last stage of the BPSK modulator is to drive the PA which is shown in Figure 2.27. The last stage consists of two inverter-amplifier where only one of them works at a time.

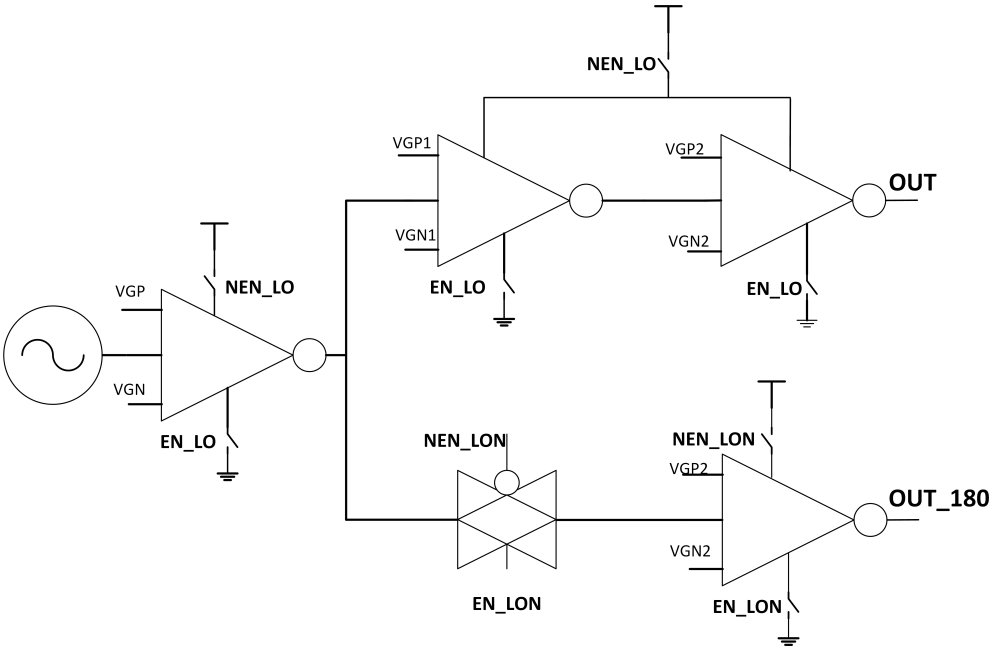

FIGURE 2.25: The BPSK Modulator Circuit

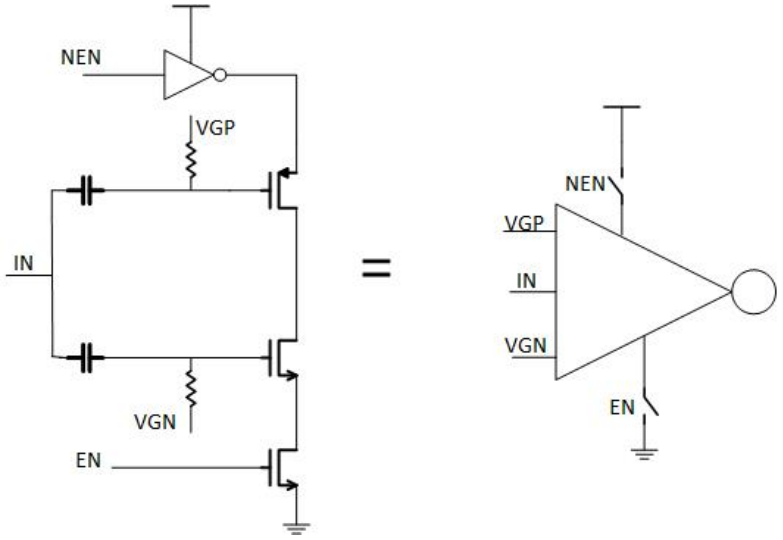

FIGURE 2.26: The Crystal Oscillator Driver for the BPSK Modulator

2.8 Digital Control of the Modulators

The purpose of this section is to transform the main modulation terms into circuit control terms. For our modulation schemes, modulation terms such as baseband data, carrier and type of modulation are transferred into circuit design terms such as enable/disable

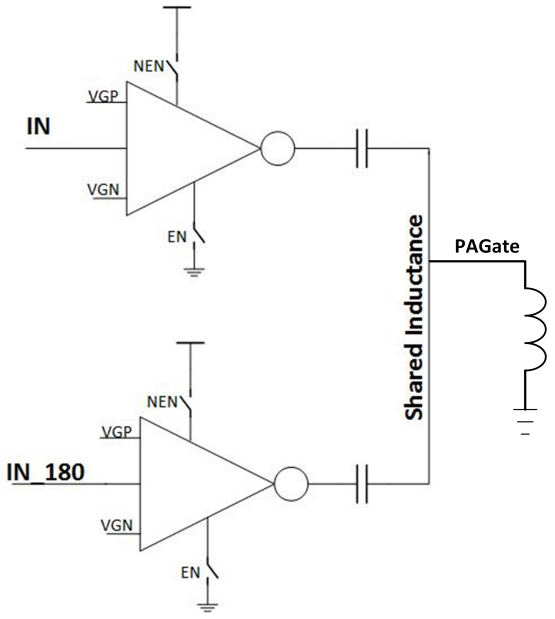

FIGURE 2.27: The PA Pre-driver of the BPSK Modulator

switches and other control signals. This mapping depends on the implemented modulators and system architecture.

Figures 2.28, and 2.29 show the mapping from modulation signals to three control signals named OOK_2, OOK_3 and OOK_4. Using these signals for the OOK modulation, modulation can be done through controlling the gate biasing of the PA, the driver enable-supply transistor and the gate voltage of the pre-driver. Three controls can be chosen separately, depending on the acceptable amount of the signal amplitude in the off-state.

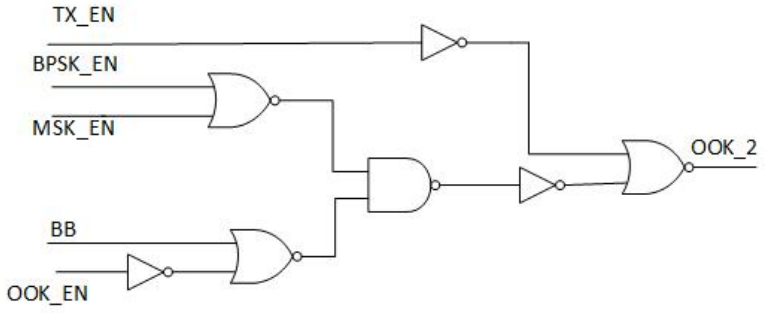

FIGURE 2.28: The Digital Control Signal of the OOK Modulation to control the gate of the PA

The control logic of the BPSK modulator is shown in Figure 2.30. The BPSK and the OOK/MSK modulators do not share the same path, which means that one path will work at a time, this is controlled by B<1>. The BPSK modulator needs to select between

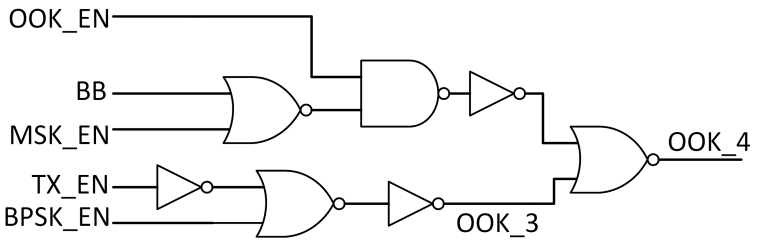

FIGURE 2.29: The Digital Control Signal of the OOK Modulation to control the Pre-driver

the two paths depending on the transmitted baseband data bit, which is controlled by B<5> and B<4>.

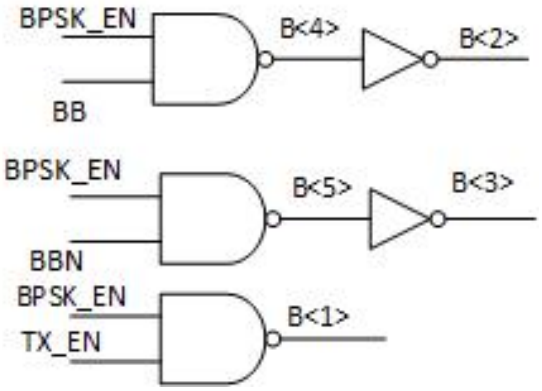

FIGURE 2.30: The Digital Control Signal of the BPSK Modulator

2.9 Power Amplifier

The RF Power Amplifier (PA) has the function of delivering RF power efficiently to the 50-Ω antenna. The power amplification usually comes by converting the DC power from the supply into RF power. The PA usually consists of an impedance transformation network and an amplification stage. The transformation network is needed to maximize the efficiency while delivering the desired output power by converting the antenna impedance into the optimum load for the amplification stage. The amplification stage is an active stage, which is used to drive a resistive impedance load.

2.9.1 ULP PA Topologies Survey

The PA topologies should be classified depending on the output power level. If the high output power PAs are used at back-off to get low output powers, they would be inefficient [29]. For WSN applications, efficient power amplifiers at low output power have been attempted be designed as given in [30][31] [32][33][34]. However, their output power is higher than that required for BAN applications. For ULP PAs, reference [10] provides a good survey for the previously implemented transmitters. It introduces the term of low-power (0 dBm or below) and typical (+10 dBm to +30 dBm) PA. For a low power PA, the impedance transformation ratio N from the antenna (50 Ω) to the PA is larger than unity, unlike most high-power PAs where $N < 1$.

Low-Power Class E PA

It is a modified version of class E PA, as shown in Figure 2.31. It was designed for WSN applications at 0 dBm output power and it achieves an efficiency of 53.5 % and the supply is 0.5-V. The driver needs to have a square wave input from a 1.2-V supply inverter driver. It uses three inductors, which consumes a large area [4].

Low-Power Class F PA

Figure 2.32 shows the modified class F PA, which is modified to give optimized results for low-power applications [5]. It uses three inductors for the PA and multiple supplies as the input comes from a different domain. It was designed for -20 dBm and achieves 42 % efficiency working at 315 MHz which decreases at higher frequencies.

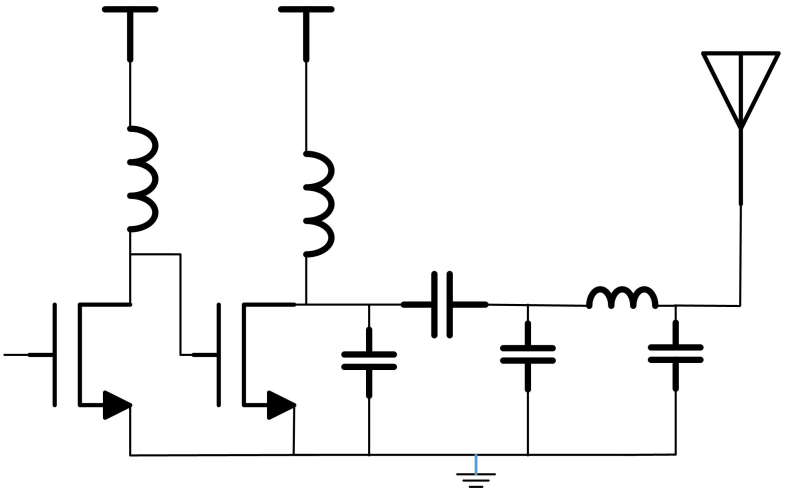

FIGURE 2.31: Low-Power Class E PA [4]

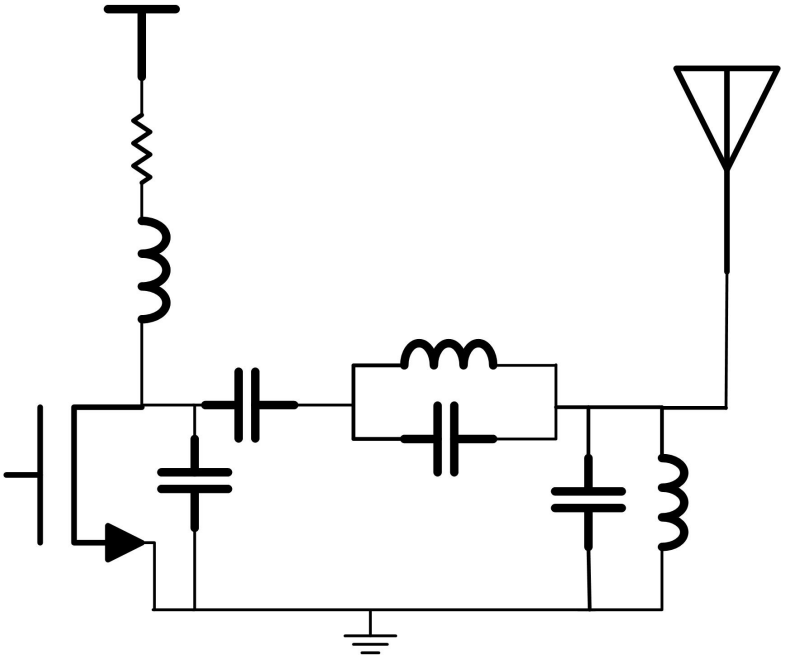

FIGURE 2.32: Low Power Class F PA [5]

The Push-Pull PA

Figure 2.34 shows the push-pull PA, which is proposed by [6], and it uses an inverter instead of the NMOS-based PA shown in 2.33 that uses a choke inductor, therefore it has less swing at the drain. The amplitude of the voltage swing for the push-pull PA is half the amplitude of the voltage swing for the NMOS-based PA which leads to a factor of 4 as relative power reduction. The design equation of the push-pull PA is equation 2.17, however, the design equation of the NMOS-based PAs is equation 2.18.

$$P = \frac{V_{DD}^2}{8 * R_L} \tag{2.17}$$

$$P = \frac{V_{DD}^2}{2 * R_L} \tag{2.18}$$

Where P is the output power, V_{DD} is the supply voltage and R_L is the impedance seen by PA. For the same output power, the push-pull PA requires less R_L which reduces the required impedance transformation ratio (N) more than the case if NMOS-based PAs is used. Thus, the impedance transformation network has a higher-quality factor than the one used in the NMOS-based PA [35]. Reference [6] was designed to work for BAN application with -10 dBm output power and 34 % efficiency as deduced from the reference. This PA is the chosen topology due to its high efficiency, simple design, and less area as only one inductor is needed.

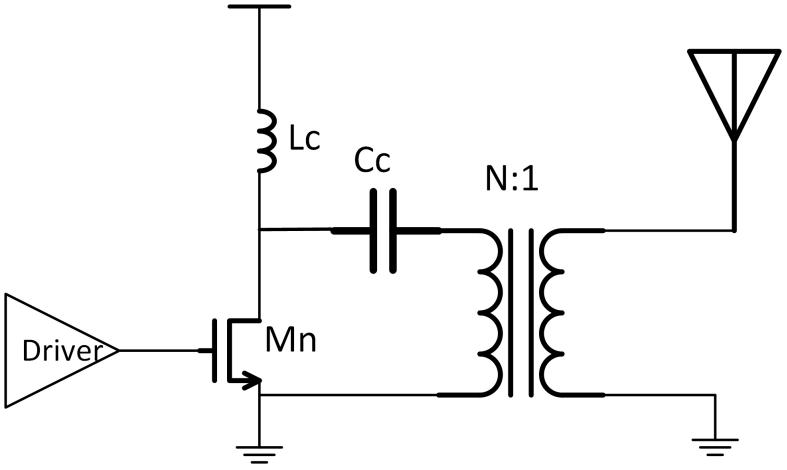

FIGURE 2.33: The NMOS-based PA Architecture with its Chocke Inductance

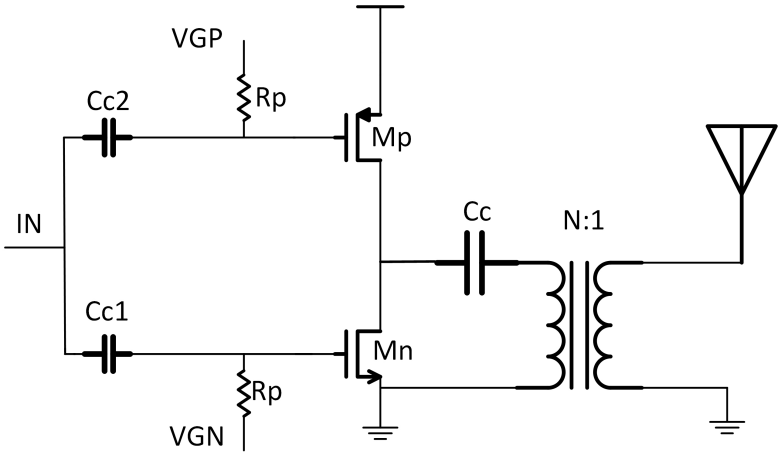

FIGURE 2.34: The Push-Pull PA Architecture Proposed in [6]

2.9.2 The Push-Pull PA Design Methodology

Using equation 2.17 for the design, the supply is chosen to be 0.5-V to increase the efficiency and to decrease the required transformation ratio. For a 100 μW (-10 dBm) output power, R_L is known and it is equal to 312.5 Ω, so the impedance transformation network can be designed. The width of the NMOS and PMOS and the gate voltages are designed together to give the maximum efficiency at the output while providing the required output power.

Impedance Transformation Network

The impedance transformation network is a passive network that is responsible for changing the antenna impedance into a suitable impedance for the amplifier to work at the full swing and high-efficiency mode. A fully integrated (on-chip) impedance transformation network was designed to save the cost of external components.
The package, bonding and ESD parasitics are modeled in Appendix A. These parasitics should be taken into consideration when designing the transformation network. Figure 2.35 shows that the input impedance seen by the impedance transformation network is calculated by considering all these parasitic effects. The input impedance is usually complex, but not real. The imaginary part can be resonated to show a real impedance. The real component is not equal to (50-Ω), in our case it is (65-Ω) which reduces the required impedance transformation ratio N.

Figure 2.36 shows the most common two types of transformation networks which are π and tapped impedance transformer. Microwave simulations, such as insertion loss,

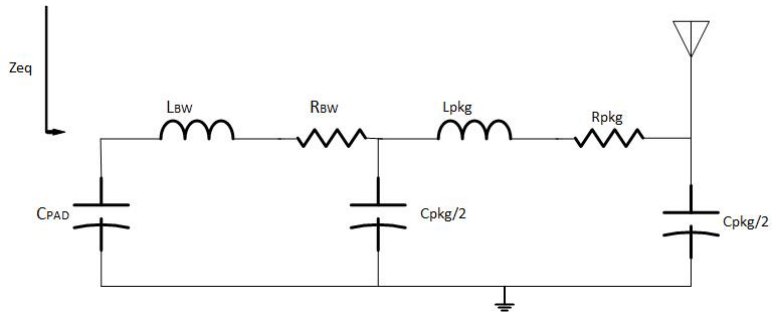

FIGURE 2.35: Equivalent Impedance at the Input of the Transformation Network

and return loss can help identifying the most suitable transformation network. Circuit simulations, especially after layout effects are done to design with the proper component values. From simulation results, the π network provides a higher efficiency than the tapped.

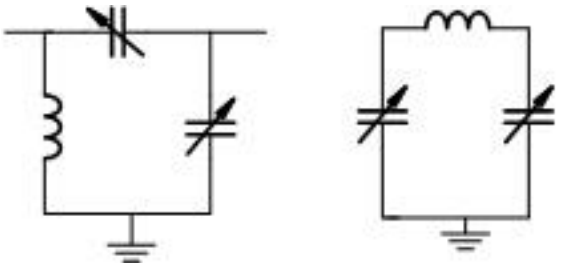

FIGURE 2.36: Impedance Transformation Network (a)Tapped (b) π

2.10 Transmit/Receive (T/R) Switch

The RF T/R switch can be divided into two separate transmit and receive switches. Separating the two switches could possibly make it easier to design each one individually. For the reception branch, it is considered a part of the Rx. In this section, the Tx switch is studied and the effects of the Rx branch is simulated at the end. The switch has been implemented with CMOS technology using integrated transistors and inductors. The RF Tx switch can be considered as a two-port network with the loss as insertion loss.

The important performance metrics of the RF switch for low-power applications are the insertion loss and the isolation loss as defined in [36].
Insertion Loss: The loss of the power between input and output ports. The insertion loss will decrease the output power level from the PA to the antenna, which affects the efficiency of the Tx.
Isolation: It indicates the amount by which the input port is isolated from the output port i.e. the amount of leakage between the two ports.

2.10.1 T/R Switch Topologies

Here, we are focusing on low-power low-voltage small-size CMOS switches, as they are suitable for our application. Reference [36] provides a good survey of T/R switches topologies that are currently used. The basic simple T/R switch consists of two-NMOS transistors placed in series with the transmit and receive paths (series topology). An ideal switch is an infinite impedance in the off mode and a short circuit in the on mode. The transistor in the on state should have a very small on-resistance, near zero, to decrease the loss in the RF signal (efficiency of the PA). In order to obtain a small on-resistance, the width of the transistor needs to be large and a high gate voltage is needed. A big transistor has a big off-mode capacitance value, which affects the matching of the RF block to the antenna, and may be unacceptable.

Series Switch

This is the simplest topology, as shown in Figure 2.37, it consists of two NMOS transistors as switches for each path. This switch is called the Single-Pole Double-Throw (SPDT) configuration. The control signal applied to the gates should have a minimum value for

the switch to be ON with a small on-resistance. Using the minimum value for the control switch i.e. threshold voltage, to get a small on-resistance the width of the MOSFET should increase a lot to effectively decrease the loss in the signal path (insertion loss). Increasing the width will increase the off capacitance of the switch which will affect the RF blocks.

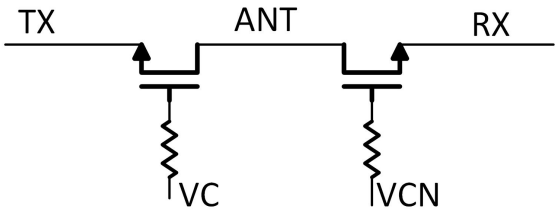

FIGURE 2.37: CMOS Series T/R Switch

Series-Shunt Switch

Figure 2.38 shows a series-shunt SPDT T/R switch. The addition of two NMOS transistors makes a fast path for the unwanted signal to the ground, which improves the isolation but degrades the insertion loss. Also, higher parasitic capacitance loads the previous stage with a higher value, due to the addition of two-transistors.

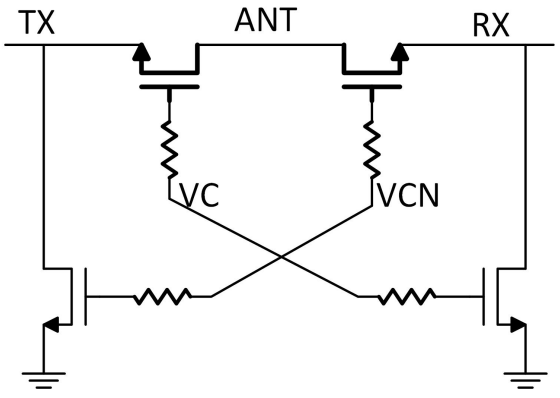

FIGURE 2.38: CMOS Series-Shunt T/R Switch

Low Voltage Switch

RF transistors are not well modeled or the model is very complicated [37], therefore, MOSFET transistors as RF switches on the path of the signal are not that preferred, as their loss is hard to be modeled. It needs either a high gate voltage or extra large device sizes for the switch, which is not suitable for ULP transceivers with low supply voltage.

LC resonators can play the role of an on/off switch. At a single frequency, a short circuit can be implemented by series resonance while an open circuit can be implemented by parallel resonance circuits [7]. Figure 2.39 represent the main idea of the switch which is based on a combination of series and parallel resonances for each single switch. Also, the gate control voltage can be decreased below the minimum voltage needed for other applications i.e. low-voltage operation are easier to achieve. The inductor loss, in the form of a series resistance, represents the main issue. However, the removal of one series switch during the on mode represents the main advantage.

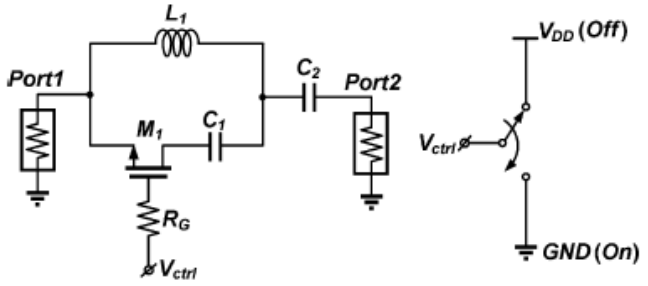

FIGURE 2.39: Resonator-Based Switch [7]

The full CMOS T/R switch [7] is shown in Figure 2.40. It consists of multiple of inductors, which is not suitable for small-area applications.

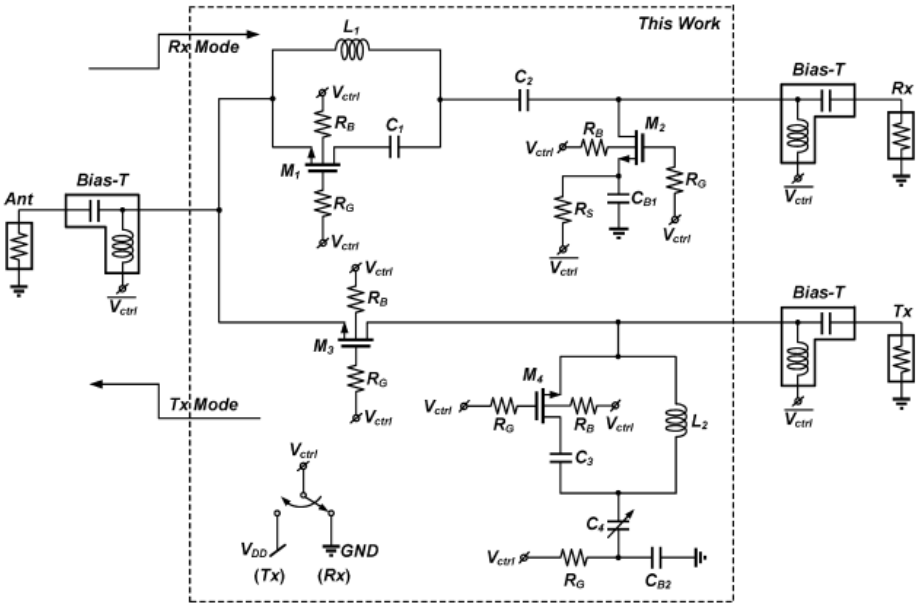

FIGURE 2.40: CMOS T/R Switch Utilizing LC Resonators for Ultra-Low-Voltage Operations [7]

2.10.2 Suggested Low-Area Low-Voltage RF Switch

For low-voltage, low-power applications, the design should manage to have a very low insertion loss in the RF signal. The series and parallel resonance concepts are used to implement the switches, because they are amenable to low-supply voltage. The on-switch is not always needed, i.e. the Tx is connected by default and only an open circuit is just needed to disconnect it from the output. The parallel tank can be used to implement the off-switches function. The tank behaves as open circuit at the resonance frequency which is the off-switch. This can work if a switch is added in the path of the parallel tank to disable/enable the switch. The switch is added in series with the capacitance not the inductance, due to the small quality factor of the integrated inductors with respect to the integrated capacitors. The switch is needed just to disconnect the antenna from the core of the PA. Thus, only one tank is needed, and the series switch tank is removed, which reduces the area. Figure 2.41 shows the idea where the parallel tank consists of L, C2 and the (NEN transmitter/EN tank) switch. Since it represents an open circuit at only a single frequency it will present a narrowband switch.

For small-area designs, the capacitance area is acceptable in size, but the inductance is the main area limitation. Thus, if we can utilize any existing inductor and make the tank work in the off mode, we can get the same performance with less area. Since usually, the last stage is a PA, which uses an impedance transformation network to enhance its efficiency, we can find an inductor easily. Also, the off capacitance of the switch can be modeled as part of the impedance transformation network. The inductor losses are not a new issue as they are already considered in the impedance transformation network. Avoiding the series switch that was in the RF signal path reduces the insertion loss.

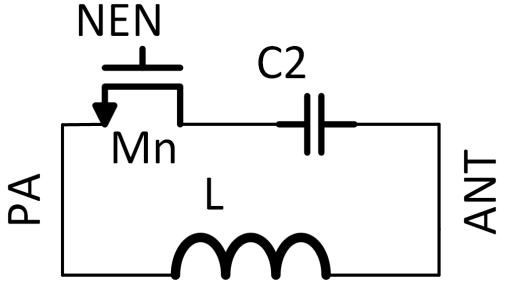

FIGURE 2.41: Basic idea of the Switch

The most common impedance transformation networks for the PA are the π and tapped impedance transformers. Ideally speaking, they do not have a big difference between

them in terms of their off switch performance. The idea can be implemented with both kinds of impedance transformation networks, i.e. the inductor can be in a signal path such as (π) shown in Figure 2.42(b) or have one common terminal to a DC source such as (tapped) shown in Figure 2.42(a). Practically speaking, there are small differences in the insertion and the isolation losses due to the non-idealities of the switch, layout wires, and passive components, which affect the different networks in a different ways. For the Tx path, the proposed switch reuses the impedance transformation network inductance to implement the same function i.e. disconnecting the PA from the antenna. A capacitor and a switch are added in parallel with the inductor of the impedance transformer to make the Tx switch with no extra resonator. The switch is tested to operate successfully with just 0.7-V enable using the digital supply.

For the receiver part, the off-resistance should be very large to decrease the leakage from the transmitter, i.e. isolation loss. The Rx switch is designed as a series switch with a large width in order not to introduce high losses in the signal, however, its off capacitance should be taken into consideration while designing the matching network.

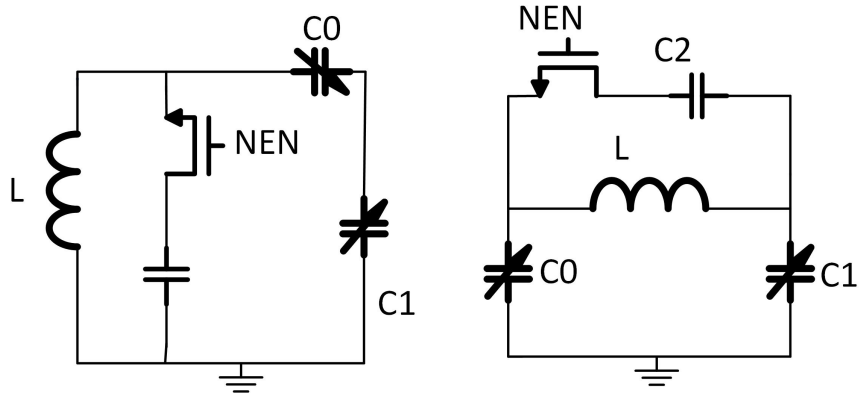

FIGURE 2.42: (a) Tapped Match with Tx Switch (b) π Match with Tx Switch

Chapter 3

Transmitter Integration and Final Results

This chapter provides the overall integration of the transmitter and its overall physical design (Layout). The first section defines the efficiency for the transmitter and each component which is important for low power designs and which will be used to compare different implementations in chapter 4. The second section provides the simulation results of the transmitter and it focuses on the implementable modulation schemes. The layouts of the circuits are shown in the third section. The parasitic effects of the layout are extracted and added to the circuit, then the circuit is re-simulated. The second simulation should give a very close result to the measurement results.

3.1 Transmitter Simulations

The most important performance metrics of the transmitter are the efficiency and the modulation schemes.

PA Simulation Results

Simulation shows the drain efficiency of the PA including all parasitic and biasing is 47 %. The matching impedance transformation and the transmit switch account to 80 % drop in the total efficiency as simulated by the circuit simulator. Then, a considerable drop in the efficiency occurs in the core to give an efficiency of 48 %. The power consumption

of the biasing circuit is equal to 10 μW. After parasitic extraction, this number drops to 42 % due to the layout effects.

Carrier Transmission

The transient response of the FBAR crystal oscillator when the supply is 0.5-V is shown in Figure 3.1. The startup time of the oscillator is less than 0.4 μs and the peak to peak amplitude of oscillation is nearly 0.5-V, which is the supply voltage. Zooming in the X axis, Figure 3.2 can provide a more clear view of the oscillation and its period of oscillation.

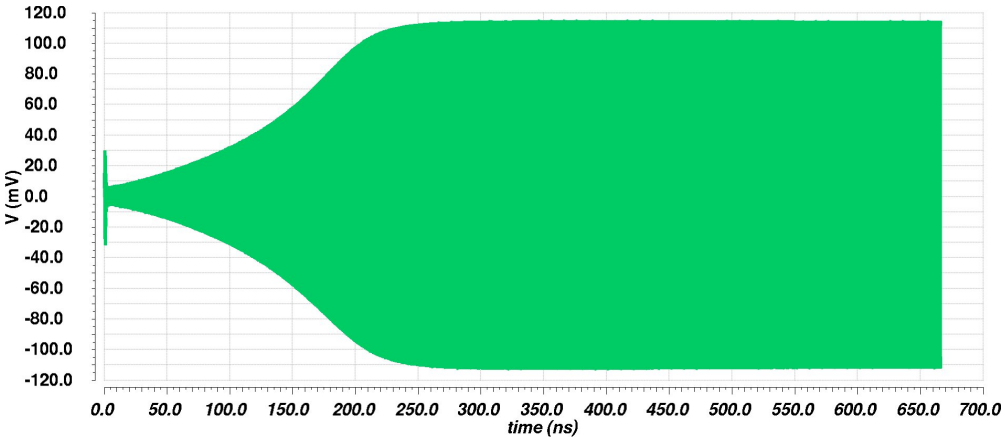

FIGURE 3.1: The Transient Output of the Transmitter with 500 mV Supply

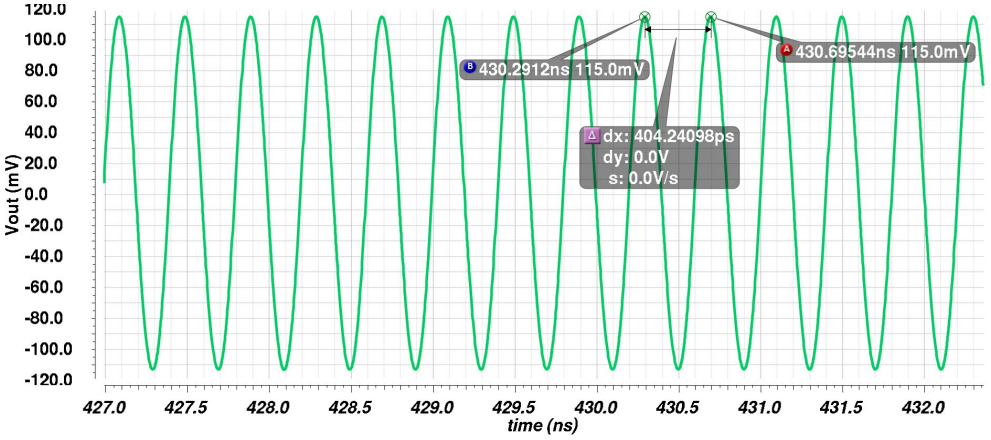

FIGURE 3.2: Zooming The Transient Output of the Transmitter

Oscillation Startup

The startup behavior and the generation of the oscillation can be shown by zooming more into the time axis. Figure 3.3 Shows the startup of the oscillation signal at the output with a considerable delay due to all other transmitter components. Figure 3.4 shows the initial startup periods of the carrier. And Figure 3.5 shows an oscillation that failed to strat up due to the lack of gain, which can be prevented by increasing gm by increasing the current consumption of the crystal oscillator.

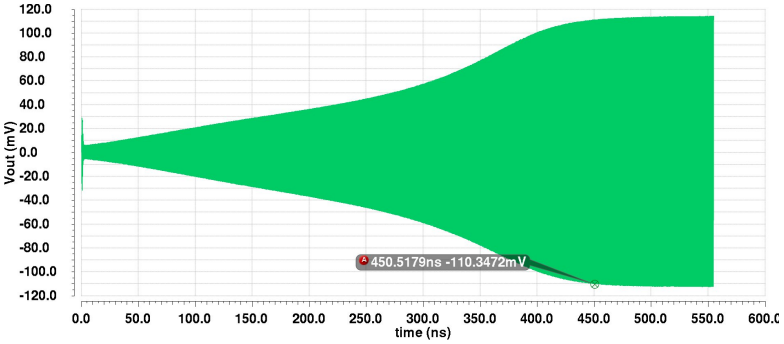

FIGURE 3.3: Oscillation Startup at the Output of the Transmitter

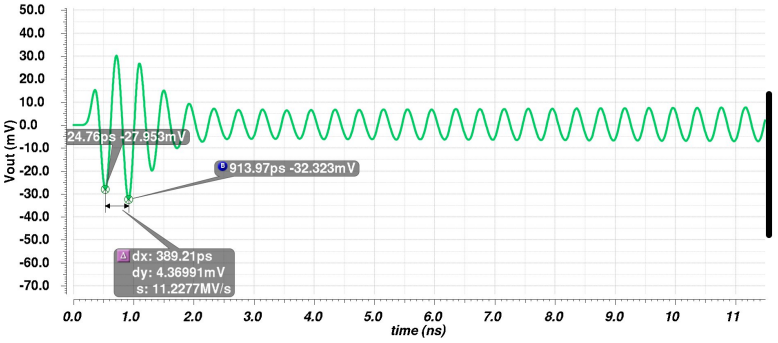

FIGURE 3.4: Zooming The Startup Transient Output of the Transmitter

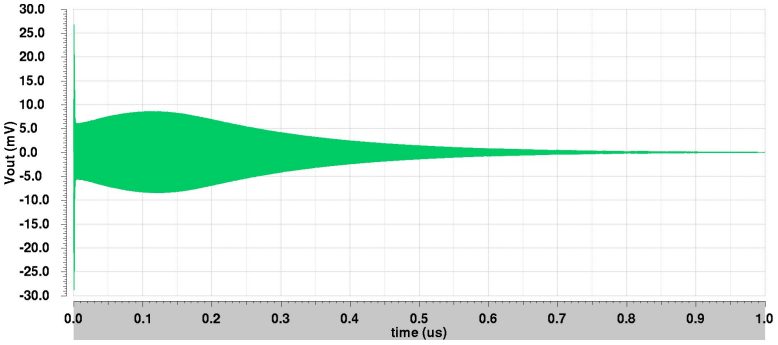

FIGURE 3.5: A Signal that Failed to Startup

Modulation Schemes

The baseband modulating signal is used with the maximum supported data rate to test the different modulators as shown in Figure 3.6.

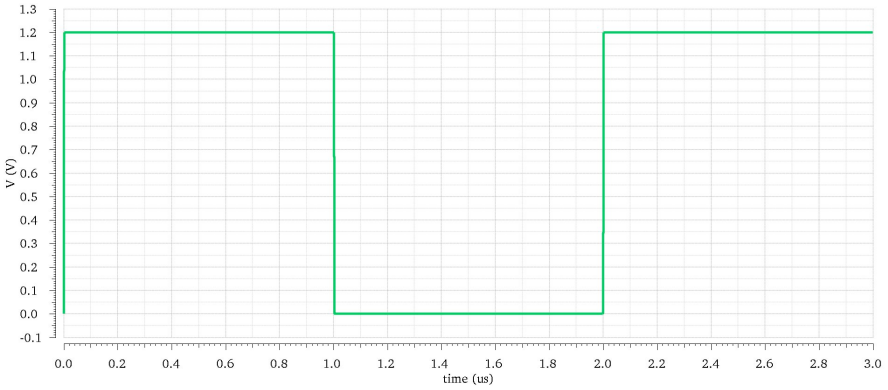

FIGURE 3.6: The Baseband Modulating Signal

OOK Modulation

Figure 3.7 shows the OOK modulated signal at the output of the transmitter. It can be considered as the multiplication of the baseband signal and the carrier scaled to the output signal levels. As shown, the off-state signal amplitude is very small relative to the on-state signal which means less error in the modulation accuracy. Figure 3.8 shows the smooth continuous transition of the amplitude from the ZERO message to the ONE message.

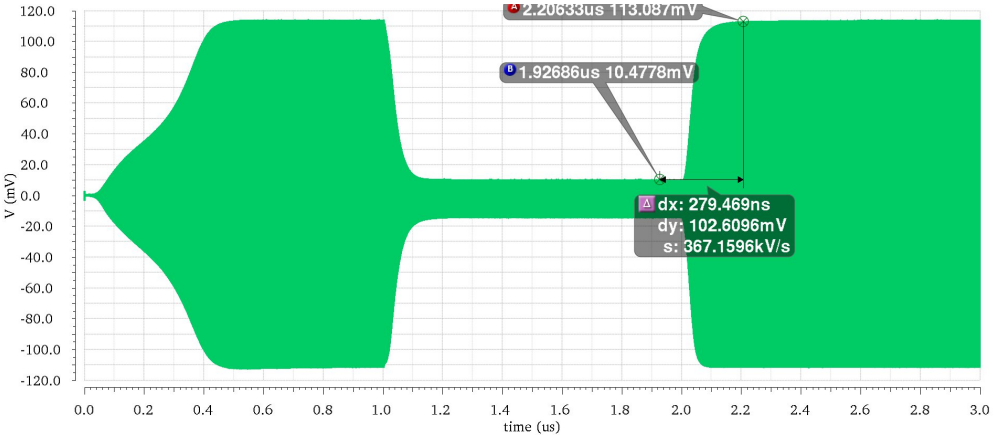

FIGURE 3.7: The OOK Modulated Signal at 1 Mb/s Data Rate

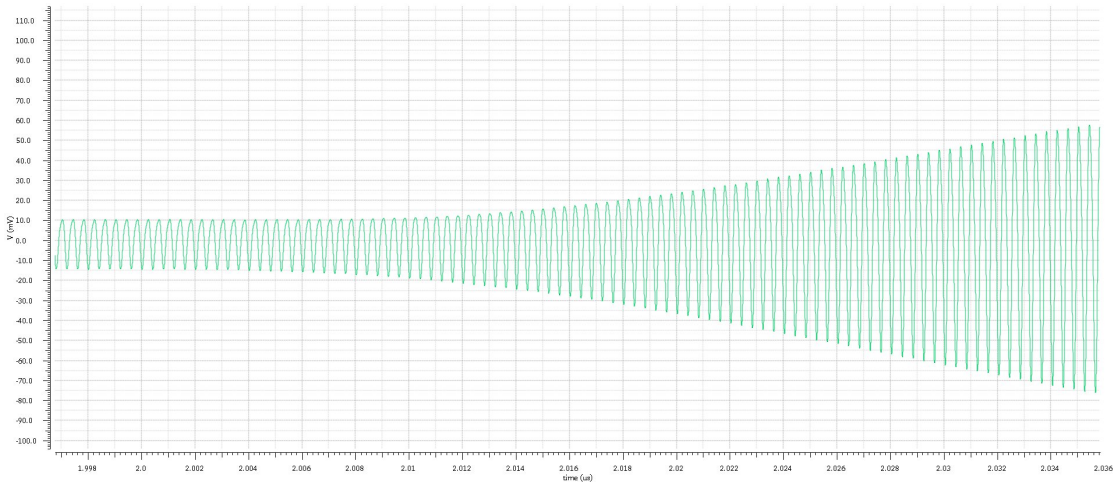

FIGURE 3.8: Zooming The Time Axis of the OOK Modulated Signal

BPSK Modulation

The BPSK modulated signal at the output of the transmitter is shown in Figure 3.9, where there is a fine transition at each period which means that the crystal oscillator does not need to startup again. Figure 3.10 shows the zooming around the transition which indicates the continuity of the oscillation. Figure 3.11 shows the more details transition from the ONE to ZERO messages.

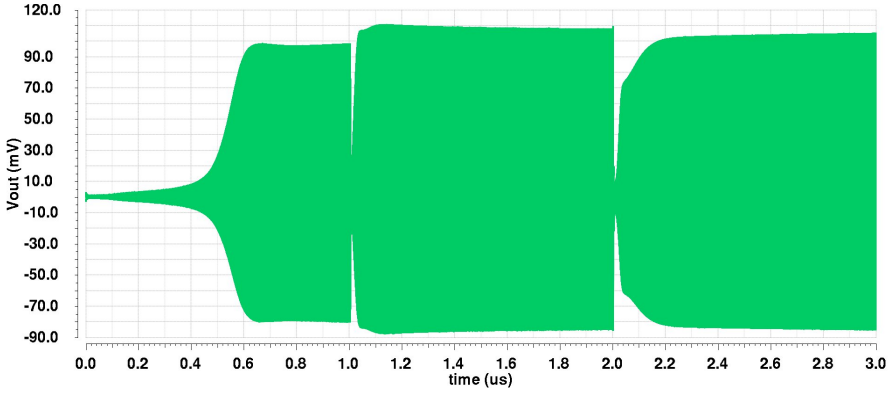

FIGURE 3.9: The BPSK Modulated Signal at 1 Mb/s Data Rate

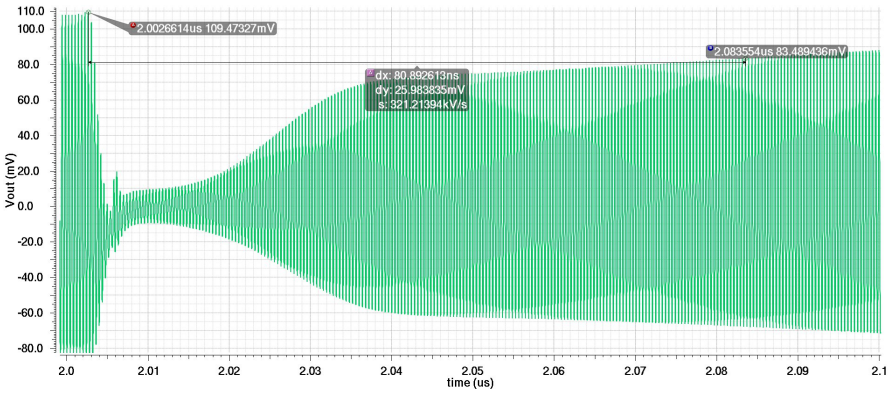

FIGURE 3.10: The BPSK Modulated Signal at 1 Mb/s Data Rate

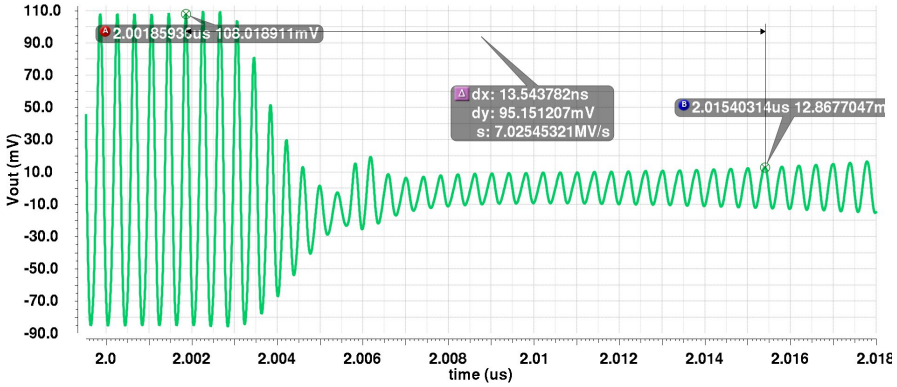

FIGURE 3.11: The BPSK Modulated Signal at 1 Mb/s Data Rate

MSK Modulation

Figure 3.12 shows the MSK modulated signal at the output of the transmitter. Figure 3.13 demonstrates that the transition between the two message is done with a continuous phase in the transmitted signal. Figure 3.14 shows the spectrum of the MSK modulated signals which show two different frequencies as the two messages modulating the carrier frequency. There is a slight difference in the amplitude of the two signals which is an error.

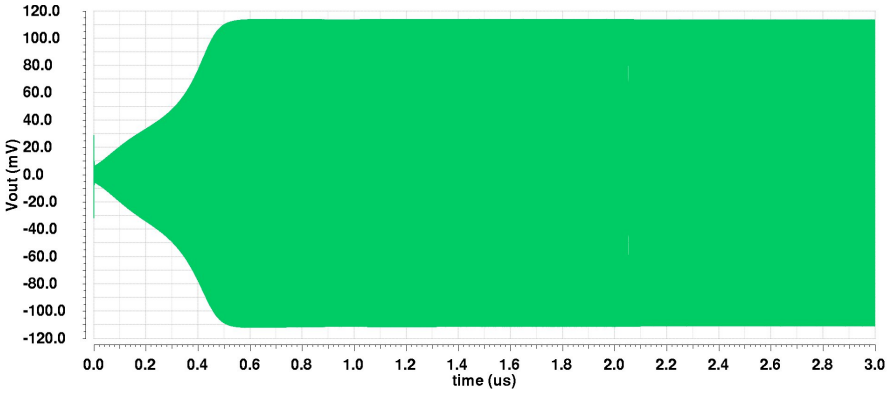

FIGURE 3.12: The MSK Modulated Signal at 1 Mb/s Data Rate

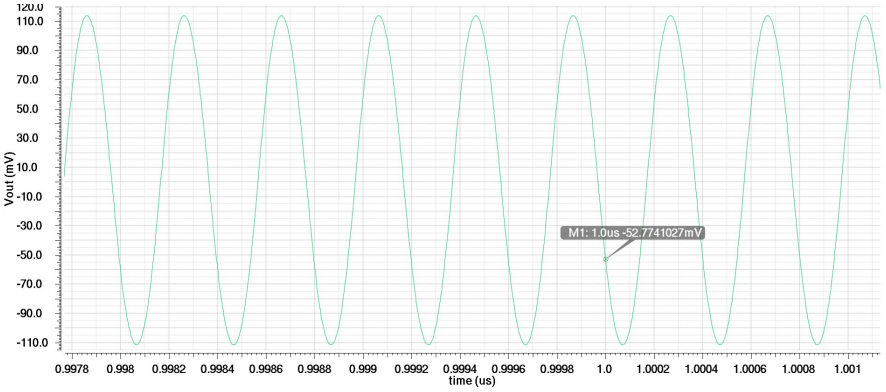

FIGURE 3.13: Zooming The MSK Modulated Signal

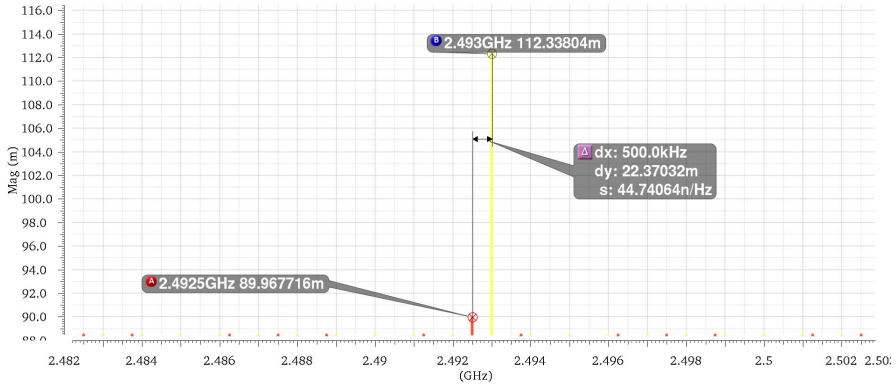

FIGURE 3.14: The MSK Modulated Signal Spectrum

3.2 Transmitter Layout

The optimization of each block layout yields optimally minimizing the area of the required transmitter. The layout affects the actual performance of the transmitter, therefore, accurate layout techniques should be used to help maintain performance near the required one. Figure 3.15 shows the layout of the four-bit resistive ladder DAC. The resistors are matched by placing them close to each other and adding a dummy resistance to decrease etch effects on the edges.

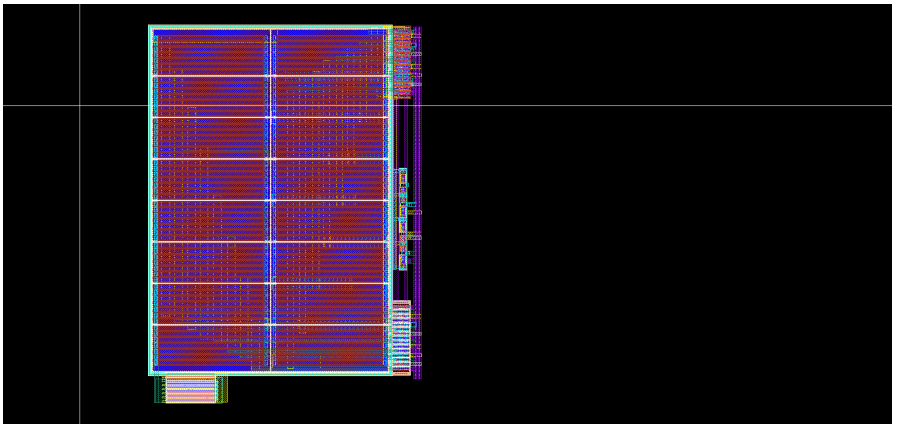

FIGURE 3.15: A 4-bit DAC Resistive Ladder Layout

In the next Figure 3.16 the opamp layout is shown. A layout that is not carefully implemented, may make the opamp unstable since it would add parasitic capacitor or parasitic resistance which may decrease the phase and gain margin at the end. The important parts are the current source and the amplifier, thus, techniques such as common centroid and interdigized layout were utilized to achieve the best results. Also, for the differential pair, matching between the two transistors is crucial since it introduces an offset error in the output signal which controls the PA or pre-driver.

RF Layout:

In RF blocks, the routing parasitics are more problematic than in baseband blocks especially for the blocks that contain the inductors.

Figure 3.17 shows the layout of the FBAR crystal oscillator which has three cores of inverter amplifier gates, two-DACs to bias the bulk, a baseband capacitance to filter the DAC output and an RF capacitance in a capacitor bank. The parasitic resistance in this block affects the quality factor of the resonator, therefore the overall power consumption. In Figure 3.18, BPSK modulator layout is shown. Figure 3.19 shows the PA pre-driver.

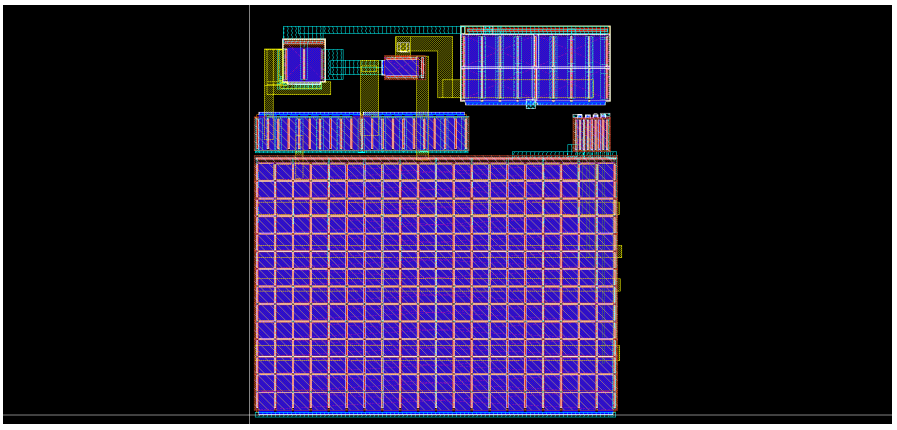

FIGURE 3.16: Low-Power Small-Area Opamp Layout

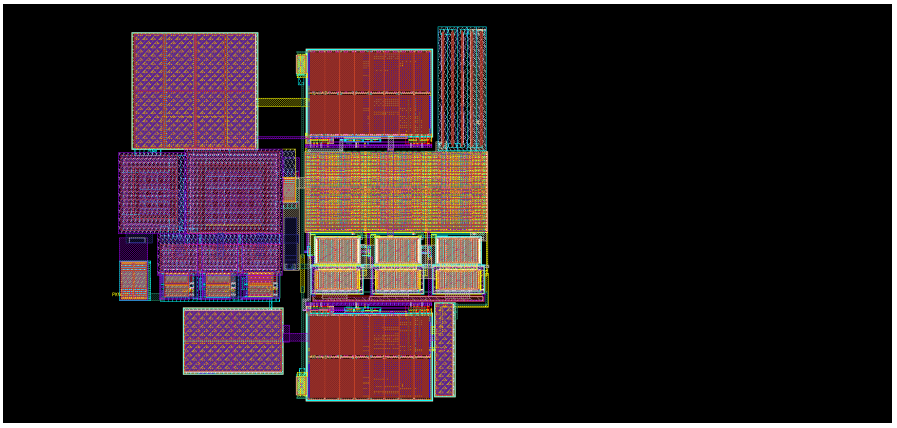

FIGURE 3.17: Layout of the FBAR Crystal Oscillator

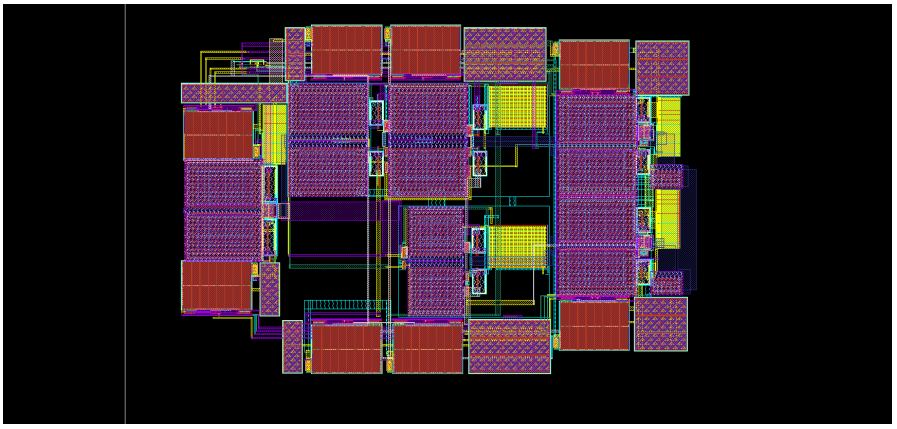

FIGURE 3.18: RF BPSK Modulator and Driver

Figure 3.20 shows the Power amplifier including matching network and transmit switch. Figure 3.21 shows all of the transmitter circuits except for the crystal oscillator.

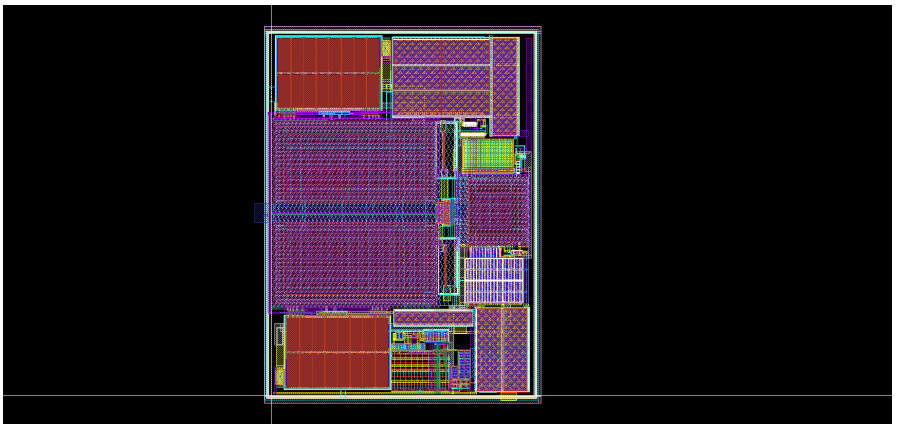

FIGURE 3.19: The PA Pre-Driver Layout

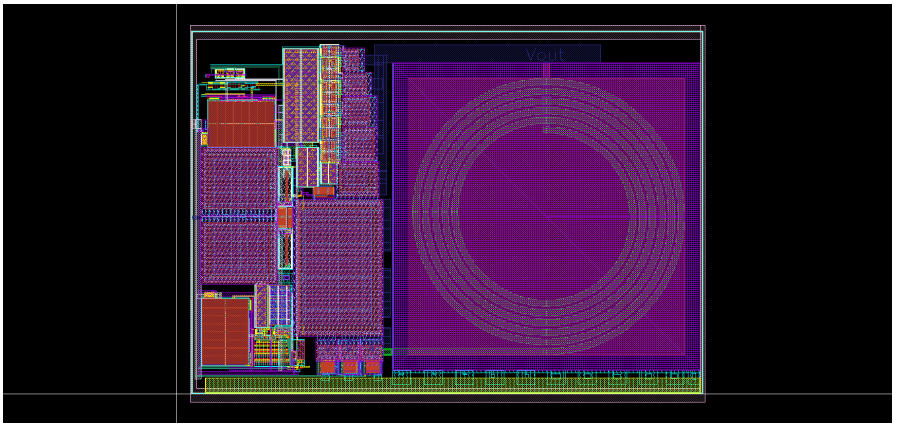

FIGURE 3.20: PA and Transmit Switch Layout

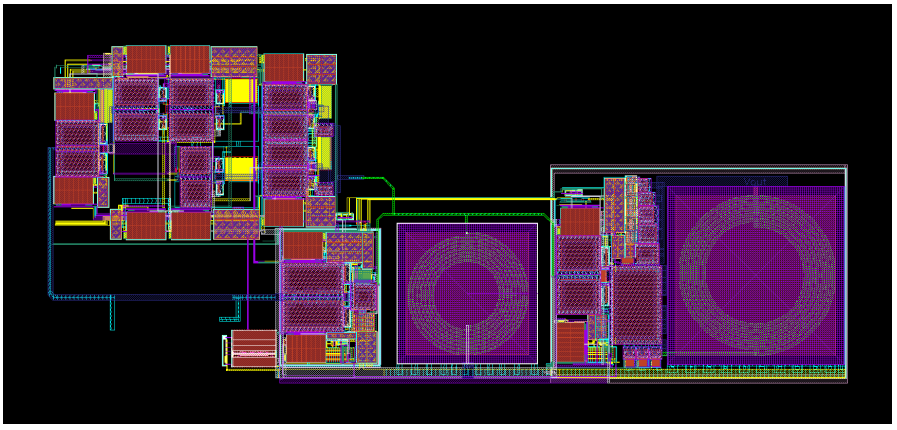

FIGURE 3.21: The Layout of PA and Pre-drivers, BPSK and OOK Modulators

3.3 Results Summary

This section provides the summary of the final results of the design.

TABLE 3.1: Transmitter Achieved Specifications

Specification	Achievements	Achievements after PEX
Supply	0.5-0.7 V	0.5-0.7 V
Digital Supply	0.7 V	0.7 V
Modulation	OOK,BPSK, MSK	OOK,BPSK, MSK
Data Rate	1MHz	1MHz
External components	Only FBAR	Only FBAR
Nominal Pout	-9.5 dBm	-10 dBm
PA Efficiency	47.62 %	42 %
GE	39.7 %	33 %
Total Eff.	22 %	17 %

3.4 Results Comparison

This section compares the achieved simulation results with the other ultra-low power transmitters reported in literature.

TABLE 3.2: Comparison of the Designed Transmitter with other ULP Transmitters

References	[38]	[5]	[6]	This Work
CMOS Tech.[nm]	40	40	65	65
Frequency [GHz]	2.4	315	2.4	2.4
Nominal Supplies [V]	0.4	0. 56-0.2	0.7-1 D	0.5-0.7 D
Area [mm^2]	0.0056[!]	0.3	0.3	0.16
Pout [dBm]	-10	-20	-10	-10
Drain Efficiency %	50	42	44	42
Gloabl Efficiency %	32	28	21	33
External Components	ITN*	ITN*	FBAR	FBAR

Note: * Impedance Transformation Network (ITN) [!] estimated from the paper

Chapter 4

Conclusions

This chapter gives a summary of the whole thesis and suggests a future research direction that can benefit from this thesis and extend its inclusion.

4.1 Thesis Summary

To summarize, this thesis presents the design of an ultra-low power radio frequency ISM band transmitter. The Transmitter is a part of a chip consisting of a transceiver and power management units dedicated to ultra-low power short range communication. First, low power wireless standards that can be used for medical applications, were compared and the required specifications for Body Area Network at 2.4 GHz radios were extracted. These standards require ultra-low output power and very high efficiency for a longer battery life time that is necessary for most applications. BAN radios need an output power of -10 dBm, low startup time, simple modulation schemes such as OOK, BPSK and MSK and a datarate of 1 Mbps. Using an ultra low supply voltage of 0.5-V helps to achieve a small output power, but the transmitter operates in subthreshold operation region which is not well modeled for the designer. The implemented transmitter system was chosen to be a direct modulation transmitter that uses an RF resonator directly, thus, a PLL is not needed which decreases the dissipated power and the area occupied. The thesis benefits from a 2.4 GHz MEMS-based FBAR crystal in order to generate its carrier signal. Different designs and implementations of each component were discussed and compared throughout the thesis and the chosen implementation achieves the lower

power consumption-area product. The crystal oscillator uses a bank of capacitor to tune the resonance frequency, which implements the MSK modulation. The startup time and the power consumption of the oscillator are controlled by enabling three different oscillator stages and generating a DC voltage to bias the bulk of the transistors. Predriver stages were designed in order to buffer and drive the PA gate capacitance and implement the OOK and the BPSK modulators. The buffer was chosen to be an inverter-based resonance buffer to reduce the power consumption, and it was optimized by biasing the gate of the NMOS and the PMOS transistors separately. The BPSK modulator was implemented by choosing a path from two paths, one having an inverter and the other a buffer. The OOK modulator is implemented by enabling or disabling the signal to pass. ULP power amplifier was designed and optimized for high efficiency. The layout effects were taken into account in the simulations. Finally, the summary of the achieved results and the contribution of this thesis was provided. The implemented transmitter works from a 0.5-0.7 V supply voltage and achieves a 33 % global efficiency including all parasitic effects. Finally, the thesis results were compared with similar research literature in order to emphasize the contribution of this work.

4.2 Future Work

Measurements: The chip will be measured and the results will be compared with the simulation, to prove the validity of the assumptions. After that, the chip will be used for a bigger module and a bigger system to enable a lot of other applications that we have in our labs. Also, hoping that the results match the simulation, we would submit a publication about the project.

Self calibrating circuits: Add the circuity that will automatically change the DAC setting and the tunable impedance transformation network to change the output power.

Multiple-standard chip: Designing a transmitter that is able to support multiple standards.

Multiple-channel frequency generation: Designing a transmitter that is able to support multiple channel operation at the ISM band.

Appendix A

Bond Wire Parasitic Modeling

For RF Simulations, any inductance, capacitance or resistance (especially on the signal path) can critically affect the performance of the circuit. For example, supply/ground bonding wires can make supply/ground DC voltage bounce, which means that the DC level at all points bounces as well. This effect can be decreased by adding a coupling capacitor between supply and ground. Other effects,such as feedback due to capacitance and inductance, should be examined as well. However, although package and bonding wires are considered as a short circuit, at high frequencies, they would behave in inductive, capacitive and resistive manners. These effects should be modeled and accounted in the design to avoid misleading results and to assure similar conditions as a real product. In fact, any wire at high frequency should be modeled as R, L and C but sometimes we can neglect inductance of wires if they have a small value.

RF Bonding Pad:

The bonding pads are used to connect the package pins to the circuit on die through the bonding wire. Depending on the application, different types are available such as supply, ground, analog and RF bonding pads. The RF bonding pad consists of electrostatic discharge (ESD) protection diodes, metal layers and passivation layer as shown in Figure A.1. They are usually modeled as parasitic capacitive and parasitic resistive effects on the circuit and it is important to simulate the RF circuits with their effects. The ESD protection consists of two back-to-back diodes from the RF supply to ground. The

equivalent model can be simplified mostly by capacitive effect and in our case, it is nearly 220 fF.

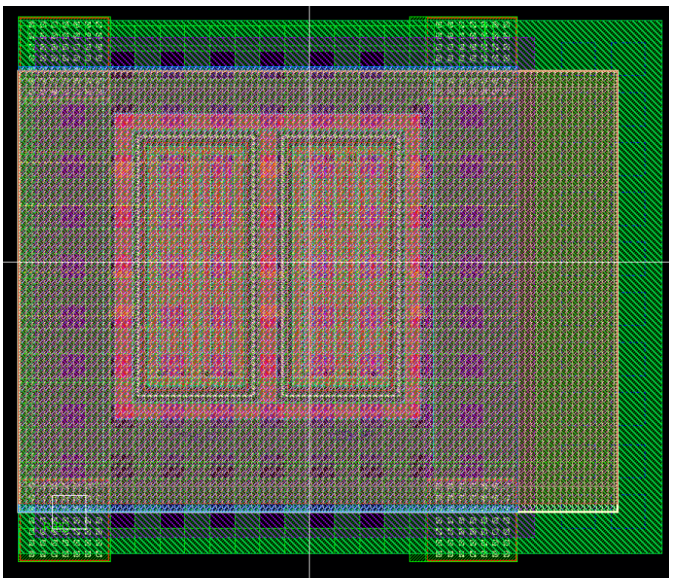

FIGURE A.1: RF Bonding Pad Layout

The QFN Package:

The package Electrical models as provided from the packaging house are as follows.

TABLE A.1: Electrical & Thermal model

PACKAGE	INDUCTANCE(nH)	CAPACITANCE(PF)	RESISTANCE(m-Ω)
8 ×8*	1.47	0.475	63
9×9**	1.221/1.895	0.395/0.496	242.3/315.6
12×12**	1.695/2.386	0.475/0.609	270.1/356.8

Note: * Simulated Results at 100MHz ** Simulated Results at 2.0 GHz

Our package is 8× 8, working at 2.5 GHz. The anticipated average values of the package parasitics are 1.3 nH inductance and 0.5 pf capacitance. The package can be modeled accurately by using the Π model with inductor resistance as shown in Figure A.2.

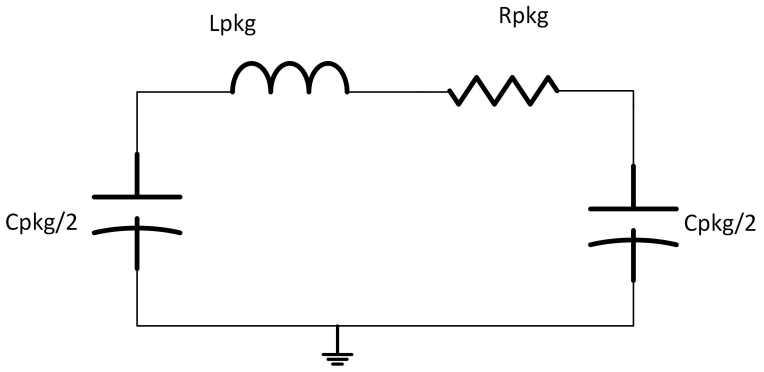

FIGURE A.2: The Package Parasitic Circuit Model

The Die Position:

Depending on the die dimensions, according to the clearance from the package and the parasitic inductance that can be tolerated, the die position with respect to the package can be chosen. Putting the die at the corner can decrease the bond wire effect for very critical RF connections, as shown in the next two Figures (A.3 and A.4). In this work, the package is put at one corner for the sake of RF antenna bond wire.

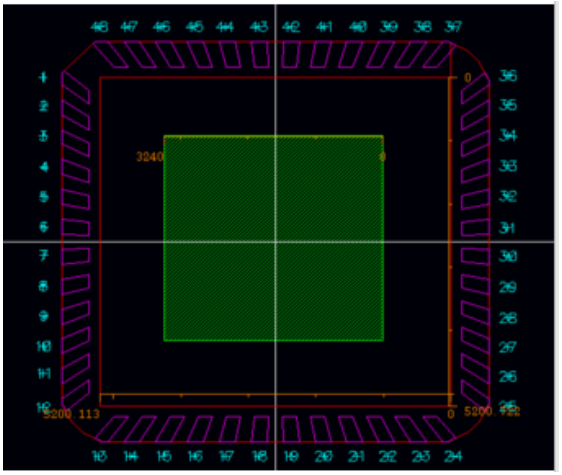

FIGURE A.3: Die at the Center

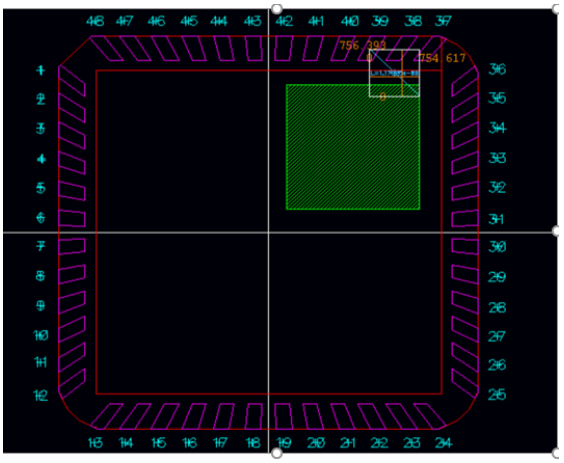

FIGURE A.4: Die at the Corner or the Edge

The Bond Wire:

Several techniques can be used to measure the inductance and the resistance of the bonding wire. Electromagnetic simulations are usually used to estimate the values. In this work, we used Velcoe Wired software from Helic company. This software makes it easy to assign values for the inductance directly from spectre simulation (Cadence). Veloce Wired defines four common types of bond wire according to the dimensions and the shape. The bonding shape cannot be known before the bonding process is finished. The Widely used ones are JEDEC ones. The parameter is given from packaging house so they are using thickness that is equal to 20um for all shapes. The next three Figures (A.5, A.6 and A.7) present these different types.

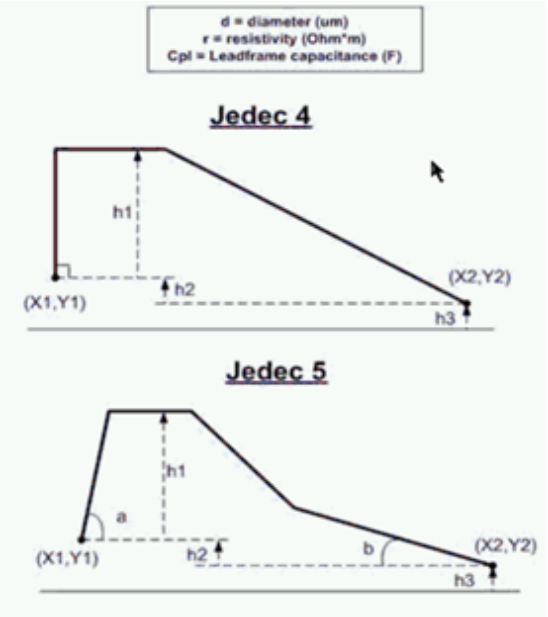

FIGURE A.5: Jedec 4 & 5 Bond wires

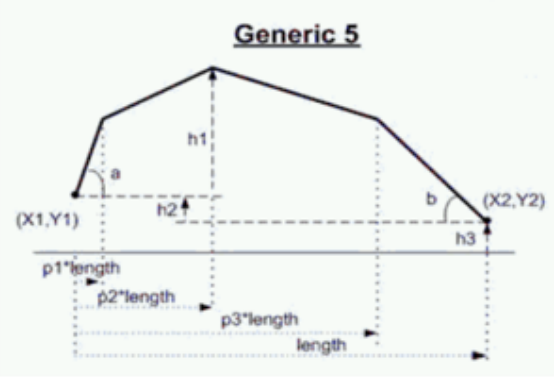

FIGURE A.6: Generic 5 Bond wire

Bond Wire Modeling Results:

It can mainly be modeled by inductance and resistance. Measuring the bond wire inductance for different total length of the wires and using curve fittings give these equations:

TABLE A.2: Electrical Model at 2.5 GHz

Type	INDUCTANCE(nH)	Resistance (m-Ω)
JEDEC 4	$-0.01 * L^3 + 0.15 * L^2 + 0.65 * L + 0.354$	$0.0038 * L^3 + 0.0053 * L^2 - 0.033 * L + 0.036$
JEDCE 5	$-0.02 * L^3 + 0.29 * L^2 + 0.25 * L + 0.62$	$0.0026 * L^3 + 0.034 * L^2 - 0.067 * L + 0.12$
Generic 4	$-0.075 * L^3 + 0.99 * L^2 - 2.4 * L + 3.1$	$0.002 * L^3 + 0.026 * L^2 - 0.042 * L + 0.11$
Generic 5	$-0.0069 * L^3 + 0.13 * L^2 + 0.7 * L + 0.44$	$0.002 * L^3 + 0.026 * L^2 - 0.042 * L + 0.11$

The circuit representation is very simple and shown in Figure A.8

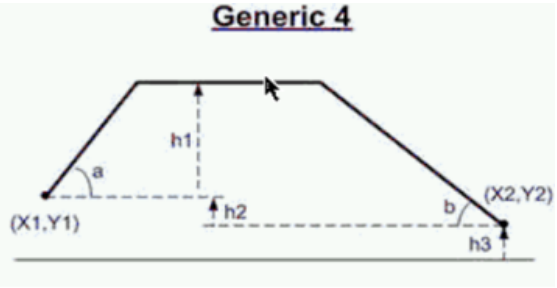

FIGURE A.7: Generic 4 Bond wire

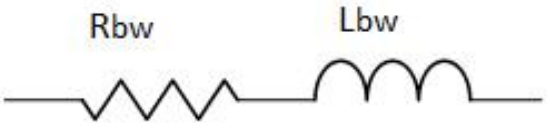

FIGURE A.8: The Circuit Equivalent Model of a Bond wire

Appendix B

Crystal Oscillator With Parasitic Effects

This appendix is very important for designing the FBAR crystal oscillator as it speaks about the parasitic effects and how to avoid the parasitic oscillation of the FBAR. Positioning the FBAR crystal inside or outside the package will change the performance of the crystal oscillator which is critical for FBAR crystals. The different performance will affect the response of the crystal which may not oscillate or oscillate at a parasitic frequency.

B.1 Simulation of FBAR with Parasitic Effects

In this section, the FBAR mBVD model is simulated with the bond wire inductor model, bonding pad model and the package parasitic model. This is done to see the effective impedance and the resonance frequency shift due to the parasitic components and how to avoid parasitic oscillation even before connecting the circuit.

According to the mBVD model of the FBAR, it consists of a motional arm (Series RLC) and a parasitic parallel capacitance which make me expect that the series resonance is the main mode of operation and the parallel is called antiresonance [39]. Figure B.1 shows that the FBAR crystal has a series resonance mode at 2.477 GHz which has minimum resistance and maximum admittance and an antiresonance at 2.511 GHz. The antiresonance has a maximum resistance and a minimum admittance.

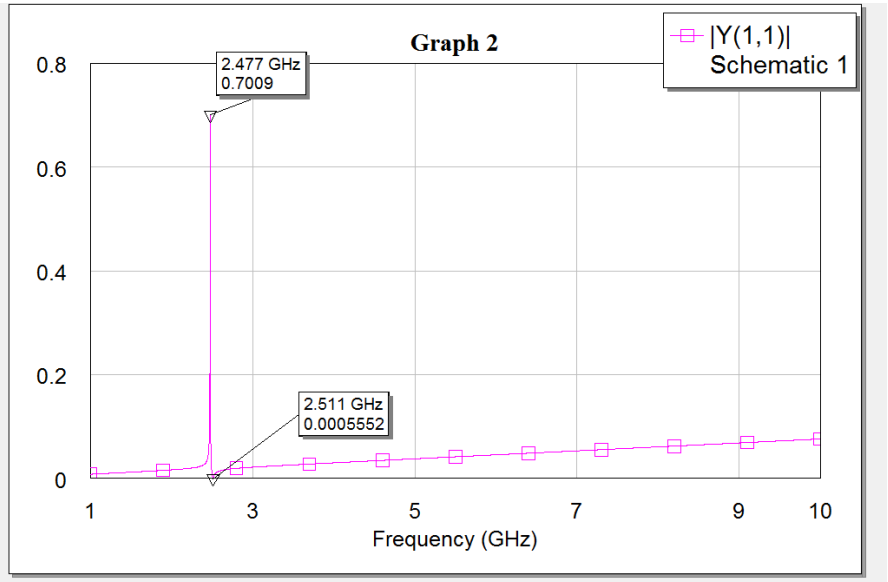

FIGURE B.1: Admittance of the FBAR crystal alone

We added a series inductance and a resistance to the model to see the effect of a bond wire inductance of 1nH and resistance 0.4 Ω. The result is shown in Figure B.2 which implies that the antiresonance is the same frequency, there is a new series resonance frequency and the old one shifts in frequency. Also, the value of the admittance increase which means better quality factor at those resonance modes.

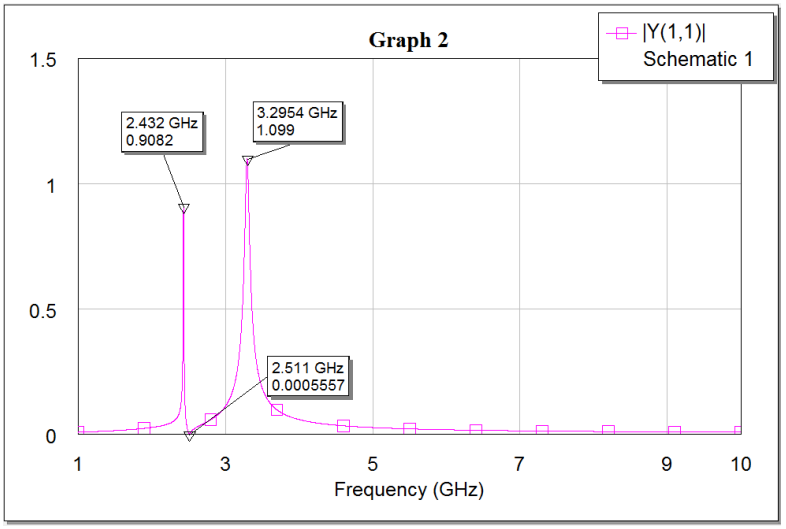

FIGURE B.2: Admittance of the FBAR Crystal With Bonding Wire of 1nH

Adding the series bonding pad, which is effectively a capacitance, will have the effects shown in Figure B.3 which introduces another antiresonance minima. Figure B.4 shows the effects of a series capacitance that is added after the bonding pad and before the

circuit connection.

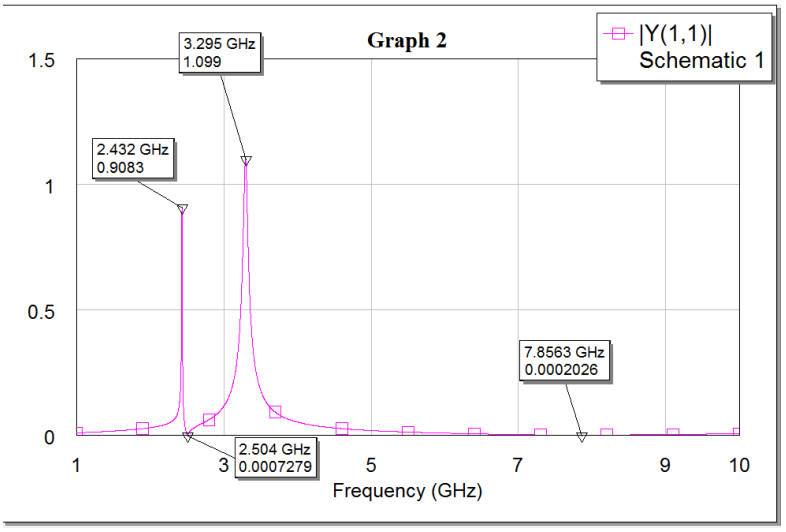

FIGURE B.3: Admittance of the FBAR Crystal With Series Bonding pad

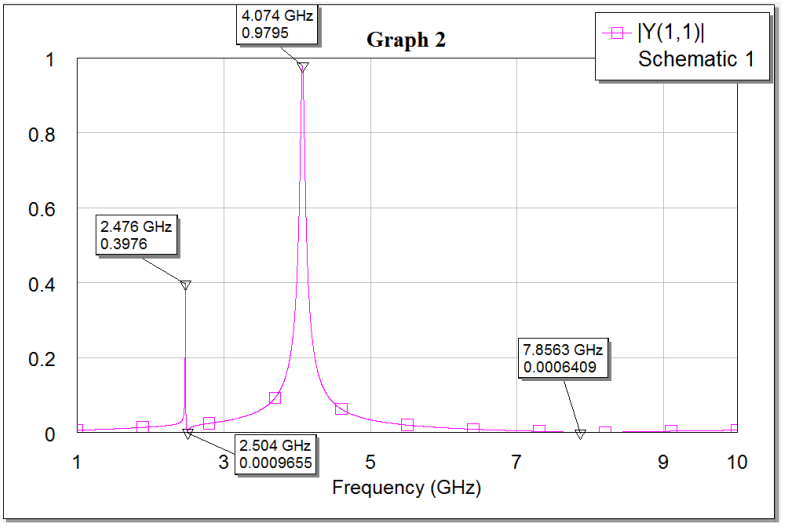

FIGURE B.4: Admittance of the FBAR Crystal With Capa. and Pad

The impedance of the last case is shown in Figure B.5. This Figure shows that the starting series resonance and parallel resonance changes but the new frequency may have a larger gain if the circuit response at that frequency is the same. Since the series resonance at 8 GHz has a lower series equivalent resistance, it has a higher quality factor. Generally the circuit gain decrease with the frequency.

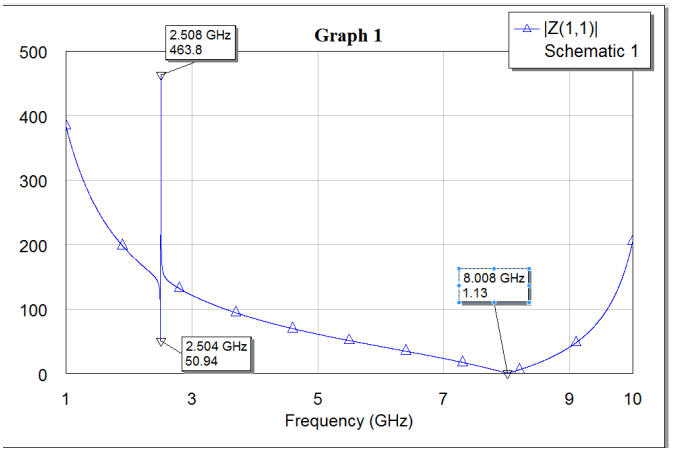

FIGURE B.5: Impedance of the FBAR with all Additions

B.2 Root Locus Analysis

This section talks about designing a very-low supply voltage GHz single ended FBAR XO while putting the crystal on-chip or inside the package. High frequency and multiple resonance oscillators should be designed with root locus, not just by using the negative feedback or the negative resistance model of the oscillators [26].

A matlab code is used to plot root locus and it is provided as a function of gm.

Note: all Values and number here are focused especially on my case 0.5-V supply 2.4 GHz FBAR with the provided values of model

```
clear all; clc;
%for root locus
C1=350*10^-15;C2=350*10^-15;Lbw=0.4*10^-9; gm=1; K1=C1*C2; K2=(C1+C2)/(K1);
%code
syms S
K=gm/(K1);
Gnum=sym2poly((1.235*10^-7)*S^2+(1.524*S)+(3.07397*10^13));
Gden=sym2poly((Lbw*1.235*10^-7)*S^5+(Lbw*1.524+1.7108*10^-7)*S^4+
(1.235*K2*10^-7+102068.259+3.07397*Lbw*10^13)*S^3+(1.524*K2+4.3676*10^13)*S^2+
(3.07397*K2*10^13+2.47217*10^25)*S);

G=tf(Gnum,Gden);
H=1;
figure;
rlocus(G*H*K);
T=feedback(G*K,H);
```

LISTING B.1: Matlab Root Locus XCO Code

First Case (Lbw=0) is achieved if FBAR is fabricated on the same CMOS wafer as the die. The root locus of this case is shown in the Figure B.6. Figure B.7 shows the zoomed in version of Figure B.6. Two values of gm can be seen, gm_{min} which is the lower bound value of gm required for oscillation to start, and gm_{max} which is the upper bound value for gm. For the first case (Lbw=0), gm_{min} = 4.72 ms and gm_{max} = 41.1 ms.

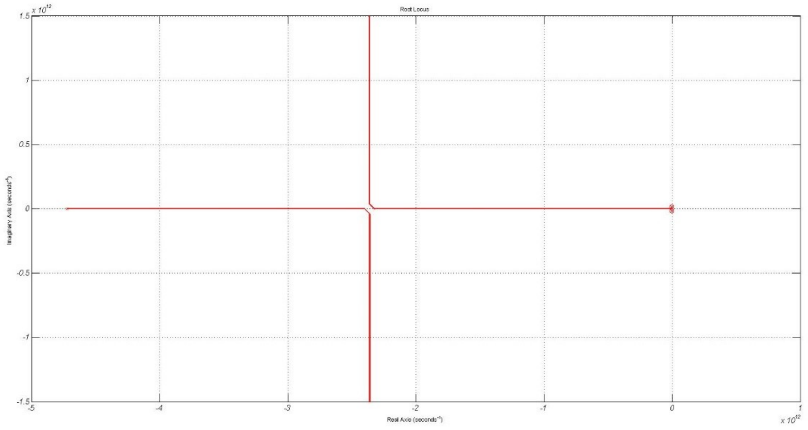

FIGURE B.6: The Root Locus If The FBAR Crystal is directly connected to the Oscillator

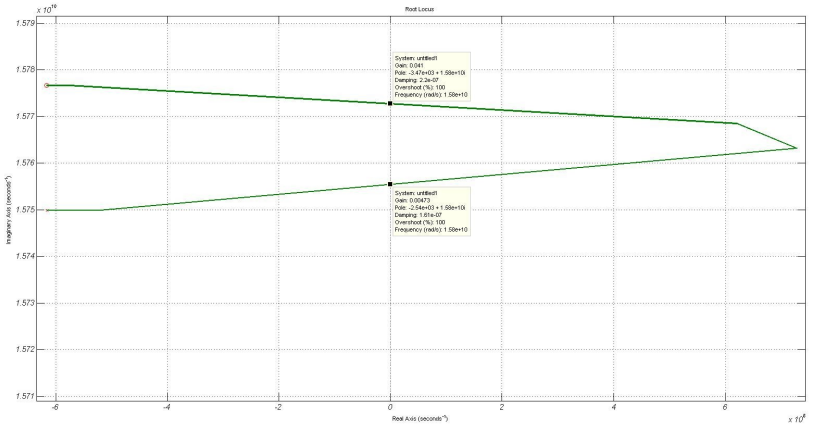

FIGURE B.7: Zooming the previous figure Root locus

Second Case (LBw=0.4 nH) is achieved by putting the FBAR inside the same package with the die, and using a short bond wires to connect both together. Figure B.8 shows the root locus of the second case, two extra lines are present, which means there is a parasitic oscillation mode. Figure B.9 shows the zoomed-in graph for the parasitic oscillation mode.

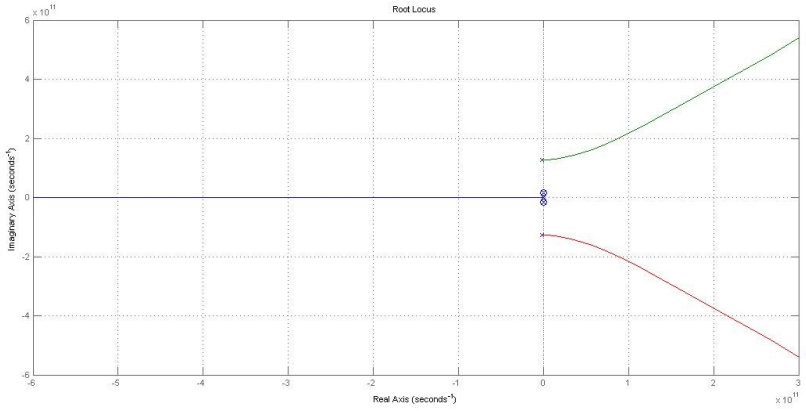

FIGURE B.8: The Root Locus in Case The FBAR Crystal is Inside Same Package as the Die

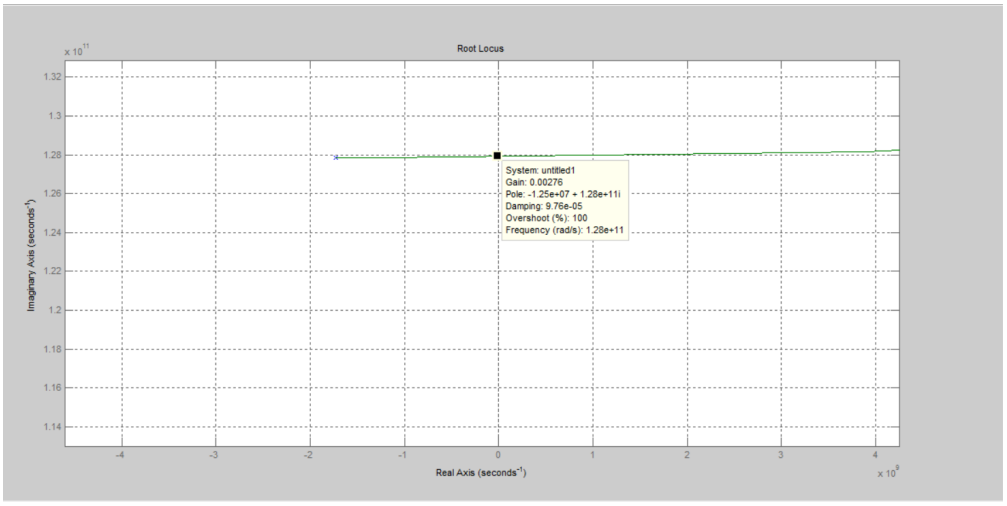

FIGURE B.9: Zooming The Root Locus for Figure B.8

The gm_{min} required for the parasitic oscillation to start at 20.34 GHz is 2.76 ms, however, the desired oscillation mode requires a gm_{min} of 3.71 ms. Therefore, designing with the gm_{min} of the desired mode initiates both resonant modes (desired and parasitic) and it makes them exist at the same time shown in Figure B.10. Finally, at steady state, the parasitic mode is damped and only the desired mode sustain. The time that is needed to reach steady state depends on the ratio of the bond wire quality factor to the FBAR crystal quality factor.

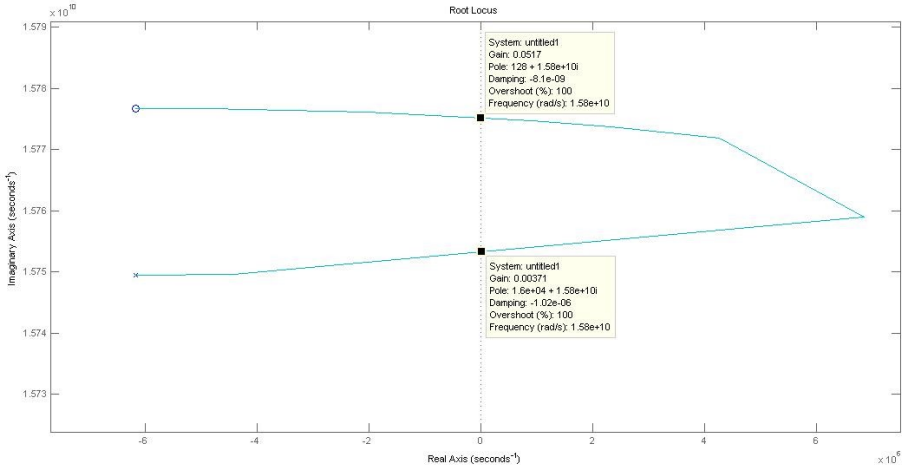

FIGURE B.10: Showing the resonant modes

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