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# Design Optimization of AlInAs–GaInAs HEMTs for High-Frequency Applications

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***Abstract*—By using a Monte Carlo simulator, the static and dynamic characteristics of 50-nm-gate AlInAs–GaInAs $\delta$-doped high-electron mobility transistors (HEMTs) are investigated. The Monte Carlo model includes some important effects that are indispensable when trying to reproduce the real behavior of the devices, such as degeneracy, presence of surface charges, T-shape of the gate, presence of dielectrics, and contact resistances. Among the large quantity of design parameters that enter the fabrication of the devices, we have studied the influence on their performance of two important factors: the doping level of the $\delta$-doped layer, and the width of the devices. We have confirmed that the value of the $\delta$-doping must be increased to avoid the reduction of the drain current due to the depletion of the channel by the surface potential. However, a higher $\delta$-doping has the drawback that the frequency performance of the HEMTs is deteriorated, and its value must be carefully chosen depending on the system requirements in terms of delivered power and frequency of operation. The reduction of the device width has been also checked to improve the cutoff frequencies of the HEMTs, with a lower limit imposed by the degradation provoked by the offset extrinsic capacitances.**

***Index Terms*—AlInAs–GaInAs, cutoff frequency, high-electron mobility transistor (HEMT), high-speed devices, Monte Carlo simulation, parasitic resistances and capacitances, semiconductor device design and fabrication, small signal equivalent circuit.**

## I. Introduction

With the recent development of broadband and satellite communications, one of the main objectives of modern microelectronics is the fabrication of devices with increasing cutoff frequency and low noise figure. Even if heterojunction bipolar devices (HBTs) have reached a good frequency performance, their noise level is much higher than in field effect devices. Thus, the state-of-the-art of high-frequency and low-noise performance is achieved by unipolar devices, mainly high-electron mobility transistors (HEMTs) [1]–[3]. With InP-based HEMTs using the AlInAs–GaInAs material system, it is possible to reach $f_t$ of more than 560 GHz [4] and $f_{\max}$ up to 600 GHz [5], improving those of usual GaAs-based pseudomorphic HEMTs.

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In order to further improve the performance of the devices, their gate length must be reduced down to the technological limit (that nowadays has reached 25 nm [4]). However, shorter gates involve an increase of short-channel effects that limit the microwave performance of the HEMTs. To avoid these problems, the layer structure and device geometry have to be correctly designed. With the use of computer simulation, the design optimization can be made in a short time and with no waste of money. In this paper, we will make use of a semiclassical Monte Carlo (MC) model to obtain the static and dynamic characteristics of 50-nm and 100-nm-gate HEMTs and to check the influence of the downscaling on the device performances. Special importance will be given to the extraction of the extrinsic cutoff frequencies ($f_t$ and $f_{\max}$) of the HEMTs, since these are the key figures of merit for high frequency applications. This is the first time, to our knowledge, that their values have been obtained through an MC simulation

In Section II, the basic features of the MC simulation will be presented, and then in Section III, the results of the simulations will be compared with experimental measurements of dc and dynamic characteristics of a similar HEMT. By using this tool, we will try to optimize the value of two of the most important design parameters: the doping level of the $\delta$-doped layer in Section IV, and the width of the devices in Section V. For this reason, results with different values of these parameters (always inside of the technological possibilities) will be shown, and their influence on the static and dynamic characteristics of the HEMTs will be analyzed.

## II. Monte Carlo Model

Classical modeling of electronic devices meets important difficulties when dealing with ultrashort gate HEMTs. The small size of these devices leads to the appearance of very high electric fields inside them, and consequently hot carrier effects [6], that can only be adequately reproduced by using the MC technique [7]. Moreover, in the case of heterojunction devices, the electron confinement can also give rise to quantum effects such as degeneracy, energy quantization in the channel, and tunneling from the channel to the gate. If a correct description were required it would be necessary to self-consistently solve Poisson and Schrödinger equations, which, for the moment, is an unaffordable task in terms of computation time for a dynamic simulation. In order to overcome these difficulties, we will make use of a semiclassical MC model that locally takes into account the effect of the degeneracy by using the rejection technique [8]. The rest of quantum effects are

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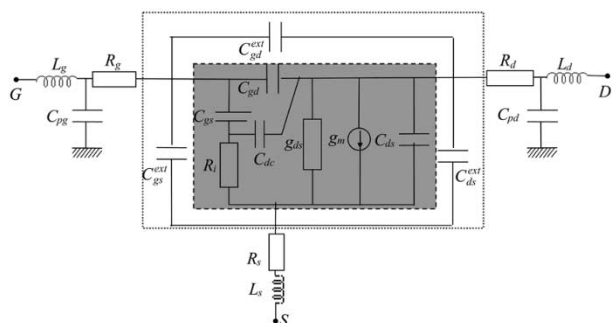


Fig. 1. Equivalent circuit of the HEMTs (the position of the capacitance $C_{\rm dc}$ is shown but it is not considered in the calculations). The shaded area represents the intrinsic elements obtained through the MC simulation, and the outer dotted box encloses the "intrinsic" equivalent circuit from the point of view of the experimental measurements: $L_s = 1$ pH, $L_g = L_d = 25$ pH, $C_{\rm pg} = 1$ fF, $C_{\rm pd} = (220\ {\rm fF/mm}) \times W$, $R_g = (250\ \Omega/{\rm mm}) \times W/3n^2$ ($n$ is the number of gate fingers, which in this work will be always 2), $R_s = (0.25\ \Omega \cdot {\rm mm})/W$, and $R_d = (0.35\ \Omega \cdot {\rm mm})/W$.

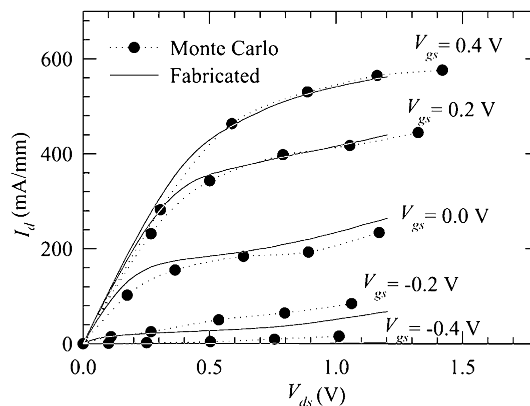


Fig. 2. Output characteristics of the real 70-nm-gate and the simulated 50-nm-gate HEMT with $\delta = 6 \times 10^{12}$ cm$^{-2}$.

not considered in order to keep the calculation time at an acceptable level. More details about the two-dimensional (2-D) MC model can be found elsewhere [9]–[14]. The validity of this approach has been checked in previous works by means of the comparison with experimental results of static characteristics, small-signal behavior and noise performance of an InP lattice-matched 100-nm-gate HEMT [9], [10]. Using this MC simulator as analyzing tool, we will present a microscopic investigation of a lattice matched 50-nm-gate $\delta$-doped $\rm Al_{0.48}In_{0.52}As$–$\rm Ga_{0.47}In_{0.53}As$ HEMTs that will allow predicting some design rules for the fabrication of these devices.

Impact ionization mechanisms are not considered in this version of the simulator since in this work we are restricted to low values of $V_{\rm ds}$ (0.5 V), where kink effect due to the appearance of impact ionization is not present in lattice-matched HEMTs (or is extremely weak). On the other hand, it has been experimentally found [15], and we have confirmed in our simulations [16], that kink effect is a slow process, only affecting the low-frequency behavior (up to some MHz) of the devices.

The intrinsic small-signal equivalent circuit of the HEMTs has been calculated taking as a basis their Y-parameters, obtained by using the classical MC technique [17]. The equivalent circuit must take into account the "extrinsic" (from the point of view of MC simulation) geometric capacitances $C_{\rm gs}^{\rm ext}$, $C_{\rm gd}^{\rm ext}$, and $C_{\rm ds}^{\rm ext}$, which are not included in the MC simulation, but from the point of view of the measurements are within the intrinsic section of the circuit [10]. The complete equivalent circuit is shown in Fig. 1, where the shaded area represents the intrinsic elements that are obtained from the MC simulation, while the dotted box encloses the "intrinsic" equivalent circuit from the point of view of experimental measurements. For the 50-nm HEMT we have taken for $C_{\rm gs}^{\rm ext}$, $C_{\rm gd}^{\rm ext}$, and $C_{\rm ds}^{\rm ext}$ the same values as for the 100-nm one ($C_{\rm gs}^{\rm ext} = 220$ fF/mm, $C_{\rm gd}^{\rm ext} = 70$ fF/mm and $C_{\rm ds}^{\rm ext} \approx 0$) since these geometrical capacitances are practically independent of the gate length. The $S$-parameter measurements were made in the 0.5–50 GHz frequency range and the small-signal equivalent circuit extracted using the cold FET method [18]. It is important to take into account the dependence of the parasitic elements on the device width $W$ (that corresponds to the nonsimulated dimension in the 2-D MC model). While the source, gate and drain inductances, ($L_s$, $L_g$, and $L_d$, respectively) and the gate pad capacitance ($C_{\rm pg}$) are almost independent of $W$, the gate resistance ($R_g$) and drain pad capacitance ($C_{\rm pd}$) are proportional to $W$, and the source and drain resistances ($R_s$ and $R_d$, respectively, representing the nonsimulated part of the contact resistances) to $1/W$.

## III. Comparison With Experimental Results

The previously explained MC model has been used to improve the fabrication process of sub-100-nm-gate InP based pseudomorphic HEMTs [19]. In the optimized layer structure used for the fabrication, the gate-to-channel distance has been fixed at 11.5 nm and the $\delta$ doping at $6 \times 10^{12}$ cm$^{-2}$. The gate-to-channel distance cannot be further reduced in order to prevent for gate-tunneling current. To improve the Schottky contact characteristics and the confinement of electrons in the channel, the aluminum content in the AlInAs layers has been fixed to a value of 0.65. Moreover, in the channel we have used an indium content of 0.65 to improve the carrier transport properties. Even if the projected gate length was 50 nm, the difficulties of the technological process (whose details are given in [19]) result, in the most favorable case, in a slightly longer gate of 70 nm. We will therefore compare the MC model with measurements of the best device that we have been able to fabricate. Even if it is not exactly the same device, the comparison of the simulation with these experimental results can be very useful to identify effects not included in the model, like the influence of the gate leakage current on the high frequency behavior of the HEMTs.

We will first compare the MC current–voltage ($I$–$V$) characteristics with those measured in the real device with $W = 100$ $\mu$m. As observed in Fig. 2, even if the real and the simulated HEMTs are not exactly the same, the results of the simulation for the $I$–$V$ curves are quite similar to the experimental measurements. Even if this similarity could be considered to be surprising, it can be explained in terms of the opposite influence of the two main differences between the real and simulated devices, namely, the gate length and the In content of the channel. The longer gate of the fabricated 70-nm

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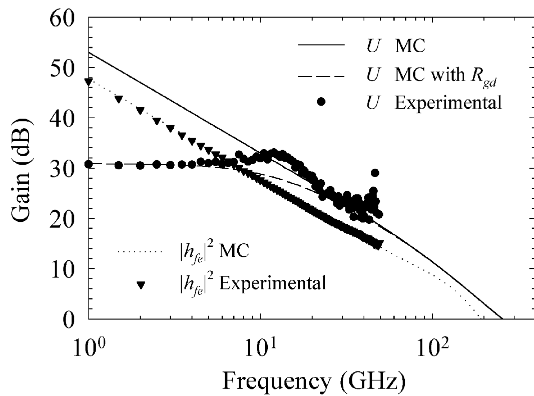


Fig. 3. Values of $U$ and $|h_{fe}|^2$ measured in the real 70-nm-gate HEMT and simulated in the 50-nm-gate HEMT with $\delta = 6 \times 10^{12}$ cm$^{-2}$ for the bias point where the maximum $f_t$ is obtained ($V_{\rm gs} = 0.1$ V). Also the value of $U$ calculated including gate shunt resistance ($R_{\rm gd} = 60$ K$\Omega$) is plotted.

$\mathrm{Al_{0.65}In_{0.35}As/Ga_{0.35}In_{0.65}As}$ pseudomorphic HEMT deteriorates the device performance (with respect to the simulated 50-nm lattice matched HEMT), which is compensated by the better electron confinement and the improved carrier mobility in the channel.

In Fig. 3, the experimental values of $U$ and $|h_{fe}|^2$ are compared with those obtained from the MC simulation. The discrepancy in the values of $U$ at low frequency ($<$10 GHz) comes from the absence of gate leakage current within the MC model. This effect can be modeled by including in the equivalent circuit of the HEMTs (Fig. 1) a gate-drain resistance $R_{\rm gd}$ in parallel with $C_{\rm gd}$. In Fig. 3, the values of $U(f)$ calculated using $R_{\rm gd} = 60$ K$\Omega$ (in good agreement with the measured values) are also plotted, showing clearly that the presence of this shunt resistance introduces a new pole in $U(f)$ at low frequency, while $|h_{fe}|^2$ remains unchanged. In this way, the overall agreement between the MC simulations and the experimental results is remarkably good.

This result shows clearly that the effect of the gate leakage current (coming from tunneling or from impact ionization-generated holes) appears at "low frequency" (in this case 10 GHz) and do not influence the calculation of both $f_t$ and $f_{\rm max}$. However, the frequency up to which the devices show a degraded performance increases with the gate current and, therefore, its value must be kept to the minimum.

## IV. Influence of the $\delta$-Doping

### A. Static Characteristics

In [9] and [10], it was shown that our MC model gives a correct estimation of the static characteristics, small-signal behavior and noise performance in the case of the 100-nm-gate-HEMT whose geometry is shown in Fig. 4(a). To avoid considerable short-channel effects, it is convenient to keep constant the aspect ratio (gate length over gate-to-channel distance) when the gate length is reduced. Therefore, the layer structure must be changed with respect to that of the 100-nm-gate HEMT: the gate-to-channel distance must be reduced. However, some constraints must be taken into account. First, the reduction of the gate-to-channel distance can lead to the appearance of a noticeable gate leakage current due to the tunneling of electrons to

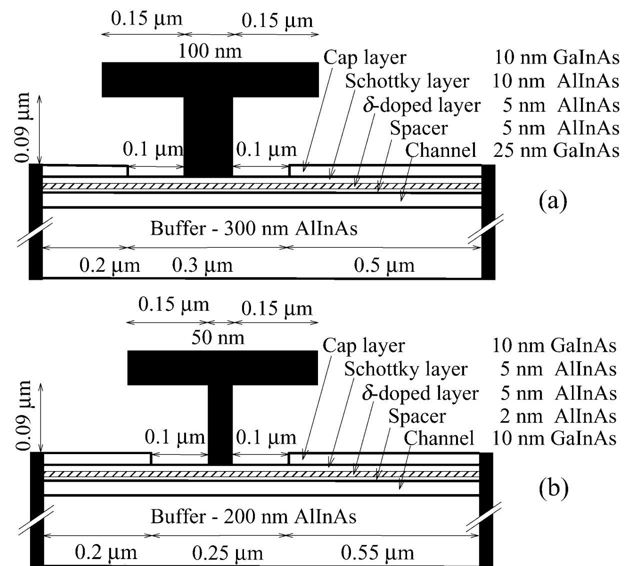


Fig. 4. Geometries of the simulated (a) 100-nm-gate and (b) 50-nm-gate HEMTs.

the channel, thus degrading the device performance. To minimize this effect, the lower limit for this distance is approximately 100 Å. Tunneling is not considered in the simulation and it can only be detected by means of the experimental measurement of the gate leakage current. Moreover, in the scaling down process, the value of the charge of the $\delta$-doping plane is a key parameter, since it must be sufficiently low to avoid conduction through this layer, but high enough to fill up the channel. The $\delta$-doped layer must also be able to screen the influence of the surface charge placed on the recess, thus avoiding the depletion of the channel effect that depends also on the gate-to-channel distance. The result of the addition of these effects will be analyzed through the MC simulation of the characteristics of the transistor when using different values for the $\delta$-doping. Taking into account all these constraints, we have performed simulations of the 50-nm-gate $\mathrm{Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As}$ (lattice-matched on InP) HEMTs whose geometry is shown in Fig. 4(b) with four different values for the $\delta$-doping: 5, 6, 7, and $8 \times 10^{12}$ cm$^{-2}$. The lowest $\delta$-doping ($5 \times 10^{12}$ cm$^{-2}$) is the same as that used in the fabrication of the 100-nm-gate HEMT previously studied [9], [10]. Even if the gate-to-channel distance has been reduced from 20 to 12 nm, the attempt to avoid tunneling current makes the aspect ratio decrease from 5.0 to 4.2. Consequently, short-channel effects are expected to be more important in the 50-nm than in the 100-nm-gate HEMT.

The intrinsic output characteristics ($I_d$–$V_{ds}$) for the 100-nm and 50-nm HEMTs are shown in Fig. 5. Comparing Fig. 5(a) and (e) we can observe that, with the same $\delta$-doping of $5 \times 10^{12}$ cm$^{-2}$ the current decreases when the gate length is reduced from 100 to 50 nm, although an increase was expected (due to an enhanced velocity overshoot of the electrons in the channel). The cause for this degradation of the transport properties is the depletion of the channel provoked by the surface charges lying in the bottom of the recess, whose effect on the potential distribution reaches the channel due to the reduction of the gate-to-channel distance in the 50-nm-gate HEMT. To solve this problem the value of the $\delta$-doping must

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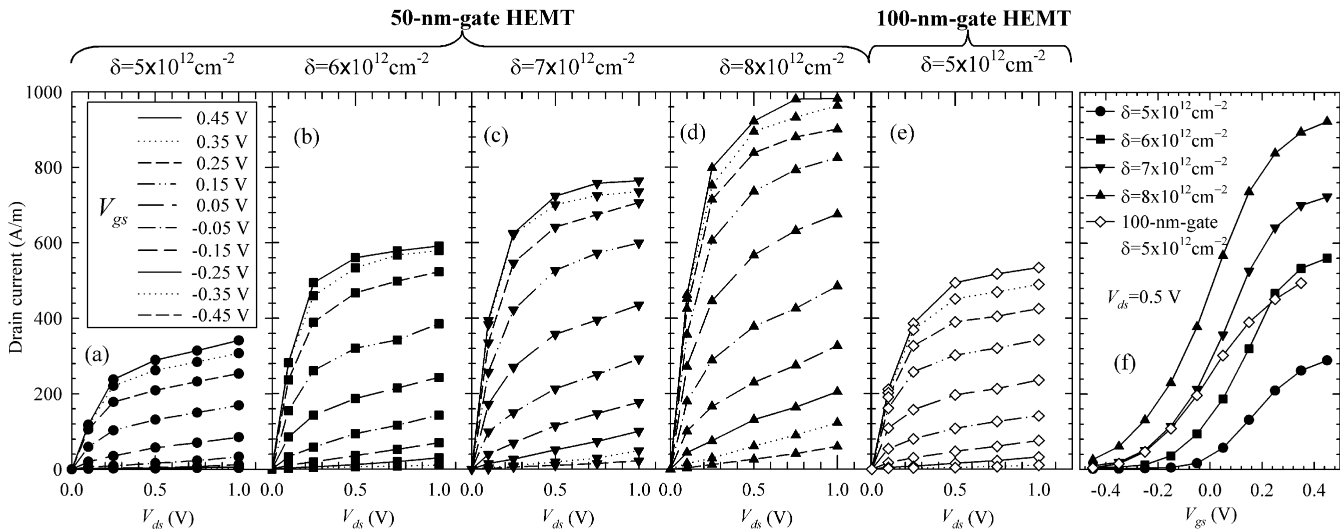


Fig. 5. (a)–(d) $I_d$–$V_{\rm ds}$ characteristics for the 50-nm-gate HEMTs with different values of the $\delta$-doping: 5, 6, 7, and 8 $\times$ $10^{12}$ cm$^{-2}$. (e) The 100-nm-gate HEMT (with $\delta = 5 \times 10^{12}$ cm$^{-2}$ [9] [10]. (f) Transfer characteristics ($I_d$–$V$gs at $V_{\rm ds} = 0.5$ V) for the 100-nm and 50-nm-gate HEMTs. In (a)–(d), the uppermost curves correspond to $V_{\rm gs} = 0.45$ V, and the increment is $\Delta V_{\rm gs} = 0.1$ V. The gate built-in potential is taken to be 0.75 V.

be raised, thus increasing the current provided by the device [Fig. 5(b)–(d)]. For a better comparison of the current level provided by the devices, their intrinsic transfer characteristics ($I_d - V_{\rm gs}$ for $V_{\rm ds} = 0.5$ V) are plotted in Fig. 5(f), showing also how the transconductance [the slope of the curves, also shown in Fig. 6(a)] of the 50-nm HEMTs is largely improved when the $\delta$-doping is increased. However, the increase of the $\delta$-doping has also its negative counterpart. First, as can be observed in Fig. 5(f), it is more difficult to achieve the channel pinchoff (the threshold voltage is more negative). Also, high values of the $\delta$-doping can lead to conduction through the $\delta$-doped layer (parasitic channel), thus increasing the drain conductance $g_d$ [Fig. 6(b)], and degrading the extrinsic performance of the device. The intrinsic voltage gain $g_m/g_d$ [Fig. 6(c)] can be used as an indicator of this effect, since, as it will be shown later, it strongly affects the value of $f_{\max}$ ($g_m/g_d$ must be maximized to obtain the best frequency performance). For the devices with $\delta = 5 \times 10^{12}{\rm cm}^{-2}$, $g_m/g_d$ is improved for the 50-nm HEMT with respect to the 100-nm one.

The dependence with the $\delta$-doping of the previously shown magnitudes can be explained with the help of Fig. 7, where the sheet carrier density in the channel of the 50-nm-gate HEMT is plotted versus the longitudinal position $x$. It can be noticed that for the lowest $\delta$-doping ($5 \times 10^{12}{\rm cm}^{-2}$) the surface charge placed at the bottom of the recess is partially depleting the channel. When the $\delta$-doping is raised to 6 $\times 10^{12}{\rm cm}^{-2}$, in addition to the increase of electrons in the whole channel, the effect of the surface charge on the channel is almost completely screened. If the $\delta$-doping is further increased the only consequence is the enhancement of the number of electrons in the channel. This explains the considerable increase of current and $g_m$ when passing from 5 to $6 \times 10^{12}$ cm$^{-2}$ as compared with the slight improvement obtained when the $\delta$-doping surpasses this value.

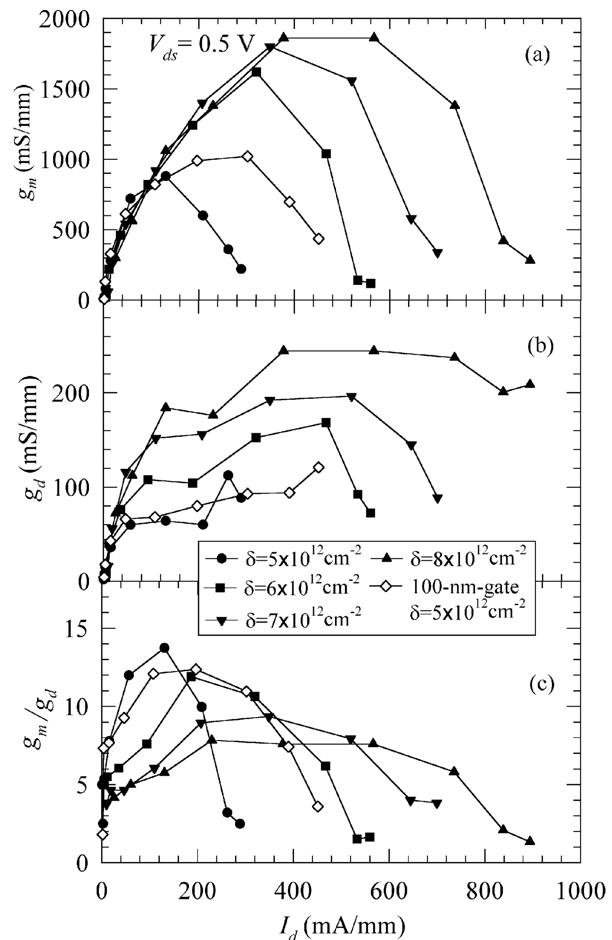


Fig. 6. (a) Transconductance $g_m$, (b) drain conductance $g_d$, and (c) intrinsic voltage gain $g_m/g_d$ as a function of the drain current for the 100-nm-gate HEMT and the 50-nm-gate HEMTs with different values of the $\delta$-doping. The intrinsic drain voltage is 0.5 V.

### *B. Intrinsic Small Signal Equivalent Circuit*

In Fig. 8, the capacitive elements of the intrinsic small-signal equivalent circuit are shown [calculated by including the effect of $C_{\rm ds}^{\rm ext}$, $C_{\rm gs}^{\rm ext}$, and $C_{\rm gd}^{\rm ext}$ (Fig. 1)]. As usual, the highest of the three intrinsic capacitances is $C_{\rm gs}$, and, as expected from geometrical considerations, its value is lower when reducing the

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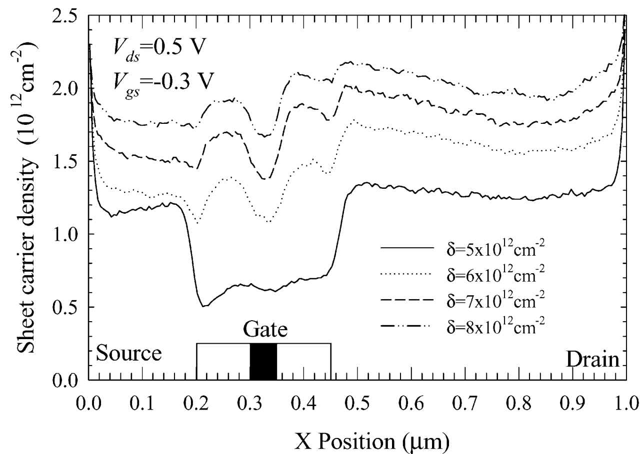


Fig. 7. Sheet-carrier density in the channel of the 50-nm-gate HEMT as a function of the position for different values of the $\delta$-doping and $V_{\rm ds} = 0.5$ V, $V_{\rm gs} = -0.3$ V. The location of the gate electrode and the recess is also shown.

gate length from 100 to 50 nm. In Fig. 8(a), another undesirable effect of a higher $\delta$-doping can be also observed; the increase of $C_{\rm gs}$. On the other hand, $C_{\rm gd}$ and $C_{\rm ds}$ [Fig. 8(b)] are almost independent of the $\delta$-doping. However, while $C_{\rm gd}$ is lower for the 50-nm HEMT than for the 100-nm one (also due to its smaller gate length, similarly to $C_{\rm gs}$), the value of $C_{\rm ds}$ increases when reducing the gate due to the stronger injection of electrons into the buffer (short channel effect, thus leading to the values of the $C_{\rm gs}/C_{\rm gd}$ ratio, also an important figure of merit of the transistors, shown in the inset of Fig. 8(a). Finally, the intrinsic cutoff frequency $(f_c = g_m/2\pi C_{\rm gs})$ increases with the higher $\delta$-doping since the enlargement of $g_m$ is more pronounced than that of $C_{\rm gs}$ [Fig. 8(c)].

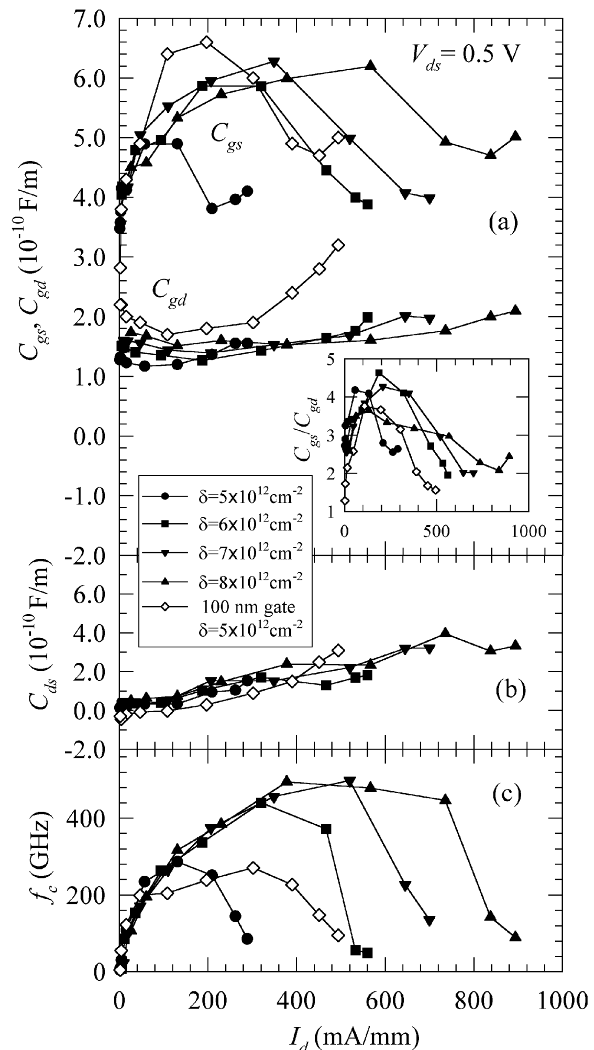


Fig. 8. (a) Gate-source $C_{\rm gs}$, gate-drain $C_{\rm gd}$, and (b) drain-source $C_{\rm ds}$, capacitances and (c) intrinsic cutoff frequency $f_c$ of the devices as a function of $I_d$ for $V_{\rm ds} = 0.5$ V. The inset shows the $C_{\rm gs}/C_{\rm gd}$ factor.

## *C. Extrinsic Frequency Performance*

We have to note that the intrinsic cutoff frequency of the devices does not take into account either the increase of $g_d$, or the influence of the $C_{\rm gd}$ and $C_{\rm ds}$ capacitances nor the contact parasitics. To characterize the extrinsic frequency performance of the devices $f_t$ and $f_{\rm max}$ are to be used instead of $f_c$. The values of the power gain with short-circuited output $|h_{fe}|^2$ and the unilateral power gain $U$ for the 50-nm-gate HEMTs with $\delta = 5 \times 10^{12}$ cm$^{-2}$ and $\delta = 8 \times 10^{12}$ cm$^{-2}$ are plotted in Fig. 9 as a function of frequency. It can be seen that at low frequencies, as long as the standard small signal equivalent circuit (shown in Fig. 1) is valid, both $|h_{fe}|^2$ and $U$ show a 20 dB/dec decay, as expected from the theoretical analysis of such equivalent circuit [6], [20]. When increasing the frequency over 50 GHz, the low-frequency equivalent circuit is not valid any more (the values that we obtain for the different elements become frequency dependent). At these frequencies not only the influence of the parasitic elements is important, but also a more complicated intrinsic equivalent circuit should be considered (a drain-to-channel capacitance $C_{\rm dc}$ associated to the dipole domain created in the high field region under the drain part of the gate, must be added [6], [20], [21]), thus, leading to a different frequency dependence of the device gains.

However, we have to stress that in our case, the dynamic behavior of the devices is not represented by means of an equivalent circuit but by their Y-parameters. Therefore, the intrinsic frequency dependence of $|h_{fe}|^2$ and $U$ is not imposed by our model but, on the contrary, it is the direct result of the MC simulation. Nevertheless, even if we are not making any assumption about the intrinsic equivalent circuit of the devices, the configuration and the values of the extrinsic elements correspond actually to a model, which has only been checked to be valid at low frequency (the equivalent circuit reproduce the experimental dynamic response). In fact, at high frequencies the description of the access reactances by means of series inductances ($L_g$ and $L_d$) and parallel capacitances ($C_{\rm pg}$ and $C_{\rm pd}$) may not be completely adequate. As a consequence of the uncertainty about the model for the parasitics we do not trust the high frequency dependence of $|h_{fe}|^2$ over 50–100 GHz (whose value is mainly determined by the values of $L_d$ and $C_{\rm pd}$) and only the extrapolated value of $f_t$ will be considered. On the contrary, the values of $U$ (even at high frequency) are not affected by the model used for the extrinsic elements of the equivalent circuit since, by definition of unilateral gain, their effects are compensated by an external passive feedback network in order to make the device unilateral. As a consequence, the values that we obtain for $f_{\rm max}$ by extrapolating the "low-frequency" behavior of $U$ (the usual technique for the experimental determination of $f_{\rm max}$,

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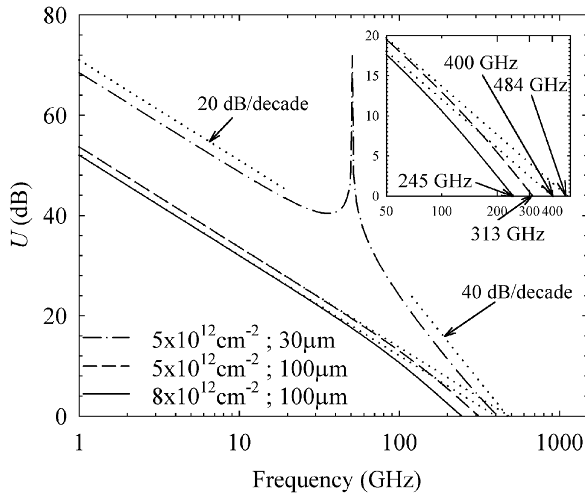


Fig. 9. Unilateral gain $U$ versus frequency for the 50-nm-gate HEMTs with $\delta = 5 \times 10^{12}\text{cm}^{-2}$ ($W = 30$ and 100 $\mu$m) and $\delta = 8 \times 10^{12}$ cm$^{-2}$ ($W = 100$ $\mu$m) together with the extrapolations of their "low frequency" behavior (decay of 20 dB/dec) for $V_{\rm ds} = 0.5$ V and the $V_{\rm gs}$ giving the maximum $f_{\max}$. The inset shows the enlargement of the frequency range for which $U$ of the devices with $W = 100$ $\mu$m go to unity (0 dB).

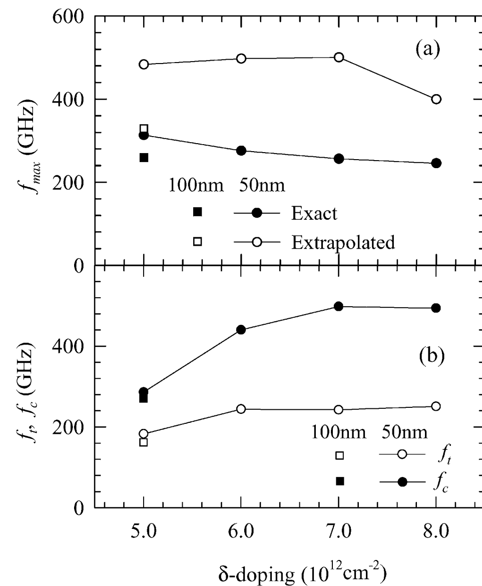


Fig. 10. Maximum values of (a) $f_{\max}$ and (b) $f_t$ and $f_c$ as a function of the $\delta$-doping for the 100-nm and 50-nm HEMTs for $V_{\rm ds} = 0.5$ V and the $V_{\rm gs}$ giving the maximum $f_{\max}$ (or $f_t$). The width of the devices is $W = 100$ $\mu$m.

since measurements are only possible up to less than 200 GHz) generally do not coincide with the frequencies for which $U$ goes to unity. Therefore, a distinction between extrapolated and exact values of $f_{\max}$ will be made in the following.

The values of $U$ at high frequencies show a faster decay than the theoretical 20 dB/dec, thus, resulting in $f_{\max}$ values lower than expected by extrapolating the "low-frequency" decrease (Fig. 9). This happens since the presence of $C_{\rm dc}$ in the equivalent circuit provokes a positive feedback in the device that increases the gain at low-frequency. Its influence on $U$ could be approximated by taking $C_{\rm dc}$ out of the model and using a lower value for $C_{\rm gs}$ [21], which is the assumption that we make in the experimental measurements. However, when $C_{\rm dc}$ is significant, neither this reduced value of $C_{\rm gs}$ nor the extrapolated $f_{\max}$ agree with their real values. Moreover, $U$ can show a resonance peak (also due to the effect of $C_{\rm dc}$) when parasitics are negligible and the condition $C_{\rm gs} \leq (g_m/g_d)C_{\rm dc}$ is fulfilled [6], [20]. Thus, this will only happen for (i) low values of $W$ (when $R_g$ is small and parasitics can be neglected) and (ii) high values of $g_m/g_d$ and nonnegligible $C_{\rm dc}$ (since $C_{\rm dc}$ is much lower than $C_{\rm gs}$). This is the case shown in Fig. 9 for $\delta = 5\times10^{12}$ cm$^{-2}$ and $W = 30$ $\mu$m. At the resonant frequency another pole is added to the frequency behavior of $U$, thus passing from the "low-frequency" 20 dB/dec decay to a stronger one of 40 dB/dec [6], [20], [21] and leading to a substantial difference between the extrapolated and the exact values of $f_{\max}$ as can be observed in Fig. 9.

The dependence on the $\delta$-doping of the maximum values of $f_{\max}$ of the HEMTs with $W = 100$ $\mu$m obtained both from the extrapolation of the "low-frequency" behavior and from the exact high-frequency dependence of $U$ are shown in Fig. 10(a). Even if a considerable difference between extrapolated and exact values of the $f_{\max}$ of the 50-nm HEMTs is observed, they follow the same trend; a degradation of their value when increasing the $\delta$-doping. Indeed, for $\delta = 8 \times 10^{12}$ cm$^{-2}$ the extrapolated and exact values of $f_{\max}$ approaches the values corresponding to the 100-nm-gate HEMT (329 and 256 GHz, respectively). On the other hand, the maximum values of $f_t$ [Fig. 10(b)] show a significant parallelism with the results of the intrinsic $f_c$ [Fig. 8(c)] since the "low frequency" behavior of $|h_{fe}|^2$ (and consequently the extrapolated $f_t$) only takes into account the influence of the extrinsic resistances and capacitances on the intrinsic transconductance and gate capacitance of the device.

## V. Influence of the Device Width

The intrinsic MC simulation of the devices does not depend on the device width, since the only output parameter is the current, which scales linearly with $W$. However, the different dependence on $W$ of the extrinsic elements of the equivalent circuit makes the extrinsic dynamic behavior of the device to be dependent on $W$. Indeed, as shown in Fig. 9, $U$ depends on the value of the parasitic resistances (and, consequently, of $W$) but is independent of the parasitic capacitances and inductances since, by definition of unilateral gain, their effects can be compensated by an external passive feedback network. Conversely, $|h_{fe}|^2$ (power gain with short-circuited output) strongly depends on the value of every parasitic element, but mainly at high frequency and therefore the extrapolated value of $f_t$ remains almost unchanged with $W$.

The values of $f_{\max}$ (exact and extrapolated) and $f_t$ as a function of $W$ for the 50-nm HEMT with $\delta = 8 \times 10^{12}$ cm$^{-2}$ are plotted in Fig. 11 for $V_{\rm ds} = 0.5$ V and the $V_{\rm gs}$ giving the maximum $f_{\max}$ (or $f_t$). One important remark that must be made before performing the analysis of the dependence on $W$ of the frequency behavior of the HEMTs is that the results shown previously (Fig. 9) were obtained by using a model for the extrinsic capacitances that considers $C_{\rm pd}$, $C_{\rm gs}^{\rm ext}$, and $C_{\rm gd}^{\rm ext}$ to be directly proportional to $W$. However, for very short $W$ these geometric capacitances do not actually vanish but reach a certain saturation value due to fringing effects. This offset (the value that the capacitances take for $W = 0$) makes the relative effect of the par-

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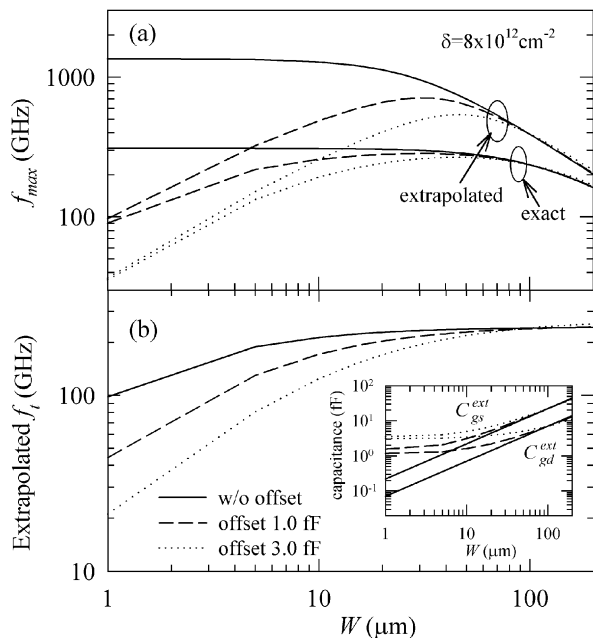


Fig. 11. (a) Extrapolated and exact $f_{\max}$ and (b) extrapolated $f_t$ for the 50-nm HEMTs with $\delta = 8 \times 10^{12}$ cm$^{-2}$ as a function of the width of the devices for $V_{\rm ds} = 0.5$ V and the $V_{\rm gs}$ giving the maximum $f_{\max}$ (or $f_t$). Three different models for the extrinsic capacitances are used; (solid lines) without offset, (dashed lines) with offset of 1 fF and (dotted lines) 3 fF. The inset shows the values of $C_{\rm gs}^{\rm ext}$ and $C_{\rm gd}^{\rm ext}$ in the different models.

asitic capacitances more important and leads to a deterioration of the values of both $f_{\max}$ and $f_t$. In Fig. 11(a) we have also represented the values of $f_{\max}$ obtained by considering offset capacitances of 3.0 fF for $C_{\rm gs}^{\rm ext}$ and $C_{\rm gd}^{\rm ext}$, respectively, ($C_{\rm pd}$ does not affect the value of $f_{\max}$). These values have been chosen according to the experimental measurements of these parameters as a function of $W$ in 100-nm-gate-HEMTs. The values obtained with lower offset capacitances of 1.0 fF are also plotted in order to show their effect on $f_{\max}$ and $f_t$. The inset of Fig. 11 shows the values of $C_{\rm gs}^{\rm ext}$ and $C_{\rm gd}^{\rm ext}$ used in the three models.

In Fig. 11, it can be observed that when using the model without offset capacitances the values obtained for $f_{\max}$ (both exact and extrapolated) considerably increase when reducing $W$, thus ratifying the importance of reducing the gate resistance to optimize the extrinsic behavior of the devices [9]. However, the strong increase of the extrapolated value is fictitious, since it is affected by the previously commented low frequency increase of $U$ associated to $C_{\rm dc}$. Focusing on the exact value of $f_{\max}$ (that seems to be more realistic than the extrapolated value), Fig. 11(a) shows that it increases when decreasing $W$, reaching a quasisaturated value when $W$ is lower than 10–20 $\mu$m. However, if the correct model for the parasitic capacitances (with offset values) is used, we can appreciate that the value of $f_{\max}$ first increases when reducing $W$, but only down to a certain value of $W$, for which $f_{\max}$ begins to decrease. Therefore, the maximum value of $f_{\max}$ is obtained for an intermediate value of $W$, around 50 $\mu$m if the experimental offset values are used (3.0 fF) and around 30 $\mu$m if the offset is reduced to 1 fF. In the figure we can clearly observe that the maximum achievable $f_{\max}$ is greatly deteriorated because of the offset capacitances. We have also checked that the most important contribution to the degradation of $f_{\max}$ is the offset value of $C_{\rm gd}^{\rm ext}$ since it acquires a higher relative importance with respect to the total value of $C_{\rm gd}$ (which is much lower than $C_{\rm gs}$). The increase of the total $C_{\rm gd}$ leads to the decrease of the $C_{\rm gs}/C_{\rm gd}$ factor, and consequently to the decrease of $f_{\max}$. A similar effect is observed in the case of $f_t$, Fig. 11(b), thus showing that the operating frequency of the HEMTs can be improved by reducing the value of the offset parasitic capacitances by means of the optimum design of the device masks to avoid the fringing capacitances. Special importance must be given to the reduction of the offset of $C_{\rm gd}^{\rm ext}$, since it leads to a significant decrease of both $f_{\max}$ and $f_t$. It is also important to choose the optimum value for the device width to reach the best possible performance. However, in this case we have not a great freedom to choose $W$, mainly at very high frequencies, since $W$ must be decreased when increasing the operating frequency of the devices to avoid problems of impedance matching of the devices [10].

## VI. Conclusions

By using a 2-D MC model, we have performed simulations of 50-nm-gate AlInAs–GaInAs lattice matched HEMTs with different values of $\delta$-doping and widths of the devices in order to determine the values of these technological parameters providing the optimum high-frequency performance (characterized by the maximum $f_{\max}$ and $f_t$).

We have checked that the effect of the surface charges can reach the channel and reduce the drain current flowing through the HEMTs and that this influence can be avoided by raising the value of the $\delta$-doping (thus also increasing $g_m$, $f_c$ and the extrapolated value of $f_t$). However, by increasing the $\delta$-doping the value of $f_{\max}$ is deteriorated. Therefore, the $\delta$-doping must be chosen as a tradeoff between high $f_t$ on one hand and high $f_{\max}$ on the other hand. Moreover, for applications needing a minimum amount of ac power, the value of the $\delta$-doping of the HEMTs must be sufficiently high to provide enough current. The dependence of $U$ at high frequency has also been studied showing that the values obtained for $f_{\max}$ by extrapolating the "low-frequency" behavior of the unilateral gain provide much higher values than the exact frequencies for which $U$ go to unity.

When trying to optimize the width of the devices it is important to choose a good model for the parasitic capacitances $C_{\rm pd}$, $C_{\rm gs}^{\rm ext}$, and $C_{\rm gd}^{\rm ext}$, since their value is not strictly proportional to $W$, but they have an offset value when $W$ equals to zero. We have observed that these offset capacitances become important when reducing $W$ (which is necessary for high frequency applications) degrading the values of $f_t$ and $f_{\max}$. Therefore, the appropriate value for $W$ must be also carefully chosen to obtain the best frequency performance, taking into account that its value must be low enough (depending on the operating frequency) to allow the impedance matching of the devices. We have also confirmed that important design efforts must be made to reduce the value of these offset capacitances (mainly that of $C_{\rm gd}^{\rm ext}$) since it can lead to a significant improvement of the frequency performance of the devices.

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