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Reliability assessment platform for the power semiconductor devices – Study case on 3-phase grid-connected inverter application

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Abstract: Because of the high cost of failure, the reliability performance of power semiconductor devices is becoming a more and more important and stringent factor in many energy conversion applications. Thus, the need for appropriate reliability analysis of the power electronics emerges. Due to its conventional approach, mainly based on failure statistics from the field, the reliability evaluation of the power devices is still a challenging task. In order to address the given problem, a reliability assessment platform is proposed in this paper. An advanced reliability design tool software, which can provide valuable reliability information based on given mission profiles and system specification is first developed and its main concept is presented. In order to facilitate the test and access to the loading and lifetime information of the power devices, a novel mission profile based stress emulator experimental setup is proposed and designed. The link between the stress emulator setup and the reliability tool software is highlighted. Finally, the reliability assessment platform is demonstrated on a 3-phase grid-connected inverter application study case.

Keywords: Reliability tool, mission profiles, stress emulator, power device, thermal cycling.

1. Introduction

Nowadays, grid-connected inverters are widely used in many mission critical applications such as, wind power generation, photovoltaics, energy distribution systems or motor drives. Due to their essential role within power systems, the reliability of the power converter is one of the main factors that influences the overall efficiency and cost of the system.

Consequently, numerous studies have been carried out in order to determine the main causes of failure in power converters, and it has been concluded that the power devices represent the most fragile components of the power electronics system, with respect to reliability [1, 2]. According to [3], the predominant source of stress for the power devices is the steady-state and cyclical temperature variation, which can result in some of the most common failure mechanisms in power modules: bond wire lift-off and solder crack [4, 5]. The unexpected wear-out failures of the power semiconductors will lead to an increase in maintenance cost, and a cutback in the total energy production of the system (due to downtime), and thus resulting in a higher cost of energy conversion.

As shown in Fig. 1, the conventional reliability improvement approach of power converters is mainly based on the failure information and statistics from the field. Due to the fact that this method is expensive and time consuming, the need for prior reliability assessment, during the design and development phase, arises. Thus, by introducing a reliability evaluation tool within the initial phases of the product life cycle, as presented in Fig. 2, the weaknesses and lifetime of the power converter can be identified before introducing the product into the market. This tool will help to optimize the design of the power converter in order to achieve a better balance between reliability and cost, and finally result in a significant cost reduction in the whole lifetime cycle of the product.

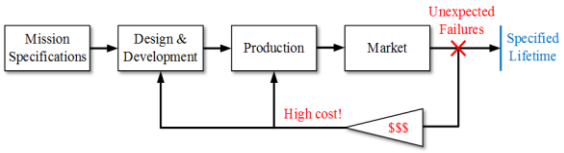

Fig. 1. Conventional reliability assessment flow.

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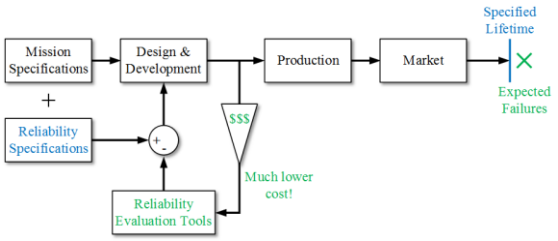

Fig. 2. New and improved reliability assessment flow.

In this paper, a reliability assessment platform consisting of a reliability evaluation tool and a stress emulator experimental setup is proposed. Initially, the main concept of the reliability tool will be introduced and a brief description of the models used within the tool will be given. Afterwards, the stress emulator setup and its operating principle and capabilities will be presented. Finally, a study case of a 3-phase grid-connected inverter application will be demonstrated.

2. Reliability tool for the design of power electronics

The reliability tool has been developed based on MATLAB and Simulink, and allows for fast and straightforward reliability assessment of the power devices according to the input mission profiles and system specifications. The tool is built in a generic manner, and thus allows various power conversion applications to be implemented (e.g. wind power generation systems, photovoltaics, motor drive, etc.). The general flow and structure of the tool for the given 3-phase grid-connected inverter application study case is presented in Fig. 3.

As it can be seen in Fig. 3, the tool employs the multi-timescale modelling concept [6], which allows the integration of the different time-constant of the system, ranging from microseconds (device switching) to days (environmental temperature variations). In order to assure a better understanding, a brief description of the models used in the tool will be given in the following.

2.1. System-level modelling

A typical 3-phase 3-level Neutral Point Clamped (NPC) grid-connected inverter application is chosen as the study case, as shown in Fig. 4. The inputs to the system are the DC-link voltage and DC current mission profiles, while the switching sequence of the active semiconductor devices is assured by means of Space Vector Modulation (SVM) technique. Additionally, an LCL filter is used in order to cancel-out the unwanted harmonics on the grid-side. In this paper, the lifetime investigation will be carried out only for the upper transistor (T_1) of the NPC power module 30A 1200V.

The system-level dynamic behaviour of the converter, resulting from running the tool, is shown in Fig. 5, where a constant DC link voltage and a step (5A → 15A) in the DC current mission profiles are assumed.

The large signal model of the converter has been build and integrated within the reliability tool.

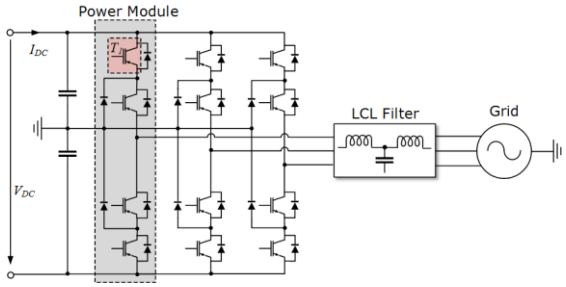

Fig. 4. Grid-connected inverter application.

2.2. Component-level modelling

The electrical outputs of the converter large signal model, such as, duty ratio (d_{abc}) or the grid phase currents (i_{abc}), will represent the inputs to the component-level block, in which the power loss and thermal model of the power device are implemented.

The power losses generated by the power semiconductors have been modelled based on the conduction and switching loss equations [7].

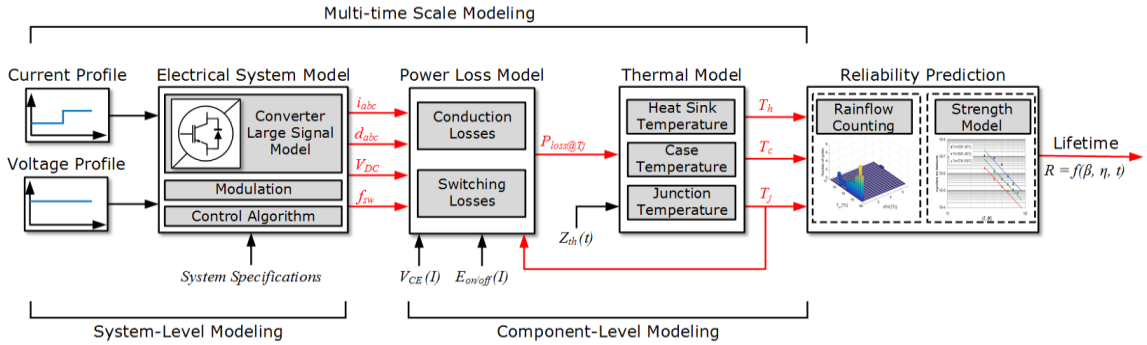

Fig. 3. General flow and structure of the tools for 3-phase grid-connected inverter application.

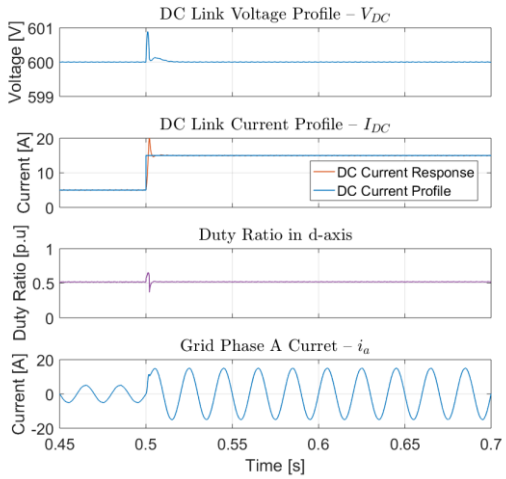

Fig. 5. System-level dynamic behaviour under given mission profile and system specification.

Additionally, due to the dependency between the loss characteristics and temperature [8], the junction temperature of the power devices has been included as a feedback from the thermal model. It should be noted that all the necessary parameters for building the average switching cycle power loss model can be extracted for the device characteristics provided by the manufacturer in the datasheet. The overall block diagram of the power loss model is shown in Fig. 6.

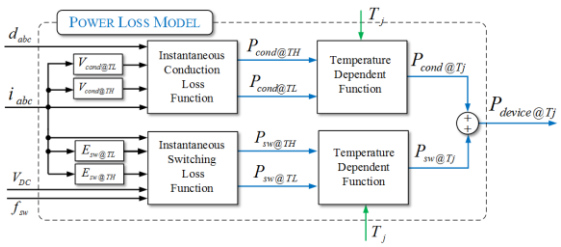

Fig. 6. Average switching cycle power loss model diagram.

The total power losses of the devices are fed into the thermal model where they can be utilized and translated into the thermal loading which occurs on the device. For the thermal calculations, a multi-level Foster thermal network is employed in order to determine the junction temperature, while the case and heat sink temperatures can be computed by filtering the power losses, through a low-pass filter (LPF), and by including the thermal network outside of the power device (e.g. thermal grease and heat sink) [9, 10]. The RC Foster thermal network is shown in Fig. 7.

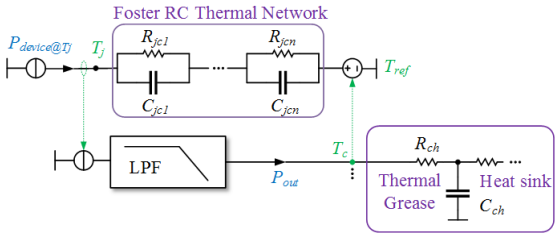

Fig. 7. RC thermal network for modelling the cooling system.

The resulting power loss and thermal loading of the upper transistor (T_1), under the given mission profiles and system specifications are shown in Fig. 8. As expected, the step in the DC current profile will lead to an increase in power losses and inherently a rise in the power device junction temperature. Additionally, the slow dynamics of the case and heat sink temperatures can be noticed.

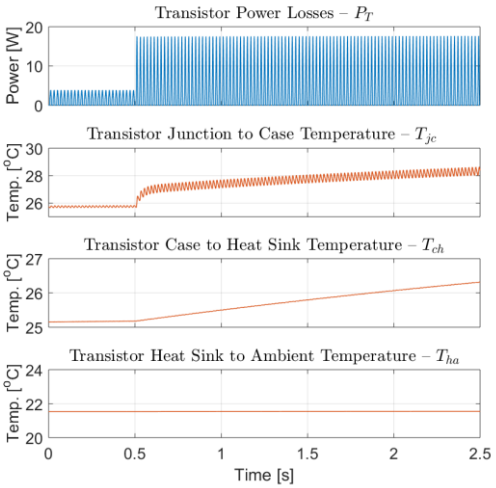

Fig. 8. Power device power loss and thermal loading.

2.3. Reliability prediction

The lifetime estimation of the power devices is conducted by means of strength models, which will apply repeated intensive thermal cycles that will accelerate the wear-out process of the components. Because the strength models require constant and regulated thermal cycles in order to be applied correctly, a rainflow counting algorithm is employed [11]. The Rainflow algorithm will determine each cycles amplitude (ΔT_j), mean value (T_{mj}) and on time period (t_{period}). Finally, the regulated thermal cycles can be linked and introduced into the Semikron lifetime model [12]. The lifetime curve for the given model is shown in Fig. 9.

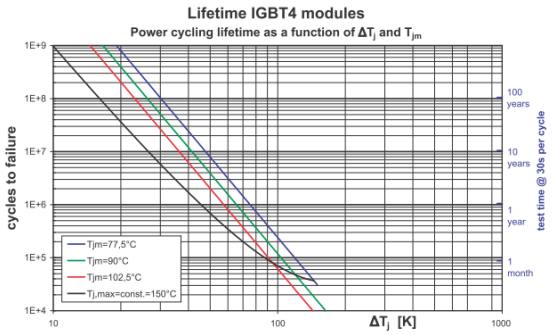

Fig. 9. Semikron strength/lifetime model [12].

Finally, the power device total accumulated damage (”consumed B10 lifetime”) can be determined by employing Miner’s rule [13].

The outputs from the reliability prediction block are shown in Fig. 7, where the amplitude and mean value of each thermal cycle, resulting from the Rainflow counting algorithm, can be observed. Additionally, the impact of the thermal cycles on the device chip damage is shown. It can be seen that the short-term cycles have little impact on the lifetime of the device due to the low cycle amplitude, while the long-term cycles will cause more damage on the device chip, and thus leading to a faster wear-out.

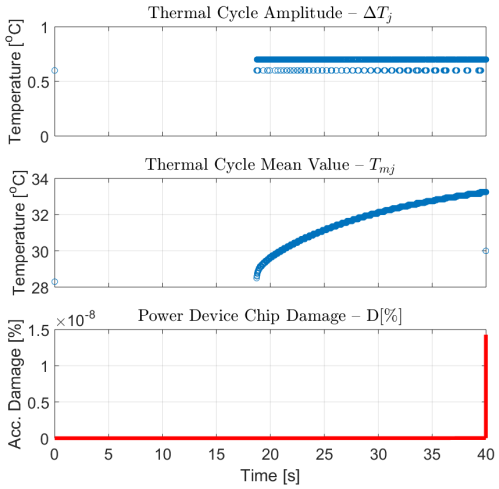

Fig. 10. Reliability evaluation of upper transistor (T_1).

3. Reliability assessment setup – Stress emulator

In order to predict the reliability performance and improve the design of the energy conversion system, the thermal loading condition of the power devices needs to be accurately assessed. However, the measurement/estimation of the thermal behaviour of the power semiconductor devices is still a challenging task, especially when considering real-field operating conditions or mission profiles.

Thus, a novel stress emulation system is proposed in this paper. The dynamical current and voltage stresses of the power devices are generated from the DC voltage and current profiles and a three level H-bridge converter setup with an inductive load (see Fig. 11), and as a result, the actual loading profiles for the power semiconductor devices considering the mission profiles of the converter are reproduced.

The load and test legs of the three-level inverter are controlled independently, the PWM signals for each leg are determined by its corresponding reference voltage, as shown in Fig. 12. The test leg is responsible for controlling the output AC voltage of the inverter, according to imposed modulation index and fundamental frequency requirements, while the load leg is used to control the output current [14].

A detailed overview of the control block diagram is shown in Fig. 12, where the dynamic behaviour of the 3-level NPC grid-connected inverter shown in Fig. 4, will represent the design target for the stress emulation system which will reproduce the same electrical/thermal stress on the power device.

4. Experimental validation

The emulation technique together with the input mission profiles have been implemented on a dSpace-controlled 10 kW H-bridge 3L-NPC converter, which can be seen in Fig. 11.

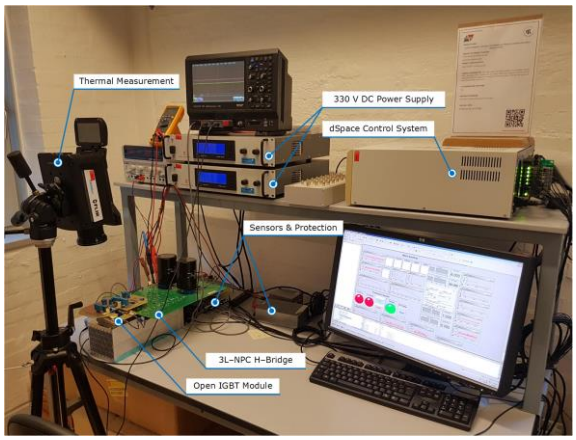

Fig. 11. Stress emulator experimental setup.

The voltage and current response of the open IGBT module under test are shown in Fig. 13,

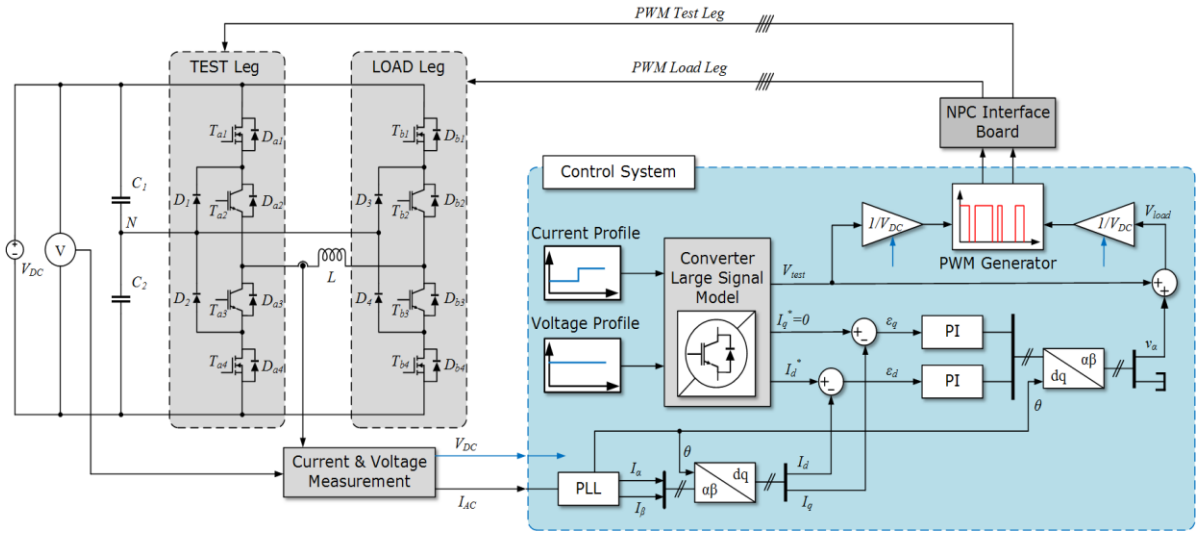

Fig. 12. Overview of control algorithm for stress emulator setup.

highlighting the fact that the stress emulator setup can accurately provide the required stress levels on the devices, and thus emulating the actual behaviour of the given grid-connected inverter application study case.

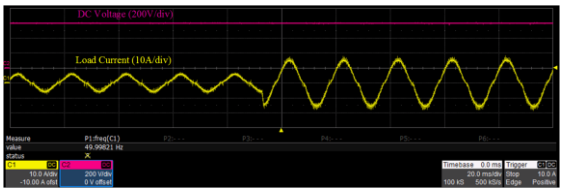

Fig. 13. Voltage and current stress levels on open IGBT module under the given mission profiles.

Finally, in order to accurately assess the thermal loading of the power semiconductor device, a FLIR infrared camera is used. The thermal distribution among the devices of the IGBT open power module recorded with the infrared camera is shown in Fig. 14.

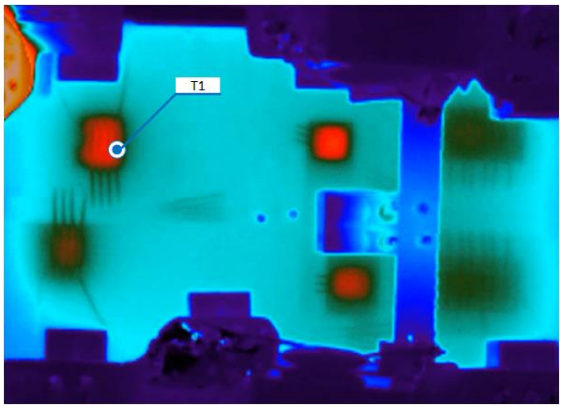

Fig. 14. Open IGBT module thermal distribution measured with FLIR infrared camera.

It should be noted that unlike the junction temperature of the device, which has been recorded with the IR camera, the case and heat sink temperatures have been measured by using an OpSens thermal fiber unit, due to their slow thermal dynamics.

As expected, the measured thermal stress on the upper transistor of the open IGBT power module satisfies the simulation results obtained through the developed reliability tools, in terms of thermal cycle amplitude and mean value, as shown in Fig. 15. The step in current amplitude will lead to more power losses generated by the upper transistor of the module. This will result in an increase in the device junction temperature cycle amplitude and mean value. On the other hand, the impact of the increase in power losses is less noticeable for the case and heat sink temperature of the device due to their slow thermal dynamics.

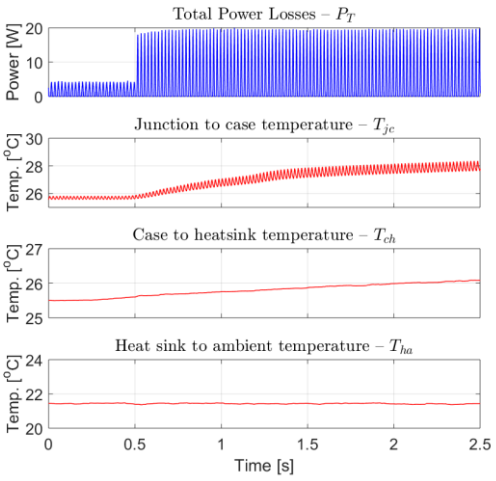

Fig. 15. Experimental validation of device thermal loading.

Thus, the correlation between the reliability tool software and the stress emulator setup can be highlighted. This will allow for the proposed reliability assessment platform to perform fast reliability / lifetime prediction simulations of power devices with the reliability tool software, and facilitate running accelerated power cycling test under the proposed stress emulator setup, for various mission profiles and system specifications.

5. Conclusions

In this paper, a reliability assessment platform for the power devices has been proposed. The platform consists of a reliability tool software and a stress emulator setup, and the correlation between them, would allow for fast and more straightforward lifetime prediction and model validation. The concept and models which are included in the reliability tool have been presented, and a 3-phase grid-connected inverter application study case has been investigated. Following, the stress emulator setup and its control method have been briefly introduced. The grid-connected inverter study case has been analysed by using the proposed stress emulator setup, and both the electrical and thermal loading of the devices have been determined. It has been established that the experimental results are in agreement with the results obtained through the reliability tool software. Finally, it can be concluded that the reliability assessment platform can be used in order to facilitate fast and accurate stress simulations, and for the design of accelerated power cycling tests for various applications, under given mission profiles, and thus improving the reliability prediction methods of power semiconductor devices.

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