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Input-Parallel Output-Parallel (IPOP) Three-Level (TL) DC/DC Converters with Minimized Capacitor Ripple Currents

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***Abstract*—This paper proposes input-parallel output-parallel (IPOP) three-level (TL) DC/DC converters with the interleaving control strategy, which is composed with two four-switch half-bridge TL (HBTL) DC/DC converters featuring with simple and compact circuit structures. Due to the IPOP structure, the component current stresses in the proposed converters are reduced. More significantly, the combination of the proposed IPOP TL circuit structure and the interleaving control strategy can largely reduce the ripple currents on the two input capacitors not only by doubling the frequencies of the ripple currents on two input capacitors but also by counteracting part of these ripple currents according to the operation principle of the proposed converters. Therefore, the proposed IPOP TL DC/DC converters with the interleaving control strategy can improve the performances of the converters in increasing the lifetimes of the input capacitors and minimizing the sizes of the input capacitors. Finally, the simulation and experimental results are presented to verify the effectiveness and feasibility of the proposed converters combined with the interleaving control strategy.**

Keywords—DC/DC converter; input-parallel output-parallel (IPOP); three-level (TL).

I. INTRODUCTION

In 1992, a three-level (TL) DC/DC converter was first proposed in [1], [2] to lower the voltage stress on the power switches for high voltage applications. Due to the advantage of low voltage stress on the power switches of the TL structure, many studies have been done on the TL DC/DC converters [3-6], which make them more applicable. In paper [7], a novel four-switch half-bridge TL (HBTL) DC/DC converter was proposed, which features only adding one block capacitor but removing two clamped diodes comparing with the conventional TL DC/DC converter [4]. Therefore, the four-switch TL DC/DC converter has simpler and more compact structure, which is the most attractive feature for an industrial application. Then, many studies have been done based on the circuit structure of the four-switch HBTL converter [8-11]. The new solutions to achieve the wide range soft-switching are discussed in [8]. A secondary-side phase-shift-controlled ZVS DC/DC converter with wide voltage gain and a three-phase DC/DC converter with low voltage stress on the power switches are proposed in [9] and [10] respectively for high voltage applications. In addition, a new control strategy is proposed to balance the voltages on the two input capacitors for the four-switch HBTL DC/DC converter [11]. The above literatures mainly focus on the topics about soft switching techniques, the converter's efficiency, and the capacitor voltage balance control strategy. But few studies pay attentions on the ripple currents flowing through the two input capacitors which make significant effects on the reliability of the converter [12].

This paper proposes the input-parallel output-parallel (IPOP) TL DC/DC converters composed of the two four-switch HBTL DC/DC converters to reduce the ripples current on the two input capacitors. Due to the IPOP circuit structure, the current stresses of the components in the proposed converters are reduced by dividing the total power among the two paralleled converters. More importantly, by combining the proposed circuit structure and the interleaving control strategy, the ripple currents on the two input capacitors can be greatly reduced not only by doubling the frequencies of the ripple currents on the two input capacitors but also by counteracting part of these ripple currents according to the operation principle of the proposed converters. Finally, the proposed IPOP TL DC/DC converters with the interleaving control strategy are verified by the simulation and experimentation results.

This paper is organized as follows. Section II illustrates the circuit structure and operation principle of the proposed converters. Section III analyzes the performances of the proposed converters associated with the interleaving control strategy. Section IV presents the simulation and experimental results to verify the proposed converters with the interleaving control strategy. Finally, the main contributions of this paper are summarized in Section V.

II. CIRCUIT STRUCTURE AND OPERATION PRINCIPLE

Fig. 1 shows the circuit structure of the proposed IPOP TL DC/DC converters, which is composed of the two four-switch HBTL DC/DC converters namely module-1 and module-2. There are two sharing input capacitors C_1 and C_2 used to split the input voltage V_{in} into two voltages V_1 and V_2 and one sharing output filter capacitor C_o as shown in Fig. 1. In the module-1, S_1-S_4 and D_1-D_4 are power switches and diodes; T_{r1} is the high frequency transformer; L_{r1} is the leakage inductance

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of T_{r1}; C_{b1} is the DC-blocking capacitor; D_{r1}-D_{r4} are output rectifier diodes; L_{o1} is the output filter inductor. The circuit structure of the module-2 is the same as that of the module-1, in which S_5-S_8 and D_5-D_8 are power switches and diodes; T_{r2} is the high frequency transformer; L_{r2} is the leakage inductance of T_{r2}; C_{b2} is the DC-blocking capacitor; D_{r5}-D_{r8} are output rectifier diodes; L_{o2} is the output filter inductor. In Fig. 1, i_{in} is the input current; i_{c1} and i_{c2} are ripple currents on C_1 and C_2, respectively; i_{p1} and i_{p2} are primary currents of T_{r1} and T_{r2}; i_{Lo1} and i_{Lo2} are currents through L_{o1} and L_{o2}; V_{cb1} and V_{cb2} are voltages on C_{b1} and C_{b2}; i_o and V_o are the output current and output voltage; V_{ab} is the voltage between point a and b; V_{cd} is the voltage between point c and d; n_1 and n_2 are turns ratios of T_{r1} and T_{r2}.

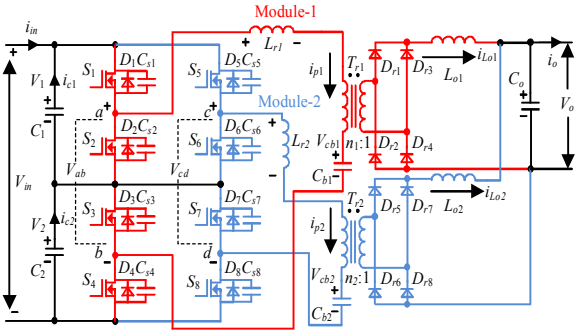


Fig. 1. Structure of the proposed IPOP TL DC/DC converters.

Fig. 2 shows the main operation waveforms of the proposed converters with the interleaving control strategy. In Fig. 2, d_{rv1}-d_{rv8} are eight driving signals of the power switches S_1-S_8, d_1, d_2 are duty ratios in one switching period, T_s is the time of one switching period, and (S_1, S_2), (S_3, S_4), (S_5, S_6), and (S_7, S_8) are complementary switch pairs. (S_1, S_7), (S_2, S_8), (S_3, S_5), and (S_4, S_6) are switch pairs having the same driving signal as shown in Fig. 2(b).

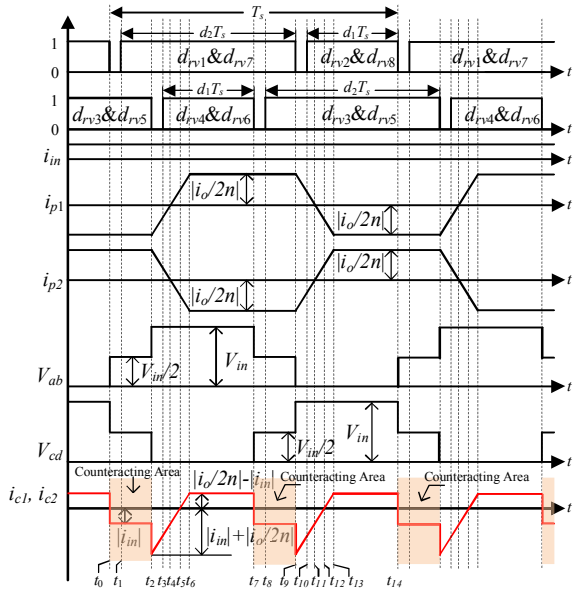


Fig. 2. Main operation waveforms.

In order to simplify the following analysis, it is assumed that: 1) the output filters inductors L_{o1} and L_{o2} are large enough to be considered as the current sources; 2) all the power switches are ideal, which means the effects of the parasitic capacitors are neglected; 3) the parameters of two modules are identical, which means $n_1 = n_2 = N$; $L_{r1} = L_{r2} = L_r$; $i_{p1} = -i_{p2} = i_p$; 4) the input current i_{in} is considered as a constant in the switching period due to the effect from the output impedance of the input power supply and impedance of the input line on the input current.

Fig. 3 shows the equivalent circuits to illustrate the operation principle of the proposed converter with the interleaving control strategy shown in Fig. 2.

Stage 1 [t_0-t_1]: At t_0, switches S_2 and S_8 are turned off. V_{ab} increases to $V_{in}/2$ and V_{cd} decreases to $V_{in}/2$. The currents i_{p1} and i_{p2} would only freewheel through D_1, S_5, L_{r2}, T_{r2}, C_{b2}, D_7, S_3, C_{b1}, T_{r1}, and L_{r1} but not flow through C_1, which means the i_{p1} through C_1 and i_{p2} through C_1 counteract each other, as highlighted in Fig. 2. Therefore, during this stage, i_{c1} and i_{c2} are the same, which are both $-i_{in}$.

Stage 2 [t_1-t_2]: At t_1, switches S_1 and S_7 are turned on at zero-voltage. The currents i_{p1} and i_{p2} would freewheel through S_1, S_5, L_{r2}, T_{r2}, C_{b2}, S_7, S_3, C_{b1}, T_{r1}, and L_{r1}, which means the i_{p1} through C_1 and i_{p2} through C_1 still counteract each other, as highlighted in Fig. 2. Therefore, these switching actions have no effect on i_{c1} and i_{c2} whose values maintain $-i_{in}$.

Stage 3 [t_2-t_3]: At t_2, the switches S_3 and S_5 are turned off. The current i_{p1} would freewheel through S_1, C_1, C_2, and D_4. V_{ab} increases to V_{in}, therefore i_{p1} starts to increase linearly. The current i_{p2} would freewheel through S_7 and D_6. V_{cd} decreases to 0 V, therefore i_{p2} begins to decrease linearly. The expressions of i_{p1} and i_{p2} are

$$i_{p1} = -\frac{i_o}{2 \cdot N} + \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) \tag{1}$$

$$i_{p2} = \frac{i_o}{2 \cdot N} - \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) \tag{2}$$

The currents i_{c1} and i_{c2} change to $-(|i_{in}|+|i_{p1}|)$ from $-i_{in}$ and start to increase. During this stage, output rectifier diodes D_{r1}-D_{r4} and D_{r5}-D_{r8} turn on simultaneously, therefore there is no power transferring from the input power and C_{b1} to the output.

Stage 4 [t_3-t_4]: At t_3, switches S_4 and S_6 are turned on at zero-voltage. The current i_{p1} would freewheel through S_1, C_1, C_2, and S_4. The voltage of V_{ab} remains V_{in}. The current i_{p2} would freewheel through S_7 and S_6. The voltage of V_{cd} still equals to 0 V. During this stage, i_{c1} and i_{c2} are still increasing and their absolute values stay at $|i_{in}|+|i_{p1}|$.

Stage 5 [t_4-t_5]: At t_4, i_{p1} increases to 0 A and i_{p2} decreases to 0 A, then current directions of i_{p1} and i_{p2} begin to change, the absolute value of i_{c1} and i_{c2} change to $|i_{in}|-|i_{p1}|$.

Stage 6 [t_5-t_6]: At t_5, the currents i_{c1} and i_{c2} increase to 0 A, then the current directions of i_{c1} and i_{c2} begin to change, the absolute value of i_{c1} and i_{c2} change to $|i_{p1}|-|i_{in}|$.

Stage 7 [t_6-t_7]: At t_6, the current i_{p1} reaches to $i_o/2N$, and then the input power begins to be transferred to output through T_{r1}, D_{r1}, and D_{r4}. The current i_{p2} decreases to $-i_o/2N$, and then the power from C_{b2} begins to transfer to output through T_{r2}, D_{r6}, and D_{r7}. i_{p1} and i_{p2} are kept at $i_o/2N$ and $-i_o/2N$. During this period, the absolute value of i_{c1} and i_{c2} remain $|i_{p1}|$-$|i_{in}|$.

The analysis of the second half switching period [t_7-t_{14}] is similar to the first half period [t_0-t_7], which is not repeated here. At t_{14}, the following operation in next period starts, which is the same as the first switching period.

Based on the above analysis, it can be observed that part of the ripple current i_{c1} can be counteracted as highlighted time periods in Fig. 2 because the primary current i_{p1} through C_1 and i_{p2} through C_1 would counteract each other during these highlighted time periods, which is illustrated in the above principle analysis of the Stage 1 and Stage 2.

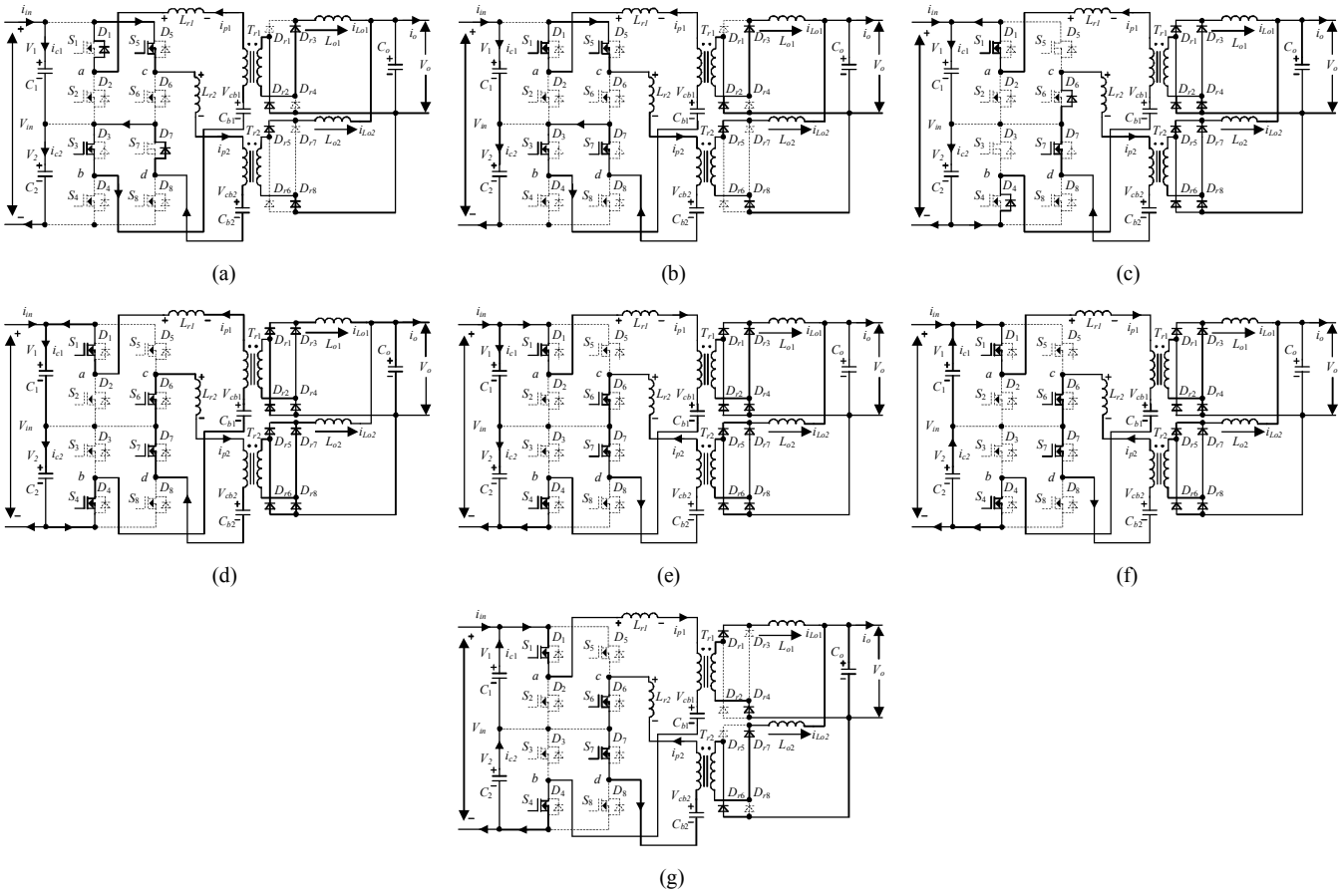


Fig. 3. Equivalent Circuits. (a) [t_0-t_1]. (b) [t_1-t_2]. (c) [t_2-t_3]. (d) [t_3-t_4]. (e) [t_4-t_5]. (f) [t_5-t_6]. (g) [t_6-t_7].

III. Performances of Proposed Converters

In this section, the performances of the proposed IPOP TL converters associated with the interleaving control strategy are analyzed in detail.

A. Voltage stresses on Power switches

The voltage stresses on the power switches S_1-S_8 are only half of the input voltage (V_{in}/2) in the steady operations due to the TL structure.

B. Duty Cycle Loss

The expression of the duty cycle loss in one switching period can be given by

$$d_{loss1} = d_{loss2} = d_{loss} = 2 \cdot (\frac{t_6 - t_2}{T_s}) = \frac{4 \cdot L_r \cdot i_o}{N \cdot V_{in} \cdot T_s} \tag{3}$$

where d_{loss1} and d_{loss2} are the duty cycle losses of the two four-switch HBTL DC/DC converters, and is the time of one switching period.

C. Output Voltage Characteristic

After considering the effect of the duty cycle loss on the output voltage V_o, V_o can be calculated by

$$V_o = \frac{V_{in}}{N} \cdot (d_1 - \frac{d_{loss}}{2}) = V_{in} \cdot (d_1 - \frac{2 \cdot L_r \cdot i_o}{N \cdot V_{in} \cdot T_s}) \tag{4}$$

where d_1 is the duty ratio for S_2, S_4, S_6, and S_8 in one cycle.

D. Ripple Currents on Input Capacitors

Due to the interleaving control strategy, the frequencies of i_{c1} and i_{c2} are twice of the switching frequency. According to Fig. 2, the ripple currents i_{c1} and i_{c2} in a half switching period can be expressed as

$$i_{c1} = i_{c2} = \begin{cases} -i_{in} & [t_0 - t_2] \\ i_{p1} - i_{in} & [t_2 - t_7] \end{cases} \quad (5)$$

By using the interleaving control strategy, the currents i_{p1} and i_{p2} are just opposite as shown in Fig. 2. The expressions of i_{p1} and i_{p2} in a half switching period can be given by

$$i_{p1} = -i_{p2} = \begin{cases} -\dfrac{i_o}{2 \cdot N} & [t_0 - t_2] \\ -\dfrac{i_o}{2 \cdot N} + \dfrac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) & [t_2 - t_6] \\ \dfrac{i_o}{2 \cdot N} & [t_6 - t_7] \end{cases} \quad (6)$$

Substituting (6) into (5), the ripple currents i_{c1} and i_{c2} in a half switching period can be rewritten by

$$i_{c1} = i_{c2} = \begin{cases} -i_{in} & [t_0 - t_2] \\ -\dfrac{i_o}{2 \cdot N} + \dfrac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) - i_{in} & [t_2 - t_6] \\ \dfrac{i_o}{2 \cdot N} - i_{in} & [t_6 - t_7] \end{cases} \quad (7)$$

The time intervals $[t_2\text{-}t_6]$ and $[t_9\text{-}t_{13}]$ as shown in Fig. 2 can be described as

$$t_6 - t_2 = t_{13} - t_9 = \frac{2 \cdot L_r \cdot i_o}{N \cdot V_{in}} \quad (8)$$

According to (7) and (8), the root-mean-square (RMS) values of i_{c1} and i_{c2} with the interleaving control strategy namely i_{c1_rms} and i_{c2_rms} can be calculated by

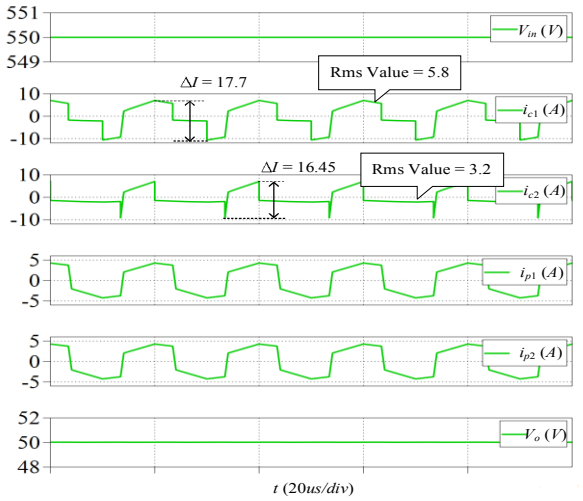
$$i_{c1\_rms} = i_{c2\_rms} = \sqrt{i_{in}^2 + \frac{i_o^2 \cdot d_1}{2 \cdot N^2} + \frac{4 \cdot L_r \cdot i_{in} \cdot i_o^2}{N^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{N} - \frac{2 \cdot L_r \cdot i_o^3}{3 \cdot N^3 \cdot V_{in} \cdot T_s}} \quad (9)$$

IV. Simultion and Experimental Verification

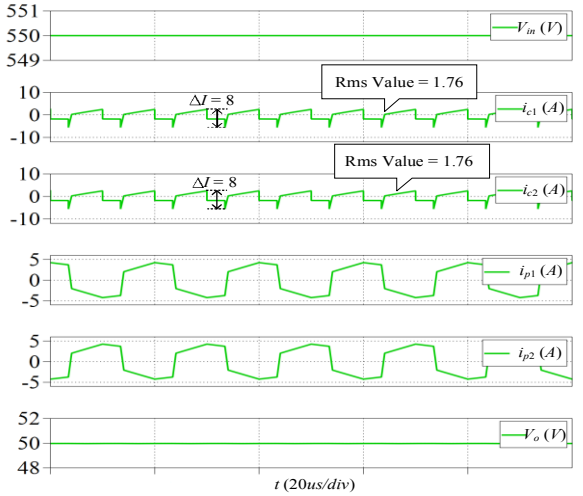
A. Simulation Verification

A simulation model is built in PLECS to verify the proposed IPOP TL DC/DC converters with the interleaving control strategy, whose circuit parameters are listed in Appendix. In the simulation, the input voltage is 550 V, the output voltage is 50 V, and the output power is 1-kW.

Fig. 4 shows the simulation results. From Fig. 4, it can be seen that the frequencies of i_{c1} and i_{c2} with the interleaving control strategy are twice of that without the interleaving control strategy. In addition, the RMS values of i_{c1} and i_{c2} are 5.8 A and 3.2 A, respectively, as shown in Fig. 4(a). After using the interleaving control strategy, the RMS values of i_{c1} and i_{c2} reduce to both 1.76 A as shown in Fig. 6(b).



(a)



(b)

Fig. 4. Simulation results. (a) Without the interleaving control strategy. (b) With the interleaving control strategy.

In order to analyze the influence of the parameter mismatch between the two modules on i_{c1} and i_{c2}, some simulation results are shown in Table I. The variables are the leakage inductors and transformer turns ratios. In Table I, $\Delta L_r = L_{r2} - L_{r1}$ and n_1, n_2 are the transformer turns ratios of T_{r1} and T_{r2}, respectively. The results of the RMS values of i_{c1} and i_{c2} are shown in Table I, where the input voltage is 550 V, the output voltage is 50 V, and the output power is 1-kW. From Table I, it can be observed that the parameter mismatch between the two modules would cause the increase of the RMS values of i_{c1} and i_{c2}, but these increasing values are very small, which means the RMS values of i_{c1} and i_{c2} when using interleaving control strategy and having parameter mismatch are still much smaller than that without the interleaving control strategy.

In summary, the simulation results verify that the ripple currents on the two input capacitors can be greatly reduced due to the combination of the proposed IPOP TL circuit structure and the interleaving control strategy.

TABLE I. SIMULATION RESULTS ABOUT PARAMETER MISMATCH BETWEEN TWO MODULES

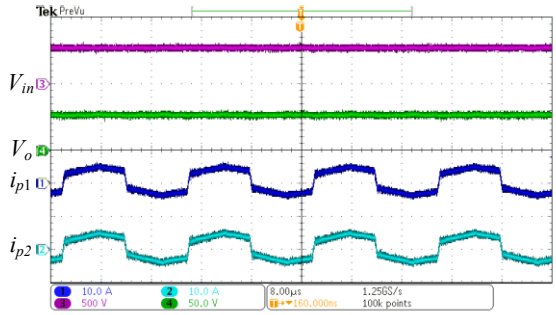
Interleaving Control Strategy	Variables					Results	
	L_{r1} (uH)	L_{r2} (uH)	ΔL_r (uH)	n_1	n_2	RMS of i_{c1} (A)	RMS of i_{c2} (A)
without	30	30	0	38/13	38/13	5.8	3.2
	30	40	**10**	38/13	**40/13**	5.5	3.0
with	30	30	0	38/13	38/13	1.76	1.76
	30	40	**10**	38/13	38/13	1.91	1.8
	30	30	0	38/13	**40/13**	2.2	1.86
	30	40	**10**	38/13	**40/13**	2.47	1.97

B. *Experimental Verification*

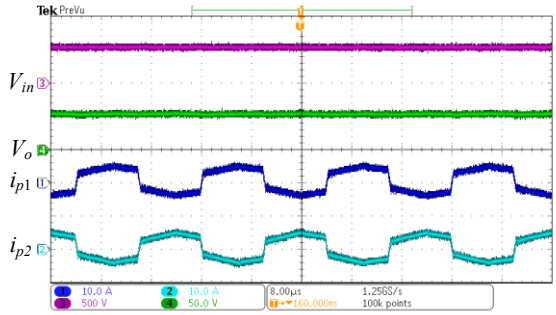
In order to verify the proposed IPOP TL DC/DC converters with the interleaving control strategy, a laboratory prototype is built, whose circuit parameters are shown in Appendix. In the built prototype, SPW47N60C3 is adopted as the primary power switches; MBR20200CTG is selected for the output rectifier diodes. In the experiments, the input voltage is 550 V, the output voltage is 50 V, and the output power is 1-kW. The performances of the established prototype are shown in Figs. 5 and 6. Fig. 5 shows the currents i_{p1}, i_{p2} and voltages V_{in}, V_o without and with the interleaving control strategy. From Fig. 5(b), it can be seen that i_{p1} and i_{p2} are just opposite because of utilizing the interleaving control strategy. Fig. 6 shows the currents i_{c1}, i_{c2} and voltages V_{ab}, V_{cd} without and with the interleaving control strategy. In Fig. 6(b), the frequencies of i_{c1} and i_{c2} with the interleaving control strategy are twice of that without the interleaving control strategy. The RMS values of i_{c1} and i_{c2} without the interleaving control strategy are 5.6 A and 3.19 A, respectively, as shown in Fig. 6(a). However, the RMS values of i_{c1} and i_{c2} with the interleaving control strategy are reduced to 1.69 A and 1.68 A, respectively, as shown in Fig. 6(b).

Based on the experimental results, it can be concluded that: 1) the frequencies of i_{c1} and i_{c2} with the interleaving control strategy are twice of that without the interleaving control strategy; 2) the part of the ripple current i_{c1} can be counteracted by combining the proposed IPOP TL circuit structure and the interleaving control strategy as highlighted in Fig. 6, which is consistent with the theoretical analysis in Section II; and 3) based on the benefits of (1) and (2), the ripple currents on the two input capacitors can be greatly reduced.

The efficiency curves with the various input voltages are shown in Fig. 7. From Fig. 7, it can be seen that the maximum efficiency with the interleaving control strategy is over 95% and the efficiencies with the interleaving control strategy are slightly higher than that without the interleaving control strategy.

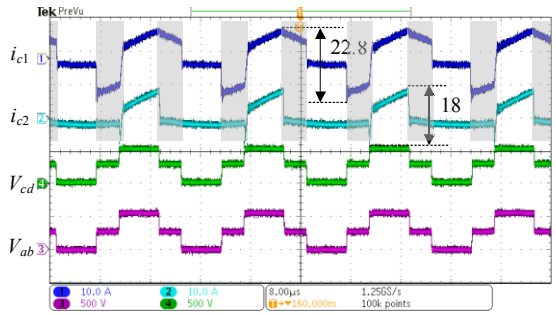


(a)

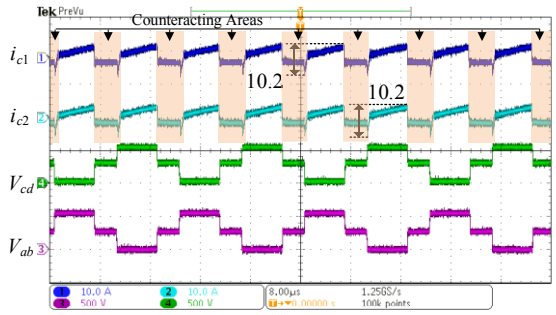


(b)

Fig. 5. Experimental results including V_{in}, V_o, i_{p1}, and i_{p2} under 1-kW. (a) Without the interleaving control strategy. (b) With the interleaving control strategy.



(a)



(b)

Fig. 6. Experimental results including V_{ab}, V_{cd}, i_{c1}, and i_{c2} under 1-kW. (a) Without the interleaving control strategy. (b) With the interleaving control strategy.

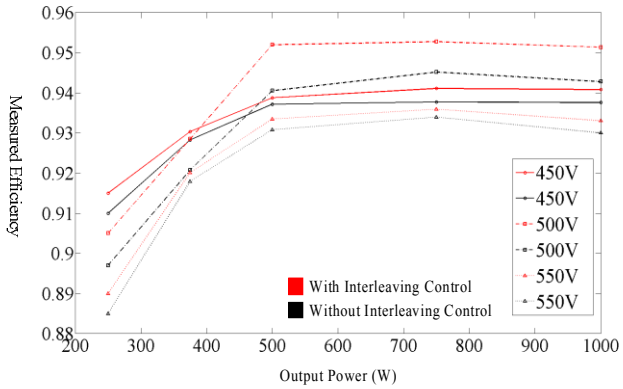


Fig. 7. Measured efficiency curves with the various input voltages.

V. Conclusion

In this paper, the input-parallel output-parallel (IPOP) TL DC/DC converters with the interleaving control strategy are proposed, which compromise the two four-switch HBTL DC/DC converters featuring with the simple and compact circuit structures. The component current stresses in the proposed converters are reduced because of the IPOP circuit structure. More importantly, combining the proposed converters and the interleaving control strategy can greatly reduce the ripple currents on the two input capacitors not only by doubling the frequencies of the ripple currents on the two input capacitors but also by counteracting part of these ripple currents due to the operation principle of the proposed circuit structure. Therefore, the proposed converters associated with the interleaving control strategy can improve the performances of the converters in reducing the input capacitors' thermal stresses, prolonging the input capacitors' lifetimes, and minimizing the input capacitors' sizes.

Appendix

TABLE II. Parmeters of Simulation Model and Experimental Prototype

Description	Parameter
Turns Ratios of T_{r1} and T_{r2}	38:13
Leakage Inductances L_{r1} and L_{r2} (uH)	30
Output Filter Capacitor C_o (uF)	470
Output Filter Inductors L_{o1} and L_{o2} (uH)	100
Input Capacitors C_1 and C_2 (uF)	14.4
DC-blocking Capacitors C_{b1} and C_{b2} (uF)	6
Switching Frequency (kHz)	50
Dead Time (ns)	400

References

[1] J. R. Pinheiro and I. Barbi, "The three-level ZVS PWM converter—A new concept in high-voltage DC-to-DC conversion," in *Proc. IEEE Int. Conf. Ind. Electron. Control Instrum. Autom.*, 1992, pp. 173–178.

[2] J. R. Pinheiro and I. Barbi, "The three-level ZVS-PWM DC-to-DC converter," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 486–492, Jul. 1993.

[3] E. Deschamps and I. Barbi, "A comparison among three-level ZVS-PWM isolated DC-to-DC converters," in *Proc. 38th Annu. Conf. IEEE Ind. Electron. Soc.*, 1998, pp. 1024–1029.

[4] F. Canales, P. Barbosa, M. Burdio, and F. Lee, "A zero-voltage switching three-level DC/DC converter," in *Proc. 22nd Int. Telecommun. Energy Conf.*, 2000, pp. 512–517.

[5] X. Ruan, Z. Chen, and W. Chen, "Zero-voltage-switching PWM hybrid full-bridge three-level converter," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 395–404, Mar. 2005.

[6] F. Deng and Z. Chen, "Control of improved full-bridge three-level DC/DC converter for wind turbines in a DC grid," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 314–324, Jan. 2013.

[7] I. Barbi, R. Gules, R. Redl, and N. O. Sokal, "DC/DC converter: Four switches $V_{pk} = V_{in}/2$, capacitive turn-off snubbing, ZV turn-on," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 918–927, Jul. 2004.

[8] Y. Shi, and X. Yang, "Wide range soft switching PWM three-level DC–DC converters suitable for industrial applications," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 603–616, Feb. 2014.

[9] W. Li, S. Zong, F. Liu, H. Yang, X. He, and B. Wu, "Secondary-side phase-shift-controlled ZVS DC/DC converter with wide voltage gain for high input voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5128–5139, Nov. 2013.

[10] T. T. Sun, H. S. H. Chung, and A. Ioinovici, "A high-voltage DC-DC converter with Vin /3—Voltage stress on the primary switches," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2124–2137, Nov. 2007.

[11] X. Yu, K. Jin, and Z. Liu, "Capacitor voltage control strategy for half-bridge three-level DC/DC converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1557–1561, Apr. 2014.

[12] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep./Oct. 2014.