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Capacitive Effects in IGBTs Limiting their Reliability under Short Circuit

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Abstract

The short-circuit oscillation mechanism in IGBTs is investigated in this paper by the aid of semiconductor device simulation tools. A 3.3-kV IGBT cell has been used for the simulations demonstrating that a single IGBT cell is able to oscillate together with the external circuit parasitic elements. The work presented here through both circuit and device analysis, confirms that the oscillations can be understood with focus on the device capacitive effects coming from the interaction between carrier concentration and the electric field. The paper also shows the 2-D effects during one oscillation cycle, revealing that the gate capacitance changes according with the shape of the electric field due to the charge distribution in the n-base. It has been identified that the time-varying capacitance leads to parametric oscillations together with the stray gate inductance, which limit the reliability of the IGBT.

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1. Introduction

The high penetration level of renewable energy technologies has set the ambitious challenge of 100% renewable electricity production for the upcoming years. However, to turn this idea into reality, semiconductor devices need to provide reliable operation having also in mind that the device will be exposed to abnormal conditions, such as short circuit. The Insulated-Gate Bipolar Transistor (IGBT) is nowadays the dominant semiconductor in the majority of power electronic applications [1]. Many efforts have been devoted to the reliability study of IGBTs, but to strengthen its position, especially with the insertion of Wide Band-Gap (WBG) materials such as Silicon Carbide (SiC), the physical mechanisms taking place in IGBTs under short circuit conditions, have to be better understood.

With regard to this, the IGBT short-circuit robustness is nowadays compromised by a ringing phenomenon occurring under adverse combinations of large stray inductances under certain operation conditions. Such oscillations have only been reported for IGBTs, for example, SiC MOSFETs do not show oscillatory behaviour during short circuit [2, 3]. The root cause has not been well understood yet and today's IGBTs may catastrophically fail in case that the gate voltage oscillation amplitude diverges, leading to a gate-oxide breakdown [4]. The experimental evidence of such phenomenon can be found in [4-10], and, recently, also for trench-gate, field-stop IGBTs [4, 10]. So far, two different approaches have been followed to cope with the oscillations: circuit analysis and device analysis. This paper gives a better understanding by including both circuit and device analyses, as presented in [11], e.g., for the diode reverse recovery.

In this paper, the short-circuit oscillation mechanism has been investigated by mixed-mode device simulations on a 3.3-kV planar IGBT cell, showing that, IGBTs have low n-base doping and high-level carrier injection features, which favours Kirk effect occurrence, especially during short-circuit. For this reason, trench IGBTs are also prone to oscillations. This work shows the 2-D effects during one oscillation cycle revealing that the gate capacitance varies according with the electric field shape. The resulting weak electric field near the emitter leads to electron accumulation effects as the main contributor to the capacitance variation.

2. Short-circuit experimental performance

The short-circuit performance of a SPT (Soft Punch Through) 3.3-kV planar single-chip IGBT has been evaluated. Fig. 1 shows the waveforms at 25ºC with a gate resistance of 2.2 Ω and collector inductance of 1 µH. The tests have been carried out at a DC-link voltage of 1 kV and 1.9 kV. Better ruggedness is demonstrated at high DC-link voltages while gate oscillations are observed at low DC-link voltages. The amplitude of these oscillations increases with the short-circuit pulse duration, which could turn into a gate breakdown failure due to excessive voltage amplitude.

The driving factors for the occurrence of the short-circuit oscillations have previously been investigated

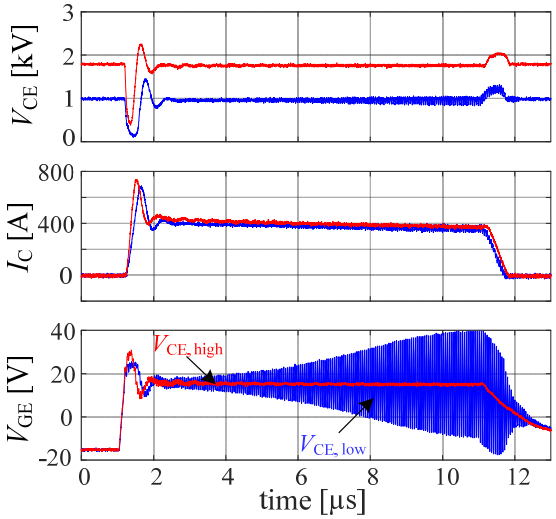

Fig.1. Short-circuit tests of a 3.3-kV planar single-chip IGBT showing oscillations at V_{DC} = 1 kV (blue) at 25 ºC.

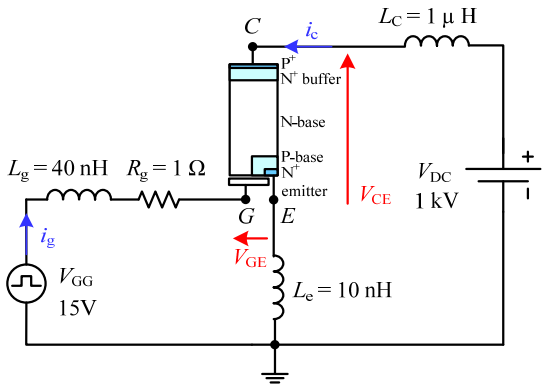

Fig. 2. Circuit used to perform the mixed-mode device simulations with Sentaurus TCAD.

by the authors in [4, 10]. From the experimental results, low collector–emitter voltage V_{CE}, high gate-emitter voltage V_{GE} and low junction temperature are the key factors to enable the short-circuit oscillations. Here, focus is given only on one parameter, V_{CE}, since its variation is crucial for having or not having oscillations.

3. TCAD short-circuit simulations

Mixed-mode device simulations have been carried out with the set of parameters presented in Fig. 2. These parameters have been selected in agreement with the ones from the experiments. The short-circuit voltage and current waveforms, simulated under two DC-link voltages of 1 kV and 2 kV can be observed in Fig 3. Through these simulations, the oscillation mechanism has been reproduced demonstrating that oscillations can only be triggered at low collector voltages. This is vital in order to identify, which parameters influence the short-circuit process and later justify the root cause of such oscillations. The oscillation frequency is slightly different, being 20 MHz for the experiments and 9 MHz for the simulations. Further adjustments can be made on the inductance and input capacitance to match the oscillation frequency. In the simulation the starting gate voltage has been set to 0V, with the purpose of minimizing computational time.

Under short circuit, the mobile carriers strongly influence the charge distribution in the n-base, which play a major role in determining the shape of the electric field. In Fig. 4, the comparison of the electric field and carrier distribution profiles under short circuit and blocking conditions is shown. The electric field during blocking conditions is only

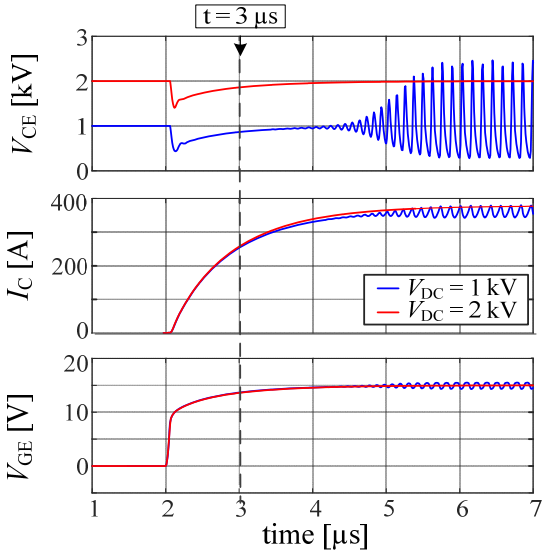

Fig. 3. Short-circuit simulation of a 3.3-kV planar IGBT half-cell showing oscillations after 3 µs at V_{DC} = 1 kV.

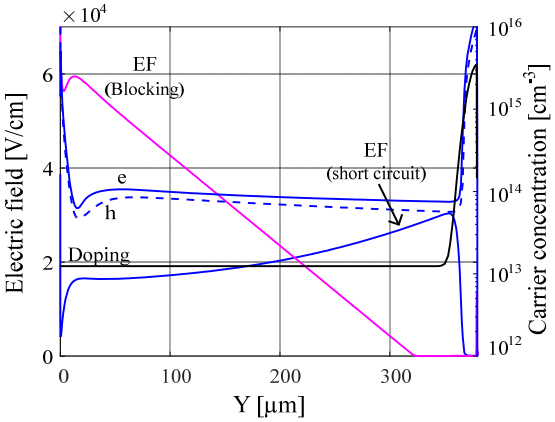

Fig. 4. Simulated electric field (EF) and carrier concentration (e, h) along a cut in the vertical direction (see Fig. 7) corresponding with t = 3 µs in Fig. 3. The blocking electric field is reported for comparison.

determined by the doping concentration and corresponds to the well-known triangular shape. However, the electric field peak rotates during short circuit and is located at the collector. This behavior is not new and commonly known as the Kirk Effect, previously presented in IGBTs in [12].

Furthermore, Fig. 5 illustrates how the collector voltage affects the position of the electrons and holes in the n-base along with the electric field. The cut has been done through the vertical axis at the time instant of t = 3 µs (Fig. 3). It can be concluded that at low V_{CE}, the electron carriers are nearer to the emitter, while the electrons are swept out from the emitter to the collector at high V_{CE}.

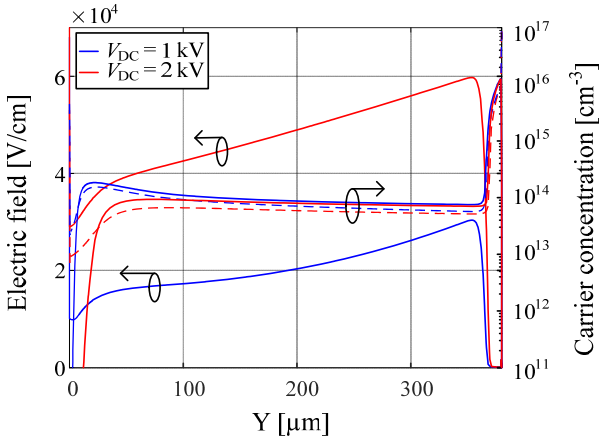

Fig. 5. Simulated electric field and electron (solid) and hole (dashed) carrier profiles during short-circuit operation under two DC-link voltages of 1 kV and 2 kV.

At sufficiently high current densities, such as in the case of short circuit, and relatively low collector voltages, i.e., V_{CE} = 1 kV for a 3.3-kV IGBT device, three important phenomena take place: (1) both hole and electron concentrations are one order of magnitude higher than the background doping of the n-base (high-injection level), as it can be seen in Figure 4. The amount of electrons becomes dominant over the sum of holes and the background doping, which changes the sign of the electric field gradient *dE/dy*; (2) an electron charge-storage effect at the emitter of the IGBT is observed at low DC-link voltages in Figure 5. This coincides with a weaker electric field near the emitter; (3) at low electric fields, both hole and electron velocities are field dependent (i.e., not saturated). The weak electric field near the emitter is associated with low carrier velocities, which in turn causes the carrier density to increase. The excess of charge coincides with a capacitance increase, as justified later.

4. Analysis of the short-circuit oscillations

The analysis presented here has been carried out when the oscillations are constant in amplitude. To that end, a time-zoom between the time instants 5.1 µs and 5.45 µs in Figure 3 can be observed in Figure 6. This helps to evaluate the relation between each electrical parameter in respect to the physical mechanisms inside the IGBT. In Figure 6, the gate current and the instantaneous input capacitance are additionally plotted. The instantaneous input capacitance has been calculated from i_g and V_{GE}

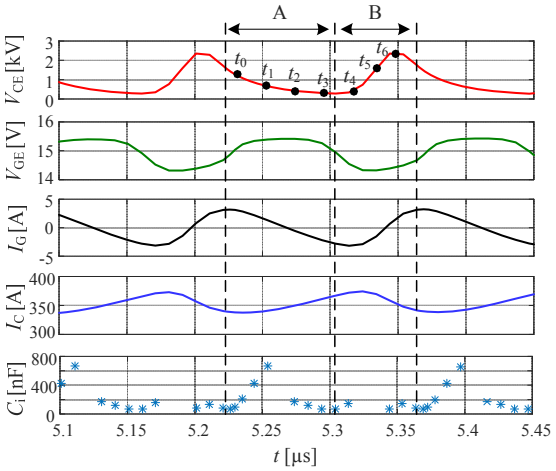

Fig. 6. Short-circuit oscillations showing the two phases (A and B) taking place in the oscillations of the IGBT, together with the instantaneous input capacitance C_i.

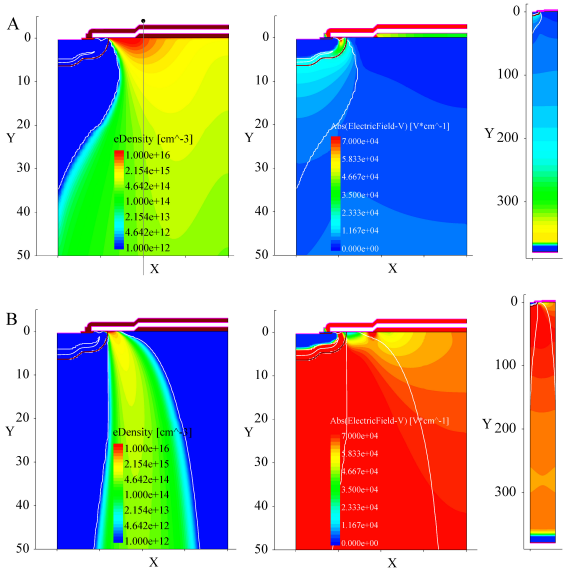

Fig. 7. The 3.3 kV planar IGBT during phases A and B. Left: electron density; middle: electric field and right: electric field through the whole cell. The cut line for Fig. 8 is highlighted.

through the formula, $C_i = i_g \, x \, dt/dV_{GE}$. One oscillation cycle is divided into two phases: phase A or charge-storage phase and phase B or voltage build-up phase. In the following sections, a detailed description is given for each phase.

3.1. Phase A: Charge-Storage Phase

A carrier accumulation effect appears at the emitter of the IGBT coinciding with an increase of

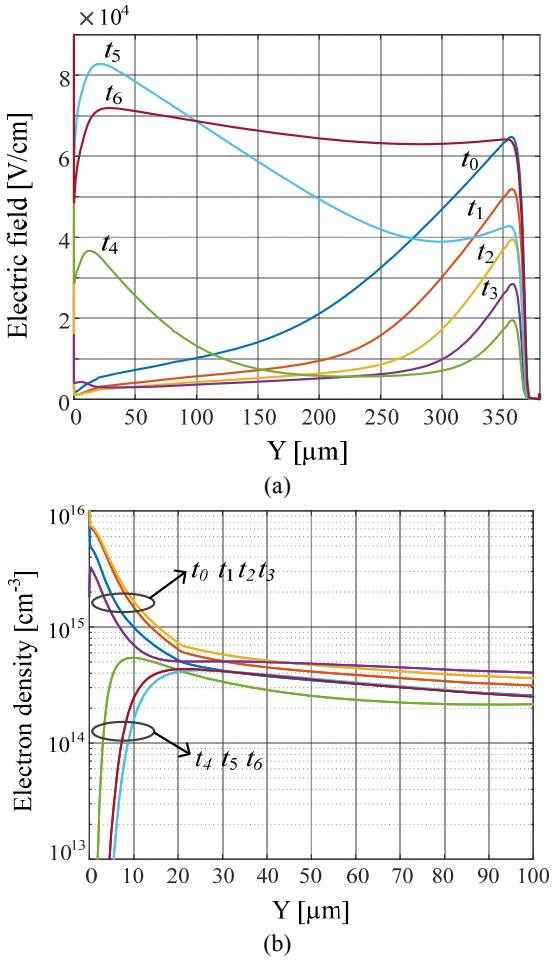

Fig. 8. Electric field variation (a) and electron density profile (b) in the planar IGBT at the time instants illustrated in Fig. 6.

the instantaneous input capacitance, about 10 times higher, as it is calculated in Figure 6. The gate voltage V_{GE} rises above 15 V (the positive gate bias is V_{GG} = 15 V), which in turn causes the collector voltage V_{CE} to drop in order to sustain the short-circuit current. The electron accumulation effect is observed as soon as V_{CE} drops. The result is that the electric field becomes weaker, especially near the emitter due to the Kirk effect, thus the drift velocity is substantially lower in this region. The observed charge-storage effect is in agreement with the assumption of constant short-circuit current, $J_n = qnv_{n,}$ implying that a lower electron velocity can only result in a higher electron density driving the IGBT into the Kirk effect mode. This is confirmed in Figure 7, where a low electric field at the surface of the IGBT coincides with an electron accumulation region. Additionally, Figure 8a and 8b show the electric field and the carrier density at different times during the oscillation, showing that, during phase A (t_0, t_1, t_2 and t_3) the electric field at the emitter is weak and the amount of electrons is high.

By looking at waveforms in Figure 6, one can observe that during phase A, the gate current changes its direction indicating that two mechanisms take place: (1) charge period: this happens when the gate current has a positive value, which means that the gate capacitance charges up. The charge period coincides with the highest capacitance value, so the energy initially stored in the gate inductance is now transferred to a larger capacitance, thus causing a slower dV_{GE}/dt. Once the current reaches zero, the capacitance is charged beyond the positive gate bias (V_{GG} = 15 V) and it starts the discharging period reversing the current through the inductance; (2) discharge period: this happens when the gate current has a negative value, thus the voltage across the large capacitance starts falling as the current through the gate inductance begins to rise. In this case, the energy stored in the gate capacitance is now transferred to the gate inductance. During this period, the gate capacitance changes its value to a lower one causing V_{GE} to decrease.

3.2. Phase B: Voltage Build-Up Phase

The excess electron concentration at the emitter of the IGBT is swept out, ending up in a smaller value of input capacitance (see Fig. 6). The gate voltage V_{GE} drops below 15 V, which in turn causes the collector voltage V_{CE} to rise in order to sustain the short-circuit current.

As soon as V_{CE} increases, the electric field builds up across the n-base of the IGBT, thus the electron velocity increases pushing the electrons to the middle of the n-base. This re-distribution of the carriers brings the benefit of counteracting the Kirk effect, so the electric field comes back to its well-known triangular shape. This is confirmed in Figure 7 and Figure 8 (i.e., t_4, t_5 and t_6) where the electric field is higher at the surface and the excess electron carriers are no longer accumulated at the surface. During phase B, the gate current charges and discharges the gate capacitance, but now the capacitance has a small value.

To sum up, the evolution of the IGBT during each oscillation cycle can be represented by two situations, as observed in Figure 9: (1) a rotated-field associated with a surface electron-accumulation region contributing to a high capacitance value, this

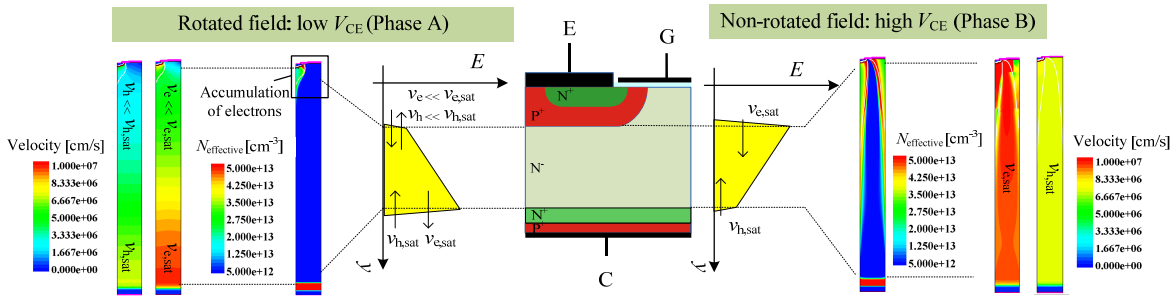

Fig. 9. The IGBT during the short-circuit oscillations (phases A and B). The excess carrier concentration at the surface is observed during phase A at low V_{CE}: v_e – electron velocity, v_h – hole velocity, $N_{effective}$ – effective charge concentration, E – electric field.

results from the low carrier velocity at low $V_{CE;}$ and (2) a non-rotated field coinciding with a low capacitance value and no electron accumulation effects as a result of low V_{CE}.

Thanks to the above observation, one can now understand how it is possible to relate the field distortions to capacitance variations by including the device excess charges during each oscillation cycle, as the main contributor to the time-varying gate capacitance. This is the basis of a parametric oscillation where the capacitance behaves as the active element.

5. Parametric oscillations in IGBTs

The results from the TCAD simulations indicate that during the oscillations, the instantaneous input capacitance behaves as a time-varying element. Its value varies according to the electric field strength at the surface of the IGBT. Based on this observation, the non-linear capacitance together with a resonant circuit, in this case the external gate stray inductance L_g, gives rise to diverging oscillations. The circuit oscillates not because the IGBT cell is behaving as an amplifier but because there is a part of the system whose parameters are changing periodically, in our case, it is the gate capacitance. This type of behavior has been studied in the literature and commonly known as a parametric oscillation; one example is the operating principle of a varactor parametric oscillator whose non-linear variable capacitor element is used to amplify [12].

A PSpice simulation is built to validate the hypothesis, whose schematic circuit is represented in Fig. 10a. The circuit represents the gate loop circuit consisting of a gate inductance, whose value is the one selected for the TCAD simulations (40 nH), a small resistor to simulate circuit losses, and two capacitors which are switched alternatively, whose values have been selected in agreement with the highest and lowest input capacitance value in Fig. 6.

The capacitance value in the PSpice simulation is switched according to the observation made in Fig. 6, where the highest value is observed when V_{GE} is above 15 V, while the lowest capacitance value is observed when V_{GE} is below 15 V:

$$C(t) = \begin{cases} C_1 + C_2 \; if \; V_{GE} > 15\,V \\ C_2 \; if \; V_{GE} < 15\,V \end{cases}$$

where C_2 is the low-concentration capacitance, and C_1 is the variation in case of high capacitance. The simulation results in Fig. 10b show a non-linear oscillation with increasing amplitude. This validates the hypothesis that a time-varying capacitance coupled with an inductance in series gives rise to oscillations. The oscillation frequency in the PSpice simulation is lower than the observed with the TCAD simulations. This indicates that the capacitance value must be smaller than the calculated one.

When V_{GE} is above 15 V, the transition from low to high capacitance is done while the energy is being transferred from the capacitance to the inductance. As a consequence, the *dv/dt* slows down because of the larger capacitance, in agreement with the results from the TCAD simulations. When V_{GE} is below 15 V, the capacitance is switched to a small value, while the energy is transferred from the inductance to the capacitance. The voltage increases its amplitude because a higher energy has to be stored in a smaller capacitance. This mechanism coincides with the operating principle of a parametric oscillator, where the capacitance is the active element changing its value every half cycle.

5. Conclusions

A detailed study of the short-circuit oscillation phenomenon in planar IGBTs is presented. The

analysis has demonstrated that the primary cause for the excess electron density at the surface of the IGBT, is the weak electric field in this region – this explains why oscillations are mainly observed at low collector voltages. In short circuit, the injected electrons become dominant over the sum of holes and the background doping, which in turn causes the effective charge to become negative. The result is that the electric field's peak moves to the collector, which makes it even weaker at the surface. During the oscillations, the electric field across the n-base is continuously changing from the emitter to the collector side coinciding with a high capacitance value when the electric field peak is located at the collector and with a low capacitance value when the electric field peaks at the emitter. Here, we can understand how to relate the field distortions to capacitance variations; and associate the capacitance variation with charge-storage effects occurring at the surface of the IGBT.

As a major achievement of this work, it has been pointed out that a parametric oscillation takes place, whose time-varying element is the Miller capacitance, leading to an amplification mechanism. To validate the hypothesis, the amplification has been modelled in PSpice. Finally, it can be concluded that oscillations can be mitigated by increasing the electric field at the emitter, as demonstrated with simulations and experiments at high V_{CE}.

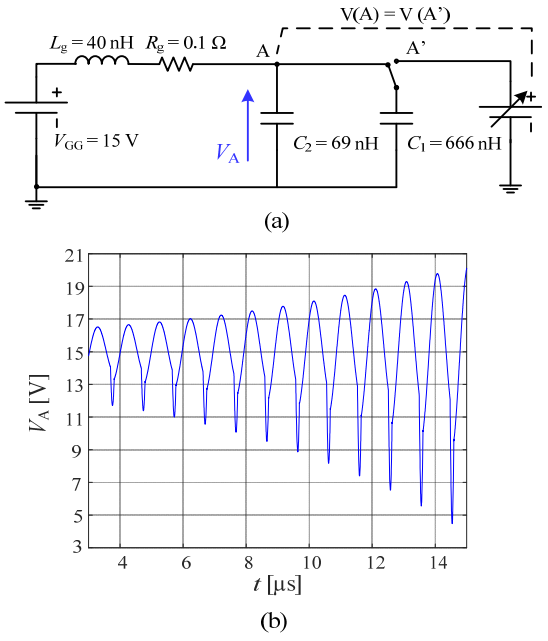

Fig. 10. PSpice simulation using switched capacitors to model the IGBT short-circuit oscillations: (a) circuit, and (b) simulation results.

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