A MULTIPROJECT CHIP APPROACH TO THE TEACHING OF ANALOG MOS LSI AND VLSI

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Abstract

Multiproject chip implementation has been used in teaching analog MOS circuit design. After having worked with computer simulation and layout aids in homework problems, students designed novel circuits including several high performance op amps, an A/D converter, a switched capacitor filter, a 1 K dynamic RAM, and a variety of less conventional MOS circuits such as a V/I converter, an AC/DC converter, an AM radio receiver, a digitally-controlled analog signal processor, and on-chip circuitry for measuring transistor capacitances. These circuits were laid out as part of an NMOS multiproject chip. Several of the designs exhibit a considerable degree of innovation; fabrication pending, computer simulation shows that some may be pushing the state of the art. Several designs are of interest to digital designers; in fact, the course has provided knowledge and technique needed for detailed digital circuit design at the gate level.

1.   INTRODUCTION

During the last few years the development of MOS IC design has advanced in two fronts. On one hand improvements in fabrication have made possible the implementation of LSI and VLSI digital systems. On the other hand, introduction of analog MOS circuit techniques has made possible single chip integration of high performance analog and analog/digital circuits (1) such as A/D and D/A converters, PCM encoders and decoders and a variety of other telecommunication systems, switched capacitor filters, microcomputers with analog interfaces, several special purpose signal processors, and high performance operational amplifiers.

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Courses and research projects in digital LSI and VLSI have been initiated in many universities. A particularly successful teaching and research vehicle is the incorporation of a number of diverse design projects on a single chip. This economical and speedy realization of new circuits and the associated design methodology have come to be called the "multiproject chip" approach (2,3). This approach has proven its value in the classroom by allowing students to be exposed to all aspects of integrated circuit design, layout and experimental evaluation of their projects. This paper describes the use of the multiproject chip approach in the teaching of a one-semester course on analog MOS circuit design, offered at MIT during the fall of 1980, with very encouraging results. The course has evolved from a similar course, taught over the last few years at Columbia University, which included the design project but not the multiproject chip implementation.

2.   COURSE OUTLINE

The course to be described is at the senior/graduate level. The assumed background is a one year junior electronics sequence (in the first offering at MIT it happened that most students in the class were graduate). No background in MOS devices and circuits is assumed. A list of the major topics covered follows:

    Semiempirical MOS transistor model
    Fabrication and computer aided layout
    Basic circuit building blocks
    Computer aided circuit analysis
    Operational amplifiers
    Large signal consideration (transient response and distortion)
    Noise
    Voltage reference sources
    Comparators
    A/D and D/A converters, PCM encoders and decoders
    Switched capacitor filters
    Detailed device physics and higher order models

The topics have been selected so as to give working knowledge for the design of high performance analog MOS circuits; in fact the design and layout of such circuits is a required project in the course. The particular order in which the topics are persented is chosen in order to allow an early start of the design project which has to meet specific deadlines associated with the multiproject chip implementation. This makes it necessary to begin the course with the presentation of a semiempirical device model which has to be taken temporarily for granted; enough plausibility arguments are presented so that the model "makes sense", and students are promised a detailed derivation from physical principles in the last part of the course. Judging from student responses to a questionnaire, this does not cause problems. Both NMOS and CMOS circuits are covered.

The standard square law equations, used for strong inversion in hand analysis of digital circuits, are often inadequate for analog design especially when the substrate doping is relatively high. A more accurate, yet simple, set of equations (4) used in the course appears in Fig. 1 (this model is modified for short channel devices to include channel length modulation).
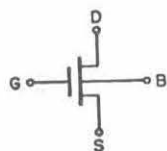
$$I_D = K \left[2(V_{GS}-V_T)V_{DS} - (1+\delta)V_{DS}^2 \right], \quad V_{DS} \geq \frac{V_{GS}-V_T}{1+\delta}$$

$$= \frac{K}{1+\delta}(V_{GS}-V_T)^2 \qquad\qquad , \quad V_{DS} \leq \frac{V_{GS}-V_T}{1+\delta}$$

$$K = K'\left(\frac{W}{L}\right)$$

$$V_T = V_{To} + \gamma\left(\sqrt{V_{SB}+\phi_B} - \sqrt{\phi_B}\right)$$

FIGURE 1   Semiempirical DC model for long channel devices.

K' is a process dependent parameter and δ is a parameter which depends on substrate doping and substrate bias. However, the quantity $1+\delta$ is only weakly dependent on substrate bias and to first order can be considered constant for a given device. Both K' and $1+\delta$ are empirically determined by fitting experimental I-V curves. The parameters V_{TO}, γ and ϕ_B in the threshold voltage expression are also empirically determined. A small signal equivalent circuit is derived from the above set of DC equations; when intrinsic device capacitances and the drain small signal conductance are added to it, the circuit of Fig. 2 is obtained (5,6,7). Junction and overlap capacitances are easily added to this model. The above models represent good compromises between accuracy and simplicity for hand analysis. Students are made aware of higher order models, but a detailed discussion of these is postponed until the last part of the course.

$$\frac{g_{mb}}{g_m} = \frac{C_{bs}}{C_{gs}} = \frac{C_{bd}}{C_{gd}} = b = \frac{\gamma}{2\sqrt{V_{SB} + \phi_B}}$$
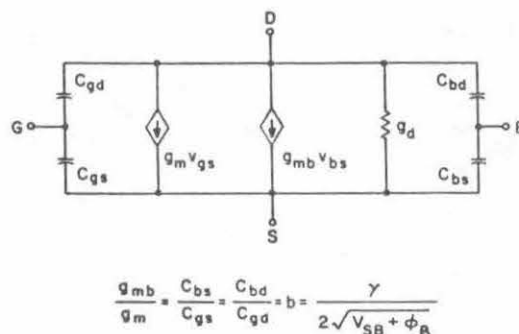
FIGURE 2   Small-signal model.

Both computer aided layout and circuit analysis are taught in conjunction with homework problems at which students are exposed early to the use of computer aids; in our case the programs AIDS (8) and SPICE (9) were used on a DEC-20/60 computer.

Basic circuit building blocks are presented at a great level of detail. Bias, low frequency small signal operation and high frequency considerations

are discussed for inverters (CMOS, depletion load NMOS and enhancement mode NMOS), source followers, differential stages, cascode stages, current sources and level shifters. The knowledge thus gained is used to discuss more complex circuit blocks. The students are at this point ready for a detailed exposure to various operational amplifier configurations; bias and small signal calculations for working operational amplifiers are treated at length. High frequency considerations and frequency compensation are emphasized. At about this point students start their project work; details are given in Section 3.

The lectures continue with the topics of transient response, distortion and noise. The approach used for noise analysis is that of Ref. (10). Voltage reference sources, comparators, A/D and D/A converters, and PCM codecs are then discussed and examples of working designs from the literature are analyzed. The emphasis in the treatment of switched capacitor circuits is on basic principles. Exact analysis is taught using the intuitively appealing concept of charge conservation within closed surfaces not crossed by conductors (11). No matrix analysis is used. The students are cautioned against carelessly using resistive equivalents of switched capacitors and illustrative examples of misuse of such equivalents are presented. Although several working filter designs are discussed, not much time is devoted to the synthesis of such circuits as it is felt that this topic is better left to a course on network synthesis.

The final topic discussed in the course is that of MOS transistor physics and models. Potentials within the semiconductor instead of energy bands are used in such a way that rigor is not compromised. Both the semiempirical model discussed above, and more accurate models are derived from first principles. Small geometry and high order effects are discussed and general capacitance and charge models are introduced.

In the MIT offering weekly homework assignments were given during the first part of the course; later these were gradually phased out to allow more time for work on the design project. A total of 8 assignments were given during the semester. Student performance was judged from the design project,

homework and personal interaction with the instructor. No midterm or final examination were given. Previous offerings of this course at Columbia University have included such examinations.

3.   THE DESIGN PROJECT

Independently of whether it is finally realized on silicon, the design project provides the student with an opportunity to pull together what he has learned on circuit design. Realization of the circuit as part of the multiproject chip offers the additional opportunity to go through the remaining steps typical in an industrial environment, these being layout and final evaluation in the lab; it also serves as an important booster to student motivation. Because it is impossible to have the chips fabricated before the end of the semester, the evaluation in the lab cannot be a required part of the course; however, experience with other courses involving a multiproject chip has shown that the majority of the students return the following semester, on their own initiative, to evaluate their circuits.

The implementation of the MIT multiproject chip is managed by MOSIS at the University of Southern California; the chip is to be fabricated by the Integrated Circuits Laboratory, Hewlett Packard, Inc., Palo Alto. A NMOS enhancement-depletion single-level polysilicon process is to be used, with nominal substrate doping of 6×10^{14} cm^{-3}. The nominal threshold voltages at 0 substrate bias are +1 V and −4 V for the enhancement and depletion transistors, respectively. The layout rules followed are those in reference (2), with $\lambda = 2.5$ μm. Minimum channel dimension for the projects was set at 3λ, as opposed to 2λ used in digital projects, to avoid modeling inadequacies at short and narrow channels. This was necessary because of lack of appropriate test transistors for detailed characterization. Polysilicon-to-depletion implant capacitors are used as the above process does not permit the implementation of higher quality structures. More appropriate processes for the purposes of this course are double-level polysilicon NMOS or CMOS, or at least a modified single-level polysilicon process that would allow the fabrication of reasonable value high quality capacitors between metal and polysilicon; although of lower performance, metal-gate processes can also be used.

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After the first third of the semester students were asked to submit a brief proposal outlining the design project they intended to work on. A high performance operational amplifier was suggested as a possible project by the instructor, and a set of state-of-the-art specifications that had to be met or exceeded was given. Minimization of power consumption was emphasized as one of the most important design goals. Recently designed high-performance operational amplifiers in the industry were claimed to have a power dissipation of only 0.75 mW, so this was set as a specification to be bettered. The students were asked to work in groups of two or more in order to reduce their work load, facilitate supervision and avoid overloading the computer facilities. All student designs were simulated using the program SPICE. The students were supplied with model parameters, which were derived from the information we had on the process to be used. Unfortunately, no appropriate test devices were available for detailed characterization, so we had to use instead devices integrated using a related process and then extrapolate the results. A further complication arose from the fact that we had no previous experience with the model in the particular version of the program SPICE we used. However, every effort was made to use as reasonable a set of model parameters as possible, and it is hoped that simulation results are a good indication of what will be seen in the laboratory when the fabricated chips are received. The design projects undertaken by the various groups are listed below:

Low power enhancement/depletion operational amplifier (5 groups)

Low power enhancement-only operational amplifier (3 groups)

High speed operational amplifier

Autozeroing operational amplifier

A/D converter

AC/DC converter

Voltage to current converter

Switched capacitor filter

Digitally programmable analog filter

1 Kbit dynamic RAM

On-chip circuitry for MOS transistor capacitance measurement

AM radio receiver

Some of the student designs will be briefly described below, and representative computer simulation results will be quoted. As can be seen in the list given above, the most popular design project was that of a low-power enhancement-depletion operational amplifier. Five groups have designed such circuits for operation from ±5 V power supplies, with power dissipation ranging from 0.4 mW to 1 mW. Low frequency gains are between 60 dB and 74 dB, and unity gain frequencies after frequency compensation is between 0.65 MHz and 3 MHz. The 1% settling times are between 0.7 μs and 4 μs for a 10 pF load. An example of a student design is shown in Fig. 3. Another design uses an architecture drastically different from that of any NMOS operational amplifier presented to date; the students who designed the circuit have asked us not to present it because they plan to apply for a patent.
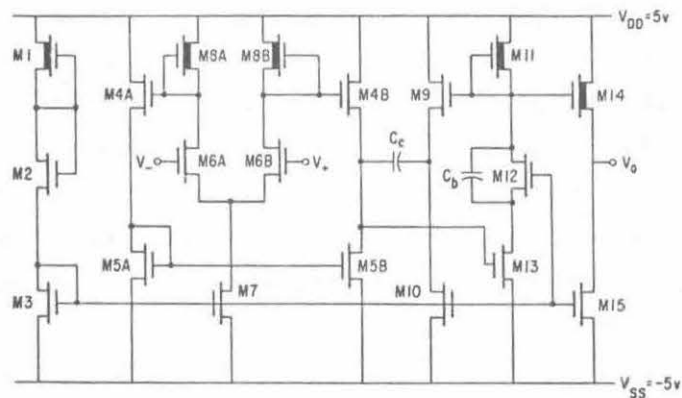

FIGURE 3 A low-power enhancement/depletion operational amplifier (M. Elbuluk and J. Harrison).

One group has decided to meet the challenge of using only enhancement devices in their operational amplifier; they have come up with the circuit of Fig. 4, and a performance certainly impressive for an all-enhancement design: a power dissipation of 0.93 mW, a low-frequency gain of 61 dB, a unity gain frequency of 420 KHz, and a 1% settling time of 2.3 μs with a 10 pF load. The circuit is more process-insensitive and has much lower distortion than most enhancement-depletion operational amplifiers.

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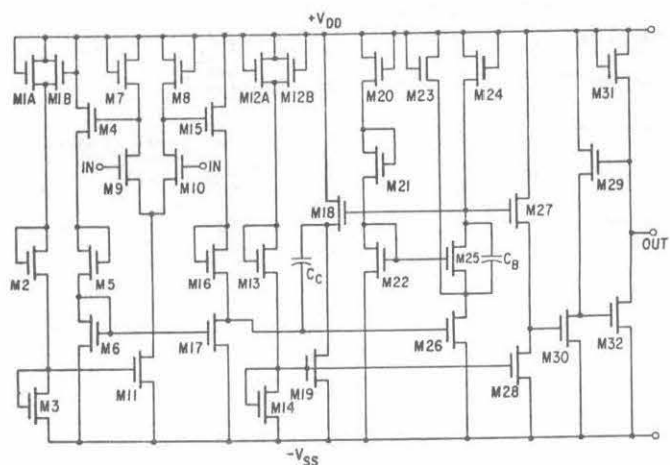Analog MOS LSI and VLSI

FIGURE 4   A low power enhancement-only operational amplifier (C. C.
Cederberg and B. V. Karlsson).

Three groups have designed high speed operational amplifiers. The
simplest and fastest design is shown in Fig. 5; it compromises gain, which is
only 40 dB, for speed. The unity gain frequency is 126 MHz, and the 1%
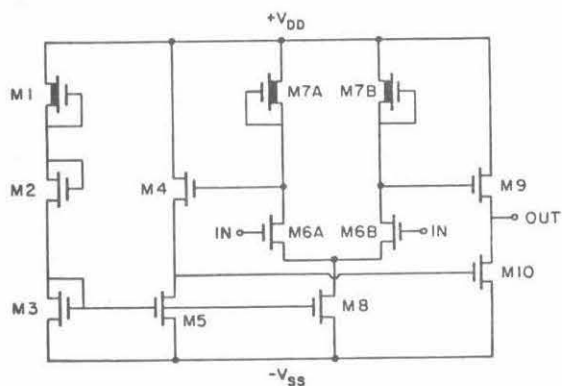settling time is only 24 ns with a 5 pf load charged through a series device.
Power dissipation is 15 mW.

FIGURE 5   A high speed, low gain operational amplifier (C. Christensen and
W. Shiley).

The autozeroing operational amplifier's concept is shown in Fig. 6; the switches are implemented with MOS transistors. The bottom amplifier is used to null alternatively the offset of itself and that of the top amplifier. This avoids the problems of commutated auto-zero designs, where at every commutation the signal output must slew from the offset value to the signal value.
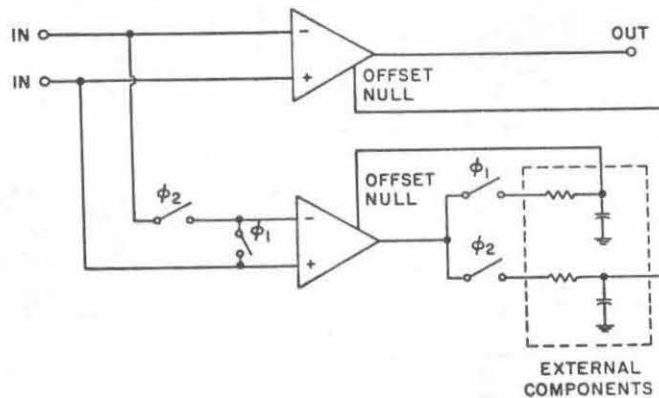

FIGURE 6   An autozeroing operational amplifier (M. Coln).

The A/D converter project employs charge redistribution using three capacitors; the analog part of the design is shown in Fig. 7. It is expected that it will perform an 8-bit conversion in 27 µs.
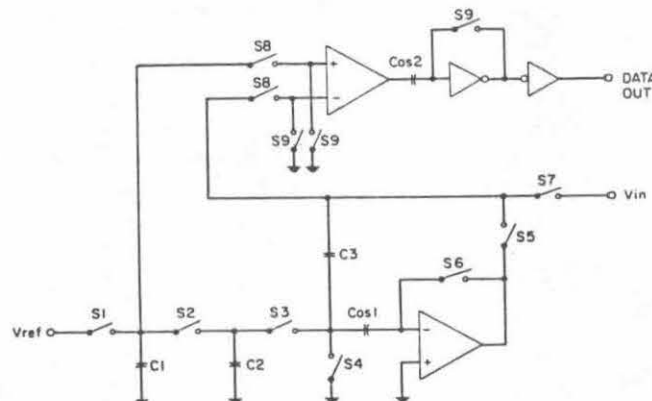

FIGURE 7   An 8-bit, successive approximation A/D converter (S. McCormick and A. Garcia).

The AC/DC converter design (Fig. 8) is aimed at instrumentation applications. It uses a zero-crossing detector which activates a switch allowing only the negative half-cycles to pass; a polysilicon resistor is used as part of the following filter. A switched capacitor amplifier is used to scale the DC output.
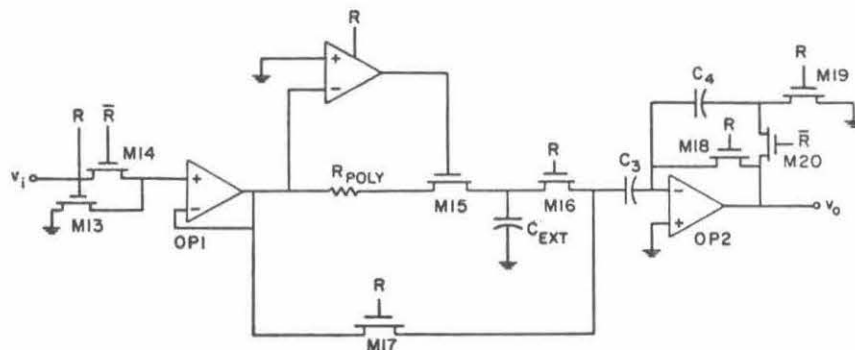

FIGURE 8   An AC/DC converter (D. K. Oka and S. Fiedler).

Another project aimed at instrumentation applications is the voltage-to-current converter of Fig. 9. One of the uses of this circuit is in developing a temperature-insensitive, supply-insensitive reference current from an existing reference voltage. The output current is produced from an internal reference current through a mirror circuit. Internal feedback circuitry adjusts the reference current until it charges a capacitor to a voltage equal to the voltage applied externally, in a specific amount of time determined by an external clock.
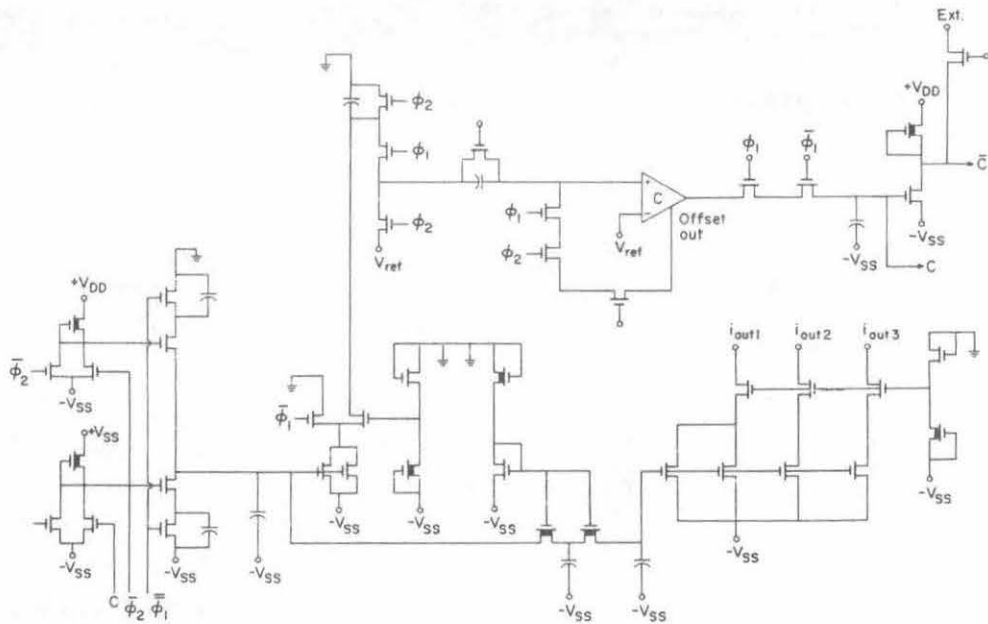
FIGURE 9   A voltage-to-current converter (M. M. Colavita and F. L. Terry,
             Jr.).

One project dealt with the design of the switched capacitor biquadratic
notch filter shown in Fig. 10; the topology is that reported in (12). This
design has been adjusted for minimum capacitance spread and minimum total
capacitance. A very good operational amplifier was part of the design; in
fact many of the "non-op amp" projects actually contained good operational
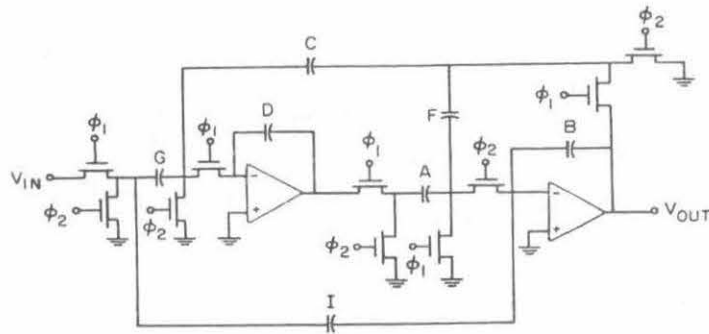amplifiers.

FIGURE 10   A switched capacitor biquad notch filter (M. M. DeSmith and D. W.
             Duehren).

The digitally programmable analog filter project undertaken by C. W.
Mangelsdorf and A. L. Robinson uses pulse width control to adjust the
transfer function coefficients; the value of these coefficients depends only
on timing and is independent of element values or even element value ratios
for some configurations (13). The circuit is laid out in such a way that both
transversal and recursive filters can be implemented. The design includes
many sample-and-hold circuits, which share two operational amplifiers using
the technique described in (14).

A good example of the extensive analog design involved in realizing
digital circuits at the gate level is a dynamic RAM; one of the projects was
the design of a one-transistor-cell, 1 Kbit dynamic RAM including sense
amplifiers, word line driver and column decoder. Its density is comparable to
that of INTEL 2104. According to the students, one of the most challenging
parts was the high voltage driver, shown in Fig. 11.
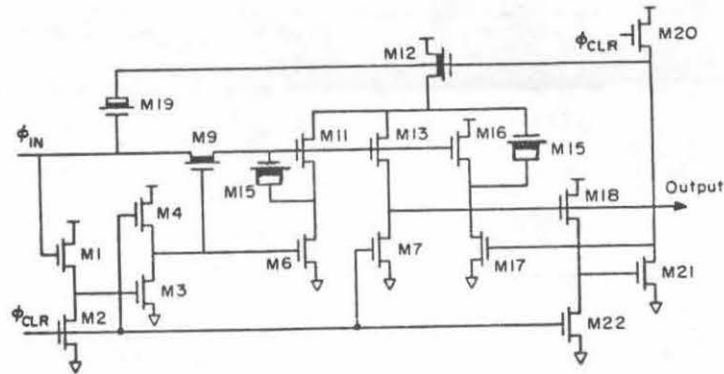
FIGURE 11   High voltage driver of a   1 Kbit dynamic RAM (J. J.   Cherry and G.
            L. Roylance).

     One of the most unconventional   projects undertaken was an inductorless,
one-chip AM radio receiver using superheterodyne   circuitry by S.   L.
Garverick, T. E. Haferd, and R. B. Iverson.   Both the RF input stage and the
local oscillator are voltage controlled. The IF stage   consists of a   cascade
of active non-switched filters. The detector   uses a scheme similar to the one
described above for the AC/DC converter project. AGC circuitry is included.
Although, in the authors' opinion, it is unlikely that the radio circuit will
work as a whole, parts of it probably will; given the short amount of time in
..hich the project had to be completed, this will   still   be satisfactory.
Problems expected include the generation of spurious components in the input
circuitry, and component mismatches in the IF stage.

     In their layout work students were careful to conserve chip area;   an
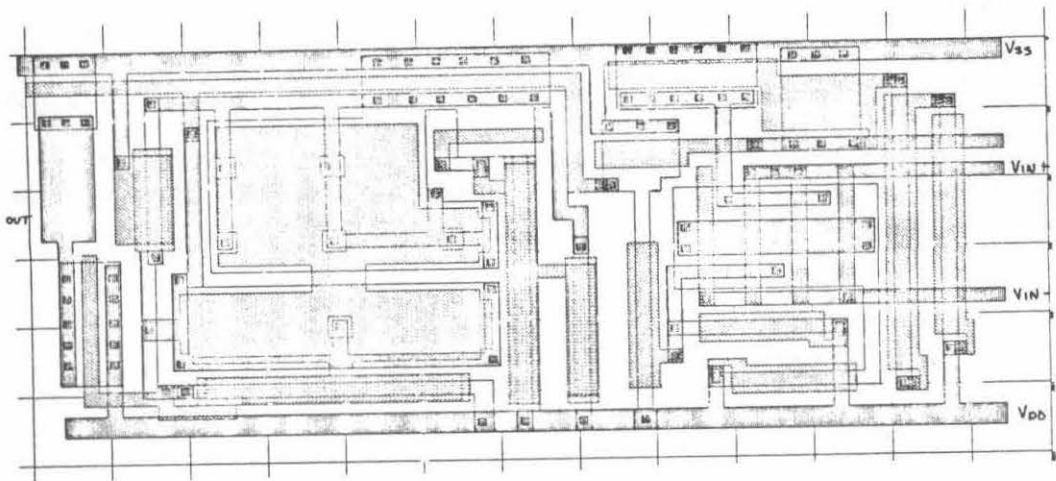example of an operational amplifier layout is shown in Fig. 12.

FIGURE 12   Layout of an operational amplifier (D. Goddeau and M. Johnson).

Student time spent on project work was a large part of the total time spent on the course; answers to a questionnaire distributed in class show that the average time spent for the course per week was 15 hours. We are looking for ways to decrease this time in future offerings, without subtracting significantly from the value of the course.

4.   CONCLUSIONS

A one-semester course on analog MOS design has been taught several times at Columbia University and recently at MIT. The course covers topics from device physics and models to detailed circuit and layout, and one of its important parts is a state-of-the-art design project in which students put together what they have learned in the lectures. In the last offering of the course (MIT), the emphasis on the project was increased; student designs will be implemented as part of a multiproject chip. Computer simulation results show that many designs are of excellent quality and are innovative; some may be pushing the state-of-the-art. Several designs are of interest to digital designers; in fact, the course has provided knowlege and technique needed for detailed digital circuit design at the gate level.

5.   ACKNOWLEDGEMENTS

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