DEVICE AND CIRCUIT DESIGN FOR VLSI

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ABSTRACT

A review of the device and circuit design complexity and limitations for VLSI is presented. VLSI device performance will be limited by second order device effects, interconnection line delay and current density and chip power dissipation. The complexity of VLSI circuit design will require hierarchial structured design methodology with special consideration of testability and more emphasis on redundancy. New organizations of logic function architectures and smart memories will evolve to take advantage of the topological properties of the VLSI silicon technology.

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I. INTRODUCTION:

As semiconductor technology has evolved from discrete to small-scale to medium-scale and through large-scale integration levels a rapid decrease in the cost per function provided by the technology have opened up new applications and industries. Today there is a large interest in the next phase of integration: very large scale integration (VLSI). The semiconductor technology will be able to fabricate chips with more than 100K devices [(1)] in the 1980's. The continuous scaling of the semiconductor devices and increase in components counts on a single chip is resulting in more complex technology developments, device and circuit designs and product definition. In this review paper, projections of how device technology will evolve in the future and the problems and limitations of device and circuit design for VLSI are presented.

VLSI TECHNOLOGIES:

In Fig. 1 a summary of the performance of the major technologies available today for LSI's is illustrated (2,3). For bipolar devices two families: the Emitter-Coupled logic (ECL) and Integrated Injection logic (T^2L) are plotted. For MOS devices the NMOS, CMOS and SOS technologies are shown. The performance of GaAs MESFET and silicon MOSFET logic are also plotted for comparison although those devices are not presently used for LSI. The speed of the bipolar and MOS logic families are limited by the transit time of the carriers across the active region of the devices (the base for the bipolar transistor and the gate for the MOS transistor), the gate configuration of the logic family (for example enhancement load, depletion load or CMOS) and the parasitic and interconnect capacitances of

the technologies. Presently bipolar devices with a base width of a few tenths of a micron have gate delay of about few hundred picosecond and a speed power product of about 10 picojoule. The I^2L family has a speed power product of few picojoules and a few nanoseconds gate delay. NMOS devices are presently fabricated with a channel length of two microns (4) providing gate delay of about 1 nsec and speed power product of 1 PJoule. CMOS logic with the same channel length as NMOS has about the same gate delay but dissipates less power. The CMOS power dissipation depends on the duty ratio. SOS with its lower parasitic capacitances has about half the speed-power product of CMOS. MESFET devices with about 1 pm gate length have gate delays of about 100 Psec and speed-power products 10 - 100 Femto-joules. As the average feature size decreases with technology evolution, the performance of all these technologies will improve.

The dimensions of the present NMOS and the smallest conceivable future MOS transistors (5) are shown in Fig. 2. Presently MOS devices have an oxide thinkness of 700 Å and an electrical channel length of 2μm. Operating from a 5V supply, they provide a gate delay of 1 nanosecond and a speed power product of 1 picojoule.* The smallest conceivable NMOS transistor is projected to have an oxide thickness of about 70 angstrom (limited by tunneling considerations) a channel length of 0.2μm (limitied by punch-thru effects and substrate doping fluctutations). It will operate from a power supply of 0.5V (≈20 KT/e) which is the minimum gate voltage swing required to change the device current by several orders of magnitudes.

*The gate delay and speed-power product $P.\tau_d$ of the MOS technology are given by the following relations:

$$\tau_d = F_1 \cdot \tau F \ , \quad P \cdot \tau_d = F_2 \cdot (\tfrac{1}{2} C_G V^2)$$

where τ_f is the time of flight or transit time of the carriers across gate of the MOS transistor, F_1 and F_2 are factors which depend on the gate configuration, fanout and parasitic capacitances, C_G the intrinsic gate capatance and V the voltage swing. In the depletion load NMOS technology $F_1 \approx F_2 \approx 50\text{-}70$ for a fanout of 3.

This device will provide a gate delay of few tens of picoseconds and a speed power product of few femtojoules. At these small dimensions, the MESFET technology may replace the MOSFET technology as it eliminates the gate oxide reliability problems and improves the threshold voltage control. (6) The base width of the smallest size bipolar device is about 500-700 angstrom (limited by punch-thru effects and doping fluctuations). When the electron transit time across the gate of the MOS transistor becomes comparable to the transit time across the base of the bipolar transistor, both devices will intrinsically provide same current drive and speed performance. The performance difference between the two devices will result from the logic configuration and the parasitic and interconnect capacitances of their technologies.

In Fig. 3, the past and expected future trend of the average feature size is illustrated. The average design rule started at 25μm in the early 60's. It has been decreasing at 11% per year and is presently about 3μm. With a projected average design rule of 0.3μm by late 1990's the device density will be of the order of $10^7/cm^2$. Improvements in the average feature size are achieved by improvements in lithography and pattern etching

technologies. In the 60's, contact printing lithography and negative resist wet etching were used. In the 70's conversion to projection printing with positive resist and plasma etching were made for higher masking yield and better resolution of the etching profiles. For 2μm average feature size in the early 80's - projection step and repeat lithography will be required. (8) For feature size below 1μm projected in the late 80's conversion to x-ray step and repeat lithography or electron beam direct writing lithography[8] and reactive ion etching may be needed. The development and capital costs of these lithography and pattern etching technologies are quite enormous. For example in the 60's the costs of a Casper-contact aligner and a wet etching station were about 20K $ and 4K $ respectively. In the mid-70's a Perkin Elmer projection aligner costs about 150K$ and a barrel plasma reactor costs about 40-50K$. A projection step and repeat aligner costs about 500K$. The cost of an x-ray step and repeat electron beam direct writing system may exceed $1 million. Also considerable efforts have to be made to reduce the average defect density as the feature size decreases. In Fig. (4) the past and expected future trend of the chip area for equal production cost is shown. In the past the chip area has been increasing at a rate of about 20% per year, because of the increase in the wafer size from 2" to 3" and the reduction in the average defect density. These were achieved by improving the quality of the masks and the materials, and using cleaner rooms. At this rate the chip area will increase to about few hundred thousand mils in the late 80's.

VLSI MOS DEVICE DESIGN

The improvements in the device parameters of MOS devices by scaling their dimensions (9) are given in Table I. Scaling of device dimensions by a factor

S at constant field to maintain the material reliability results in substantial improvements in the gate delay and speed-power product (energy per switching operation). However the delay required to drive an external capacitance does not scale as favorable as the intrinsic gate delay because of the larger number of stages required to buffer the signal.[10] Note that the power dissipation per unit area remains constant. Thus the power dissipation of logic chips will increase with the chip area which creates difficulties in heat removal from packages. In order to limit the logic chips power dissipation, either the speed or the chip area will have to be reduced. Therefore the power dissipation limitation with scaling will make technologies with lower intrisic power dissipations, such as CMOS and SOS, more attractive.

It has been verified that with the appropriate scaling of the MOS transistor parameters, its characteristics scale as predicted.[9] However, not all device parameters can be scaled proportionally due to practical technological constraints. With selective scaling of few device parameters second order device effects dominate the device characteristics as its dimensions reach its physical limits. In Fig.(5) and (6) the strong dependence of the gate voltage threshold and drain punchthrough voltage on the device dimensions and doping profile in the channel and isolation regions are due to the three dimensional field distribution in the device. Accurate device models have to be used for proper device design for VLSI.[11,12]
The past and expected future trends of the NMOS technology gate delay and speed-power product are illustrated in Fig. (7) and (8). The gate delay has been decreasing very rapidly from 80nsec with p channel metal gate technology in the late 60's to 1nsec with scaled n channel silicon gate depletion load technology[4] in 1978. The improvement in gate delay has been

achieved with technology and circuit innovations such as silicon gate, n channel, depletion loads, and reduced parasitic capacitances. The gate delay is projected to continue to decrease rapidly as more parasitic capacitances are reduced and transistor parameters are scaled. In the 1990's the decrease in gate delay will slow down, due to electron velocity saturation in the channel and limited reduction of residual parasitic capacitances. The lower limit of gate delay of few tens of psec is more than an order of magnitude lower than present technology gate delay. In Fig.(8) the rapid improvement in speed-power product from 500pJ in late 60's to 1pJ in 1978, is attributed to the decrease in gate delays, parasitic capacitances and power supplies. The reduction in speed-power product is projected to continue reaching a lower limit of few Femtojoule with 0.5V supply.

VLSI CIRCUIT DESIGN:

In Table II the interconnect scaling relations are illustrated assuming constant conductor resistivity and equal scaling of all conductor dimensions by a factor S. This results in a response time and voltage drop which do not scale and a conductor current density which increases up with the scaling factor S. Presently current density in aluminum conductors are limited to about 10^5 amps/cm^2 to provide adequate reliability against metal migration. These unfavorable scaling properties of the interconnection lines can be reduced by decreasing the conductor resistivity and thickness scaling and development of better alloys. The difference in the scaling properties of the device and the interconnection lines have profound effects on how devices and circuits designs are going to evolve in the future. The fact that the intrinsic device delay scales favorably with device scaling while interconnection line and external capacitance drive delay do not scale, means that technologies

with lower parasitic capacitance and less current drain, such as CMOS and SOS, will become more attractive. This means also that future designs will take special care to minimize interconnection lines (where substantial portion of the delay and energy will be dissipated) and external drives by proper partitioning between the chips and increasing the level of chip integration. Larger integration results in larger chips. In order to maintain the yield and cost per function, redundancy techniques will have to be used.

Redundancy techniques in memory and logic design will have to be used for VLSI, not only to lower the cost per function but also to take advantage of the improvements in the intrinsic device performance with scaling. Redundancy consists of using spare units to replace defective ones so that larger chips with more function complexity and high rates of faults can be used to achieve lower cost per function, better performance and high reliability. Substantial improvements in yield with redundancy have been reported using existing wafer yield models.(13) Redundancy techniques can be applied at different levels on the system, the wafer or the chip level. In applying redundancy on the system level, the chip profiles are generated and stored in a system directory and the system implements the personalization of the partial chips. Redundancy on the wafer level (wafer scale integration) promises potential improvement in packing density and reliability as the wafer is the final package unit. The implementation of redundancy on the chip and wafer levels involves testing to generate a profile of the nonfunctional areas and personalization to replace the defective areas with functional spare areas. Personalization with non-volatile factory programmable elements (such as laser zapped or fusable links) non-volatile field programmable storage elements (such as MNOS and FAMOS) and on-chip latches have been proposed.

The complexity level of circuit design for VLSI requires a new type of design methodology. Design of logic chips with 100K devices and more takes more than 50 men-years. Management of such complex designs will require coordination between the functional definition, the architectural description, the logic interpretation, the circuit design, the physical layout design, the wafer fabrication and testing with verification and validation at each of these levels. This requires proper partitioning of the design into small blocks and macros of manageable sizes whose design can easily evolve with technology advancement. In order to make the testing of these complex chips feasible, testability have to be designed in by providing means to test inaccessible nodes in the circuits, structuring the design into independently testable blocks and/or incorporating circuits to perform self-checking routines. The implementation of these complex designs will rely on the use of computer aids and interactive graphics for the simulation, design and verification at the different phases of the design.

FUTURE TRENDS

Since the integrated circuit revolution started in the early 60's, the number of components per chip have increased by about five orders of magnitudes.(1) Today memory devices with 64K bits per chip and 16 bit microprocessors with 30K devices per chip are becoming available. Projecting that increase in the future until the devices reach their physical limits indicate that complexity of few hundred million components per chip will be reached by the end of the century. This is more than three orders of magnitude increase in component complexity per chip.

The rate of technology development in the future will be limited by the ability to model, design and fabricate devices with dimensions approaching its physical limits. The interconnection lines delay and current density, the device second order effects and the chip power dissipation will limit the technology performance. Therefore complementary and low parasitic capacitance technologies will become more attractive. It is also quite likely that the MESFET technology will replace the MOSFET technology as device dimensions reach the physical limits due to higher reliability and better threshold voltage stability.

The complex design and product definition in VLSI will limit the component complexity on logic chips. The development of programmable function logic chips, such as microprocessors and control chips, will follow two paths. One path will follow present architecture with more CPU, memory and I/O circuits runnning at a faster rate and a better user interface. By 1990's logic chips of few million gates complexity will run at 100MHz from 0.5V supply dissipating few watts. In the other path, new architectures will be developed to provide better matching between the silicon technology and its topological properties and the function architecture software and human interface. The important topological properties of the VLSI silicon technology are the facts that a substantial part of the delay and energy is dissipated in communication across the interconnection lines and that both memory and logic are built with the same technology.

The memory device design will continue to lead the technology development. Denser memory cells will be made with scaled devices and more complex vertical structures. For optimum speed, signal sensing margins and testing considerations, memories will be organized in blocks with more emphasis on redundancy.

Memory design will also follow two paths. One path will follow present function organization with more memory running at a faster access time and lower power per bit. In the other path new organizations with smarter functions on the chip will be developed.

CONCLUSIONS

VLSI offers tremendous challenges in product definition, circuit design, device modeling and design, technology developments and capital investments. The complexity of product definition will limit the component counts on system function logic chips. The complex circuit designs will require hierarchical structured design methodology with considerations to testability heavy reliance on computer design aids and more emphasis on redundancy. The interconnection line delay and current density, the device second order effects and chip power dissipation will limit the technology performance.

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TABLE I

FET DEVICE SCALING FOR CONSTANT FIELD

DEVICE/CIRCUIT PARAMETRE	SCALING FACTOR
DEVICE DIMENSIONS L, W, T_{OX}	1/S
DOPING CONCENTRATION	S
VOLTAGE	1/S
FIELD	1
CURRENT	1/S
DEVICE EQUIVALENT RESISTANCE	1
GATE DELAY	1/S
EXTERNAL CAPACITANCE DRIVE	1/S.LnS
POWER DISSIPATION/DEVICE	$1/S^2$
POWER DENSITY	1
SPEED POWER PRODUCT/DEVICE	$1/S^3$

TABLE II

INTERCONNECT SCALING RELATIONS

PARAMETRE	SCALING FACTOR
LINE RESISTANCE $R_L = \rho L/Wd$	S
LINE CAPACITANCE $C_L = \epsilon LW/D$	1/S
LINE RESPONSE TIME $R_L C_L$	1
LINE VOLTAGE DROP IR_L	1
LINE CURRENT DENSITY I/Wd	S

FIGURE CAPTIONS

Figure (1) Performance of various technologies in 1978.

Figure (2) The 1978 NMOS transistor and the 1990's smallest size MOS transistor.

Figure (3) Past and projected future trend of average design rule.

Figure (4) Past and projected future trend of MOS LSI die size for equal manufacturing cost.

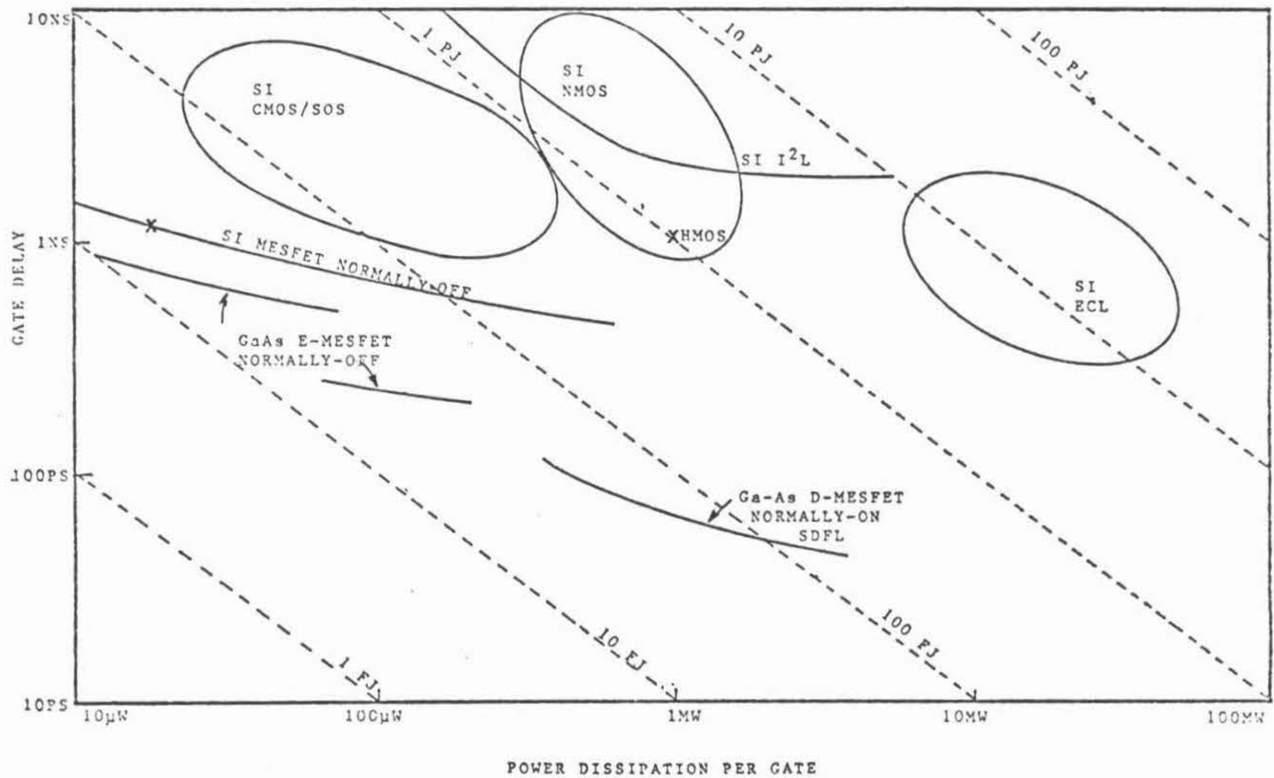
Figure (5) The dependence of gate threshold voltage on the device geometry and doping profile.

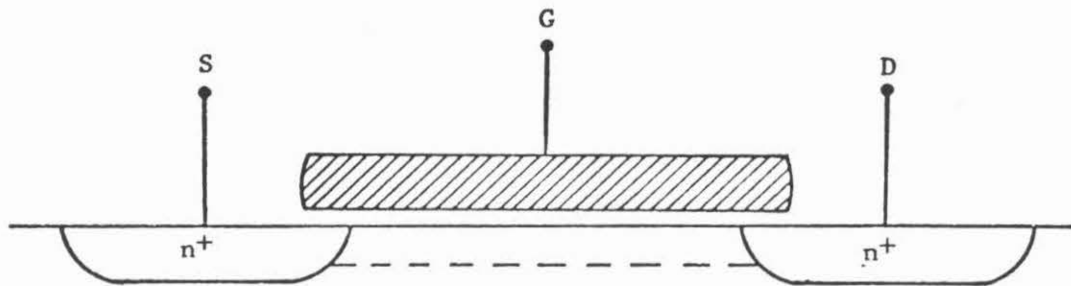
Figure (6) The dependence of drain punchthrough voltage on the device geometry and doping profile.

Figure (7) Past and projected future trend of NMOS technology gate delay.

Figure (8) Past and projected future trend of NMOS technology speed-power product.

SPEED POWER PRODUCT OF VARIOUS TECHNOLOGIES AT 1978

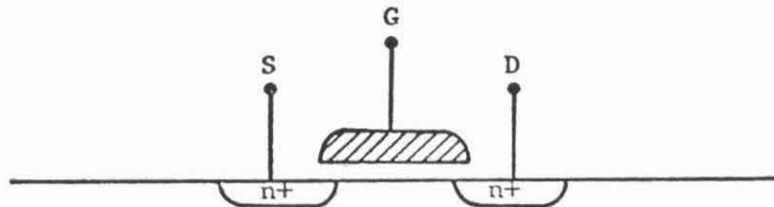




1978 NMOS

L_{CH} = 2μM, T_{OX} = 700A°, X_J = 0.5μM

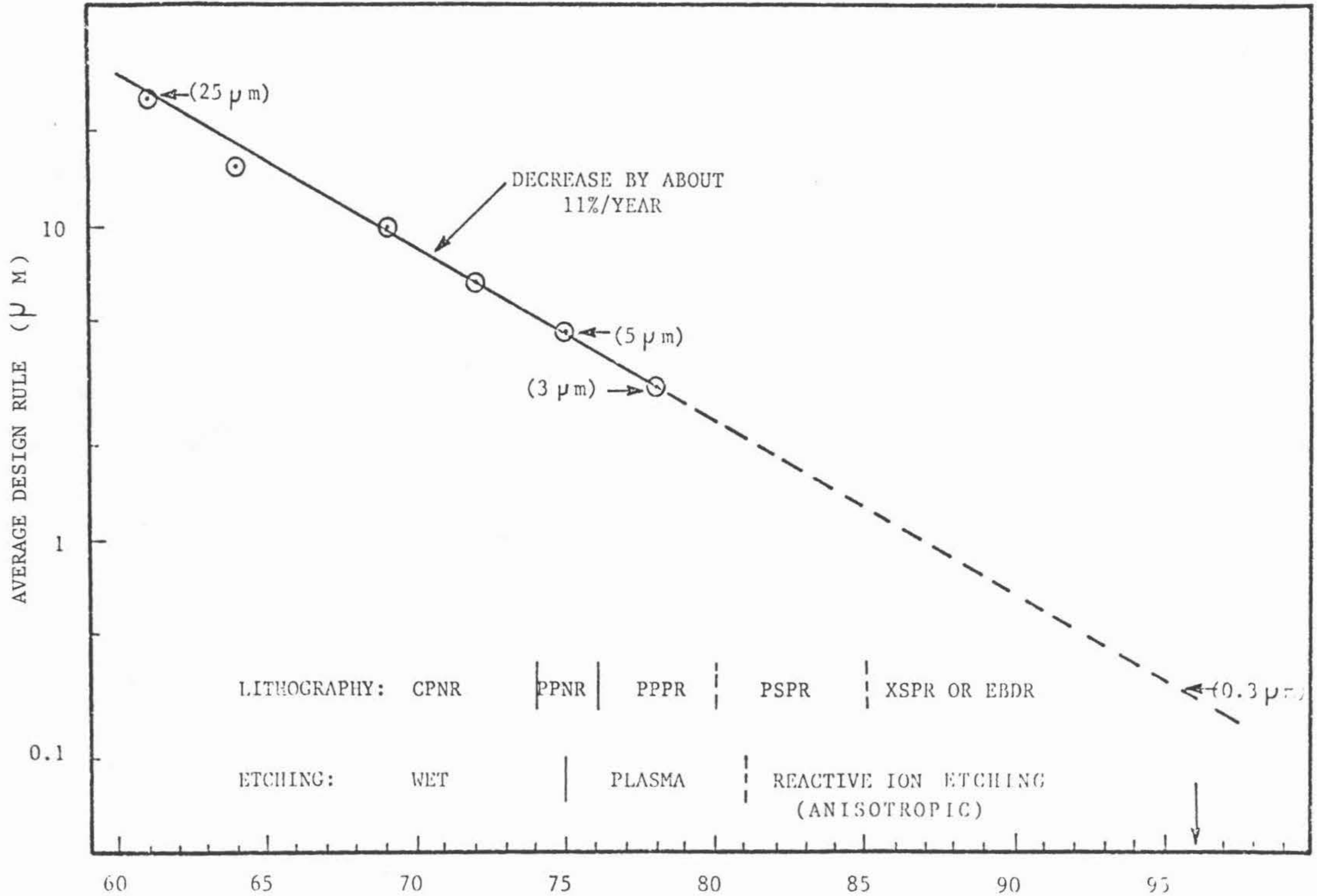
τ_F = 15PSEC, τ_D = 1NSEC, $P\tau_D$ = 1PJ, V_{CC} = 5V

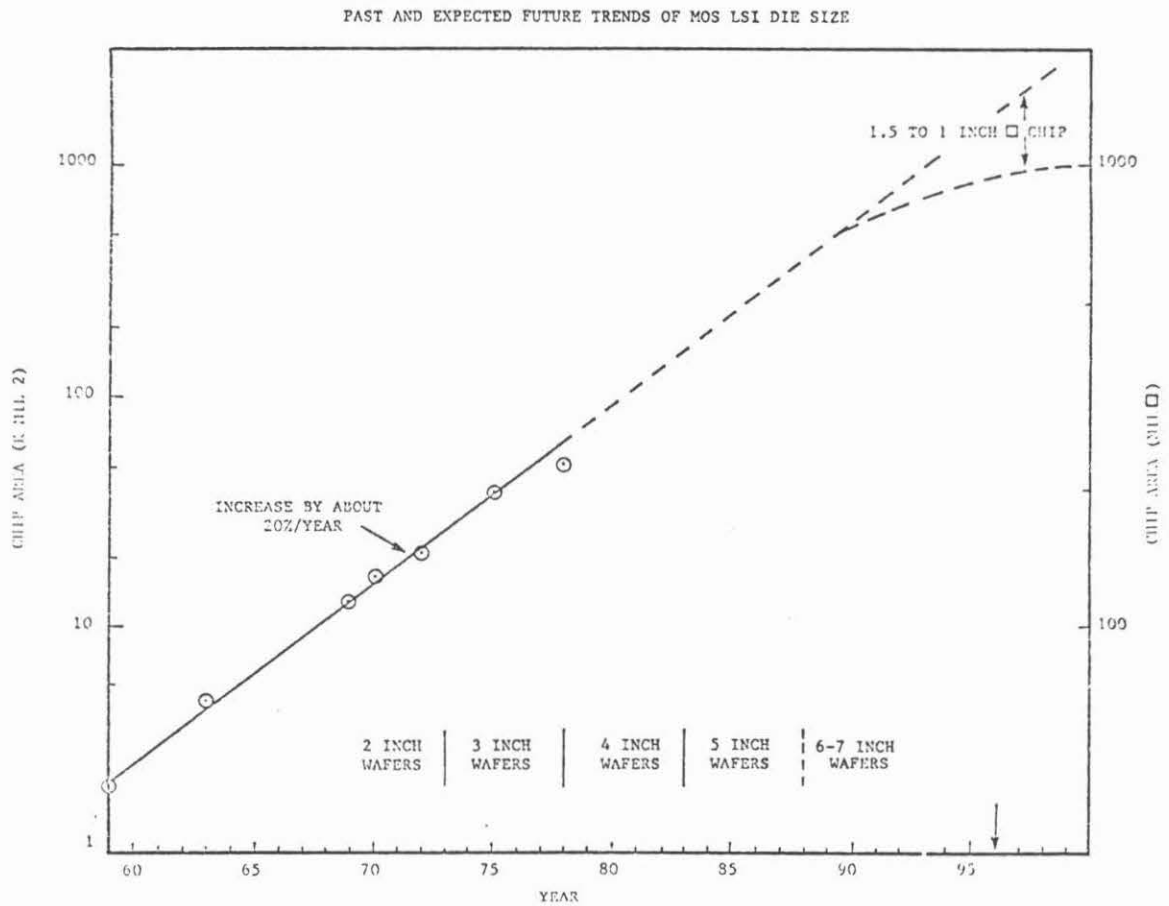


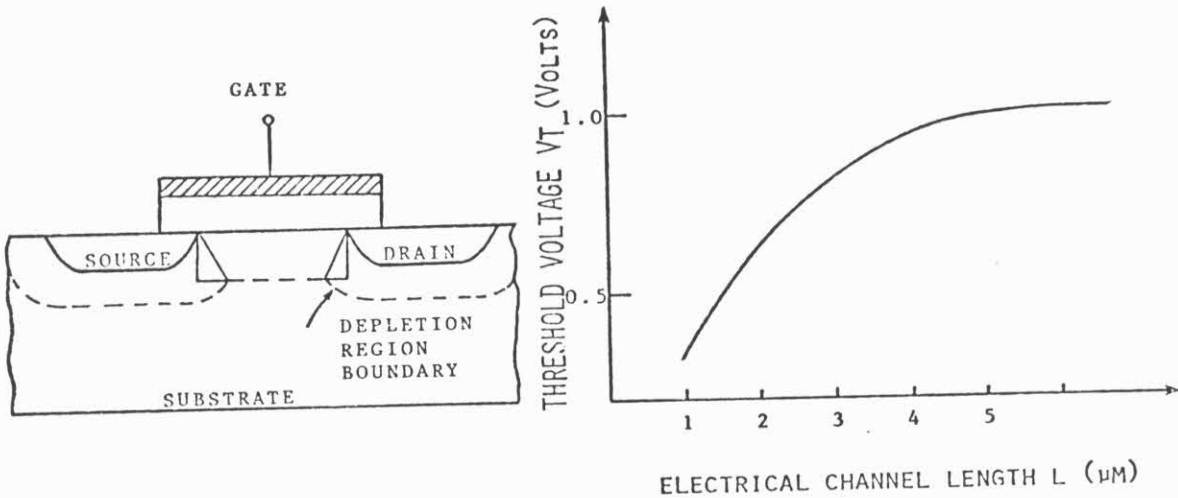
1990's NMOS

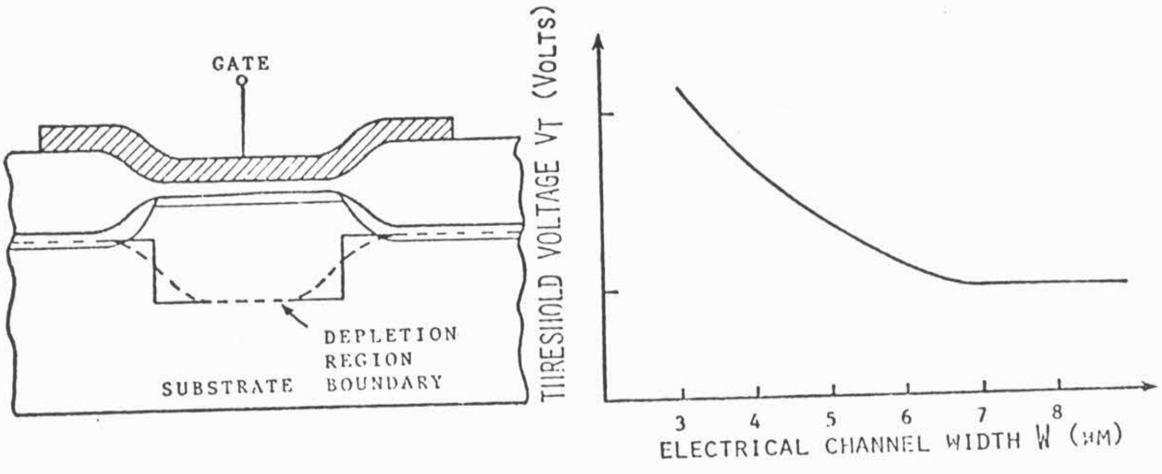
L_{CH} = 0.2μM, T_{OX} = 70A°, X_J = 0.05μM

τ_F = 1 PSEC, τ_D = 50PSEC, $P\tau_D$ = 2FJ, V_{CC} = 0.5V


PAST AND EXPECTED FUTURE TREND OF AVERAGE DESIGN RULE
AVERAGE DESIGN RULE (μM)
10
1
0.1
(25 μm)
DECREASE BY ABOUT 11%/YEAR
(5 μm)
(3 μm)
(0.3 μm)
LITHOGRAPHY: CPNR
PPNR
PPPR
PSPR
XSPR OR EBDR
ETCHING: WET
PLASMA
REACTIVE ION ETCHING (ANISOTROPIC)
60
65
70
75
80
85
90
95


PAST AND EXPECTED FUTURE TRENDS OF MOS LSI DIE SIZE
1000
100
10
1
1000
100
CHIP AREA (K MIL 2)
CHIP AREA (MIL □)
1.5 TO 1 INCH □ CHIP
INCREASE BY ABOUT 20%/YEAR
2 INCH WAFERS
3 INCH WAFERS
4 INCH WAFERS
5 INCH WAFERS
6-7 INCH WAFERS
60
65
70
75
80
85
90
95
YEAR


GATE
SOURCE
DRAIN
DEPLETION
REGION
BOUNDARY
SUBSTRATE
THRESHOLD VOLTAGE VT (VOLTS)
1.0
0.5
1
2
3
4
5
ELECTRICAL CHANNEL LENGTH L (μM)


GATE
DEPLETION
REGION
BOUNDARY
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THRESHOLD VOLTAGE VT (VOLTS)
3
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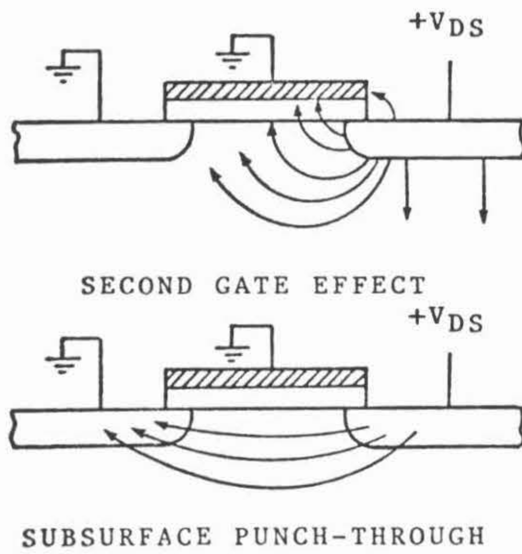
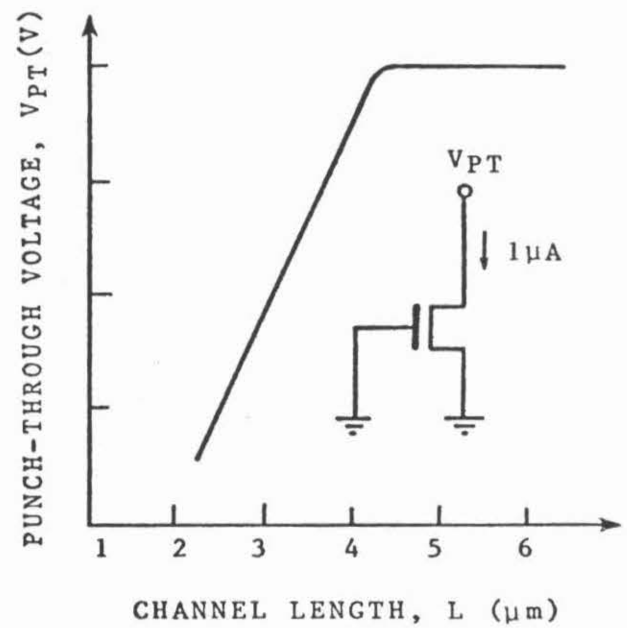
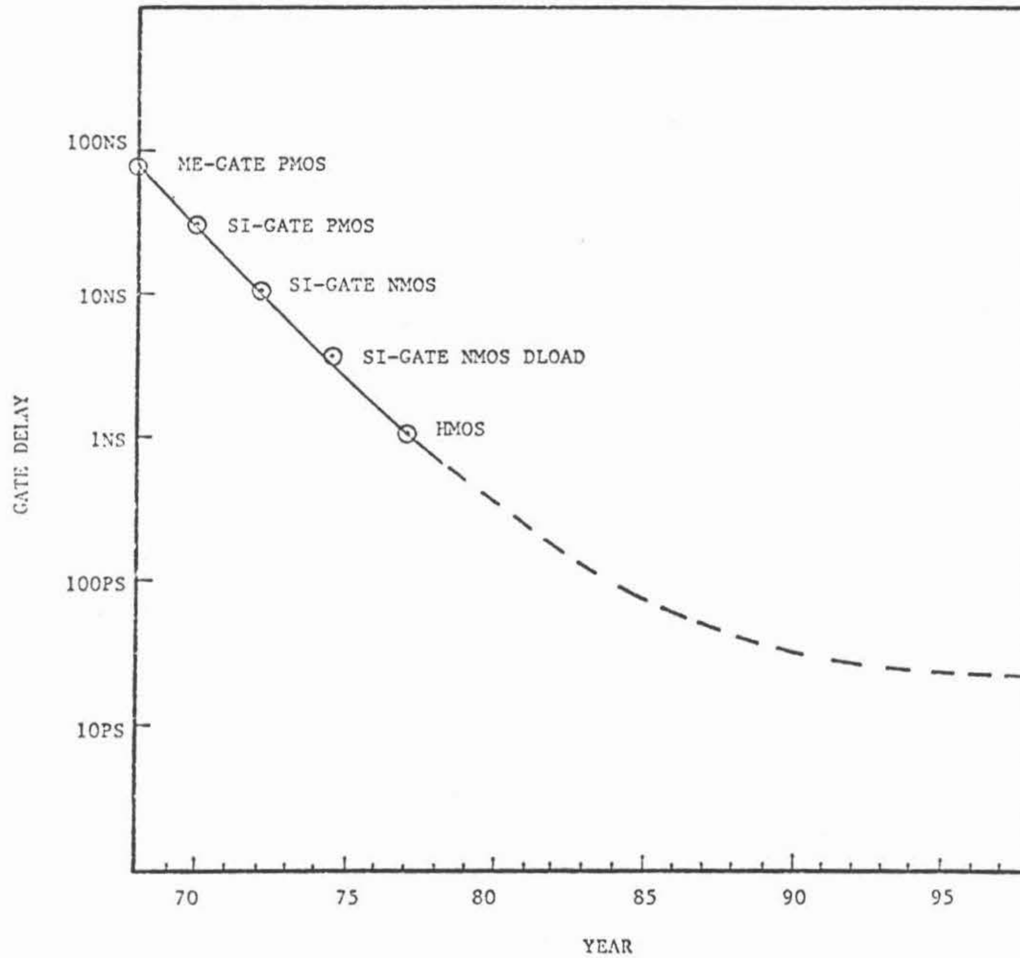
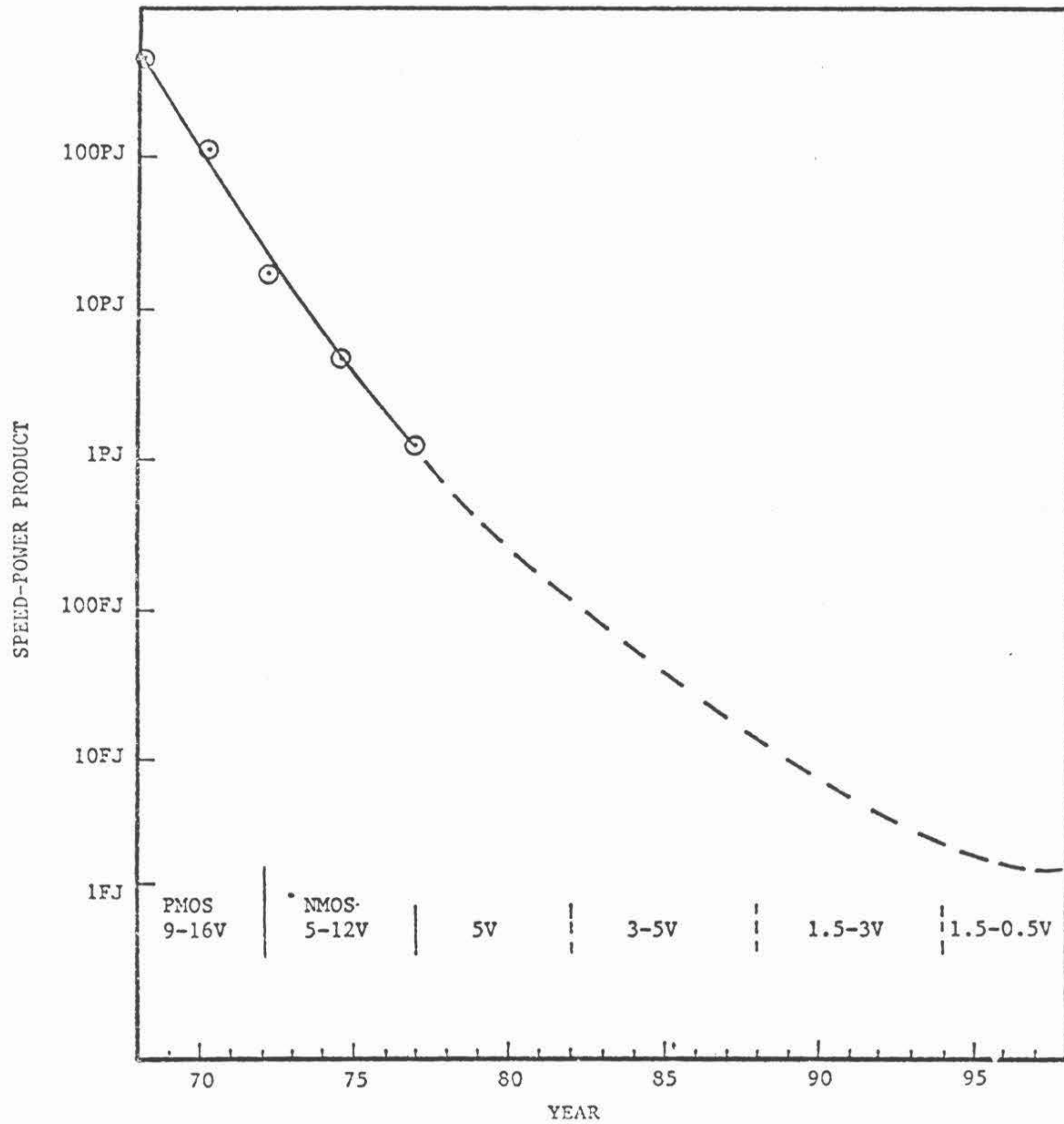
ELECTRICAL CHANNEL WIDTH W (μM)


+VDS
SECOND GATE EFFECT
+VDS
SUBSURFACE PUNCH-THROUGH


PUNCH-THROUGH VOLTAGE, VPT(V)
VPT
1μA
1
2
3
4
5
6
CHANNEL LENGTH, L (μm)


PAST AND EXPECTED FUTURE TREND OF MOS TECHNOLOGY
GATE DELAY
100NS
10NS
1NS
100PS
10PS
GATE DELAY
ME-GATE PMOS
SI-GATE PMOS
SI-GATE NMOS
SI-GATE NMOS DLOAD
HMOS
70
75
80
85
90
95
YEAR


PAST AND EXPECTED FUTURE TREND OF MOS TECHNOLOGY SPEED-POWER PRODUCT
SPEED-POWER PRODUCT
100PJ
10PJ
1PJ
100FJ
10FJ
1FJ
PMOS
9-16V
NMOS
5-12V
5V
3-5V
1.5-3V
1.5-0.5V
70
75
80
85
90
95
YEAR