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A Sub-Critical Barrier Thickness Normally-Off AlGaN/GaN MOS-HEMT

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Abstract—A new high-performance normally-off gallium nitride (GaN)-based metal–oxide–semiconductor high electron mobility transistor that employs an ultrathin subcritical 3 nm thick aluminium gallium nitride ($Al_{0.25}Ga_{0.75}N$) barrier layer and relies on an induced two-dimensional electron gas for operation is presented. Single finger devices were fabricated using 10 and 20 nm plasma-enhanced chemical vapor-deposited silicon dioxide (SiO_2) as the gate dielectric. They demonstrated threshold voltages (V_{th}) of 3 and 2 V, and very high maximum drain currents (I_{DSmax}) of over 450 and 650 mA/mm, at a gate voltage (V_{GS}) of 6 V, respectively. The proposed device is seen as a building block for future power electronic devices, specifically as the driven device in the cascode configuration that employs GaN-based enhancement-mode and depletion-mode devices.

Index Terms—GaN, AlGaN, MOS-HEMT, normally-off, enhancement-mode, insulated gate, PECVD SiO_2.

I. INTRODUCTION

GALLIUM nitride (GaN) based wide bandgap semiconductor transistor technologies demonstrate high breakdown electric fields and high current densities, and so are actively being researched for power electronics applications. Conventional GaN-based HEMTs are of depletion mode type but enhancement mode (E-mode) or normally-off devices would be preferable for power electronics since they simplify circuit design and provide highly desirable essential feature of fail-safe operation [1], [2].

Common approaches to achieve normally-off GaN-based HEMTs are based on the conventional d-mode devices (~20nm thick AlGaN barrier (~25% Al-content) with an inherent two dimensional electron gas (2DEG) channel) and include recessed-gate, fluorine ion implantation or growth of a p-type GaN or AlGaN cap layer to locally deplete the channel underneath the gate [2]. These approaches suffer from non-uniformity in device performance, device instability and

low V_{th}, respectively. They generally also do not exhibit high enough V_{th} for power switching applications for which values in the range of 3–5 V are preferred in order to prevent the mis-operation caused by noise.

Uniform E-mode device performance can be obtained through the use of a non-recessed thin barrier, i.e. an AlGaN thickness of under ~10 nm [3]–[7]. The channel can be easily depleted under the gate for normally-off operation due to the reduced 2DEG density, but the devices suffer from reduced drain currents and high on-resistances since the low density 2DEG is across the entire source-drain region. To reduce the access resistance between the gate-source and gate-drain regions, SiO_2 passivation layers have been used in these regions in Refs. [4] and [5]. In Ref. [6] the use of an epitaxial AlN cap layer that was selectively etched from the gate region was also demonstrated. V_{th} of these devices is around 0 V.

GaN MOSFETs with no gate-source and no gate-drain separation (and without a barrier layer, i.e. no heterostructure) have been demonstrated, but suffer from high On-resistances etc. [7]. Recently, a thin 12 nm barrier normally-off AlGaN/GaN MOS-HEMT with an overlap gate structure, i.e. also no gate-source and no gate-drain separation, and using a thick HfO_2 with a large dielectric constant as a gate insulator was proposed [8]. The device demonstrated a V_{th} of +3 V and I_{DSmax} of 730 mA/mm at V_{GS} of 10 V. Normally-off operation was attributed to negative charge in the gate dielectric which depleted the 2DEG channel for $V_{GS} < V_{th}$.

This letter describes a high performance E-mode AlGaN/GaN MOS-HEMT similar in layout to that in Refs. [7] and [8], i.e. using the gate overlap structure, but employing an ultrathin sub-critical 3 nm AlGaN barrier layer and with a SiO_2 gate dielectric. There is no inherent 2DEG channel at the AlGaN/GaN interface in this structure as the AlGaN thickness is below that required for 2DEG formation [9]. For 25% Al-content, the critical thickness beyond which 2DEG forms is around 6 nm [4], [10]. Devices with high positive threshold voltages and high current operation have been demonstrated.

II. DEVICE STRUCTURE AND FABRICATION

Fig. 1 shows a cross-section of the proposed normally-off AlGaN/GaN metal-oxide/(insulator)-semiconductor (MOS) HEMT. It consists of a sapphire substrate, 2–5 nm AlN nucleation layer, 3 μm GaN channel, and 3 nm $Al_{0.25}Ga_{0.75}N$
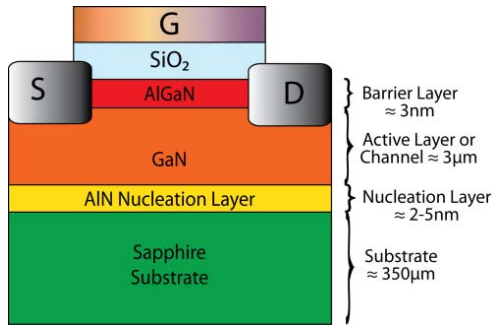
Fig. 1.   Cross-section of the proposed E-mode AlGaN/GaN device.

barrier layer. The structure was grown using molecular beam epitaxy (MBE) by SVT Associates. The device consists of source and drain Ohmic contacts nominally overlapped by the gate contact and employs a gate dielectric. With no or low gate-to-source voltage (V_{GS}), there is no 2DEG channel at the AlGaN/GaN interface to allow conduction of current between the drain and source contacts as the AlGaN barrier thickness is below the critical thickness required for the formation of such a channel [9]. However, if a large enough positive bias voltage V_{GS} is applied, it causes the formation of a quantum well at the AlGaN/GaN interface into which electrons from the source and drain Ohmic regions are attracted (by the positive gate voltage), effectively creating a 2DEG channel, and so the structure is a normally-off field effect transistor. As the critical device feature required for normally off operation, the AlGaN layer, is grown epitaxially, this eliminates the drawbacks experienced with previous techniques such as recess-etching in which the uniformity of the etch and hence that of the threshold voltages (V_{th}) is difficult to achieve. V_{th} is set further by the thickness and properties of the gate dielectric.

Single finger 100 μm wide devices were fabricated to test the device concept using process modules from our earlier work [10]. The source/drain Ohmic contacts were formed by photolithography, metal deposition (Ti/Al/Ni/Au, 30nm/180nm/40nm/100nm) and lift-off. The sample was then annealed at 775 °C for 30 seconds and then a layer of SiO_2 was deposited by PECVD at 300 °C using the following conditions: rf power of 15 watts, pressure of 1 torr, flow rate (SiH_4/N_2O/N_2) of 7/200/85 sccm, and a deposition rate of about 70 nm/min. The gate contacts were then formed by photolithography, metal deposition (Ni/Au, 50nm/150nm) and lift-off. Ohmic bond pad patterns were then defined by photolithography and the SiO_2 dielectric etched to expose the Ohmic contacts to complete the processing.

III. DEVICE OUTPUT AND TRANSFER CHARACTERISTICS

Results from typical devices from 2 samples are presented here. One sample employs a nominal 10 nm, while the other 20nm thick SiO_2 dielectric. Both devices employ 6 μm long and 100 μm wide gates. Output and transfer device characteristics as well as the transconductance were measured using Agilent's Device Analyzer B1500A. Fig. 2(a) shows the output characteristics of the device with 10 nm thick SiO_2 gate dielectric which demonstrated I_{DSmax} of over 450 mA/mm at V_{gs} = 6 V and V_{ds} = 10 V. Fig. 2(b) shows the output
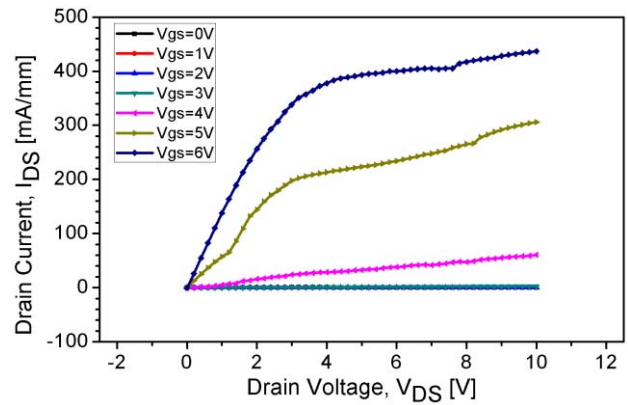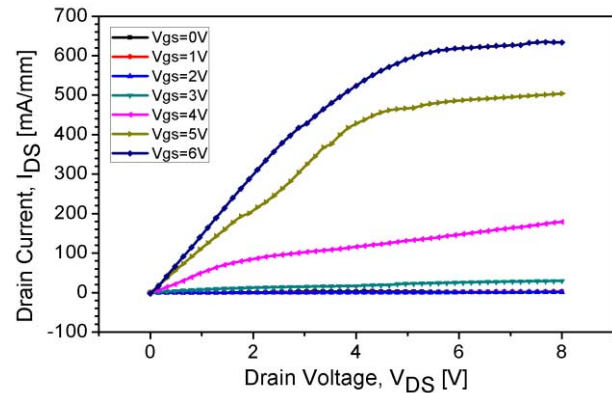
Fig. 2.   (a) Output characteristics of an E-mode 6μm × 100μm AlGaN/GaN MOS-HEMT with 10 nm thick SiO_2 gate dielectric. Note the (near) zero drain currents for V_{GS} of 0V, 1V, 2V, and 3V. (b) Output characteristics of an E-mode 6μm × 100μm AlGaN/GaN MOS-HEMT with 20 nm thick SiO_2 gate dielectric. Drain current traces for V_{GS} of 0V, 1V, and 2V are overlapping.

characteristics of the device with 20 nm thick dielectric. This device demonstrated I_{DSmax} of over 650 mA/mm at V_{gs} = 6V and V_{ds} = 8V. The measured currents are comparable to those of conventional depletion-mode devices demonstrating the equally good properties of an induced 2DEG channel (these are being quantified in on-going work). A procedure to extract contact resistances for this non-conducting structure (when no 2DEG is present) is being developed, but the low knee voltages indicate good contacts.

Transfer characteristics and transconductance at low drain bias voltages for the devices whose output characteristics are shown in Fig. 2(a) and (b) are plotted in Fig. 3. The threshold voltages are +3V and +2V (estimated at 1μA/mm) for the 10 nm and 20 nm thick gate dielectric devices. The enhancement-mode nature of the devices can be seen from these characteristics. The drop in threshold voltage with higher thickness of the SiO_2 may be due to the SiO_2 having positive charge, increased film stress etc.

IV. OFF-STATE BREAKDOWN CHARACTERISTICS

Off-state (V_{GS} = 0 V) breakdown characteristics are shown in Fig. 4. The breakdown voltages were 9 V and 17 V for the devices with 10 nm and 20 nm thick SiO_2 gate
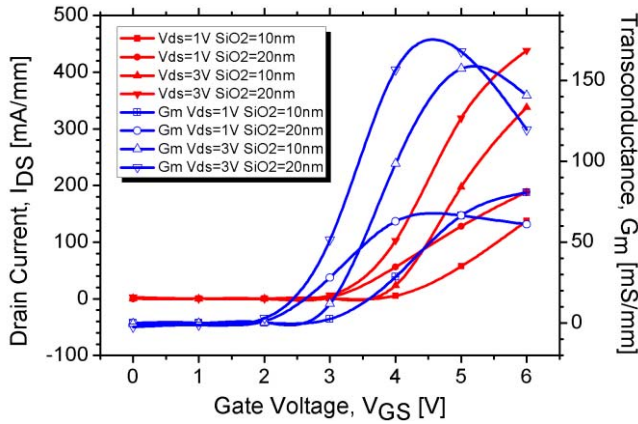
Fig. 3.   Transfer characteristics and transconductance of E-mode AlGaN/GaN MOS-HEMTs at low drain bias voltages of 1 V and 3 V.
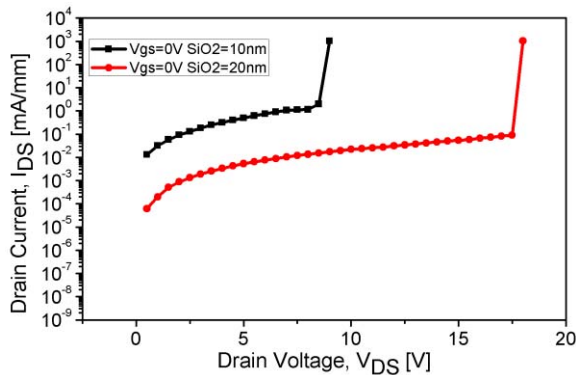

Fig. 4.   Breakdown characteristics of E-mode $6\mu m \times 100\mu m$ AlGaN/GaN MOS-HEMTs with 10 nm and 20 nm thick SiO_2 gate dielectrics.
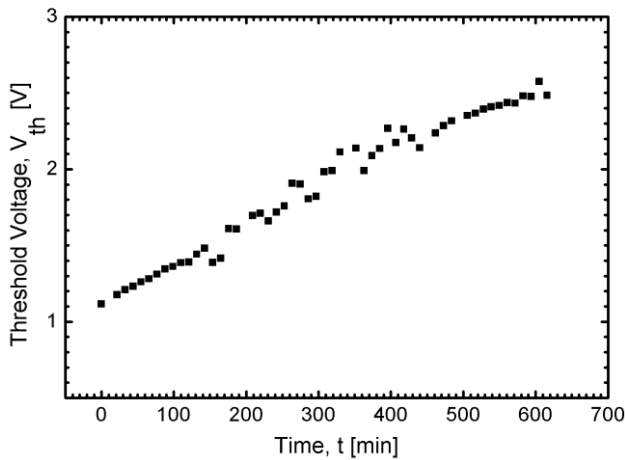

Fig. 5.   Variation of the threshold voltage of the proposed E-mode MOS-HEMT employing 20 nm thick SiO_2 gate dielectric with stress time.

dielectrics, respectively. The current rises sharply from about 1mA/mm to over 1000 mA/mm (set by equipment compliance) on breakdown. The measured breakdown field of ~9 MV/cm suggests that device breakdown is limited by the dielectric thickness, as seen in devices of similar geometry [7].

V. DEVICE RELIABILITY

Devices with 20 nm SiO_2 gate dielectric were assessed for stability. A stress test with $I_{DS} = 30$ mA/mm and $V_{DS} = 10$ V

was performed at 10 minute intervals. Fig. 5 shows the variation of the threshold voltage, V_{th} with stress time. V_{th} increased by 0.25V within the first hour and continued to rise with stress time, and increased by ~1.25V after 10 hours. Device stability is being investigated via capacitance-voltage techniques for atomic layer deposited (ALD) high-k dielectrics namely alumina, hafnia and zirconia that are deemed the best suited for this device structure. Note that similar instability is a present problem in other insulated gate GaN devices [11].

VI. CONCLUSION

We have fabricated high performance enhancement-mode AlGaN/GaN HEMTs on a sapphire substrate. The proposed device relies on an induced 2DEG for operation. The fabrication is repeatable and reproducible. The proposed device could be used to replace the low-voltage enhancement-mode silicon transistor used to drive the high-voltage depletion-mode transistor in the hybrid high-voltage cascoded GaN switch configuration [12]. On-going work is focused on improving the stability of the devices and on realising and characterising larger gate periphery and high breakdown voltage all-GaN cascode devices on silicon substrates.

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