



Thoms, Stephen, Macintyre, Douglas, Docherty, Kevin, and Weaver, John (2014) *Alignment verification for electron beam lithography*. Microelectronic Engineering. ISSN 0167-9317.

Copyright © 2014 Elsevier Science

A copy can be downloaded for personal non-commercial research or study, without prior permission or charge

Content must not be changed in any way or reproduced in any format or medium without the formal permission of the copyright holder(s)

When referring to this work, full bibliographic details must be given

<http://eprints.gla.ac.uk/91489/>

Deposited on: 19 February 2014

Alignment Verification for Electron Beam Lithography

Stephen Thoms, Douglas Macintyre, Kevin Docherty^a, John Weaver

School of Engineering, University of Glasgow, Glasgow, G12 8QQ, UK

a) Kelvin Nanotechnology Ltd, Glasgow, G12 8LT, UK

Corresponding Author: Stephen Thoms, +44 141 330 5656,
stephen.thoms@glasgow.ac.uk

Alignment between lithography layers is essential for device fabrication. A minor defect in a single marker can lead to incorrect alignment and this can be the source of wafer reworks. In this paper we show that this can be prevented by using extra alignment markers to check the alignment during patterning, rather than inspecting vernier patterns after the exposure is completed. Accurate vernier patterns can often only be read after pattern transfer has been carried out. We also show that by using a Penrose tile as a marker it is possible to locate the marker to about 1 nm without fully exposing the resist. This means that the marker can be reused with full accuracy, thus improving the layer to layer alignment accuracy. Lithography tool noise limits the process.

Keywords

electron beam lithography; alignment; Penrose tile

1 Introduction

Alignment of patterns defined by electron beam lithography is often required to sub 10 nm accuracy [1], for example when using double patterning [2] or fabricating photonic [3] or diffractive optic elements [4]. The use of this degree of accuracy has moved from fabricating occasional novel devices to a routine requirement, and thus the reliability of such alignment is of increasing importance. As with all fabrication steps it is important to have test structures [5] that can be used to monitor the quality of the lithography step in a non-destructive manner, ideally giving feedback immediately after the step has been carried out and before further processing. Vernier test structures, which are used to compare the developed resist with the marker level on the wafer and can be read with an optical microscope immediately after development, are often used. Unfortunately these cannot give the desired level of accuracy; the typical precision and accuracy of such verniers are around 50 nm. Usually the only way to ascertain if the alignment has been carried out satisfactorily is to carry out pattern transfer after resist development, and then inspect the wafer using a scanning electron microscope. As well as being time consuming, this has the serious drawback that faults are discovered too late. If there is an error, then the wafer must be scrapped and the only saving is that of avoiding unnecessary fabrication steps.

Fresh alignment markers need to be used for each level because of the high exposure dose generally given to each marker during the exposure process [3]. Alignment errors generally arise from either misshaped or misplaced markers, but also arise from the fact that different markers are used for each lithography level. This is because when a different set of markers is used there is an extra level of indirection in the alignment process. In other words, the errors arise not only from the alignment process itself, but also from the errors in position between the two sets of markers. This latter error may only be of the order of a few nanometres, but is important in the context of sub 10 nm alignment.

Penrose tiles have been shown to have many desirable properties for electron beam markers when using image correlation as the mark locate method [6]. One property which was predicted but not previously explored is the ability to reduce the applied dose during marker search so as to avoid exposing the resist. This paper shows that this is possible without losing marker search accuracy. It also demonstrates that collecting an image of a Penrose tile during exposure can be an effective alternative to a vernier test structure, and can be used to obtain sub 10 nm alignment information in a non-destructive and rapid manner.

2 Theory

There are a number of important considerations when choosing a marker design for correlation search. The ideal marker should have a sharply peaked autocorrelation, which from the Wiener-Khintchine theorem is equal to the Fourier transform of the power spectral density (PSD). This means that the PSD itself is broad, implying the presence of all frequencies in the Fourier transform. A Penrose tile satisfies this requirement because of its aperiodic nature.

In addition the autocorrelation should be well behaved under the condition of undersampling. This is important when seeking to avoid fully exposing the resist during marker search. This requires a reduction in the exposure dose imparted to the resist during image capture, while maintaining the signal to noise ratio. A constant signal to noise ratio is obtained by maintaining both the pixel dwell time during image

capture, and also the same number of pixels. Under these circumstances the only way in which the average dose can be reduced is to increase the pixel spacing, which results in undersampling. Patterns with edges aligned to the horizontal and vertical axis, such as squares and Barker codes, behave badly under conditions of undersampling, whereas a Penrose tile maintains the sharpness of its autocorrelation function as the pixel spacing improves, as is illustrated in Fig. 1. The autocorrelations are all normalised to enable better comparison of the central peaks. The Sierpinsky carpet pattern for alignment can give a sharp autocorrelation peak when undersampled, but not for all pixels sizes, as illustrated in Fig. 1. Even when it does give a sharp autocorrelation peak, it is not as sharp as that obtained using the Penrose tile pattern, which remains sharp for all pixel spacings.

It may also be necessary to defocus the beam in order to prevent exposure of an array of dots during image collection. The effect of a moderate defocus on the spot size is to increase the Gaussian size of the beam. The effect on the correlation function is simply to convolve it with the Gaussian beam profile, which leads to a Gaussian peak at the centre of the correlation. This broadens as the defocus increases. Even for zero defocus the beam profile is approximately Gaussian, so its centre can be always be found by fitting to a Gaussian.

3 Methodology

All electron beam lithography exposures were carried out using a Vistec VB6 tool operated at 100 kV. The resist used in all cases was a bilayer of PMMA (polymethylmethacrylate) with molecular weights of 85k and 360k; the developer used was a 2.5:1 mixture of IPA:MIBK (isopropyl alcohol : methyl isobutyl ketone), which results in a resist sensitivity of $366 \mu\text{C}/\text{cm}^2$ for large features on a silicon substrate.

To find the size of the image required to avoid fully exposing PMMA, a series of images of PMMA on silicon were collected using the VB6 with a beam defocused to between 30 and 150 nm, and a capture rate suitable for correlation mark location. Each image was a 100 pixel square and used the same scan rate, but had increasing image size (2, 4, 5, 8, 10, 15, 20 μm), thus decreasing the applied dose. The size, L, for which the resist was not fully exposed was determined.

A second test was designed to compare two different methods of monitoring the alignment error between lithography levels. This test was carried out on a 3" silicon wafer with multiple 1 cm square cells. Each cell contained local alignment markers, and an array of alignment test patterns. The test pattern consisted of a Penrose tile marker larger than L adjacent to the first level of a conventional vernier pattern with 2 nm resolution. The vernier pattern was designed to be read using a scanning electron microscope. After development a gold liftoff process (10 nm Ti / 50 nm Au) was carried out. A second lithography level was aligned to the first level in which the second level of the verniers was written and images of the Penrose markers were collected. Again, gold liftoff was carried out.

During the writing of the second level, the image collection method varied from site to site in two ways. In the first variation, images of different sizes were collected sequentially from the same Penrose tile to investigate whether undersampling of the Penrose tile made any difference to the marker search accuracy. The second variation consisted of changing the defocus of the beam, again to see how this affected the

correlation-based image location algorithm. We also compared the two methods of measuring the alignment error between the two lithography levels.

We carried out a final test to measure the effect of defocus on the exposure of dot arrays during image collection. To do this simple rectangles were exposed using a large beam step size to simulate image collection. The rectangles were exposed at various doses and defocus settings. The defocus required to prevent exposure at a given defocus was then observed.

4 Results and Discussion

4.1 Exposure Dose and Undersampling

Image sizes up to 4 μm were fully exposed by the beam, whereas images 5 μm square and above were not. The elapsed time for collecting a 100 pixel square image was 0.4 seconds, which corresponds to a dose of 1600 $\mu\text{C}/\text{cm}^2$ for a size of 5 μm and a beam current of 1 nA. The actual dose required to clear a 5 μm square is 710 $\mu\text{C}/\text{cm}^2$ indicating that about 50 % of the image collection time is taken up with overheads. A Penrose tile suitable for 20 μm square images was designed and tested, which is sufficient to keep the average dose below 50 $\mu\text{C}/\text{cm}^2$ during the image collection. Because the beam is sharply focused there is a danger of the resist being exposed in a series of dots, and this is considered in section 4.2.

4.2 Effect of Defocus and Undersampling on Mark Locate Accuracy

First the defocus was calibrated as follows. The final lens was adjusted to set the focal plane at different height offsets from the sample, and the amount of defocus generated measured from the image by an inverse convolution method. The spot size increased linearly by 3.0 nm per μm of height offset for the 1 nA beam used in this study.

Correlation marker locates were then carried out on the same marker using varying amounts of beam defocus and different image sizes. In one series of measurements the defocus was cycled 100 times through the sequence 0, 10 and 20 μm ; for each defocus images were collected at sizes of 2 and 20 μm . In this way the effect of both image size and defocus on the located marker position could be monitored, and statistics collected. The marker search repeatability was found to be 1.0 nm in x and 1.2 nm in y (1 sigma). In another set of measurements the defocus was set to 0, 20 and 50 μm . These results are summarised in Fig. 2(a), which shows how the central peak in the correlation blurs as the defocus is increased. Another set of measurements investigated the effect of undersampling by using image sizes of 2, 8, 16 and 20 μm for the correlation marker locate. The results are shown in Figure 2(b).

Neither a moderate height offset nor undersampling had any significant effect on the measured mark location. Both behave as expected from theory. The variation in the position measurement was the same in all cases and appears to be defined by the noise floor for the lithography tool.

The effect of defocus on dot exposure was measured for moderate amounts of defocus. Writing rectangle with a dose similar to that used for image collection the written dot size increased from 30 to 55 nm when the height offset changed from 0 to 10 μm . No dots were observed at a height offset of 20 μm , which is therefore a safe defocus to use when using PMMA as the resist. For a more sensitive resist a defocus equivalent to a 30 μm height offset gives an error in marker position of less than 5 nm and reduces the spot area by a further factor of 2.25. So it may be possible to use this

method to monitor alignment on resists such as ZEP520 (typical dose $120 \mu\text{C}/\text{cm}^2$) without exposing them, for instance, but not with very sensitive resists such as UVIII ($50 \mu\text{C}/\text{cm}^2$).

4.3 Monitoring Alignment Errors

The alignment errors measured using the verniers were compared with the errors measured using the correlation search method. Fig. 3(a) shows a detail of one of the verniers captured using an electron microscope. The long tick under the third line from the left indicates that this is the centre point of the vernier. The difference in period between the bottom and top grating is 2 nm, and the two gratings overlap for about 1/3 of the line length. It can be seen by comparing several lines that the leftmost and rightmost of the displayed lines show symmetrical errors, and therefore the reading of this vernier is +2 divisions, or 4 nm. We estimate the error in reading these verniers to be about ± 2 nm.

Fig 3(b) compares the errors measured by the two methods across a number of sites on the wafer. The dotted line is a guide to the eye and has unity gradient. It corresponds to a perfect correlation between the two measurements; the maximum measured deviation from this was 8.1 nm, with an average deviation of (0.6, -3.2) nm and a standard deviation of about 3 nm. The errors in this measurement include not only the measurement errors for both the correlation search and vernier, but also field and stage placement errors.

The use of extra alignment marks can therefore be used to monitor the accuracy of the alignment process during, or even prior to exposure, with an accuracy of better than 10 nm. This not only has the advantage of accuracy over using resist verniers read against existing features on the wafer, but also gives the possibility of aborting an incorrect exposure in the first place. There is an overhead in time in using such additional markers, but this is of the order of 1 second per marker, and for lengthy exposures on valuable wafers this may well be a worth while expenditure.

5. Conclusions

Penrose tile markers can be used for accurate marker search without fully exposing the resist, which means they can be used again for subsequent lithography levels. By using an extra marker after the alignment process, the accuracy of the alignment can be tested prior to the exposure process, thus avoiding costly wafer reworks if the initial alignment is erroneous for any reason.

Acknowledgements

The authors would like to acknowledge the support of the staff in the James Watt Nanofabrication Centre when carrying out this work.

References

1. Anderson, E.H., D. Ha, and J.A. Liddle, *Sub-pixel alignment for direct-write electron beam lithography*. Microelectronic Engineering, 2004. **73-4**: p. 74-79.
2. Bolten, J., N. Koo, T. Wahlbrink, and H. Kurz, *Definition of 15 nm half pitch grating structures by electron beam lithography double exposure techniques*. Microelectronic Engineering, 2013. **110**: p. 224-228.

3. Qi, M.H., E. Lidorikis, P.T. Rakich, S.G. Johnson, J.D. Joannopoulos, E.P. Ippen, and H.I. Smith, *A three-dimensional optical photonic crystal with designed point defects*. *Nature*, 2004. **429**(6991): p. 538-542.
4. Chao, W.L., E.H. Anderson, P. Fischer, and D.H. Kim, *Towards sub-10 nm resolution zone plates using the overlay nanofabrication processes - art. no. 688309*. *Advanced Fabrication Technologies for Micro/Nano Optics and Photonics*, 2008. **6883**: p. 88309-88309.
5. Stapper, C.H., F.M. Armstrong, and K. Saji, *Integrated-Circuit Yield Statistics*. *Proceedings of the Ieee*, 1983. **71**(4): p. 453-470.
6. Docherty, K.E., S. Thorns, P. Dobson, and J.M.R. Weaver, *Improvements to the alignment process in a commercial vector scan electron beam lithography tool*. *Microelectronic Engineering*, 2008. **85**(5-6): p. 761-763.

Figure Captions

Figure 1. Three different marker designs and their autocorrelation using different amounts of undersampling. (a) Shows a 2 μm square marker, (b) shows a Sierpinsky carpet with minimum rectangle size of 80 nm, and (c) shows a Penrose tile with minimum feature sizes around 100 nm. The centre of the autocorrelations are all shown with the same normalised brightness scale.

Figure 2. The effect of (a) defocus and (b) undersampling on the measured correlations for Penrose tile markers. The position shifts are relative to the focused beam (defocus 0) in (a) and the 2 μm image size in (b). The numbers on the correlation images in (a) indicate the height offset in the defocus for that image in μm .

Figure 3. (a) shows a typical alignment error as measured using the vernier pattern; (b) compares the vernier measurements with the results from the correlation measurement. The dotted line is a guide to the eye only, and corresponds to perfect agreement between the two methods.

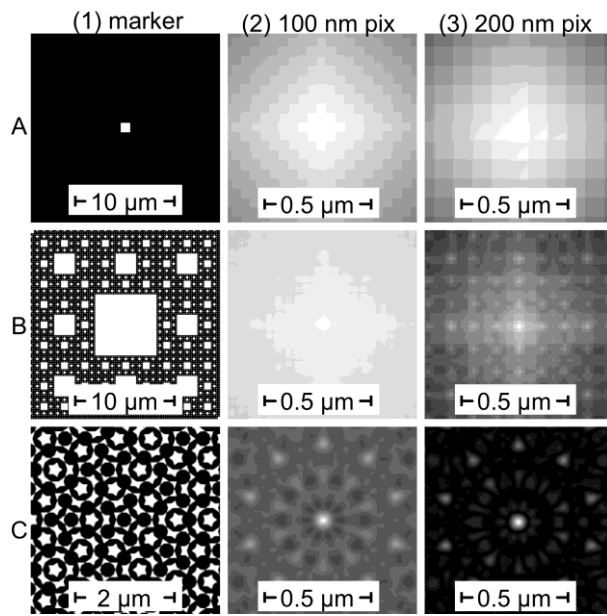


Figure 1

Centre of Correlation

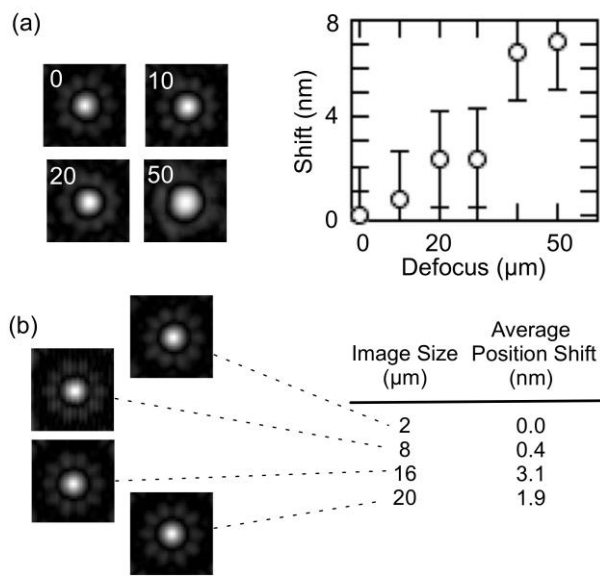


Figure 2

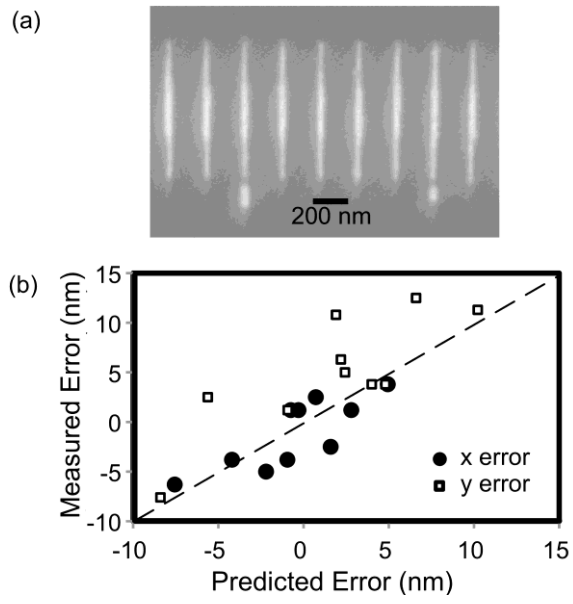


Figure 3