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Development of Edgeless n-on-p Planar Pixel Sensors for future ATLAS Upgrades

M. BOMBEN[a,*], A. BAGOLINI[b], M. BOSCARDIN[b], L. BOSISIO[c], G. CALDERINI[a,d], J. CHAUVEAU[a], G. GIACOMINI[b], A. LA ROSA[e], G. MARCHIORI[a], N. ZORZI[b]

[a]*Laboratoire de Physique Nucleaire et de Hautes Énergies (LPNHE) Paris, France*
[b]*Fondazione Bruno Kessler, Centro per i Materiali e i Microsistemi (FBK-CMM) Povo di Trento (TN), Italy*
[c]*Università di Trieste, Dipartimento di Fisica and INFN, Trieste, Italy*
[d]*Dipartimento di Fisica E. Fermi, Università di Pisa, and INFN Sez. di Pisa, Pisa, Italy*
[e]*Section de Physique (DPNC), Université de Genève, Genève, Switzerland*

Abstract

The development of n-on-p "edgeless" planar pixel sensors being fabricated at FBK (Trento, Italy), aimed at the upgrade of the ATLAS Inner Detector for the High Luminosity phase of the Large Hadron Collider (HL-LHC), is reported. A characterizing feature of the devices is the reduced dead area at the edge, achieved by adopting the "active edge" technology, based on a deep etched trench, suitably doped to make an ohmic contact to the substrate. The project is presented, along with the active edge process, the sensor design for this first n-on-p production and a selection of simulation results, including the expected charge collection efficiency after radiation fluence of $1\times10^{15} n_{eq}/cm^2$ comparable to those expected at HL-LHC (about ten years of running, with an integrated luminosity of 3000 fb^{-1}) for the outer pixel layers. We show that, after irradiation and at a bias voltage of 500 V, more than 50 % of the signal should be collected in the edge region; this confirms the validity of the active edge approach.

Keywords: Fabrication technology, TCAD simulations, Planar silicon radiation detectors

*corresponding author

1. Introduction

Planar pixel sensors are nowadays the standard choice for particle tracking and vertex reconstruction in high energy physics experiments. The ATLAS collaboration will upgrade its current Pixel Detector [1] in two phases: in 2013-2014 an additional 4th pixel layer will be inserted (Insertable B-Layer, IBL) [2], while for the High Luminosity phase of LHC (HL-LHC) [3] (beyond 2020) a completely new Pixel Detector is envisaged. The new pixel sensors will integrate a fluence of about $10^{16}\text{n}_{\text{eq}}/\text{cm}^2$ in the innermost layer, down to a fluence of $\phi = 1\times10^{15}\text{n}_{\text{eq}}/\text{cm}^2$ in the mid-outer layers, for an integrated luminosity of 3000 fb^{-1}, with an instantaneous luminosity of $10^{35}\text{cm}^{-2}\text{s}^{-1}$. These harsh conditions demand radiation-hard devices and a finely segmented detector to cope with the expected high occupancy. Several options are under investigation for the upgrade of the ATLAS pixel detector, including diamond [4], silicon 3D [5], HV-CMOS [6] and planar sensors [7].

The new pixel sensors will need to have high geometrical acceptance: the future material budget restrictions and tight mechanical constraints require a geometry inefficiency below 2.5% [2]. For example, the inactive areas at the device periphery should be less than 450 μm wide for IBL sensors [2]. In conventional sensor designs there is a relatively large un-instrumented area at the edge of the sensor to prevent the electric field from reaching the rim, where a large number of defects are present due to the wafer cutting; for example the current ATLAS pixel sensor has an un-instrumented region of 1.1 mm at the edge [1], including Guard Rings (GRs). GRs, placed all around the pixel area, can help to improve the voltage-handling capability.

One way to reduce or even eliminate the insensitive region along the device periphery is offered by the "active edge" technique [8], in which a deep vertical trench is etched along the device periphery throughout the entire wafer thickness, thus performing a damage free cut (this requires using a support wafer, to prevent the individual chips from getting loose). The trench is then heavily

doped, extending the ohmic back-contact to the lateral sides of the device: the depletion region can then extend to the edge without causing a large current increase. This is the technology we have chosen for realizing n-on-p pixel sensors with reduced inactive zone.

Since a high bias voltage is required after heavy irradiation to maintain a deep depletion region and to ensure efficient charge collection in the presence of trapping effects, several GRs are commonly used. However, adding one or more GRs spoils the gain of the active behavior of the sensor edge. Indeed, once carriers are created in the guard ring area, or even outside, electrons are collected by the guard rings, which, since are floating, re-emit the charge toward all the pixels next to them. Such charge, being distributed among a large number of pixels, beyond the fact that it is insufficient to trigger a hit, cannot give any information about the hit position. A compromise should be found between minimization of pixel to trench distance and presence of one or more GRs. In order to gain a better insight into this point, detectors with different termination structures, with and without GRs, have been simulated, designed and fabricated.

In this paper the active edge technology (Section 2) is presented; it has been chosen for a first production of n-on-p planar sensors at FBK (Section 3). Studies performed with TCAD simulation tools (Section 4) helped in defining the layout and making a first estimation of the charge collection efficiency expected after irradiation.

2. The active edge sensor fabrication at FBK

The sensors are fabricated on 100 mm diameter, high resistivity, p-type, Float Zone (FZ), <100> oriented, 200 μm thick wafers. The active edge technology [8] is used, which is a single sided process, featuring a doped trench, extending all the way through the wafer thickness, and completely surrounding the sensor. For mechanical reasons, a support wafer is therefore needed, making the back inaccessible after wafer-bonding. Thus, as first process steps, a uni-

form high-dose boron implant has been performed on the back side, followed by a thermal oxide growth on both sides.

The wafers have then been shipped to Sintef [9], to be wafer-bonded to a 500 μm thick silicon substrate. After having received back the wafers, the remaining process has been performed in the FBK clean-room. A solution will be identified to remove the support wafer and separate the devices[1]; for the time being all the detectors have been designed in order to allow conventional saw-cut separation and substrate biasing from the front-side, through a dedicated ohmic contact ("bias tab") . In this way, the efficiency of the edge region before and after irradiation can be studied even without removing the support wafer.

Up to the trench definition, the process follows standard steps. Since the read-out electrodes are n-type, they will be shorted together by the electron inversion layer, induced by the positive fixed charge present in the oxide, unless a p-type implant, compensating such charge, surrounds the pixels. Both homogeneous ("p-spray") and patterned ("p-stop") implants have been used; the process splittings adopted in the fabrication batch only concern the presence and the doses of these implants, as detailed in table 1. Electrical tests on irradiated devices will tell which combination can better guarantee both junction isolation and high breakdown voltages (which are competing demands, since they are in favor of high and low boron doses, respectively), even after years of operation in a harsh radiation environment.

Two patterned high dose implants, a phosphorus implant forming the pixel and GR junctions and a boron implant for the ohmic contact to the substrate ("bias tab"), are then performed.

The etching of the trench is accomplished by a Deep Reactive Ion Etching (DRIE) machine, the same used for the fabrication of 3D detectors [10]. In the latter case, a 10 μm diameter and 200 μm deep hole has to be etched; the etching mask is made by multiple stacks of dielectrics (oxide and nitride) plus a thick photoresist. The trenches in an active edge sensor must be fully passing,

[1]The easiest solution is the lapping of the support wafer once the sensors are diced.

p-spray	p-stop
low dose	absent
high dose	absent
low dose	present
high dose	present
absent	present

Table 1: List of the different isolation solutions adopted in the process.

i.e. their bottom has to reach the silicon oxide, which separates the active wafer from the support wafer. In the etching of a trench, a problem arises from the fact that the photoresist tends to wear out and/or lift along the sides of the trench, and then to be a less effective mask. Thicker stacks of dielectrics are thus needed.

After the trench is etched, its walls are boron-doped in a diffusion furnace. Thus, a continuous ohmic contact to the substrate is created on the trench wall and to the backside. FBK technology can routinely obtain very uniform, well defined and narrow trenches, as shown for example in Figure 1. For a 200 μm thick bulk the typical trench width is of 5 μm. Functional planar p-on-n devices with active edge have been already fabricated and reported [11].

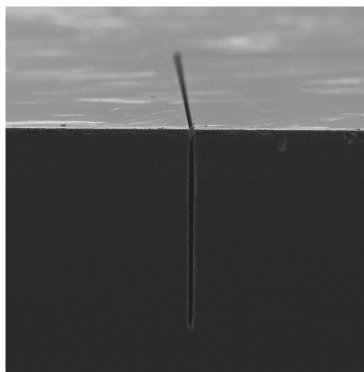

Figure 1: SEM picture of a test trench, after cleaving the wafer perpendicularly to the surface and to the trench itself.

99 The trenches are then oxidized and filled with polysilicon. The remaining
100 processing, arriving at the final device, whose cross-section is sketched in Fig-
101 ure 2, is quite standard, and includes the following steps:

102 • contact opening

103 • metal deposition and patterning

104 • deposition of a passivation layer (PECVD oxide) and patterning of the
105 same in the pad and bump-bonding regions.

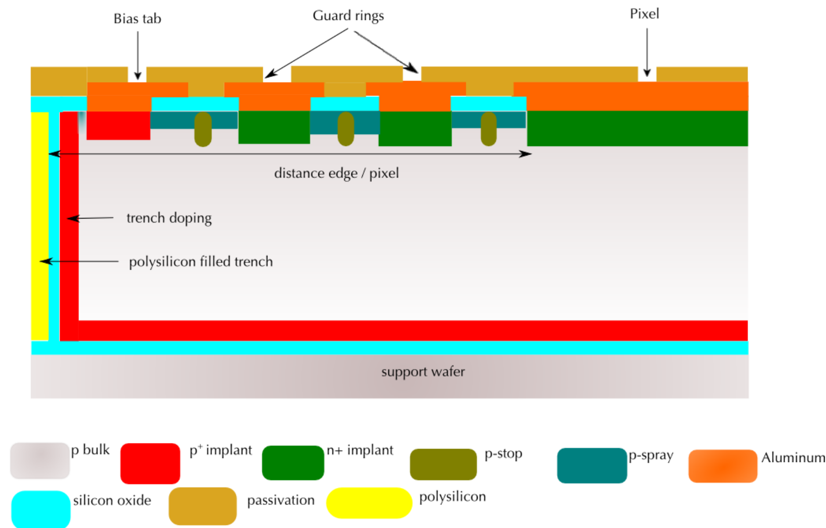

Figure 2: Schematic section of the pixel sensor. The region close to the sensor's edge is portrayed, including the pixel closest to the edge, the edge region, including GRs (when present), the bias tab (present only on one edge of the device), the vertical doped trench, and the support wafer.

106 Since some sensors will be bump-bonded to FE-I4 [12] read-out chips, it
107 is necessary to select good sensors at the wafer level, by measuring their I-V
108 characteristics. For this purpose, an additional layer of metal is deposited over
109 the passivation and patterned into stripes, each of them shorting together a
110 row of pixels, contacted through the small passivation openings foreseen for the
111 bump bonding. This solution has already been adopted for the selection of good

112 3D FE-I4 sensors for the ATLAS IBL [14]. After the automatic current-voltage
113 measurement on each FE-I4 sensor, the metal will be removed by wet etching,
114 which does not affect the electrical characteristics of the devices.

115 3. The wafer layout

116 FE-I4 compatible pixel sensors consist of an array of 336 × 80 pixels, at a
117 pitch of 50 μm × 250 μm, for an overall sensitive area of 16.8 mm × 20.0 mm.
118 Thus, on a 100 mm wafer, there is space for nine FE-I4 compatible pixel sensors;
119 a detail of one of them is shown in Figure 3.

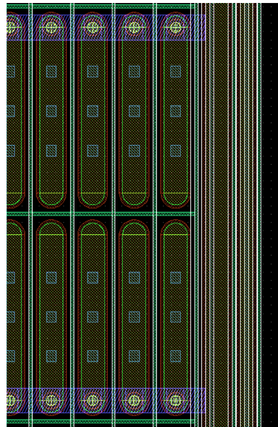

Figure 3: Layout of a detail of an FE-I4 compatible pixel array.

120 The nine FE-I4 sensors differ in the pixel-to-trench distance (100, 200, 300,
121 and 400 μm) and in the number of the guard rings (0, 1, 2, 3, 5, and 10)
122 surrounding the pixel area (see Figure 2). The sensor with 3 GRs and a 200 μm
123 pixel-to-trench distance features two different GR designs, and each of them
124 is repeated twice. A list of the different FE-I4 sensor versions is reported in
125 Table 2.

126 A bias tab for substrate biasing (either by probing or by wire bonding),
127 located internally to the surface delimited by the trench, is placed at about
128 1.5 mm from the pixelated area on one of the sides (see also Figure 2).

Multiplicity	Number of GRs	pixel-to-trench distance (μm)
1	0	100
1	1	100
1	2	100
4	3	200
1	5	300
1	10	400

Table 2: List of FEI4 sensors. The number of the sensors (first column) is reported for each combination of number of GRs and pixel-to-trench distance. Two different designs are envisaged for the sensor with 3 GRs and 200 μm pixel-to-trench distance. See text for more details.

129 The wafer layout also includes four sensors compatible with the FE-I3 read-
130 out chip [13] (array of 160×18 pixels at a pitch of $50\mu\text{m} \times 400\mu\text{m}$, for an overall
131 area of about 8 mm $\times$ 7.2 mm). The trench-pixel distance is 100 μm for all of
132 them, while they differ in the number of GRs (1 or 2). In addition, four sensors
133 compatible with the OmegaPIX readout chip [15] are present (array of 96×24
134 pixels at a pitch of $35\mu\text{m} \times 200\mu\text{m}$, for an overall area of about 3.4 mm $\times$ 4.8
135 mm).

136 At the periphery of the wafer, there is room for a large number of test
137 structures, *i.e.* square diodes and small arrays of FE-I4-like pixels, which differ
138 in the number of GRs surrounding the active area and in the trench-to-pixel
139 distance. Several possible combinations have been implemented, including all
140 those used for the FE-I4 sensors. The aim of these structures is to test the
141 isolation and to measure the high-voltage behavior before and (possibly) after
142 irradiation, in order to find the best sensor configuration to be bump-bonded to
143 the read-out chip and to select the best combination of GR number and trench
144 distance for a possible future production.

145 To study the charge collection properties of the sensors, particularly in the

146 edge region, “stripixel” arrays have also been designed. They are small 1-D
147 arrays of about 2 mm long strips, which are an elongated version of the FE-I4
148 pixels with the addition of a pad at one end, so that they can be wire bonded to a
149 readout chip for strip detectors. Also in this case, there are several combinations
150 of trench distances and number of GRs.

151 4. TCAD simulation

152 In order to explore and compare the properties of the design variations
153 considered, numerical simulations were performed with TCAD tools from SIL-
154 VACO [16]. 2D structures analogous to the one sketched in Figure 2 have been
155 simulated, varying parameters like the number of GRs and the pixel-to-trench
156 distance. The break down (BD) behaviour of the devices, the electrical field
157 distribution and the charge collection efficiency (CCE) were studied, for simu-
158 lated un-irradiated and irradiated sensors, with a fluence $\phi = 1 \times 10^{15} \mathrm{n_{eq}/cm^2}$.
159 This is the expected fluence for the outer pixel layers of the new tracker at the
160 end of the HL-LHC phase.

161 In the following, details on dopant parameterization, on device physics mod-
162 els adopted and on the radiation damage parameterization will be presented,
163 followed by a selection of results from simulations.

164 *4.1. Doping parameters*

165 Each of the doped regions (n^+ for the pixel and the GRs, p^+ for the backside,
166 p-stop, p-spray, bias tab and the trench walls) have been modeled with simple
167 functions, depending on a set of parameters like the peak concentration, the
168 reference concentration, *i.e.* the concentration value at a distance equal to the
169 “rolloff” [2] from the peak position, and the vertical “rolloff” distance. The values
170 used are summarized in Table 3.

[2] The doping concentration decreases from its peak value to its reference value over a distance equal to the rolloff

Doped region	impurity	function	peak value (cm^{-3})	reference value (cm^{-3})	rolloff (μm)
Pixel and GR	D	gaussian	2×10^{19}	10^{16}	1.0
Back	A	gaussian	2×10^{19}	10^{16}	1.0
Trench	A	erf	2×10^{19}	10^{12}	2.0
Bias tab	A	gaussian	2×10^{19}	2×10^{16}	0.5
P-spray	A	gaussian	5×10^{16}	7×10^{15}	0.5
P-stop	A	gaussian	5×10^{17}	7×10^{16}	0.5

Table 3: Implant parameters for simulated detectors; A (D) is for acceptor (donor) impurities.

171 *4.2. Physics models and radiation damage parameterization*

172 SILVACO TCAD uses a complete set of physical models for semiconduc-
173 tor device simulation. Among them, models for concentration dependent mo-
174 bility, field dependent mobility, bandgap narrowing, concentration dependent
175 lifetime, trap-assisted and Auger recombination were used. Oxide fixed charge
176 density (with surface density $Q_{\rm ox} = 10^{11}/{\rm cm}^2$ before irradiation, and $Q_{\rm ox} =$
177 $3 \times 10^{12}/{\rm cm}^2$ after), generation-recombination lifetimes and surface recombina-
178 tion velocity have been set according to measured IV and CV characteristics of
179 diodes from previous n-on-p CiS[3] productions.

180 The defects at the edge have been modeled with a 1 μm wide region in which
181 the generation-recombination lifetime was set to a very small value (10^{-12} s; for
182 comparison, before irradiation the corresponding value for the bulk is of 10^{-5} s).
183 If the trench doping were not effective, a large current would appear as soon as
184 the electric field reaches the edge area.

185 To describe the radiation damage, an effective model based on three deep
186 levels in the forbidden gap was used [17]. Each of these deep levels is defined as
187 either donor (D) or acceptor (A), and is characterized by its energy (with respect
188 to the closest energy band), its capture cross-sections for electrons (σ_e) and holes
189 (σ_h) and its introduction rate η, which is the proportionality term between

[3] Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH

190 defect concentration and radiation fluence, expressed as 1 MeV n_{eq}/cm^2. In
191 Table 4 these properties are summarized.

Type	Energy (eV)	$\sigma_e(cm^2)$	$\sigma_h(cm^2)$	$\eta(cm^{-1})$
A	E_C -0.42	9.5×10^{-15}	9.5×10^{-14}	1.613
A	E_C -0.46	5.0×10^{-15}	5.0×10^{-14}	0.9
D	E_V +0.36	3.23×10^{-13}	3.23×10^{-14}	0.9

Table 4: Relevant parameters for acceptors (A) and donor (D) deep levels in the bandgap, describing the radiation damage.

192 The deep level close to the centre of the bandgap is an highly effective
193 generation center affecting the leakage current, while the other two contribute
194 to the change of the effective doping concentration of the bulk and hence the
195 depletion voltage.

196 Radiation-induced interface traps at the Si-SiO_2 interface are also included
197 in the simulation, as described in [18].

198 The model was validated by comparing simulation results to the change in
199 depletion voltage and leakage current in irradiated n-on-p diodes from previous
200 n-on-p CiS productions.

201 *4.3. Simulation results*

202 The structure in Figure 2 was slightly modified in the simulations: the sup-
203 port wafer was not present and the backside p^+ implant was metallized. This
204 was done in order to simulate a sensor ready for use.

205 The sensors were simulated under reverse bias, applying a negative voltage
206 to the back contact while keeping the pixel at ground potential; the bias tab was
207 left floating. Different geometries were simulated, varying the number of GRs
208 and the pixel-to-trench distance; see Table 5 for the list of simulated geometries.
209 If present, the GRs were left floating during the simulations.

# of GRs	pixel-to-trench distance (μm)
0	100
1	100
2	100
0	200
1	200
2	200

Table 5: List of simulated sensor layouts.

210 *Current-voltage characteristic and break down voltage*

211 Figure 4 shows the current-voltage curves of all the simulated designs, before
212 irradiation. The depletion voltage has been estimated using AC analysis for
213 simulations, determining the depletion voltage value from the fit to the $log(C)-$
214 $log(V)$ curve; the result was checked against the aforementioned measurements
215 on n-on-p diodes from a former production. A sensor with a design compatible
216 with the current ATLAS pixel modules was also simulated; it features a pixel-
217 to-trench distance of 1.1 mm and 16 GRs.

218 From Figure 4 it can be seen that before irradiation the BD voltage exceeds
219 by at least 100 V the depletion voltage for all the designs we considered. The
220 ATLAS-like sensor shows higher BD voltage with respect to those predicted
221 for our edgeless detectors, but all sensors are largely over-depleted before BD.
222 Increasing the pixel-to-trench distance yields a higher bulk-generated current,
223 since the depleted volume can further extend laterally. Adding more GRs helps
224 greatly in increasing the value of BD voltage, extending the operability range
225 of the sensors. The best performance is obtained from a device with 2 GRs
226 and a $100\mu m$ pixel-to-trench distance. The BD voltage from simulations is in
227 agreement with other active edge productions; see for example [19] [4]

228 As reported in the literature by different groups (*e.g.* [20]), after irradiation

[4]The trenches are doped with a four-quadrant ion implantation of boron ions.

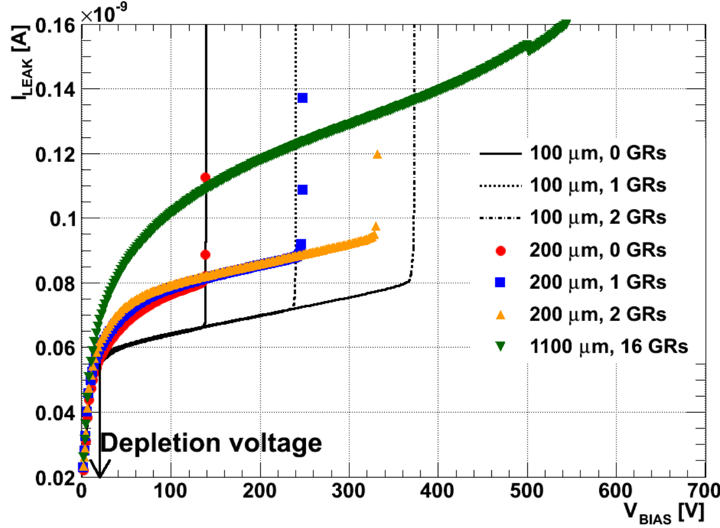

Figure 4: Simulated IV curves for the pixel closest to the edge, for several sensor designs before irradiation (see text for details). The simulated current has been scaled to reproduce the behaviour of a 50 μm wide pixel in the edge direction. The depletion voltage is indicated by the arrow.

229 the BD voltage increases to much larger values. Our simulations of irradiated
230 devices confirm this observation, as it can be seen in Figure 5 where the same set
231 of sensors of Figure 4 is now presented after a simulated fluence of $10^{15}\mathrm{n_{eq}/cm^2}$.
232 No BD is observed in any sensor up to 1000 V bias voltage.

233 *Electric field distribution*

234 In Figure 6 the electric field distribution is shown for an un-irradiated detec-
235 tor with 2 GRs and 100μm pixel-to-trench distance, for a bias voltage of 50 V. It
236 can be seen that the detector is fully depleted and the electric field is maximum
237 in the region of the p-stops, with a value of some units in 10^4V/cm. It can also
238 be observed that the electric field in the edge region is non negligible, hence
239 signal should be collectable from there.

240 In Figure 7 the electric field distribution is reported for a sensor with 2 GRs
241 and 100μm pixel-to-trench distance, after a simulated fluence $\phi = 10^{15}\mathrm{n_{eq}/cm^2}$.

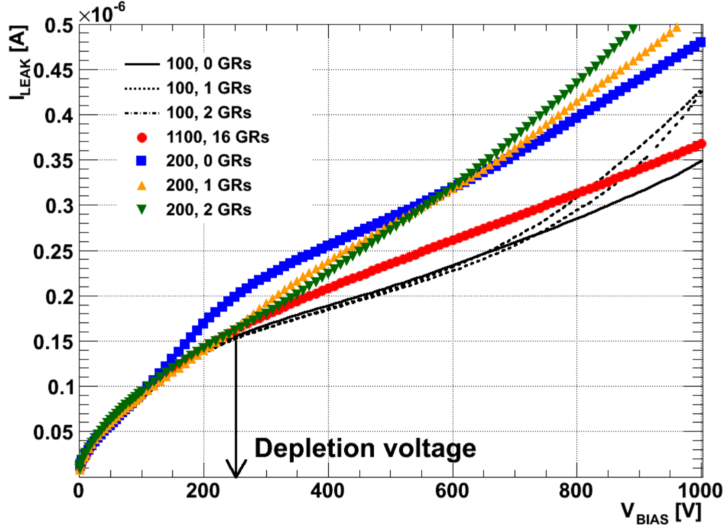

Figure 5: Simulated IV curves for the pixel closest to the edge, for several sensor designs after a simulated fluence of $10^{15}\mathrm{n_{eq}/cm^2}$ (see text for details). The simulated current has been scaled to reproduce the behaviour of a 50 μm wide pixel in the edge direction. The depletion voltage is indicated by the arrow.

242 In Figure 7, top, the detector is biased at 50 V; a large portion of the volume
243 is non-depleted, *i.e.* the electric field is negligible. An interesting feature is an
244 increase of the high electric field close to the back implant and to the trench:
245 this is a known effect called double peak (DP) [21]. The fact that it is accounted
246 for by our simulation supports the reliability of the simulation itself.

247 In Figure 7, bottom, the electric field distribution is reported for the same
248 irradiated detector at a bias voltage of 400 V, well beyond the depletion volt-
249 age ($\sim$ 250 V). The electric field extends all over the bulk, although a small
250 undepleted region is still present at the edge, near the back-side; nonetheless,
251 a large portion of the region between the pixel and the trench shows a sizable
252 electric field, confirming the possibility of charge collection in the edge region,
253 after irradiation too. As before irradiation, the electric field is maximum in the
254 region of the p-stops, but now its value is in the 10^5V/cm range.

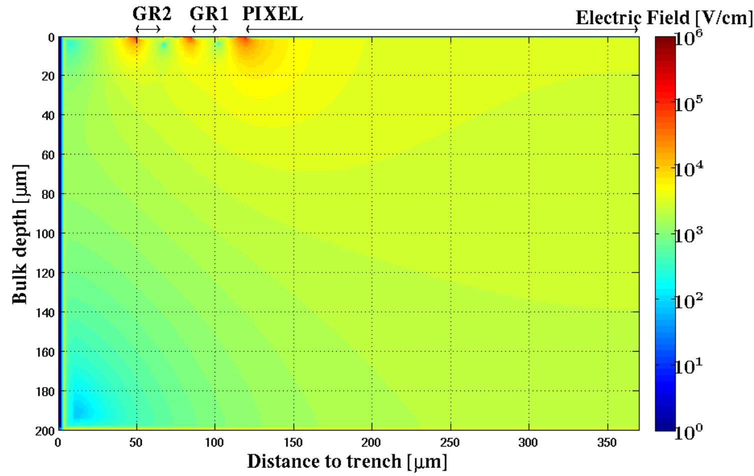

Figure 6: Electric field distribution for non-irradiated device at $V_{bias} = 50\,V$. The sensor has 2 GRs with a 100 μm distance between trench and pixel.

255 *Charge collection efficiency*

256 To study charge collection efficiency (CCE) after irradiation, charge creation
257 in irradiated sensors was simulated. The most interesting case is when the
258 charge is released in the gap between the pixel and the trench, when no GRs
259 are present. If a significant amount of charge can be collected after irradiation
260 in that region, the edgeless concept would be verified to work.

261 Our sensor was illuminated from the front side with a simulated 1060 nm
262 laser beam, setting its power in order to generate the same charge that would
263 be released by a minimum ionizing particle (MIP) traversing 200 μm of silicon
264 ($\sim$ 2.6 fC). The laser beam was originating above the front side of the detector,
265 with a 2 μm wide gaussian beamspot. The duty cycle of the laser was 50 ns,
266 with the power ramping up in 1 ns, remaining constant for 10 ns and ramping
267 down in the next nanosecond.

268 The CCE was studied as a function of the bias voltage for the detector with
269 no GRs and a 100 μm trench-to-pixel distance. Two incidence points of the
270 laser beam have been considered: one within the pixel and the other in the edge

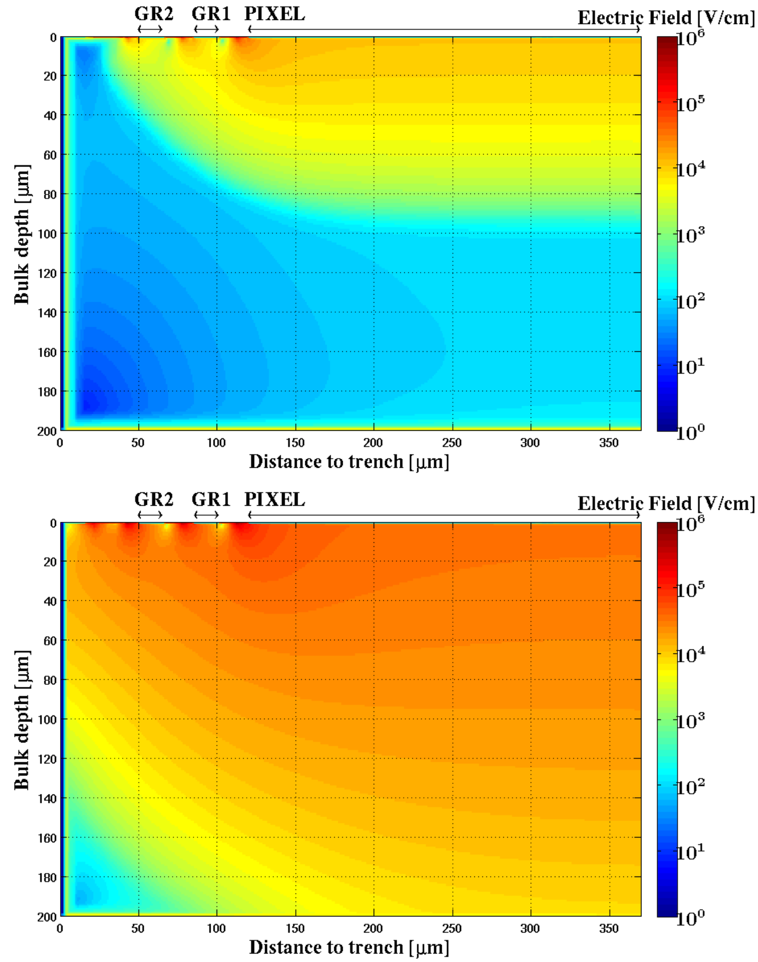

Figure 7: Electric field distributions for a device irradiated with a fluence $\phi = 10^{15}\mathrm{n_{eq}/cm^2}$. Top: $\mathrm{V_{bias}} = 50\,\mathrm{V}$; bottom: $\mathrm{V_{bias}} = 400\,\mathrm{V}$. The sensor has 2 GRs and a 100 μm distance between edge and pixel.

region, at 50 μm distance from the pixel. In the following they will be identified as "Pixel" and "Edge", respectively.

Based on the properties of the laser beam and of the target material, the simulation program determined the charge of carriers photogenerated inside the device by one pulse. The charge collected by the pixel was defined as the integral over the laser duty cycle of the current flowing through the pixel, once the stable

leakage current had been subtracted. Finally, the CCE was obtained by dividing this collected charge by the total photogenerated charge.

In Figure 8 the CCE is presented as a function of the bias voltage for the simulated fluence for the two incidence points of the laser beam.

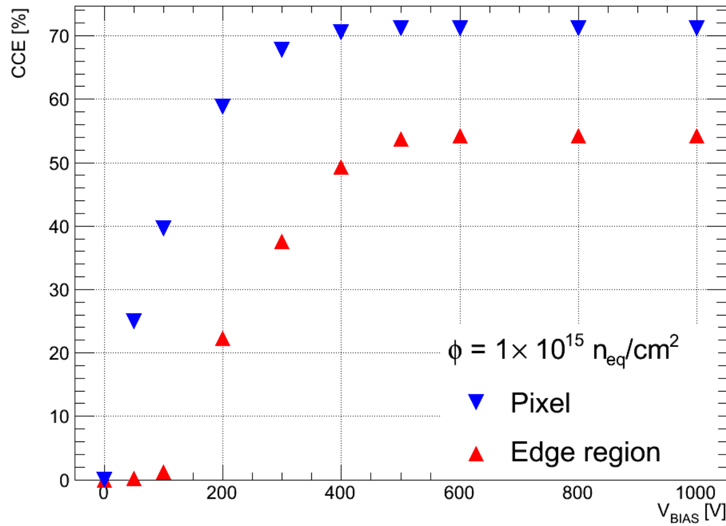

Figure 8: Charge collection efficiency as a function of bias voltage for an irradiated device at a fluence $\phi = 10^{15}\mathrm{n_{eq}/cm^2}$. The laser is entering the detector either in the pixel region ("Pixel") or in the un-instrumented region ("Edge region"). The sensor has no GRs, and a 100 μm distance between edge and pixel.

At a fluence $\phi = 10^{15}\mathrm{n_{eq}/cm^2}$ more than 50 % of the signal is collected in the "Edge" region at a bias voltage of 500 V; as a comparison, 70 % of the signal is retained in the "Pixel" region. The expected collected charge in the "Edge" region is then of ~8 ke [5], which corresponds to a signal large enough to trigger the FEI4 readout chip. Both in the "Pixel" and in the "Edge" region the effect of trapping can be observed: the collected charge reaches a *plateau* at high voltage, but there the CCE is not of 100 %. No charge is collected

[5] the MPV for the charge created by a MIP in 200 μm is 16 ke

288 from the "Edge" region below 100 V: indeed at 100 V bias the electric field
289 is negligible in that region when there are no GRs. It can be seen that while
290 the maximum CCE for a charge created in the pixel region is reached at a bias
291 voltage above $\sim$ 400 V, in the "Edge" region a bias voltage of 600 V is needed:
292 this is consistent with the depletion zone extending laterally.

293 Calculations based on trapping time experimental data [22] for our sensor
294 thickness and our target fluence produce CCE estimations in agreement with
295 our simulations.

296 5. Conclusions and outlook

297 In view of the Large Hadron Collider High Luminosity (HL-LHC) phase, an
298 upgrade of the ATLAS Inner Detector is envisaged. New pixel sensors will have
299 to work in an unprecedentedly harsh environment; moreover, material budget
300 restrictions and tight mechanical constraints demand for a reduction of the
301 inactive region at the edge of sensors.

302 FBK Trento and LPNHE Paris are developing new planar n-on-p pixel sen-
303 sors for the ATLAS detector upgrade, characterized by a reduced inactive region
304 at the edge thanks to a vertical doped lateral surface at the device boundary,
305 the "active edge" technology. Simulation studies show the effectiveness of this
306 technique in reducing the dead area while retaining a large margin of operabil-
307 ity in terms of bias voltage, even after simulated fluences comparable to those
308 expected at the end of the HL-LHC phase for the external layers; they also
309 show that after irradiation more than 50 % of the signal is retained, even in the
310 "Edge" region for the sensor with 100 μm pixel-to-trench distance.

311 Next steps will be a full electrical characterization of these "active edge"
312 devices, followed by functional tests of the pixel sensors with radioactive sources
313 and eventually in a beam test, after having bump bonded a number of pixel
314 sensors to the FE-I4 read out chips.

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