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Design of DG-MOSFETs for High Linearity Performance

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In the sub-50nm scale, aggressive scaling of MOSFETs are expected to stop at dual-gate (DG) architectures on SOI substrates [1-3]. So far the design efforts on these novel structures have concentrated on the digital performance. However, beyond the traditional digital circuit building blocks, sub-50nm MOSFETs will be strong contenders also for analogue RF applications in lucrative wireless communications market. This is guided by the fact that peak CMOS cutoff frequencies are now in excess of 100 GHz, doubling every three years [4]. Hence it is imperative to analyze the potential of DG-MOSFETs also for analogue applications.

Linearity is an essential requirement in integrated CMOS RF systems, ensuring that high order harmonics and inter-modulation terms are negligible at the output. Although there are system level techniques to improve linearity, they all require complex circuitry [5]. A transistor-level linearization is more appropriate for the power amplifiers in the portable systems. To date, there is no report on the linearity figures of DG-MOSFETs or on how it is affected by the choice of design parameters. In this work, we carry out such a study for the first time and investigate the linearity of DG-MOSFETs using accurate 2-D device simulations.

Contrary to digital applications, drain saturation current and V_T are not suitable figures of merit in a *direct* evaluation of RF analogue performance of MOSFETs. A reliable and simple metric used to evaluate linearity performance of individual MOSFETs is input-referred IP3 point [6]. This measures the input power (P_{IP3}) where the output amplitude of 1st (main) and 3rd harmonics are equal due to inter-modulation inherent to device operation.

Although traditionally compact models are used for linearity analysis, such approximations are either totally inadequate or currently non-existent for RF performance evaluation of sub-50 nm MOSFETs with complex channel-gate charge coupling features. The use of physics-based device simulators provides a more complete and accurate analysis alternative. In this study, we use ISE TCAD suite [7] to simulate terminal characteristics of generic DG-MOSFET structures similar to FIG.1. Specifically, we consider symmetric and asymmetric DG-MOSFET designs [8,9]. Asymmetric DG-MOSFET, which has a single electron channel with a larger peak density (FIG.2) has been shown to be a good competitor to the symmetric one [8]. In this work, we show that these devices are superior to symmetric ones also in terms of linearity. We also show that the DG-MOSFET linearity may be optimized by use of non-uniform doping techniques, including low-high and delta-doping profiles.

In our analysis, DC transfer characteristics similar to those in FIG.3 are used to obtain transconductance (g_m) and its second derivative, by using high order polynomial fits (>7th-degree) to simulated data (FIG.4). These results are in turn employed in the calculation of signal power P_{IP3} (FIG.5) [5]. A comparison of the linearity figures of DG-MOSFETs indicates that asymmetric device consistently outperforms the symmetric counterpart. Uniform channel doping improves the linearity figures for both cases. We observe (see FIG.6) that a step (low-high) profile dramatically improves the linearity of the asymmetric design, while its impact on symmetric device is less pronounced. The improvement for the asymmetric device with an optimum doping profile may reach as much as ~10 dBm, which is quite appreciable. Moreover, this figure is even larger, if compared against the undoped device.

We present a full account of changes introduced by the use of similar doping techniques to general and linearity performance of DG-MOSFETs with smaller gate length and channel thickness. A comparison with standard planar architecture is also attempted to clarify true analogue performance of DG-MOSFETs.

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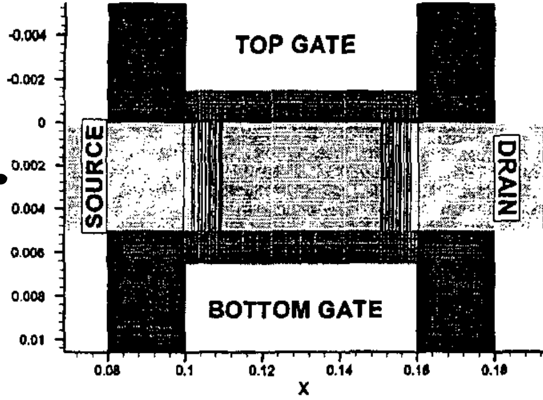

FIGURE 1: Generic DG-MOSFET structure with L_{eff}=50nm and the corresponding 2D mesh. All contacts are shown as void. The barrier height for the top and bottom gates are different for symmetric (ΦB=0.55eV) and asymmetric (Φ_B=±0.55eV) devices investigated.

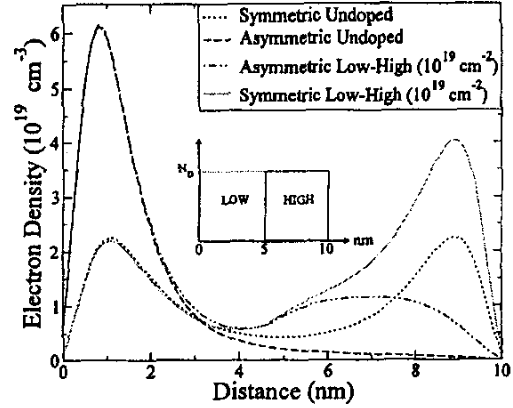

FIGURE 2: Electron density profiles of undoped asymmetric (V_G=1.0 V) and symmetric (V_G=1.6 V) DG-MOSFET structures investigated. For comparison, density profiles belonging to step-like (low-high) doped devices are also plotted. Note that asymmetric device has a single channel.

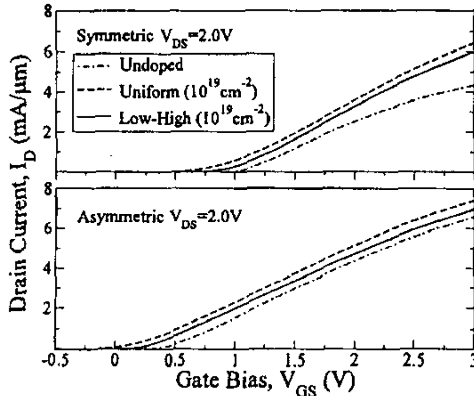

FIGURE 3: Comparison of transfer characteristics of DG-MOSFETs with asymmetric and symmetric designs. In these simulations, we employ HD transport model to account for non-stationary effects and density gradient method to include quantum mechanical confinement.

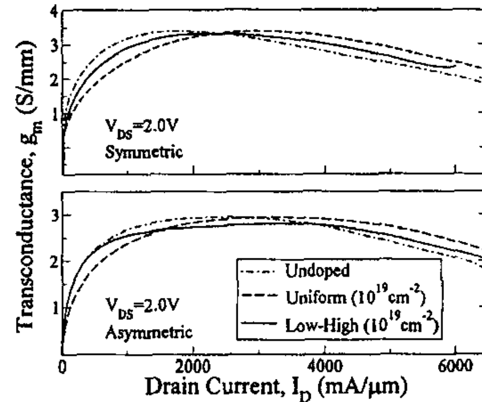

FIGURE 4: Transconductance characteristics of asymmetric and symmetric DG-MOSFETs with three different doping profiles. The better linearity of asymmetric design with low-high doping profile is visible by the flat top of the g_m curve. We use 7th order polynomials to differentiate I_d-V_g data.

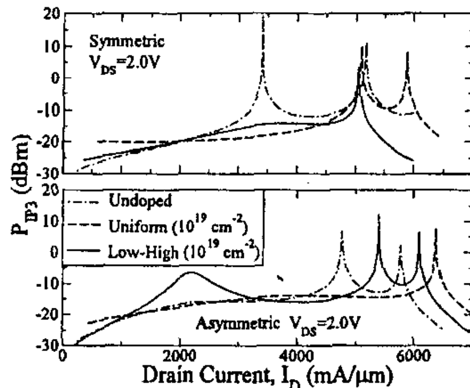

FIGURE 5: Analysis of linearity performance of DG-MOSFETs with transfer characteristics from FIG.3&4. The low-high doping greatly improves asymmetric device linearity around the maximum transconductance point (gm_{max}), where linear amplifiers are expected to operate.

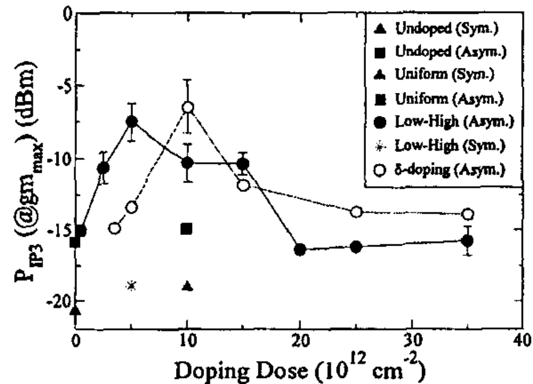

FIGURE 6: Summary of linearity performance of DG-MOSFETs at the vicinity of maximum transconductance point. Asymmetric device is superior and easier to optimize using low-high doping profiles or δ-doping. In both cases, a dose of ~10^{13}cm^{-2} improves linearity as much as 10dBm.