Improving speed of Tunnel FETs logic circuits

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Tunnel transistors are one of the most attractive steep subthreshold slope devices which are being investigating to overcome power density and energy inefficiency exhibited by CMOS technology. These transistors exhibit asymmetric conduction which can cause sustained noise voltage pulses (bootstrapping) within digital TFETs circuits leading to delay degradation. In this paper, we propose a minor modification of the complementary gate topology to avoid the bootstrapping problem and show its impact on speed at the circuit level. Speed improvements up to 33% have been obtained for 8-bit Ripple Carry Adders when implemented with our solution.

Introduction: Scaling of CMOS tecnhnology is facing big challenges. Among them, the 60 mV/decade minimum subthreshold slope (SS) of CMOS devices impedes the reduction of the threshold voltage without leading to unacceptable off-state leakage currents, so that supply voltage cannot be reduced without significantly degrading circuit speed. This translates in power density problems for high performance applications requiring nominal supply voltages or energy inefficiency for low voltage applications. Thus, high research efforts on devices exhibiting a steeper subthreshold slope (SS < 60mV/dec) are going on. Reduced SS allows lowering threshold voltage while keeping leakage current under control, enabling low voltage operation with acceptable speed, leading to power and energy savings. Tunnel transistors are one of the most attractive steep subthreshold slope devices [1,2]. And subthreshold swing under 60mV/dec has been experimentally obtained in different material system and research on TFETS has been advancing rapidly in recent years [3].

There are several application challenges of the TFET regarding circuit design. Among them, a major one is their asymmetric conduction, also referred as unidirectional current-conduction. Unlike MOSFETs, n-type (p-type) TFET transistors with negative (positive) drain to source voltage exhibit very low conduction. It is well known, that due to this characteristic, it is necessary to modify the topology of pass-transistor logic circuits or SRAM cells [4], but there are also circuit operation effects in complementary logic circuits associated to the asymmetric conduction. Relatively high voltages can be bootstrapped within digital TFETs circuits which may have significant speed and reliability impacts [5]. Logic redesign including buffer insertion and input ordering swapping has been proposed to mitigate the effect. However this solution is not systematic and might be costly in terms of design effort. Alternatively, we propose a minor modification of the gate topology to overcome the problem.

Delay degradation associated to sustained noise voltage pulses. Figure 1 illustrates the bootstrapping phenomenon using the original example in [5]. Simulations have been carried out using TFET transistor models from Notre Dame University [6]. These models are valid in all four operating quadrants of the TFET (positive and negative V_{DS} and V_{GS}). In particular the model for the double-gate p-i-n InAs TFET has been used in this paper.

It is observed that the rising switching of the OUT signal is capacitively coupled to the output of the inverter (Ina). Due to the low conduction of P-TFET with positive V_{DS}, transistor p0 cannot discharge Ina which results in a sustained voltage (542mV) over *VDD* (350 mV). In a MOSFET counterpart of this circuit, the symmetric characteristic of the transistor reduces magnitude and duration of noise on Ina. The magnitude of the sustained coupling noise is related to the ratio of the fixed to coupling capacitance and supply voltage. It increases with the later and decreases with larger fixed capacitance. Examples showing accumulation of voltage bootstrapping along logic stages or as the result of repetitive input switching are also shown in [5].

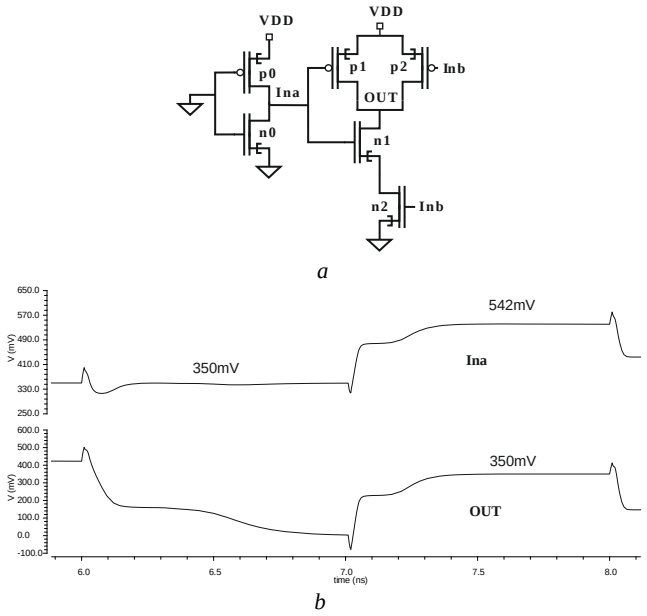

Fig. 1 *Bootstrapping phenomenon reported in [5].*
a Schematic.
b Signal OUT is capacitively coupled to Ina and, thus, bootstrapped to 542mV.

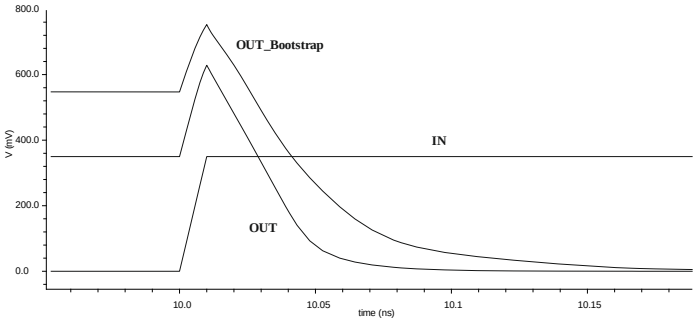

Fig. 2 *Responses of an inverter loaded with a NAND gate for different inputs conditions.*

Although no logic failure is produced by this effect, there are timing and reliability concerns. Delay increases due to larger voltage swing and, in addition, it becomes history depending complicating timing analysis. Figure 2 illustrates delay increment for *VDD* equal to 350mV. The responses of an inverter loaded with a NAND gate for different inputs conditions to the gate are compared. Signal OUT_Bootstrap is the output of the inverter when the NAND output is switching producing sustained noise pulses as in Figure 1. OUT is the response of the inverter when the NAND output is at logic 0. Propagation delay increases by 60% as a consequence of bootstrapping.

It can easily be shown that not only voltages exceeding positive supply voltages are produced (positive noise pulse in the following), but also that voltages under the negative bias are bootstrapped (negative noise pulse). Simply converting the NAND gate in Fig.1 into a NOR gate and fixing the inverter input now to *VDD* allow observing this behavior.

Proposed Complementary gate topology: The rationale of our proposal is providing a conduction path alternative to the natural (but very low conductive in TFETS) one to charge/discharge noise voltage pulses at the gate output. By natural one, we mean the p transistor of the inverter (in general the p pull-up network) for positive noise pulses and the n transistor (in general the n pull-down network) for the negative ones. Clearly, a p-type transistor with its source connected to the output node, its drain to *VDD* and its gate connected to ground would be able to discharge a positive noise pulse. In the same way, an n–type transistor with its source connected to the output node, its drain to ground and its gate to *VDD* would be able to charge a negative noise pulse. Thus, adding both, the gate is protected from both types of bootstrapping. Figure 3a depicts a generic complementary gate with additional n and p transistors. However, the p-transistor might be also useful to cope with

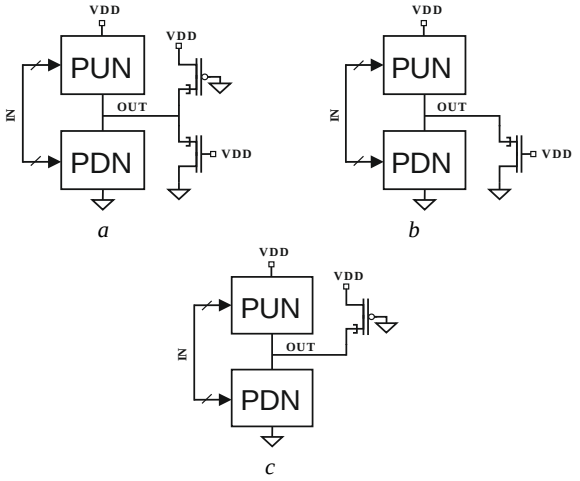

Fig. 3 *Proposed topologies to avoid bootstrapping.*
a With n and p transistor
b Only n transistor
c Only p transistor

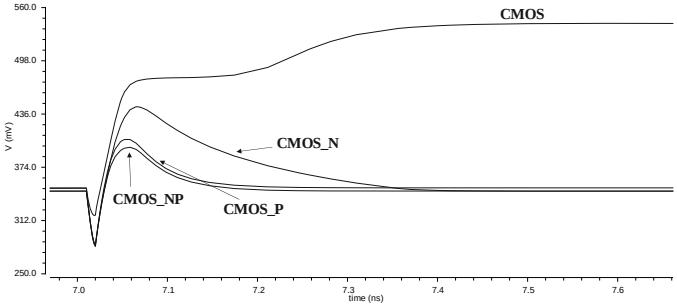

Fig. 4 *Comparison among output responses of the conventional CMOS inverter (CMOS) and the proposed topologies (CMOS_N, CMOS_P and CMOS_NP), where positive bootstrapping effect is removed.*

a negative noise pulse due to the current occurring for enough large positive V_{DS}. Note that the transistor in this situation exhibits a drain to source voltage greater than *VDD*. Equivalently, the added n-transistor could be able to discharge a positive noise pulse. Therefore, topologies with a single added transistor (n or p) are also explored (Figure 3b and 3c).

Figure 4 depicts simulation results for circuit in Figure 1 with four different inverters: conventional complementary inverter as in Figure 1 (CMOS) and inverters with the topology in Figure 3a (CMOS_NP), 3b (CMOS_N) and 3c (CMOS_P). It can be observed that the three proposed topologies are able to solve the positive bootstrapping phenomenon exhibited by the conventional inverter. Clearly, the p-transistor is more effective than the n-one. The solution with both of them is very slightly better than the one with the p transistor. The capability of the proposed topologies to handle negative noise pulse has been also validated. As expected, the n-transistor is now more effective.

Circuit Level Evaluation. In order to analyse the impact of this problem at the circuit level and to evaluate the speed improvement associated with the elimination of the voltage bootstrapping effect using our proposed solution, different 8-bit ripple carry adders have been designed and evaluated. First two distinct logic designs have been considered. One uses inverters and NAND gates (RCA_NAND) while the other is built from inverters and NOR gates (RCA-NOR). Four different version of each one has been implemented. Versions CMOS use conventional CMOS gates. Versions CMOS_N (CMOS_P, CMOS_NP) uses the CMOS gates with added n transistor (p transistor, n and p added transistors). Gates have been sized using minimum transistor length and width except for serial connected transistor. The conventional rule of multiplying the minimum width by the number of serial transistors is applied.

The sustained voltage pulses are observed in CMOS version but not in the others. Delays for input stimulus producing sustained voltage pulses in CMOS and which propagates through carry chain (worst case delays) have been measured for each circuit at two different supply voltages. Table 1 reports obtained results. It can be observed that CMOS designs are slower than the others. The three designs with the modified topologies exhibit similar delays in the RCA_NOR adders. Best results are obtained by CMOS_NP designs in the RCA_NAND adders. Delay of CMOS is around 30% (20%) larger than the proposed ones at 0.5V (0.3V).

Table 1: Delay performance comparison among several 8-bit RCA designs with conventional CMOS inverters and the proposed inverter topologies.

		Delay (ns)			
VDD	Circuit	CMOS	CMOS_N	CMOS_P	CMOS_NP
0.5V	RCA_NAND	1.63	1.28	1.24	1.22
	RCA_NOR	1.62	1.22	1.23	1.22
0.3V	RCA_NAND	7.39	6.32	6.19	6.10
	RCA_NOR	7.40	6.09	6.08	6.07

Conclusion: Solutions at the transistor level are proposed for the bootstrapping phenomenon occurring in TFET digital circuits. The conventional complementary gate topology is modified by adding one or two transistors able to discharge (charge) the sustained noise voltage pulses and avoiding the delay degradation associated to them. The proposed solutions are validated at the circuit level. Speed improvements up to 33% have been obtained for 8-bit Ripple Carry Adders when implemented with our solutions.

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