Efficient Simulation of Thermo-Mechanical Stress in the On-Chip Metallization of Integrated Power Semiconductors

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***Abstract*—Integrated power semiconductors are often used for applications with cyclic on-chip power dissipation. This leads to repetitive self-heating and thermo-mechanical stress, causing fatigue on the on-chip metallization and possibly destruction by short circuits. Because of this, an accurate simulation of the thermo-mechanical stress is needed already during the design phase to ensure that lifetime requirements are met. However, a detailed thermo-mechanical simulation of the device, including the on-chip metallization is prohibitively time-consuming due to its complex structure, typically consisting of many thin metal lines with thousands of vias. This paper introduces a two-step approach as a solution for this problem. First, a simplified but fast simulation is performed to identify the device parts with the highest stress. After, precise simulations are carried out only for them. The applicability of this method is verified experimentally for LDMOS transistors with different metal configurations. The measured lifetimes and failure locations correlate well with the simulations. Moreover, a strong influence of the layout of the on-chip metallization lifetime was observed. This could also be explained with the simulation method.**

***Index Terms*—Integrated power technologies, integrated circuit modeling, power semiconductor devices, on-chip metallization, thermo-mechanical stress, degradation, reliability.**

I. Introduction

TODAY, integrated power technologies that combine analog and digital circuitry together with LDMOS transistors as power devices on the same chip are used in many commercial, industrial, and automotive applications. Often, the LDMOS transistors are subject to repetitive power dissipation as in injection valve drivers. This leads to pronounced self-heating especially in advanced technologies with small device sizes. In such applications which are often found in automotive sector, a typical failure mechanism of the LDMOS is the degradation of its metallization due to repetitive thermo-mechanical stress, which can eventually lead to a short circuit between LDMOS source and drain [1]–[4].

Therefore, an accurate prediction of the stress in the metallization is required already in the design phase to ensure that lifetime requirements are fulfilled. However, the LDMOS metallization in advanced technologies is complex, typically consisting of many metal fingers in several layers, connected by even more vias and contacts. Hence, a thermo-mechanical simulation taking all details into account is not practical due to an excessively long simulation time.

Because of this, several approaches for reducing the simulation time were suggested. One of them is the non-conforming discretization method, e.g., [5]. Here, the regions of interest (usually those where the highest stress is expected) must be specified in advance. They are investigated with a fine mesh while the other regions are meshed coarsely. However, correctly specifying regions of interest is difficult without previous knowledge of the stress distribution. Furthermore, due to the high computational effort required for calculating the interface conditions between fine and coarse meshes, the reduction of simulation time is not significant for 3D simulations, see [5].

Another approach to reduce meshing effort and thus simulation time is to substitute regions that require a very dense mesh (for instance the many metal fingers of the LDMOS with the vias and contacts) by an equivalent layer consisting of a single homogeneous material, e.g., as described in [6]–[9]. This results in much easier meshing, however, simulation accuracy is lower because the structure of the substituted regions is lost.

Nevertheless, this can be used successfully in submodeling as shown in [8]–[10]. First, a simplified simulation with a partly homogenized structure (as described above) is performed to identify the regions with high stress. Then, in a second step, only these small regions including all details neglected in the first (simplified) simulation are simulated, but now more accurately with a high spatial resolution. Due to the small size of the considered region, the thermo-mechanical simulation can be done in an acceptable time. This procedure can be extended to more levels. This so-called multilevel submodeling is preferred for simulations with a high aspect ratio, e.g., [8]–[10], and allows accurate thermo-mechanical simulations within an acceptable time.

Until now, submodeling was shown for copper interconnects [9], [10], solder bumps [11], and interlayer dielectric

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cracking in flip chip assemblies [12]. In this paper, it will be demonstrated that homogenization combined with two-level submodeling is already sufficient to accurately model degradation in the on-chip metallization of LDMOS transistors.

The simulation approach used for this work was already presented in [13], the first experimental results in [14]–[16]. In this paper, the results are extended by additional simulations and experiments. Furthermore, the presented approach is verified by measurements for several integrated LDMOS transistors with different metallization layouts.

The paper is structured as follows. Section II describes the test structures and shows the experimental results which serve as a reference for the simulations. Section III presents the proposed simulation approach in more detail. The simulation results for the presented test structures are shown in Section IV. Section V discusses how the lifetime can be estimated for the different metallization variants. The paper ends with the conclusions in Section VI.

II. Test Structures & Measurements

A. Test Structures

Dedicated test structures were used to evaluate and verify the proposed simulation approach. They contain an LDMOS transistor that closely resembles typical automotive applications. Its heat-dissipating active area is 620 μm $\times$ 310 μm, see Fig. 1. The test structures were fabricated in a 0.18 μm integrated power technology with four thin lower metal layers and a thick upper power metal layer. The LDMOS has 32 source fingers and 33 drain fingers. The lower four metal layers transport the LDMOS current mostly vertically from the drain and source contacts to the upper power metal layer which forms the (lateral) connection to the pads. This layout, which is also commonly used in many applications, leads to a comparatively small resistance and thus limits the voltage drop inside the metallization. Four different test structures with wide and narrow metal lines and with or without additional floating sense lines[1] between the source and drain metallization in the four lower metal layers were investigated, see Fig. 2 for the top views and cross-sections. The layout of the test structure with narrow metal lines corresponds to the transistor layout in automotive application.

B. Measurement Procedure and Results

The measurements are carried out on-wafer with a needle card. The test structures have large drain and source pads so that several needles can be used in parallel to decrease the current per needle and the overall contact resistance. Nevertheless, the drain-source voltage is measured with additional sense needles. To stress the LDMOS transistor, the test setup of Fig. 3 is used, see also [16]. The device is heated by applying a drain-source voltage of 30 V and a constant drain current of 1.67 A for a duration of 0.66 ms, resulting in a peak temperature of 500 °C. This is repeated 50 times per second (the cooling time between the pulses is 19.34 ms) until the device fails. The tests were performed at room temperature and the backside of the wafer was held at a constant temperature of 25 °C.

[1]Floating sense lines are promising candidates for sensors that measure the degradation of the metallization system and detect its impending failure, see [14], [16] for a more detailed discussion.

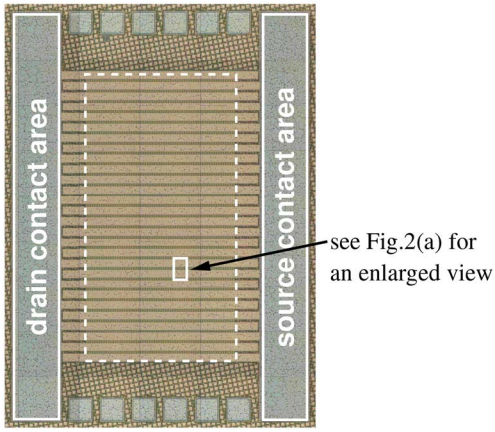

Fig. 1. Top view of an LDMOS test structure with wide lower metals and wide power metal. The white dashed rectangle shows the heating area, and the white solid rectangle indicates the device part which is enlarged in Fig. 2(a).

Device failures arise due to the repetitive thermo-mechanical stress, which causes an increasing plastic deformation of the on-chip metallization. After many cycles, the strain is so large that cracks in the dielectric appear, which are rapidly filled with metal. This eventually leads to a short circuit between LDMOS source and drain, causing a catastrophic failure of the device as described in [1]–[3]. This is detected by the measurement setup, and the drain current is then turned off after a few μs. Nevertheless, there is also a visible burn mark on top of the device (see Fig. 4), indicating the failure location.

For the experiments, between 17 and 24 samples of each test structure variant were stressed and destroyed, following the procedure described above. The failure locations and the number of cycles to destruction have been recorded. The lifetime as shown in Fig. 5 follows a Weibull distribution as is expected for this type of failure mechanism, see [17]. The average lifetime of each type is given in Tab. I.

The failure locations of the test structure with wide metals and narrow metals are shown in Fig. 6. It is observed that the failure locations are not in the device center (where the temperature is the highest) but elliptically distributed around the center, agreeing with [1].

III. Simulation Approach

A. Simulation Procedure

A numerical thermo-mechanical simulation of the test structure taking all vias and contacts into account is not feasible because of their large number. As already discussed in Section I, considering them would require a very fine mesh, leading to extreme memory requirements and unacceptably long CPU times. Because of this, the simulation approach already proposed in [13] is used. It consists of two steps as illustrated in Fig. 7.

1) Step (Coarse Simulation): The complex regions of the structure under consideration (here the lower four thin metal layers with the many vias in between and contacts, see Fig. 2) are replaced by an equivalent homogeneous layer. Because of

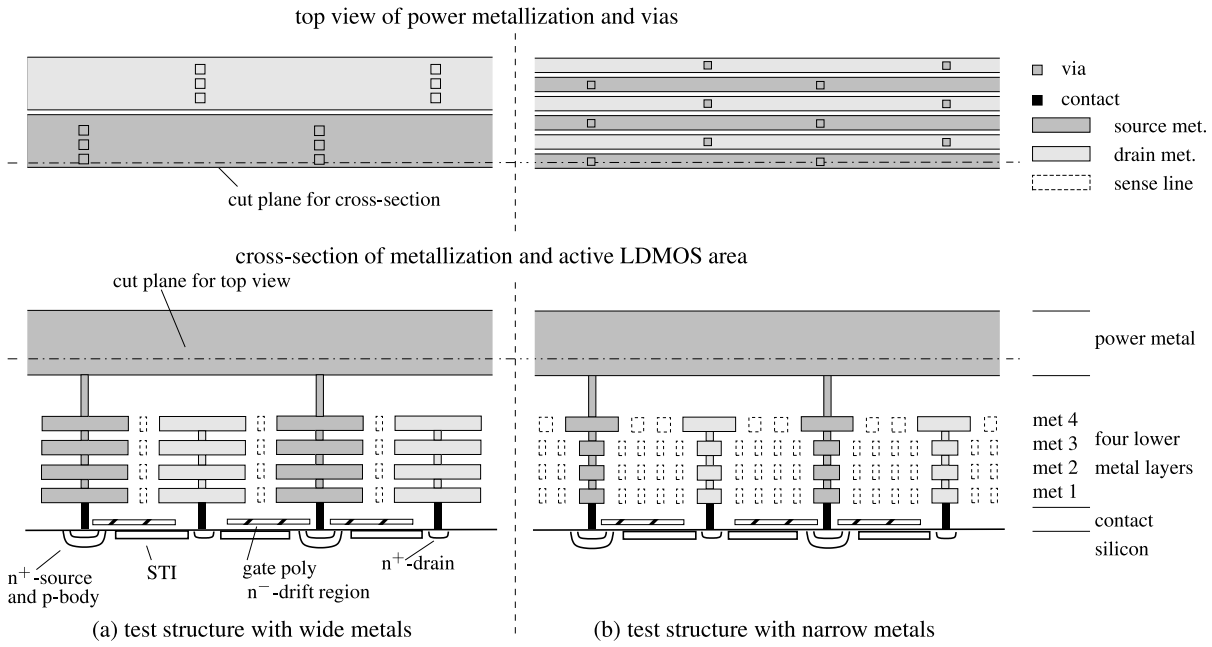

Fig. 2. Top view and cross-section of metallization and active LDMOS area of a test structure with (a) wide metals and (b) narrow metals. The figures are not to scale. The upper layer in the cross-section is the thick power metal, below are the four thinner lower metal layers and the silicon. Variants with and without floating sense lines (shown here with dashed lines) were fabricated.

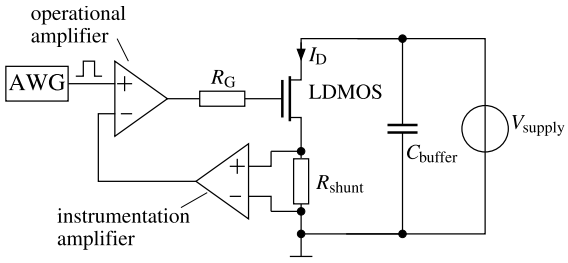

Fig. 3. Simplified schematic of the test setup used to stress the LDMOS. The instrumentation amplifier and the operational amplifier driving the gate via R_G form a feedback loop that keeps the drain current I_D (measured from the voltage drop over R_{shunt}) at the level defined by the output voltage of the arbitrary waveform generator (AWG). The large capacitor C_{buffer} provides the energy necessary for the pulses.

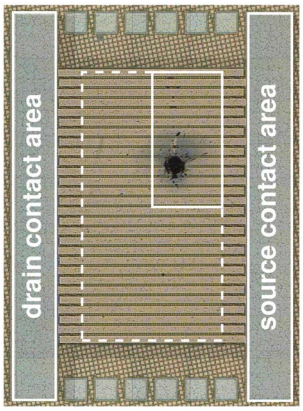

Fig. 4. Typical burn mark indicating the failure location of a device under test. The white dashed rectangle shows the heating area as in Fig. 1. The white solid rectangle represents the part of the device which is used for the simulation described below in Section III.

this, meshing complexity is greatly reduced, so that a simulation of the whole structure can be done quickly. From this, the critical regions are identified, i.e., those where peak values of the von Mises strain are reached, which is where the failure will occur.

2) Step (Detailed Simulation): The stress and strain in the metallization are then investigated by a detailed simulation. Here, only the critical regions are simulated, but now taking all details into account, i.e., without homogenization. The boundary conditions are taken from the coarse simulation [see the red boxes in Fig. 7(b)]. Since only a small part of the device is investigated, a short calculation time can be achieved even though a high spatial resolution is used.

B. Homogenization

The homogenization procedure used in this paper is explained with the help of the structure in Fig. 8, containing n stacked layers of volume V_i each. If a force is applied in x- and y-direction, the strain ($\frac{\Delta l_x}{l_x}$ or $\frac{\Delta l_y}{l_y}$) is assumed to be the same for all layers. Then, the total force F results as

$$F = F_1 + F_2 + \cdots + F_n. \tag{1}$$

TABLE I
CYCLES UNTIL 50% OF THE INVESTIGATED SAMPLES FAILED FOR THE INVESTIGATED TEST STRUCTURE VARIANTS

	with sense lines	without sense lines
wide metals	20,000	18,000
narrow metals	59,000	128,000

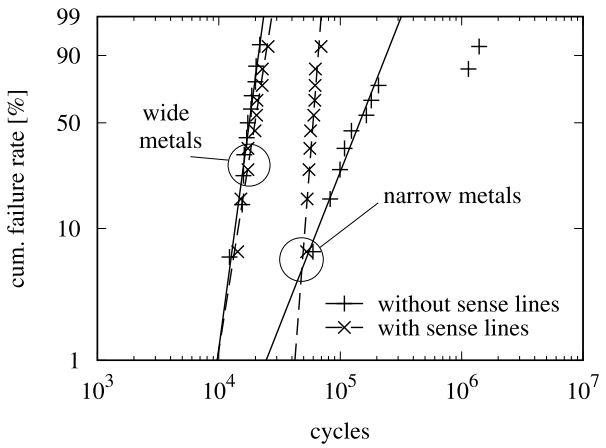

Fig. 5. Weibull plot for the lifetime of the test structures with wide and narrow metals, see Figs. 2(a) and 2(b), with and without sense lines. For a better presentation only half of the measured samples are marked on the graph.

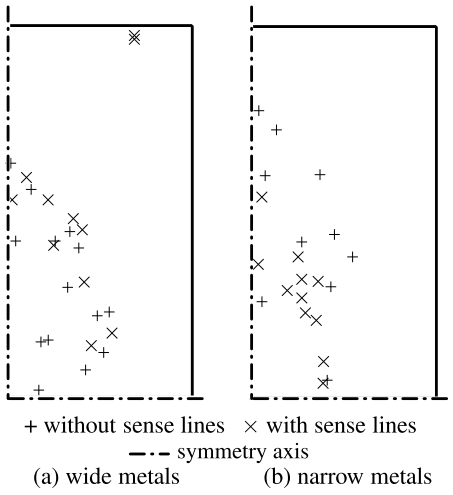

Fig. 6. Measured failure locations for the test structures with (a) wide metals and (b) narrow metals. Due to symmetry, all results are mapped into the upper right quarter of the test structure (see the white solid rectangle in Fig. 4). Different symbols are used for the variants with and without sense lines. Note that only 46 samples are shown because not all samples were photographed.

This is illustrated by Fig. 8a. In z-direction, the total force of each layer is the same, i.e.,

$$F = F_1 = F_2 = \cdots = F_n. \tag{2}$$

Then,

$$\Delta l = \Delta l_1 + \Delta l_2 + \cdots + \Delta l_n. \tag{3}$$

On the basis of these equations, the material parameters of the homogeneous equivalent layer are obtained as in Tab. II with the help of Hooke's law [18] for a structure as in Fig. 8. The homogenization approach applied here has been proven effective in mechanical engineering for many years (see [18]).

The simple structure shown in Fig. 8 varies only in one dimension, which does not hold for the typical LDMOS metallization of Fig. 2. However, it should be noted that the homogenization procedure described above can be applied nonetheless by hierarchically selecting and homogenizing parts that vary only in one dimension. For example, a layer

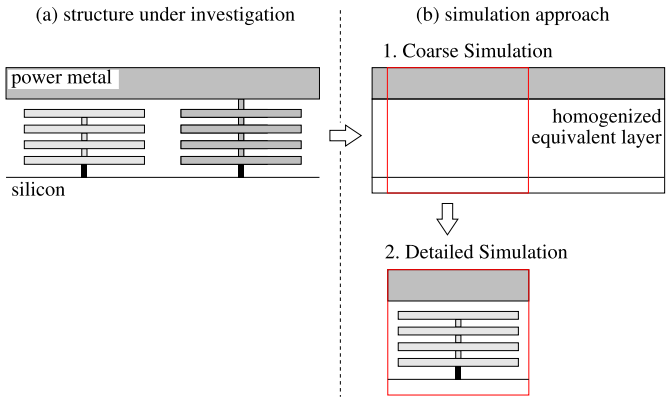

Fig. 7. Overview of the proposed approach. The structure under consideration is shown in (a), the simulation flow in (b). First, a coarse simulation is carried out with a homogenized equivalent layer replacing the complex metallization layers. Then, a second detailed simulation is performed for a small subset of the structure. The boundary conditions (red boxes) are taken from the coarse simulation.

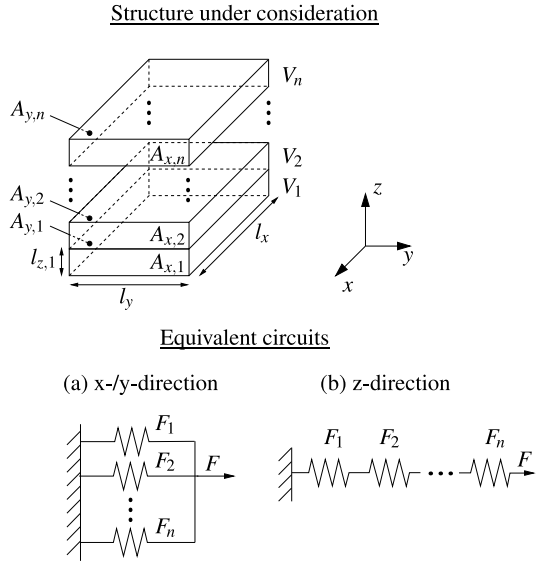

Fig. 8. Explanation of the homogenization for a structure consisting of n layers with volume V_i each. The face sides are denoted by $A_{x,i}$ and $A_{y,i}$, the lengths by $l_{z,i}$.

consisting of a via array as shown in Fig. 9(a) cannot be homogenized in one step. In this case, an intermediate step is required to obtain an equivalent homogeneous layer. First, each via row (the vias and the oxide in between) is replaced by a stripe of homogeneous material, leading to Fig. 9(b). Then, these stripes are merged with the remaining oxide, and a homogeneous layer results as shown in Fig. 9(c). A similar approach is also used for the four thin metal layers, eventually resulting in a layered structure similar to Fig. 8, which can then be homogenized as discussed above.

C. Material Properties

Most materials are considered in the simulation with an anisotropic elastic and temperature-dependent material model. This simplification is acceptable because some materials are brittle (silicon and silicon oxide) and there is no plastic deformation during device life. (If they break, failure is

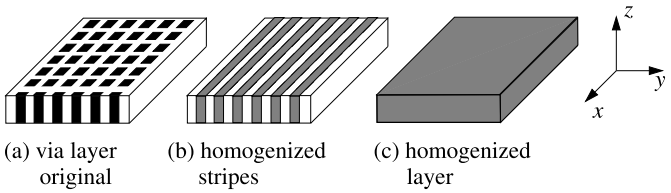

Fig. 9. Explanation of the homogenization for a via layer. Figures are not to scale.

TABLE II
EQUATIONS USED FOR THE HOMOGENIZATION

Parameter	x-direction (y-direction similar)	z-direction
Elastic modulus E	$E_x = \sum_{i=1}^{n} E_{x,i} \frac{A_{x,i}}{A_{x,tot}}$	$E_z = \frac{1}{\sum_{i=1}^{n} \frac{l_{z,i}}{E_{z,i} l_{z,tot}}}$
Poisson ratio ν	$\nu_{\parallel} = \sum_{i=1}^{n} \nu_{x,i} \frac{A_{x,i}}{A_{x,tot}}$	$\nu_{\perp} = \nu_{\parallel} \frac{E_z}{E_x}$
Density ρ	$\rho = \sum_{i=1}^{n} \frac{V_i}{V_{tot}} \rho_i$	
Thermal expansion coefficient α	$\alpha_x = \sum_{i=1}^{n} \alpha_{x,i} \frac{A_{x,i} E_{x,i}}{A_{x,tot} E_x}$	$\alpha_z = \sum_{i=1}^{n} \alpha_{z,i} \frac{l_{z,i}}{l_{z,tot}}$
Specific heat capacity c	$c = \frac{\sum_{i=1}^{n} \rho_i c_i l_{z,i}}{\sum_{i=1}^{n} \rho_i l_{z,i}}$	

$$A_{x,tot} = \sum_{i=1}^{n} A_{x,i} \text{ (see Fig. 8)}$$
$$\text{similarly, } l_{z,tot} = \sum_{i=1}^{n} l_{z,i} \text{ and } V_{tot} = \sum_{i=1}^{n} V_i.$$

imminent.) Other materials have a significantly higher yield strength than aluminum (in this work tungsten and copper) so that their plastic properties can also be neglected. Contrary to that, the lower metal layers mainly consist of aluminum which is ductile (plastic deformation is possible without breaking). An anisotropic, temperature-dependent, and plastic behavior (Chaboche) material model is used, which is based on [19] and [20].

IV. SIMULATION RESULTS

Due to the symmetry of the test structure, only one quarter of the geometry is simulated as shown by the white rectangle in Fig. 4. The test structure can move freely in the simulation, similar to the measurements where the low force of the vacuum cannot hold the wafer firmly on the wafer prober chuck.

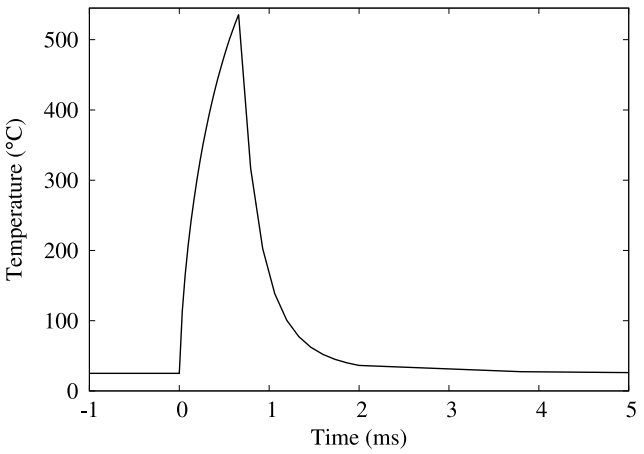

Fig. 10. Peak temperature in the LDMOS over time. The 50 W pulse is turned on at 0 ms and turned off after 0.66 ms. After the pulse, the device temperature drops quickly to 25 °C as imposed by the chuck of the wafer prober. (Note that this plot shows only the first few milliseconds for clarity.)

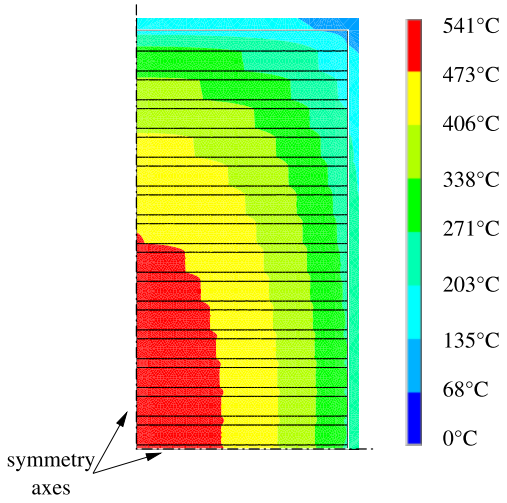

Fig. 11. Temperature distribution in the lower metal layer 4 (see Fig. 2) after a 0.66 ms long 50 W pulse shown for the test structure with wide metals. Only the right upper quarter is shown due to symmetry. The black lines denote the thick power metallization, see also Fig. 1.

A. Temperature

First, a temperature simulation is carried out to determine the temperature throughout the structure as a function of time. These results are required for the subsequent thermo-mechanical simulations. With the heating pulse of 50 W for 0.66 ms as in the experiments at room temperature, a peak temperature of 541 °C is obtained, see Fig. 10. This slightly overestimates the measurement results of 500 °C, see [14]. This is due to the homogenization of the thin metal layers, vias, and contacts, necessary for fast simulations as discussed before. The wafer is placed on a temperature-controlled chuck, causing the device temperature to quickly drop to the chuck temperature of 25 °C within the 19.34 ms long cooling phase so that no gradual increase of the wafer temperature is observed. Hence, the temperature profile is the same for all heating cycles, taking into consideration that the degradation of the metal layers does not noticeably affect the main heat dissipation path through the bulk substrate.

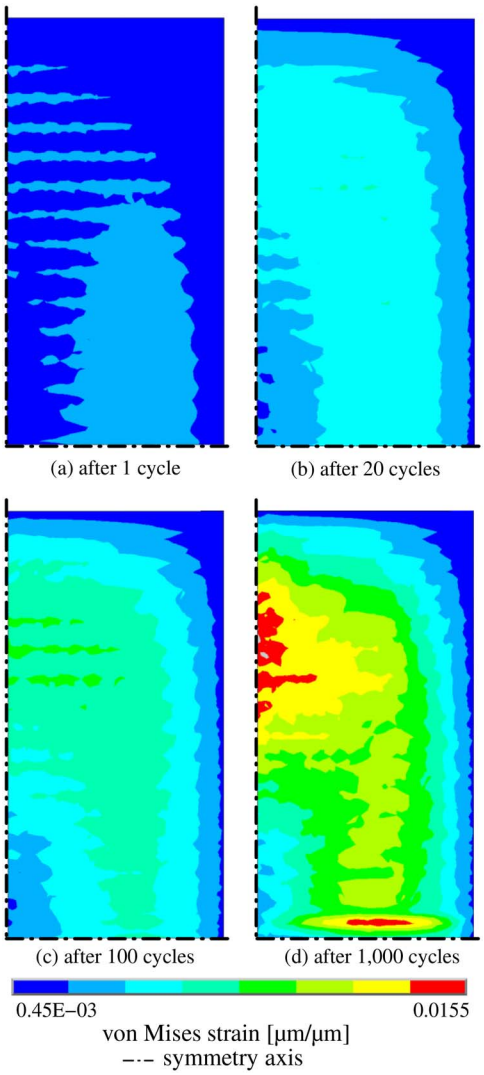

Fig. 12. Von Mises strain in the metal layer 4 for the upper right quarter (see Fig. 4) of the test structure with wide metals and without sense lines, see Fig. 2(a). Shown are the results of the coarse simulation at the end of the cooling time after (a) 1, (b) 20, (c) 100, and (d) 1,000 heating cycles. The horizontal stripes correspond to the power metallization, see also Fig. 11.

Note that the device is operated at the temperature compensation point where the LDMOS current density does not depend on the device temperature (see [21]). Hence, the power dissipation density is uniform, and the peak temperature is observed in the center of the test structure as expected due to symmetry. This is also confirmed by the numerical simulation result in Fig. 11. The temperature contours are ragged because of the power metallization layout with its alternating copper and silicon oxide stripes, see Fig. 1 and the top view in Fig. 2(a). Note that the temperature distributions of all test structures are nearly identical, the influence of the metal layout is negligible.

At the end of the chip fabrication, there is a tempering step at 175 °C so that the structure is stress-free at this temperature. This has been considered in the thermo-mechanical simulation by an initial temperature step from 175 °C down to the chuck temperature of 25 °C.

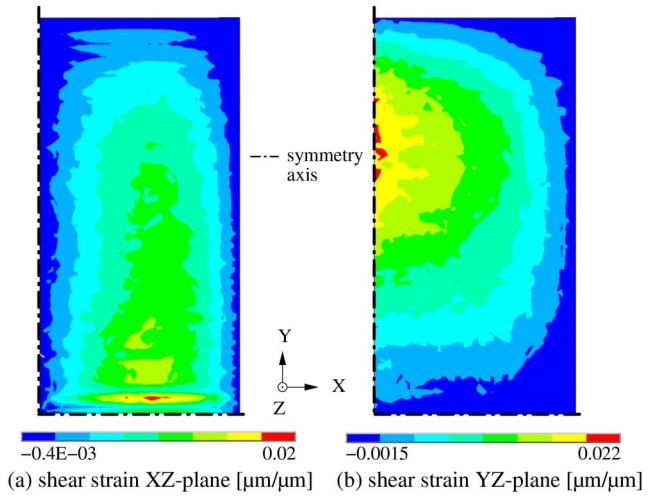

Fig. 13. Shear strain in (a) the XZ- and (b) the YZ-plane direction. Shown are the values after 1,000 cycles, corresponding to Fig. 12(d).

B. Coarse Simulation Results

Using the temperature data calculated above, the mechanical stress and strain are now determined with a *coarse simulation*, i.e., the lower metal layers, vias, and contacts are replaced by an equivalent homogeneous layer as described in Section III-B. The thermo-mechanical stress due to the heating pulses is sufficiently large to cause plastic deformation which will grow with every cycle. Fig. 12 shows the von Mises strain after 1, 20, 100, and 1,000 heating cycles as obtained at the end of the cooling phase as in [4]. It can be seen that the areas with higher von Mises strain assume an elliptic shape after 20 cycles. The elliptic shape can be explained by closely inspecting the simulation results and is due to the shear strain in XZ- and YZ-plane directions, see Fig. 13, agreeing with the observation in [1] that the shear stress causes this elliptic shape. It should be noted that such a coarse simulation is very fast, requiring only 112 min for 20 cycles of a test structure with wide metals even though 30 time steps are used per cycle.

The simulated strain distribution is confirmed by the experimental results of Fig. 6. Only very few failures were observed close to the center of the device. (Note that only the upper right quarter is shown in Fig. 6 and Fig. 12. The device center is at the intersection of the symmetry axes.) The majority of the burn marks agrees well with the areas with higher strain, being arranged on an elliptic shape, see Figs. 12(b) - 12(d). It is important to note that multiple cycles are required for this shape to emerge, only one cycle is not sufficient as shown by Fig. 12(a). Hence, the built-up of plastic deformation is crucial and must clearly be considered in the simulation.

Since the simulation time is short, the von Mises strain can be easily calculated for multiple heating pulses. In Fig. 14, the peak values over 100 consecutive cycles are plotted for all four test structures. The lowest peak value occurs for the test structure with narrow metals and no sense lines. This corresponds well with the experiments (see Fig. 5 and Tab. I), where this variant has the highest lifetime. In addition, the simulation predicts that the test structure with narrow metals and sense lines has a higher strain and is therefore less robust than the

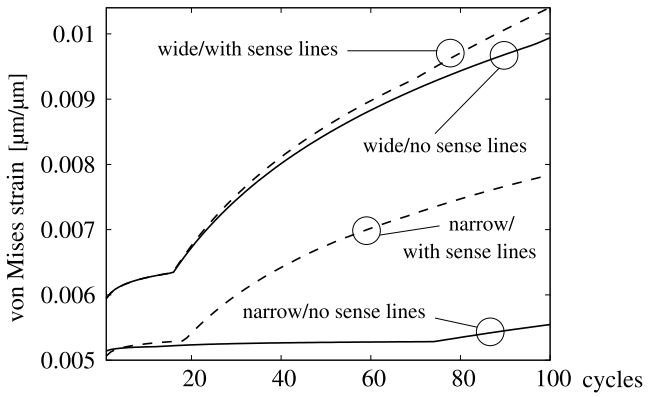

Fig. 14. Peak von Mises strain of all four test structures over 100 cycles. All curves have a bend after the first few ten cycles because the position where the peak value occurs changes (in this case from the power metal to the homogenized layer).

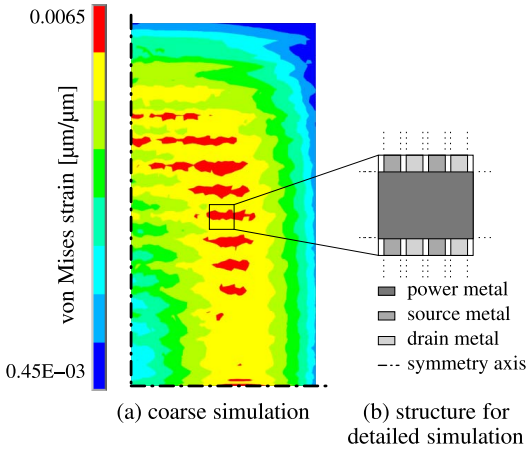

Fig. 15. Plot (a) shows von Mises strain results from a coarse simulation after 20 cycles as already presented in Fig. 12(b) but now with a different scale. Only the enlarged part on the right side (b) is considered in the detailed simulation.

variant without sense lines, but still better than the variants with wide metals which reach even higher strain values. This is also clearly confirmed by the measurements.

The higher lifetime of the test structures with narrow metals can be explained by considering the metal content. The percentage of soft metal is higher for the test structure with wide metals, which lowers the overall stiffness and is reflected in the shorter lifetime. This is more important than using interdigitated structures where metal and oxide are tightly coupled, which is often recommended to improve lifetime.

C. Detailed Simulation Results

With the coarse simulation, the location of the failure can be predicted. Moreover, the results of the coarse simulation give a good indication of the impact of the metallization layout on the lifetime. However, to calculate more accurate results as required for a qualitatively correct prediction of lifetime, a detailed simulation is needed as described in Section III. For this, the location where the von Mises strain reaches its peak value in the coarse simulation is identified and investigated by a detailed simulation. As mentioned before, the device is expected to fail in this location. Accordingly, if several regions with similar peak values are found, it is sufficient to consider only one as the detailed simulations would yield similar results.

Here, only a small part (19.32 µm × 22.19 µm × 8.25 µm) of the device is simulated, but now all metal layers and vias are correctly considered (no homogenization is applied anymore), see Fig. 15. The simulation takes ≈25 min. for the test structures. Simulations of larger parts as in Fig. 15 yield similar results showing that it is sufficient to consider only comparatively small parts in the detailed simulation.

Note that no transient simulation is needed (contrary to the coarse simulation). In this work, only the state at the end of the cooling phase is calculated in the detailed simulation, in agreement with [4]. It should be noted that the strain at the end of the heating phase when the device reaches the peak temperature is higher. Nevertheless, in the authors' opinion the strain at the end of the cooling phase is a better indicator for the

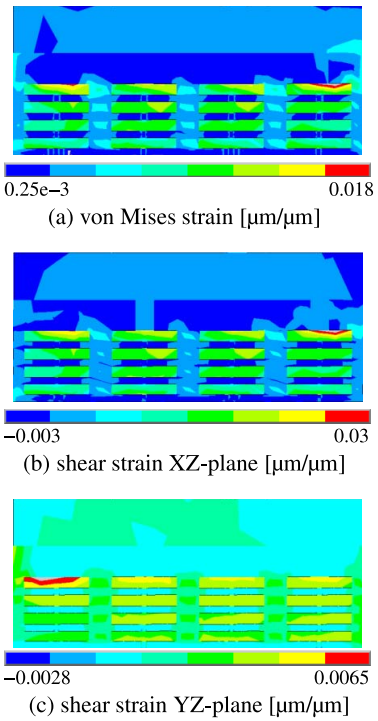

Fig. 16. Detailed simulation results of the test structure with wide metals without sense lines as shown in Fig. 2(a). Plot (a) shows the cross-section results of von Mises strain, (b) the strain in XZ-plane direction, and (c) the strain in YZ-plane direction after 20 cycles. Note the different scaling of the strain values.

growing degradation of the metallization because it increases over many pulses in our simulations, whereas the strain at peak temperature does not change significantly, remaining almost constant.

The results for the structure with wide metal without sense lines, see Fig. 16, show that the maximum von Mises strain occurs in the lower metal layer 4. This failure location has been confirmed experimentally, see [16], and also agrees

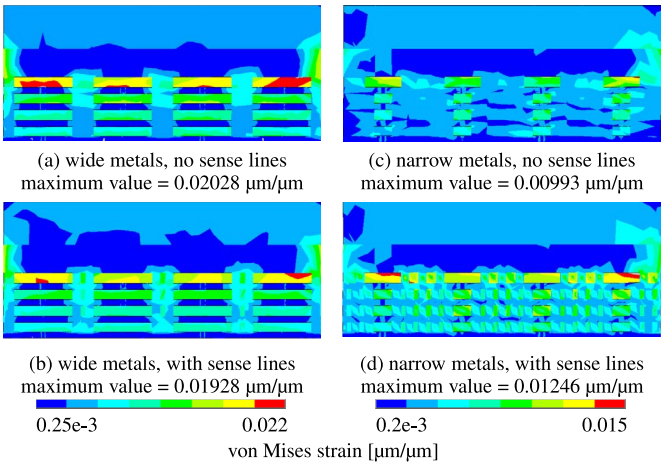

Fig. 17. Detailed simulation results of von Mises strain for the test structure variants with wide and narrow metals, see Fig. 2(a) and (b), with and without sense lines. Shown is the von Mises strain after 100 cycles. The peak values are given in the subplot captions.

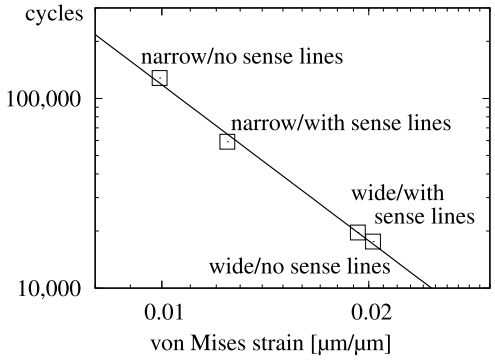

Fig. 18. Comparison of measured and modeled lifetime. The four symbols show the measured average cycle number until failure as extracted from Fig. 5 for the four test structure variants. They are plotted over the von Mises strain as determined from the detailed simulation of Fig. 17. The fit with the lifetime model is shown with a solid line. The coefficients of (4) are $C_1 = 0.4937$ and $C_2 = -2.6815$.

with [2] and [4]. As before, the shear strain, here in XZ-plane direction, is the main factor for failure, as already observed in [1].

Considering the results of the detailed simulations for all investigated test structures, it is observed (and also confirmed by experiments, see [16]) that failure always occurs in the metal layer 4 where the von Mises strain has the highest value, see Fig. 17. Furthermore, the detailed simulation results (see subplot captions of Fig. 17) show that the test structures with narrow metals have lower von Mises strain values than the structures with wide metals, agreeing with the coarse simulation. Moreover, the structure with wide metal and sense lines has now a lower strain than the variant without sense lines. This matches with the experiments – contrary to the coarse simulation where the variant with sense lines has a higher strain, see Fig. 14. This demonstrates that the detailed simulation is required for accurate results.

The test structure with wide metal and sense lines has a slightly lower strain and thus higher lifetime than the variant without sense lines. For wide metals, sense lines do not change the metal content significantly. Now, the additional metal/oxide interdigitation of the sense lines improves the stability so that the lifetime is slightly increased.

V. Application to Lifetime Prediction

Most lifetime predictions made today are based on the *temperature* change ΔT, as, e.g., in [3]. But, it is important to note that considering only the temperature is not sufficient to explain the large lifetime variations observed for the test structures because they all have almost the same ΔT, see Section IV-A. However, using results from the detailed thermo-*mechanical* simulation should enable a physics-based and thus more accurate lifetime prediction. This will be investigated now.

For active power cycling where repetitive heating and cooling cause plastic deformation, strain-based fatigue models should be used [22]. They commonly have the form of a simple power law, see [23], e.g., the well-known empirical Coffin-Manson model. Since the von Mises strain has been used in the coarse simulation to identify the regions that are expected to fail first and are, therefore, investigated in the detailed simulation (see Section III-A), the von Mises strain, denoted below as ε_{vM}, will also be used as parameter in the lifetime model

$$N = C_1(\Delta\varepsilon_{vM})^{C_2} \tag{4}$$

where N is in this work the average cycle number to failure and C_1 and C_2 are fitting coefficients.

The plot in Fig. 18 shows that the lifetime model fits the measurements very well. This confirms that the von Mises strain is a suitable parameter to explain the different lifetimes observed for the four test structure variants, contrary to the temperature change ΔT as discussed above.

VI. Conclusion

This paper presents an efficient simulation approach for thermo-mechanical stress in the on-chip metallization of integrated power semiconductors. This can be achieved by a simplified coarse simulation identifying the regions with the highest stress and a subsequent detailed simulation of only those regions.

The approach was verified experimentally by test structures with different metallization layouts. The failure locations were correctly predicted. Moreover, the simulation results indicate that the highest stress occurs in the upper of the thin metal layers, which was also confirmed by the measurements. In addition, the different lifetimes of the test structures could be explained. It was shown that the content of soft metal is more important than using interdigitated layouts.

The results also clearly demonstrate that the metallization layout affects the lifetime drastically. This cannot be accounted for from the temperature change alone. Hence, a thermo-mechanical simulation as presented in this paper is mandatory to correctly predict lifetime and to optimize the layout. A strain-based fatigue model was evaluated and shown to match well with the experiments.

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