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INKJET PRINTED METAL OXIDE THIN FILM TRANSISTORS INCORPORATING POLYETHYLENEIMINE

Master´s Programme in Chemical, Biochemical and Materials Engineering
Major in Chemistry

Master's thesis for the degree of Master of Science in Technology submitted for inspection, Espoo, June 27th 2017.

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Title of thesis Inkjet Printed Metal Oxide Thin Film Transistors Incorporating Polyethyleneimine

Degree Programme Chemical, Biochemical and Materials Engineering

Major Chemistry

Thesis supervisor Professor Antti J. Karttunen

Thesis advisor(s) / Thesis examiner(s) D. Sc. (Tech.) Ari Alastalo

Date 27.06.2017 **Number of pages** 79 **Language** English

Abstract

Fully inkjet printed fabrication of thin film transistors (TFTs) is desirable to enable reproducible, high throughput, low cost production of electronics under mild conditions. However, TFT devices fabricated from printable materials typically exhibit inferior performance to those of non-printed. For example, there is a lack of well performing source-drain electrode materials for metal oxide semiconductors. In contrast to vacuum-deposited Al, printed Ag has a high contact resistance and work function, with poor charge carrier injection to the semiconductor. Therefore, there is a requirement to improve electrical performance of TFTs incorporating printed electrode material such as Ag. The approach to achieve this through this work is by inclusion of an inkjet printed thin film of polyethyleneimine (PEI) at the interface between semiconductor and source-drain contacts. PEI contains tertiary amine groups, which possess lone pairs of electrons available to assist charge injection and lower the interfacial resistance.

Two sets of reference devices were prepared, both with inkjet printed In_2O_3 semiconductor. One set was fabricated by vacuum deposition of Al for source drain electrodes, the other set with inkjet printed Ag source drain contact electrodes. The solution-based processing method limits the thermal budget to 300°C. Devices with Al electrodes provided charge carrier saturation mobility (μ_{sat}) of 4.3 ± 0.93 $cm^2\ V^{-1}\ s^{-1}$, whereas those with Ag contacts exhibited an expected lower μ_{sat} of $8.0 \cdot 10^{-3} \pm 3.9 \cdot 10^{-3}\ cm^2\ V^{-1}\ s^{-1}$. Addition of an inkjet printed interfacial thin film containing PEI between the semiconductor and Ag contact electrodes significantly increased the μ_{sat} to 3.1 ± 0.53 $cm^2\ V^{-1}\ s^{-1}$.

Interfacial engineering in this work yielded TFTs possessing printed Ag contacts that display electrical performance comparable with devices incorporating vacuum-deposited Al contacts. The impact of this result is the possibility for high performance fully printed TFTs. Development of this fabrication route might facilitate low temperature solution based roll-to-roll production of electrical components containing fully inkjet printed TFT devices.

Keywords Polyethyleneimine, indium oxide, thin film transistor, inkjet printing.

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Preface

This research was undertaken as part of the EU ROLL-OUT project at VTT Technical Research Centre of Finland, Espoo, from January to June 2017. I am very grateful to Dr. Maria Smolander for this opportunity, and thankful to the entire Printed Sensors and Electronic Devices team for such a warm welcome. Particular gratitude is extended to Mr. Kim Eiroma for his inkjet advice.

I am indebted to Dr. Jaakko Leppäniemi for patiently taking me under his wing to show me the ropes and guide me through all avenues of this work.

I wish to thank my thesis advisor Dr. Ari Alastalo for driving this research forward with his encouragement, advice, and key ideas.

The enthusiasm and willing assistance of my thesis supervisor Prof. Antti J. Karttunen is gratefully acknowledged.

Finally, thank you to my family for backing my decision to pursue this path. Most importantly, this work would not have been possible without the boundless support from my partner Sofia.

Liam Gillan

Espoo, June 27th 2017

Symbols and abbreviations

Symbol	Description
μ	Charge carrier mobility
μ_{eff}	Effective mobility
μ_{FE}	Field effect mobility
μ_{sat}	Mobility in saturation regime
C_G	Gate capacitance
C_{GD}	Gate-drain capacitance
C_{GS}	Gate-source capacitance
C_{OV}	Overlap capacitance
C_{OX}	Gate dielectric capacitance
E	Young's modulus
f_T	Transit frequency
g_d	Drain conductance
g_m	Transconductance in saturation regime
I_D	Drain current
$I_{D.lin}$	Drain current in linear regime
$I_{D.sat}$	Drain current in saturation regime
I_G	Gate current
I_{ON}/I_{OFF}	Current on/off ratio
k	Dielectric constant
l	Inkjet nozzle diameter
L	Thin film transistor channel length
$L_{OV,TOT}$	Total overlap length between gate-source
Oh_n	Ohnesorge number
R_c	Contact resistance
R_{ch}	Channel resistance
Re_n	Reynolds number
R_T	Total resistance
S	Sub threshold swing
T_g	Glass transition temperature
v	Velocity
V_D	Drain voltage
V_G	Gate voltage

V_{hyst}	Hysteresis voltage
V_{on}	Turn on voltage
V_{th}	Threshold voltage
W	Thin film transistor channel width
We_n	Weber number
Z	Z parameter of printability
γ	Surface tension
$\Delta G_f°$	Gibbs free energy of formation
η	Viscosity
θ_C	Contact angle
ρ	Density
σ_{LS}	Liquid-substrate surface energy
σ_{LV}	Liquid-atmosphere surface energy
σ_{SV}	Substrate-atmosphere surface energy

Abbreviation	**Description**
2-ME	2-methoxyethanol
ACE	Acetone
a-MOS	Amorphous metal oxide semiconductor
ASCC	Automatic Sequence Controlled Calculator
AZO	Aluminium-zinc oxide
CBM	Conduction band minimum
CTE	Coefficient of thermal expansion
CVD	Chemical vapour deposition
DC	Direct current
DIW	Deionised water
DOD	Drop on demand
DOS	Density of states
EG	Ethylene glycol
FET	Field effect transistor
HDPE	High-density polyethylene
IGZO	Indium-gallium-zinc oxide
IPA	Isopropyl alcohol
ITO	Indium-tin oxide
IZO	Indium-zinc oxide
LCD	Liquid crystal display
MOS	Metal oxide semiconductor

MOSFET	Metal oxide semiconductor field effect transistor
OLED	Organic light emitting diode
PEI	Polyethyleneimine
PEN	Polyethylene naphthalate
PET	Polyethylene terephthalate
PTFE	Polytetrafluoroethylene
PVD	Physical vapour deposition
PVP	Polyvinylpyrrolidone
SAM	Self-assembled monolayer
TCO	Transparent conducting oxide
TGA	Thermogravimetric analysis
TFT	Thin film transistor
VBM	Valence band maximum
VTFT	Vertically aligned thin film transistor

Chapter 1

Introduction

Electronic devices have evolved significantly since the mid-20th century. From machines reliant on bulky electromechanical components, such as IBM's enormous 16 m long 4500 kg Automatic Sequence Controlled Calculator (ASCC) (Figure 1), to miniaturised integrated circuit technologies like smart phones, with the latter providing superior computing performance. [1] An electrical component called a transistor is chiefly responsible for the significant reduction in size and increased performance of contemporary electronics.

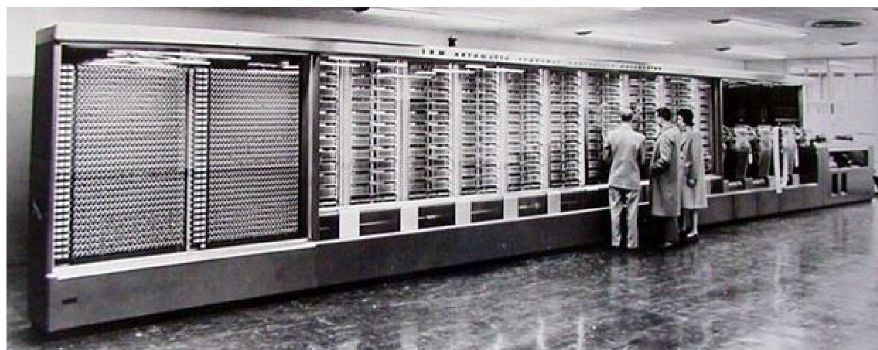

Fig. 1. IBM's ASCC at Harvard's Cruft Laboratory in 1948. A machine with inferior computing capacity to a modern pocket sized smart phone. [1]

Thin film transistors (TFTs) are a rapidly developing area of transistor electronics. Semiconductor materials are active components in TFTs, with metal oxide semiconductors (MOS) such as In_2O_3 recently drawing attention. [2] Conventional TFT devices fabricated from Si semiconductors [3] are rapidly becoming surpassed by MOS TFT devices in the search for high performance materials to suit applications requiring flexibility and transparency. [4] Amorphous MOS (a-MOS) are of particular interest because they possess high charge carrier mobility via s-band conduction [5,6] and avoiding undesirable scattering resulting from crystalline grain boundaries. [7,8] a-MOS materials reportedly possess smooth surfaces, limiting interfacial traps and scattering of charge carriers. [9] Formation of amorphous In_2O_3 is possible by controlled annealing. [2]

Inkjet printing is a route for accurate, repeatable patterning of TFT components including In_2O_3 on varied substrates, with potential for scaling up to roll-to-roll production. [10]. Fully inkjet printed TFT fabrication is high throughput and avoids cumbersome processes such as vacuum evaporation of source-drain electrode material. Unfortunately, there are limitations to materials suitable for inkjet printing as source-drain electrodes. For example, Ag is printable but has a low work function, commonly resulting in poor charge injection and high interfacial contact resistance when coupled to oxide semiconductors. [11] Polyethyleneimine (PEI) is an adhesion promoter material with lone electron pairs on tertiary amines to enable charge injection. [12] Applying a thin PEI layer (Figure 2) may lower the interfacial resistance between In_2O_3 and Ag by n-doping the semiconductor via electron donation and covalently bonding with the Ag. This interfacial bridging layer of PEI might enhance electrical performance, providing a pathway to satisfying demand for fully printed TFTs.

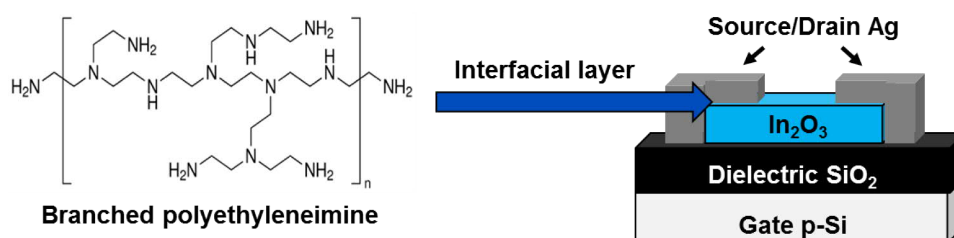

Fig. 2. Schematic concept of polyethyleneimine as an interfacial layer in a thin film transistor.

The research question this work aims to answer is whether PEI might enhance the electrical properties of TFTs with printed Ag source-drain contacts. The approach focuses on solution based TFT device fabrication by inkjet printed deposition of sequential thin films.

This thesis contains five chapters. First, a literature survey describes the background of the topic. Subsequently the experimental methods are detailed, followed by presentation and critical discussion of the results. The thesis concludes with a summary of the work and proposed outlook for further research.

Chapter 2
Background

2.1 Thin film transistor fundamentals

A transistor is an electrical device that can switch an electrical signal between an off or on state. Ideally, a transistor switch device will provide either infinite resistance in its off condition (open circuit) or zero resistance in its on condition (short circuit), without any intermediate. Used as a switch a transistor can implement digital logic gates and as a result is a fundamental component of complex digital electrical systems. [13]

Field effect transistors (FET) are a class of transistors that rely on device control by applying an electric field. An FET device contains three conductive terminal electrodes; gate, source, and drain. In addition to these, devices typically contain semiconducting and dielectric/insulating materials. A TFT is an FET device comprising stacked thin films. [14] There are varied options for arrangement of TFT device components (detailed in Section 2.3), including the bottom-gated structure presented in Figure 3a below, depicting the mechanism of field effect in a TFT. This example of bottom-gated configuration shows stacked layers of a gate electrode at the base of the device, followed by dielectric, semiconductor, and source/drain electrodes, respectively. Applying positive voltage between the gate and source (V_G) creates an accumulation of free charge carriers in the semiconductor material near the semiconductor/ dielectric interface (Figure 3b). This accumulation towards the gate contact occurs because of charge carrier attraction to the applied electric field, known as the field effect. [15] Application of V_G results in polarisation of the dielectric material to provide slight surface charge. Free charge carriers in the semiconductor are attracted to the polarised dielectric and accumulate near the interface of the two materials. Accumulated charge carriers allow control of current through the semiconductor channel* by applying voltage between the drain and source (V_D). [16] The number of charge carriers accumulated near the interface is proportional to V_G.

* Channel length and width are defined as the gap between and width of source-drain contacts, respectively.

This means the channel thickness and width (W) of the accumulated charge carriers depends on the applied voltage. Greater V_G results in channel broadening (to a certain extent) and greater possible conductance between drain and source. Ideally there is no current from drain to source (I_D) when V_G = zero (other than negligible amount of saturation current from minority charge carriers). When V_G is gradually increased > zero and V_D maintained fixed > zero, current will begin to flow between the drain and source when a given V_G is reached. This amount of V_G is threshold voltage (V_{th}). [16] Where $V_G < V_{th}$, I_D = zero. In this state, the TFT device is off. Where $V_G > V_{th}$, the device is capable of I_D > zero. In this state, the device is on. [17] Thus explaining how a TFT may act as a switching device for I_D. A quirk of history resulted in Benjamin Franklin assigning current flow from positive to negative charge. It is important to realise that electrons flow in the opposite direction, towards positive charge. In the case where majority charge carriers are electrons, they are injected at the source electrode and flow towards the drain.

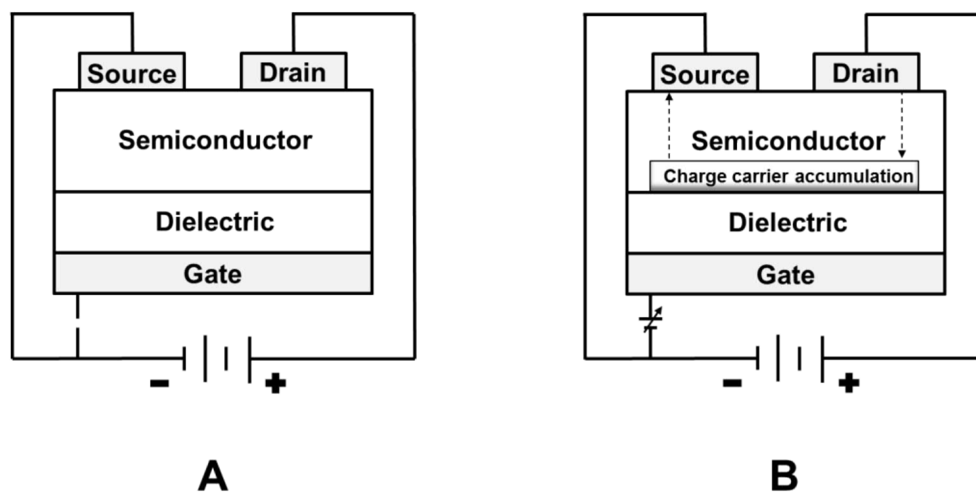

Fig. 3. Cross section of a bottom gated thin film transistor switched between an off state (A), or an on state (B) with current from drain to source electrodes controlled by voltage applied from source to gate electrodes, resulting in field effect accumulation of free charge carriers.

Research into solid-state FET devices commenced in the early 20th century. Seminal work was that of concept patents submitted by J. E. Lilienfeld. [18,19] in the 1930's. However, this work was conceptual and the first operational device was a point contact transistor fabricated in 1947 at Bell laboratories by J. Bardeen, W. Brattain and W. Shockley. [20] The team discovered that Au contacts added to a Ge crystal resulted in a signal with a greater output than that of the input signal. This work resulted in the trio being awarded the Nobel Prize in Physics in 1956 "for their researches on semiconductors and their discovery of the transistor effect". [21] The

first reported TFT was in a landmark publication by Weimer in 1962. [22] Weimer used Au contacts, a CdS semiconductor, and SiO dielectric. In 1964, Koelmans reported construction of a transparent SnO_2 semiconductor based TFT. [23] This use of a metal oxide as a semiconductor was the first reported example of a MOS based TFT. At the start of the 21st century, work on ZnO provided reasonable electrical performance from MOS TFT devices. [24-26] In 2003, Nomura et al prepared an $InGaO_3(ZnO)_5$ (IGZO) single crystal thin film transparent channel material which displayed exceptional electrical performance. [27] The following year, Nomura's group reported room temperature fabrication of flexible, transparent TFTs making use of a-MOS materials. [6] Since these milestones, MOS materials for TFTs have been subject to ongoing research.

Solution processing of MOS TFTs promises scalability, opening doors to possibilities for a myriad of practical applications. Emerging applications for electronic devices enabled by TFTs are diverse and include: textile integrated [28] and wearable systems, [29] intelligent packaging, [30], biomimetics, [31] flexible transparent [32] and active matrix displays, [8] X-ray [33] and bio-sensors, [8] and medical tools. [34] These applications require device properties including stability, transparency, and flexibility. TFTs have potential to display all of these properties and their further development is likely to assist consumer demand for a variety of electrical devices. [14,35,36]

2.2 Thin film transistor materials

Constituent materials directly influence the electrical performance of TFT devices. This section introduces semiconductor, dielectric, electrode, and substrate materials for TFTs, detailing materials within the scope of this thesis work.

2.2.1 Semiconductors

TFTs operate based on the field effect on charge carriers in semiconductor materials. This means the semiconductor material is an integral component of a TFT device, ultimately responsible for the level of device performance.

Semiconductor materials possess temperature related electrical conductivity that is opposite to metals. For example, intrinsic semiconductors typically display increasing electrical conductivity relative to elevating temperature as the concentration of charge carriers increases. Metals experience increased resistivity relative to increased temperature because of enhanced electron/phonon interactions

with the metal lattice. Semiconductors have higher electrical resistance than metals, but lesser resistance than insulators. [37] To understand why this occurs, it pays to consider a material's electrons in terms of density of states (DOS). DOS describes the number of available states for electrons to occupy per interval in each energy level. Large DOS means there are a large number of available states for electrons to occupy. In contrast, a DOS of zero means that no electrons may occupy a given energy level. The lowest range of unfilled energy bands (devoid of electrons) is called the conduction band, and the highest range of occupied bands is called the valence band. The range of energy between the valence and conduction bands where no electron states exist is known as a band gap. The band gap is equivalent to the energy required for a charge carrier to move from the valence band to the conduction band. [38] Band gap determines electrical conductivity of solid materials. A large band gap results electrical resistivity, as seen with organic (plastic) or ceramic insulators. Very small or no band gap (overlap of conduction and valence bands) results in the high conductivity possessed by metals. Semiconductors have smaller band gaps than insulators, but larger than metals. Figure 4 below depicts the relation between band gap and conductivity, where the Fermi level describes the energy (at 0 K) below which all of the available states are occupied and above which no states are filled. Where T > 0 K, electrons can be excited into states above the Fermi level as described by the grey shading (Figure 4). In a solid semiconductor at thermal equilibrium, excitation of an electron from the valence band to the conduction band leaves a hole in its wake. [39] Just as electrons are mobile charge carriers, so too are holes. However, where electrons are negative charge carriers, holes are positive charge carriers.

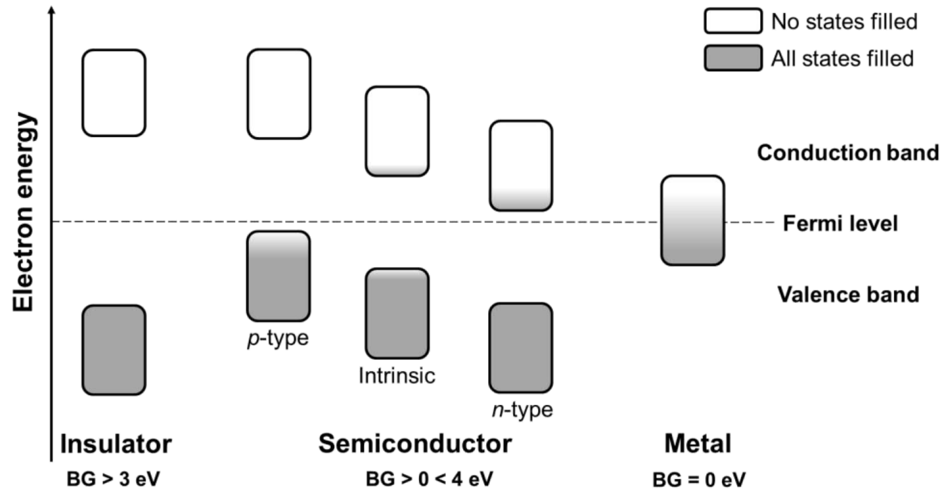

Fig. 4. Band gap (BG) between valence and conduction bands of different materials based on occupation of energy states by electrons.

Figure 4 presents three types of semiconductor, one intrinsic and two extrinsic (*p*-type and *n*-type). Extrinsic semiconductors are doped by the addition of impurity species, altering the concentration of mobile charge carriers at thermal equilibrium. Doped semiconductors are classified as *p*-type or *n*-type according to the concentrations of their dominant charge carriers. Dopant species are either electron donors, or acceptors. Donor dopants have more valence electrons than the species they replace, providing their extra electrons to the material's conduction band and increasing the negative charge carrier concentration of the material. Semiconductor materials with greater concentration of negative charge carriers are classed as *n*-type. Acceptor dopants have less valence electrons than the species they replace, accepting electrons from the material's valence band and increasing the positive charge carrier concentration of the material, making it *p*-type. In contrast to extrinsic semiconductors, the concentration of charge carriers in intrinsic semiconductors is a property of the material itself, not a result of doping. For example, holes in the valence band of an intrinsic semiconductor may result from thermally generated electron excitation to the conduction band, not from electron loss to an acceptor dopant. For *n*-type semiconductors, the Fermi level is closer to the conduction band than the valence band than it is for intrinsic semiconductors. For *p*-type semiconductors, the Fermi level is closer to the valence band than the conduction band. Figure 4 depicts these relations.

Three key groups of TFT semiconductor materials are Si, metal oxide, and organic species. Both Si and organic materials are well-known, widely applied semiconductors in electronic devices. However, these materials have limitations as TFT semiconductors for applications requiring transparency or flexibility such as

displays or sensors. [8] For example, a small bandgap limits optical transparency of Si materials. [6] Si typically requires high temperature processing. In addition, the Young's modulus of Si is high (E = 130-188 GPa) limiting applications requiring device flexibility. [40]

Organic materials such as pentacene or thiophene derivatives allow processing at lower temperatures, display greater flexibility and optical transparency than Si. [11,41] However, a major limiting factor for organic semiconductors in TFTs is their low charge carrier mobility (a measure of electrical performance) causing poor circuit speed and current density. [42] The third key group of semiconductor materials for TFT channels are oxides of post transition metal elements, for example In_2O_3. These MOS materials provide good mobility, [10] can be optically transparent [27] and flexible. [32]

The unoccupied s orbitals of MOS materials facilitate paths for mobile charge carriers. [8] MOS materials may be binary such as In_2O_3, [2] SnO_2 [11] and ZnO. [43] The mobile charge carrier concentration is high for SnO_2 and ZnO, which makes it difficult to control conductance and threshold voltage when used as MOS materials for TFTs that require low electron concentrations. [8] In_2O_3 has a large band gap (> 3 eV), a high intrinsic concentration of mobile charge carriers, with high mobility. [44] These properties have resulted in research of In_2O_3 as an MOS for TFTs since the mid 90's, including providing a host matrix for doping by other species. For example, ternary (e.g. indium-zinc oxide ((IZO)) or quaternary (e.g. indium-gallium-zinc oxide (IGZO)) mixtures of post transition metal cations can show improved device performance over binary MO materials. [45,46] For example, high performance n-type multicomponent systems such as IGZO [6] enable transparent, flexible TFT device production at low temperature. [27] Doping of In_2O_3 with Zn or Ga assists formation of amorphous phase material. This is because the dopant species have a greater affinity for O than In does. [47] Ga-O bonds form in preference to In-O. This process limits formation of oxygen vacancies in the material, in turn limiting generation of mobile electrons, improving device performance. However, high Ga content compromises electron mobility, hence addition of Zn component for stabilisation. [48] a-MOS materials are of particular interest for TFT devices. Electronic structure helps explain why, by considering the bonding differences between Si and oxide materials. In covalently bonded Si, conduction band minimums (CBMs) are formed from antibonding sp^3 orbital states (σ^*), and valence band maximums (VBMs) are formed from bonding sp^3 orbital states (σ) of sp^3 hybridised orbitals. The band gap in Si arises from the energy splitting of σ^* to σ. [47] Conduction band sp^3 orbitals in polycrystalline Si make charge carrier movement directionally limited by bond angles. This means random structure in amorphous Si results in lower charge carrier mobility than for crystalline Si. [6,49] This difference

is significant, with intrinsic crystalline Si exhibiting electron mobility around 1500 times greater than a-Si. [47]

In contrast to the purely covalent bonding in Si, the partly ionic interactions in MO materials provide different properties. In MO materials, the CBM and VBM are commonly formed of different ionic species, explained by the Madelung potential. The Madelung potential is the potential energy felt by a given ion in an ionic lattice resulting from the total electrical field of all the lattice constituent ions. The Madelung potential raises the energy levels in metal cations, and lowers those in oxygen anions. This means the CBM is chiefly empty metal cation s orbitals (available for movement of mobile charge carriers), and the VBM is built from occupied 2p orbitals of oxygen anions. This large Madelung potential helps explain why MOS materials have a large band gap and appear transparent. [47] The CBM s-orbitals of metal cations in a-MOS materials are not spatially dependent due to their isotropic shape. [6] This results in high charge carrier mobilities in s-band conduction, regardless of crystalline phase. The almost spherical s-orbital wave function overlap is insensitive to amorphous random structure. [5] In addition to s-orbital overlap, a-MOS materials possess particularly high mobility by lacking crystalline grain boundaries that cause scattering of charge carriers. [7,8] Another benefit of amorphous phase in contrast to crystalline regions, is device uniformity over an extended range. [49] It is clear that the electrical properties of intrinsic MOS materials may altered somewhat if desired by doping. Research is likely to continue investigation of various dopants for materials with applications in TFTs.

In_2O_3 is the semiconductor selected for TFT devices fabricated during this thesis work. The MOS material is prepared and deposited by inkjet printing as a thin film, building on a recently reported method for intrinsic In_2O_3. [2]

2.2.2 Dielectrics

Overshadowed by the vast research on metal oxide semiconductors, optimisation of dielectric materials for TFTs appears comparatively ignored. [42] This is surprising because the operation of a TFT device relies on accumulation of charge carriers at (or near) the semiconductor/ dielectric interface, where properties of the dielectric material play a role in determining device performance. For example, defects or charge trapping caused by the dielectric material could hinder device performance. [14,17] To alleviate such hindrance, materials with a high dielectric constant (high-*k)* (capacity to retain electric charge) may be desirable. Another benefit of these materials is reduced power consumption in devices by diminishing the driving voltage range. [49] Unfortunately, such materials can exhibit poor electrical

properties [50] and exhibit scattering by possessing grain boundaries due to polycrystallinity. [51,52] One way of incorporating high-*k* materials such as Y_2O_3, [53] HfO_2, [54] or Ta_2O_5, [55] is combining them with traditional dielectrics such as SiO_2 or Al_2O_3 to retain amorphous structure, avoiding grain boundary scattering. This mixed dielectric approach has proven to reduce charge trapping, [56] is compatible with metal oxide semiconductors in TFTs, [57] and has enabled process temperatures as low as 150°C. [58]

Thermally grown SiO_2 on p-Si wafer was the dielectric material used for this thesis work because the Si is a suitable substrate for inkjet printed deposition of subsequent layers. [2]

2.2.3 Contacts

A variety of conductive materials are suitable for gate, drain, and source terminal contact electrodes in TFTs. For example, a study on metals [59] showed varying gate contact material to include Cr, Ti, Cu and Pt had only a minor influence on electrical performance of IGZO TFTs. Many other metals are employed as TFT gate contact materials including Au, [60] Mo, [61] Ni, [62] Al, [63] and metal blends or alloys including TaN, [64] MoTi, [65] and AlNd. [66] In addition to metals, oxide materials find applications as TFT gate contacts. For example, indium tin and zinc oxides (ITO/IZO), [67,68] aluminium zinc oxide (AZO) [69] and In_2O_3. [70] The gate electrode is not required to conduct a large current in a TFT device. Therefore, compatibility with the fabrication process is a limiting factor in determining the choice of gate contact material. [14]

Source and drain electrodes for TFTs require high electrical conductivity and limited contact resistance (R_C) with the semiconductor material. [14] Because metals have high electrical conductivity, they are a common material used for source and drain electrodes in TFTs. Examples include, Mo, [61] Au, [71] Ti, [72] Pd, [73] Cu, [74] and Al. [75] Multi layered contacts are one approach in minimising R_C. This involves depositing a layer of adhesion promoting metal at the semiconductor interface beneath the bulk contact material. For example; Ni/Au, [76] Cr/Au, [77] Mo/Al, [75] and Ti/Au. [78] Unfortunately, metals do not generally provide optical transparency,[†] so transparent conducting oxides (TCOs) ITO [6] and IZO [79] can be used for these applications.

This thesis work aimed to reproduce a reported method for evaporation of Al source/ drain contacts through a shadow mask [10] and then optimise a solution

[†] A notable exception where a metal has provided a transparent electrode is that of inkjet printed arrays of µm sized nanoparticle Ag "coffee rings". [172]

based inkjet deposition of contacts for comparison with evaporated Al. Inkjet printed nanoparticle Ag has been reported previously. [80-91] These reports suggest that inkjet printed Ag can be highly conductive. However, it is difficult to form an ohmic contact with the semiconductor material. To realise ohmic contact, materials need good charge injection and minimal R_C at the contact-semiconductor interface. Suitable source-drain materials ideally have a low work function. Work function is the minimum energy required to remove an electron from a material into vacuum. Ag has a high work function (~ 4 eV), [11] resulting in a poor interfacial interaction when printed on In_2O_3. Another reason for the poor performance of Ag source-drain contacts is the somewhat noble characteristic of Ag (e.g. with regard to processes including oxidation). A layer of Ag_2O might reduce R_C when compared to elemental Ag. However, the formation of Ag_2O has a high Gibbs free energy of formation (ΔG_f^o = -11.21 kJ mol^{-1}) [92] which is not thermodynamically favourable. Applying a thin layer of an additional material at the Ag-In_2O_3 interface might reduce R_C. PEI reportedly lowers the work function of Ag from 4.6 ± 0.06 eV to 3.6 ± 0.06 eV. [93] Therefore, the addition of a thin film of PEI might lower the work function and corresponding interfacial resistance between In_2O_3 and Ag. This thesis work investigates a possible pathway for this approach, using the electron-donating polymer PEI (Section 2.5) as an interfacial layer between inkjet printed Ag contacts and In_2O_3 semiconductor.

The gate electrode for this thesis work is boron doped *p*-Si because this material doubles as a suitable substrate material for device fabrication. [2]

2.2.4 Substrates

TFTs fabrication typically involves deposition of sequential layers onto a certain material that might (e.g. dielectric) or might not (e.g. insulator) influence the device operation. A substrate is such a material, the choice of which depends on factors including the intended device application and processing conditions. For example, glass is applicable as a transparent, insulating TFT substrate material, but is not flexible. [94] Plastic substrates including polyethylene naphthalate (PEN), [95] polyimide (PI), [96] and polyethylene terephthalate (PET) [97] are used where both transparency and flexibility are required. However, processing temperature limits plastic substrate use, as many polymers are not thermally tolerant, having large coefficients of thermal expansion (CTE)‡ and low glass transition temperatures (T_g) causing restricted flexibility upon temperature elevation. In addition, such polymers

‡ The CTE for non-alkali glass (~ 3 ppm/K) is significantly smaller than that of PET (~ 10 ppm/K). [49]

suffer moisture/ gas permeation [49] and may not be complete insulators. Paper is another TFT substrate that is cheap and environmentally sound, but not thermally stable or resistant to moisture/ gas permeation. [98] Si materials are generally thermally tolerant substrates, although neither flexible nor transparent. Si is useful as a substrate for fabrication of reference devices. [2]

This thesis work relied on silicon wafer substrates, consisting of an underlying B doped *p*-Si layer that operates as a gate electrode, and a top layer of thermally grown SiO_2 as a dielectric material onto which the remaining TFT components are sequentially deposited.

2.3 Thin film transistor configuration

TFTs are FET devices relying on the field effect accumulation of charge carriers at the semiconductor-dielectric interface as introduced in Section 2.1. There are a number of possible stacking arrangements for TFT device constituents to achieve the field effect, as depicted in Figure 5. Each of these variations has advantages and disadvantages for various applications. Note that Figure 5 provides basic schematic examples (not drawn to scale) that are often modified in practice. Such modification may include the addition of layers such as highly doped semiconductor at the source-drain interface to limit contact resistance, or encapsulation of the entire device with a protective medium such as SU-8.[§] TFTs are similar to another class of transistor devices called metal oxide semiconductor field effect transistors (MOSFETs). The key differences between a TFT and a MOSFET are that the semiconductor of a TFT is not typically single crystal as in a MOSFET. Use of a single crystal is achieved through a high processing temperature (often > 1000°C) which limits use of thermo sensitive materials. TFTs benefit from lower processing temperatures to allow integration of thermo sensitive materials. In addition, a MOSFET semiconductor contains *p*-*n* junction doped regions at the source-drain interface (Figure 5 G). Although both TFTs and MOSFETs rely on the field effect to control conductance in the semiconductor, MOSFETs rely on creation of an inversion region (e.g. *n*-type conductive layer formed within a *p*-type semiconductor) whereas TFTs operate by an accumulation layer. [42]

[§] SU-8 is an organic photo resist material so named because of eight epoxy groups that cross link to provide the final stable structure. [173]

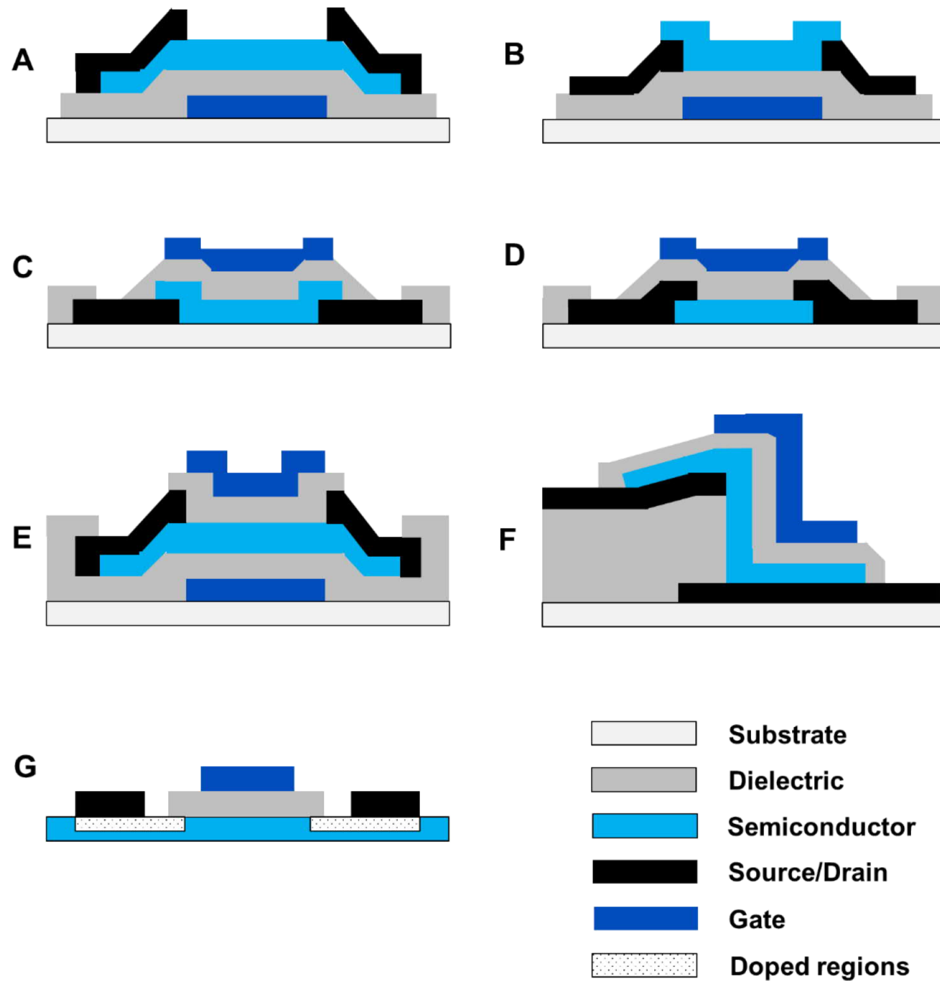

Fig. 5. Cross sections of conventional TFT structures: A) bottom-gated staggered TFT, B) bottom-gated coplanar TFT, C) staggered top-gated TFT, D) top-gated coplanar TFT, E) double-gated TFT, F) vertical TFT, and G) MOSFET device. Adapted from Refs [14,42,49]

Coplanar TFTs (Figure 5 B and D) are fabricated such that the active channel is in the same plane as the source-drain contacts. This configuration has low contact resistance. [99] Staggered bottom-gated devices (Figure 5 A) have been used for Si based TFTs and for liquid crystal displays (LCDs) because of easy processing and reliable device performance. [49] Here, the gate electrode shields light sensitive a-Si from back light emission in LCDs. However, coplanar top-gated configuration (Figure 5 D) is more applicable for poly-Si devices because this allows deposition of thermo sensitive components after high processing temperature of the semiconductor. [42,100] Another benefit of coplanar top-gated configuration (Figure 5 D) is encapsulation, providing mechanical and chemical protection of the semiconductor layer from environmental influences that may adversely affect device performance. [47] Top-gated TFTs (Figure 5 C and D) provide a pathway for

fabrication in as little as two steps, [53] with low photosensitivity from upper OLED emissions. [101] Double-gated TFTs (Figure 5 E) provide enhanced static performance by controlling a large region of the semiconductor channel, particularly in the vertical direction. [102,103] Demand for minimal device footprints and channel lengths has led to vertically aligned TFTs (VTFTs), (Figure 5 F) with the channel defined by thickness of certain layers. [72,104-106]

The TFT devices fabricated during this thesis work are of staggered bottom-gated configuration (Figure 5 A).

2.4 Thin film transistor operation and performance

This section describes TFT key performance indicators, and explains how devices are electrically characterised. The key direct current (DC) electrical performance parameters in TFT operation are from current-voltage characteristics according to the gradual channel approximation. [49,107] Plotting of two forms of current-voltage data relations provides information about TFT electrical characteristics. Firstly, a logarithmic plot of I_D over V_G provides a transfer curve, which can often include gate current leakage (I_G) plotted over V_G. Secondly, a logarithmic plot of I_D over V_D provides an output curve. These curves present two key operating regimes, linear and saturation. [14] The linear regime holds for small values of V_D (where $V_D << V_G - V_{th}$). In this case, I_D may be approximated according to the Shichman-Hodges model (Equation 1): [108]

$$I_{D.lin} = \frac{W \cdot \mu \cdot C_{OX}}{L} \cdot (V_G - V_{th}) \cdot V_D \qquad (1)$$

where μ is mobility of free charge carriers, C_{OX} is capacitance (loosely defined as the ability for storage of electrical charge) of the gate dielectric (per unit area), and L is the TFT channel length. For larger values of V_D (where $V_D \geq V_G - V_{th}$), TFT devices operate in saturation regime, with I_D provided by Equation 2 as:

$$I_{D.sat} = \frac{W \cdot \mu \cdot C_{OX}}{2 \cdot L} \cdot (V_G - V_{th})^2 \qquad (2)$$

Note that Equations 1 and 2 consider the channel dimensions L and W. This is because the physical shape and size of a TFT limits electrical performance, with

optimum devices having semiconductor and dielectric thickness that is vastly smaller than the L, with W around 15 times larger than L. [22]

Linear extrapolation of the I_D-V_G transfer curve for linear regime, or $I_D^{1/2}$-V_G curve for saturation regime, yields V_{th}. [109]

Current on/off ratio (I_{ON}/I_{OFF}) is the ratio of maximum to minimum I_D (typically in the saturation regime). [107] Maximum I_D is inherent of the semiconductor material, based on effectiveness of field effect accumulation of charge carriers. Minimum I_D may result from background instrument noise, or I_G. Large I_{ON}/I_{OFF} of ≥ 10^6 are typically required for TFT devices as useful I_D switches. [110,111] However, I_{ON}/I_{OFF} of ≥ 10^4 is adequate for analog circuitry. [112]

Turn on voltage (V_{ON}) is the value of V_G where a conductive channel forms, enabling I_D > zero, due to field effect accumulation of charge carriers. In a transfer curve, V_{ON} is evident as the point at which I_D begins to increase, the V_G required to turn the TFT device off. [113]

Overlap capacitance (C_{OV}) between the source-drain and gate electrodes has an influence on TFT device speed of operation. [107] C_{OV} is obtained by first considering a relation of total gate capacitance (C_G): [14]

$$C_G = C_{GS} + C_{GD} = C_{OX} \cdot W \cdot \left(L + L_{OV,TOT}\right) \tag{3}$$

where C_{GS} is the gate-source capacitance, C_{GD} represents gate-grain capacitance, and $L_{OV,TOT}$ is overlap length (total) between the source-drain and gate electrodes. [107] The above relation (Equation 3) allows construction of a plot of C_G over V_G, with C_{OV} found to be the minima of C_G. [14]

Transit frequency (f_T) provides information about the speed of a TFT device [107] and may be estimated using Equation 4 as follows: [114]

$$f_T = \frac{1}{2 \cdot \pi} \cdot \frac{g_m}{C_G} \propto \frac{\mu \cdot (V_{GS} - V_{th})}{L \cdot \left(L + L_{OV,TOT}\right)} \tag{4}$$

where g_m is the transconductance** in the saturation regime obtained from the following relation: [115]

$$g_m = \left(\frac{dI_D}{dV_G}\right)\bigg|_{V_D} \tag{5}$$

** Transconductance is the ratio of current change to voltage change, in this case referring to the ratio of changes in I_D and V_G, respectively.

Sub threshold swing (S) refers to the V_G required to increase I_D by one decade. This provides an indication of how efficiently a TFT device can switch between on or off states [14] and is related to the dielectric-semiconductor interface quality. [107] Small S provides low power consumption and high speed of TFT devices, with ideally $S << 1$. [116] S is the inverse of the TFT transfer curve slope maxima according to Equation 6: [14,42]

$$S = \left(\left. \frac{d \log_{10}(I_D)}{dV_G} \right|_{max} \right)^{-1} \tag{6}$$

μ is a measure of efficiency of charge carrier movement. High μ permits high I_D, allowing rapid f_T. Factors that limit μ include scattering of charge carriers by structural defects including grain boundaries, interfacial roughness, impurities, and lattice vibrations. A number of methods follow that apply for determination of TFT μ as described by Schroder. [117] Effective mobility (μ_{eff}) from drain conductance (g_d) with a low V_D:

$$\mu_{eff} = \frac{g_d}{C_{OX} \cdot \frac{W}{L} \cdot (V_G - V_{on})} \tag{7}$$

where g_d is obtained from the following relation: [115]

$$g_d = \left. \left(\frac{dI_D}{dV_D} \right) \right|_{V_G} \tag{8}$$

Field effect mobility (μ_{FE}) from g_m with low V_D:

$$\mu_{FE} = \frac{L}{W \cdot C_{OX} \cdot V_D} \cdot g_m \tag{9}$$

Saturation mobility (μ_{sat}) from g_m with a high V_D:

$$\mu_{sat} = \frac{\left(\frac{d^2\sqrt{I_D}}{d\,V_G} \right)^2}{\frac{1}{2} \cdot C_{OX} \cdot \frac{W}{L}} \tag{10}$$

Generally, literature only reports the peak values for μ_{eff}, μ_{FE}, and μ_{sat}. However, plotting of these factors as a function of V_G can highlight μ degradation resulting from scattering or contact resistance relative to increasing V_G. [42]

R_C between the source-drain electrodes and semiconductor material is of particular importance in short channel devices with $L \leq 5$ µm, where high R_C can result in poor f_T and μ_{FE}. [118] R_C is affected by such things as the contact-semiconductor interface [119] and interfacial treatments, [99] as well as the source-drain electrode material. [120] Analysing the transfer curves of a set of TFT devices with varying L provides a value for total resistance (R_T) according to Equation 11:

$$R_T = R_{ch} \cdot L + R_C \tag{11}$$

where R_{ch} is the channel resistance per unit of channel length. [120] Plotting R_T values at varying V_G allows determination of R_C. An alternative method for obtaining R_C is from the ratio of two transfer curves from the same TFT device, recorded at two different V_D values. [121]

In summary, rapid switching between on or off state is desirable for TFT devices. To enable this behaviour requires very small S, V_{th} close to zero, and high μ. [49] Electrical characterisation of TFT devices in the form of transfer and output curves not only provides quantitative device information in the form of the above-described parameters, but also yields a qualitative visual indication of device performance.

2.5 Inkjet printed thin film transistor fabrication

Printing is a useful method for production of MO TFT devices, with low cost and high throughput. [4] Various forms of printing processes for MO TFT fabrication have developed since the first report of a printed electronic device by Sihvonen *et al* in 1967. [122] Contemporary printing methods include inkjet, [123-127] flexographic, [10,128] and gravure printing. [129] Direct printed TFT fabrication avoids the multiple steps, and capital required for lithography, etching, and vacuum processing such as chemical or physical vapour deposition (CVD, PVD). [4] Low temperature processing of inks allows compatibility with thermo sensitive materials such as substrates (e.g. PET or PEN) or dielectrics (e.g. SU-8 or PVP). Printed production can lead to large area or so called reel-to-reel (or roll-to roll) fabrication. [130] This process involves a flexible substrate rolled off a reel and onto another, with TFT devices deposited during a number of stationary steps. Of the various forms of print-based TFT production, inkjet printing is of particular interest due to a number of advantages.

Inkjet printing relies on digitally controlled fluid droplet ejection to a desired location. The method uses mild conditions (ambient temperature and pressure). Only small quantities of ink are required, with minimal wastage. Variable digital patterning is achievable with fine resolution, and multiple functional inks are able to be layered sequentially. Inkjet printing is a non-impact method because there is no equipment contact with the sample, which is good for samples with topography, or fragile substrates. Challenges for inkjet processing include stable ink formulation, suitable viscosity and surface tension for good droplet formation, and ink-sample surface interactions. [131]

In 1878, Lord Rayleigh birthed the idea of an inkjet, proposing that a jet of liquid with constant radius falls vertically under influence of gravity. As length of the liquid jet increases to reach a critical point, it decomposes from a cylindrical form into a stream of individual uniform droplets (Figure 6). [132]

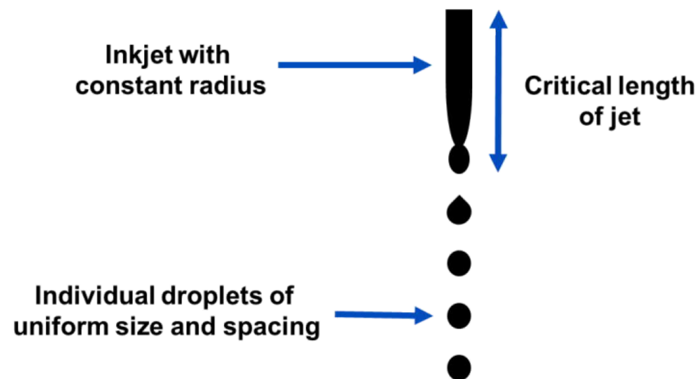

Fig. 6. Instability of a fluid jet with a constant radius under gravity, fracturing into individual droplets.

Controlling of the principle depicted in Figure 6 was achieved in 1974 when a pulsed drop on demand (DOD) system was devised, allowing ejection of droplets as required rather than continuously. [133] Nowadays, there are a number of different DOD inkjet systems available, driven by piezoelectric, thermal, electrostatic, electro hydrostatic, valve, and acoustic ejection print heads.[††] [134] Piezoelectric inkjet methods are suitable for fabrication of MO TFTs. This process relies on electronic impulse deformation of a piezoceramic plate within a print head. The deformation generates a wave of pressure, ejecting ink from a reservoir and out from the nozzle(s). [135] Following the electronic impulse, the piezoceramic plate relaxes to its original form and ink replenishes the reservoir. [136] These electronic impulses

[††] A print head is an integral part of inkjet printer equipment that usually consists of an ejection mechanism, ink reservoir, and faceplate with multiple nozzles.

are controlled using detailed waveforms tailored for ejection of inks according to properties including surface tension and viscosity. Figure 7 below depicts a basic waveform example, showing voltage changes over time applied to a piezoelectric element for controlling the ejection of ink from a print head chamber. This waveform has divided sections for specific ejection operations described as follows. Firstly, in the start phase there is a bias voltage applied to power on the print head and depress the piezo element in the ink chamber to a neutral position. Next (phase one), the voltage is reduced to zero, drawing ink into the chamber as the piezo element is distorted. Once the ink chamber is full, the voltage is increased (phase two) which generates pressure inside the chamber as the piezo element compresses the ink. This pressure increase results in ejection of ink from the print head nozzle(s). After droplet ejection, there is a partial voltage reduction (phase three) to decompress the chamber slightly, with the aim of pulling backwards on the ejected droplet to avoid formation of satellite droplets. Formation of smaller droplets called satellites can occur where a ligament or tail accompanies the main droplet upon ejection, and is then broken free to either follow the primary droplet, or fall outside of the main droplet trajectory. A final voltage reduction (stage four) returns the chamber to a neutral, part filled state. The slope of these phases and dwell time between voltage changes is altered in practice as determined by the properties of different inks.

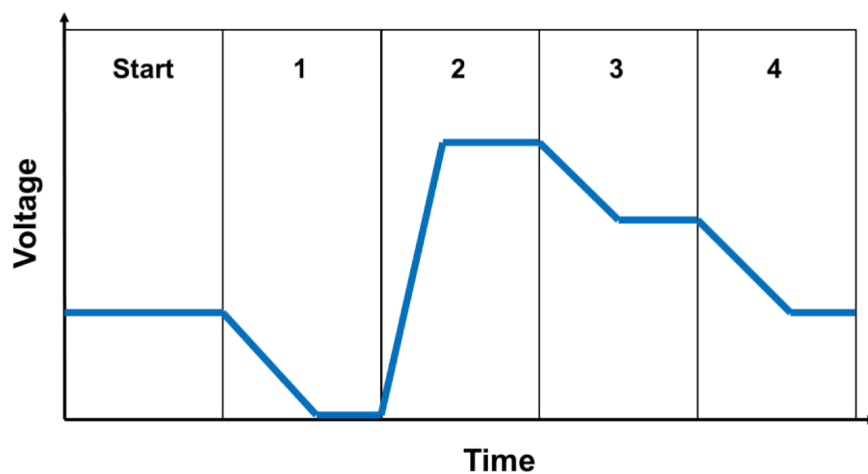

Fig. 7. Model inkjet waveform of piezoelectric print head ink voltage over ink ejection time, comprising phases start to four with increasing printing duration. Adapted from Refs [131,137]

Rheology is an aspect for consideration when formulating inks for inkjet printing. The ink properties must be compatible with the print head hardware to ensure correct droplet formation. Poorly formulated inks can suffer from spraying of ink from nozzles, or seeping of ink from nozzles causing wetting of print head faceplate. Calculation of theoretical printability of an ink can assist formulation and

relies on a number of fluidic parameters. Firstly, the following relation represents the Reynolds number (Re_n): [138]

$$Re_n = \frac{\rho \cdot v \cdot l}{\eta} \qquad (12)$$

where ρ is ink fluid density (kg m^{-3}), v is droplet velocity (m s^{-1}), l is the characteristic length of the ink liquid (nozzle diameter/ m), [2,131] and η is dynamic viscosity of the ink fluid (Pa·s). Optimal *Re* falls in the range of 50–500. A second important fluid parameter is the relation for calculation of Weber number (We_n): [134]

$$We_n = \frac{v^2 \cdot \rho \cdot l}{\gamma} \qquad (13)$$

where γ represents surface tension of the ink (N m^{-1}). Acceptable We_n is between 20 and 300. [134] A third important relation is provides the Ohnesorge number (Oh_n): [139]

$$Oh_n = \frac{\sqrt{We_n}}{Re_n} = \frac{\eta}{\sqrt{\gamma \cdot \rho \cdot l}} \qquad (14)$$

The suggested window for Oh_n is $0.1 > Oh_n < 1$. [140] The inverse of Oh_n is a key indicator of ink printability called the *Z* parameter: [141]

$$Z = \frac{1}{Oh_n} \qquad (15)$$

Stable droplet formation generally occurs at $1 > Z < 10$, [142] with $Z > 10$ causing satellite droplets, and $Z < 1$ leading to insufficient ink ejection (e.g. from high viscosity). [2]

Formulating inks for production of MO TFTs requires consideration of not only droplet behaviour, but also desired final material and required post-print processing. Often the bulk of the ink is a carrier liquid solvent, which enables the desired material to remain suspended or dissolved as a stable ink, and be ejected as droplets. Often there is a requirement for additional cosolvents to adjust the surface tension and viscosity of the ink fluid. [143] Addition of cosolvents assists spherical droplet formation and helps to avoid ink leaking from (with low surface tension), or clogging (with high surface tension) nozzles. There are two main approaches for MO TFT ink formulation, nanoparticle suspensions, or molecular precursors. [42] Although these routes are relatively new, other groups have previously achieved reasonable results,

with the molecular precursor path providing lower post-printing annealing temperatures than that of nanoparticles. [10] For example, metal halides, [123] acetates, [144] and nitrates [145] have been formulated for solution based MOS fabrication. $In(NO_3)_3$ based precursor inks have proved successful in converting from salts by thermal decomposition of the anions from the metal, to form metal-oxygen-metal bonding at relatively low temperatures. [2,125,146,147]

Once ink formulation and droplet ejection is optimised, inkjet printed feature resolution (typically of the order of tens of μm) [131] depends on factors including the droplet volume, distance of nozzle from sample surface, and interaction of ink with sample surface. [148] Completely printed TFT devices demand control of interactions between the ink and substrate, where wetting, diffusion, and adhesion behaviour is critical. Substrate properties such as surface energy and topography influence ink-substrate interactions. If ink is ineffective in wetting of the sample surface, then individual droplets may remain rather than merge together to form a uniform printed area. Measurement of contact angle quantifies wetting of sample surface (e.g. substrate) by ink, with a high contact angle typical of poor wetting, and low contact angle indicative of good wetting. Ink on a sample with a contact angle of 180° is non-wetting, a contact angle of < 90° is wetting, and 0° contact angle is perfect wetting. Figure 8 depicts three different examples of wetting.

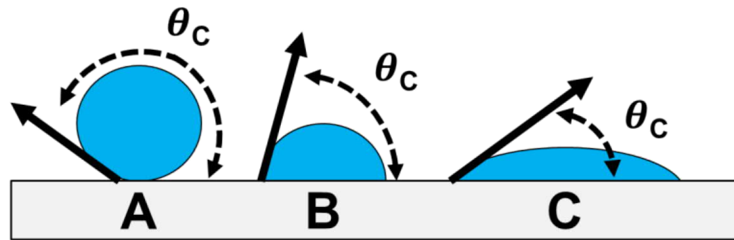

Fig. 8. Schematic of substrate (grey) wetting by ink droplets (blue) with decreasing contact angle (θ_C) from A (> 90°) to C (< 90°) indicative of improved wetting.

A liquid ink that has come to rest on a solid substrate surface, will spread depending on an energy equilibrium for constituent interfacial energies, expressed by the Young equation: [148]

$$\sigma_{SV} = \sigma_{LS} + \sigma_{LV} \cos\theta_C \tag{16}$$

where σ_{SV} is substrate-vapour (atmospheric) surface energy, σ_{LS} is liquid-substrate surface energy, σ_{LV} is liquid (ink)-vapour surface energy, and θ_C is contact angle of

ink wetting on solid sample. If poor wetting occurs, surface energy altering sample treatment may be required to assist droplet coalescing and formation of uniform printed areas. For example, plasma activation/cleaning of solid sample to assist interfacial interactions such as modifying the θ_C of the ink on the sample surface. [99]

In addition to ink stability, droplet formation, and wettability of the sample by ink, consideration of a number of other factors is important in order to obtain good results in inkjet printing of MO TFTs. For example, inter-drop spacing of individual ink droplets on incident on a sample is an important consideration for uniformly printed areas. Too high a drop spacing leads to individual, isolated droplets or scalloping of boundary lines as shown in Figure 9 A and B, respectively. If drop spacing is too low as in Figure 9 D, large amounts of ink become localised, resulting in non-uniform layer thickness and boundary bulges. [149]

Fig. 9. Schematic illustration of drop spacing effect on boundary line edge of inkjet printed areas, showing drop spacing decreasing from A to D, with C presenting the cleanest edge.

Alignment of detailed patterns is paramount, especially multilayer designs. Here print head accuracy can be a limiting factor. Coffee ring effect from Maragoni flow during evaporation can be an issue caused by evaporation of solvents from printed materials. [150] This phenomenon results in the edges of a printed area having greater proportion of material than the centre and calls for careful ink formulation (such as multicomponent solvent systems) and deposition conditions. [151] There is a higher evaporation flux at the edges of the printed area. Compensation for greater evaporation at the edge than centre of the print area results in capillary driven flow of ink liquid towards the print area edge. [152]

Consideration of solvent systems and ink deposition can alleviate coffee ring effects and other issues that limit controlled print resolution. [153]

This thesis work focuses on formulation and subsequent inkjet printing of $In(NO_3)_3$ based precursor inks for In_2O_3 as a semiconductor for TFTs. A subsequent step involves inkjet printed Ag nanoparticle source-drain contacts, and investigation of methods to enhance the semiconductor-contact interfacial interactions.

2.6 Polyethyleneimine

Polyethyleneimine (PEI) is a polymeric species commercially available since 1938. [154] PEI is composed of amine functional groups separated by aliphatic R-CH_2-CH_2-R spacing units. PEI exists in three forms, linear, branched, or dendrimeric [155] forms as depicted in Figure 10 below.

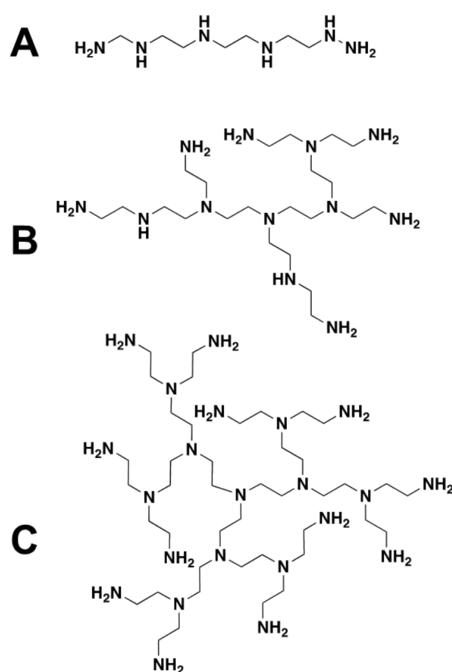

Fig. 10. Linear (A), branched (B), and third generation dendrimer (C) forms of polyethyleneimine (PEI) subunits.

A key feature of PEI is inclusion of amine functional groups. Amines are classed as primary, secondary, tertiary, or quaternary, depending on their substituents as depicted in Figure 11. Ammonia is similar to an amine, being a molecule with a

nitrogen atom bonded to three hydrogen atoms. The nitrogen atom in a primary amine is bonded to two hydrogen atoms and one other species (usually carbon based) such as an aryl or alkyl group.‡‡ A secondary amine is bonded to one hydrogen atom and two other species (which may be the same). The nitrogen atom in a tertiary amine is not directly bonded to a hydrogen atom, but rather three substituents (which may be the same). A quaternary amine has a nitrogen boded to four substituents (which may be the same). Figure 11 below presents differences in amine structure. Note the inclusion of two dots on the nitrogen atoms, which represent a lone pair of electrons. This lone pair is two valence electrons of nitrogen that are not shared with another species. Note that a quaternary amine (Figure 11) has no lone pair of electrons. Electrons have negative charge, so as the lone pair is drawn away from the nitrogen nucleus towards the carbon atom during bonding with the methyl group, so too is the partial negative charge of the nitrogen. This is why the nitrogen in a quaternary amine molecule (e.g. tetramethylammonium in Figure 11) possesses a positive charge.

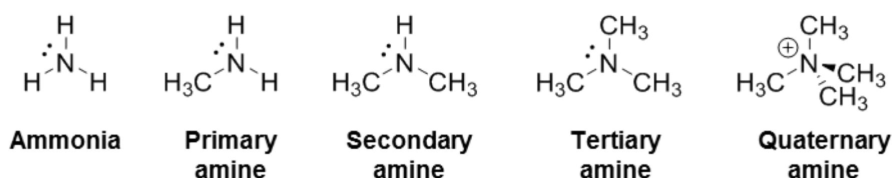

Fig. 11. Structural comparison of amine functionality as dependent on substituents, methyl groups in this case.

Branched PEI is composed of a combination of primary, secondary, and tertiary amino groups. PEI dendrimers contain tertiary and primary amines. Linear PEI only possesses secondary amine functionality. The lone pair of electrons in PEI is available for interactions with other species. Such interactions include electron donation, suggesting PEI might be useful for applications requiring an electron donor material to enhance charge carrier transport. For example, PEI might donate its extra valence electrons to the conduction band of a semiconductor material, increasing the mobile carrier concentration of the semiconductor. This electron donation by PEI might result in a shift in the Fermi level of the semiconductor towards the conduction band. [156] The semiconductor would become *n*-type because of this doping. This approach of using PEI as an electron donor has been reported for metal oxide [44] and organic TFTs, [157] TFT pH sensors, [158] graphene, [159] organic light emitting

‡‡ A nitrogen atom directly attached to a carbonyl group (R-N-CO-R) is an amide functional group, not an amine.

diodes (OLEDs). [160] The electron donating ability of PEI might enable the polymer to assist interfacial interactions by charge carrier injection, resulting in improved contact of neighbouring layered materials. The improved contact because of electron donation from PEI to electron acceptor materials may be due to formation of an interfacial dipole, which assists in reducing the work function. [93,160] The PEI may also work to increase the energy barrier, supressing hole transport, with positive charge carriers trapped by PEI lone pairs. [157] Ag cations can be coordinated by the PEI lone pairs, leading to covalent bonding of Ag-N. [161] Such PEI:MOS interactions would improve interfacial binding between the contacts and MOS. In fact, PEI based products are commercially available as adhesion promotor materials. [12] In light of the above, it is possible that a thin layer of PEI (or material containing PEI) between the Ag source-drain contacts and In_2O_3 might reduce R_C, leading to improved TFT device performance.

Chapter 3

Experimental

3.1 Ink formulation

All inks were prepared and stored in non-transparent, high-density polyethylene (HDPE) screw cap containers (Nalgene).

3.1.1 Semiconductor ink preparation

Working under nitrogen atmosphere inside a glovebox (O_2 ~ 10 ppm, MBraun MB 200) following a reported method, [2] indium nitrate ($In(NO_3)_3 \cdot 2.5H_2O$, 99.99%, EpiValence UK) [10] was dissolved in 2-methoxyethanol (2-ME) (anhydrous, 99.8%, Sigma-Aldrich) with heating (75°C, 17h) and magnetic stirring (500 rpm) to obtain a 0.2M solution. The mixture was heated (75°C, 17 h) with magnetic stirring (500 rpm). The solution was filtered through a 0.45 μm polytetrafluoroethylene (PTFE) Acrodisc, before adding 10 wt.% ethylene glycol (EG) (anhydrous, 99.8%, Sigma-Aldrich) and then shaken, (room temperature, 250 rpm, 15 min, IKA KS260 shaking table) resulting in an optically transparent liquid, pH ~ 4.5.

3.1.2 Polyethyleneimine ink preparation

Under nitrogen, polyethyleneimine (PEI) (anhydrous, 99.9%, branched, M_w ~ 25 000, OR 50 wt.% in H_2O, branched, M_w ~ 2 000, Sigma-Aldrich) was dissolved in 2-ME (anhydrous, 99.8%, Sigma-Aldrich) with stirring (room temperature, 17 h) to form a 0.4 wt.% solution. The solution was filtered through a 1.0 μm glass Acrodisc, before adding 10 wt% EG (anhydrous, 99.8%, Sigma-Aldrich) then mixed (room temperature, 60 min, Interroll Drive Control 20 roller) to obtain an optically transparent liquid, pH ~ 9.5.

3.1.3 Polyethyleneimine indium nitrate composite ink preparation

Following agitation, (room temperature, 30 min, Interroll Drive Control 20 roller) PEI ink (Section 3.1.2) was added to semiconductor ink (Section 3.1.1) to a concentration of 1 wt% PEI (relative to $In(NO_3)_3$). The combined solutions were mixed, (room temperature, 2 h, Interroll Drive Control 20 roller) yielding an optically transparent liquid, pH ~ 4.5.

3.2 Inkjet printing

Inkjet printing patterns were designed using AutoCAD software, and then converted to Dimatix Materials Printer (DMP) compatible format using Inkscape and MS Paint software, respectively. Ink solutions were printed with a DMP-2831 (Fujifilm, USA) inkjet printer, with a print head containing a piezoelectric cartridge (DMCLCP-11610) and samples vacuum situated on a platen. The area of platen not containing samples was protected from ink spillage by a plastic film (Figure 12). The cartridge temperature was 30°C for all inks, with a platen temperature also 30°C. Ink droplets were optimised for an in-flight speed of ~ 7 m s^{-1}. For the semiconductor (Section 3.1.1), PEI (Section 3.1.2), and PEI composite inks (Section 3.1.3), ten adjacent nozzles were optimised using a customised waveforms (Appendix A), before printing 10 pL droplets with a drop spacing of 75 µm (339 dpi). Ag ink (Advanced Nano Products, Silverjet DGP 40LT-15C) and SU-8 ink (MicroChem, XP PriElex SU-8 1.0) were filtered (0.2 µm glass Acrodisk) and printed using tailored waveforms (Appendix A), a single nozzle, with 40 µm drop spacing (635 dpi). Print pattern alignments were achieved by optimising the printing location of a droplet matrix of 5 x 5 droplets (drop spacing of 225 µm) to the desired X, Y printing start point, verified with optical microscope (Zeiss, Germany).

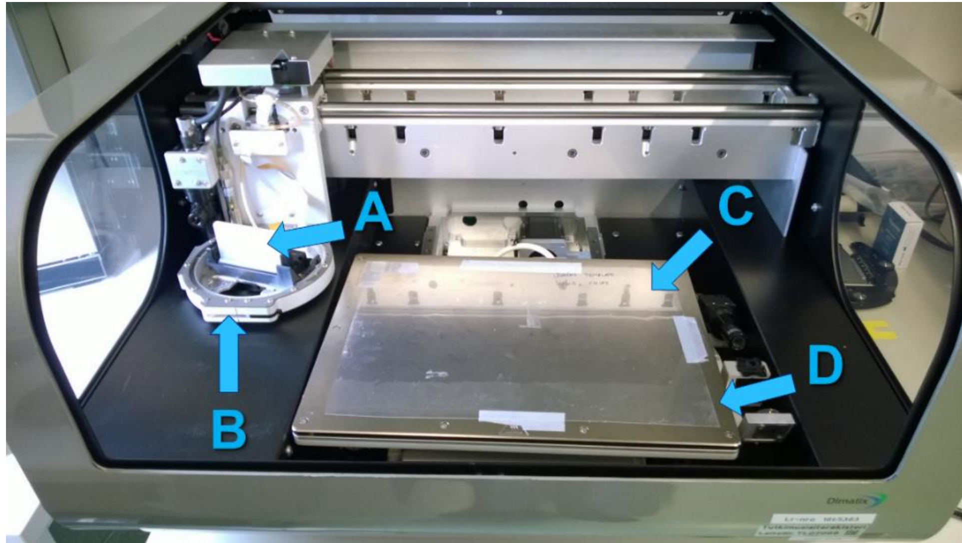

Fig. 12. Dimatix DMP-2831 inkjet printer annotated to show the print cartridge (A), print head (B), protective platen sheet (C), platen (D).

3.3 Substrates

Substrates for TFT devices were cut from 6”, 625 µm thick, B doped *p*-type Si wafer (E&M, Japan) with thermally grown SiO_2 (~100 nm oxide thickness) to provide C_G of ~ 35 nF cm^{-2}. [147] To protect against fragment damage during cutting, substrate wafer was spin coated with AZ 5214 E photo resist (15 s at 500 rpm, 45 s at 1500 RPM), then hotplate baked (90°C, 1 min). Following spin coating, the wafer was cut for individual sample dimensions of 13.52 mm x 13.52 mm. Photo resist was removed from substrates by acetone (ACE) bath (60°C, 10 min). Substrates were cleaned by washing in ultrasonic bath (40°C, 15 min, VWR) with deionised water (DIW), ACE, and isopropyl alcohol (IPA), respectively.

3.4 Thin film transistor fabrication

Devices were fabricated by sequential deposition of thin films onto Si substrates by either spin coating, or inkjet printing.

Spin coating of materials was undertaken to produce reference thin films to investigate surface properties prior to designing inkjet experiments. Spin coated materials include semiconductor ink (Section 3.1.1) and PEI ink (Section 3.1.2). Prior

to spin coating In_2O_3 precursor ink, Si chip substrates were activated with plasma (60 s, 4 mL min^{-1} O_2, 200 W, Diener Nano). Prior to spin coating PEI precursor ink, Si chip substrates were activated with plasma (12 s, 4 mL min^{-1} Ar, 200 W, Diener Nano) then printed with SU-8 (Section 3.2) which was hotplate dried (135°C, 5 min). Substrates were situated in a spin coater (WS-400B-6NPP/LITE, Laurell Technologies Corp.) and vacuum fixed into position. Next, four drops of material were added to the sample via syringe through a filter (0.1 µm glass Acrodisc for PEI, 0.45 µm PTFE Acrodisc for $In(NO_3)_3$) (Figure 13) Excess liquid was removed by spinning (5 s at 500 rpm, then 60 s at 8 kRPM) to obtain a thin film. Spin coated PEI was hotplate dried (200°C, 15 min) to remove solvents. Samples spin coated with semiconductor material were hotplate dried (90°C, 15 min) and annealed (300°C, 30 min).

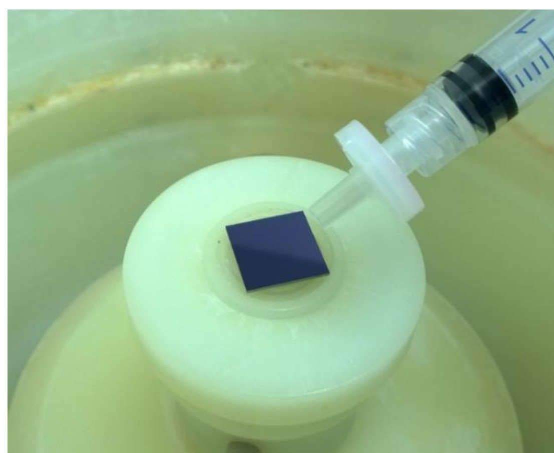

Fig. 13. Application of In_2O_3 precursor ink to Si sample during spin coating.

Prior to printing of the semiconductor layer, substrates were activated with oxygen plasma (60 s, O_2 4 mL min^{-1}, 200 W, Diener Nano). In_2O_3 semiconductor was inkjet printed as two successive layers (no drying step between) then hotplate dried (90°C, 15 min) and annealed (300°C, 15 min) in air. Next the semiconductor surface was plasma treated (6 s, 4 mL min^{-1} Ar, 200 W, Diener Nano) before interfacial PEI or PEI:In_2O_3 layer was inkjet printed as a single layer, then hotplate dried in air (200°C for 15 min for PEI, 300°C for 30 min for PEI:In_2O_3). The source/drain contact electrodes were deposited either by inkjet printing (Ag), or by thermal vacuum evaporation (Al). Plasma treatment (12 s, Ar 4 mL min^{-1}, 200 W, Diener Nano) was required before printing Ag contacts, which were deposited as a single layer. Samples were then oven sintered (150°C, 30 min, Memmert UNE400). For the evaporated contacts, 50 nm thick Al (99.999% pure, Testboune Ltd) was evaporated using equipment developed in house (Figure 14), to deposit Al on samples through

a shadow mask, forming *W* of 1 mm and *L* of 120 μm (*W*/*L* ~ 8.3). Post contact annealing (150°C, 30 min) was performed on a hotplate in air.

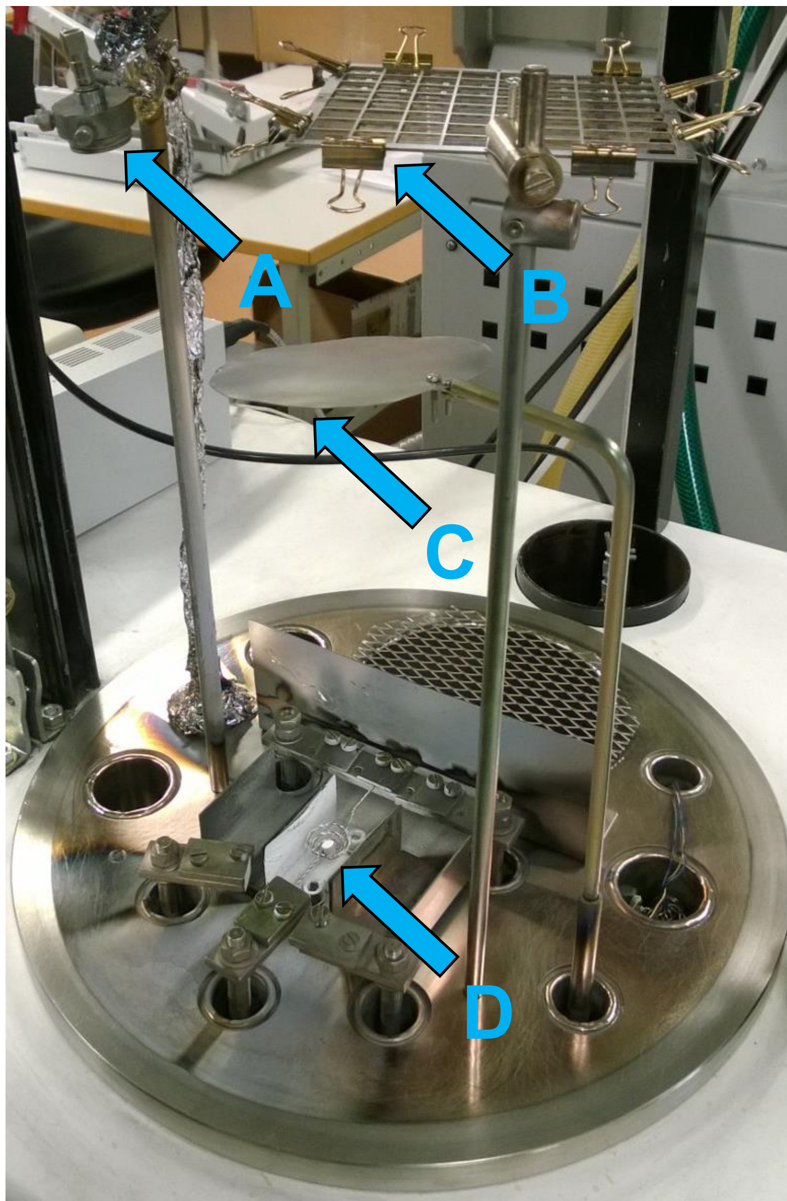

Fig. 14. Interior chamber of vacuum evaporation equipment showing layer thickness sensor (A), shadow mask containing seated samples (B), movable shield (C), and a basket containing an Al pellet (D).

3.5 Material characterisation

In addition the electrical characterisation methods below, devices and ink behaviour on printing surfaces was inspected using optical microscope (Olympus BX60) with camera (Olympus, SC30 U-CMAD3, U-TV1X-2) and measurement software (Stream Basic) both during and post fabrication. The pH of inks was approximated using colour indicator strips (Merck, Universalinikator).

3.6 Electrical characterisation of thin film transistor devices

Samples were prepared for analysis by etching the dielectric to expose the gate material, then applying Ag paint (SCP, Electrolube, HK Wentworth) to enable gate contact (Figure 15 A). Electrical performance of the TFT devices was analysed with a three-probe station (Cascade Microtech cabinet with Motic MLC-150C lighting) in dark condition at room temperature, with measurement data recorded using a Tektronix Keithley 4200 SCS analyser. Transfer curve data collection was made at the saturation region (V_D = 20 V) by sweeping V_G in 0.5 V increments with 0.01 s step duration for both forward and reverse directions of the transfer curves. Similarly, output curve data were collected by sweeping V_D by increments of 0.5 V using 0.01 s step duration.

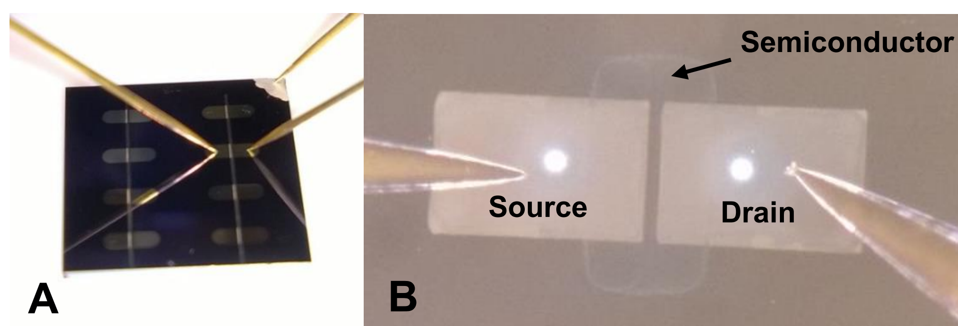

Fig. 15. Three-probe electrical measurement of TFT devices as viewed from the side (A) with probes on source, drain, and gate contacts (from left to right) of one of eight TFTs on the sample. As viewed from above (B) showing source-drain electrode and semiconductor layers.

Chapter 4

Results and discussion

The aim of this work was to investigate whether PEI can assist the electrical performance of TFT devices with inkjet printed Ag source-drain contacts, by reducing R_C at the contact to In_2O_3 semiconductor interface and enhancing μ_{sat}. This chapter presents the main findings observed while seeking to answer this research question.

4.1 Printing templates

Print patterns were devised in order to realise fully inkjet printed TFT devices. This was achieved using AutoCAD software to develop multi-layer patterns for sequential printing of material thin films as depicted in Figure 16. The print patterns were designed using a grid-snap system considering drop spacing dimensions to best align edges of printed layers. This is particularly important when defining a specific TFT channel length and width at micro scale. Another consideration in devising print patterns is the number of nozzles employed during printing. For example, the semiconductor ink printing involved ten sequential nozzles in a single printing sweep, as reflected in the print pattern. Problems with thin film uniformity and homogeneity may arise if the print pattern failed to avoid cross sweeps in a print area.[§§] Using Inkscape and MS Paint software to alter scaling and drops per inch (DPI) resolution, AutoCAD patterns were converted into DMP format for compatibility with the printer drivers. This process proved simple and enabled inkjet printing of inks with precise and accurate deposition according to desired patterns.

[§§] In these experiments, the print head sweeps in direction of the y vector (Figure 16) with ten nozzles depositing the semiconductor ink for a TFT device during a single sweep. If the printing area was extended beyond that achieved by the ten nozzles in a single sweep, then the print head would return in additional sweeps to deposit the required material. This could cause a gap between sequentially deposited material, or some other inhomogeneity.

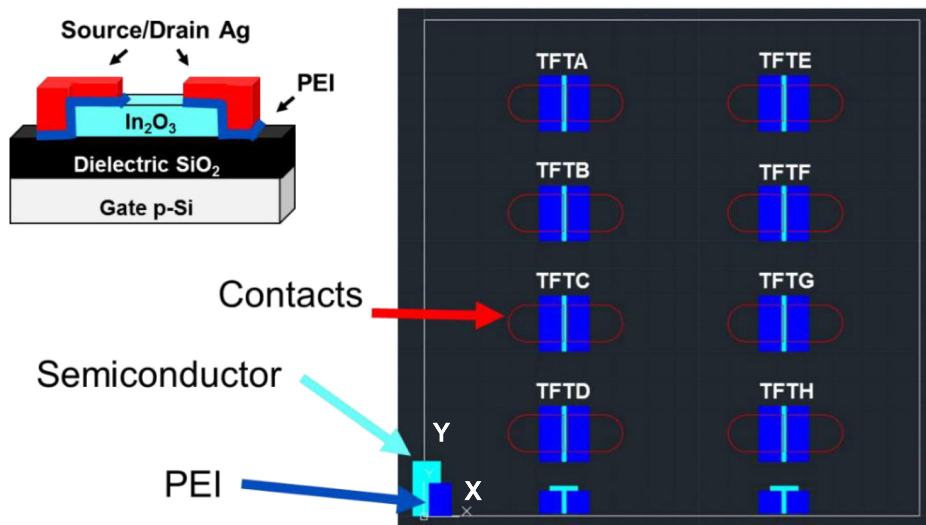

Fig. 16. Multi-layer print pattern produced using AutoCAD software for inkjet printing of sequential TFT components, showing eight labelled devices per sample area (right image). The left image presents schematic sliced side view of a device.

4.2 Indium oxide semiconductor material

Semiconductor precursor ink formulation and subsequent printing described in Chapter 3 is a highly reproducible method for production of thin film In_2O_3. A schematic path for the method is depicted in Figure 17, which includes a micrograph of the resulting material. Note the presence of visible lighter and darker blue regions of the semiconductor, indicative of morphology caused by some shape retention from individual printed precursor ink droplets.

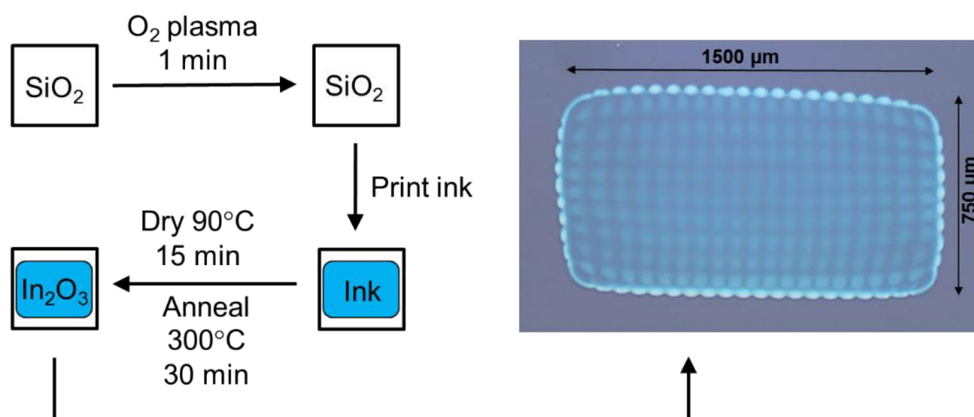

Fig. 17. Preparation of inkjet printed In_2O_3 semiconductor layer.

To realise the thin film semiconductor product depicted in Figure 17 above required method optimisation. This section (4.2) describes how the semiconductor precursor ink, its printing and post printing treatments were explored during this research.

4.2.1 Semiconductor ink printability

Previous work reports optimisation of the formulation of the semiconductor ink for printability by including EG cosolvent with 2-ME. [2] EG enhances printability by increasing ink viscosity to limit ejection of trailing ink after each droplet, while maximising recoil of trailing ligaments. Determining Oh_n according to Equation 14 (Section 2.5) allows for estimation of the Z parameter for the semiconductor ink according to Equation 15 (Section 2.5). Given that ρ for 2-ME = 965 kg m^{-3} and ρ for EG = 1113 kg m^{-3}. ρ of the semiconductor ink solution is estimated by considering the constituent cosolvents according to Equation 17 as follows for 10 g of ink comprising 9:1 2-ME:EG:[***]

$$\rho = \frac{0.01\ kg}{\left(\frac{0.009\ kg}{965\ kg\ m^{-3}}\right)+\left(\frac{0.001\ kg}{1113\ kg\ m^{-3}}\right)} = 978\ kg\ m^{-3} \tag{17}$$

Using the ρ value from Equation 17, calculation of Oh_n is possible given the following reported properties for the semiconductor ink at ambient temperature and pressure: η = 3.62·10^{-3} Pa·s, γ = 3.24·10^{-2} N m^{-1}, and l = 2.1·10^{-5} m. [2] Entering the given values into Equation 14 yields:

$$Oh_n = \frac{3.62\cdot10^{-3} Pa\cdot s}{\sqrt{3.24\cdot10^{-2} N\ m^{-1}\cdot 978\ kg\ m^{-3}\cdot 2.1\cdot10^{-5} m}} = 0.140$$

Armed with a value for Oh_n, Equation 15 is used to calculate the Z parameter for the semiconductor ink:

$$Z = \frac{1}{0.140} = 7.13$$

This Z value (~ 7) sits within the suggested margin (1 > Z < 10) [142] for stable droplet formation.

[***] This calculation assumes that the effect of the metal salt component of the ink on ρ is negligible and that the sum of the co-solvents equals the total mixture mass and volume.

The semiconductor precursor ink printing (Section 3.2) required some optimisation of the droplet ejection. The DMP equipment includes a stroboscope, which enables the ejected droplets to be viewed while adjusting waveform parameters. By altering the ejection voltage for each nozzle, the droplets were arranged in a line relative to the nozzles, where all droplets have the same velocity, with a straight trajectory, and no satellites or tails by the time they reach the sample surface (Figure 18).

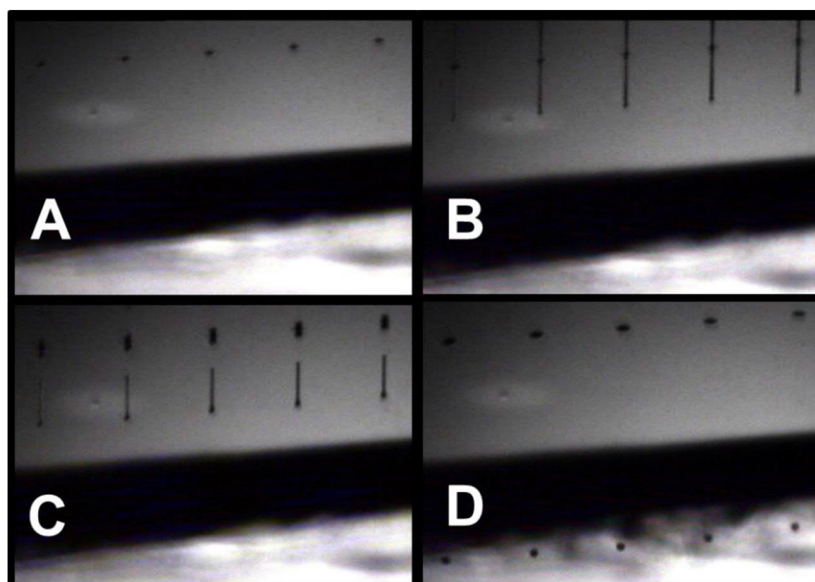

Fig. 18. Stroboscopic images of In_2O_3 precursor ink droplet trajectory from nozzles at (A, 0 µs) as ejected (B, ~ 20 µs) to form tailed droplets (C, ~ 40 µs), which form spherical droplets with no satellites (D, ~ 100 µs) before impact with the sample.

4.2.2 Effects of relative humidity

Ambient humidity of the laboratory environment where the TFTs are fabricated is subject to seasonally dependent fluctuations. This is of concern, because the semiconductor precursor ink contains moisture sensitive components (e.g. hygroscopic $In(NO_3)_3$). This issue was highlighted by the presence of what appeared to be formation of crystallites in a spin coated layer of In_2O_3 produced from preparation of the precursor ink and spin coating (with subsequent drying/annealing) in ambient conditions. Figure 19 presents a micrograph of this observation alongside a typical sample. The strange behaviour of the spin-coated material (Figure 19, B)

occurred with the sample being prepared in low ambient humidity of ~ 16% RH, whereas the typical sample (Figure 19, A) was prepared in ~ 32% RH. †††

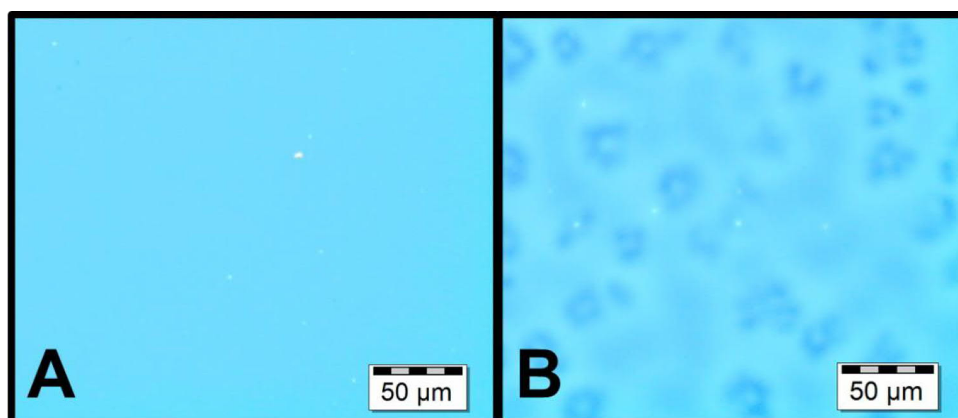

Fig. 19. Micrographs of two spin coated In_2O_3 samples showing (A) typical thin film appearance when prepared with RH ~ 32% and (B) presence of inhomogeneity when prepared in low RH of ~ 16%.

The experimental method (Chapter 3) provides a number of pathways for the influence of moisture in air. For example, weighing of hygroscopic $In(NO_3)_3$ powder before adding solvent is likely to introduce water into the formulation, in amounts that are very difficult to quantify. Another possible mechanism for the effect of humidity is during the overnight mixing of $In(NO_3)_3$ with 2-ME in a bottle with a headspace of air containing moisture. Ideally, the experimental method should be as reproducible as possible, which means that in this case the moisture content of the semiconductor inks should not vary from batch to batch. In an attempt to avoid humidity related effects, inks were formulated inside a glove box under nitrogen atmosphere with H_2O ~ 1 ppm. [147] Some water is required for the hydrolysis and condensation that occurs in processing the metal nitrate precursor to the oxide semiconductor material. Titration experiments have confirmed that the $In(NO_3)_3$ starting material species is coordinated with ~ 2.5 water ligands. This means that some water is available for reaction, even if the inks are prepared in dry atmosphere (glove box). However, it is unknown whether this amount of water is optimal. In an experiment to investigate an aqueous route for In_2O_3, the precursor salt was dissolved in Millipore water and resulted in a white precipitate, which clogged a number of filters when attempting to remove. A colleague (Joana Almeida) who slowly prepared the precursor ink

††† Low ambient humidity is typical indoors in Finland during harsh winter weather where outdoor temperatures plummet significantly below 0°C. Equally, humidity of the working environment is an important factor in areas of elevated humidity such as those close to the equator.

(Section 3.1.1) in air (exposing the metal salt to moisture from ambient humidity) observed a similar phenomenon of a white precipitate, which hindered subsequent ink filtration. These accounts suggest that the presence of an abundance of water limits the potential to produce an optically transparent ink, by restricting mechanical filtration. Controlling the amount of water available to the metal salt during formulation might assist uniform, reproducible ink production. Figure 19 suggests there is an absence of inhomogeneity in an In_2O_3 film produced in 32% RH. Therefore, the question arises as to whether it is possible to prepare the ink under inert conditions (in a glove box) and simply add the required amount of water to replicate a headspace with air of 32% RH. This method might alleviate effects of fluctuating relative humidity such as Figure 19 B. However, it is cumbersome to quantify the amount of water trapped in a bottle headspace as a result of humid air. Table 1 presents a screenshot from a Microsoft Excel spreadsheet devised to estimate the quantity of water in a 5 cm^{-3} headspace of air (typical of this experimental method) with 32% RH at room temperature (21°C) and ambient pressure (101325 Pa).

Table 1. Estimation of water content in the headspace air of a reaction vessel.

Variable	Value	Notes
RH Target relative humidity (%)	32	RH(%)=(PPWV/SVP)*100
T (K)	294.15	Approximate lab T (21°C)
DHA Density of humid air (kg/m^3)	1.200009429	DHA=(PPDA/(GCDA*T))+ (PPWV/(GCWV*T))
PPDA Partial pressure of dry air (Pa)	101322.909	PPDA=(DDA*GCDA)*T
GCDA Gas constant for dry air (J/kg K)	287.05	-
PPWV Partial pressure of water vapour (Pa)	1.28	PPWV=(RH/100)/SVP [mbar])*100
GCWV Gas constant for water vapour (J/kg K)	461.495	-
DDA Density of dry air (kg/m^3)	1.2	Where pressure = 101325 Pa
DWV Density of water vapour (kg/m^3)	9.57335E-06	DWV=(PPWV*0.0022)/T
SVP Saturation vapour pressure at 21°C (mbar)	25	-
Volume of air (cm^3)	5	Headspace of ink bottle
Volume of air (m^3)	0.000005	Vol (m^3) = cm^3 / 1000000
HR Humidity ratio (kg water/ kg moist air)	7.8574E-06	HR=(0.62198*PPWV)/(PMA-PPWV) From the ideal gas law
PMA Pressure of moist air (Pa)	101324.189	PMA=PPDA+PPWV
Mass of water per Vol air (kg/m^3)	6.00005E-06	Mass=DHA*Vol
Mass of water (g)	3.00002E-08	Water required to simulate 32% RH
Density of water (g/cm^3)	0.9982	-

The result from Table 1 suggests $3 \cdot 10^{-5}$ mg of water, per ink formulation batch, which is less than the smallest amount possible to add by micropipette (~ 1 mg). Nevertheless, the concept of working in a dry inert atmosphere (glove box) and

adding a controlled quantity of water to the formulation was trialled. To probe the effect of water content in the semiconductor ink, a set of inks was prepared using the typical method (Section 3.1.1) but with varying amounts of water added. The amount of water added to the sample set was based on the reported uptake of water by anhydrous $In(NO_3)_3$ [162] based on ~ 0.7 g of starting material in each ink. The sample set comprised four inks containing water at 0.005 wt.%, 0.035 wt.%, 0.07 wt.%, and a control with no added water. These may sound like small percentages, but consider that the percentage estimated in Table 1 for a reaction vessel headspace containing air of 32% RH is ~ $3 \cdot 10^{-7}$ wt.% (assuming the headspace air is the only water from external sources). The four inks with varying water contents were spin coated to produce thin films comparable with those presented in Figure 19. The result was that none of the set presented the inhomogeneity noted in the sample prepared in low RH (Figure 19, B). If low humidity caused this strange inhomogeneity, then it might be expected that the control sample prepared with no added water would present an inhomogeneous film. Because this was not the case, it suggests that varying RH might most significantly affect the semiconductor material during spin coating (and subsequent thermal treatment) rather than during ink formulation (except where significant water is available as in the examples above yielding white precipitate). These observations led to all subsequent drying and annealing of semiconductor material done in a controlled RH of ~ 32%.

4.2.3 Solvent removal

Previous research at VTT has resulted in the optimisation of the annealing temperature (300°C) of the semiconductor to remove impurities and achieve maximum charge carrier mobility without an exceptionally high thermal budget. [10] However, the solvent removal (drying) step has received less attention. In an attempt to confirm that the drying temperature of 90°C provides optimum electrical performance, the semiconductor material was dried at a range of temperatures (all for 15 min duration), to produce different TFT devices. The results of this test are plotted in Figure 20 below. Each point on Figure 20 represents data from a sample with a set of eight TFT devices, however the data for each point is obtained from less than eight devices.[‡‡‡] The error bars show the variation between the devices on a given sample. It appears that the optimum charge carrier mobility is achieved when the semiconductor is dried at a temperature of 100°C. A more thorough investigation

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[‡‡‡] All of the samples fabricated during this research were prepared with eight individual TFT devices as explained in Section 4.1. However, it is rare that all eight devices on a given sample will operate due to short circuit issues. For example, pinhole defects which allow electrons to escape through the SiO_2 dielectric.

(including a greater range of temperatures from 70-140°C) is required before certain conclusions could be drawn about whether the devices would benefit from an increased drying temperature > 90°C. Therefore, a drying temperature of 90°C was used for all semiconductor material in this research.

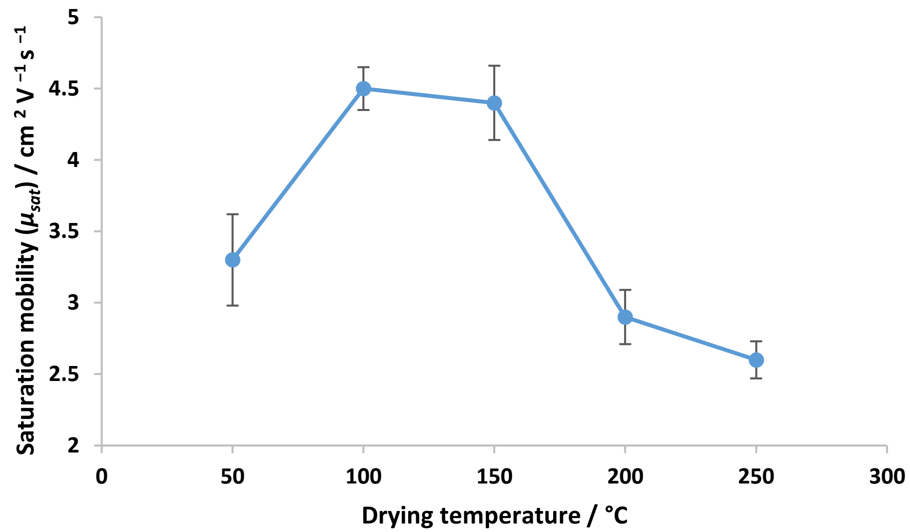

Fig. 20. Effect of semiconductor ink drying temperature on TFT charge carrier mobility.

4.3 Reference devices with Al contacts

To act as a control, a set of reference devices was produced incorporating components recently reported to provide good device performance. [2] Figure 21 presents a schematic of a cross section of such a reference TFT device alongside an image of an actual TFT fabricated during this research, showing Al contacts evaporated onto an inkjet printed In_2O_3 semiconductor layer.

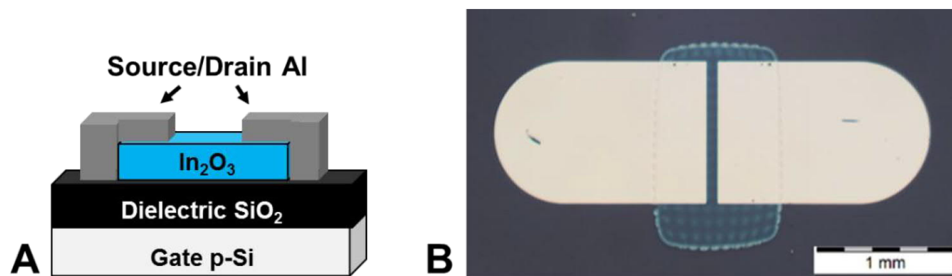

Fig. 21. Cross section schematic (A) and top view micrograph (B) of reference TFT device with evaporated Al source-drain electrodes.

Note that the TFT device depicted in Figure 21 B does not have source-drain electrodes positioned precisely centrally over the printed semiconductor area. This is because the shadow mask, through which Al is evaporated onto samples, allows some free movement of the Si chip samples. Some free movement is required to ensure samples sit flat against the mask plate. However, at such a small scale (of the order of a few microns) even slight movement results in off-centre deposition of evaporated material. This is not a significant issue for the reference devices in Figure 21, but proves troublesome when attempting to align multiple thin film layers with identical channel gap. This alignment difficulty supports the emphasis of developing fully printed TFT fabrication methods.

Electrical characterisation (Section 3.6) of a typical reference sample yielded data presented in Figure 22 below. In this case, data were collected from the five working devices on the sample. Here transfer curves for all five working devices from the sample are presented to illustrate typical differences within a sample set. Please note that further figures within this thesis will typically only include a single transfer curve representative of a given sample set, with the variation in results (e.g. μ) stated as an error margin (±) in the body text.

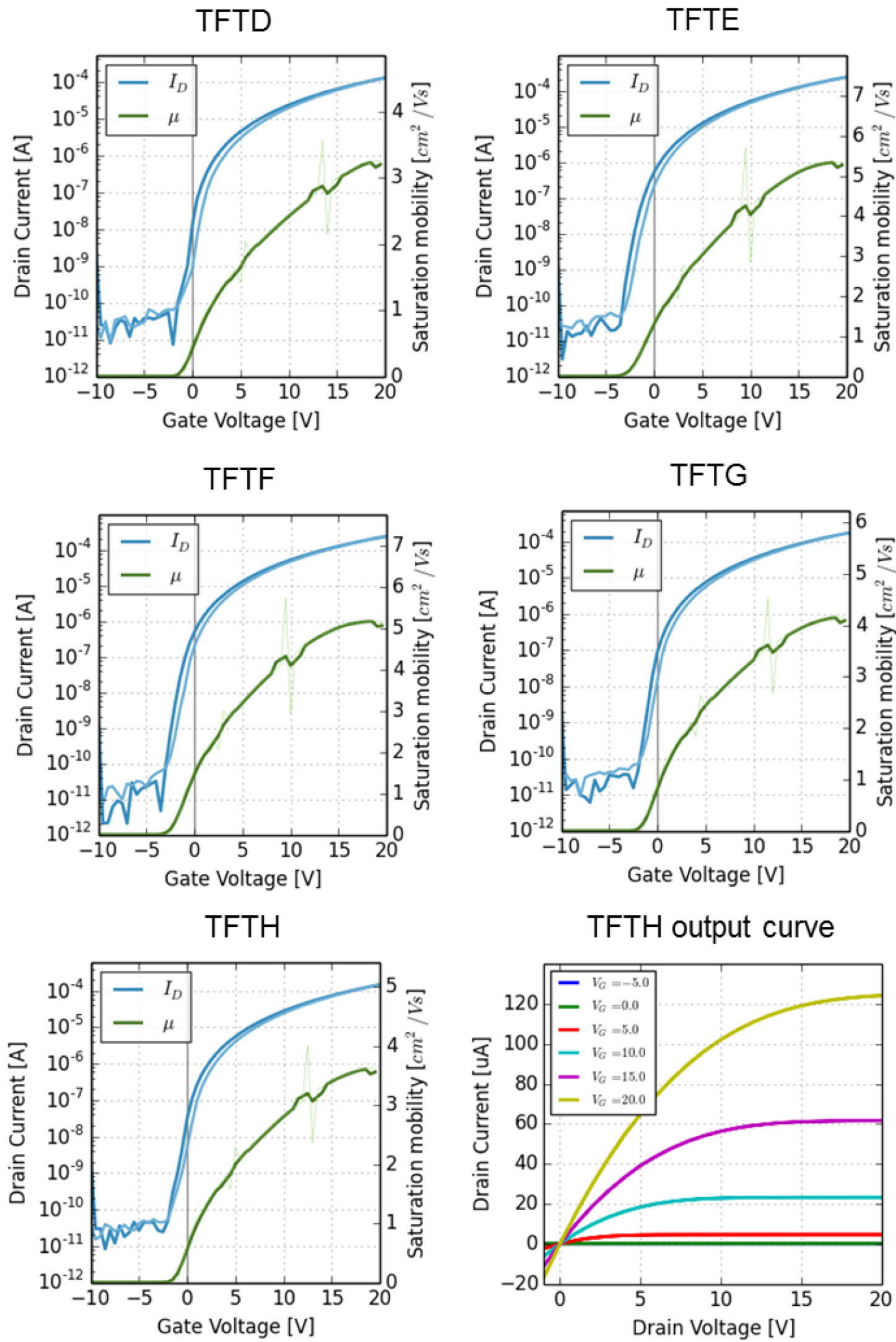

Fig. 22. Electrical characteristics of TFT devices from a reference sample with five working devices from a total of eight. Transfer curves are presented for all working devices, along with one output curve representative of the sample set. Note that transfer curves in this thesis are depicted with I_D sweeps forward and reverse being dark and light blue, respectively.

The Figure 22 transfer curves provide mean results for the sample set listed in Table 2 below. An additional parameter of interest is V_{hyst} of the transfer curve. This

parameter describes the variation between forward and reverse sweeps of the transfer curve, with this sample set showing relatively low V_{hyst} of 0.78 ± 0.07 V. These values are indicative of good TFT performance and provide a basis for comparison with devices fabricated using alternative components (e.g. PEI or Ag).

Table 2. Electrical characteristics of reference devices with Al contacts.

Count	V_{hyst} (V)	I_{ON}/I_{OFF}	V_{ON} (V)	μ_{sat} ($cm^2 V^{-1} s^{-1}$)
5	0.78 ± 0.07	$1.3 \cdot 10^7 \pm 1.7 \cdot 10^7$	-3.1 ± 0.94	4.3 ± 0.93

4.4 Polyethyleneimine interlayer devices with Al contacts

Inkjet printing of PEI has been reported, [163] but not, to the best of our knowledge, as applied to MOS TFTs. A stable ink formulation is required in order to incorporate an inkjet printed thin film of PEI in TFT devices. The first stage in achieving this was to attempt formulation of an ink using the same solvent system as for the semiconductor material. This is because it is known that the solvent system prints well, and the materials were readily available. PEI has been reported to dissolve in 2-ME at a concentrations as high as of 0.4%, [93] so this concentration was selected for this research. The PEI species used in this and the following section (4.5) was anhydrous with high molecular weight (see Chapter 3). An initial trial of dissolving PEI in 2-ME alone proved difficult to print, with ink creeping from the nozzles to wet the nozzle plate. Despite the large size of the PEI molecules, the creeping behaviour suggests that PEI molecules can exit the nozzles. In addition, tailing, poor droplet trajectory, and ink spray residue from nozzles was observed. Addition of 10 wt.% EG (as per the semiconductor formulation) resulted in well resolved droplet formation presented in Figure 23 below.

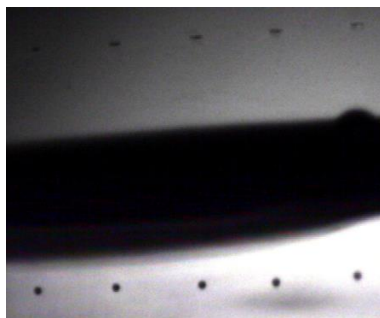

Fig. 23. Strobograph of stable droplet formation from PEI ink.

Despite the PEI ink forming well-resolved droplets, it proved difficult to print patterns with clearly defined edges. Drop spacings of 50, 75, and 125 μm were printed onto In_2O_3 (prepared by spin coating), with 75 μm drop spacing providing the best resolution. However, the PEI ink behaved differently when the same process was applied on printed In_2O_3. The as printed PEI ink poorly wetted the semiconductor material with what appears to be a high θ_C (Figure 24, A). Application of a second ink layer (Figure 24, B) with no drying step between gave a channel with scalloped edges and provided a film of PEI that might be too thick for sufficiently low R_C. A reduction in drop spacing may improve wetting by coalescing individual droplets, but would also increase the layer thickness in a similar manner to the double layer of PEI with 75 μm drop spacing.

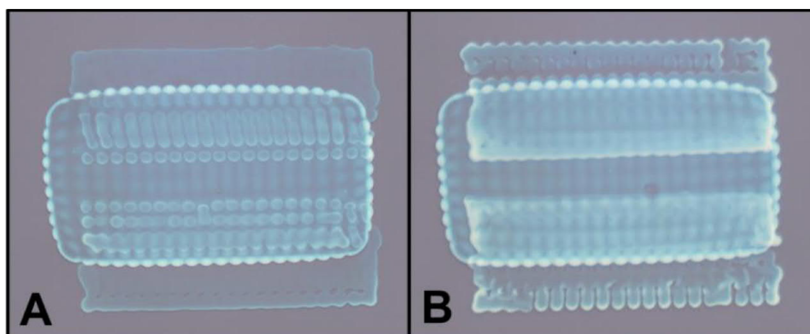

Fig. 24. PEI ink as printed in single (A) and double (B) layers on In_2O_3.

Treatment of the In_2O_3 using the minimum available plasma (6 s, Ar) altered the surface energy of the semiconductor such that the result was significantly improved surface wetting by PEI. It also appeared that the increased wetting caused the PEI ink to spread into a thinner film, which is a desirable result. Design of a print pattern to suit the new wetting behaviour resulted in control of a defined channel length and width. However, close inspection of the channel gap reveals that the morphology of

the In_2O_3 (retained from the printing process) appears to cause the PEI ink to creep across peaked areas with a poorly defined edge (Figure 25).

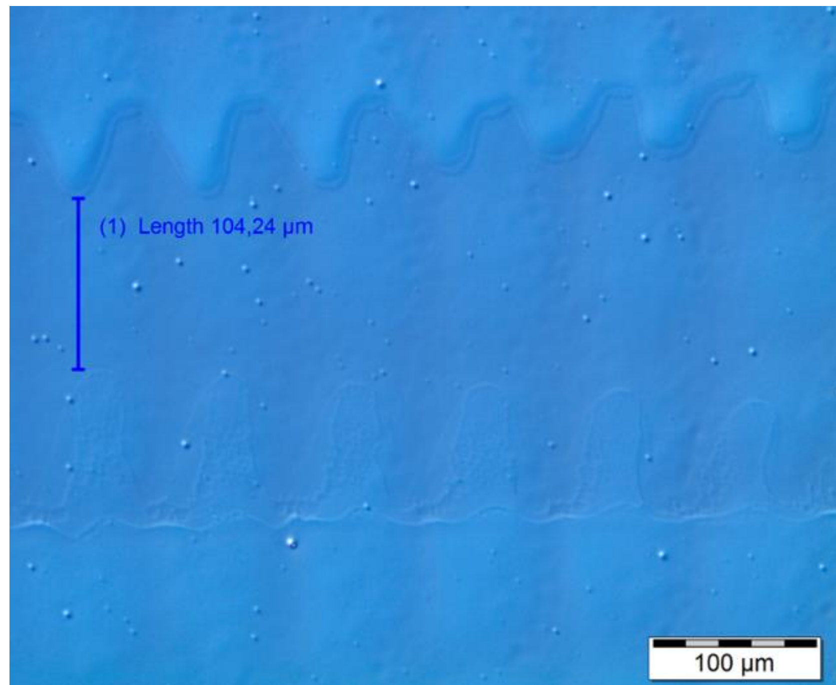

Fig. 25. Micrograph of two areas of printed PEI ink creeping towards one another across the plasma treated In_2O_3 surface.

Prior to source-drain contact deposition, post-printing treatment was required to remove residual solvent from printed PEI thin films. It is known that PEI decomposition commences from 250°C, [164] so thermal treatment of PEI ink would ideally be less than this. Therefore, samples were dried at 200°C to ensure solvent removal without compromising the molecular integrity of the PEI. Another benefit of a low thermal budget is the compatibility of processing TFTs on temperature sensitive substrates. Ideally the method could be altered to enable a thermal budget of < 150°C for compatibility with transparent, flexible substrates such as PET or PEN.

Following the drying step, evaporation of Al source-drain electrodes yielded operational devices, with electrical characteristics of a representative TFT presented in the transfer curve depicted in Figure 26 below.

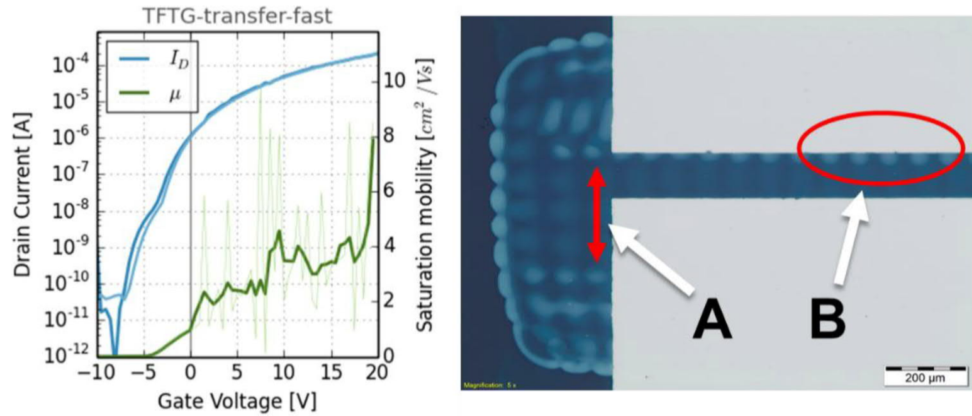

Fig. 26. Transfer curve of TFT (left) incorporating printed PEI and Al source-drain contacts. Micrograph of same device (right) showing poor alignment of contacts (large grey areas) with respect to PEI channel area (A) resulting in PEI material within the TFT channel between the contacts (B).

Mean results for the sample set are given in Table 3, which imply that the PEI layer does not adversely affect device performance significantly. Shift of transfer curve to a more negative gate voltage suggests that PEI might act to *n*-dope the devices as was expected, which is promising for applications with Ag contacts.

Table 3. Electrical characteristics of devices with PEI and Al contacts.

Count	V_{hyst} (V)	I_{ON}/I_{OFF}	V_{ON} (V)	μ_{sat} ($cm^2 V^{-1} s^{-1}$)
3	0.7 ± 0.3	$9.2{\cdot}10^6 \pm 8.4{\cdot}10^6$	-7.1 ± 1.0	5.6 ± 2.0

The overall result from Section 4.4 is that defining a TFT channel length by alignment of multiple layered materials is troublesome, particularly using the evaporation equipment provided. However, addition of PEI appears to *n*-dope the TFT devices, shifting V_{ON} more negative, and increasing μ_{sat} such that these observations warrant further experiments with Ag contacts.

4.5 Polyethyleneimine composite devices with Al contacts

Recent research reports fabrication of well performing TFTs with In_2O_3 semiconductor doped with 1% PEI to form a-MOS material. [44] These reported devices comprised *p*-Si gate, SiO_2 dielectric, three spin coated layers of composite material, and evaporated Al source-drain. Incorporation of PEI composite increased

μ from 4.18 ± 0.11 $cm^2 V^{-1} s^{-1}$ (no PEI) to 8.37 ± 0.28 $cm^2 V^{-1} s^{-1}$ (with PEI). To build on this work, this research formulated an ink for a similar composite material with 1% PEI. Devices were fabricated by inkjet printing the 1% PEI composite as the semiconductor material. PEI ink (Section 4.4). The results of which are presented in Figure 27, which shows a typical device and associated transfer curve. Note the less clearly defined edge of the PEI containing semiconductor in comparison with pure In_2O_3 in Figures 17 and 21 B.

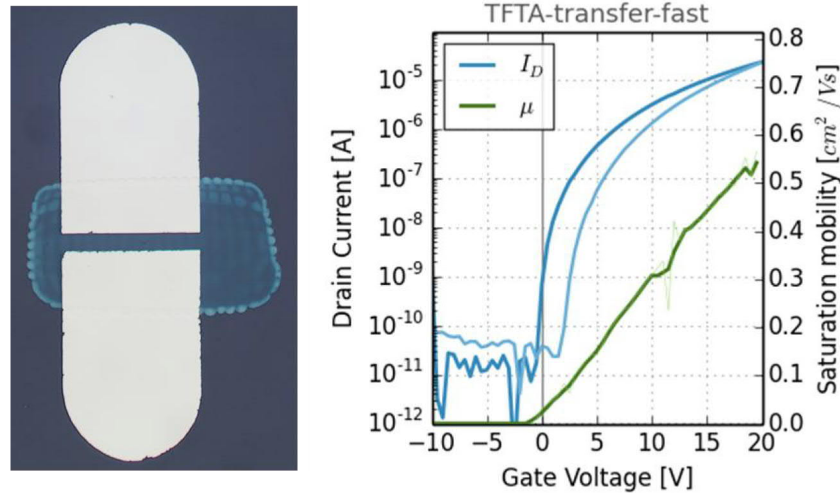

Fig. 27. Micrograph (left) and transfer curve (right) of a TFT device with Al contacts over In_2O_3 semiconductor containing 1% PEI.

Despite V_{ON} close to zero, the electrical performance of this double layer printed sample set is poorer than the triple layer spin coating method reported in the literature,[44] with some hysteresis and low μ. Data obtained for the sample set appear in Table 4 below.

Table 4. Electrical characteristics of devices with PEI doped semiconductor and Al contacts.

Count	V_{hyst} (V)	I_{ON}/I_{OFF}	V_{ON} (V)	μ_{sat} ($cm^2 V^{-1} s^{-1}$)
7	3.7 ± 0.74	$2.3 \cdot 10^6 \pm 8.5 \cdot 10^5$	-1.2 ± 0.48	0.55 ± 0.032

Next, the PEI composite ink was deposited according to the print pattern for PEI ink described in Section 4.4. Printing of the PEI composite ink proved significantly easier than that of the PEI ink, with a more clearly defined edge between the two areas of ink printed on each device. Subsequent evaporation over the printed material resulted in devices with some composite material in the TFT channel area, but fairly well aligned. Figure 28 provides a representative image of such a device, along with its transfer characteristics.

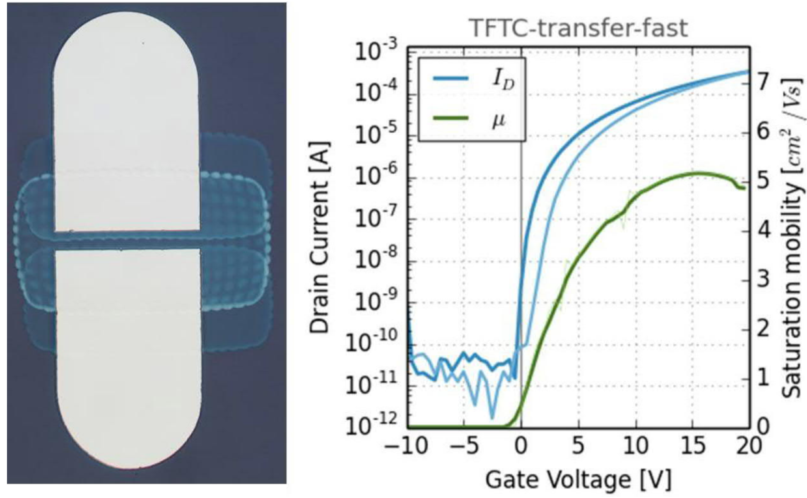

Fig. 28. Micrograph (left) and transfer curve (right) of a TFT device with Al contacts over 1% PEI in In_2O_3, printed over In_2O_3 semiconductor.

Unfortunately, only two of the eight devices on the Figure 28 sample were operational. Nevertheless, the electrical characteristic data yielded by the sample set are given in Table 5.

Table 5. Electrical characteristics of devices with PEI composite and Al contacts.

Count	V_{hyst} (V)	I_{ON}/I_{OFF}	V_{ON} (V)	μ_{sat} ($cm^2 V^{-1} s^{-1}$)
2	1.8 ± 0.13	$2.1 \cdot 10^7 \pm 1.4 \cdot 10^7$	-1.3 ± 0.26	4.6 ± 0.84

The results observed in this section (4.5) suggest that a layer of 1% PEI in In_2O_3 could enhance TFT device performance through increased μ. Experiments to this point using evaporated Al source-drain contacts have paved the way by providing reference data to compare and contrast with devices fabricated using printed Ag source-drain electrodes.

4.6 Reference devices with Ag contacts

Seeking to satisfy demand for fully printed MOS TFTs has led to investigation of inkjet printed Ag as source-drain contacts. However, device performance is still relatively low. [80] The aim of this research was to develop a path for improved device performance of TFTs incorporating inkjet printed source-drain contacts. Successful fabrication of inkjet printed source-drain contacts requires a method for

deposition of Ag ink with good spacial resolution to ensure a defined TFT channel area. Some optimisation of Ag ink printability was required to realise this. For example, construction of a suitable waveform (Appendix A) assisted stable droplet formation (Figure 29).

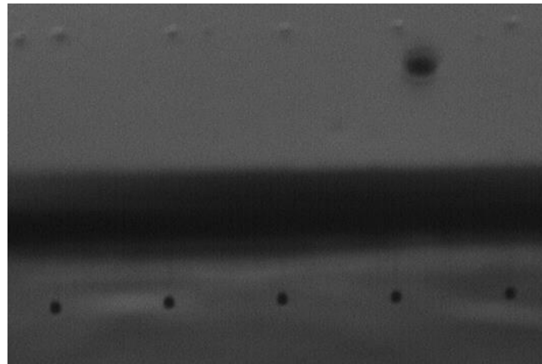

Fig. 29. Strobograph showing stable Ag ink droplets.

The semiconductor required plasma treatment (12 s, Ar) for sufficient wetting by the Ag ink. Various drop spacings were trialled (Figure 30), with 40 μm selected to provide the cleanest edge for printed areas, avoiding scalloping or bulging.

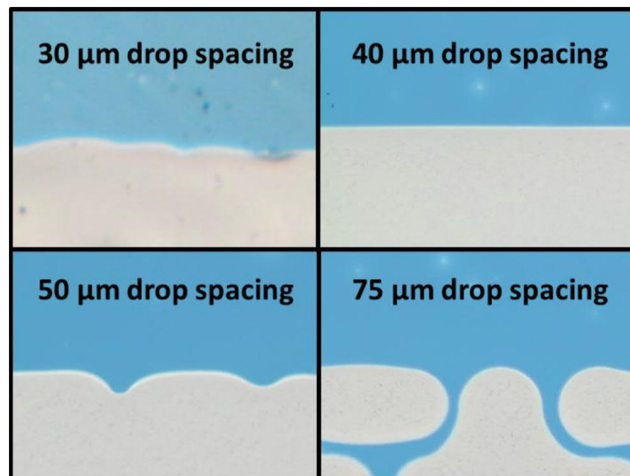

Fig. 30. Various drop spacings of Ag ink printed on In_2O_3.

Literature suggests printing Ag ink onto a substrate of elevated temperature (> 30°C) might provide high μ and low R_C. [80,83,85] To investigate this, a number of different platen temperatures were trialled, however solvent evaporation resulted in presence of areas suffering from coffee ring effect (Figure 31 left). In addition, increasing platen temperature caused increased wetting of the semiconductor,

resulting in reduction of channel length (Figure 31, right) These observations led to all further Ag printing done with a platen temperature of 30°C.

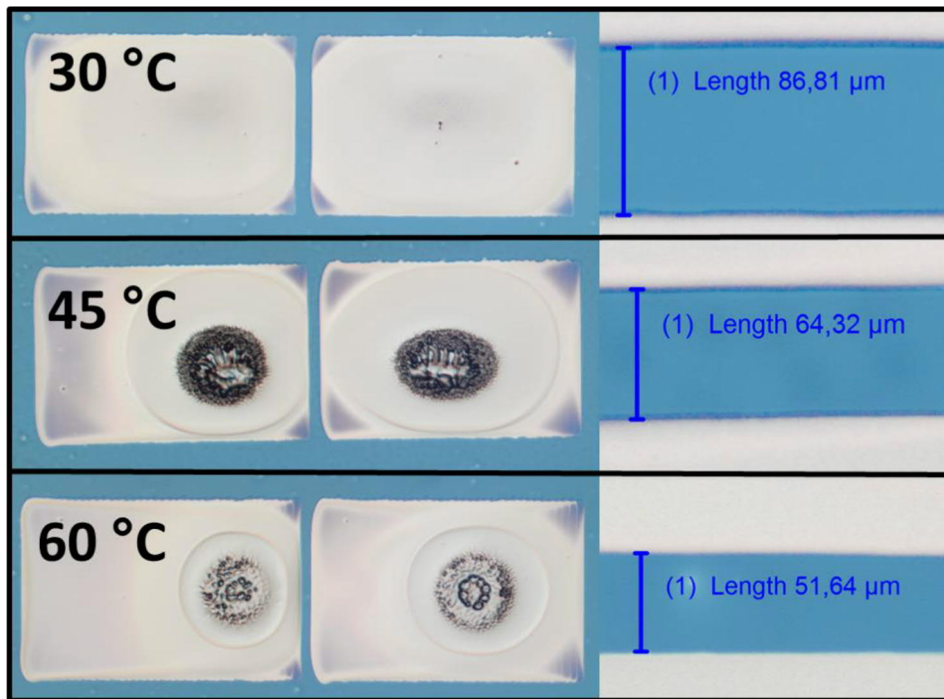

Fig. 31. Inkjet printed Ag on In_2O_3 showing effect of increasing platen temperature on solvent evaporation related coffee ring effect (left) and reduction of TFT channel length (right).

The Ag selected for use contains nanoparticles of active metal component, which requires post printing thermal treatment, for solvent removal and sintering of nanoparticles to obtain optimum material conductivity. For this thermal treatment, a temperature of 150°C (30 min duration) was selected to allow compatibility with thermo sensitive device components (e.g. PEI, PET, or PEN). Use of a hotplate for such treatment resulted in coffee ring effect (similar to Figure 30 observations), even when temperature was increased with stepwise increments (75°C, 15 min > 90°C, 15 min > 150°C 30 min). Single step thermal treatment of 150°C, 30 min in an oven (rather than hotplate) alleviated this issue.

Using the optimised printing detailed above, devices were fabricated with inkjet printed Ag over In_2O_3, with layer dimensions replicating devices with Al contacts (Section 4.3). This enables comparison of TFT performance from inkjet printed Ag, to evaporated Al source-drain electrodes. Figure 32 presents a micrograph (left) and transfer curve (right) of a TFT device with Ag contacts.

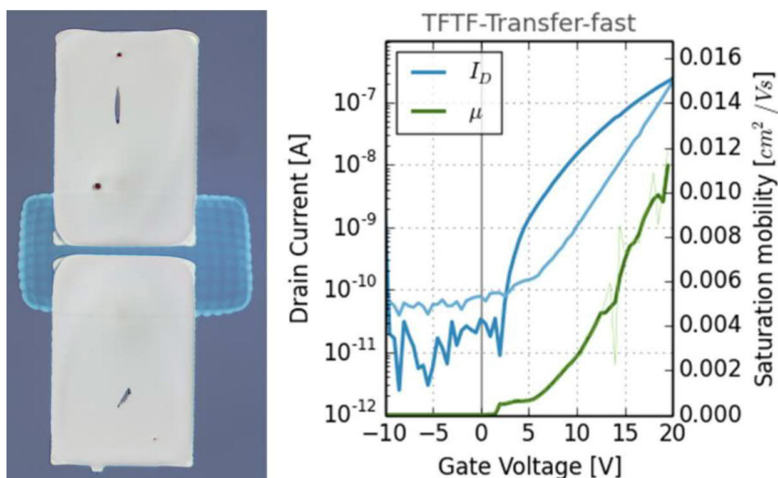

Fig. 32. Micrograph (left) and transfer curve (right) of a TFT device with inkjet printed Ag source-drain contacts.

A sample containing a set of six devices provided the results presented in Table 6 below. These results are significantly poorer than observed from TFTs with Al contacts. Notably, the Ag results in large V_{hyst} and low μ. This result provides the expected confirmation that Ag contacts yield devices with inferior performance in comparison to those with Al contacts.

Table 6. Electrical characteristics of reference devices with Ag contacts.

Count	V_{hyst} (V)	I_{ON}/I_{OFF}	V_{ON} (V)	μ_{sat} ($cm^2 V^{-1} s^{-1}$)
6	6.3 ± 1.2	$6.3 \cdot 10^3 \pm 3.0 \cdot 10^3$	-0.11 ± 4.0	$8.0 \cdot 10^{-3} \pm 3.9 \cdot 10^{-3}$

4.7 Polyethyleneimine interlayer devices with Ag contacts

To evaluate whether the presence of PEI assists the performance of TFTs with Ag contacts, devices were produced with a thin film of PEI printed between the semiconductor and contact material. The Ag contacts proved significantly easier to align with the PEI defined TFT channel than was experienced with evaporated Al. Representative device micrograph and transfer curves are presented in Figure 33.

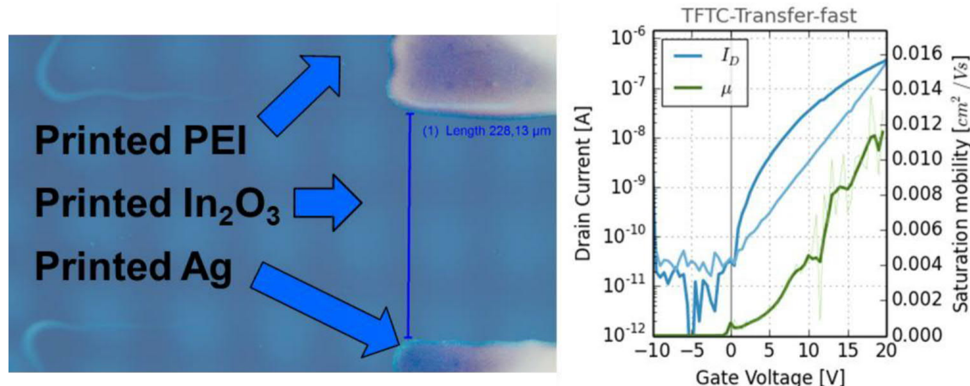

Fig. 33. Micrograph (left) and transfer curve (right) of a TFT comprising three sequentially inkjet printed layers.

The result of this sample set is somewhat underwhelming, yielding the characterisation data in Table 7. This data does not suggest that a layer of PEI provides any significant electrical improvement to TFTs with Ag contacts. It is possible that the deposited PEI layer is of a thickness such that it causes insulating behaviour, challenging tunnelling or conduction of electrons.

Table 7. Electrical characteristics of devices with PEI and Ag contacts.

Count	V_{hyst} (V)	I_{ON}/I_{OFF}	V_{ON} (V)	μ_{sat} (cm^2 V^{-1} s^{-1})
6	6.5 ± 1.2	$9.7 \cdot 10^4 \pm 7.2 \cdot 10^4$	-1.7 ± 1.2	$3.4 \cdot 10^{-2} \pm 3.2 \cdot 10^{-2}$

4.7.1 SU-8 defined channel

It is possible to define the channel with an additional material to alleviate issues aligning multiple thin film layers such that a well-defined channel is obtained. For example, printing a strip of material directly onto the semiconductor at the desired TFT channel *L*, might reduce the effect of variation in distance between subsequent layer depositions, and even allow a defined channel *L* beneath spin coated material. In this case, SU-8 (an epoxy-based material commonly used as a photo resist) was selected for the task. The method for inkjet printing of SU-8 was optimised (Chapter 3) to ensure a well-defined TFT channel *L*, then subsequently spin coated with PEI, before printing Ag contacts. A representative device from this method is displayed in Figure 34, along with its transfer curve.

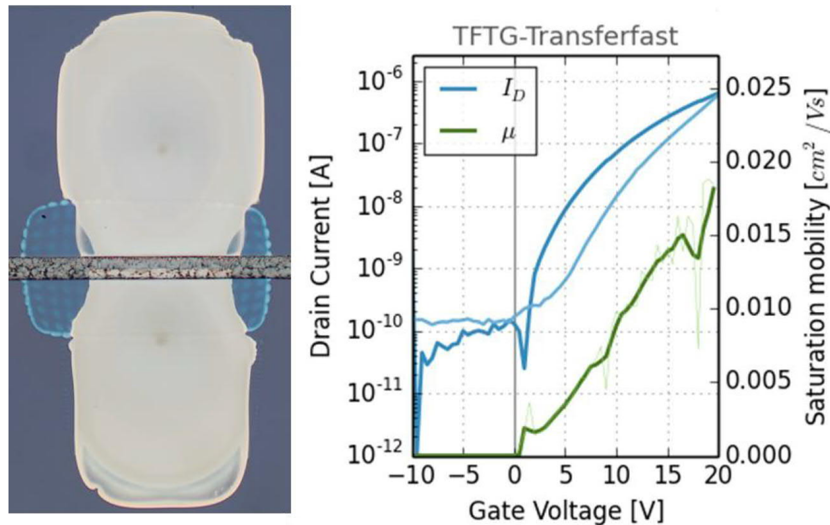

Fig. 34. Micrograph (left) and transfer curve (right) of a TFT with a printed SU-8 defined channel *L* over printed In_2O_3, spin coated PEI, and printed Ag contacts.

The data gained from the sample that provided the results in Figure 34 is given in Table 8, along with results from a similar sample fabricated using lower molecular weight aqueous PEI. It appears that the smaller mass polymer provides marginally greater performance. Unfortunately, these results do not incite much enthusiasm for the SU-8 defined channel and the aim is to fabricate printed devices, so the spin coated PEI route was abandoned.

Table 8. Electrical characteristics of spin coated PEI devices with an SU-8 defined TFT channel and Ag contacts.

	Count	V_{hyst} (V)	I_{ON}/I_{OFF}	V_{ON} (V)	μ_{sat} ($cm^2 V^{-1} s^{-1}$)
Lg M_w PEI	6	4.2 ± 0.94	$1.8 \cdot 10^4 \pm 2.2 \cdot 10^4$	0.37 ± 0.93	$1.9 \cdot 10^{-2} \pm 5.2 \cdot 10^{-3}$
Sm M_w PEI	2	8.7 ± 1.5	$5.2 \cdot 10^4 \pm 1.4 \cdot 10^4$	-2.6 ± 0.89	$5.1 \cdot 10^{-2} \pm 2.7 \cdot 10^{-2}$

4.8 Polyethyleneimine composite devices with Ag contacts

For comparison of Ag contacts with the Al contact devices fabricated with PEI composite as the semiconductor material, TFTs were fabricated using two inkjet printed layers of 1 wt.% PEI:In_2O_3 as the semiconductor, with Ag source-drain contacts subsequently printed. Unfortunately, the results (Table 9) show that the

alternative semiconductor does not greatly enhance device performance in comparison with the reference Ag sample set (Table 6).

Table 9. Electrical characteristics of devices with PEI:In_2O_3 composite as semiconductor, with Ag contacts.

Count	V_{hyst} (V)	I_{ON}/I_{OFF}	V_{ON} (V)	μ_{sat} ($cm^2 V^{-1} s^{-1}$)
7	5.9 ± 0.49	$1.7 \cdot 10^4 \pm 9.3 \cdot 10^3$	-0.58 ± 0.71	$2.2 \cdot 10^{-2} \pm 9.3 \cdot 10^{-3}$

Despite the poor performance of devices incorporating PEI composite as the semiconductor itself, the high μ_{sat} provided by including the composite of 1 wt.% PEI in In_2O_3 detailed in Section 4.5 warrants investigation of the material as a thin film between In_2O_3 and Ag contacts. As a result, devices were prepared by sequentially inkjet printing thin films layers of In_2O_3 semiconductor, PEI:In_2O_3 composite, and Ag source-drain contacts. 1 wt.% PEI:In_2O_3 composite materials were prepared using both aqueous (50 wt.% in H_2O) and anhydrous PEI as detailed in Section 3.1.3. The following data (Table 10) obtained from devices incorporating aqueous PEI suggest no significant improvement from Ag reference devices omitting the composite (Section 4.6).

Table 10. Electrical characteristics of devices incorporating aqueous PEI:In_2O_3 composite and Ag contacts.

Count	V_{hyst} (V)	I_{ON}/I_{OFF}	V_{ON} (V)	μ_{sat} ($cm^2 V^{-1} s^{-1}$)
7	5.9 ± 0.49	$1.7 \cdot 10^4 \pm 9.3 \cdot 10^3$	-0.58 ± 0.71	$2.2 \cdot 10^{-2} \pm 9.3 \cdot 10^{-3}$

It is possible that thermal decomposition (during annealing) of the relatively small polymer chains degrades the PEI, rendering it ineffective for device enhancement. In addition, the added water content may influence the results. Fabrication of devices with a layer of PEI composite from anhydrous PEI yielded the TFT and associated transfer curve presented in Figure 35 below (transfer curves for other TFTs from the sample set are presented as supporting information in Appendix B).

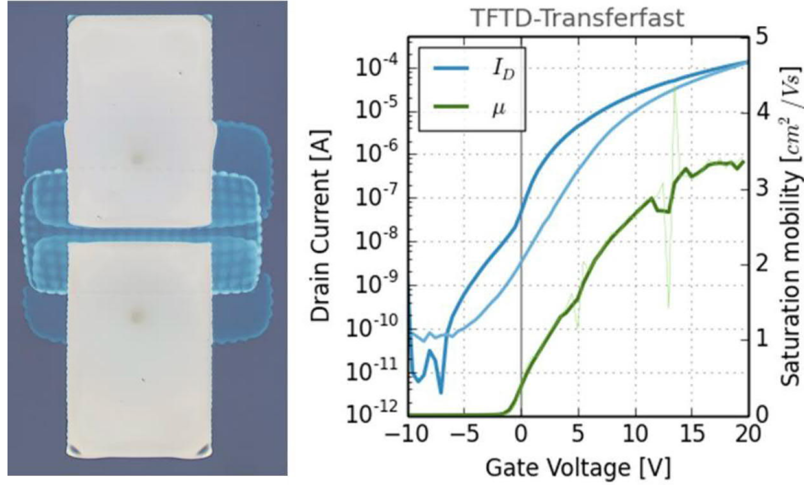

Fig. 35. Micrograph (left) and transfer curve (right) of a TFT device with Ag contacts over 1% PEI in In_2O_3, printed over In_2O_3 semiconductor.

Table 11 presents electrical characterisation data from the Figure 35 sample set. The devices from this sample set are arguably the most exciting from this research, exhibiting exceptionally high charge carrier mobility for printed Ag contacts. Device performance from this sample set is comparable to that of reference TFTs with evaporated Al contacts (Section 4.3).

Table 11. Electrical characteristics of devices incorporating anhydrous PEI:In_2O_3 composite and Ag contacts.

Count	V_{hyst} (V)	I_{ON}/I_{OFF}	V_{ON} (V)	μ_{sat} ($cm^2 V^{-1} s^{-1}$)
7	5.0 ± 0.87	$5.2 \cdot 10^6 \pm 5.1 \cdot 10^6$	-6.4 ± 0.93	3.1 ± 0.53

A significant kink is observed at V_G ~ 0 V in Figure 35. It is possible that this occurs due to the shortening of the TFT channel by introduction of the additional (composite) layer between the contacts and the semiconductor. Here an alternative pathway is provided for the charge carriers. This reduced channel length becomes evident as an additional transfer curve (where $V_G < 0$ V) which disappears as it is consumed by the curve from the longer channel (where $V_G > 0$ V). This suggested explanation of an additional current path in the TFT channel is known as parasitic resistance behaviour. [165]

A final experiment can confirm that inclusion of the PEI composite is the cause for enhanced electrical behaviour, not simply the increased thickness of the In_2O_3 semiconductor material. To answer this, devices were prepared with an additional layer of semiconductor as per the above, but omitting the PEI component from the composite to obtain Table 12 results. The obtained μ_{sat} data strongly contrasts that of devices with PEI composite. Therefore, it is concluded that additional In_2O_3 alone

is not responsible for the observed improvement in device performance. This result suggests the potential for development of TFT devices with inkjet printed source-drain contacts, to alleviate cumbersome evaporation processes.

Table 12. Electrical characteristics of devices incorporating additional In_2O_3 in the PEI pattern, with Ag contacts.

Count	V_{hyst} (V)	I_{ON}/I_{OFF}	V_{ON} (V)	μ_{sat} (cm^2 V^{-1} s^{-1})
7	5.2 ± 1.6	$5.3 \cdot 10^4 \pm 4.6 \cdot 10^4$	-8.8 ± 0.6	0.14 ± 0.031

A plausible explanation for the positive result gained in this section is that the composite precursor ink forms a material of amorphous phase, containing free electron pairs. a-MOS components are known to enhance TFT device performance as described in Section 2.2.1. It is reported that PEI doped In_2O_3 might frustrate crystallisation to assist formation of amorphous material. [44] A possible mechanism for this observation is hereby proposed.

Just as the tetramethylammonium molecule (Figure 11) possesses a partial positive charge on the nitrogen atom, so too does a tertiary amine in PEI that becomes protonated (bonded to an additional hydrogen atom) to become quaternary. [166] Such protonation occurs where pH < pK_a (pK_a for ammonium is 9.25). Such conditions exist in an acidic solution (~ pH 4.5) of 1% PEI:$In(NO_3)_3$ in 2-ME and EG, the precursor ink used to generate the PEI composite material in this work. This positive charge on PEI nitrogen atoms likely has affinity for negatively charged species. This assumption is supported by reports that PEI binds with anionic metal complexes, [167,168] and has been used as a stabiliser for suspension of colloids bearing negative surface charge. [169] It is possible that the In (III) species in the ink is coordinated such that the overall complex possesses negative charge. This is difficult to determine, however it may be possible if the coordination complex contains hydroxo or nitrato species. If so, then given the low pH in the ink, positively charged PEI molecules would likely coordinate with negative indium complex species and could lead to a uniform distribution as the polymer prevents convergence of indium species. This uniform distribution, with PEI molecules acting as a barrier to singular crystal formation, might assist in formation of an amorphous product at sufficiently low annealing temperature. However, elevating the thermal budget > 300°C may lead to single crystal development, [10] particularly at temperatures causing significant PEI decomposition. Thermal decomposition of solvents, nitrates and water from the precursor ink means PEI is no longer protonated following annealing.[§§§] Therefore, after annealing of the composite

[§§§] It is possible that there is some thermal degradation of PEI molecules at an annealing temperature of 300°C.[164] However, some residual nitrogen species possessing lone pairs

material, PEI nitrogen atoms have a lone pair of electrons available for donation to enhance negative charge carrier μ, or to act as traps for positive charge carriers (holes). When Ag is subsequently printed on this material, the PEI lone pairs could coordinate with Ag cations and lead to covalent bonding to lower R_C, resulting in improved charge carrier injection through to the semiconductor. Thus, providing an explanation for the observed increase in μ_{sat} for devices incorporating the PEI composite as an interfacial layer.

likely remain, as indicated by the enhanced device performance compared to TFTs omitting the composite material.

Chapter 5
Summary and outlook

The research question for this work was whether PEI might assist the electrical performance of TFT devices with inkjet printed Ag source-drain contacts. This was answered with the positive result that TFT device performance is enhanced by inclusion of an inkjet printed interfacial layer incorporating PEI. The outcome of the research was successful fabrication of devices with printed Ag contacts that exhibit comparable performance to those with evaporated Al contacts. This result suggests the possibility for production of fully printed TFTs, with reduced cost and increased product throughput when compared to current industrial methods such as vacuum deposition.

This work proposes a mechanism for the observed increase in device performance, considering pH related behaviour and thermal degradation of the PEI composite precursor ink formulation. It is suggested that the PEI composite likely assists TFT device performance by promoting formation of amorphous phase material containing free electron pairs, which acts as an *n*-doped bridging species that leads to reduced R_C at the contact-semiconductor interface.

Figure 36 below presents a summary of experimentally obtained transfer curves, depicting the significant improvement of μ_{sat} in TFTs with printed Ag contacts resulting from incorporation of an interfacial layer of PEI composite between the semiconductor and source-drain contacts.

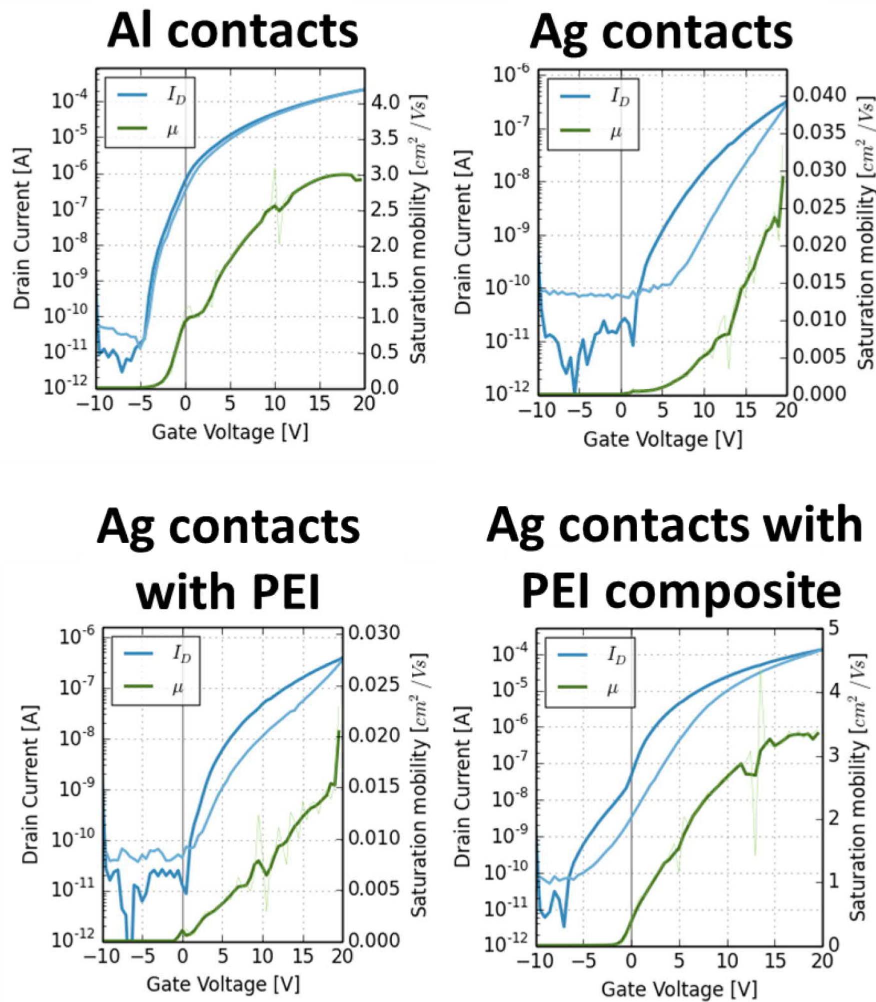

Fig. 36. Graphical summary of the research results, with transfer curves representative of each sample set showing how poor μ_{sat} of TFTs with printed Ag source-drain contacts can become comparable to devices with evaporated Al contacts by incorporation of PEI:In_2O_3 composite.

The results from this work generate questions that might be addressed by further research. For example, devices with an interfacial layer of PEI did not appear to perform as well as those with the PEI composite (Figure 36). In the former, it is possible that there was an excess of PEI material forming a barrier to electron conduction or tunnelling. A lower concentration of precursor PEI ink (< 0.4 wt.%) might alleviate this problem. Another approach could be to wash the excess material after a given time period. This assumes that the PEI in the printed ink would form a self-assembled monolayer (SAM) on the oxide. Washing might selectively remove excess PEI molecules whilst retaining the SAM. This form of washing has been reported for PEI in other applications. [159,160,170]

Formulation of a PEI:Ag composite ink might prove fruitful in assisting the contact-semiconductor interface. Polymer blends with Ag nanoparticle inks have been trialled by other groups. [171] In addition, further optimisation of sintering conditions for the printed Ag may enhance device performance.

X-ray diffraction experiments could confirm that the PEI composite material is amorphous, in support of the proposed mechanism for enhanced μ_{sat} (Section 4.8).

Thermogravimetric analysis (TGA) might provide information on the decomposition of PEI, to probe whether the drying temperature of the PEI ink might be reduced to enable processing on transparent, flexible polymer substrates such as PET or PEN.

This work developed a method for inkjet printing of SU-8, which could be exploited to encapsulate the TFT devices for enhanced longevity. A thin film encapsulation of SU-8 might protect against environmental influences such as device degradation from moisture and atmospheric gases.

Using In_2O_3 semiconductor with the PEI:In_2O_3 composite on PET or PEN substrates and TCO contacts (e.g. ITO) could help develop transparent, fully inkjet printed MOS TFT devices.

In conclusion, this research has proven that MOS TFT devices with inkjet printed source-drain electrodes are enhanced by the interfacial engineering of PEI addition between the semiconductor and source-drain contacts. It is likely that this approach will be further improved using PEI, or another species, to realise practical applications.

Reports of well performing metal oxide TFTs with printed Ag source-drain contacts could not be located during the literature review of this thesis. As such, the research findings herein appear novel. The results of this and ongoing research will be presented at an international conference in late 2017 and will likely be reported in a scientific journal.

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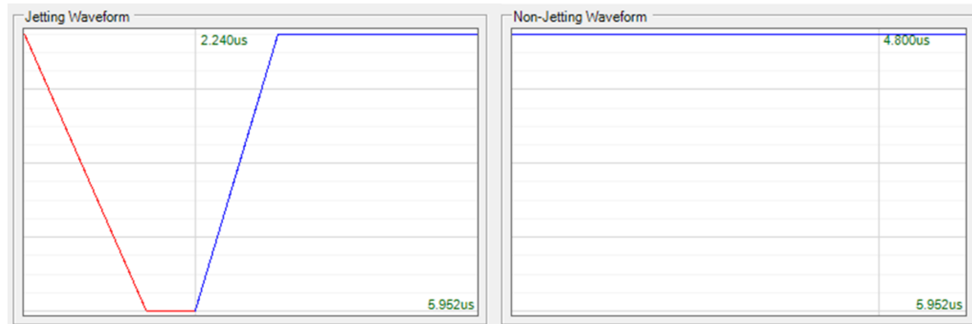
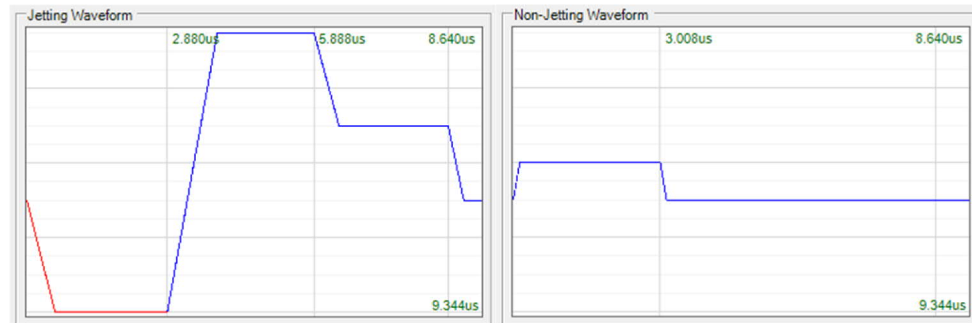
Appendices

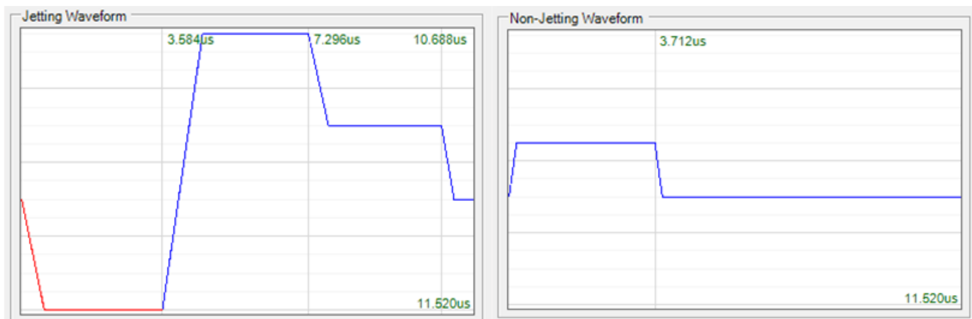
Appendix A – Inkjet waveforms



Inkjet printing waveform for In_2O_3 precursor ink.

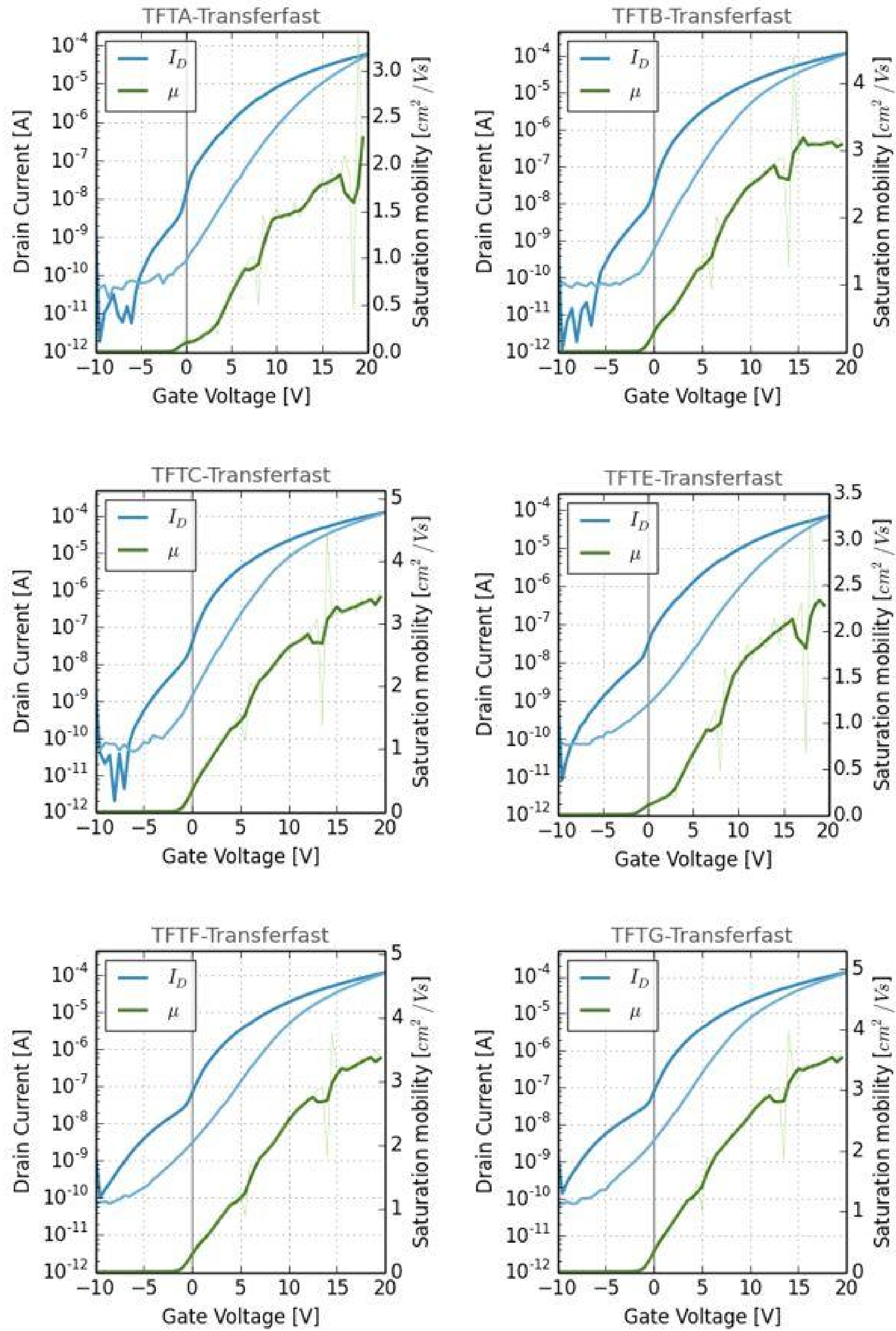


Inkjet printing waveform for PEI precursor ink.



Inkjet printing waveform for SU-8 precursor ink.

Appendix B – Section 4.8 supporting information



TFT transfer curves from a sample set with printed In_2O_3 semiconductor, printed 1 wt.% PEI:In_2O_3, printed Ag source-drain contact electrodes.