Opening the Box: Survey of High Power Density Inverter Techniques From the Little Box Challenge

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Abstract—**The Little Box Challenge (LBC) was a competition sponsored by Google and the IEEE Power Electronics Society in 2014-2015, where participants were challenged to design a high power-density single-phase 2 kVA inverter. This paper surveys the designs from eight different participating teams, including academic grant awardees, finalists, and the winners. Inverter topologies, power decoupling circuits, and thermal management strategies are overviewed for each team. Wide bandgap switches were heavily utilized in both the inverter and power decoupling circuits, particularly GaN switches. Most teams utilized a full-bridge inverter with some variations and the most common power decoupling strategy was the use of a synchronous buck converter and a power buffering capacitor. One team used a multi-level inverter approach and a number of teams proposed innovative power decoupling topologies. Heat sinks and active cooling systems, many of which were custom made, were crucial for teams to stay within the 50 °C case temperature limit. The resulting power density of the surveyed teams ranged from 55.8 to 216 W/in^3, all of which exceed the 50 W/in^3 LBC requirement. This paper surveys the approaches for various teams, shares experimental results from the Taiwan Tech team, and highlights some innovations from the teams that participated in the LBC.**

Index Terms—**Higher power density, Little Box Challenge, single-phase inverter, wide bandgap switches.**

I. Introduction

HIGH power density converters are an important trend in power electronics for many modern applications, including electric vehicles and renewable energy. In light of this trend, Google and IEEE Power Electronics Society announced the Little Box Challenge (LBC) in July 22, 2014 to incite innovation and developments for high power density inverters. Specifically, the LBC called for designs and testable prototypes of a single-phase inverter rated at 2 kVA with a power density of at least 50 W/in^3. The LBC provided detailed specifications and testing requirements, detailed in [1]. A grand prize of 1 million USD would be awarded to the team that developed a single-phase inverter with the highest power density that met the requirements.

Google Research also announced that it would provide academic research grants to institutions to support research on high power density converters for the LBC. The academic research grants were awarded in December 2014 [2]. The list of awardees is provided in Table I. Competitors were required to submit a Technical Approach and Testing Application document for their proposed inverter designs by July 22, 2015. Based on those documents, 18 finalists were selected to submit prototypes for testing. The list of finalists is also listed in Table I, however three teams dropped out of the competition before final testing. The prototypes were submitted by October 21, 2015 and subject to testing at the Renewable Energy Laboratory (NREL). In February 2016, the CE+T Power's Red Electrical Devils team from industry was announced as the winner with 142.9 W/in^3 power density, with the Schneider Electric team in second with 96.2 W/in^3, and Virginia Tech's Future Energy Electronics Center in third with 68.7 W/in^3 [3].

The competition results were exciting news that generated positive public attention for the power electronics community [4], but the more significant results are in the innovations and technological advances that came from various teams participating in the LBC. The purpose of this paper is to survey the design approaches and techniques utilized by various teams to achieve the target high power density inverter. Although the Technical Approach documents were shared for all the finalists, they do not generally contain deep technical detail. Fortunately, a number of teams that participated in the LBC have published their designs and results [5]-[12].

This paper summarizes and compares the final LBC designs for the following teams: National Taiwan University of Science and Technology (Taiwan Tech), Texas A&M University (Texas A&M), ETH Zürich !verter (ETH !verter), University of Illinois Urbana-Champaign UIUC Pilawa Group (UIUC), Virginia Tech Future Energy Electronics Center (VT FEEC), Red Electrical Devils, Schneider Electric, and the University of Tennessee (Univ. Tennessee). In Section II, general challenges for high power density inverter designs are discussed. Comparisons of the dc-ac inverter stage, power decoupling design, and thermal management design are given in Section III. A general discussion of the overall approach is provided in Section IV, followed by concluding remarks in Section V.

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TABLE I
PARTICIPANTS IN THE LITTLE BOX CHALLENGE

Academic Grant Awardees	Finalist Teams	Country
University of Colorado Boulder	-	USA
National Taiwan Univerity of Science and Technology	-	Taiwan
Universidad Politécnica de Madrid	-	Spain
Texas A&M University	-	USA
ETH Zürich	!verter	Switzerland & Germany
University of Bristol	-	UK
Case Western Reserve University	-	USA
University of Illinois Urbana-Champaign	UIUC Pilawa Group	USA
University of Stuttgart	-	Germany
Queensland University of Technology	-	Australia
-	Adiabatic Logic*	UK
-	AHED	Germany
-	AMR	Argentina
-	Cambridge Active Magnetics	UK
-	Energylayer	Ukraine
-	Fraunhofer IISB	Germany
-	Future Energy Electronics Center (3rd)	USA
-	Helios*	USA
-	LBC1*	Slovakia
-	OKE-Services	Netherlands
-	Red Electrical Devils (1st)	Belgium
-	Rompower	USA & Romania
-	Schneider Electric Team (2nd)	France
-	The University of Tennessee	USA
-	Tommasi-Bailly	France
-	Venderbosch	Netherlands

*Team dropped out of the competition before final testing.

II. CHALLENGES FOR HIGH POWER DENSITY INVERTERS

A. Magnetics Size Reduction

One major challenge in achieving high power density for any power converters are the size of the magnetics. Magnetic components in power converters are used for basic power conversion, filtering, and galvanic isolation. While these components are difficult to design out of power converters, their physical size is often reduced by increasing operating frequencies [13]. Recently, wide-bandgap (WBG) semiconductor switches have come to market, which have significantly higher switching speeds than traditional Si switches. These WBG switches have allowed for much higher switching frequencies in power converters, which allows the size of the magnetics to be reduced.

B. Thermal Management

Another general challenge in designing high power density converters is thermal management. As the converter size is reduced, losses are dissipated over a smaller volume, which can result in very high temperatures. If the heat is not properly, managed, higher temperatures can reduce component performance or, in extreme conditions, damage components. Thus, thermal management is important at all levels of the design, from the PCB layout to the case enclosure. Fortunately, using WBG switches reduces switching losses compared to Si switches. For this reason, WBG switches are crucial for high power density converters and were heavily utilized in the LBC prototypes.

C. Single-Phase Inverter Power Ripple

While three-phase inverters have steady output power attributed to the power balance between the phases, single-phase inverters have a substantial power ripple at twice the line frequency [14]. Generally, large electrolytic capacitors can be used to store bulk energy to reduce the voltage ripple, but these bulky capacitors limit the power density and reliability of the converter [15]. To address the power ripple problem, a number of passive and active techniques were utilized in the LBC prototypes. This topic attracted a significant amount of research attention that will be further discussed in Section III. B.

III. LBC INVERTER DESIGNS

This paper focuses on three major aspects of single-phase inverters: dc-ac inverter, power decoupling, and thermal management. The different approaches for various LBC teams are outlined and compared in the following sections. Table II summarizes the design aspects for each team.

A. Inverter Power Stage

For the dc-ac inverter power stage, the topology, type of switches, and operating frequencies are examined. For the inverter topology, the standard topology is to use a full-bridge inverter. Most teams used the full-bridge inverter approach with some modifications in the control or how the decoupling circuit interacts with the inverter.

1) Taiwan Tech

The Taiwan Tech team used the standard full-bridge topology, as shown in Fig. 1. However, an asymmetric control scheme was implemented, where the first leg switches at higher frequencies and the second leg switches at a low frequency, carrying out the unfolding operation. The high-frequency leg switched at a range of 25 to 800 kHz and the low-frequency leg switched at 120 Hz, twice the line frequency. The switch used in the inverter stage was the GaN Systems GS66516T,

TABLE II
INVERTER DESIGN ASPECTS

Team	Topology	Switches	Switching Frequency	Power Decoupling	Thermal Management
Taiwan Tech	Full-bridge, asymmetric control	GaN Systems, GS66516T, 650 V, 60 A	DC-AC: 25-800 kHz DC-DC: 200-680 kHz	Active, synchronous buck to buffer capacitor	Six fans, heat sink connected to aluminum case
Texas A&M	Full-bridge, 3rd leg decoupling circuit	GaN Systems, GS66508P, 650 V, 30 A	100 kHz	Active, decoupling circuit similar to inverter 3rd phase, as in [5]	Unspecified cooling system with heat sink
ETH !verter	Full-bridge, interleaved paralleled legs	Infineon, CoolGaN, 600 V	200 kHz-1 MHz	Active, synchronous buck to buffer capacitor	forced air cooling by utilizing high fin-number heat sinks and six ultra-flat blowers
UIUC	Multilevel, 7-level flying capacitor inverter	EPC, GaN EPC2003, 150 V, 48 A	Switch: 120 kHz Effective: 720 kHz	Active, series-stacked buffer architecture	Copper enclosure, 2 mm tall heat sink fins, 6 radial fans
VT FEEC	HERIC	DC-DC: Transphorm TPH3002LD, GaN, 600 V, 9 A DC-AC: GaN Systems, GS66516T, 650 V, 60 A	DC-AC: 60 kHz DC-DC: 400 kHz	Active, interleaved buck as first power stage	Copper enclosure, 10 micro-fans on side wall
Red Electrical Devils	Full-bridge, paralleled legs	GaN Transistors	35-240 kHz	Active, synchronous buck to buffer capacitor	Copper enclosure, with gap-pad
Schneider Electric	Full-bridge	SiC MOSFETs, TO247 package	45 kHz	Active, ripple filter full-bridge to buffer capacitor	Heat sink over power switches with small fan, two air inlets on case
Univ. Tennessee	Full-bridge	GaN Systems, GS66508T, 650 V, 30 A	100 kHz	Passive, notch filter	Heat sink over power switches, two small fans, air inlets on top and side

rated at 650 V and 60 A. The main choice for employing an asymmetric control strategy is to reduce the total switching losses compared to standard PWM control, which both increases efficiency and reduces heat generation.

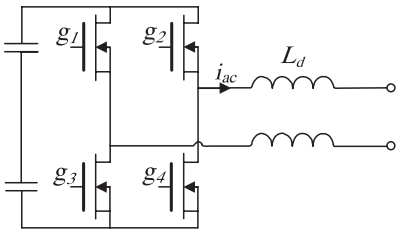
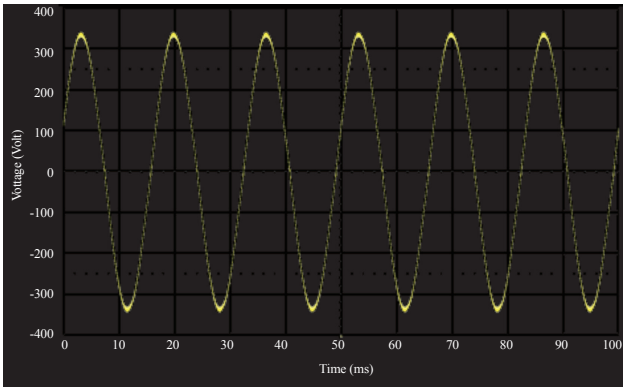


Fig. 1. Basic full-bridge inverter topology.

As an example of the inverter output performance achieved with this topology, Fig. 2 shows the experimental waveforms at the full 2 kW power rating. Fig. 2(a) shows the ac output voltage at 231.7 V rms with 1.29% THD, and Fig. 2(b) shows the ac output current at 8.6 A rms with 1.30% THD. The output shows very little distortion and meets the LBC requirements.

2) Texas A&M

The Texas A&M Team also uses a full-bridge topology for the inverter stage. The decoupling circuit is connected in parallel to the inverter input, such that it looks similar to a 3rd leg of the inverter, but the decoupling circuit will be discussed in the following power decoupling section. After a number of different wide bandgap switches were compared in [5], the GaN Systems GS66508P, rated at 650 V and 30 A, was selected for the inverter design. The switches operate at a switching frequency of 100 kHz [5].



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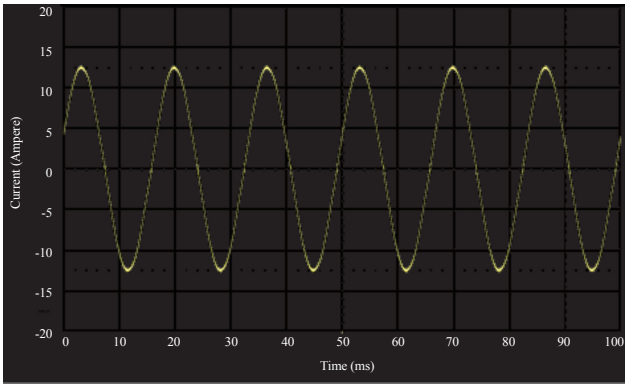


(b)

Fig. 2. Ac output voltage (a) and current (b) for the Taiwan Tech team's full-bridge inverter at full power.

3) ETH !verter

The ETH !verter team used an interleaved full-bridge inverter with four inverter legs, as shown in Fig. 3, where the power for each phase is split over two legs. The inverter is controlled in triangular current mode (TCM), such that soft switching is achieved to reduce switching losses. The switches used are Infineon CoolGaN^{TM} transistors, rated at 600 V, switching at a frequency range of 200 kHz to 1 MHz, depending on the output voltage [6], [7].

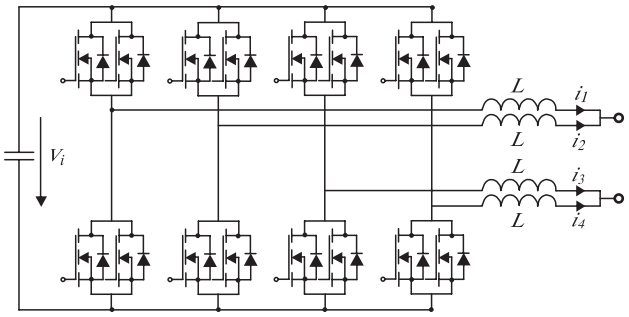


Fig. 3. Parallel full-bridge inverter topology.

4) UIUC

Different from other teams, the UIUC team chose a multi-level topology rather than the standard full-bridge topology. The main motivation for using a multilevel inverter is its lower inherent THD, which means that the EMI filter size can be reduced, leading to higher overall power density. The design used for the LBC was a 7-level flying capacitor topology, which consists of 5 flying capacitors, an inductor, an output capacitor and four switches, is shown in Fig. 4. The switches used were the EPC EPC2003, rated at 150 V and 48 A. Compared to the full-bridge topology, this approach has significantly more switches, which requires more complex control. The transistors switch at 120 kHz, but the effective frequency of the multilevel converter is 720 kHz [8].

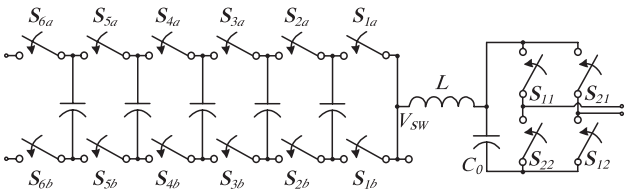


Fig. 4. 7-level flying capacitor inverter topology.

5) VT FEEC

The VT FEEC team used an inverter topology with the trade name HERIC, which stands for highly efficient and reliable inverter concept. The inverter topology is shown in Fig. 5 and utilizes two series-connected switches across the inverter output. For switches, the team used the GaN Systems GS66516T, rated at 650 V and 60 A. The switching frequency for the inverter was 60 kHz [9].

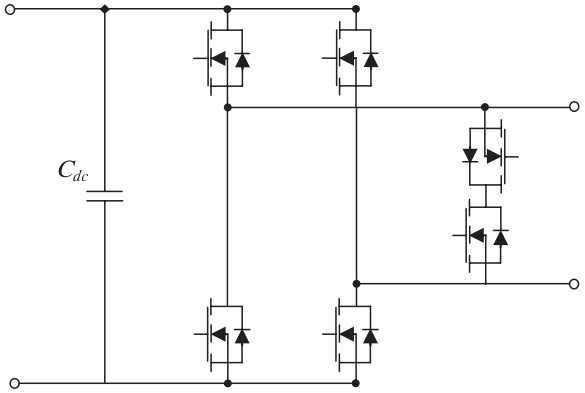


Fig. 5. HERIC inverter topology.

6) Red Electrical Devils

The Red Electrical Devils team used the a full-bridge inverter, with four inverter legs (two legs for each side of the output. The technical document [10] states a five-legs topology, but this is simply four legs for the parallel full bridge and one leg for decoupling. The approach is essentially the same as the ETH !verter team, shown in Fig. 3. Although GaN transistors were used for all bridge legs, neither the part number nor the manufacturer were stated [10]. The switching frequency ranged between 35 and 240 kHz to achieve soft switching, which helped in reducing losses.

7) Schneider Electric

The Schneider Electric team used a full-bridge inverter operating in PWM mode, but details about the control strategy are not given in their technical approach document [11]. For the four switches in the inverter, SiC MOSFETs in a TO247 package were used (exact part number is not given in [11]) and the switching frequency was 45 kHz. This is one of the few teams that used SiC switches rather than GaN switches.

8) Univ. Tennessee

The Univ. Tennessee team used the standard full-bridge inverter where the switches are hard-switched rather than soft-switched. The switches used were the GaN Systems GS66508T, rated at 650 V and 30 A. The switching frequency was 100 kHz and the inverter operation is controlled using unipolar continuous sinusoidal pulse-width modulation [12].

B. Power Decoupling Designs

The approaches for power decoupling in the single-phase inverter varied greatly among the teams and was an area of innovation for many teams. While the traditional approach is to use passive, bulky components, almost all teams took active decoupling approaches in order to reduce the volume. The decoupling circuits are overviewed for each team.

1) Taiwan Tech

The Taiwan Tech team utilized a synchronous buck converter that transfers power to and from a buffer capacitor to decouple the power, as shown in Fig. 6. This allows power to

vary at double-line frequency without causing voltage swings in the inverter input voltage. The switches used in the decoupling buck converter are also GaN Systems GS66516T. The switching frequencies varies from 200 to 680 kHz according to the current level. The buck converter operates in this way to achieve ZVS mode to reduce losses and heat generation.

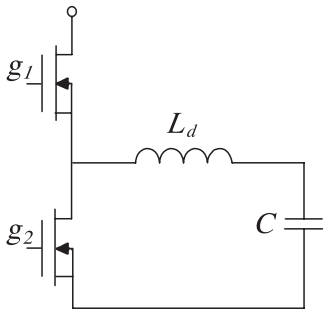
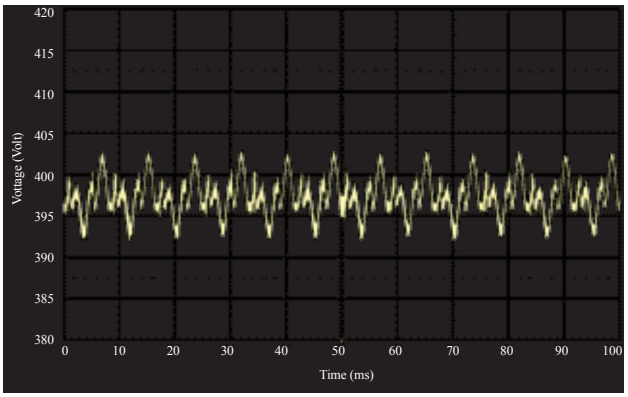


Fig. 6. Synchronous buck power decoupling topology.

The effectiveness of the synchronous buck power decoupling circuit to reduce the ripple at the dc input for the Taiwan Tech team is shown in Fig. 7. Experimental results were taken at full power. Fig. 7(a) shows the voltage ripple of the dc input and Fig. 7(b) shows the current ripple of the dc input. As shown, the voltage ripple is 10.8 V peak-to-peak and the current ripple is 0.86 A peak-to-peak, which shows good performance of the synchronous buck power decoupling circuit.



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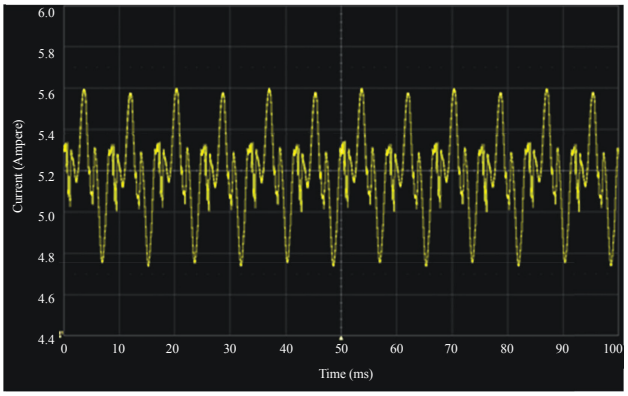


(b)

Fig. 7. Input voltage (a) and current (b) for dc input to the inverter for the Taiwan Tech team's design at full power.

2) Texas A&M

The Texas A&M team focused mainly on the power decoupling circuit and proposed a circuit that connects from the dc input to one line of the ac output. The proposed decoupling circuit, shown in Fig. 8, is a kind of half-bridge power decoupling topology that is fully detailed in [5]. The advantages of this topology are that the decoupling capacitor carries the ac voltage such the capacitor is fully utilized and its size is minimized. Further, compared to a full-bridge inverter decoupling circuit, which uses four switches, this solution uses only two switches. The decoupling circuit can also be thought of as a third leg of the inverter, such that it helps to balance out the power, which also distributes power dissipation in the inductors [5]. This decoupling approach was developed specifically for the LBC, and was a unique approach.

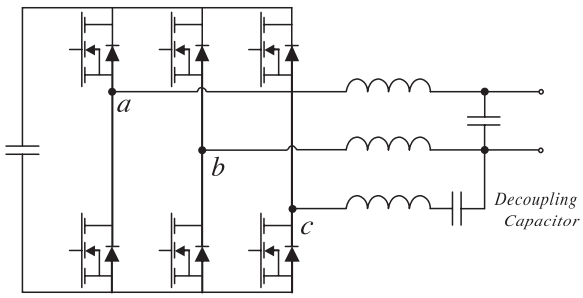


Fig. 8. Half-bridge power decoupling topology, as in [5].

3) ETH !verter

For power decoupling the ETH !verter team also used a synchronous buck converter to buffer power to and from a capacitor, as shown in Fig. 6. Although his method does not fully utilize the capacitor's capacity, the team employs high energy-density ceramic capacitor to reduce overall size [6], [7].

4) UIUC

The UIUC team utilized a unique active power decoupling

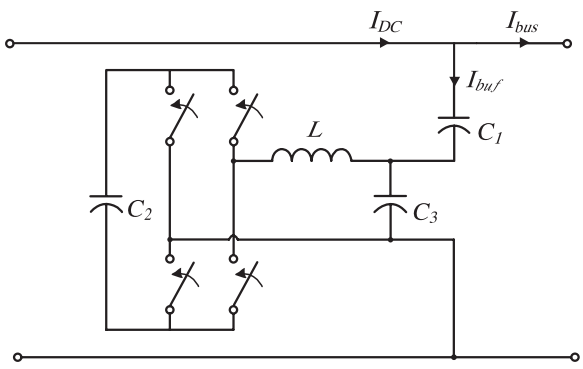


Fig. 9. Series-stacked power decoupling circuit topology.

technique that utilizes a series-stacked type of differential power processing architecture, as shown in Fig. 9. The advantage of this topology is that the energy storage capacitor's capacity is fully utilized such that the capacitor's size can be minimized and power losses can be minimized by reducing the amount of power processed in transferring power to and from the storage capacitor. One tradeoff is that there are four switches rather than two used in many of the other power decoupling circuits [8]. However, the UIUC team's overall design did not shy away from complex switching circuits, which resulted in a small overall converter volume.

5) VT FEEC

The VT FEEC team utilized a 2-phase interleaved buck converter as a first dc-dc stage before the dc-ac stage. The switch for the buck converter was Transform TPH3002LD, a GaN switch rated at 600 V and 9 A, and the diode was a SiC diode, Cree C3D1P7060Q. The converter switched at 400 kHz, which helps reduce the inductor size [9].

6) Red Electrical Devils

Similar to other teams, the Red Electrical Devils used a synchronous buck converter for power decoupling, as shown in Fig. 6. Ceramic capacitors were used as the buffer capacitor to maintain a small size. Although not clearly specified in the [10], the same GaN switches and switching frequency range as the inverter stage was likely utilized for the buck converter as well.

7) Schneider Electric

The Schneider Electric team used a low-voltage full-bridge inverter in series with the inverter input voltage, which they called an active ripple filter. This circuit requires four switches, rather than two, as shown in Fig. 10. Silicon MOSFETS were used rather than wide-bandgap switches [11].

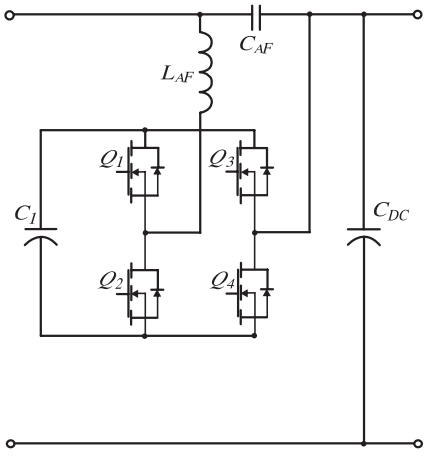


Fig. 10. Active ripple filter in series with the inverter input capacitor.

8) Univ. Tennessee

Different that the other teams, the Univ. Tennessee team was the only team to choose a passive power decoupling method, rather than an active method. A resonant notch filter tuned to 120 Hz was used. This filter allowed for high attenuation at the target frequency but can be implemented with a relatively small capacitor size [12].

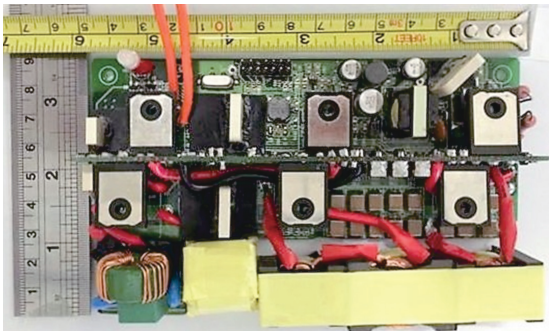
C. Thermal Management

Most teams assumed that their inverter operated at an efficiency of around 97%, such that at least 60 W of heat would need to be dissipated. In general, all teams concluded that forced air flow, using fans, was necessary and conducted detailed thermal modeling for their LBC designs.

1) Taiwan Tech

For heat dissipation, Taiwan Tech used multiple fans at the air inlet and outlet of the enclosure. A fan was also used near the GaN switches to ensure sufficient airflow around them. In total six fans were utilized. A heat sink was also utilized near the switches, which was thermally linked to the aluminum case to further improve heat dissipation.

The prototype of the LBC inverter prototype for the Taiwan Tech team is shown in Fig. 11. The circuit board is shown in Fig. 11(a), along with the top-view of the prototype in Fig. 11(b), and the side-view in Fig. 11(c). As shown, the dimensions of the enclosure are 5.985 in by 3.685 in x 1.000 in, which is a volume of 22.055 in^3. In experimental testing at full load with an ambient temperature of 29 °C, the maximum enclosure temperature was 57 °C, which is below the 60 °C requirement for the LBC.



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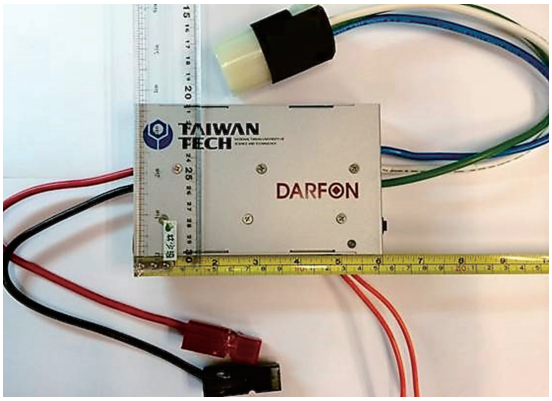

(b)

Fig. 11. The internal circuit board (a), case top-view (b), the Taiwan Tech team's LBC prototype.

(c)

Fig. 11. (*Continued*..) Case side-view (c) the Taiwan Tech team's LBC prototype.

2) Texas A&M

The cooling system for the Texas A&M team is only generally described in [5]. A heat sink of dimensions 60 mm by 25 mm by 24 mm is utilized. The use of fans is not explicitly stated, but are likely incorporated in the cooling system as the cooling system and auxiliary circuits were cited as contributing to the inverter's size.

3) ETH !verter

For thermal management, for the ETH !verter team also utilizes forced air cooling by utilizing high fin-number heat sinks and six ultra-flat blowers. The relatively flat cooling system in placed on the top of the enclosure to facilitate the natural convection flow [6], [7].

4) UIUC

The cooling system for the UIUC team incorporates an enclosure that is milled out of copper with heat-sink fins on the exterior. Six small blower fans are also integrated on the outside of the enclosure. Testing results in [8] state a maximum case temperature of 57 °C.

5) VT FEEC

The VT FEEC team managed the heat by using forced-air cooling and the case as a heat sink. The case was made out of copper to act as a heat sink and ten 0.1 W micro-fans forced air across fins mounted on one side wall of the case. Testing results in [9] shows the maximum case temperature as 53.6 °C.

6) Red Electrical Devils

The Red Electrical Devils team put a significant amount of attention into the thermal management design. Heat sinks were custom made by electrical discharge machining and were connected to an 0.012-in-thickness PCB using micro-spring contacts. Silicone foam was used to spread the GaN contact pressure evenly over the heatsink. The heat sink was made of copper in a honeycomb pattern that is layered between other component layers. The team also employed a gap-pad between the external copper enclosure and the internal copper shielding. The purpose is to extract heat from the hottest components without creating local hot spots in the external enclosure. An axial fan was placed in the middle of the front plate to facilitate forced air flow through the various converter layers [10].

7) Schneider Electric

The Schneider Electric team used heat sink mounted on the power switches with a small fan directly above the heat sink [11]. Two outlets on opposite faces of the enclosure to allow airflow.

8) Univ. Tennessee

For thermal management, the Univ. Tennessee team utilized a heat sink above the GaN switches with thermal interface materials between the switches and heat sink. There are two main fans above the heat sinks with air inlets on the top and side of the enclosure. Results in [12] show that the maximum case temperature is just below the 60 °C requirement for the LBC.

IV. Discussion

Performance of the various designs is summarized in Table III for the efficiency, dimensions, volume, and power density. Note that because the performance of all the final prototypes tested for the LBC were not all made public, the values are based on either technical documents or papers published about the inverter.

From the inverter designs outlined in Table II, most teams utilized a full-bridge topology, with some variations, like the HERIC or using parallel legs. Only the UIUC team utilized a multi-level converter, which had the most number of switches by far. WBG semiconductor switches were a fundamental part of all designs due to achieve high density. All but one team used GaN switches and only the Schneider Electric team used SiC switches. The switching frequencies for fixed-frequency approaches ranged from 45 to 120 kHz while the variable frequency strategies ranged from 25 kHz up to 1 MHz. The ranges are relatively reasonable and did not push the present-day limits for switching, mainly to reduce heat generation from switching loss. Further, many teams employed soft switching methods to further reduce switching losses.

The power decoupling methods showed a wider variety and a number of innovative solutions. Only the Univ. Tennessee team used a passive solution and the rest utilized active circuits to reduce the size of the passives and magnetics. The synchronous buck converter connected to a buffer capacitor was the most common active power decoupling solution, but the half-bridge power decoupling topology used by the Texas A&M team, the series-stacked power decoupling circuit used by the UIUC team, and active ripple buffer used by the Schneider Electric team were unique approaches that fully utilized the buffer capacitor. These approaches are worth further analysis and investigation for future high power density designs.

For the surveyed designs, the thermal management normally involved detailed modeling, analysis, and a customized cooling system. Based on the expected power losses, forced-air cooling using fan and heat sinks was the standard approach. Three of the teams used copper enclosures, utilizing the case itself as a heat sink. For the fans, many of the teams used multiple small fans that directed airflow evenly across the enclosed converter.

TABLE III
INVERTER PERFORMANCE

Team	Efficiency	Inverter Dimensions (in)	Volume (in^3)	Power Density (W/in^3)	Source
Taiwan Tech	96.5% (CEC)	6.00 x 3.69 x 1.00	22.06	90.68	reported here
Texas A&M	98% (conditions unspecified)	5.3 x 5.2 x 1.3	35.8	55.8	[5]
ETH !verter	95.07% (CEC)	-	14.8	134	[6], [7]
UIUC	97.0 %(CEC)	4.02 x 2.42 x 0.95	9.24	216	[8]
VT FEEC	98.59% (peak)	-	29.1	68.7	[9], [3]
Red Electrical Devils	not provided	2.5 x 1.615 x 3.41	13.77	145.2	[10], [3]
Schneider Electric	not provided	-	20.8	96.2	[11]
Univ. Tennessee	96.9% (CEC)	4.38 x 3.47 x1.29	19.6	102	[12]

Although the first, second, and third winners of the LBC were the Red Electrical Devils, Schneider Electric, and VT FEEC teams, respectively, a number of other teams showed power densities higher than the winners. Because the prototype testing for the LBC was not public, it is not clear which specifications the teams that claimed higher power density failed to meet. Based on this survey, the winning teams all seemed to use straight-forward inverter topologies and had robust thermal designs with extra margin from the 60 °C case limit, which may have been an advantage during on-site testing in a new environment.

Based on the power densities in Table III, the highest power density was the UIUC team, which used the 7-level flying capacitor inverter and series-stacked power decoupling circuit. That design made a clear trade-off of using more switches in order to reduce magnetics, even if it meant more complicated control. Based on the results of the LBC and the survey provided here, the first step towards higher power density inverter seems to be through the standard full-bridge topology and more well-established power decoupling techniques, but the future steps may move towards multi-level inverters and newer power decoupling topologies to reach the next level of high power density inverters.

V. CONCLUSION

This paper surveyed the designs for eight teams that participated in the LBC including: Taiwan Tech, Texas A&M, ETH !verter, UIUC, VT FEEC, Red Electrical Devils, Schneider Electric and University of Tennessee. The information surveyed here was based on the technical approach documents from the LBC and from papers published by participating teams. WBG switches, especially GaN, were widely used in both the inverter and power decoupling stages. Soft-switching approaches were also heavily utilized to reduce switching losses and associated heat generation. Various active power decoupling topologies, including a number of newly proposed circuits, were used to decrease the size of passive components used in traditional single-phase inverters. Thermal management was a crucial challenge for high power density and teams utilized custom heat sink solutions with forced cooling using small fans. Although the LBC officially had only one official winner, the contribution of the competition was not just the design of the winning team, but the various approaches and design from the many teams that participated in the LBC.

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