Master's Thesis

CAN-FD Transceiver Design & Implementation with Improved Matching on Switching Behavior

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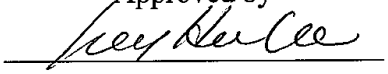

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6. 14. 2017

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ABSTRACT

In the automotive industry, the automotive Integrated Chips (ICs) require a high level of Electromagnetic Immunity (EMI) and low Electromagnetic Emission (EME). EME is more important to the Controller Area Network with Flexible Data-rate (CAN-FD) because the CAN bus acts as an antenna, disturbing the other automotive ICs. In this thesis, a new architecture of CAN-FD transmitter with improved matching of the CAN bus on switching behavior is proposed resulting in reducing EME.

The proposed transceiver presents the new architecture of the transmitter for driving the CAN bus using 30 step cascading current sources and a Cross-control Method which can increase matching of the CAN bus on switching behavior. The circuit implementation of the proposed transceiver was fabricated using a 0.18μm automotive BCDMOS process. The measurement results show that the result is better at matching of the CAN bus than other CAN-FD transceivers. It also shows good matching at a data-rate of 10Mbps.

KEYWORD: Automotive IC, Controller Area Network with Flexible Data-rate, Transceiver, CAN bus Matching.

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GLOSSARY

BCDMOS	Bipolar, CMOS and LDMOS
BGR	Band-gap Reference
CAN	Controller Area Network
CAN-FD	CAN with Flexible Data-rate
CM	Common-mode
DPI	Direct Power Injection
ECU	Electronic Control Unit
EFT	Electrical Fast Transient
EM	Electromagnetic
EME	Electromagnetic Emission
EMI	Electromagnetic Immunity
ESI	Error Status Information
IC	Integrated Chip
IVN	In-vehicle Network
ISO	International Organization for Standardization
LDO	Low Dropout
LDMOS	Lateral Diffused MOS
RF	Radio Frequency
RX	Receiver
RXD	Receive Data
SOA	Safe Operating Area
TRX	Transceiver
TSD	Thermal Shutdown
TX	Transmitter
TXD	Transmit Data

1. Introduction

The use of Electronic Control Units (ECUs) in a vehicle has increased to support new applications which need more complex and intelligent functions for passenger conveniences. The number of ECUs exceed over 100 units in some automotive vehicles [1]. As the increase of the number of ECUs, the Electromagnetic Emissions (EMEs) of the automotive Integrated Chips (ICs) have also drastically increased. In this noisy electromagnetic environment, it is the challenge for the automotive ICs to work without functional failures.

In this section, the background of classical Controller Area Network (CAN) and CAN with Flexible Data-rate (CAN-FD) is described. After that, this section focuses on the Electromagnetic Compatibility (EMC) issues which are the objective of the research.

1.1 Classical CAN and CAN-FD

Classical CAN is one of the automotive In-vehicle Networks (IVNs). It is internationally standardized by the International Organization for Standardization (ISO) [2]. Using a differential signaling method, the CAN network can achieve robust operation supporting a maximum data-rate of 1Mbps. Fig. 1.1 shows the waveforms of CANH and CANL of a CAN bus. Recently, CAN-FD has been introduced which has also been standardized by ISO. It supports higher data-rate, up to 5Mbit/s in ISO documents, and is able to send a longer message than classical CAN. Some changes exist in CAN-FD frame formats. CAN-FD allows bit times for certain fields that are shorter than the classical CAN bit time [4]. By reducing the bit time, the number of data bytes of the data field increases to 64 bytes compared to 8 bytes in the classical CAN. Fig. 1.2 shows the difference of the frame format between CAN and CAN-FD.

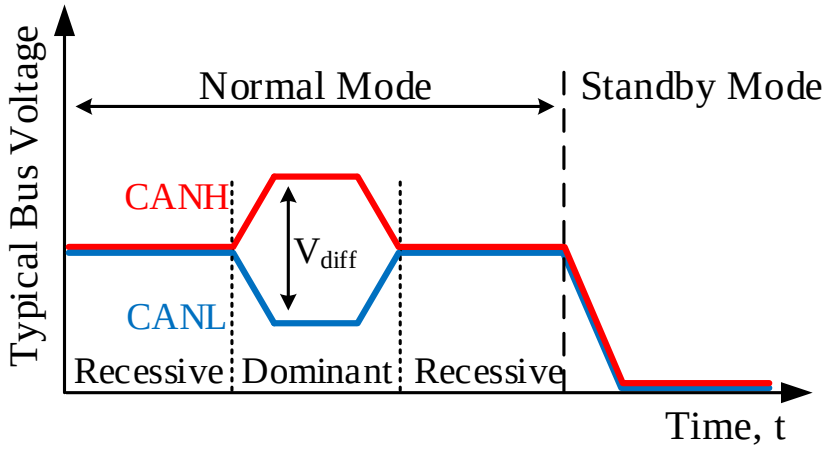


Fig. 1.1 A signal definition of the CAN protocol at CAN bus [3].

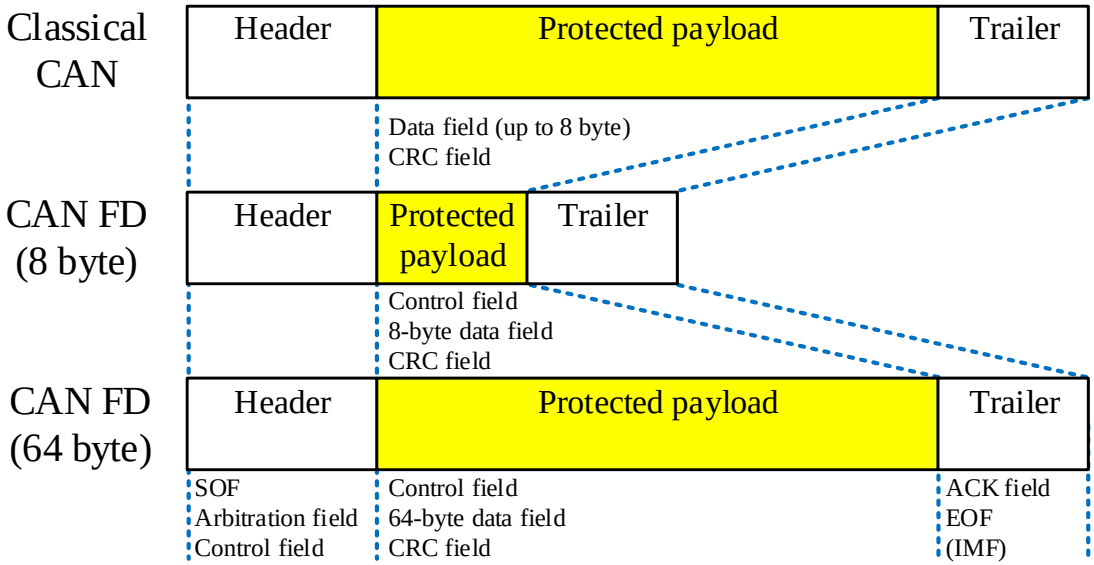


Fig. 1.2 Data frames compared with classical CAN and CAN-FD [6].

1.2 EMC Issues of the Automotive ICs

EMC issues have been one of the main reasons for redesigning automotive ICs [8] [9]. The automotive industry requires a high level of EMC [10] [11] [12]. Achieving robustness against EMI and low EME is one of the most major challenges in designing a CAN-FD transceiver. The automotive communication networks such as classical CAN, CAN-FD and Local Interconnected Network (LIN) function as antennas which can emit and receive Radio Frequency (RF) disturbances [9]. Using CAN-FD with a high data-rate, the fast transitions of the CAN bus signals generate high-frequency RF disturbances affecting other automotive ICs sensitive to EMI. The RF disturbances on the bus can also cause corrupting duty-cycle and change the logical state on the bus signals [9] [11] [13]. These issues result in functional failures which are the most critical problem in the communication network. Designing a low EME CAN-FD transceiver, matching the CAN bus on switching behavior is the key factor in reducing EME and the cost of RF filters [14] [15].

To overcome these problems, this thesis shows the new implemented CAN-FD transceiver with matching the CAN bus on switching behavior, using Cross-control Method. The design considerations for a proposed CAN-FD transceiver are presented in Section 2. Using the Cross-control Method, a principle of the proposed CAN-FD transceiver which improves matching the CAN bus on switching behavior is presented in Section 3. The experimental setup and measurement results are shown in Section 4. Section 5 discusses future works. Finally, the conclusions are presented in Section 6.

2. Design Considerations for CAN-FD Transceiver

2.1 Design Considerations for Automotive Environment

When designing the CAN-FD transceiver, the automotive environment should be considered. The automotive environment is a very harsh environment compared to the normal environment. It includes a wide range of temperatures and a variation in supply voltage, Electrical Fast Transient (EFT), mechanical and unwanted exposures. Also, the automotive transients must be considered according to ISO 7637 standard [16]. For example, Load Dump, which causes transitions up to 40V, is an important consideration. Table 2.1 shows the hazards in the automotive environment [17]. Some of these hazards, which include Temperature, voltages and electromagnetic impulses, are concerns when designing the automotive ICs. Fig. 2.1 shows the specification of an automotive battery [17].

Table 2.1 The hazards in the automotive environment [17].

Temperature	Driver interior	-40℃ to +85℃
	Underhood	-40℃ to +125℃
	On-engine	-40℃ to +150℃
	In the exhaust and combustion areas	-40℃ to +200-600℃
Mechanical Shock	During assembly (drop test)	3000g
	On the vehicle	50-500g
Mechanical Vibration		15g, 100Hz to 2kHz
Electromagnetic Impulses		100 to 200V/m
Exposure to	Common	Humidity, salt spray
	In some application	Fuel, oil, brake fluid, transmission fluid, ethylene glycol, exhaust gases

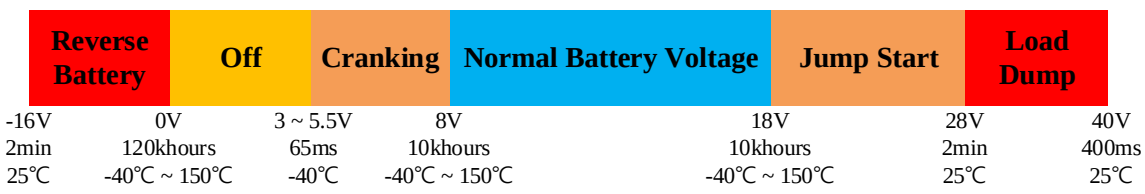


Fig. 2.1 Specification of automotive battery [18].

2.2 Specific Requirements for Classical CAN

Classical CAN has been introduced and widely used to communicate between microprocessors in an automotive system [1] [19] [20]. In ISO 11898, there are specifications for the CAN physical layer which refer to the CAN transceiver. Table 2.2 shows the maximum rating of ports from ISO11898-5 which are one of the specifications for the CAN physical layer [2]. The voltage ranges from -27V to 40V should be guaranteed at the CAN bus pins. This is because the CAN bus can be short-circuited to the supply lines even in the double battery and inverted double battery condition.

Table 2.2 Maximum ratings of CANH, CANL, and VSPLIT [2].

Nominal batter voltage (V)	Pin name	Voltage	
		Vmin	Vmax
14	VCAN_H	-27.0	+40.0
	VCAN_L	-27.0	+40.0
	VSplit	-27.0	+40.0

2.3 Specific Requirements for CAN-FD

The ISO standard of CAN-FD requires dynamic properties to cover higher bit-rates than classic CAN. The specific properties should be met when designing a high bit-rate transceiver. The properties are listed below [21]:

- Transceiver loop delay symmetry
- Transceiver transmitter (TX) delay symmetry
- Transceiver receiver (RX) delay symmetry

Table 2.3 shows the relationship between properties and parameters in ISO 11898-2 [2]. Table 2.4 to 2.6 shows the specific requirements of Loop delay symmetry, TX delay symmetry and RX delay symmetry.

Table 2.3 The relationship between properties and parameter in ISO 11898 [21].

Parameters in ISO	Link	Properties in CiA
Received recessive bit width $t_{Bit(RXD)}$	The minimal and maximal values of $t_{Bit(RXD)}$ => Calculate loop delay symmetry.	Loop delay symmetry
Transmitted recessive bit width $t_{Bit(Bus)}$	The minimal and maximal values of $t_{Bit(Bus)}$ => Calculate TX delay symmetry.	TX delay symmetry
Receiver timing symmetry Δt_{Rec}	Δt_{Rec} defines RX delay symmetry.	RX delay symmetry

Table 2.4 Loop delay symmetry characteristics [21].

Bit-rate (data phase)	Recessive $t_{Bit(RXD)}$ (min)	Recessive $t_{Bit(RXD)}$ (max)	t_{Bit} (nominal)	t_{Loop}	Load on the CAN bus	Load at RXD
1 Mbit/s	n.a.	n.a.	1000 ns	≤255 ns	60Ω||100pF	15pF
2 Mbit/s	400 ns	550 ns	500 ns	≤255 ns	60Ω||100pF	15pF
5 Mbit/s	120 ns	220 ns	200 ns	≤255 ns	60Ω||100pF	15pF

Table 2.5 TX delay symmetry characteristics [21].

Bit-rate (data phase)	$t_{Bit(BUS)}$ (min)	$t_{Bit(BUS)}$ (max)	t_{Bit} (nominal)	Load on the CAN bus
1 Mbit/s	n.a.	n.a.	1000 ns	60Ω||100pF
2 Mbit/s	435 ns	530 ns	500 ns	60Ω||100pF
5 Mbit/s	155 ns	210 ns	200 ns	60Ω||100pF

Table 2.6 RX delay symmetry characteristics [21].

Bit-rate (data phase)	Δt_{Rec} (min)	Δt_{Rec} (max)	t_{Bit} (nominal)
1 Mbit/s	n.a.	n.a.	1000 ns
2 Mbit/s	-65 ns	40 ns	500 ns
5 Mbit/s	-45 ns	15 ns	200 ns

2.4 Additional Design Considerations for CAN-FD Transceiver

The CAN-FD transceiver can be divided into two important parts: a transmitter and a receiver. The transmitter sends the signal to the CAN bus, converting a digital signal to an analog signal. The receiver performs the opposite operation, converting a bus differential signal into a digital signal [14]. The additional design considerations of the CAN-FD transceiver are to increase IC's lifetime, reduce the EME, and to increase RF immunity, which can lead to EMI [14] [15] [22].

A. Transmitter

Fig. 2.2 is the most common structure of a transmitter which drives the CAN bus. The power stage consists of two pairs of Lateral Diffused MOS (LDMOS) operating as switches and diodes protecting supply rails from the reverse polarity voltage of bus pins. Two switches in the power stage operate in the triode region and are controlled by each driver block which turns the switches on and off. The switches are modeled on-resistances and the width of MOSFETs should be large. Reducing the on-resistances compared to the load, the CAN bus current is dependent on the load. But this structure has some disadvantages which are critical factors that disturb the normal operation. As a result, there are some additional design considerations.

First, the switching behavior of the power stage potentially has a danger of breakdown. The operating point of two switches can get out of the region of the Safe Operating Area (SOA), as shown in Fig. 2.3. This can reduce component lifetime and cause permanent failure [23] [24]. New implementation of the power stage should be prepared to increase the robustness. Fig. 2.4 shows the circuit implementation of the power stage using current sources [22].

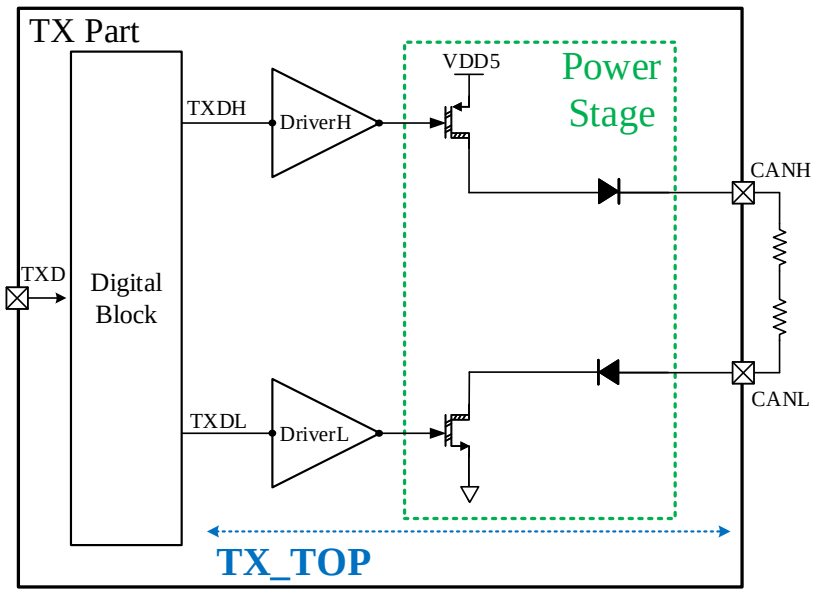


Fig. 2.2 Typical structure of transmitter part.

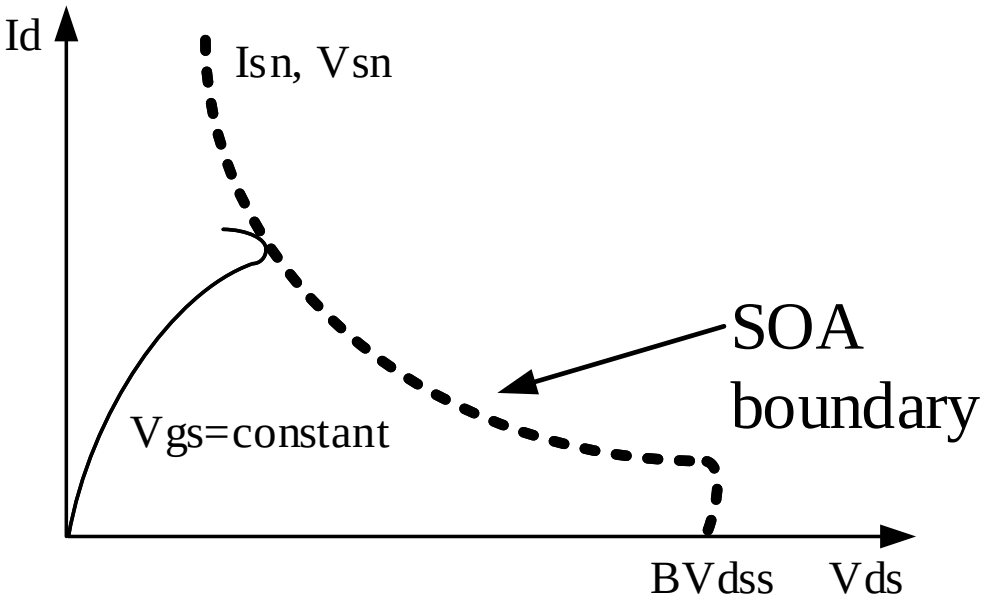


Fig. 2.3 Safety Operating Area (SOA) of LDMOS. The SOA boundary is defined by the onset negative resistance at Isn and Vsn [23].

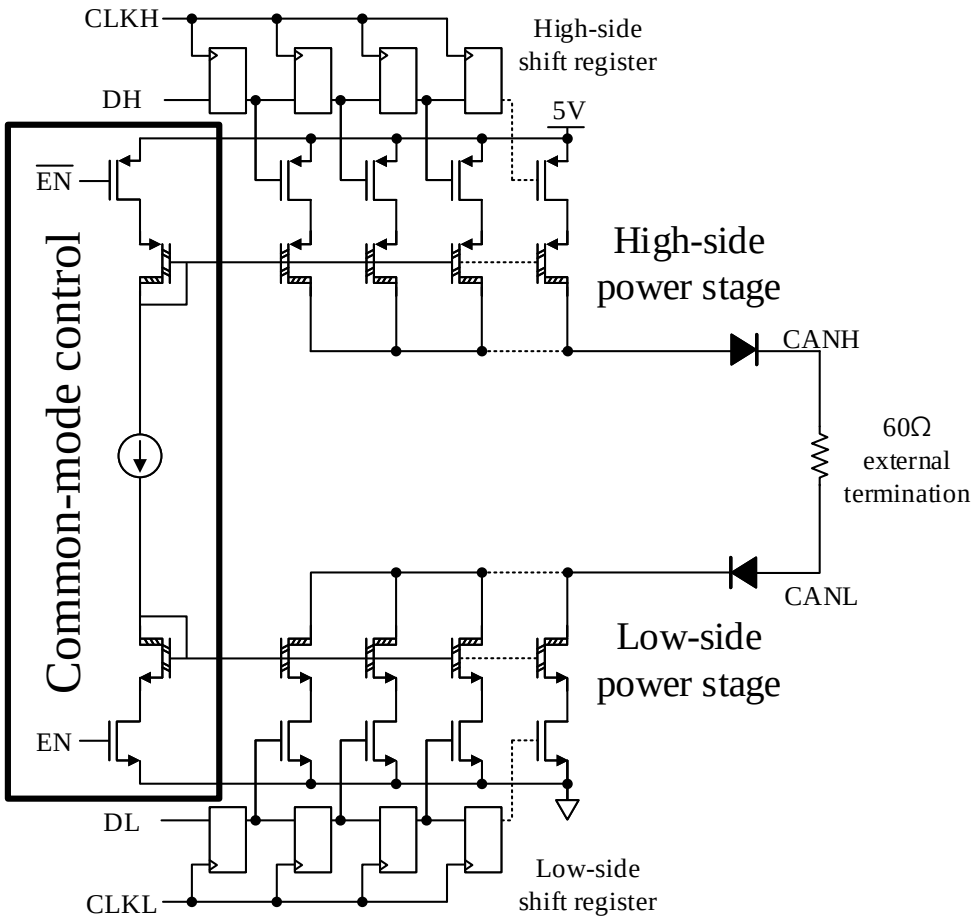


Fig. 2.4 CAN transmitter using current sources at the power stage of transmitter [22].

Second, it is difficult to match symmetries, including matching of the CAN bus and on-resistances of both switches. Defined as VCAN_H+VCAN_L in ISO 11898-5, Driver symmetry is the parameter of matching the CAN bus. Fig. 2.5 shows the example of the mismatch between CANH and CANL [15]. When applying the differential signals to the CAN bus, the transitions and noise in the common-mode signal can occur. This results in increasing EME at the CAN bus [14] [15] [22]. Fig. 2.6 shows the ideal transitions of the CAN bus. It shows that a matched signal and twisted wires help CAN bus to reduce EME, canceling each other's radiated electromagnetic field [15]. Thus, the matching of the CAN bus of the two switches is necessary for canceling the EM fields of each other's bus line.

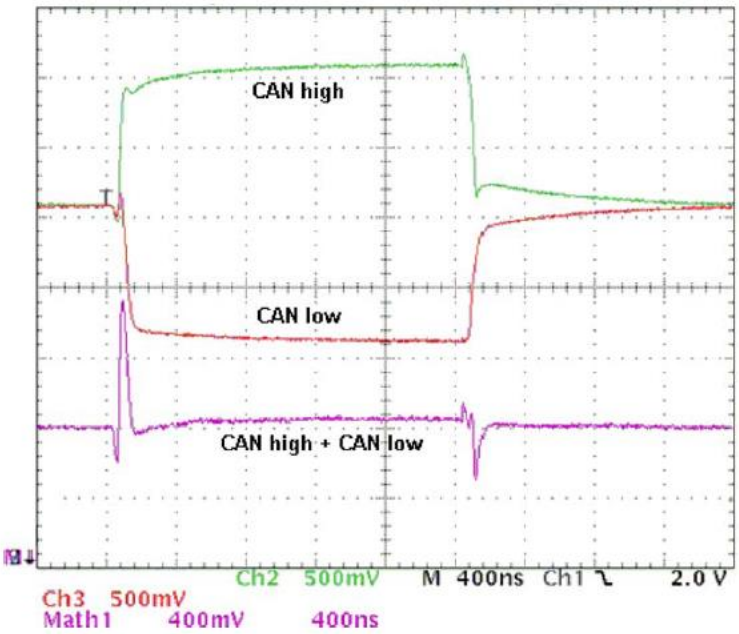


Fig. 2.5 The measurement results of the CAN bus and their addition (VCANH+VCANL) [15].

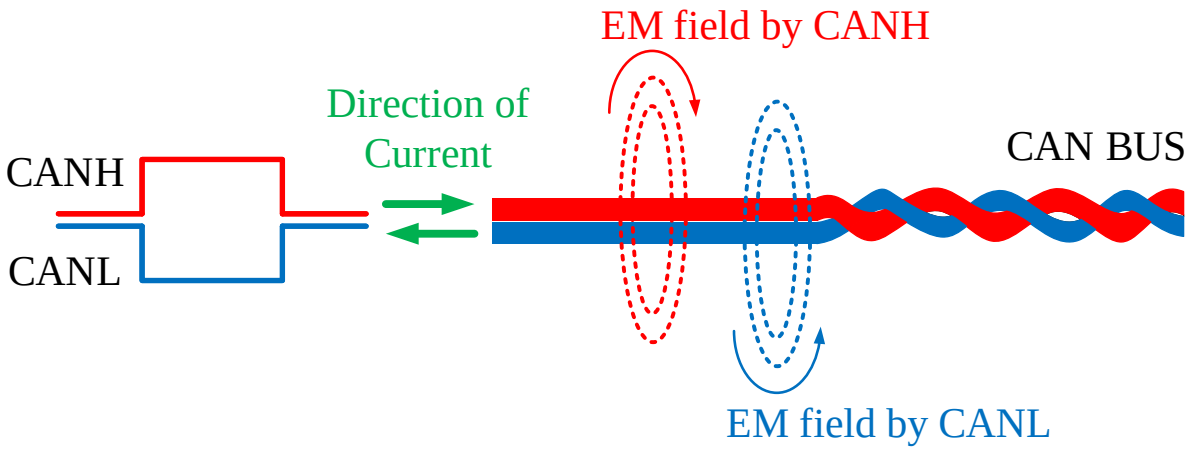


Fig. 2.6 The CAN bus cancels the radiated EM fields which generated by both wires [15].

Fig. 2.7 shows other implementations of CAN transmitter structures which attempted to improve the matching of the CAN bus [14]. Fig. 2.7 (a) shows a trial to match both switches using the same type of MOSFET. However, this approach doesn't operate two switches in the same condition. Also, this needs an additional circuit for operating high side switches such as the charge pump. Fig. 2.7 (b) is the most common structure used in a CAN transceiver. But this structure cannot solve the matching of the CAN bus on switching behavior when the transitions occur on the CAN bus. Fig. 2.7 (c) uses a feedback loop, but this can distort the signal by interference. Also, the stability of the circuit is hard to achieve as the bus topology changes.

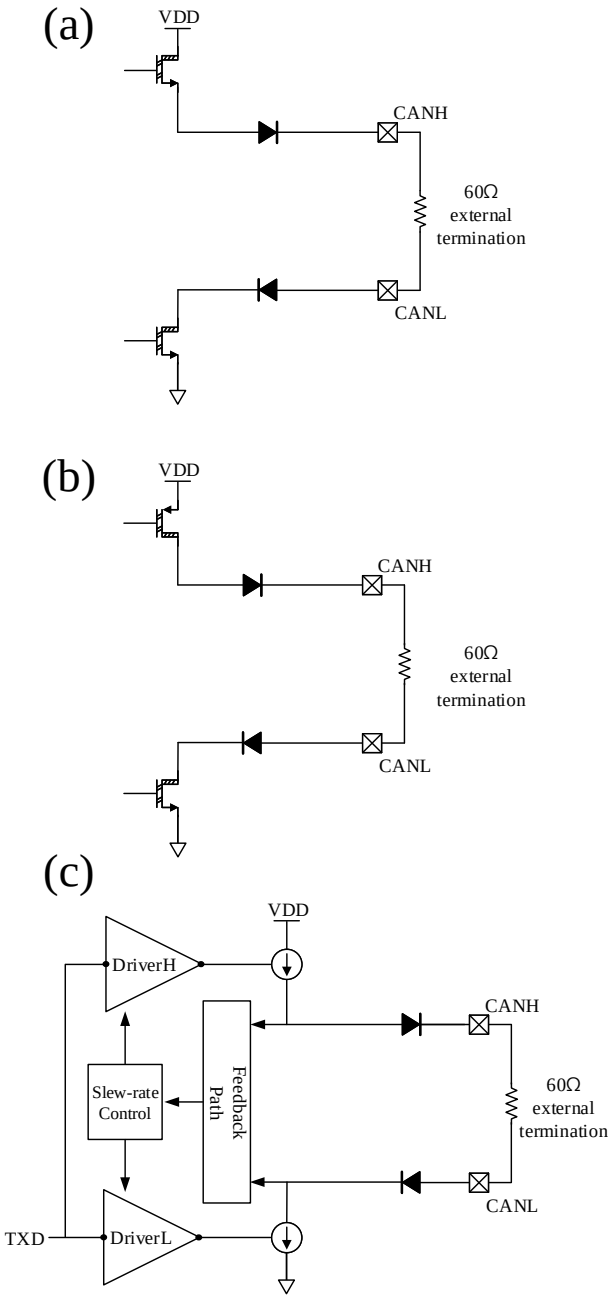


Fig. 2.7 The approaches to improve matching characteristics of the CAN bus [14]. (a) Using same devices, (b) Using different devices, (c) Feedback structure.

Finally, EMI should be considered. Fig. 2.8 (a) shows the typical termination of the CAN bus, where R_L is 120Ω and C_s is 4.7nF. To improve the capability of EMI, in Fig. 2.8 (b), the 4.7nF capacitor can be connected at the middle of resistors, each of 60Ω. Additionally, split termination can be connected with CM voltage generated from the transceiver's CM voltage generator (VSplit). Split termination is in the middle of the termination resistors and capacitor of the CAN bus.

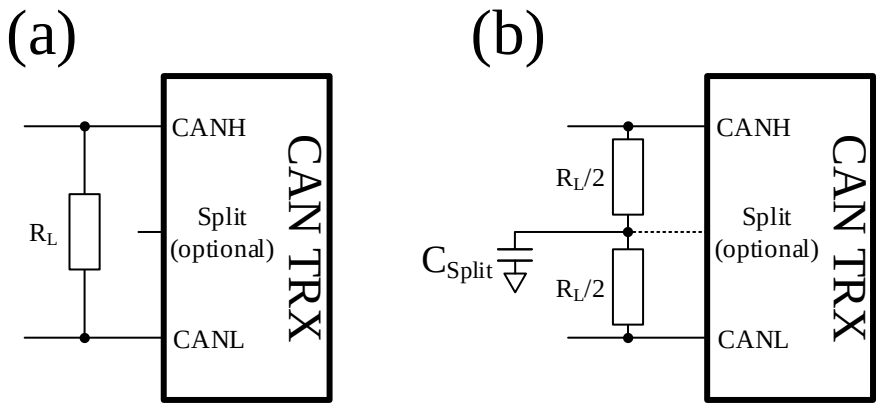


Fig. 2.8 (a) Typical Termination, (b) Split Termination with 4.7nF capacitor [2].

B. Receiver

There are additional design considerations for the receiver. The EMI of the receiver can be considered when designing the receiver [22]. If the receiver can detect a small differential signal in a noisy common-mode signal, high immunity of the CAN-FD transceiver can be achieved [22]. There are some approaches that reduce noise from the bus by adding bypass capacitors at the inputs of the receiver [7] [22]. Fig. 2.9 shows an example of the receiver using a low-pass filter in front of the receiver which consists of three stages [22]. The capacitors in a resistive ladder reduce high-frequency disturbances. At the end of the stages, the hysteresis comparator can be used to generate a signal which is robust to the disturbances from the CAN bus.

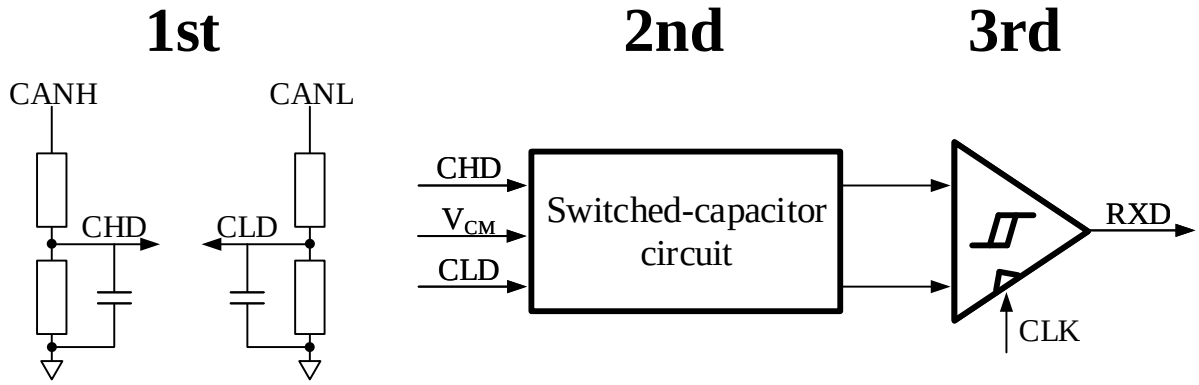


Fig. 2.9 The receiver of classical CAN transceiver with three stages. [22].

3. Principle of Proposed CAN-FD Transceiver

3.1 Features of the Proposed Architecture of CAN-FD Transceiver

To deal with all of these considerations as mentioned before, the new implementation of CAN transceiver with a new architecture is needed. In this section, a new architecture of the transmitter of the CAN-FD transceiver is presented which is different to an ordinary structure. There are key features of the proposed architecture which were considered in the designing process:

- Use current sources at power stage of LDMOS which increase component lifetime.
- Use 30 step cascade stages for driving power stage to design accurate rise time for supporting high data-rate.
- Use Cross-control Method at power stage for matching the CAN bus on switching behavior.

3.2 Structure of Transmitter

Fig. 3.1 shows the block diagram of the transmitter. Compared with the typical transmitter shown in Fig. 2.2, it consists of a Digital block, pre-driver (PD), power switch (PSW) and interface switch (IFSW). PSW and IFSW are included in the power stage which drives the CAN bus. Digital block converts TXD signal from MCU into TXDH and TXDL signals which can drive the high and low sides of power stage (PSW and IFSW) at the same time. PD consists of several unit blocks, called as PD, forming 30 cascade stages, and drives both sides of the power stage. PSW consists of 30 cascade stages of unit PSWs which can drive CANH and CANL to 1.1mA. This structure achieves linear slopes of transitions at the CAN bus. Each unit PSW acts as a current source, generating a constant current so as to achieve the symmetry of the CAN bus voltages. The objective of IFSW is to protect the transceiver from the reverse voltage on the CAN bus, which ranges from -27V to 40V. Outside of the chip, the equivalent resistors of terminal resistors of the CAN bus are represented as 60Ω.

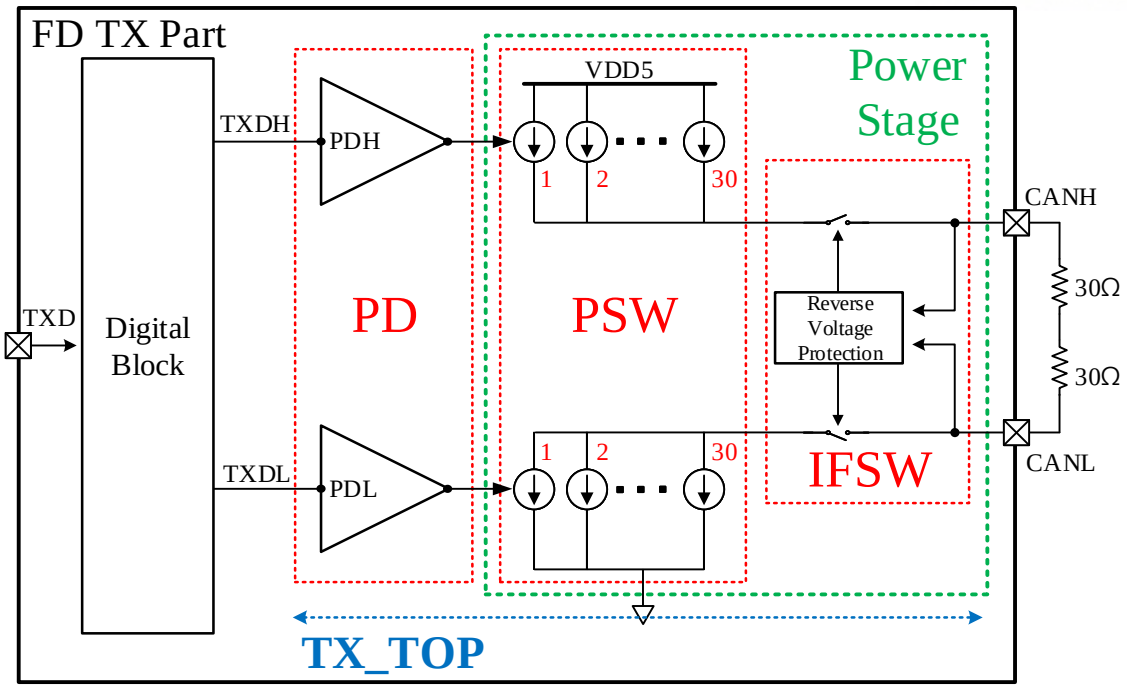


Fig. 3.1 Block diagram of the transmitter part.

Table 3.1 shows the signal information of the transmitter path from TXD to the CAN bus. The signals of CANH and CANL is shown as the voltage levels which are the analog signals. Fig 3.2 shows the sub-block configuration of TX_TOP. PD is separated by PD_H and PD_L which drive both sides of the power stage. A pair of unit PD blocks is connected to unit PSW block. Each unit PSW block is connected to CANH and CANL pins driving the CAN bus at the same time. IFSW blocks act as diodes in Fig. 2.2. They sense the CAN bus voltages and determines whether or not they connect the node between PSW and the CAN bus using the switches.

Table 3.1 The signal information in the transmitter path.

State	TXD	TXDH / TXDL	CANH / CANL
Dominant	Low	Low	3.5V / 1.5V
		High	
Recessive	High	High	2.5V
		Low	

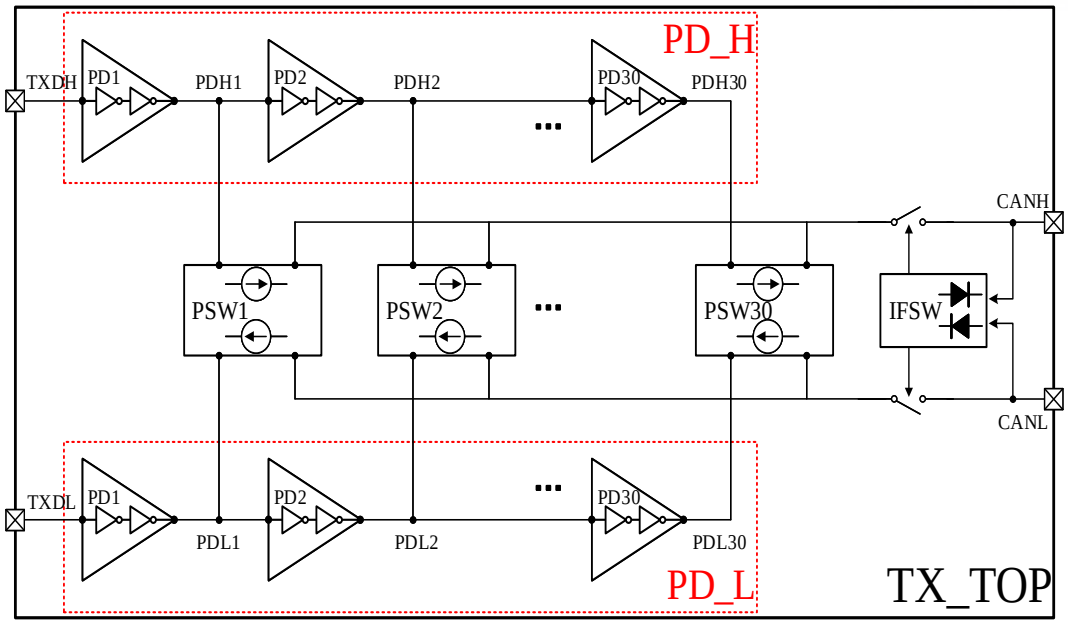


Fig. 3.2 Sub-block configuration of the TX_TOP.

Fig. 3.3 shows the signal transitions of the CAN bus voltage when the transmitter is sending a recessive-to-dominant and dominant-to-recessive signals. If the transmitter sends a recessive to dominant signal, the current drives through the CAN bus using 30 stepwise current sources to achieve a linear rise time. On the other hand, when sending a dominant to recessive signal, it stops driving the current sources.

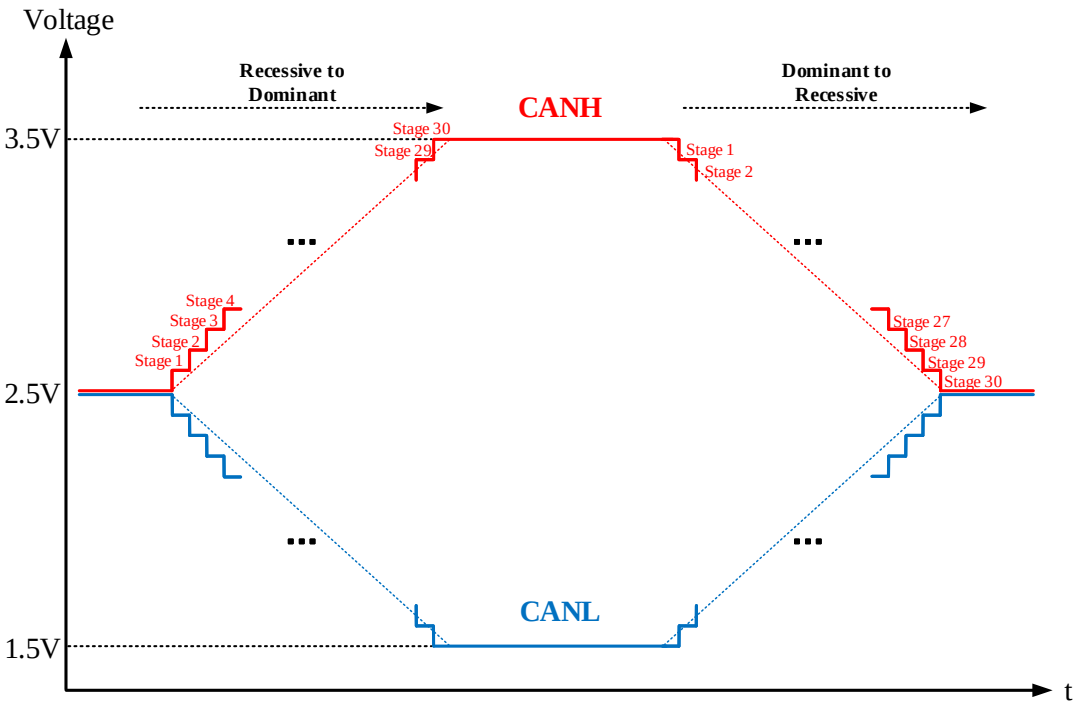


Fig. 3.3 The signal transitions at the CAN bus using 30 steps current sources.

Fig. 3.4 shows the process of sending a dominant signal from the MCU to the transmitter of the CAN transceiver. In normal operation, IFSW blocks turn on the switches to connect PSW and the CAN bus. The driving process proceeds with 30 steps of unit PSW block. Each unit PSW block drives the stepwise current of 1.1mA through the CAN bus.

If MCU sends a dominant signal (Logic 0) to TXD pin, the digital block controls the PD block. At the PD block, each unit PD drives each unit PSW. In Fig. 3.4 (a), the TXDH and TXDL signals arrive at a pair of PD1 blocks which drive PSW1. PSW1 drives CANH and CANL connected with the CAN bus, driving a current of 1.1mA through the CAN bus. At the same time, PD1 blocks drive the next PDs (PD2). They also drive PSW2, resulting in driving an additional current of 1.1mA through the CAN bus. This process proceeds in series until the TXD signal arrives at the end of the PDs (PD30). In Fig. 3.4 (c), all the PD blocks drive PSW blocks. The total current flowing through the CAN bus is 33.3mA, where the voltage levels are 3.5V at CANH and 1.5V at CANL.

On the other hand, if the MCU sends a recessive signal (Logic 1) to a TXD pin, each pair of PD blocks turns off the PSW block in series. This reduces the current from 33.3mA to 0A in 30 steps (Each step is 1.1mA). In the recessive state, the bus voltage results in 2.5V of CANH and CANL.

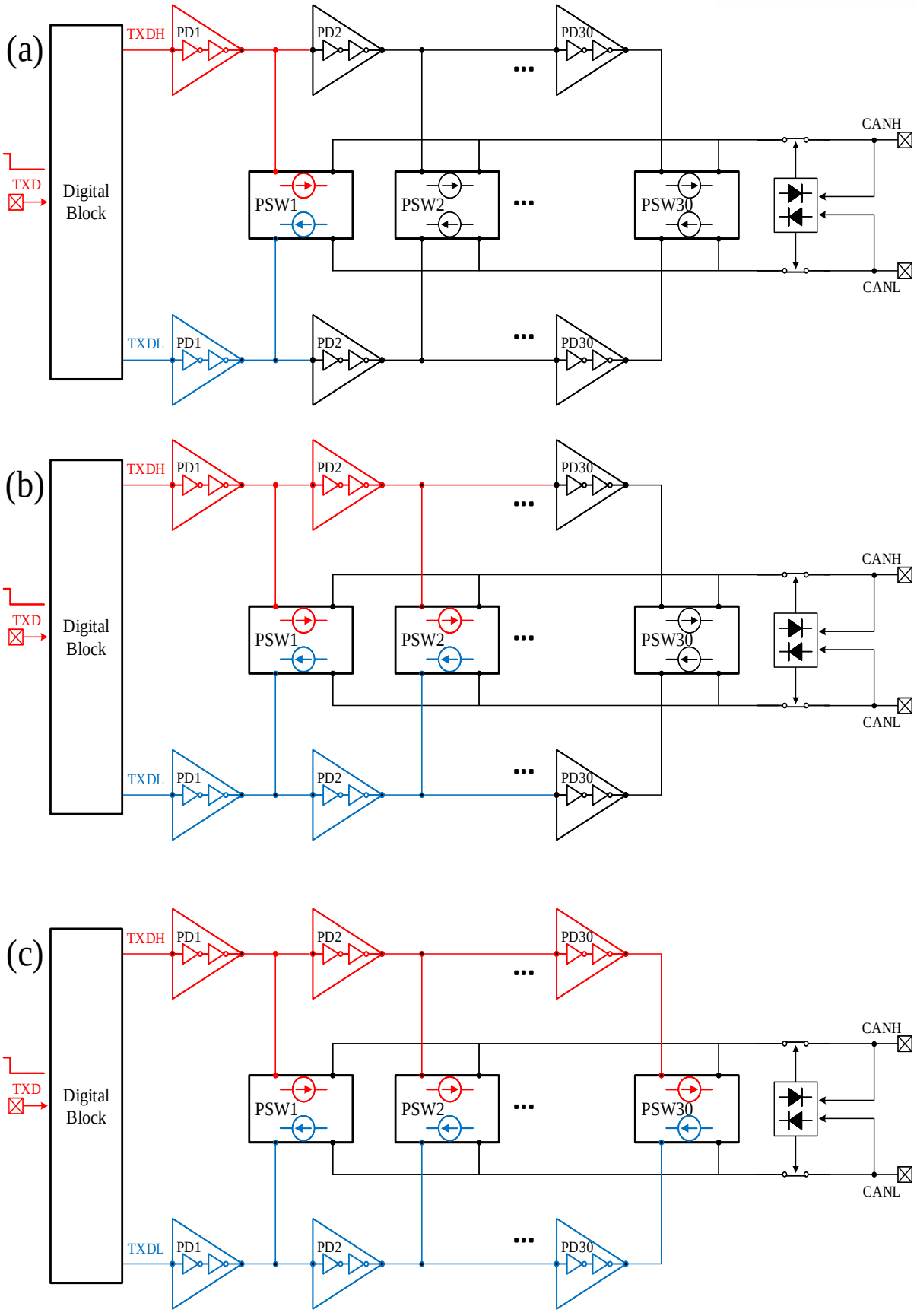


Fig. 3.4 The process of sending a dominant signal from MCU to the transmitter.

3.3 Structure of Receiver

The receiver part is shown in Fig. 3.5, where i_canh and i_canl are input pins connected to the CAN bus and o_rxd is an output pin connected to Digital block [7]. This is the receiver which has been used for the classical CAN transceiver [7]. Compared with Fig. 2.9, this receiver consists of analog blocks which don't need a clock. RxFEDiv block is the level-scalier which reduces the voltage from the CAN bus. It prevents the over-voltage injection from breaking the gate oxide of MOSFETs of the receiver. RxFEOfs block is the block that makes the offset to recognize the recessive state of the CAN bus signal. This is because the voltage levels of the recessive state at CANH and CANL are common-mode voltage. To recognize it as a recessive signal at the comparator, the shifts of voltage levels at CANH and CANL are needed. RxFEComp block is the comparator which has hysteresis function. Noise at the CAN bus signal can cause output transition above and below the threshold voltage resulting in an erratic output signal. Thus, the hysteresis range should be wide enough to reject the noise from the CAN bus. It converts the CAN bus signal to the digital signal for the Digital block of the CAN transceiver.

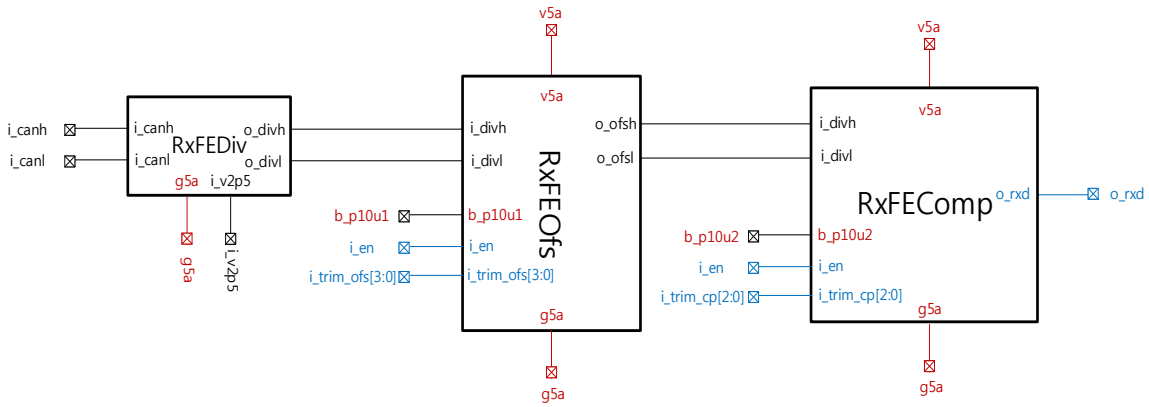


Fig. 3.5 Sub-block diagram of receiver part [7].

3.4 Concept of Cross-control Method

In this part, a new concept is introduced, the Cross-control Method, which involves the controlling of two switches located in high and low sides, Cross-control Method, is introduced. The key point of the Cross-control Method is to control the two separate switches accurately, reducing the process variations and device difference of the two switches. The features which are different with the ordinary method are following below.

First, two drivers directly control each unit cell of the switches. Unlike the ordinary structure, both switches consist of a summation of the unit cells. Each unit cell is controlled by each driver to achieve accurate operation. This structure can reduce the process variations and the difference of current at both switches.

Second, each driver alternates the unit cells of both switches stopping a chain reaction of the unit cells of each switch. Fig. 3.6 shows the difference of the threshold voltages between NMOS and PMOS using the same current driving strength at the operating point, where the red line is the maximum voltage gate-source and V_{th} is the threshold voltage of MOSFET. Because of this difference, it is difficult to match two switches in the conventional method of sequentially turning on and off only one unit MOS. This cross-control reduces the mismatch of the operation of the two switches. If the driver finishes controlling one cell of the low switch, the driver controls one cell of the other switch.

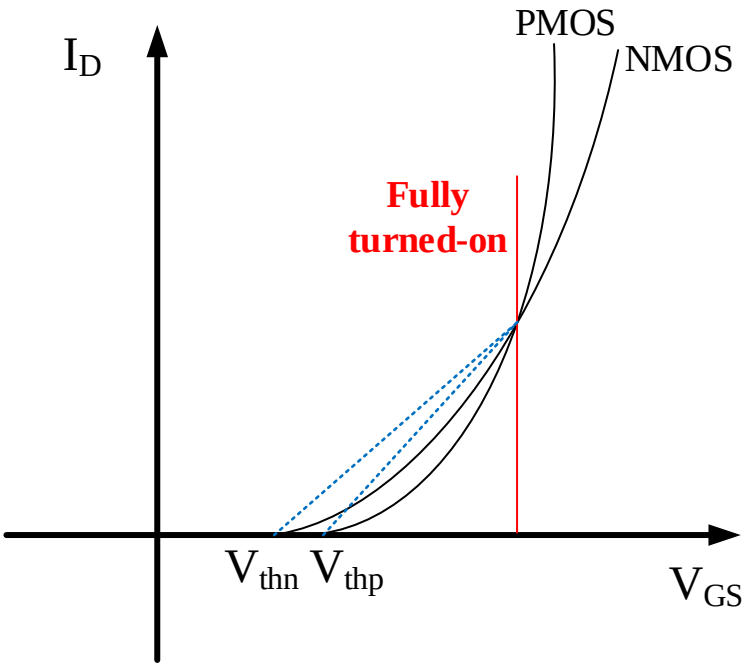


Fig. 3.6 The difference of the threshold voltages between PMOS and NMOS.

Fig. 3.7 shows the block diagram of the Cross-control Method. Both high and low side switches consist of n pair of unit cells ranging from P1 and N1 to Pn and Nn where NMOS and PMOS are used. Each driver which has n channels, DriverH and DriverL, alternates the unit cells of both switches.

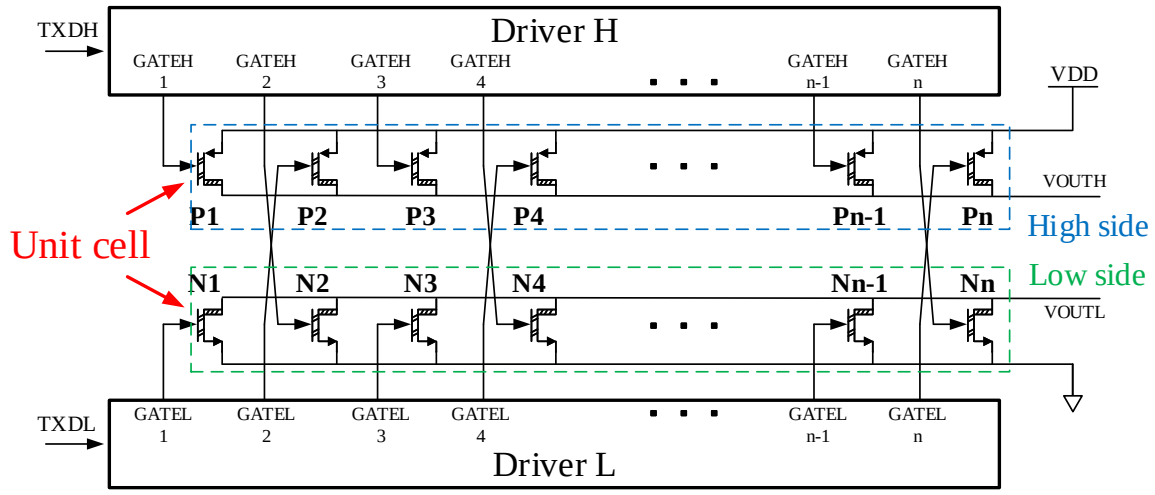


Fig. 3.7 The block diagram of the Cross-control Method.

To introduce the operation of the Cross-control Method, Fig. 3.8 shows the simple drivers which have 4 channels to control 4 pairs of unit cells. Because threshold voltages of both MOS are different, a turn-on time of PMOS and NMOS are different to each other. Let $T_{on,N}$ and $T_{on,P}$ be the turn-on time of NMOS and PMOS. If the unit cells have a small width and low driving capacity of the drain current, the relation between the gate voltage and the drain current of the MOSFET which is in the triode region can be linearized, as shown in equation (1).

$$V_{gs} \propto \frac{1}{R_{on}} \propto I_D \tag{1}$$

Fig 3.9 shows the timing diagram operated by DriverH and DriverL and the current difference between the high side switch and low side switch, where $T_{on,N}$ and $T_{on,P}$ is the turn-on time of NMOSs and PMOSs. DriverH drives P1, N2, P3 and N4 in series and DriverL drives N1, P2, N3, P4 in series. Using the Cross-control Method, the drivers are designed to keep the current difference at zero to avoid mismatch. This method can automatically try to match the operation of both sides of switches without using feedback structure or trimming bits of the drivers. Also, the turn-on and turn-off time of both drivers are the same as $2T_{on,P} + 2T_{on,N}$. This method matches the average operating time of both switches, regardless of the process variations.

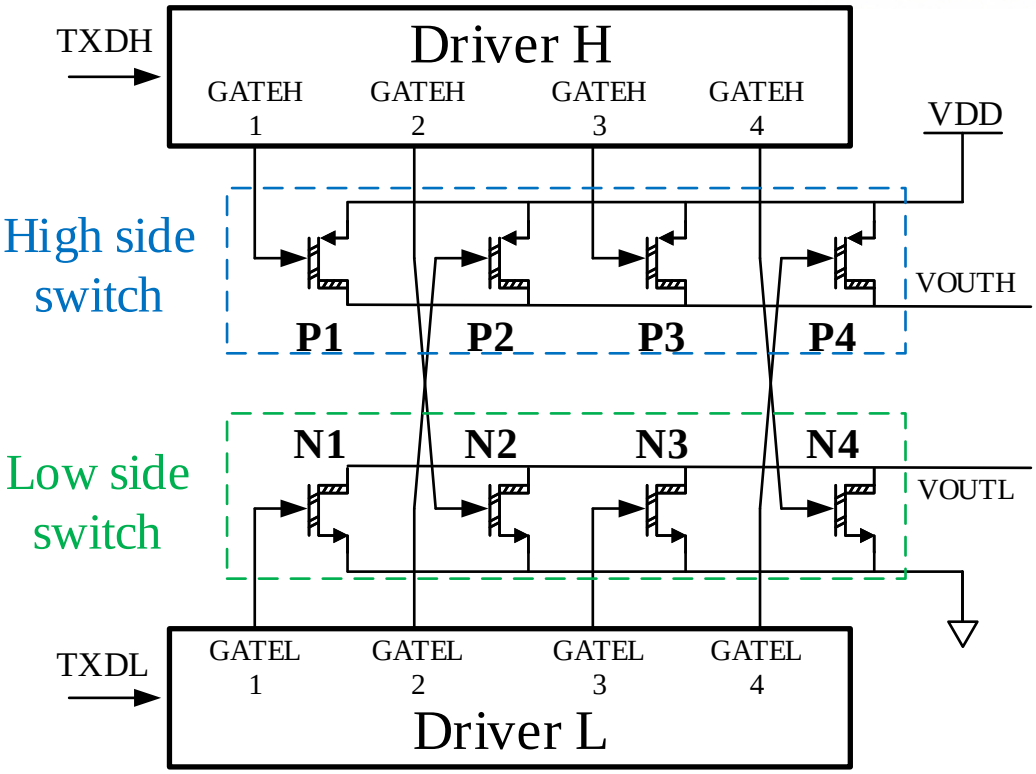


Fig. 3.8 The simple drivers with 4 channels. N1~N4 and P1~P4 are the unit cells.

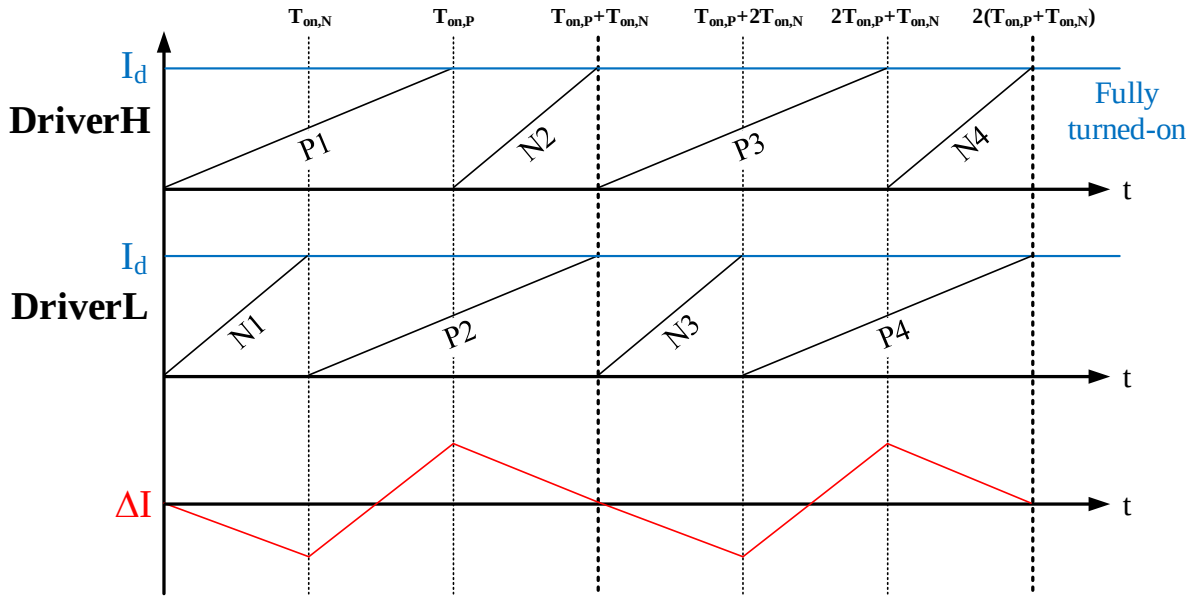


Fig. 3.9 The timing diagram of the drivers. Red line is the current difference between both switches.

3.5 Application of Cross-control Method in the Transmitter

The Cross-control Method controls both sides of the current source, known as PSW, which drives the CAN bus. When both pre-drivers turn the current sources on and off, this method matches the turn-on and turn-off time of the current sources. Also, this method reduces the difference of the current flowing through the CAN bus. In the ordinary power stage shown in Fig. 2.2, each driver independently turns on and off each side of the switch in the power stage resulting in a mismatch of the CAN bus on switching behavior. But, this method improves matching the CAN bus on switching behavior. Fig. 3.10 shows the application of the Cross-control Method in the transmitter. Unit PSW blocks are applied to this method.

Fig. 3.11 shows the circuit implementation of unit PSW which applies to the Cross-control Method. Unit PSW consists of 4 pairs of high and low side current sources which drive the CAN bus, 3 stages of the cross-control mirrors (#1 ~ #3) to match the drive strength of high and low side current sources. The circuit implementations using multiple stages improves matching the CAN bus on switching behavior. Each of the current sources is controlled by each stage of the cross-control mirrors. The cross-control mirror controls the next current sources located at the opposite side of the cross-control mirror. For example, if the cross-control mirror gets the bias current from the current source of low side, it controls the current of the next current source located at the high side.

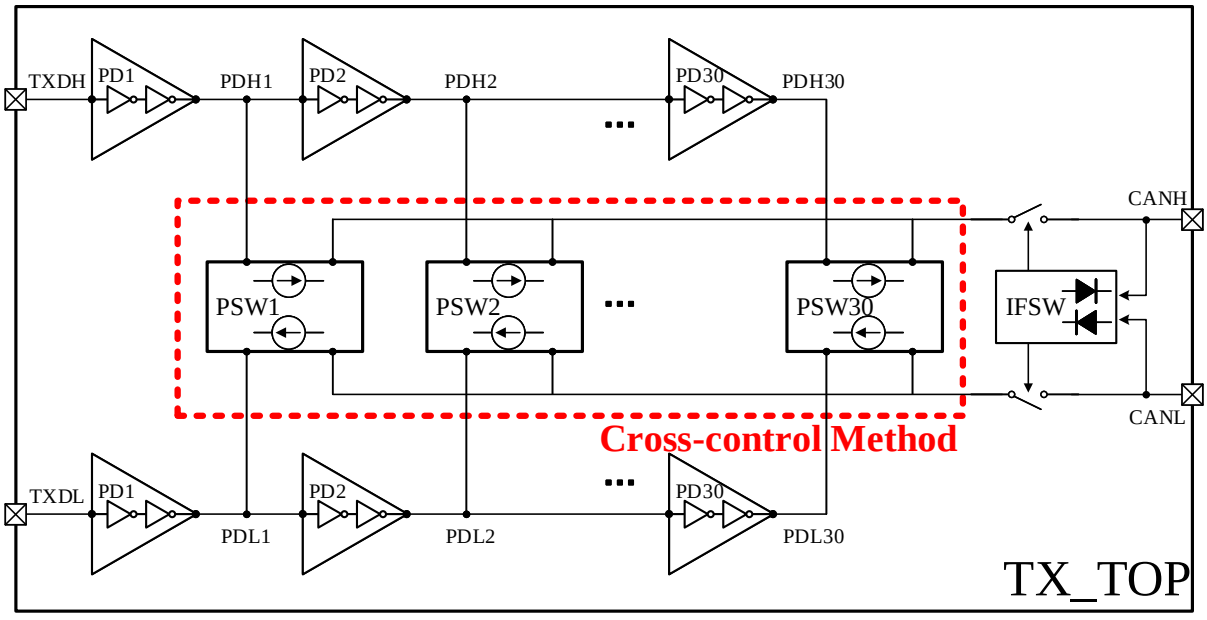


Fig. 3.10 The application of the Cross-control method in the transmitter.

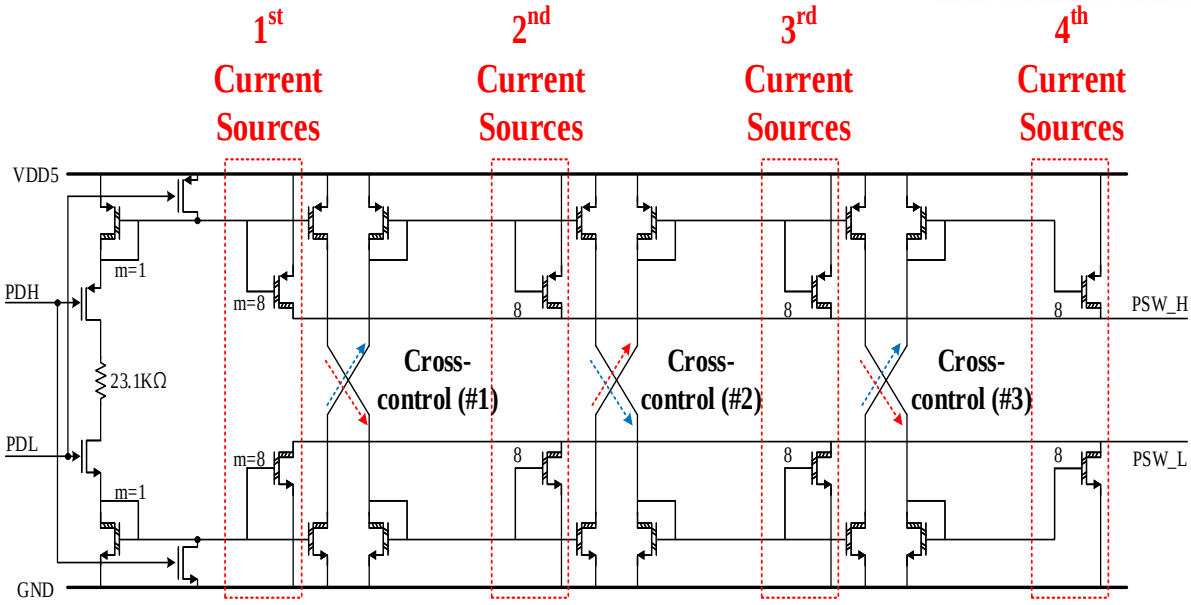


Fig. 3.11 The circuit implementation of unit PSW block.

Fig. 3.12 shows the process of sending a recessive-to-dominant signal in a unit PSW, where PDH and PDL control the switches which activate current bias. Fig. 3.12 (a) shows the moment when the unit PSW receives the signal from both sides of PD blocks. At this moment, the current bias is activated turning on the first current sources around 270μA of the current generation. Fig. 3.12 (b) shows that the first stage of the cross-control mirrors which are connected to the other side of the current sources turn on the second current sources. By turning on the current sources, the second stage of the cross-control mirrors is simultaneously activated, as in Fig. 3.12 (c). Using the Cross-control Method, the second stage of cross-control mirrors turn on each third current source on the opposite side. Finally, in Fig. 3.12 (d), the third stage of cross-control mirrors is activated with the fourth current sources. Thus, the current by unit PSW rises up to 1.1mA sequentially through the CAN bus.

The operating process for sending a dominant-to-recessive signal is the reverse process of sending the recessive-to-dominant signal. Fig. 3.13 (a) shows the moment when the PSW receives the signal from both sides of PDs. The switches in the bias path turn off the current bias. The bias of the first current sources turns off the first stages. Fig. 3.13 (b) to (d) shows the process of turning off the current sources using the Cross-control Method. The process proceeds with the four pairs of current sources in series by turning off sequentially.

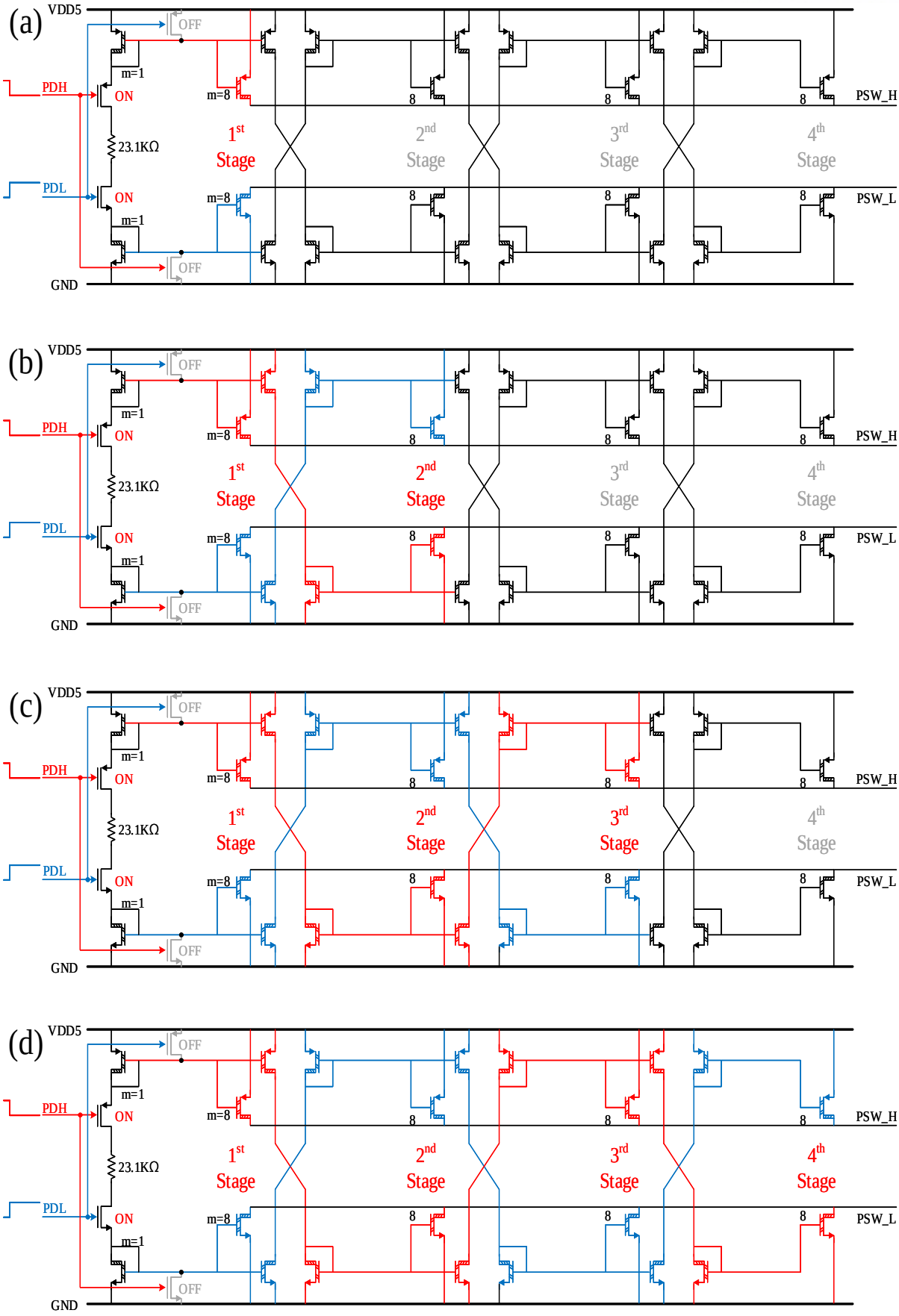


Fig. 3.12 The process using a Cross-control method which sends a recessive-to-dominant signal.

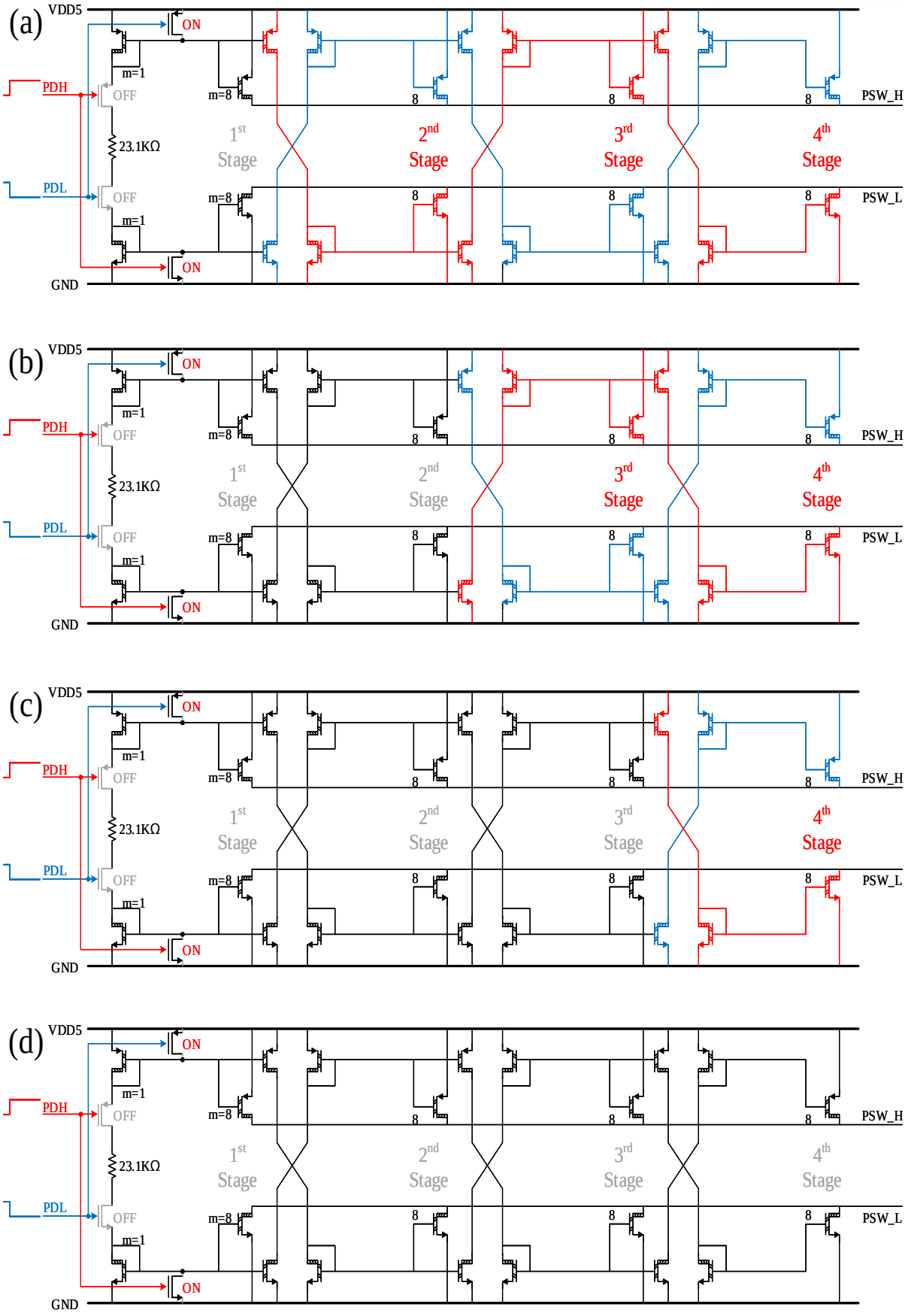


Fig. 3.13 The process using a Cross-control method which sends a dominant-to-recessive signal.

3.6 Circuit Implementations of the Cross-control Method

The circuit implementations of the Cross-control Method were applied to the transmitter.

A. PD Block

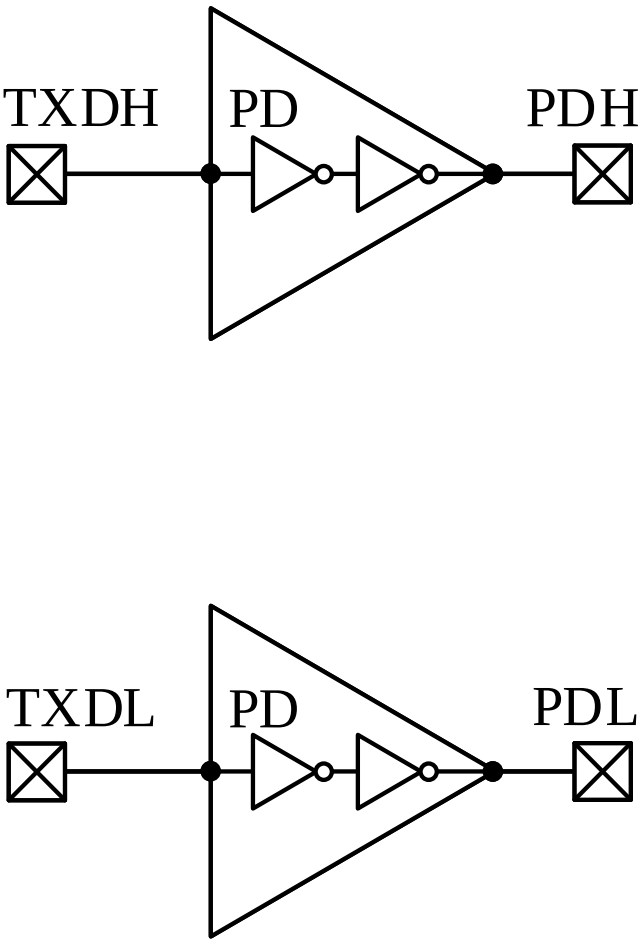


Fig. 3.14 The circuit implementation of a pair of PD block.

Fig. 3.14 shows a pair of PD blocks. The PD block is a pre-driver of the transmitter connected to the unit PSW block. This block consists of two inverters which act as a buffer. It also delays the timing of the signal at each unit PSW block for sequential control of 30 step current sources. Therefore, it can achieve the targeted slope at the CAN bus for a high bit-rate. TXDH and TXDL are input pins connected to the output of a Digital block which converts data signals from the MCU into two separated signals. They have different logic levels: if TXDH is logic 1, TXDL should be logic 0. OPDH and OPDL are output pins connected to unit PSW block which is a single power stage of the CAN bus. These pins are also connected to the next stages of unit PD blocks up to 30 steps.

B. PSW Block

PSW block is the power stage of the CAN bus. It is the core part of the proposed transmitter which improves matching the CAN bus on switch behavior presented as the Cross-control Method.

Implemented with LDMOSs, unit PSW consists of 4 pairs of high and low side current sources with 4 cascade stages, 3 stages of cross-control mirrors and a current bias. The 4 pairs of current sources are connected in parallel. Each current source is controlled by the cross-control mirror. The cross-control mirror consists of a pair of the typical current mirrors. Fig. 3.15 shows the circuit implementation of the unit PSW, where PDH and PDL are the input pins from PD block, PSW_H and PSW_L are the output pins connected to the CAN bus through IFSW blocks. The blue box shows the current bias and the red box shows 3 pairs of cross-control mirrors. The green box has 4 pairs of current sources.

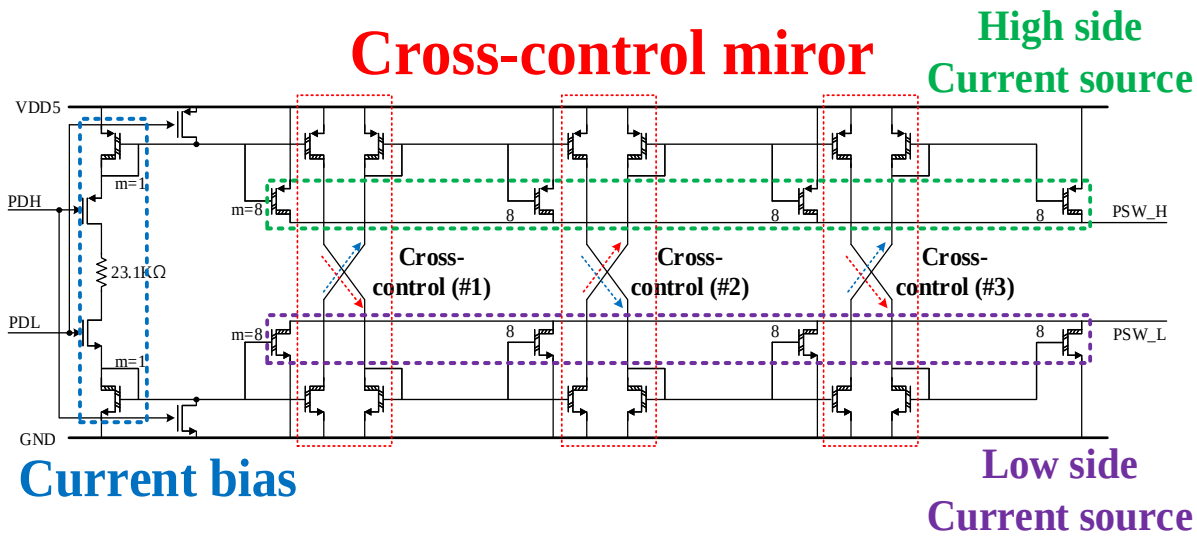


Fig. 3.15 The circuit implementation of PSW block.

C. IFSW Block

Fig. 3.16 (a) shows the power stage with IFSW block which is the protection block of the power stage. It prevents the breakdown of IC from a high-voltage injection at CANH and CANL pins. This block acts in a similar operation to the pair of diodes in Fig. 2.2. The protection range of IFSW is from -27V to 40V of voltage change on the CAN bus which can occur by automotive battery specification. Fig. 3.16 (b) shows the circuit implementation of IFSW, where PSW_H and PSW_L are connected with 30 unit of PSWs, CAN_H and CAN_L are output pins connected to the CAN bus. M1 and M2 act as switches. They are operated by comparing the reference voltage with the voltage level of the CAN bus. If the CAN bus voltage exceeds 4V, M1 is turned off to protect the 5V source. On the other hand, if it drops to 1V, M2 is turned off to protect over-current from the ground to the CAN bus.

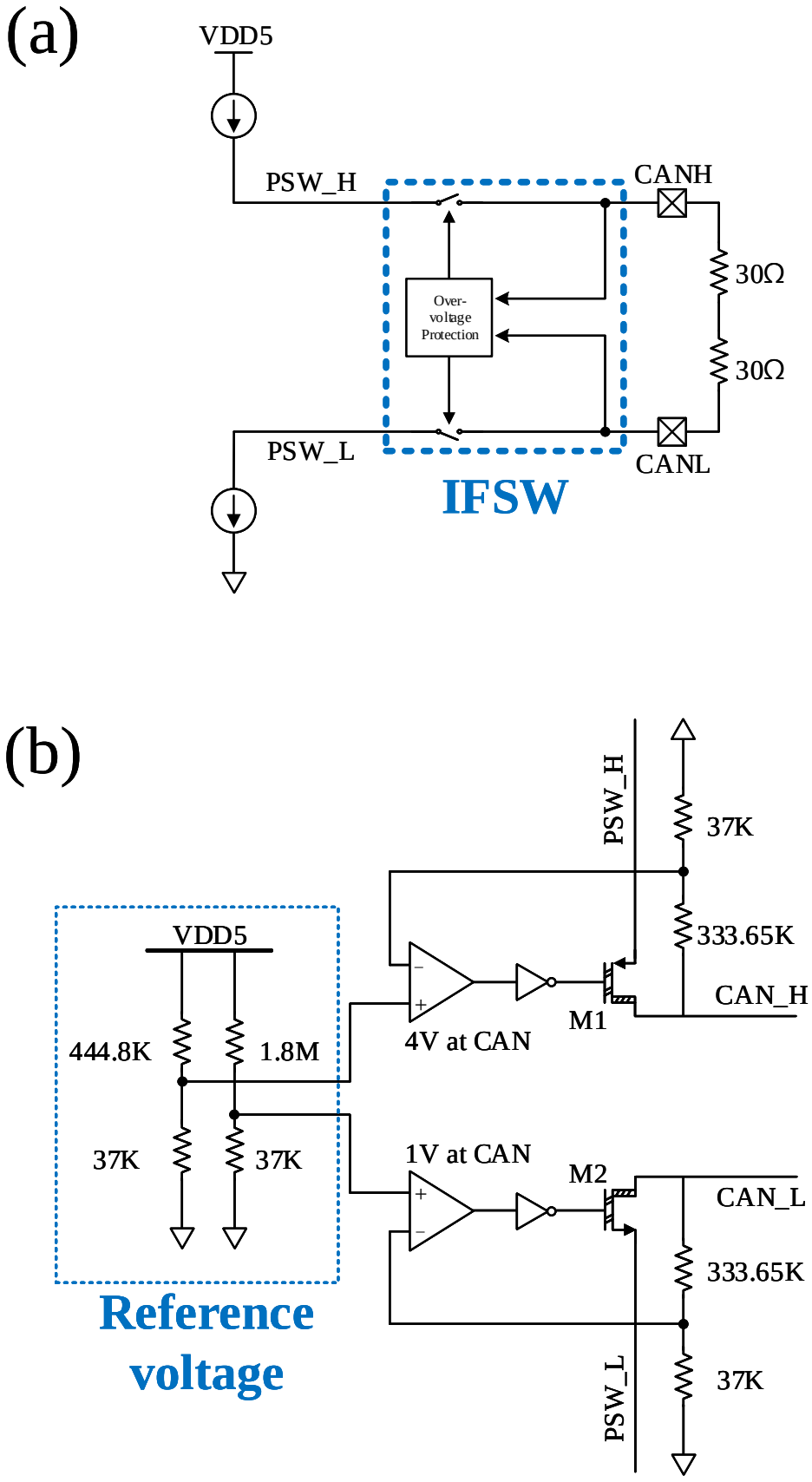


Fig. 3.16 The block diagrams IFSW block. (a) is the block diagram of the power stage and (b) is the circuit implementation of IFSW block.

3.7 Simulation Results

To verify the proposed CAN-FD transceiver, two kinds of CAN-FD transceivers were implemented. Version 1 is the core structure circuit which has a transmitter and receiver. Version1 aims to show the improvement of the transmitter and its suitability with receiver block in classical CAN transceiver [7]. Version 2 is the stand-alone transceiver. Version2 aims to check the suitability of the transmitter with peripheral blocks in classical CAN transceiver [7].

3.7.1 CAN-FD Transceiver Version I: Core-structure Version

Fig. 3.17 shows the proposed CAN-FD transceiver with Core-structure version. This version includes only analog parts, which are the transmitter, receiver and other peripheral blocks. BI is the transmitter, RxFE is the receiver, BGR supplies a reference voltage to Igen. Igen is a current generator for BI and RxFE blocks. BGR and Igen are in a 3V domain and 5V domain includes BI and RxFE. TXDH and TXDL are the input pins which are directly injected into the transmitter, RXD is the output pin from the receiver, VDD3 and VDD5 are supply voltages, GND is the ground pin and CANH and CANL are the output pins connected to the CAN bus. TXDH and TXDL should be the same frequency and phase except for the logic level. If TXDH sends logic 0, TXDL should send logic 1 with the same frequency and phase.

3.7.2 CAN-FD Transceiver Version II: Stand-alone Version

Fig. 3.18 shows the stand-alone CAN-FD transceiver with the proposed circuit, where the Digital block and peripheral blocks are added from Fig. 2.20. This version can communicate between the MCU and the CAN bus. TXD and RXD are input and output pins communicating with the MCU. Power-on Reset (PoR) is the enable block waiting for the digital block to operate properly. Thermal Shutdown (TSD) is the protection block from the high-temperature condition. It stops operation of IC in high temperatures of around 160℃. Low Dropout (LDO) is the linear regulator generating 3V domain from 5V domain supplying power to BGR and Igen.

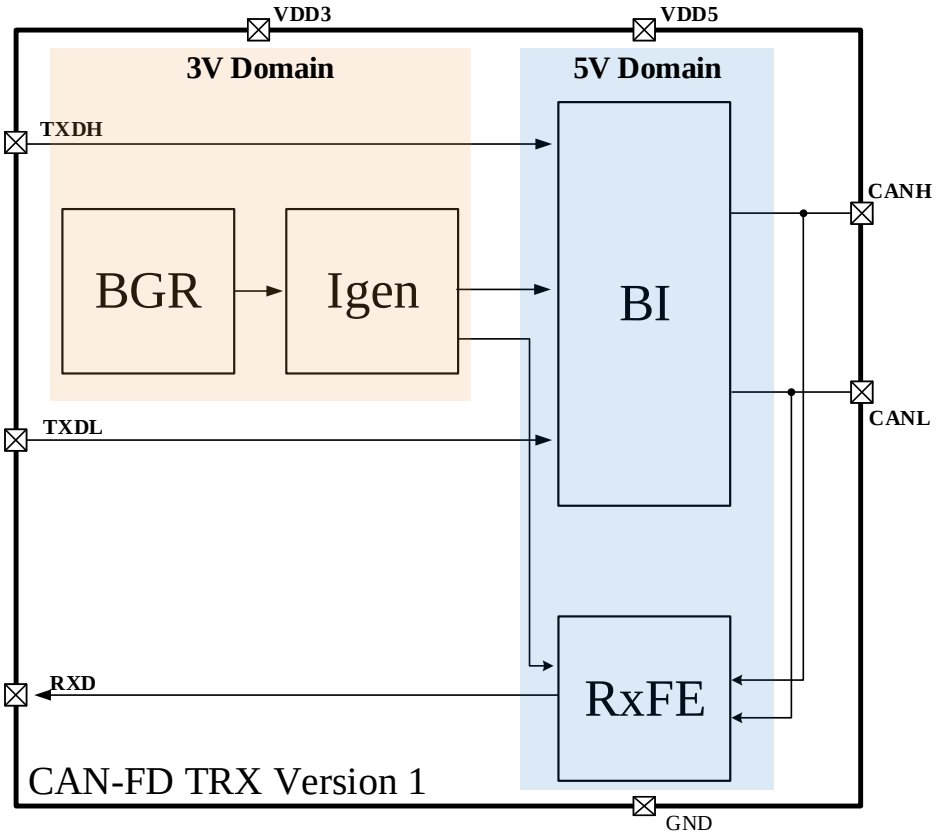


Fig. 3.17 Block diagram of CAN-FD TRX Version 1.

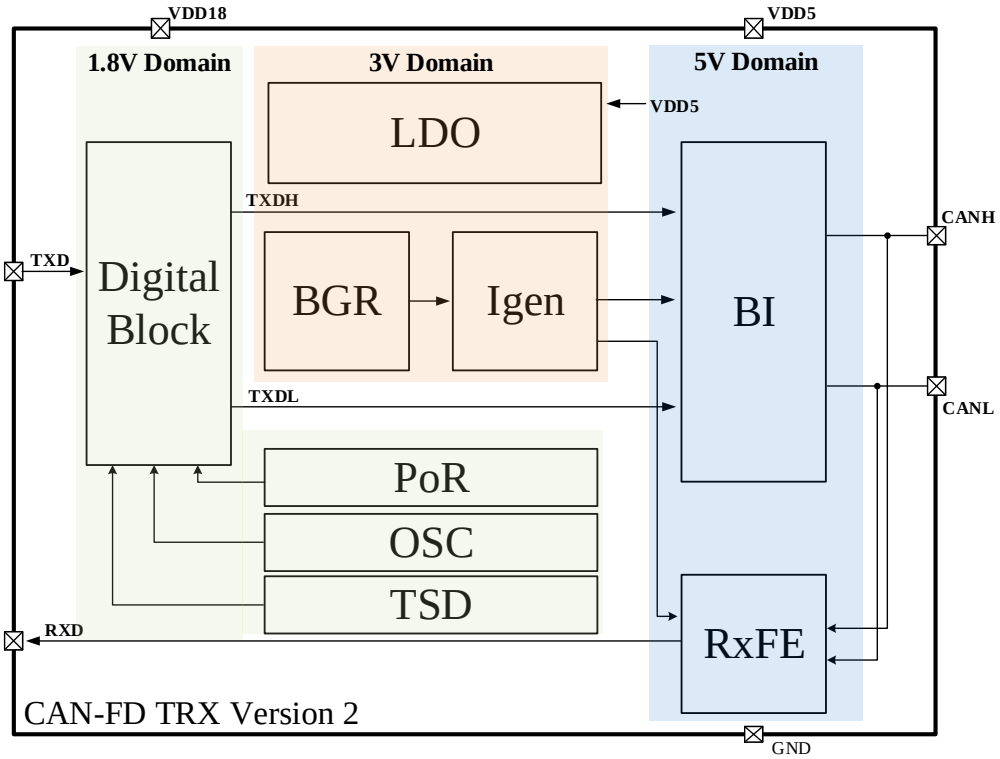


Fig. 3.18 Block diagram of CAN-FD TRX Version 2.

3.7.3 Simulation Results of Proposed CAN-FD Transceiver

Fig. 3.19 shows the simulation result of the CAN-FD transceiver Version1 in a typical process using SPICE simulation. This result shows symmetry of voltage level between CANH and CANL showing the same current driving capacity between high and low side current sources. CANH+CANL is the parameter to check matching of the CAN bus. It shows little change of voltage level verifying good symmetry on switching behavior. Both Fig. 3.19 and Fig. 3.20 show a small variation of 26mV at CANH+CANL.

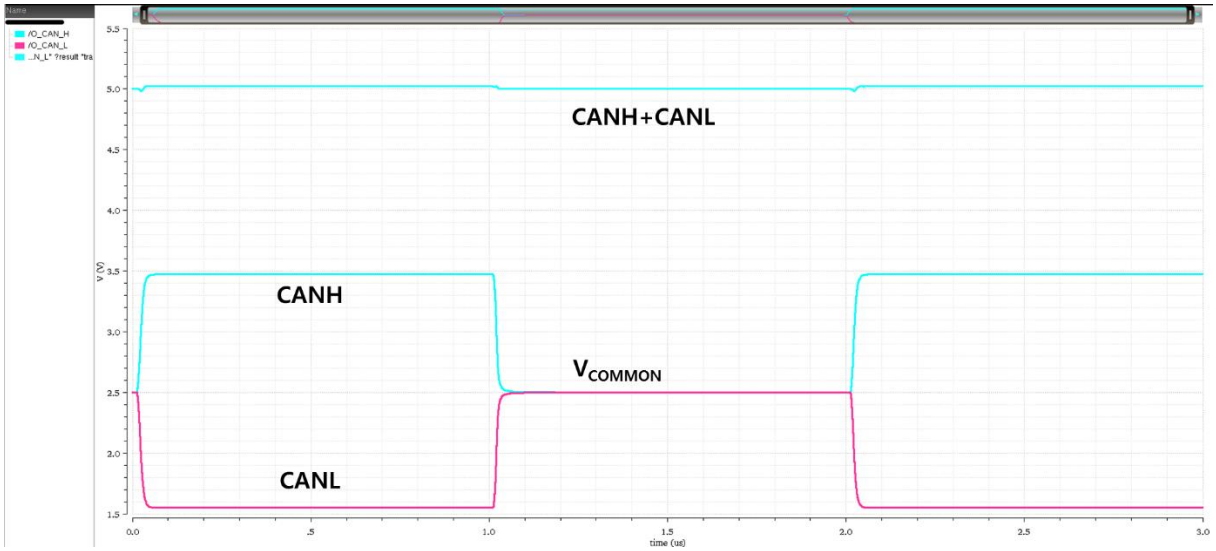


Fig. 3.19 Simulation result of CAN-FD TRX Ver1.

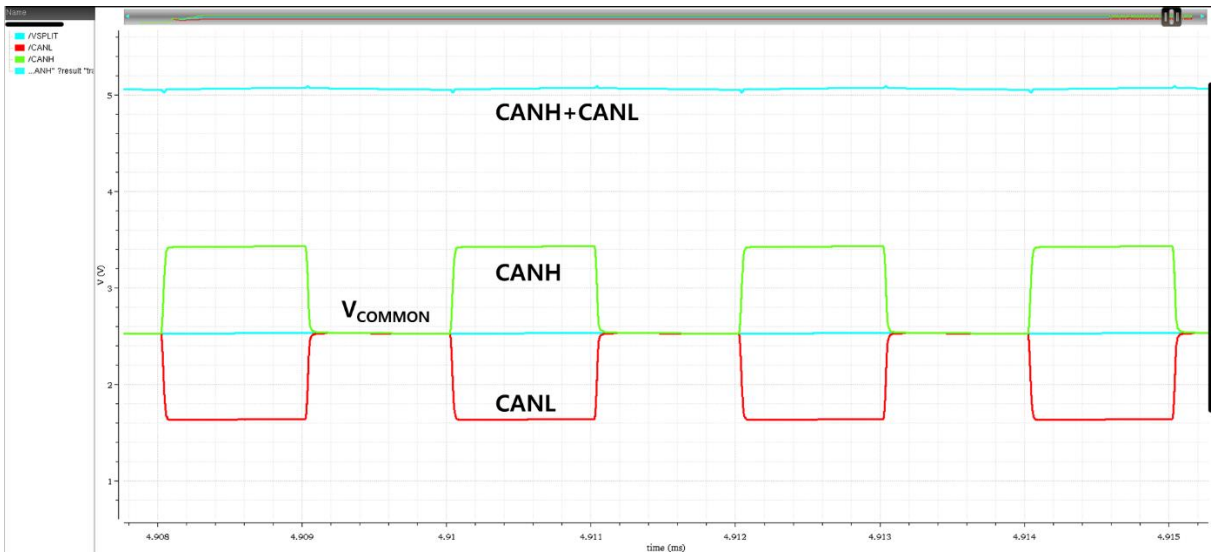


Fig. 3.20 Simulation result of CAN-FD TRX Ver2.

3.8 Layout Information

Two versions of the proposed CAN-FD transceivers including proposed architecture were fabricated using 0.18μm automotive BCDMOS process. Fig. 3.21 and Fig. 3.22 show their layouts.

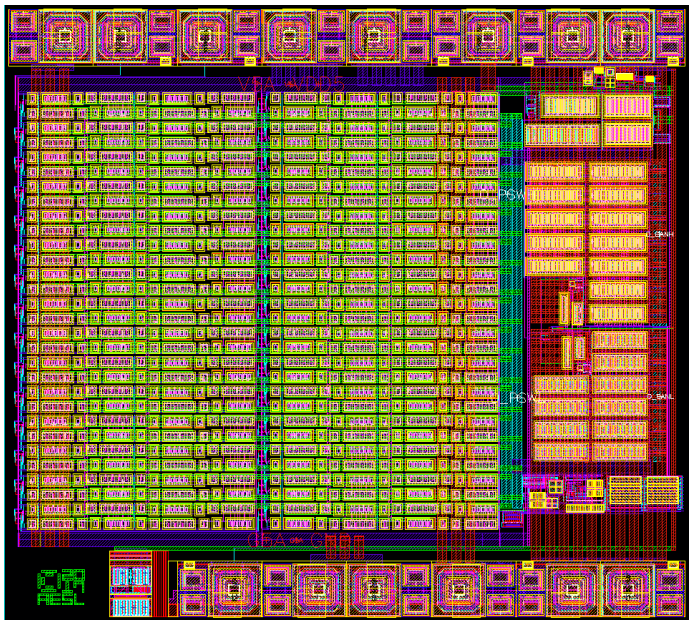


Fig. 3.21 The layout of the proposed CAN-FD TRX Ver1. The size is 1490um X 1350um.

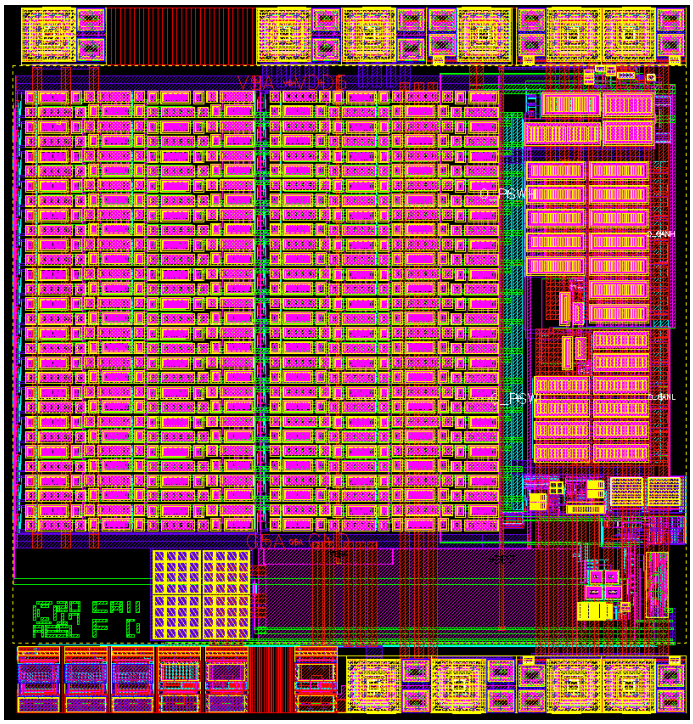


Fig. 3.22 The layout of the proposed CAN-FD TRX Ver2. The size is 1480um X 1550um.

4. Measurement Results

4.1 Experimental Setup

The experimental setup of the proposed CAN-FD transceiver is shown in Fig. 4.2. Using a power supply, a function generator and an Oscilloscope, an experiment using a single node is performed on the CAN bus. The function generator is used to supply TXD signal which controls the power stage. The power supply supplies 3V and 5V domain powers. The oscilloscope checks the CAN bus and RXD signals. Fig. 4.3 shows the experimental setup for industrial product, TCAN1041GVDQ1 [3], to compare its performances with the proposed transceiver. In both set-ups, 30Ω and 60Ω of load resistors (R_L) and 4nF of load capacitors (C_L) are used in the experiments to check the performance of each transceiver. Additionally, 0.1μF of bypass capacitors are connected to a 5V domain power line of both set-ups [3].

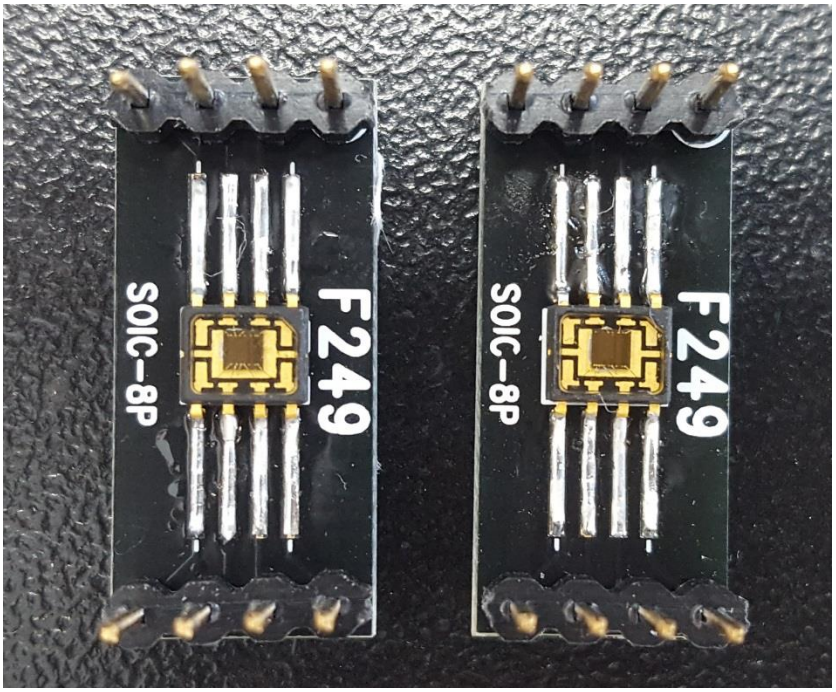


Fig. 4.1 The packaged chips (Left side is Ver1 and the right side is Ver2).

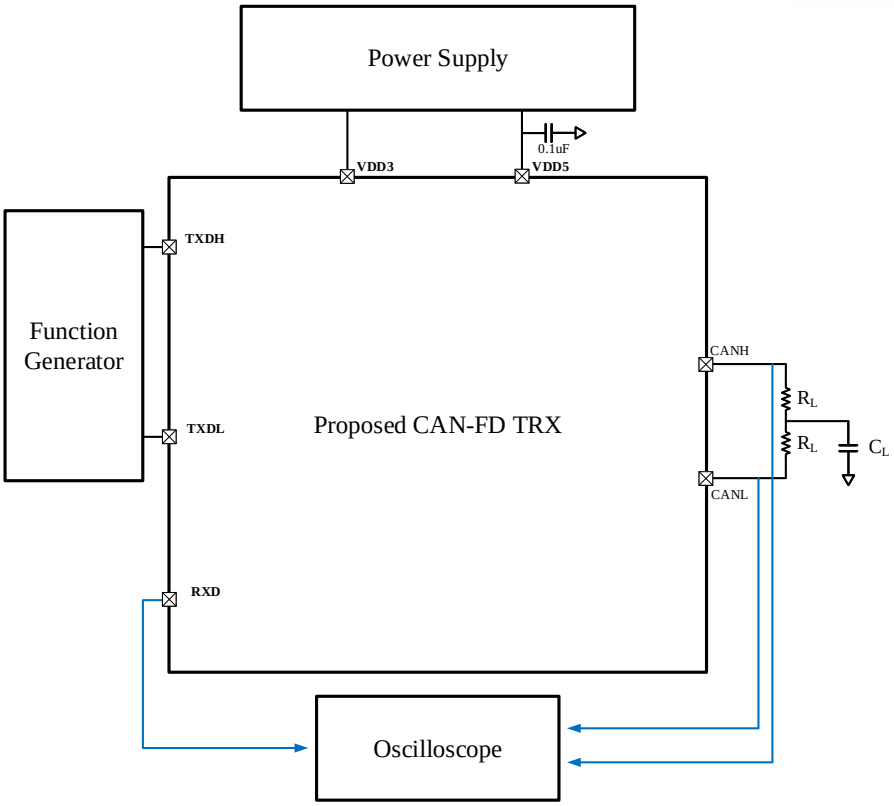


Fig. 4.2 The experimental set-up of proposed TRX.

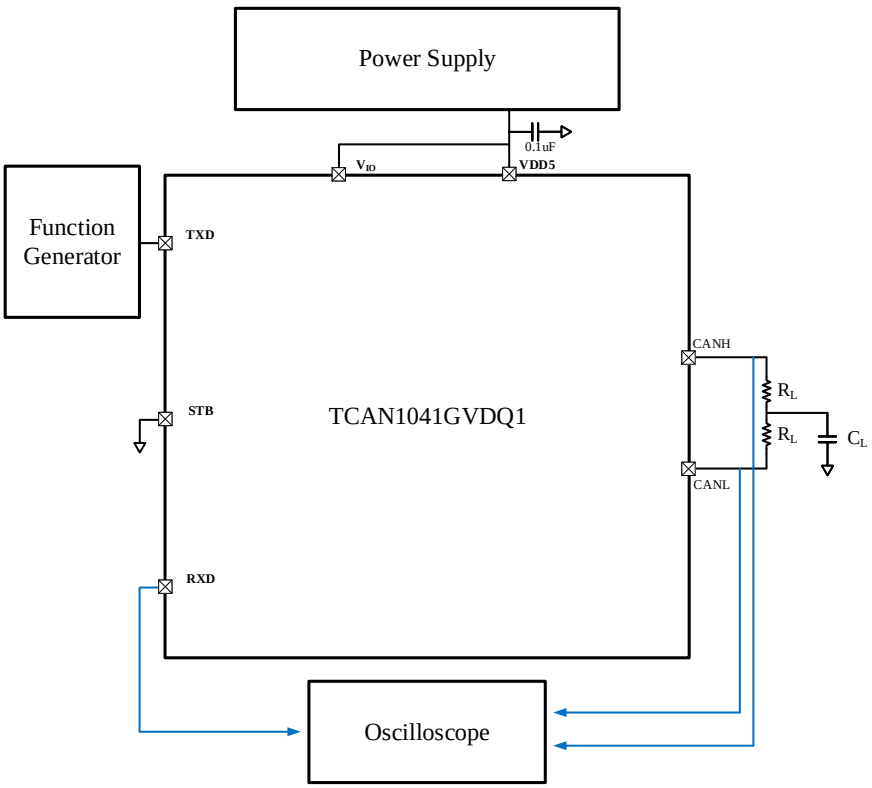
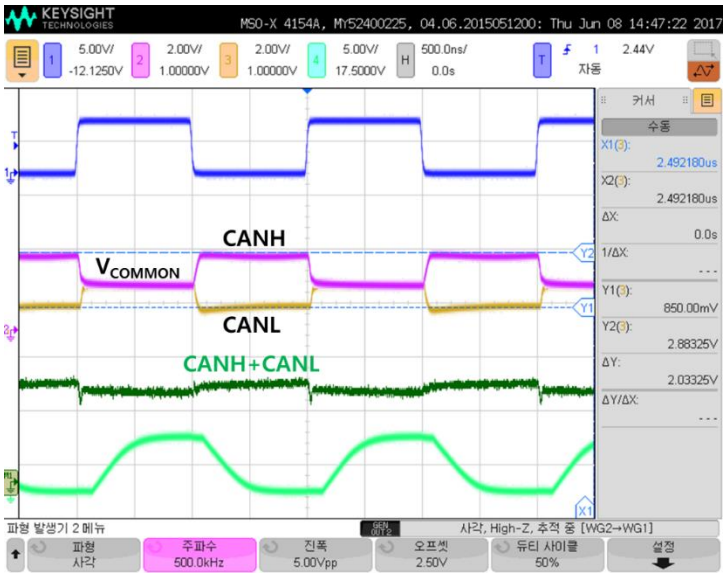


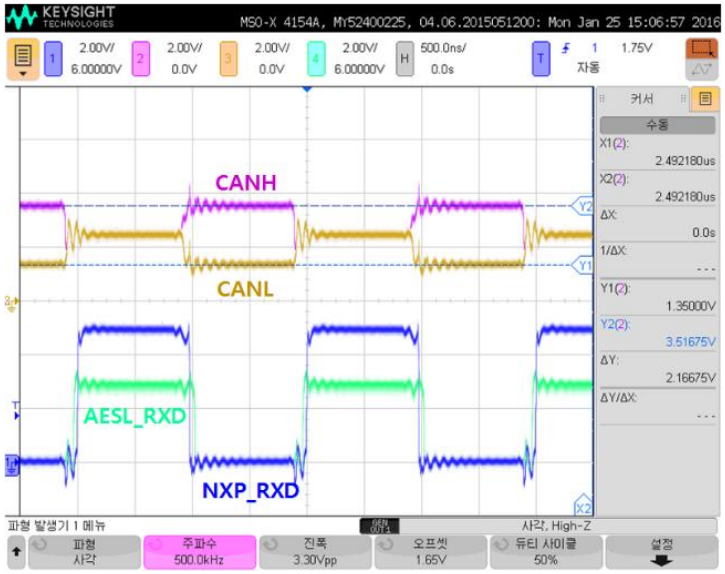
Fig. 4.3 The experimental set-up of TCAN1041GVDQ1 TRX.

4.2 Measurement Results Compared with Other Products

Fig. 4.4 to Fig. 4.6 shows the measurement result of the proposed CAN-FD transceiver comparing it with ordinary transceivers at each data-rate. CANH and CANL are the voltage levels of the CAN bus, V_{COMMON} is common-mode voltage and CANH+CANL is the voltage level symmetry of the CAN bus. Compared to other transceivers, the classical CAN transceiver [7] and TCAN1041GVDQ1 [3], the proposed transceiver shows better matching of the CAN bus on switching behavior. Fig. 4.4 shows the comparison between the proposed transceiver and the classical transceiver at 1Mbps [7].



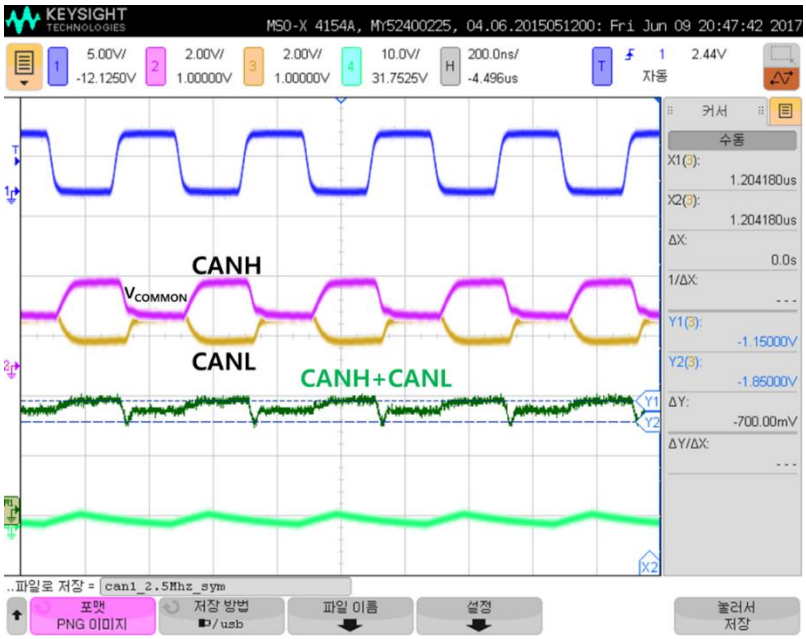
(a)



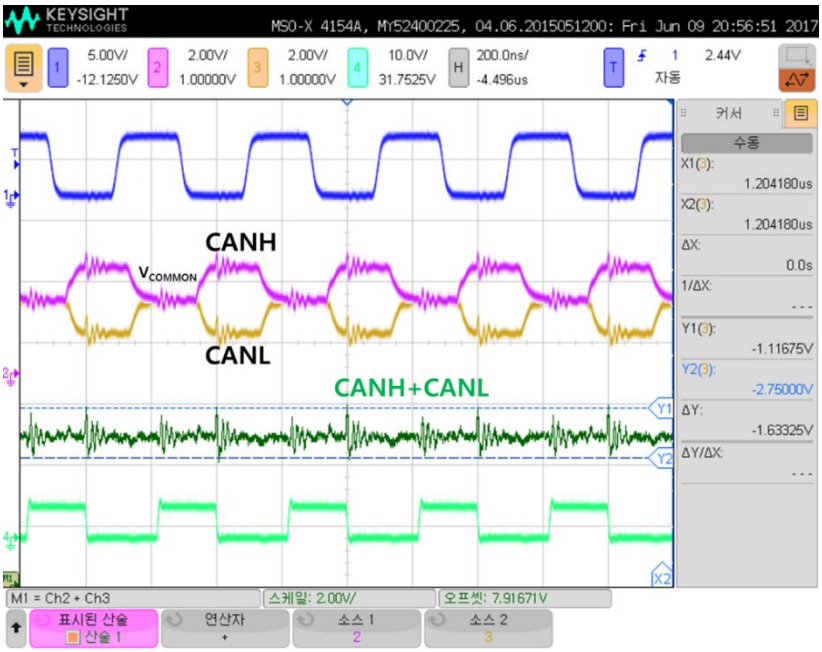
(b)

Fig. 4.4 Measurement results at 1Mbps (a) Proposed TRX (b) Classical CAN TRX [7].

Fig. 4.5 shows the comparison between the proposed transceiver and TCAN1041GVDQ1 transceiver at 5Mbps with 200ns of the bit time. The parameter of VCANH+VCANL shows 700mV of variation while TCAN1041GVDQ1 shows 1.63V of variation. These results show that the proposed transceiver is better at matching of the CAN bus on switching behavior.



(a)



(b)

Fig. 4.5 Measurement results at 5Mbps (a) Proposed TRX (b) TCAN1041GVDQ1 TRX.

Fig. 4.6 shows matching property at 10Mbps with 100ns of the bit time. The parameter of VCANH+VCANL shows 866mV of variation. The proposed CAN-FD transceiver shows good matching even at a data-rate of 10Mbps.

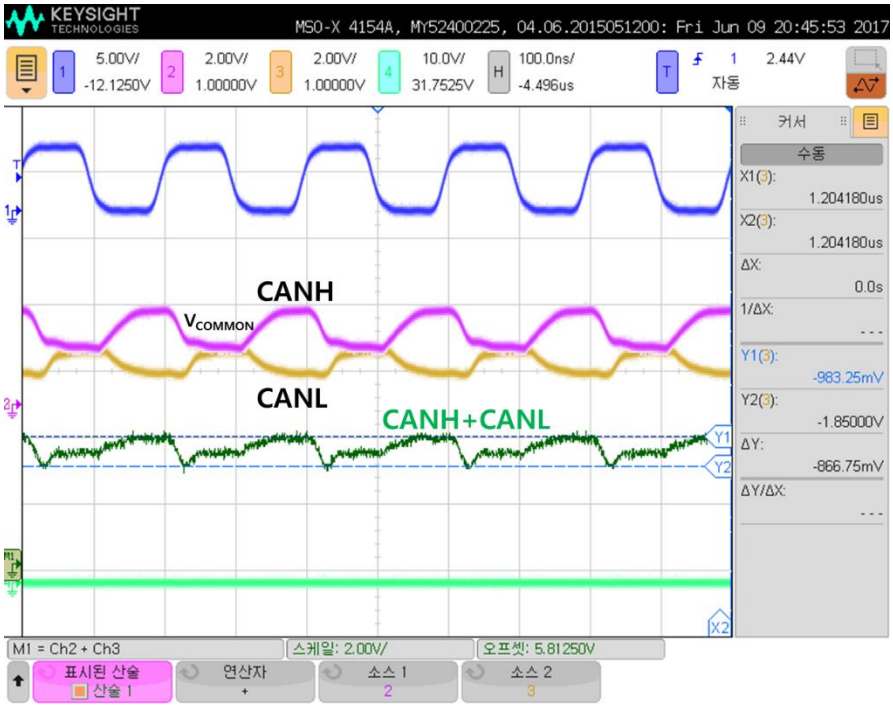


Fig. 4.6 Measurement results of proposed TRX at 10Mbps.

5. Future Works

With the proposed CAN-FD transceiver, some additional research is needed to improve the communication of the network or improve the operation of the transceiver.

First, to recognize the signal of the CAN bus, the new CAN-FD receiver design should be implemented with less propagation delay compared to the bit-time of the data frame at 5Mbps.

Second, the receiver should be optimized to meet the specific requirements of the ISO standard which include loop delay symmetry, TX delay symmetry and RX delay symmetry.

Third, the conformance test should be done according to the ISO standard which is going to be released soon.

Fourth, whether or not it is compatible with other industrial CAN-FD products, interoperability tests in a CAN-FD should proceed with other industrial products.

Finally, whether or not the transceiver meets the requirement of the automotive industry, the EMC performance of the proposed CAN-FD transceiver can be evaluated according to the IEC/TS 62228 test standard [25] for which Direct Coupling Method [26] and Direct Power Injection (DPI) [27] is used to evaluate EMC performance. Fig 5.1 shows the EMC measurement set-up to characterize EME and EMI [22].

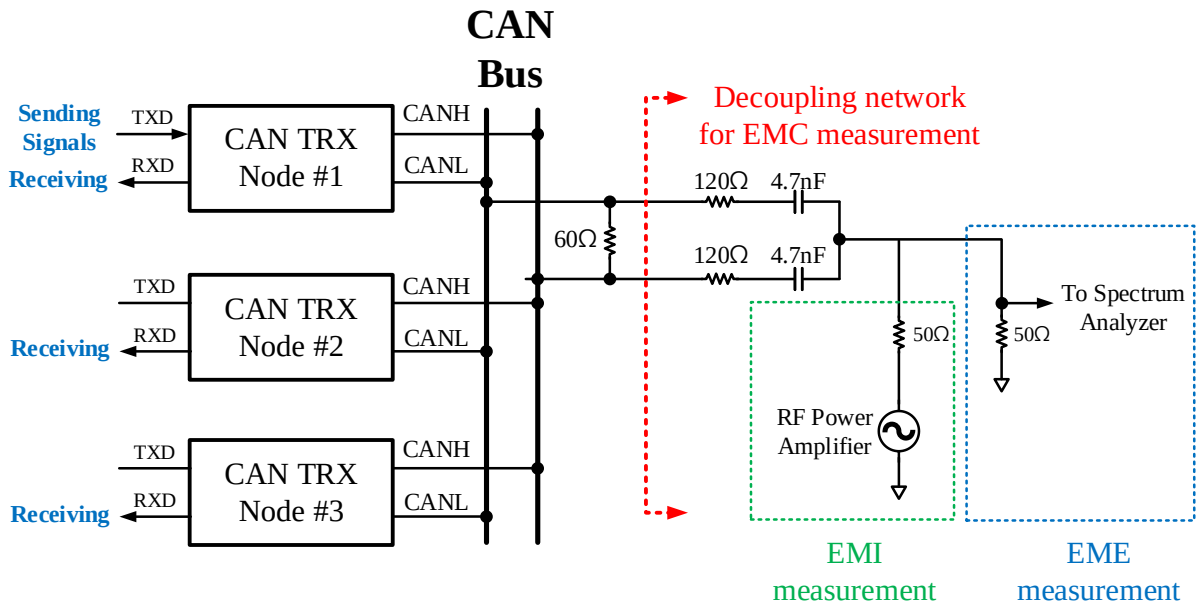


Fig. 5.1 The EMC measurement set-up to characterize EME and EMI [22].

Additionally, when applying CAN-FD to various network topologies such as star topologies or hybrid topologies, as shown in Fig. 5.1, the ringing on the CAN-FD bus occurs because of impedance mismatches in a network [28]. This limits the maximal possible data-phase bit-rate disturbing the recognition of a signal [28] [29]. Therefore, the ringing suppression circuit should be implemented to support various CAN- FD topologies.

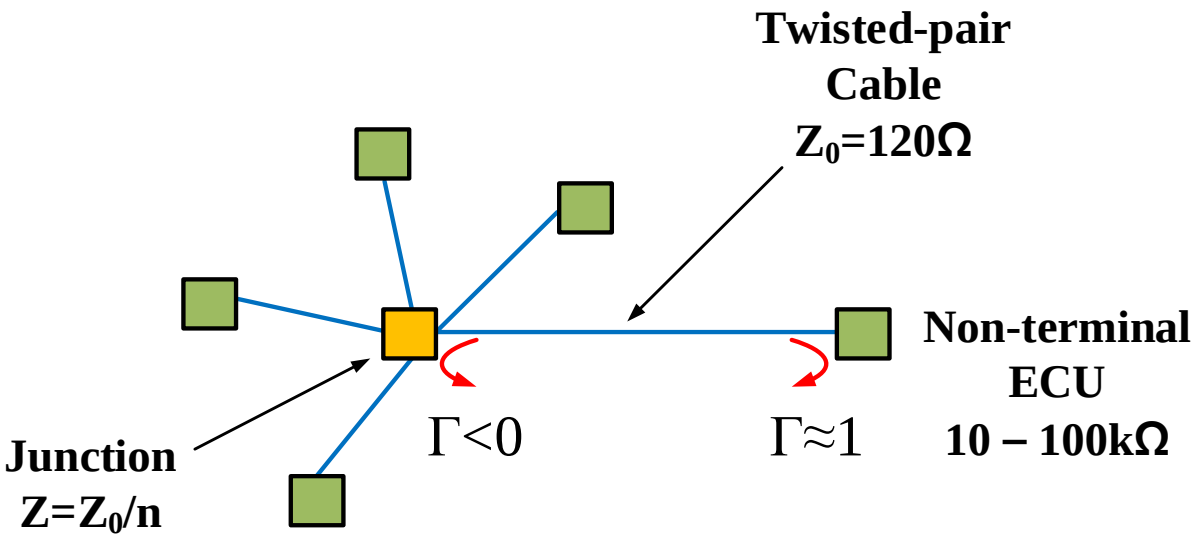


Fig. 5.2 Generation mechanism of ringing on the CAN-FD bus [28].

6. Conclusions

In this thesis, a new architecture of CAN-FD transmitter has been presented, which offers a low EMI. The proposed transceiver using the Cross-control Method and 30 step cascading current sources was used to improve matching the CAN bus on switching behavior. Two versions of the CAN-FD transceivers that include the proposed architecture were fabricated using 0.18μm automotive BCDMOS process. The measurement results show that the proposed architecture improves matching of the CAN bus on switching behavior compared to other transceivers at each data-rates. The proposed CAN-FD transceiver shows good matching even at of a data-rate of 10Mbps. Some additional research is needed to use as CAN-FD transceiver with other industrial products or to apply in another network topologies.

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