

EUR 4835 e

COMMISSION OF THE EUROPEAN COMMUNITIES

**A TIMECODER FOR NEUTRON
TIME-OF-FLIGHT EXPERIMENTS**

by

S. DE JONGE

1972



**Joint Nuclear Research Centre
Geel Establishment - Belgium
Central Bureau for Nuclear Measurements-CBNM**

LEGAL NOTICE

This document was prepared under the sponsorship of the Commission of the European Communities.

Neither the Commission of the European Communities, its contractors nor any person acting on their behalf:

make any warranty or representation, express or implied, with respect to the accuracy, completeness, or usefulness of the information contained in this document, or that the use of any information, apparatus, method, or process disclosed in this document may not infringe privately owned rights; or

assume any liability with respect to the use of, or for damages resulting from the use of any information, apparatus, method or process disclosed in this document.

This report is on sale at the addresses listed on cover page 4

at the price of B.Fr. 40. -

When ordering, please quote the EUR number and the title, which are indicated on the cover of each report.

Printed by Ceuterick, Louvain
Luxembourg, May 1972

This document was reproduced on the basis of the best available copy.

EUR 4835 e

A TIMECODER FOR NEUTRON TIME-OF-FLIGHT EXPERIMENTS

by **S. DE JONGE**

Commission of the European Communities
Joint Nuclear Research Centre — Geel Establishment (Belgium)
Central Bureau for Nuclear Measurements — CBNM
Luxembourg, May 1972 — 20 Pages — 9 Figures — B.Fr. 40.—

The described timecoder is designed for neutron time-of-flight experiments at the linear accelerator of the CBNM at Geel, Belgium.

By the use of MECL II integrated circuits it features simple design and low cost. Basic channelwidth is 40 ns, which can be multiplied in 8 succeeding regions with a factor of 1 to 99, which may be different for each region. In regions where no events have to be stored, address counting is inhibited which results in optimal use of the 4096 output channels (12 bits).

The deadtime of the coder together with a buffer memory is 280 ns, permitting several events to be registered during one measurement cycle.

EUR 4835 e

A TIMECODER FOR NEUTRON TIME-OF-FLIGHT EXPERIMENTS

by **S. DE JONGE**

Commission of the European Communities
Joint Nuclear Research Centre — Geel Establishment (Belgium)
Central Bureau for Nuclear Measurements — CBNM
Luxembourg, May 1972 — 20 Pages — 9 Figures — B.Fr. 40.—

The described timecoder is designed for neutron time-of-flight experiments at the linear accelerator of the CBNM at Geel, Belgium.

By the use of MECL II integrated circuits it features simple design and low cost. Basic channelwidth is 40 ns, which can be multiplied in 8 succeeding regions with a factor of 1 to 99, which may be different for each region. In regions where no events have to be stored, address counting is inhibited which results in optimal use of the 4096 output channels (12 bits).

The deadtime of the coder together with a buffer memory is 280 ns, permitting several events to be registered during one measurement cycle.

EUR 4835 e

A TIMECODER FOR NEUTRON TIME-OF-FLIGHT EXPERIMENTS

by **S. DE JONGE**

Commission of the European Communities
Joint Nuclear Research Centre — Geel Establishment (Belgium)
Central Bureau for Nuclear Measurements — CBNM
Luxembourg, May 1972 — 20 Pages — 9 Figures — B.Fr. 40.—

The described timecoder is designed for neutron time-of-flight experiments at the linear accelerator of the CBNM at Geel, Belgium.

By the use of MECL II integrated circuits it features simple design and low cost. Basic channelwidth is 40 ns, which can be multiplied in 8 succeeding regions with a factor of 1 to 99, which may be different for each region. In regions where no events have to be stored, address counting is inhibited which results in optimal use of the 4096 output channels (12 bits).

The deadtime of the coder together with a buffer memory is 280 ns, permitting several events to be registered during one measurement cycle.

EUR 4835 e

COMMISSION OF THE EUROPEAN COMMUNITIES

**A TIMECODER FOR NEUTRON
TIME-OF-FLIGHT EXPERIMENTS**

by

S. DE JONGE

1972



**Joint Nuclear Research Centre
Geel Establishment - Belgium
Central Bureau for Nuclear Measurements-CBNM**

ABSTRACT

The described timecoder is designed for neutron time-of-flight experiments at the linear accelerator of the CBNM at Geel, Belgium.

By the use of MECL II integrated circuits it features simple design and low cost. Basic channelwidth is 40 ns, which can be multiplied in 8 succeeding regions with a factor of 1 to 99, which may be different for each region. In regions where no events have to be stored, address counting is inhibited which results in optimal use of the 4096 output channels (12 bits).

The deadtime of the coder together with a buffer memory is 280 ns, permitting several events to be registered during one measurement cycle.

KEYWORDS

TIME OF FLIGHT METHOD
LINEAR ACCELERATORS
DEAD TIME
MULTI-CHANNEL ANALYZERS
INTEGRATED CIRCUITS
TIME ANALYZERS
MEMORY DEVICES

CONTENTS *)

	<u>Page</u>
1. Design considerations	5
2. Realised specifications	5
3. Simplified logic diagram	6
4. Circuit description	8
4.1. Clock oscillator	8
4.2. CW counter	8
4.3. ZL counter	9
4.4. Address and phasing 1	9
4.5. Address and phasing 2	11
5. Conclusions	11

*) Manuscript received on April 5, 1972

A TIMECODER FOR NEUTRON TIME-OF-FLIGHT EXPERIMENTS

1. DESIGN CONSIDERATIONS

In order to make efficient use of memory storage in neutron time-of-flight experiments the channelwidth is increased when flight time increases, keeping the neutron energy resolution about constant. Neutron energies of several MeV's down to 0.025 eV corresponding to flight times of 0.5 μ s up to 45 ms on a 100 meter flight path, have to be analysed and stored in a 12 bit (4096 channels) memory.

To meet the above mentioned requirements the timecoder should have 8 zones within one measurement cycle, where it should be possible to multiply the basic channelwidth with a factor of 1 to 99. One or more of these zones could be zones without interesting events, where storage has to be inhibited (Fig. 1 and 2). The minimum channelwidth determines the resolution and as special equipment is available for higher resolution measurements 40 ns is to be considered as sufficient at the CBNM Linac.

Precision and stability of this basic channelwidth have to be better than 10^{-5} a figure being determined by the timing uncertainty at the neutron source. A normal quartz crystal in the clock oscillator meets these requirements.

Differential linearity of the coder should be better than 1%. This implies that the channels should be of equal width. Careful lay-out and decoupling of the phasing circuits for the T_o - and T_n -signals will keep the threshold of these circuits constant and no timing errors will occur.

As several operations such as opening and closing of measurement zones, readout of address scaler etc., have to be performed within one clock period fast switching elements should be used. MECL II circuits with a propagation delay of 2 - 9 ns will be suitable.

2. REALISED SPECIFICATIONS

Channelwidth:	40 ns
Precision:	$5 \cdot 10^{-6}$
Stability:	$1 \cdot 10^{-6}$
Differential linearity:	0.5%
Number of zones:	8
Minimum zone length:	400 ns
Deadtime:	280 ns
Maximum range:	320 ms
Output:	12 bits and 4 routing bits.

3. SIMPLIFIED LOGIC DIAGRAM (Fig. 3)

Under normal working conditions there are 2 inputs; a T_0 -signal which starts the timecoder program and a T_n -signal being the event of which the time $T_n - T_0$ has to be coded. A third input (Pretrigger) can eventually be used as a safety reset.

At the arrival of the pretrigger, reset OS 1 is fired resetting the following circuits: T_0 FF, zone scaler, CW counter, ZL counter and address scaler. It should be noticed that the zone scaler is reset to position 111, which is decoded and the first group of digitswitches is selected by the level adapter.

A group of digitswitches consists of:

1. A sign switch, which indicates whether events should be recorded (+ = \overline{ZD}) or not (- = ZD) in the concerning zone.
2. Two decades indicating the channelwidth multiplication factor.
3. Four decades indicating the zone length in number of channels.

The reset pulse passing through OR gate 1 transfers ZD or \overline{ZD} into the ZDFF and the channelwidth multiplication factor into the CW register.

After the reset pulse has occurred a pulse is generated by the circuit called "Shaping" and through OR gate 2 the zone length is transferred into the zone length counter by AND gate 3. Also a clock pulse is fed to the zone scaler, causing its position change to 000 and the second group of digitswitches is selected.

At the same time the channelwidth from the channelwidth register is transferred into the channelwidth counter by AND gate 5. When T_0 arrives the flip-flop T_0 FF is set. Next the output of T_0 FF is brought in phase with the clock in such a way, that the clock gates 6 and 7 are opened just inbetween two clock pulses. This phasing is done in T_0 FFTD, which is a tunnel diode flip-flop. A MECL II flip-flop, giving a turn-on delay up to 30 ns for small overlap between set and clock pulse, cannot be used for this purpose, as the triggerdelay should be less than half a clock period (20 ns).

The CW counter, a BCD downcounter, is driven now by clock pulses and every time the counter arrives at position 00 one clock pulse is fed through overflow gate 8. This overflow performs the three following functions:

1. The channelwidth multiplication factor which is still in the CW register is transferred again in the CW counter.
2. The address scaler is driven with clock pulses by gate 9, when events should be recorded in the first zone.
3. The ZL counter is driven by clock gate 6.

The ZL counter is a 4 decade BCD downcounter. When this counter reaches position 0000, an overflow is generated, which transfers through gate 2 the length of zone 2 into the ZL counter. At the same time the channelwidth multiplication factor and the information "Zone Dead" or "Zone Dead" for zone 2 are transferred into the CW register and ZDFF.

The zone scaler advances to position 001 selecting digitswitch group 3.

The propagation delay in zone scaler - decoder - level adapter insures that this advance in selection does not occur too early and limits at the same time the minimum zone length to 400 ns. This process goes on until the last zone is reached, selected by the digitswitch "Number of Zones", which enables gate 11.

The next overflow of the ZL counter fires reset OS 2, which closes the transfer gate 12 and at the same time triggers reset OS 1. The program which was selected on the digitswitches is ended and the coder returns to its original state.

The three bit output of the zone scaler can be used as routing inputs for the address register, so that every coded event is accompanied by the number of the zone in which the event occurred.

The events of which the flight time have to be measured ($T_n - T_o$) enter through gate 13, which is normally open.

The T_n flip-flop is set by the leading edge of this signal and further phased with the clock in such a way, that the transfer gate 12 opens inbetween two clock pulses. T_nFF and T_nFFTD are self resetting after 40 ns.

If the event falls in a zone in which it should be registered, the transfer gate is enabled by the level Zone Dead.

The transfer flip-flop is set, which on its turn closes the transfer gate and the input gate 13 through OR gate 14.

The single output pulse of the transfer gate strobes the address register, which takes its binary coded time information from the address scaler.

The address scaler is read in flight inbetween two clock pulses. The state of the transfer flip-flop indicates that the coder is ready.

The output adapter or buffer store sequentially reads the address and generates a reset. This reset signal resets the transfer flip-flop and at the same time keeps the input gate 13 closed. The trailing edge of the reset signal at the output of gate 14 is slowed down by a capacitor. Input gate 13 opens slowly. If at this time an input signal would be present, the output rise time of gate 13 is too slow to trigger the T_n flip-flop. In this way registration of an event having false timing is prevented.

4. CIRCUIT DESCRIPTION

4.1. Clock oscillator (Fig. 4)

The clock oscillator is a 25 MHz overtone oscillator (1) constructed with 1/4 MC1010. Capacitors C_3 and C_4 are giving a certain ratio between clock-up time and clock-down time for the two outputs, assuring proper timing in the CW counter and phasing flip-flops.

4.2. CW counter (Fig. 4 and Fig. 9)

The CW counter is a programmable two decade BCD down counter (2) constructed with J-K flip-flops of the type MC1013. The dividing factor (1 to 99) can be set into the counter from the register 4E-4H. When clock gate $6D_a$ is open (T_{OFF} is true) clock pulses arrive from $6D-6$.

Overflows of the least significant digit are detected by gate $8F_a$, the output of which serves as the clock input for the preceding decade. Gate $8F_b$ detects the overflow of this decade. If an overflow occurs the clock line is inhibited and at the same time gate 8E is enabled at input 10.

Furthermore gate 8E gives an output when the least significant decade arrives at position 0001. Its clock line is inhibited and gate $6D_b$ is opened with delay, caused by R_9 and the gate input capacitance.

The next clock pulse, occurring at the time at which the contents of the whole scaler would be zero, is passing through and transfers the contents of the CW register again into the scaler. These cycles continue until clock gate $6D_a$ closes.

The first stage of the scaler (6F) has double steering, as it does not return to zero, which is the case for the other stages. When data are transferred into the scaler, spurious pulses can occur at the clock line of the second decade, caused by differences in propagation delay in the scaler stages. The clock line is decoupled with 82 pf to suppress these pulses.

The reset line, which is distributed throughout the coder, enters through a low pass filter, to improve the noise immunity.

Before a measurement cycle starts the information of the CW register is transferred into the CW counter by signal \boxed{B}

As the S and R input of the J-K flip-flop (MC1013) do not always dominate the J-K inputs, the clock lines have to be kept high during setting and resetting. When not, some decades start oscillating during this action, resulting in a faulty scaler contents.

The clock lines are kept high by the gates 6C during these actions. The CW counter has two overflow outputs. One at gate 5C-6 serving as the clock input for the ZL counter and one at gate $6D_b$ -13 serving as the input for the address scaler. The latter being gated

(wired AND) by the output of the Zone Dead flip-flop (ZDFF). The ZDFF is driven with delay from another flip-flop for proper timing. The outputs Gated Clock and \overline{ZD} are respectively used as clock input and enable input of the transfer gate. Level T_0 FF opens the clock gates at the beginning of a measurement cycle.

4.3. ZL counter (Fig. 5 and Fig. 9)

The ZL counter is a 5 decade BCD down counter and is built up in the same way as the CW counter.

The output pulse \overline{B} appearing at gate 5D-6 after the trailing edge of the reset pulse transfers through gate 5C the contents of the first group of digitswitches, indicating the zone length. The ZL counter has the following outputs:

1. FST BIN, which is the output of the first counter stage and used for monitoring as discussed later.
2. ZONE OFLO, with functions:
 - a. Transfer of the sign (ZD or \overline{ZD}) of the digitswitch into the ZD flip-flop.
 - b. Advance of the zone scaler.
 - c. Termination of the measurement cycle if the selected number of zones is reached.
3. XFER CW, appearing just before the end of a zone, which transfers the channel width of the next zone into the CW register.

Several lines on the printed circuit board are longer than 7 cm, what causes ringing after transients. To damp these oscillations the longer lines are terminated with a voltage divider of $2 \times 220 \Omega$ between supply voltage and ground.

This method gives rise to a decreased noise immunity as the gate output voltage swing decreases. In practice however no problems occurred in connection with this effect.

4.4. Address & Phasing 1 (Fig. 6)

The zone counter consists of a three stage binary counter, constructed with J-K flip-flops. Its outputs are decoded and these are amplified by 8 identical level adapters (T_1 and T_2) to levels between GND and -5V. These outputs serve as the selection level of the 8 groups of digitswitches.

As the BCD outputs of the digitswitches are diode OR-ed it is not possible to select the switches with the MECLII level, because of the diode voltage drop.

The negative start pulse for the coder (T_0) enters through level adapter T_{24} and sets flip-flop 6F.

A current $i = \frac{VEE - (V_{d1} + V_{d2})}{R_e + R_{69}} = 3.3 \text{ mA}$ is switched into

the tunnel diode. (Re is the internal emitter resistor of 6F, being 1K5). If now a clock pulse occurs, or was already present from 6E-11, a current of 3 mA is added and the tunnel diode switches to its high state.

When flip-flop 6F is reset, the tunnel diode resets at the same time because it has voltage drive for positive transitions of the preceding flip-flop. The diode D₁ adds ~ 0.75 V to the tunnel diode voltage and brings it just to MECLII levels. The width of the clock pulse is less than 20 ns, so that the time jitter on the phased signal is less than 20 ns with respect to the clock. This fact allows the clock gates of the CW counter to be opened just in between two clock pulses by the signal T₀FF.

The used phasing method which is the same for the events (T_n) causes triangular time channels with a width of 40 ns on half height. When the channel width multiplication factor is greater than 1 the time channels have a trapezoidal shape.

The output of the T_n flip-flop (T_nFF) is fed through a series of 4 inverters (6C), acting as a delay, in order to obtain the proper phase relation with the clock at gate 6D-1.

The reset signal which enters at 1B is at TTL levels and adapted to MECLII levels by T₂₃. The reset input signal at gate 6A-4 is slowed down to such an extent that the output of gate 6A-6 has a rise time of 40 ns, when an input (T_n) was present during resetting.

The drive at the set input of T_nFF is insufficient and registration of an input signal having no proper timing is prevented. If an event has to be registered the first clock pulse passes through gate 6D_a (for conditions: T_nFF.ZD.RESET.XFERFF) and sets the transfer flip-flop, which on its turn closes gate 6D_a and the input gate of T_nFF. Resistor R₄₀, together with the gate input capacitance is acting as a delay, in order to keep gate 6D_a open, long enough to have a whole clock pulse passing through. This single pulse transfers the contents of the address scaler into the output register.

The reset one shot (3) which terminates the measurement cycle consists of gate 6E_a and 6D_b. It is enabled by the level from digit switch "NO OF ZONES" (DS₉) and is fired by the zone overflow. Enabling occurs also when the concerning digit switch is in position 8 during the reset cycle of the coder. As the zone overflow is present at the trailing edge of the reset signal the gating level T₀FF is necessary to prevent firing at this time.

The address and phasing 1 circuit has three outputs for external use:

1. READY, a level which indicates that coding of an event has taken place and the output address is available.
2. ZI (zone of interest), a level which is only present during the time that events have to be accepted.
3. PR (program), a signal for monitoring on an oscilloscope, showing the timecoder program during every measurement cycle.

4.5. Address & Phasing 2 (Fig. 7)

The address scaler is a twelve bit synchronous binary counter constructed with J-K flip-flops of the type MC1013. Coupling between the groups of stages is done with clock gates of the type MC1023, keeping the propagation delay of the J-K conditions to a minimum. ($t_{pd} \text{ MC1013} + 3 \cdot t_{pd} \text{ MC1023} = 15 \text{ ns}$). The signal XFER ADDR, arriving between address scaler contents n and $n+1$ transfers the address n into the address register 5A - 3A, composed of D flip-flops. On the command READ the information appears on the output lines in DTL levels.

The address register contains 4 bits which can be used either for routing purposes (switches on external) or for indication of the zone address (switches on internal).

The reset signal for the timecoder is delivered by the one shot 1H and distributed to all counters.

The input PT (pretrigger) is an external reset input, which may serve as a safety reset, preceding every start pulse(T_0).

5. CONCLUSIONS

Partition of time-of-flight spectra in different zones with different channel width can be done in the timecoder itself. The quantity of hardware is considerably reduced, compared with systems where coding is done first in a coder and partition and channelwidth multiplication in a conditioner (4).

In high frequency logic circuitry like the here described timecoder MECLII integrated circuits have proved to be attractive building blocks. Due to the low propagation delay there are little or no timing problems encountered, what allows relatively simple and straight forward logic design.

For prints of a reasonable size (timecoder: 170 x 280 mm) double-sided printed circuits can be used, if the supply ground is connected to the integrated circuits by a stripline (see fig. 9).

Ringings on long signal lines causes a problem, which can be solved either by parallel resistors or by series resistors (5).

The first method has the disadvantage of decreased noise immunity, the second one causes a significant increase in connections on the printed circuit board.

Several timecoders of the type here described have been constructed and are operating to complete satisfaction.

REFERENCES

- (1) Motorola application note AN 417.
IC crystal controlled oscillators.
- (2) Motorola application note AN 456.
A 50 MHz programmable counter designed with MECLII
integrated circuits.
- (3) Motorola application note AN 233.
Design of monostable multivibrators using MECL
integrated circuits.
- (4) F. Colling and W. Stüber, Nucl. Instr. and Meth. 64
(1968) N° 1.
A conditioner with integrated circuits for neutron
time-of-flight experiment data selection.
- (5) Motorola application note AN 277.
Overshoot and ringing in high speed digital systems.

LIST OF FIGURES

- Fig. 1: Timecoder programming for the spectrum of Fig. 2.
- Fig. 2: Transmission spectrum of Mn+U²³⁸ (20 - 300 eV).
- Fig. 3: Timecoder simplified diagram.
- Fig. 4: CW & ZL counter 1.
- Fig. 5: CW & ZL counter 2.
- Fig. 6: Address & Phasing 1.
- Fig. 7: Address & Phasing 2.
- Fig. 8: Frontview of the timecoder.
- Fig. 9: The CW & ZL counter.

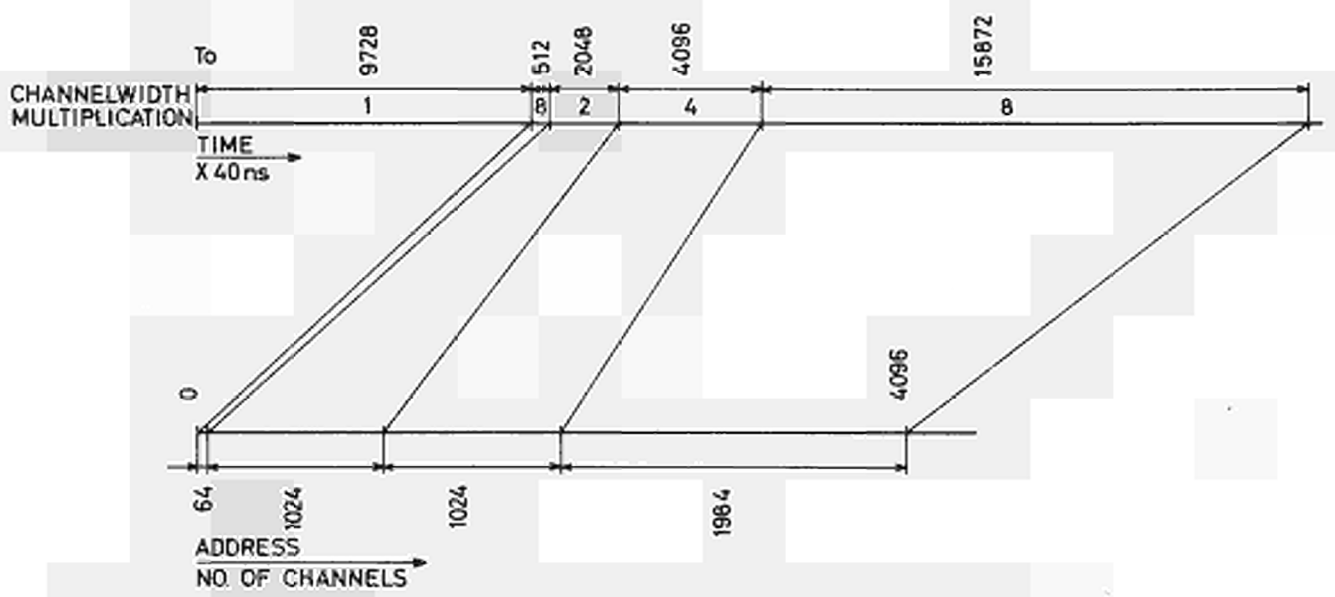


Fig.1 TIMECODER PROGRAMMATION FOR THE SPECTRUM OF FIG.2

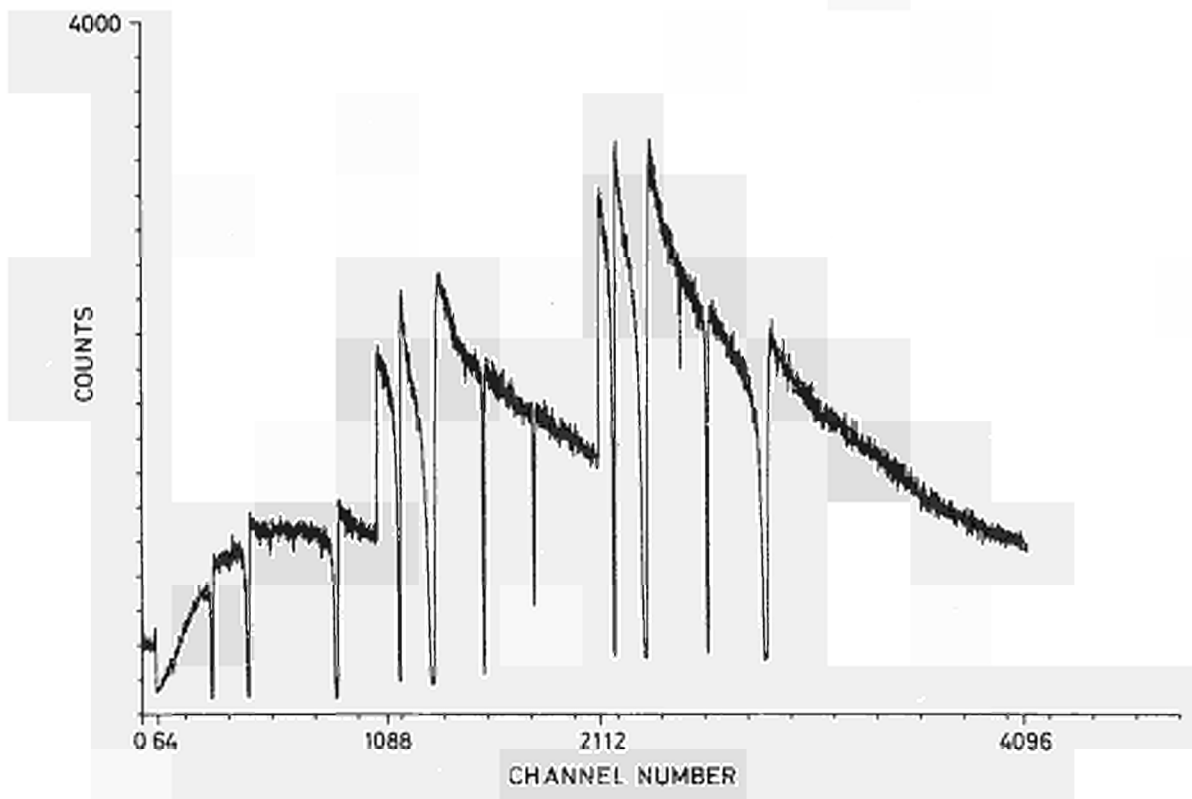


Fig.2 TRANSMISSIONSPECTRUM OF Mn + ²³⁸U (20-300 eV)

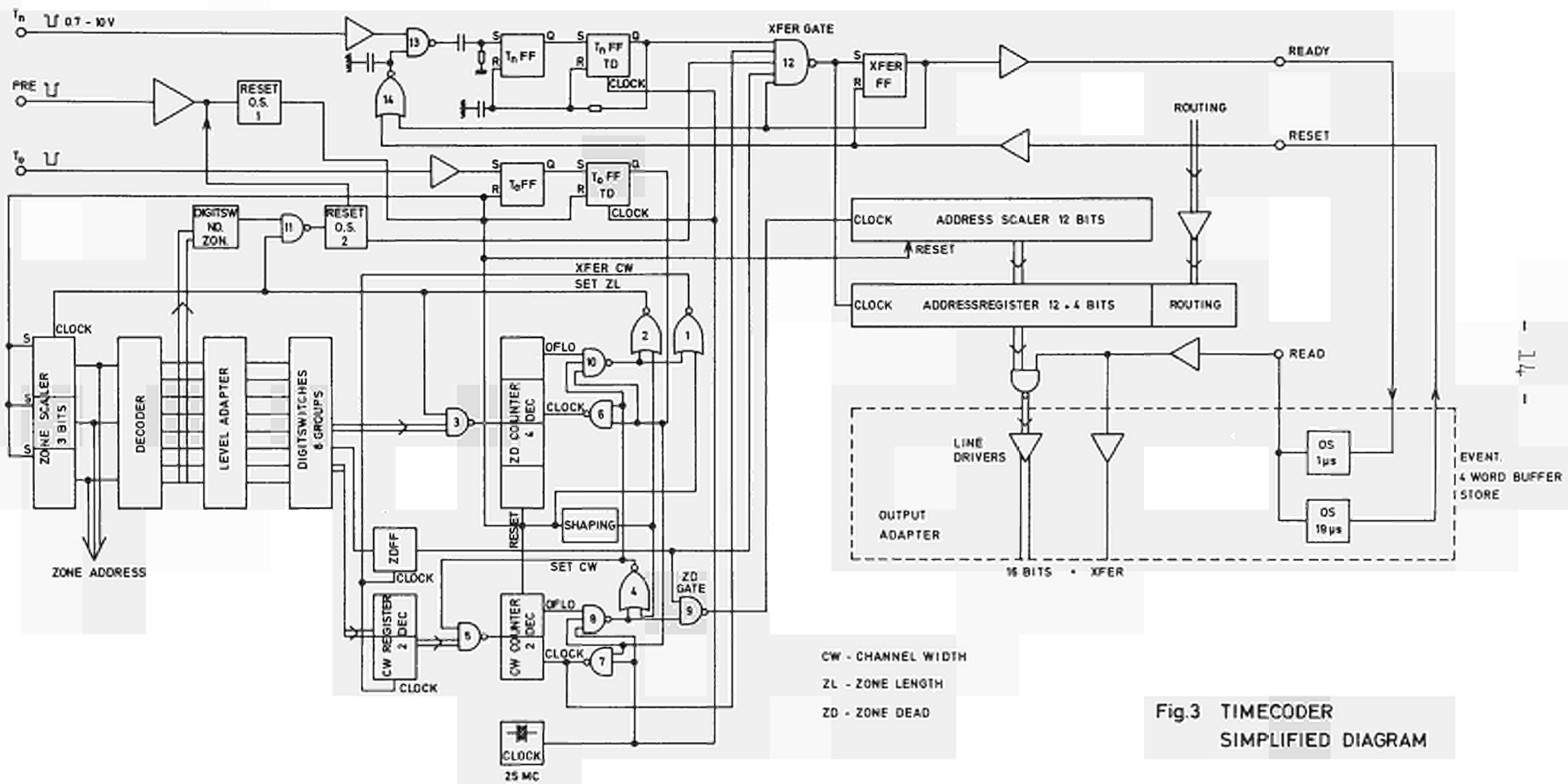


Fig.3 TIMECODER SIMPLIFIED DIAGRAM

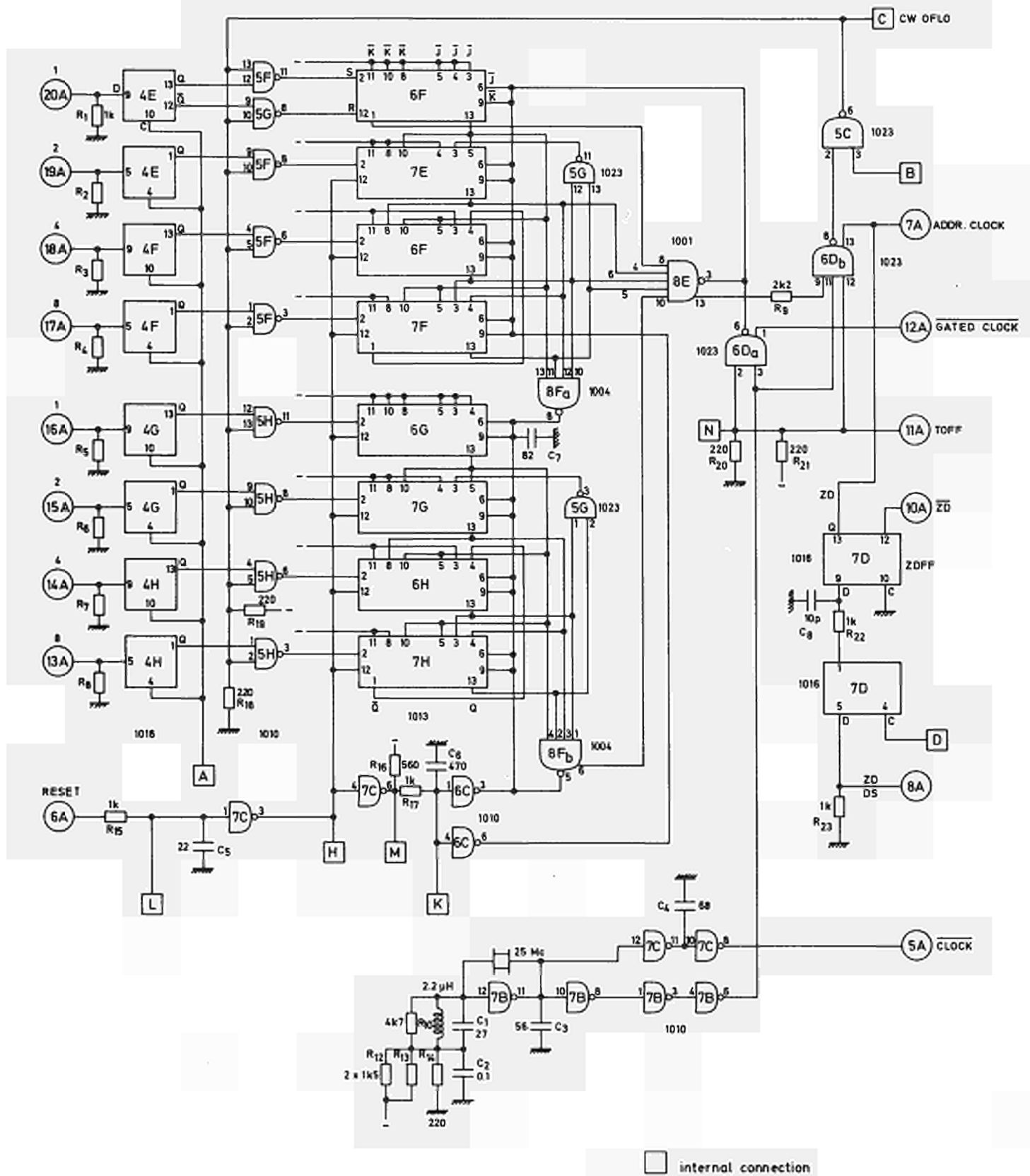
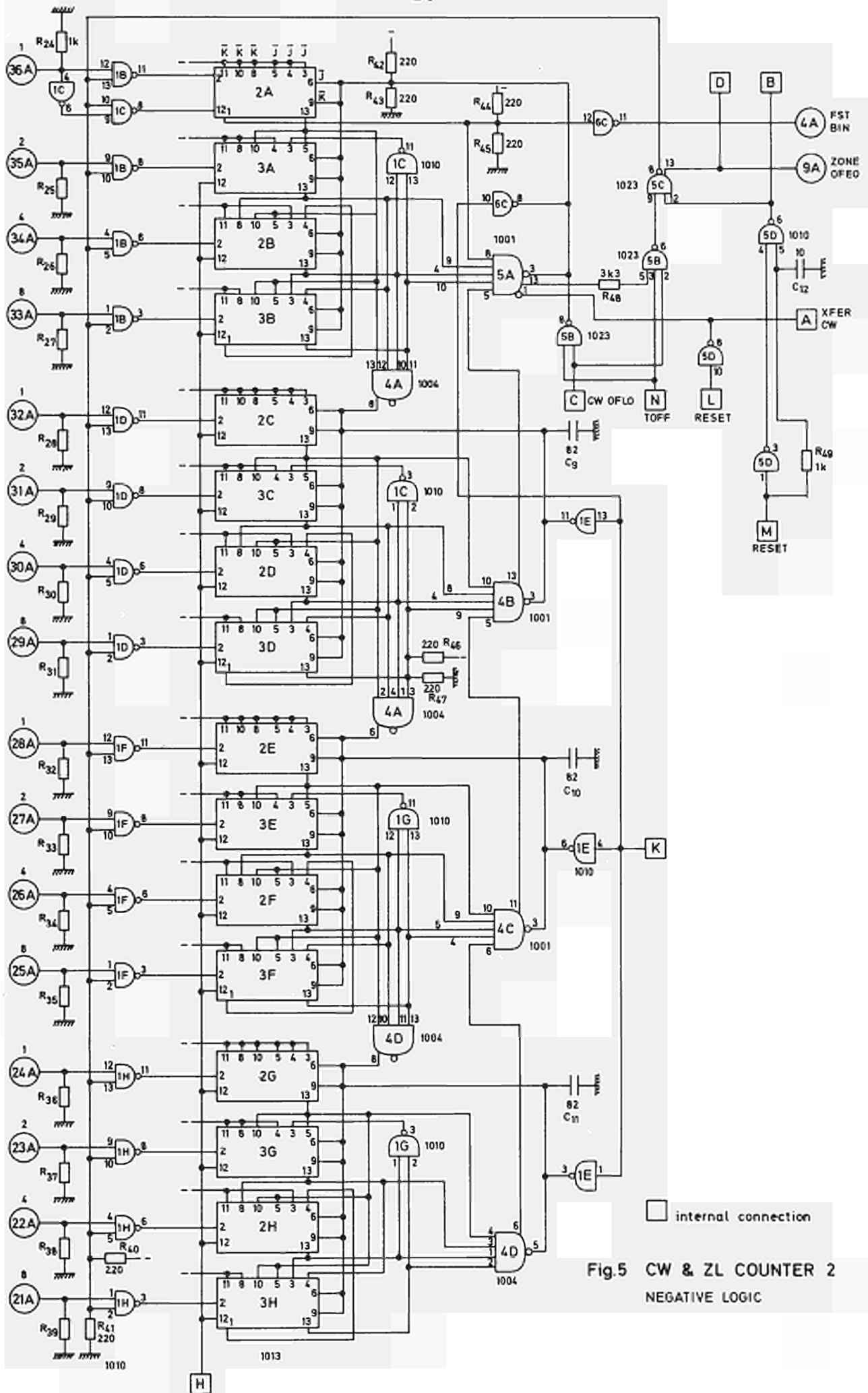


Fig.4 CW & ZL COUNTER 1
NEGATIVE LOGIC



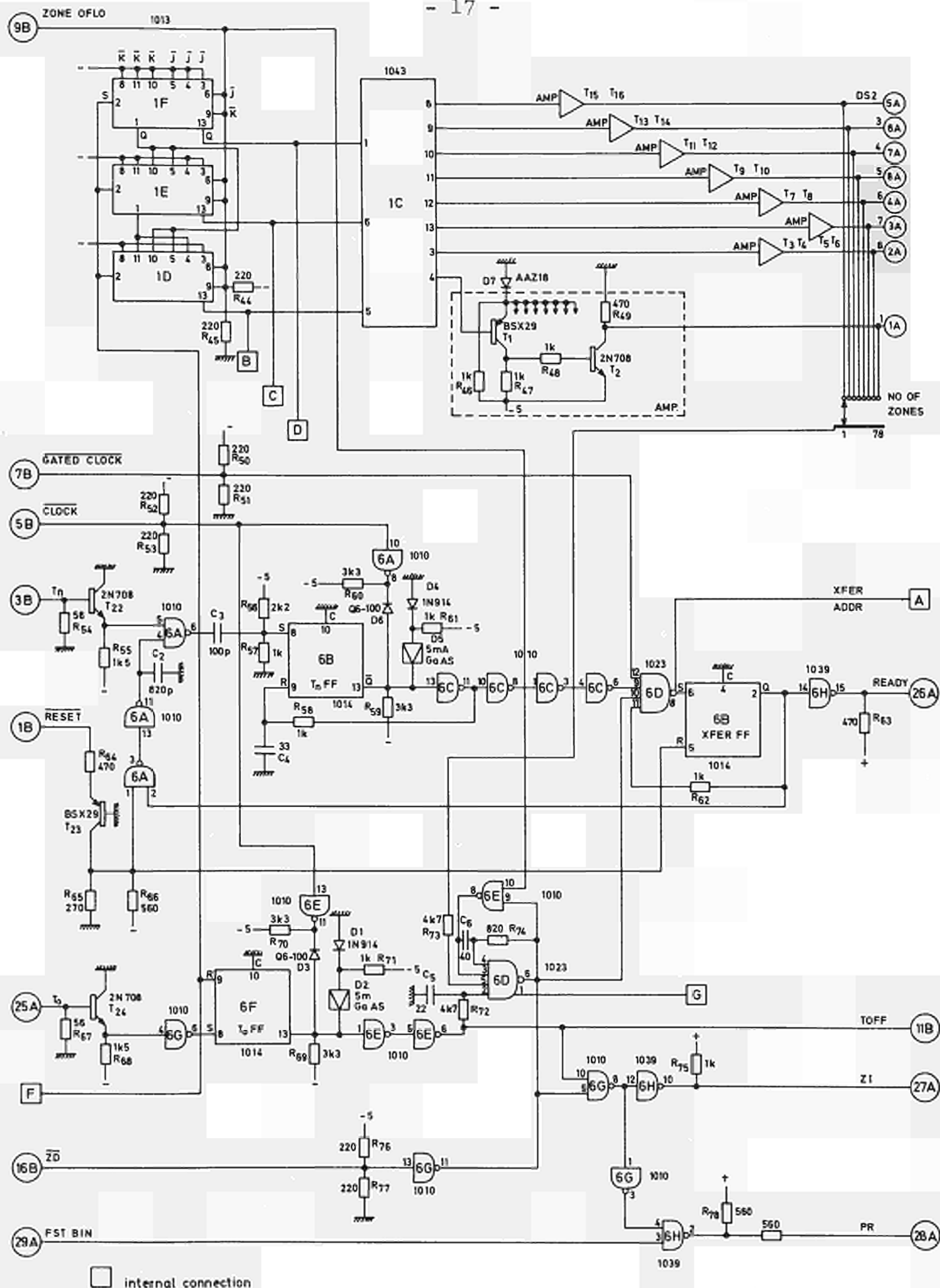
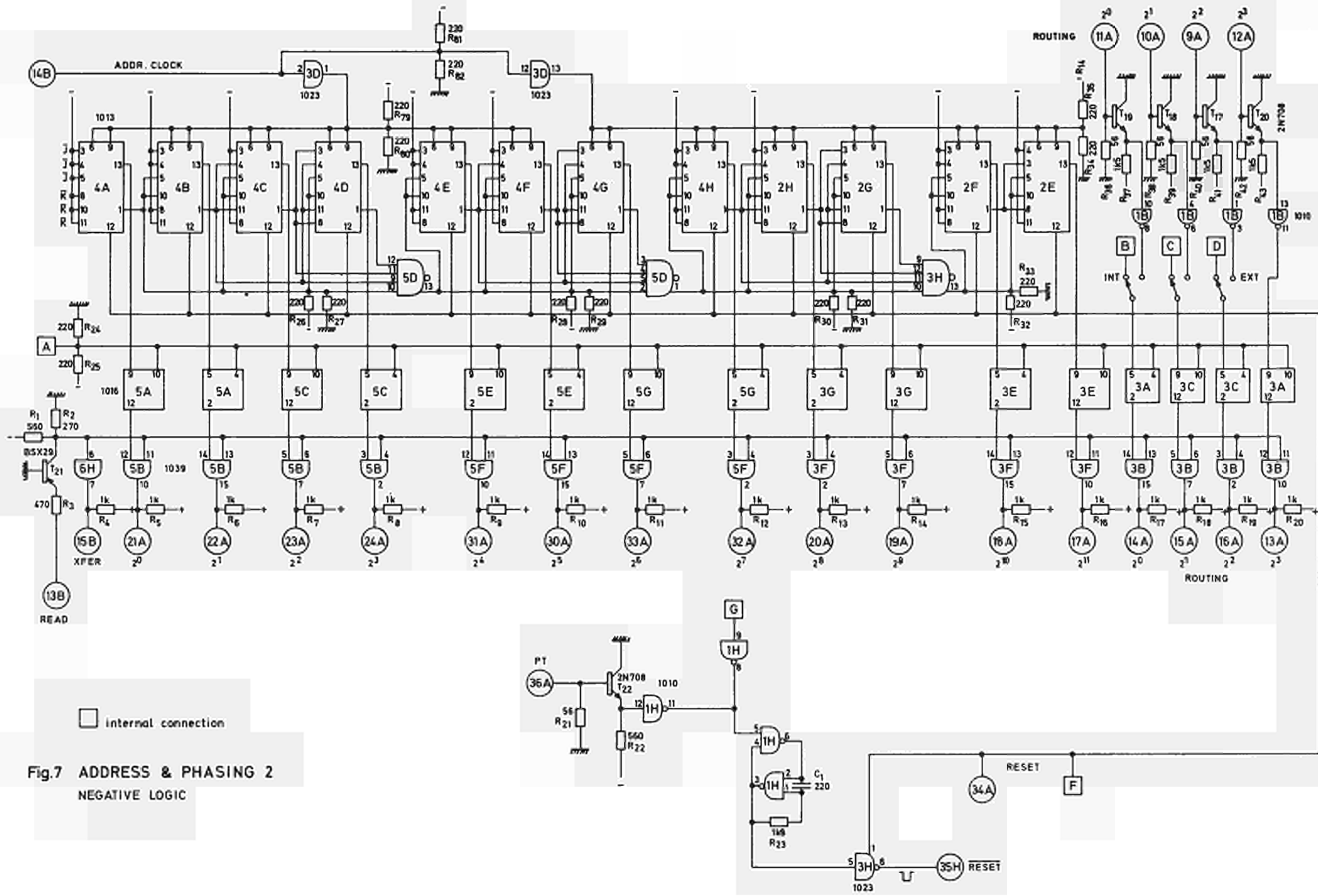


Fig.6 ADDRESS & PHASING 1
NEGATIVE LOGIC



□ internal connection

Fig.7 ADDRESS & PHASING 2
NEGATIVE LOGIC

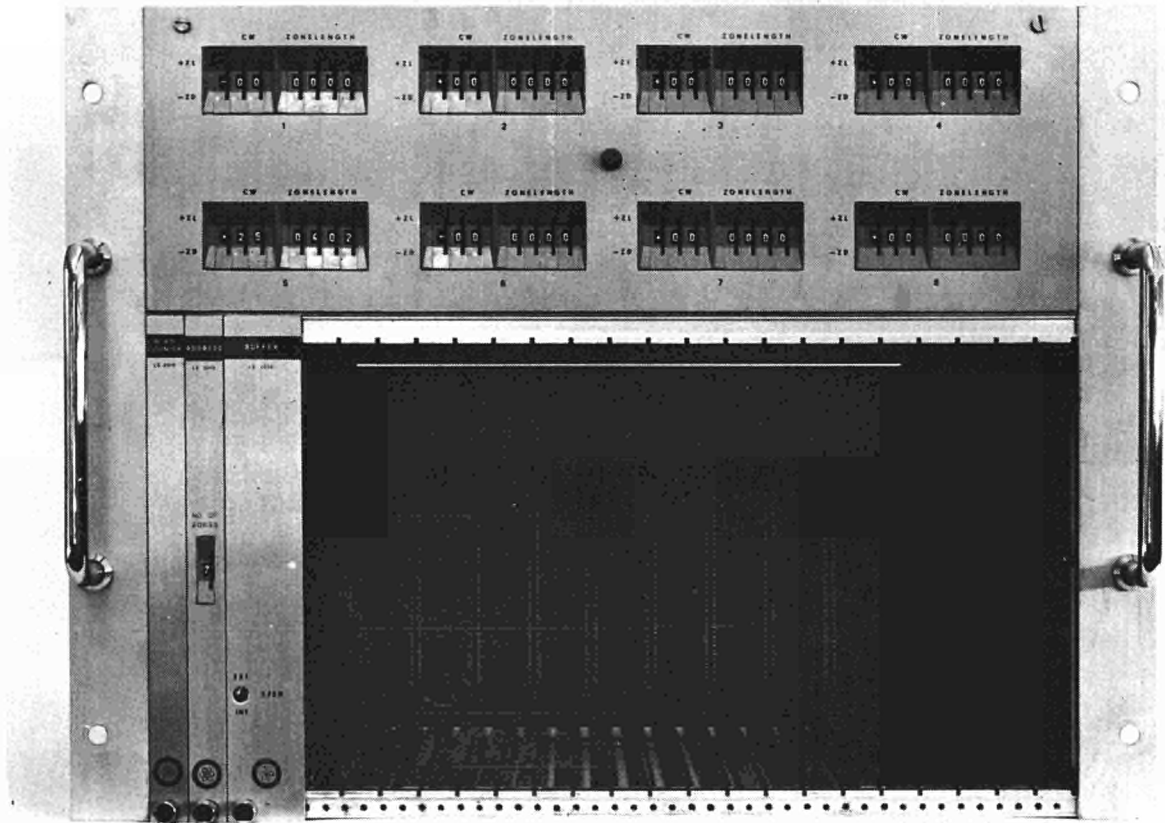


Fig. 8: Frontview of the timecoder, equipped with a 4 word buffer memory. Spare slots are available for input or output electronics.

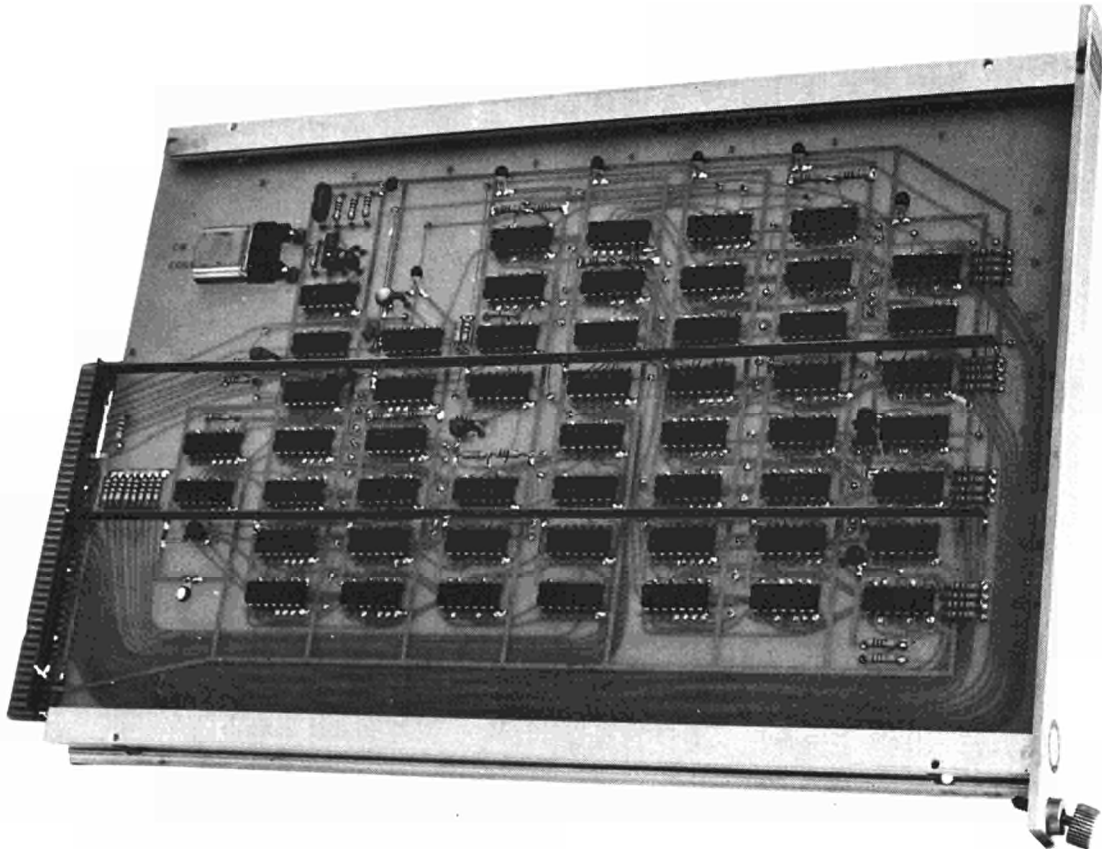
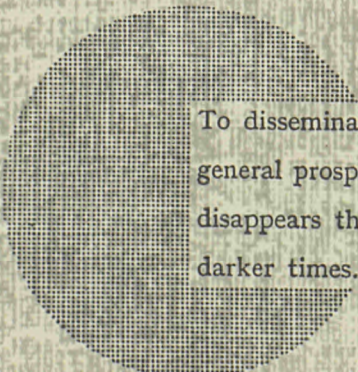


Fig.9: The CW & ZL counter.

NOTICE TO THE READER

All scientific and technical reports published by the Commission of the European Communities are announced in the monthly periodical “euro-abstracts”. For subscription (1 year: B.Fr. 1025) or free specimen copies please write to:

**Sales Office for Official Publications
of the European Communities
P.O. Box 1003
Luxembourg 1
(Grand-Duchy of Luxembourg)**



To disseminate knowledge is to disseminate prosperity — I mean general prosperity and not individual riches — and with prosperity disappears the greater part of the evil which is our heritage from darker times.

Alfred Nobel

SALES OFFICES

All reports published by the Commission of the European Communities are on sale at the offices listed below, at the prices given on the back of the front cover. When ordering, specify clearly the EUR number and the title of the report which are shown on the front cover.

OFFICE FOR OFFICIAL PUBLICATIONS OF THE EUROPEAN COMMUNITIES

P.O. Box 1003 - Luxembourg 1
(Compte chèque postal N° 191-90)

BELGIQUE — BELGIË

MONITEUR BELGE
Rue de Louvain, 40-42 - B-1000 Bruxelles
BELGISCH STAATSBLAD
Leuvenseweg 40-42 - B-1000 Brussel

LUXEMBOURG

OFFICE DES
PUBLICATIONS OFFICIELLES DES
COMMUNAUTÉS EUROPÉENNES
Case Postale 1003 - Luxembourg 1

DEUTSCHLAND

VERLAG BUNDESANZEIGER
Postfach 108 006 - D-5 Köln 1

NEDERLAND

STAATSDRUKKERIJ
en UITGEVERIJBEDRIJF
Christoffel Plantijnstraat - Den Haag

FRANCE

SERVICE DE VENTE EN FRANCE
DES PUBLICATIONS DES
COMMUNAUTÉS EUROPÉENNES
rue Desaix, 26 - F-75 Paris 15^e

ITALIA

LIBRERIA DELLO STATO
Piazza G. Verdi, 10 - I-00198 Roma

UNITED KINGDOM

H. M. STATIONERY OFFICE
P.O. Box 569 - London S.E.1

Commission of the
European Communities
D.G. XIII - C.I.D.
29, rue Aldringen
L u x e m b o u r g

CDNA04835ENC