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A NANOSECOND TIME CODER WITH GREAT ANALYSIS RANGE FOR TIME-OF-FLIGHT EXPERIMENTS

by

P. KLOPF, H. MEYER, W. STÜBER, H. VERELST

1963



Joint Nuclear Research Center Geel Establishment - Belgium

Central Bureau for Nuclear Measurements (CBNM)

Text presented at the "Colloque International sur l'Electronique Nucléaire", Paris (France) - November 25-27, 1963

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smallest channel width, $\triangle t$ min of one nanosecond; maximum possible channel number for a time accuracy of one channel, greater 2¹³ channels; a regulation system was developed to increase this value up to about 2th. An overall differential accuracy of \pm 0.15 nanosecond was reached for input pulses with a risetime up to 20 nanoseconds and a dynamic range of 10 max. The development results show the possibility of decreasing the smallest channel width down to 0.25 nanosecond for reliable function.

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smallest channel width, $\triangle t$ min of one nanosecond; maximum possible channel number for a time accuracy of one channel, greater 2^{13} channels; a regulation system was developed to increase this value up to about 2^{18} . An overall differential accuracy of \pm 0.15 nanosecond was reached for input pulses with a risetime up to 20 nanoseconds and a dynamic range of 10 max. The development results show the possibility of decreasing the smallest channel width down to 0.25 nanosecond for reliable function.

The planned ,,multiple storage per analysis cycle,, and a prebuffer store under development will probably allow a storage time down to 128 nanoseconds for an event to be analysed.

The unit is a combination of a chronotron type system with the classical Argonne system. Active elements used are tunnel diodes and transistors. Layout of equipment will be described and discussed.

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A NANOSECOND TIME CODER WITH GREAT ANALYSIS RANGE FOR TIME-OF-FLIGHT EXPERIMENTS

SUMMARY

A first version of a nanosecond time coder for "on line" and "off-line" time-of-flight analysis was built with the following main characteristics :

smallest channel width, $\triangle t$ min of one nanosecond; maximum possible channel number for a time accuracy of one channel, greater 2¹³ channels; a regulation system was developed to increase this value up to about 2¹⁸. An overall differential accuracy of ± 0.15 nanosecond was reached for input pulses with a risetime up to 20 nanoseconds and a dynamic range of 10 max. The development results show the possibility of decreasing the smallest channel width down to 0.25 nanosecond for reliable function.

The planned "multiple storage per analysis cycle" and a prebuffer store under development will probably allow a storage time down to 128 nanoseconds for an event to be analysed.

The unit is a combination of a chronotron type system with the classical Argonne system. Active elements used are tunnel diodes and transistors. Lay-out of equipment will be described and discussed.

INTRODUCTION

The aim of our work was to realize a time coder for flight time analysis with a best time resolution, i.e. smallest channel width of one nanosecond, an analysis range of more than ten thousand channels and high stability for long time running experiments, especially for the measurement of neutron energy spectra. Such a unit can be helpful, especially, for future work in high resolution time-of-flight analysis, with pulsed sources of sufficiently small burst width and where burst rate, intensity of neutrons and suitable energy threshold values will allow flight paths long enough to have a great dynamic range, also for acceptable measuring times.

The system realized can be used for the experimental program of the BCMN of Euratom with its pulsed neutron sources. For this program several main instrumentation systems are planned or developed, as for instance 4096-channel on-line analysis systems, including time coders with 10 nanosecond smallest channel width which are realized by developmental contracts with two industrial firms. Another system, especially for complex off-line analysis of flight times in a wide range and/or multiparameter spectra is under development in our laboratories. The developed time coder shall be used together with this handling system, but also directly with memory computer systems of 256 to 4,096 channels.

For a time coder with the mentioned characteristics, a direct application of chronotron or vernier chronotron systems (1) is not practical and very probably not to realize because of the great analysis range needed. Time expanding technics are not suitable because of insufficient stability and accuracy for long time running experiments and great analysis ranges. (Examples for such technics are : a) introducing a charge to a capacity for the time distance to be measured and extracting this charge afterwards with a slow pulse train or lower discharge current (2); b) the measurement of the phase difference of two sine waves generated by two oscillators, one started at the beginning and another at the end of a time distance having a small difference in frequency, the phase of which is measured after mixing (3).) The same arguments are valid for time to amplitude conversion principles. For accurate time measurements also sampling technics as used in sampling oscilloscopes were proposed (4), but the long term accuracy will be insufficient and an easy analysis of wide range spectra too complicated.

For the characteristics needed, a system with direct time to digital conversion was necessary; the earliest type of such a system was practically the well-known Argonne analyser developed by Shumann and others (5). The last version of such a system with 10 nanosecond resolution are the units made for us by developmental contracts as mentioned before.

FUNCTION AND LAY-OUT

To have a channel width of one nanosecond and a great analysis range, in principle a combination of the chronotron type with the classical Argonne system was chosen.

Let me first explain the general function (see Fig. 1) :

The unit will be started by a reference output of the neutron generator, as for instance a pulse from a master clock or a pulse detected from the primary particle burst or from the γ -flash. Such a pulse will go through an input circuitry and trigger on a cable oscillator with a frequency of 125 Mc/s, i.e. after start, this oscillator delivers pulses with a time distance of 8 m μ sec. The oscillator pulses run through a line to which eight coincidence stages are coupled by cable transformers at a time distance of 1 ns, and after passing a gate, they are counted in a binary address scaler consisting of three tunnel diodes per stage. This scaler is at the start in a presetted condition and will deliver an output pulse when all stages are brought to the "zero" state. The number of pulses necessary to reach this condition is dependent on the adjustable state of the "zero time delay switches", which have delivered before "start" during the "reset" function pulses of suitable polarity to the binary stages.

The time between "start" and the first output pulse from the scaler is called "zero time trigger delay". This output pulse opens a gate at the "stop" input and allows now that particles to be analysed and converted in a suitable detector can initiate the "stop" function for analysis of their flight time. Such a stop pulse will go through an input circuitry with adjustable threshold and peak detection mode for amplitude independent time definition to the second inputs of the eight coincidence stages, to the scaler gate interrupting the flow of oscillator pulses to the scaler and also to the triggered oscillator for stopping this unit. In addition "readout" of information is started after a delay great enough to "set" the address. The coincidence width of the coincidence stages is $1,5 \text{ m}\mu/\text{sec}$, i.e. they are overlapped by 50 %, which assures that always one, sometimes two, but never three stages are activated. The outputs of the coincidence stages are bistable tunnel diode circuits which are connected to a diode matrix and the number of the coincidence stages are activated, the second one in time will be immediately reset by the first one. Obviously the coincidence units together with the coding matrix perform like the first 3 binaries of a 1,000 Mc/s scaler.

The state of the address scaler, determined by the number of pulses counted in this unit after opening the "stop" input, will appear through dc-coupled stages at the output in binary coded form, i.e. for a ten stage binary scaler, the state of thirteen binaries determine the analysis time. By a channel width switch for the moment eight of them are selected for readout to a buffer memory or memory register.

When "read-out" initiated by the "stop" function is finished, the storage device will start the "reset" function by which the address scaler with the "zero time delay switch" unit, the coincidence stages and all gates with bistable function are reset.

The channel width selector selects not only the channel width, but also the analysis time range. If no event arrives during analysis time, the last binary of interest will initiate directly the "reset" function ("address overflow") and no read-out can occur.

The blocks in Fig. 1 shown with dashed lines are for improvement and extension of the coder. There is first the regulation system to reach a better long term frequency stability of the cable oscillator, which has at the moment a stability of 10^{-4} in a limited temperature range. This will be good enough for the momentary conditions — 2^{13} mµsecs max. zero trigger delay and 2^{12} mµsecs analysis region that means a maximum analysis range of about 12,000 channels for the smallest channel width of one nanosecond. For the planned extension of the analysis range by a factor of 32 (i.e. 5 additional stages for the address scaler), the stability has to be improved.

The regulation system we have developed for this purpose is relatively simple. It interrupts the analysis function each second and compares for about four milliseconds the frequencies of the cable oscillator and a crystal stabilised unit. A regulation current proportional to the deviation from a mean value of difference frequency and held until the next regulation cycle begins, will correct and stabilize the frequency of the cable oscillator. The interruption of the analysis function will be done always when an analysis cycle is finished in order to avoid malfunction and complex circuitry. With the regulation system the accuracy can be about 10^{-5} .

The coder described so far can measure one event per analysis only. For a maximum analysis region of more than 100 μ secs it becomes probable that more than one event will arrive during one analysis cycle for analysis and should be measured. This is possible by switching over the flow of oscillator pulses through the scaler gate from the address scaler to a deadtime scaler instead of closing the gate and stopping the oscillator. When the deadtime scaler delivers an output pulse, i.e. will overflow, settling of the address scaler and readout must be finished and this output pulse will correct the address scaler, reset the coincidence output stages, open again the stop gate and switch back the scaler gate. The deadtime for the analysis of one event will probably be 27 m μ secs, but surely not higher than 28 m μ secs.

In Fig. 2 you see a more detailed block diagram of the realized coder to explain in more detail circuitry and functions responsible for the realized characteristics and the limiting factors.

The accuracy is mainly limited by the stability of the cable oscillator (integral accuracy) and the influence of delay jitters in the circuitry (differential accuracy) (*) which were kept low by the predominant use of fast tunnel diodes. Both inputs of the coder have adjustable amplifiers and thresholds to avoid the influence of background. At the stop input, the events of which the arrival time is to the analysed will have a certain dynamic range of pulse amplitude; therefore a limiter and peak sensitive circuitry is foreseen to avoid the influence of excessive time jitter. As known, this jitter can be a multiple of the rise time of pulses, if their amplitudes are only by a small amount greater than a chosen threshold value.

With the realised input circuitry, the jitter from input pulse shape will be smaller $\pm 0.1 \text{ m}\mu\text{sec}$ for rise times smaller than 20 m μsecs and an amplitude range of ten. If the reference pulses are not fast enough or of constant amplitude, the start input will also need a peak sensitive

(*) The differential accuracy given in the text contains three main influences : first, the statistical fluctuations of channel width;

second, channel width fluctuations and shifts because of input conditions (shape and dynamic range of those pulses which determine beginning and end of a time interval to be analysed) and because of the stability of the responsible parts of the measuring equipment;

third, channel width differences because of calibration errors.

The first influence becomes negligible for high numbers of counts per channel.

circuitry. The differential accuracy is determined besides the input circuitry by the switching accuracy of the other elements in the start- and stop path, i.e. the start flip-flop (FF₁) and the oscillator (IO) in the start path and the amplifiers, shapers and the stop gate (G₁) in the stop path. In addition, there is the influence of the coincidence stages. Altogether the jitter is not greater than about \pm 0.15 mµsec.

For correct functioning the propagation delay of pulses from both inputs to the first coincidence stage must normally be equal. In our case the delay in the stop input is made 64 musecs longer, and this for the following reason : At the end of the zero time trigger delay, i.e. when an oscillator pulse switches all binary stages back from the "one" to the "zero" state, the binary scaler delivers an output signal for opening the "stop" gate. But because of the propagation delay of the scaler (1.6 musecs/stage) and the logic circuitry on the way to the "stop" gate, some analysis pulses will be counted in the scaler before the gate can be opened. Therefore the scaler must be reset and the system has to start counting the analysis time at the moment the first possible stop pulse after opening of the stop gate can arrive at the first coincidence stage. The reset of the scaler is done by gating off the first pulse from the 3rd to the 4th binary which appears after the end of the zero time trigger delay. This means a reset of 64 m μ secs in the scaler. As gate pulse the suitably delayed scaler output pulse is taken. Because of a possible propagation delay jitter of the oscillator pulse on its way through the system which opens finally the "stop" gate, this gate must be opened a little later than is necessary to analyse in channel "l" in order to avoid a possible malfunction which could occur if the stop gate would be opened a little too early and a "stop" pulse would be there at that moment. Then the scaler would have been stopped before the 64 m μ /sec reset was finished. The mentioned necessary precaution because of jitter influences will only introduce wrong analysis in the first one or two channels of smallest width.

Another possible malfunction — in this case an analysis error of eight channels — can occur if under the worst conditions a coincidence will appear in stage C7 and the scaler gate has not been closed early enough to avoid counting of the oscillator pulse belonging to this coincidence or if a coincidence will appear in C0 and the scaler gate is closed before the preceding oscillator pulse has been counted. Such a malfunction is completely avoided by closing the scaler gate with the stop pulse only for a coincidence in C0 to C3 and introducing the gate function for a coincidence in C4 to C7 by the output pulses of the coincidence stages themselves and in addition by right adjustment of delays as further explained in Fig. 3.

If during the chosen analysis time no analysis will happen, i.e. the address will "overflow", a pulse from the last address binary of interest will activate the "reset" function through gate G4, which is only possible at the end of the analysis time, because G4 has to be preset by FF3 which is activated by the pulse opening of the stop gate at the beginning of analysis. For the future system with the possibility of multiple storage per analysis cycle, the "address overflow" function will always initiate "reset".

OUTPUT CONNECTIONS

As mentioned before, storage devices are connected to the output stages of the coder through a channel width selector which selects the binary stages of interest for read-out.

Storage is initiated by a "start-of-storage" pulse from the coder (FF4) and its reset function by an "end-of-storage" pulse from the storage device.

For the moment a developed buffer store with 10 words of 20 bits for off-line analysis and existing core memory systems with up to 4,096 channels can be connected to the coder. A fast prebuffer with 3 words of 20 bits is in preparation. Because the address bistables are d c coupled to the coder output, practically a buffer of one word is included.

CHARACTERISTICS

In Fig. 4 you find the characteristics realised and in brackets the planned extensions mentioned earlier.

In Fig. 5 the frequency variation of the cable oscillator vs. temperature is given. It should be mentioned that because of special lay-out no duty cycle effects after the start of the oscillator will influence the accuracy of analysis.

Fig. 6 shows the stability of propagation delay for the input unit with amplitude independent time definition for various input pulse conditions. An influence of ambient temperature on characteristics was not measurable between 20° C and 35° C.

More details about the cable oscillator, the address scaler, which could count pulse rates up to 300 Mc/s and the input system with amplitude independent time definition will be published in the near future.

In Fig. 7 measurements are shown to demonstrate the differential accuracy and also the internal jitter influences at temperatures between 20° C and 30° C. For testing the integral accuracy, time distances of several microseconds were measured with one nanosecond resolution using shaped pulses from a crystal controlled oscillator.

Figs. 8, 9 and 10 will give an idea of the technology used for the equipment.

POSSIBLE IMPROVEMENTS

Besides the planned extensions mentioned, i.e. increasing the maximum analysis time by a factor of 32 and the integral accuracy up to a value better than 10^{-5} and also the introduction of multiple storage per analysis cycle, other improvements are not planned for the moment, but remain possible.

With the results shown, there exists the possibility of reducing minimum channel width. A factor of two to four can probably be realized, if adjustments are carefully made and jitter effects are reduced, as for instance by compensating the temperature dependence of the thresholds in the coincidence circuits. For a reduction of the minimum channel width by a factor of four, the number of coincidence stages should be increased by a factor of two and a second pulse train available from the cable oscillator occurring one half period later than the first train will be used. Then the address scaler must count a pulse rate of 250 Mc/s.

Such improved configurations are possibly practical for certain applications, as for instance the precise determination of an electron emission up to 2 μ secs after the arrival of a μ meson as mentioned by Pizer (4) (Determination of the "Muon gyromagnetic ratio").

An improvement of integral accuracy from 10^{-5} for the moment in mind with the mentioned regulation system up to about 10^{-6} seems to be possible with a more elaborated regulation circuitry.

RESUMING REMARKS

In resuming the results of our developmental works and studies for fast time coders with great analysis range, one can say that in comparison with equipment realized earlier, the smallest channel width (i.e. energy resolution) for such systems was improved by a factor of ten and can be improved further by a factor of two to four.

In addition, especially advantageous for use with accelerators of high particle density per burst, the necessary time for the analysis of one event will be about 0,1 to 0,2 μ sec.

In order to fully use the advantages of the realized system for neutron time-of-flight analysis improvement of accelerators will be necessary.

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Fig. 2 - NANOSECOND TIME CODER

More detailed block diagram of the first version of the time coder realized



Fig. 3 — Time conditions at the scaler gate for the stop function [Gate closure by a pulse from the stop input (sto) and/or a pulse from a coincidence unit (C_n)].

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Fig. 4 — CHARACTERISTICS OF NANOSECOND TIME CODER

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Analysis time	$1.5 \cdot 2^{13} \text{ m}\mu\text{sec} = 12.288 \ \mu\text{sec} \text{ max.} \ [\times 32].$
Zero time trigger delay	2^{13} mµsec = 8.192 µsec max. [×32] adjustable in steps of 8 mµsec; 8 mµsec. min.
Analysis range	$4,096/_{channel width}$ channels [$\times 32$].
Channel width	: 1, 2, 4, 8, 16 mµsec.
Accuracy	: better (10 ⁻⁴ × Analysis time) + 0.5 mµsec in the temperature range 20° C - 30° C.
	$[10^{-5} \times \text{Analysis time} + 0.5 \text{ m}\mu\text{sec}].$
Number of events, which can be stored per	
analysis cycle	: one,
	[More than one; minimum necessary time for the storage of one event $< 0.2 \mu$ sec it a prebuffer storage is used].



Fig. 5 - Frequency of the unregulated cable oscillator vs. temperature





a) Definitions for the identification of differential accuracy :

 $d_{ik} t_{ik}$ = accuracy of channel width vs. channel number

 $t_1 =$ accuracy of channel location vs. channel number

f(cal) = calibration accuracy; f(T) = accuracy vs. temperature

 t_{sl} = slope of channel borders (10 $\frac{0}{\sqrt{0}}$ to 90 $\frac{0}{\sqrt{0}}$ of max. relative intensity)

Reached values :

 $f_w(\text{cal})$, $f_l(\text{cal})$ at 20° C $\leq 0,1$ mµsec $t_{sl} = 0.25 \pm 0.05$ mµsec (temperature influence 20° C - 30° C included) $f_t_w(\text{T})$, $f_t(\text{T})$ for a temperature change from 20° C to 30° C ; see figure



b) The measurement of $\triangle t_{w}$, $\triangle t_{l}$ and t_{sl} by taking the oscillator pulse, which opens the'' stop'' gate also as stop pulse, will show the accuracy of ring propagation delay. The changes of $\triangle t_{w}$, $\triangle t_{l}$, t_{sl} in comparison with *a*) are smaller 0.1 mµsec.

Fig. 7 — Differential accuracy of time analysis (a); Accuracy of "ring" propagation delay (b) [tring is the delay of the opening pulse for the stop gate on the way Co-U₂ -B₃ -B₁₂ -FF₃ -FF₂ -G₁ -A₅ -Co]



Fig. 8 — Time coder, first version (provisional)



Fig. 9 — Cable oscillator with start and stop gates



Fig. 10 — 10-bit binary address scaler with tunneldiodes

