

Automatika



Journal for Control, Measurement, Electronics, Computing and Communications

ISSN: 0005-1144 (Print) 1848-3380 (Online) Journal homepage: http://www.tandfonline.com/loi/taut20

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To cite this article: Jean Marie Vianney Bikorimana, Mohannad Jabbar Mnati & Alex Van den Bossche (2017) Frequency synchronization of a single-phase grid-connected DC/AC inverter using a double integration method, Automatika, 58:2, 141-146

To link to this article: http://dx.doi.org/10.1080/00051144.2017.1372122



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Published online: 26 Sep 2017.



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Frequency synchronization of a single-phase grid-connected DC/AC inverter using a double integration method

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ABSTRACT

Many traditional grids have started to integrate the DC/AC inverters in their networks. This requires a good control to enhance the power quality. The grid frequency behaviour is one of the principal indicators that reveal the power quality. Therefore, it must be strongly controlled. Up to now, the most popular frequency synchronization method is based on phase-locked loop (PLL) control. It is known that setting a current proportional to voltage does not work well and it creates a negative resistor in a wide frequency range because the circuit is not passive. This paper presents an alternative idea of synchronization of a single-phase grid-connected DC/AC inverter by using a double integration method. It is simpler than PLL since it needs neither a phase comparator, nor a local oscillator. It provides a signal in phase with the current.

The art of the method is how to remove the integrating constants without degrading the signal.

ARTICLE HISTORY

Received 14 November 2016 Accepted 7 August 2017

KEYWORDS Frequency control; DC/AC inverter; DISM

1. Introduction

The integration rate of the microgrids by single-phase inverters to the grid have increased a lot, mainly in the dense populated countries where photovoltaics (PV) is put on the roof [1]. In the early days, an algorithm such as a current proportional to voltage control has been tried out but it tends to instabilities, since during starting generation period, some "negative" resistors in parallel to the grid are presented. When the equivalent parallel Thevenin impedance of the grid is higher than the equivalent negative resistance, oscillation is almost certain. Control methods using high-performance digital signal processors (DSPs) and field-programmable gate array (FPGA) have recently been used to implement some control techniques. The most popular ones are the dead beat repetitive, capacitor current feedback and slidingmode control [2,3]. Some other techniques have been developed such as a D-Q synchronous frame controller for single-phase inverters (SRFPI). Phase-locked loop (PLL) controller techniques recognize the fundamental without making a "negative resistor", but there is still a hidden dynamic phenomenon as well [4,5].

Making a rotating vector or a known angle in the period requires a minimum of two independent phases in a system [6]. The single-phase inverter voltage output has only one and a second signal would be needed in order to construct a second phase of 90° shift [7]. The more common used method is the PLL control; however, it has a number of drawbacks. It does not use a second signal but it does use a phase comparator that has the tendency to inject a second harmonic in the

feedback, which has to be filtered out by some kind of a notch filter [5]. The filtering can introduce an unwanted transient response [8]. Moreover, a system having a filtering subsystem increases the computing time. The filtering system might be averaged over a half or full period. But this also needs time and it has a dynamic phenomenon that makes it difficult to start in the first periods when the grid is just enabled. To avoid the drawbacks of the briefly discussed methods, a double integration synchronization method (DISM) can be used to synchronize the DC/AC current to the grid frequency. The method is known and has been used in different applications; however, the problem of the drift phenomenon has been a challenge [9,10]. The art of the method presented in this paper is how to employ DISM and remove the integrating constants without degrading the signal.

2. Proposed control: DISM for a single-phase inverter

This paper proposes a DISM for synchronizing.

The implementation of the DISM can be perfectly done starting from a single-phase signal. The double integrator makes a reference signal 180° shifted, so perfectly synchronized with the grid, independently from the grid frequency changes.

Figure 1 shows the simplified principle of DISM. The double integration is applied on grid voltage which is multiplied with the set current. The set current from a MPPT (Maximum Power Point Tracker in the PV

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Figure 1. DISM scheme (without removal of integrating constant).

case) [11] is compared to measured current. The PI control is applied to make correction of the DC offset error. Based on the DISM response, the PWMs are generated which control the H-bridge inverter and the buck boost converters.

The following paragraph analyses the effect of double integration. Assuming that the DC/AC inverter is square-wave full-bridge type, hence the voltage at grid level at the inverter in Figure 1 including some perturbation has the following equation:

$$V(t) = \sum_{n=1,3,5,7,\dots} \frac{2V_{DC}}{n\pi} [\sin(\omega_1 t) - \sin(\omega_1 t - \varphi)], \quad (1)$$

where $V_{\rm DC}$ is the dc link voltage, $\omega_1 t$ is the angular rate and φ is the phase shift.

Applying a double integration on (1), the following mathematical expression presents the reference current with a phase shift of -180° .

$$I(t) = \sum_{n=1,3,5,7,...} \frac{-2 V_{DC}}{(n\pi)\omega_1^2} [\sin(\omega_1 t) - \sin(\omega_1 t - \varphi)] + \omega_0,$$

where ω_0 is the angular rate at an initial condition. (2)

Based on (2), it is obvious that the amplitude of the current is inversely proportional to the grid frequency. However, the current phase synchronizes with the voltage phase. To some extent, the integrator behaves as a low-pass filter.

To make the control system presented in Figure 1 more effective, the DC offset of the integrator has to be removed. The feedback from the removal of the offset should not interfere with forward integrator in a continuous mode, as it might introduce a phase shift or harmonics.

3. Analog equivalent for removing offset

The principle described in Figure 1 is normally challenged by the presence of an integrating constant, which caused a lot of trouble. On the one hand, some engineers prefer a fast removal of the integrating constant; however, it ends by affecting the phase accuracy of the double integrator. On the other hand, slow removal of it results in a long transient at start-up or after heavy disturbances, such as a large dip or a phase angle shift in the grid. A compromise leads to an understandable analog PI controller with a nonlinear feedback in Figure 2.



Figure 2. DISM with removal of integrating constant concept.

This is done by a nonlinear feedback and a "hold" circuit. In other words, the offset correction of the double integrator occurs when it is needed at any initial condition or transient. Figure 2(a) shows the equivalent analog circuit. The first operational amplifier integrates the grid voltage without considering the initial conditions.

Since the non-consideration of the initial condition of a small offset can cause an integrating constant and/ or drift in the output signal, the feedback integrator corrects the offset based on the voltage across D1 and D2. Figure 2(b) presents the proposed related algorithm which can be employed to implement the DISM in digital format. Different constraints are formulated to avoid the presence of the drift phenomena. Figure 2 (a,b) explains the first part of the integrator. The second integrating part is similar to the first part. R4, R2 and R3 are gains for forward and feedback integrators.

Taking into account that the integrator's input signal is a state of derivative of its output signal, the following equations can be considered:

$$I_{2}(t) = \int_{t_{0}}^{t} u(t)dt + I_{20},$$
 (3)

where the I(t) and u(t) are input and out signals, respectively. I_{20} is the initial condition.

Using an almost dead zone control is quite easy both in analog and in programming. Based on Figure 2(c)and Equation (3), the drift control model is developed in the following equation:

$$I(t) := \begin{cases} \frac{K_1 u(t)}{Vd_1} + K_1 & \text{if} \quad I(t) \ge Vd_1 \\ \frac{K_2 u(t)}{Vd_2} - K_2 & \text{if} \quad I(t) \le Vd_2 \\ \left(\frac{K_1 + Vd_1/K_1}{Vd_1}\right) u(t) & \text{if} \quad 0 \le I(t)(t) \le Vd_1, \\ \left(\frac{K_2 + Vd_2/K_2}{Vd_2}\right) u(t) & \text{if} \quad Vd_2 \le I(t) \le 0 \end{cases}$$
(4)

where Vd_1 , Vd_2 are D_1 and D_2 voltage drop, respectively. The voltage drop is estimated at 0.6 V dc, which is the boundary condition used to investigate whether the input signal has high gain or low gain. K_1 and K_2 are coefficients of I(t). In order to control the drift, K_1 and K_2 are -1 and 1, respectively. D1 and D2 are employed to define the break points of the boundaries. For the third and fourth cases, the drift phenomenon is avoided to happen, whereas for the first and second cases, the integrator auto reset has to be handled by the feedback integrator. The interval between peak points is used to add or subtract a constant value to the input signal which is scaled by the slope of the dead zone interval. This is done for the first and second integrals. Hence, (4) is a key tool to implement DISM digitally. The following paragraph explains the dynamics behaviour of the DISM in MatlabTMSimulink.

4. DISM simulation

The DISM simulation was done in MatlabTM. The forward and feedback integrator sampling times are f_s and $1/4^*f_s$, respectively. Hence, the forward integrator is faster than the feedback integrator is. This helps the algorithm to detect and remove the drift phenomenon so that the integrator resetting can take few milliseconds. Figure 3(a–d) presents the synchronization of an inverter current to the grid voltage frequency at 50, 45, 55 and 60 Hz, respectively. The reference current is synchronized with the grid voltage (Figure 3). However, the variation of the frequency affects the reference current amplitude. The higher the grid frequency becomes, the lower the current amplitude becomes.

This can be corrected by the MPPT (Figure 1) or a gain value in the control after some periods. On a short time transient, the grid frequency rises and a small amount of current is injected into the grid. For more power injected to the grid, the inverter frequency decreases. If the grid is connected to a PV panel



Figure 3. DISM Matlab simulation of the analog circuit in steady state for different frequencies (with nonlinear PI feedback to remove the integrating constant).

converter, the MPPT will restore the frequency after some period by adjusting the power grid [11].

The DISM rejects the amplitude of harmonics. A third harmonic is reduced by a factor of 9, and a fifth is reduced by a factor of 25, which is enough in practice. If a square wave is applied, 1/27 third harmonic is expected compared to the fundamental and 1/125 for the fifth harmonics (Equation (2)). Consequently, the value of the reference current does not content significant harmonic component.

5. Lab experiments

Before implementing digitally the double integrator synchronization method for the future work, the analog circuit has been used to test the dynamics of the system. The analog system has been used to calculate and tune well the gains of the first and second integrators. A simple operational amplifier, TL084, was used to conduct the experiment. In Figure 4(a), the first integrator lags 90° referring to the original signal. In Figure 4(b), the second integrator output in purple is synchronized with the input signal, grid voltage, after being amplified by a gain of k = -1. In fact, the second integrator could be -180° phase shift referring to the input signal. The circuit is simple and works well for the grids ($50 \times (1 \pm 10\%)$) Hz and ($60 \times (1 \pm 10\%)$) Hz. Practically, it can handle frequencies from 40 to 70 Hz. In practice, variable gains are required in a real circuit to get a variable amplitude in the current set value to the grid. Making a variable gain is not so easy in analog, and therefore, the digital system, modern technology, is required, but the analog system is still rather easy to build and simulate. Figure 4(c) presents the transient state of the input signal, square wave form, at a starting point and Figure 4(d) presents the steady state of the input signal. The square wave form signal was used to test if the DISM does not deteriorate the input signal.

6. Qualitative comparison with PLL systems

A PLL has an integrating process from frequency to phase; the loop integrator has to be used with a phase compensation to avoid an oscillatory response [11]. The traditional variable frequency oscillator is replaced in digital with a shift of the angle at each sampling moment. PLL systems react also on harmonics, but it happens by a frequency modulation [7]. In PLL systems, the loop gain should be high at synchronizing, and slow in a normal operation. This decision-making is not that easy, and it is difficult to implement well in case of phase shift or large voltage dips or missing periods. As a comparison, the DISM has a natural way to recover from transients, as the same nonlinear feedback is always active.



Figure 4. DISM measurement on the analog circuit, with removal of integrating constant at the transient states.

7. Conclusions

An alternative synchronization method is presented. It uses a different principle from the PLL methods. A DISM can be used to synchronize the DC/AC frequency to the grid frequency. The paper presents how the integrator initial constant can be removed in order of not deteriorating the input signal. This has been approved by the experimental results summarized in Figure 4. In order words, the simulations and lab results obtained from the experimental work can be applied on real system. The DISM algorithm is always active, which makes it robust against disturbances. Besides, it delivers useful signals from the first period.

The DISM is simpler to design, program and simulate than a PLL since it does not need the D-Q decomposition techniques.

Acknowledgment

The first author is thankful for the facilities that University of Ghent has been offering to him via BOF funds.

Disclosure statement

No potential conflict of interest was reported by the authors.

Funding

Ghent University BOF funds.

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