

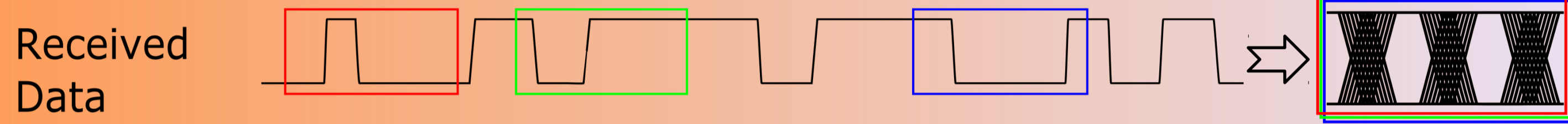
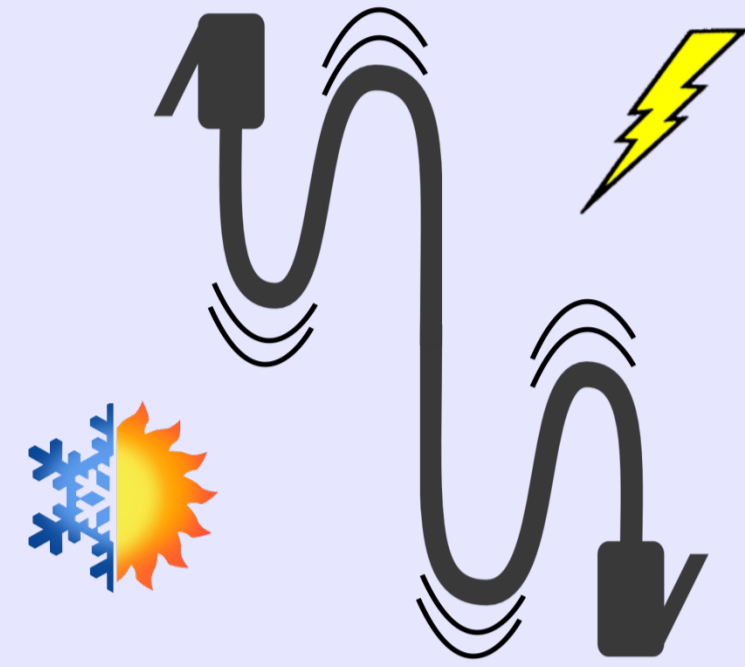
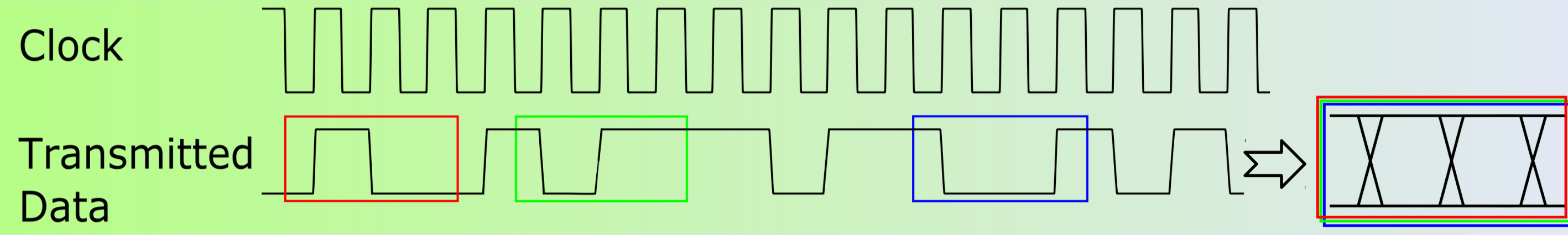
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¹INTEC design, Ghent University – iMinds – IMEC

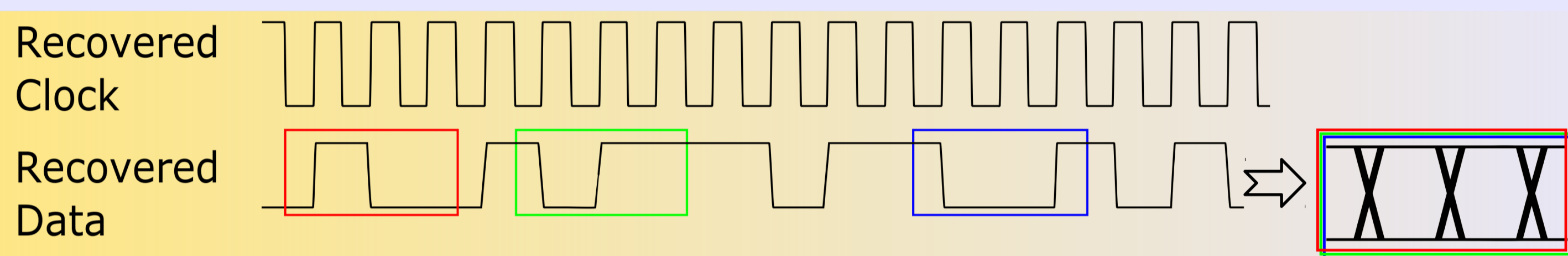
²CAS – ELIS, Ghent University

Why Clock and Data Recovery circuits are indispensable

Transmitter

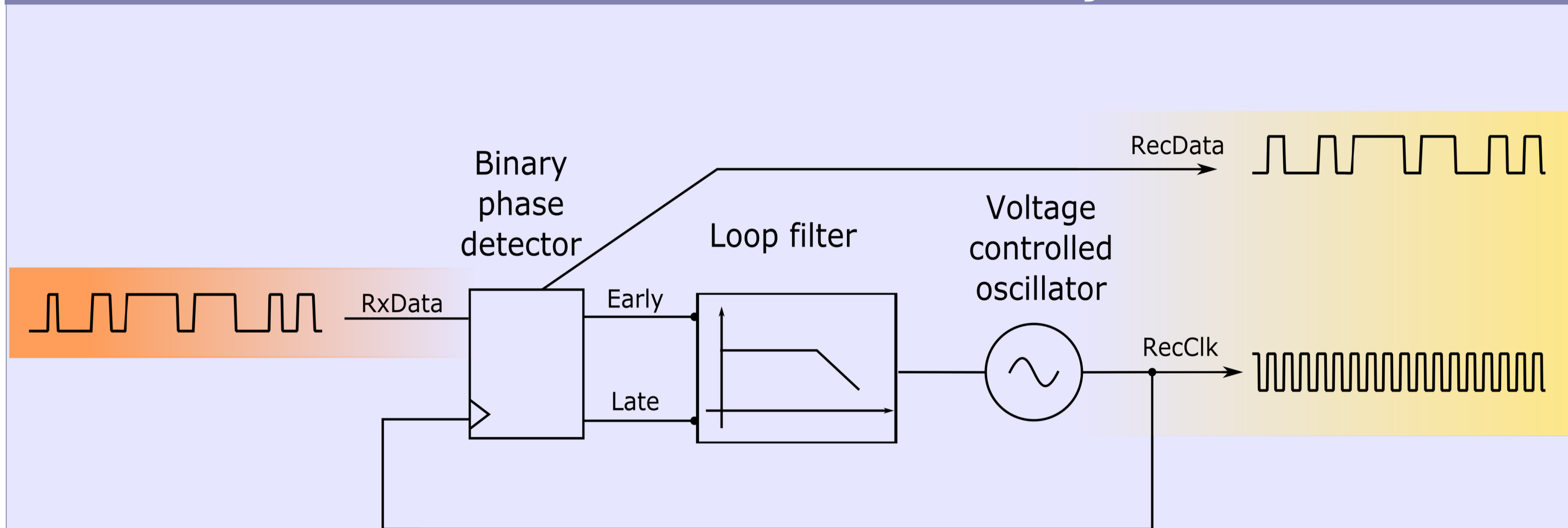


Receiver: CDR

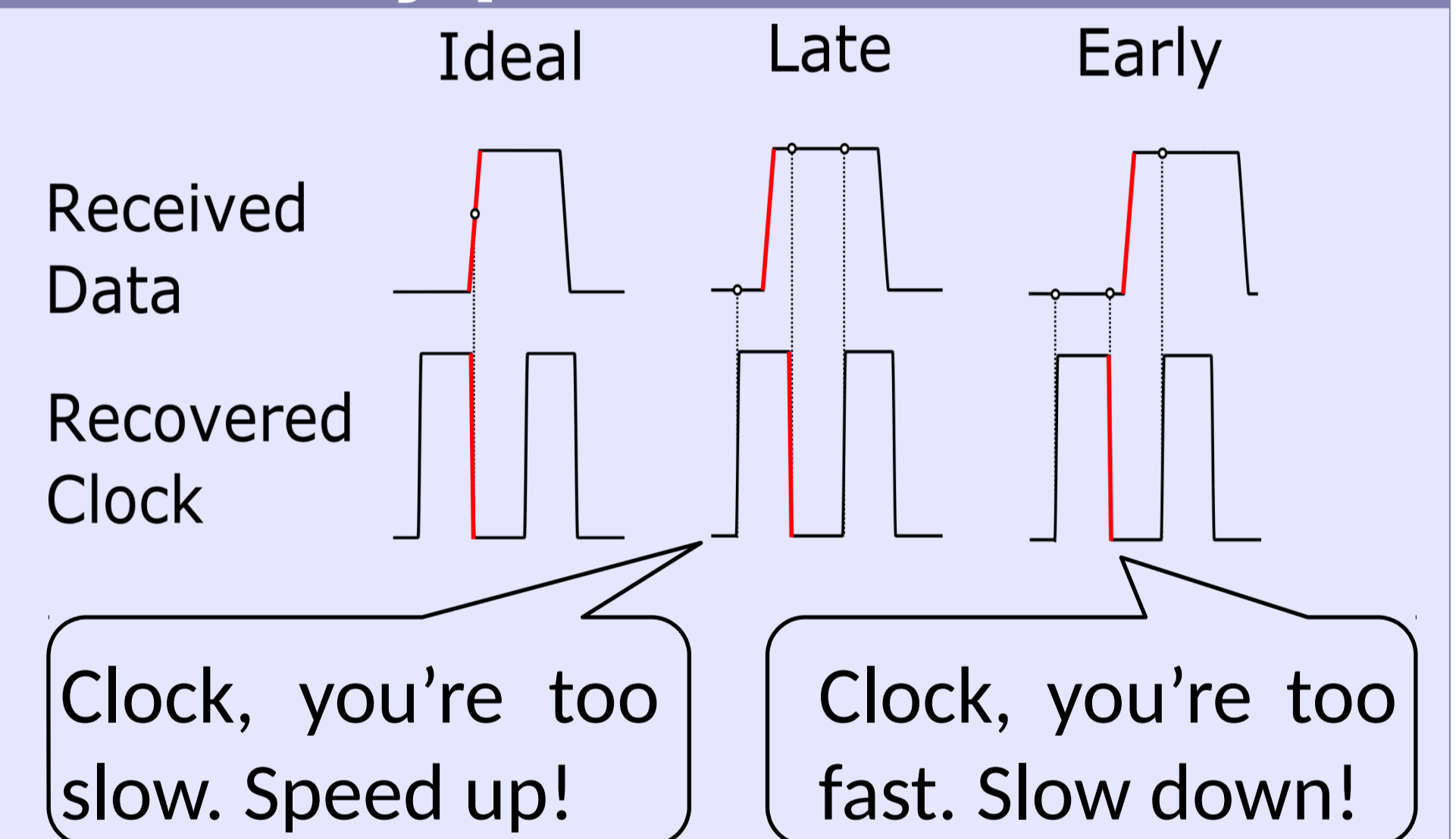


- High-speed serial data streams are sent without an accompanying clock signal
- Unwanted effects of long interconnections and other stress factors on the communication link distort the transmitted data signal
- The receiver recreates a clock signal (timing information) from the received data signal
- Using the recovered clock, the digital data is extracted from the deteriorated signal and can be further processed

Clock and Data Recovery

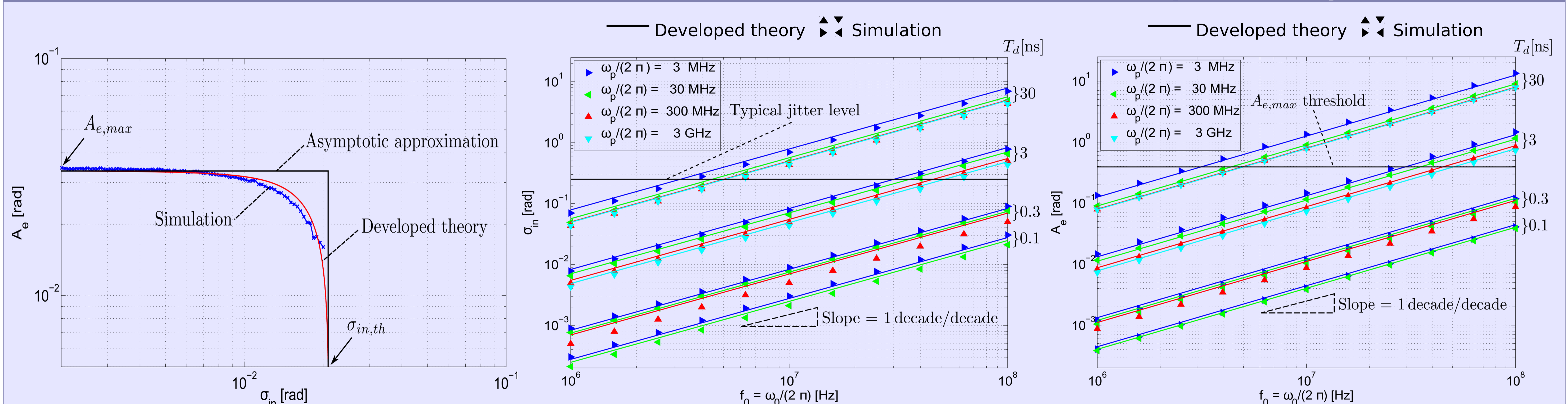


Binary phase detector



- Non-linearity → hard to analyze
- Solution: quasi-linearization technique**

Close match between the simulation results and the developed theory



Fast determination of instability

- Stability = essential property of the system
- New method is **1000x faster** than brute-force simulation
- Further analytical approximations lead to simple equations for a **quick check!**

$$A_{e,max} \approx \frac{8\alpha}{\pi^2} T_d \omega_0$$

$$\sigma_{in,th} \approx \frac{1}{2} \sqrt{\frac{\pi}{2}} A_{e,max}$$

Acknowledgements

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