Abstract
High-speed electronic circuits are crucial to the success of optical interconnects. This Chapter focuses on the driver electronics in the transmitter and the transimpedance amplifier in the receiver. These critical circuits need to be closely integrated and co-designed with the electro-optic and opto-electronic devices such as VCSELs and photodiodes. The most practical modulation schemes for optical interconnects are also discussed and the basic driver and transimpedance amplifier circuit architectures are introduced together with some state-of-the-art research results.

Key words
VCSEL driver, transimpedance amplifier, co-design

10 Electronic Drivers/TIAs for optical interconnects

10.1 Introduction

High-speed electronic circuits are crucial to the success of optical interconnects, not only to generate, process and store huge amounts of data, but also to interface between purely digital devices (such as network processors) and rather analog electro-optic (E/O) and opto-electronic (O/E) devices, such as lasers, optical modulators and photodiodes. These high-speed electronic front-end circuits, being the driver in the transmitter and the transimpedance amplifier (TIA) in the receiver are the main topics of this Chapter.

The functionality of the driver and TIA are illustrated in Figure 1. The driver chip receives the data to be transmitted from a digital CMOS chip, which typically includes a "clock and data recovery" (CDR) circuit to synchronize the different data streams and a serializer to combine the multiple data streams in to one high-speed data signal for transmission. Due to the high bit rates, the interface between the digital chip and the driver chip is typically a low-voltage differential digital signal e.g. using current-mode-logic (CML). The driver chip then converts the incoming data voltage waveform into appropriate current or voltage pulses of particular amplitude, eventually superimposed on a certain bias current or bias voltage to optimize the operating point of the optical laser or modulator. The driver circuit is designed such that the resulting optical waveform is an accurate representation of the digital data. Realizing such high-quality optical modulated waveforms is one of the main challenges of the driver design, despite the E/O transfer function of the laser/modulator and the parasitics of the electrical interface between driver and laser/modulator. Moreover, as the characteristics of optical devices depend generally on the temperature, the driver functionality must be adapted accordingly for best performance. When the E/O bandwidth is marginal for the targeted bit rate, equalization needs to be introduced in the driver or receiver circuitry as well. Excessive parasitics on the other hand, contributed by interconnections, can degrade the modulating waveform due to reflections, overshoot, ringing etc.

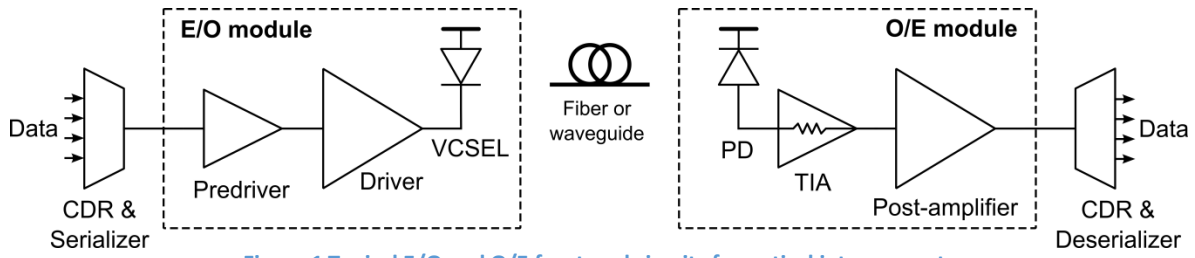


Figure 1 Typical E/O and O/E front-end circuits for optical interconnects

At the other side of the optical fiber, the receiver must be capable of reconstructing the digital data from the optical waveform. The optical signal is typically attenuated and eventually distorted by dispersion in the fiber. As the received optical signal is typically weak due to losses in the optical interfaces (and in the optical modulator when external modulation is applied), a low-noise TIA is

needed to convert the weak photodiode current into a voltage waveform, which is strong enough for further processing. The TIA output voltage is then further amplified in a post-amplifier (PA) and the data is then extracted by CDR circuitry. The particular TIA design challenges will be discussed in Section 10.4, considering sensitivity, dynamic range, offset compensation and automatic gain control (AGC). Notwithstanding the optical interconnects are short, the required receiver sensitivity is a considerable challenge, because the transmitted optical power levels are constrained due to power consumption constraints, technology limitations or due to coupling losses. Moreover, the fastest optical transmitters today are limited in extinction ratio, i.e. ratio between high and low modulation levels, making the reception even more difficult in combination with crosstalk.

In datacenters, multiple transceivers are applied in parallel to realize higher bit rate point-point connectivity inside racks or between racks. This could be implemented using fiber ribbons, wavelength division multiplexing (WDM) or using multi-core fibers. In future, multiple modes may be considered as well, but today, it seems that datacenter infrastructure will migrate towards single-mode fibers to be futureproof, while multi-mode technology is showing very interesting progress as well. Irrespective of the optical multiplexing technology, applying multiple data streams in parallel requires multi-channel driver and receiver electronics. This brings additional challenges to the electronics design, on top of the need for ever faster and lower power transceiver circuitry. Multi-channel devices need to fit in specific packages, requiring a tight integration of electronics and photonics. This tight integration not only brings challenges for the assembly, but restricts power consumption and introduces additional issues such as thermal crosstalk from electronics to photonics, mutual parasitics, electrical crosstalk, power/ground integrity…, making the design of datacenter transceivers particularly challenging.

As transceiver circuits for optical interconnects need to be low cost, low power and small in footprint to fit in small packages, the circuit complexity should find a good balance between modulation efficiency and implementation efficiency of the analog/digital circuits. For this reason, the basic modulation schemes NRZ (2-level), duobinary (3-level) and PAM-4 (4-level), illustrated in Figure 2, are the most practical options. Whether one or the other is better, depends on the channel attenuation and frequency response including fiber and the E/O devices. More complex schemes typically require a high-speed digital-to-analog converter (DAC) and a high-speed analog-to-digital converter (ADC) in combination with high-speed digital signal processing (DSP). For long reach applications, this complexity is justified by the higher spectral efficiency and higher throughput. However, for datacenter applications, complexity is a competitive threshold.

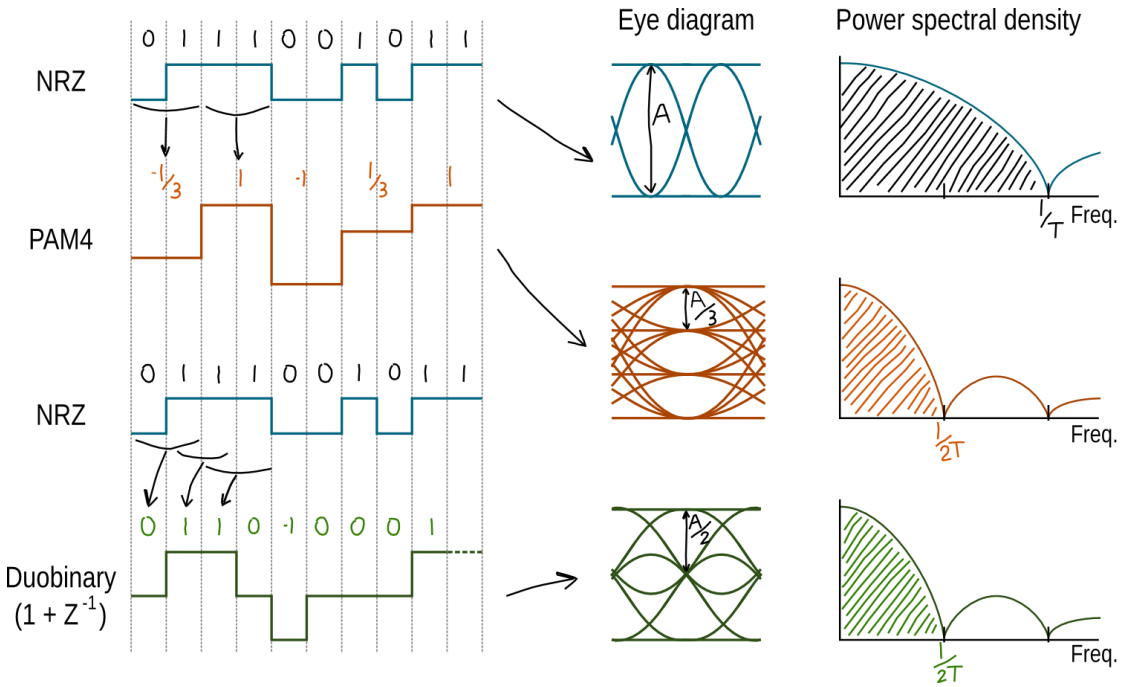


Figure 2 Simplified comparison of the basic modulation schemes: NRZ, PAM4 and duobinary

Today, 25Gb/s VCSEL links are widely commercially available, using NRZ modulation and multi-mode mode fibers up to a few hundred meters. As long as sufficient bandwidth is available, NRZ, eventually assisted by equalizer circuits, will be preferable because of its minimum complexity and lowest latency. Now, moving towards 50Gb/s line rates, or even 100Gb/s, puts traditional NRZ signaling under pressure. As a result PAM4 is widely being adopted for achieving higher serial data speeds (50 Gbps and higher) with a lower relative bandwidth. Meanwhile, a powerful alternative, duobinary, is often overlooked or misunderstood. However, scientific discussions and experiments in the literature recognize that duobinary actually provides more performance in most cases [Jensen2016]. The main criticism against duobinary is that duobinary circuits need to operate at the full baud rate, however, this is no problem as demonstrated in [Kerrebrouck2016] at 100Gb/s using custom transceiver chips in a mature 130nm SiGe BiCMOS process.

In this section, we will briefly introduce the concept of these basic modulation schemes. Extensive comparisons of these schemes are presented in [Kerrebrouck2016], considering electrical interconnections inside a rack and in [Jensen2016], considering short-reach optical links. In general, the goal of most advanced modulation schemes is to limit the needed bandwidth in order to achieve higher serial data rates. In this process SNR is typically traded for bandwidth. When using PAM4, this is done by combining two NRZ bits into a single PAM4 symbol, so that the same throughput is achieved at half the rate, resulting in about half the required bandwidth. As PAM4 combines two bits in the amplitude of one symbol, 4 different levels can be obtained, leading to an SNR which is theoretically three times smaller compared to NRZ, assuming the same maximum swing.

Duobinary limits the bandwidth in a completely different way. By adding the previous bit to the current NRZ bit, a stream of duobinary symbols is created (function: $1 + z^{-1}$). This leads to a three level signal with a symbol rate identical to the original NRZ bit rate. However, the bandwidth (shown by means of the power spectral density (PSD) in Figure 2) is compressed by the addition of bits that make it impossible to have high speed signals transitions. E.g. +1 can never go directly to -1 in one bit period, but takes at least two bit periods. SNR is thus traded in for bandwidth compression by going to three level symbols. Note that the SNR penalty of duobinary is lower compared to PAM4. Moreover, duobinary can be created very easily, by sending the NRZ stream through a low pass filter

which adds intersymbol interference (ISI) corresponding to $1 + z^{-1}$. This can be done by using the channel response of the transmission medium together with some equalization at either the transmitter or the receiver. In this way part of the channel loss is exploited to create the duobinary stream from an NRZ signal which means this loss doesn't need to be compensated. This allows to have a simple NRZ transmitter providing backwards compatibility to NRZ systems, but requiring less equalization. However, despite its advantages, duobinary is not (yet) included by the main standardization bodies, so in the near future we will mainly see NRZ and PAM4 transceiver products for optical interconnects in datacenters.

10.2 Co-design and co-simulation of electronics and photonics

Due to the very high bit rates in today's optical interconnects, the design and simulation processes of optical transmitter and receiver front-ends need to include accurate models for the electronic circuits, the on-chip and off-chip interconnects, the electrical parasitics of the photonic devices and the electro-optic response of the photonic devices. Such a co-simulation approach is illustrated in Figure 3 and allows for a real co-design of electronics, interconnects and photonics in order to identify the trade-offs between various parameters and to predict the system-level performance. For example, considering a conventional positive-intrinsic-negative (PIN) photodiode (PD), a larger active area will capture more photons, so a larger PD will have a higher responsivity, which is beneficial on one hand, but a larger PD junction will also show a higher capacitance, reducing the receiver bandwidth. So a co-design approach can yield the required insight to quantify the relevant trade-offs and to find a good balance between conflicting requirements in order to derive an overall optimum considering various specifications.

In practice, the "design space" or degrees of freedom are often restricted somewhat by the chosen suppliers or technology platform, and in worst case, it may not be possible to change anything to the photonic devices e.g. when the design of laser, modulator and PD are fixed. In such case, the co-optimization process focuses on the electronic circuit topologies and the layout of the interconnections.

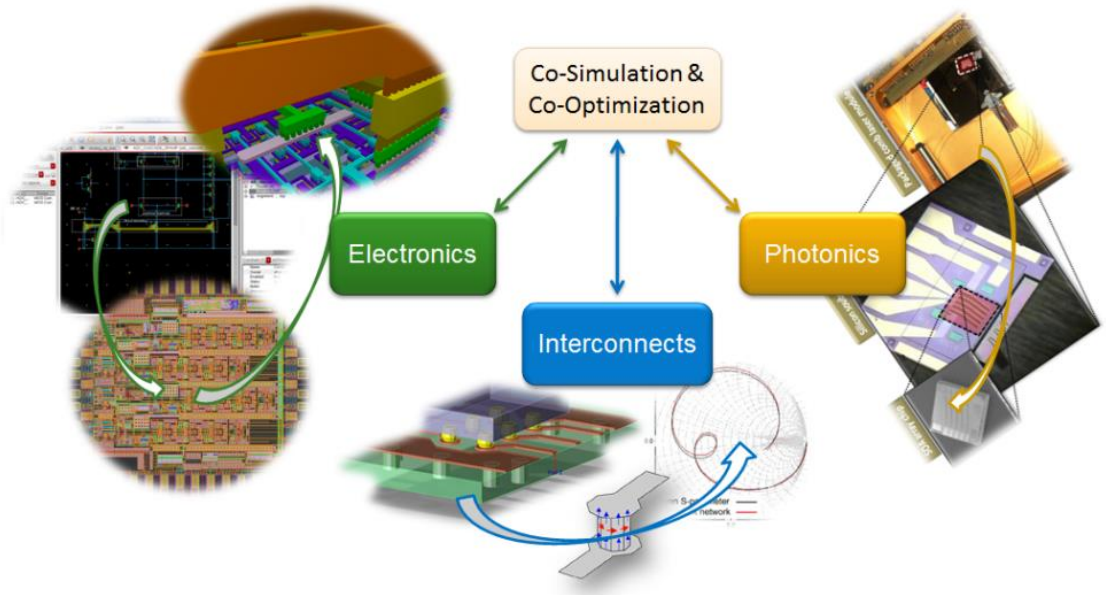


Figure 3 Co-design and co-simulation of electronics, interconnects and photonics

It is clear that for the co-simulation process, one needs to bring together the models of the different parts in one simulation bench. For this purpose, advanced circuit design tools such as Cadence

Virtuoso or ADS are well suited because the most complex circuits to be considered for the transceiver design are in the electronic circuitry and, in the end, the electronic circuitry determines largely the performance (power consumption, bandwidth, sensitivity, signal quality…) for the given photonic devices. Moreover, such professional electronic IC design tools, can mix transistor level circuitry with different kinds of models to combine subsystem and system simulations and various simulators are available in these tools to efficiently simulate different aspects (transient, S-parameter, harmonic balance, noise, stability…).

To derive a model for the interconnects and the photonic devices, one typically starts from S-parameter measurements. S-parameters are measured in the frequency domain under small-signal conditions. The interconnects are electrically "passive" so these can be considered as linear elements, but one has to be aware of crosstalk. It is possible to include S-parameter models in a circuit simulation, but often it is more efficient (shorter simulation time) to first derive an equivalent circuit description. When the interconnect is short compared to the wavelength of the highest frequency involved, then a lumped equivalent circuit is used. However, for increasing frequencies, the lumped approximation is not accurate anymore so then multiple sections or distributed elements (transmission lines) need to be used. For more complex devices, besides circuit equivalents, it is often very convenient to use a hardware description language such as VerilogA e.g. to include a fiber model, the rate equations of a laser or to model an optical modulator.

To illustrate such an S-parameter fit, Figure 4 shows the measured S-parameters of the fastest C-band single-mode VCSEL to date, at a bias of 6mA, showing 22GHz of bandwidth [Spiga2016]. From the measured S-parameters, a small-signal equivalent model was developed that includes the electrical response (determined by parasitics) and the electro-optic response. Such a simulation model allows co-simulating the driver circuitry with the VCSEL response to trade-off eye quality, equalizer complexity and power consumption.

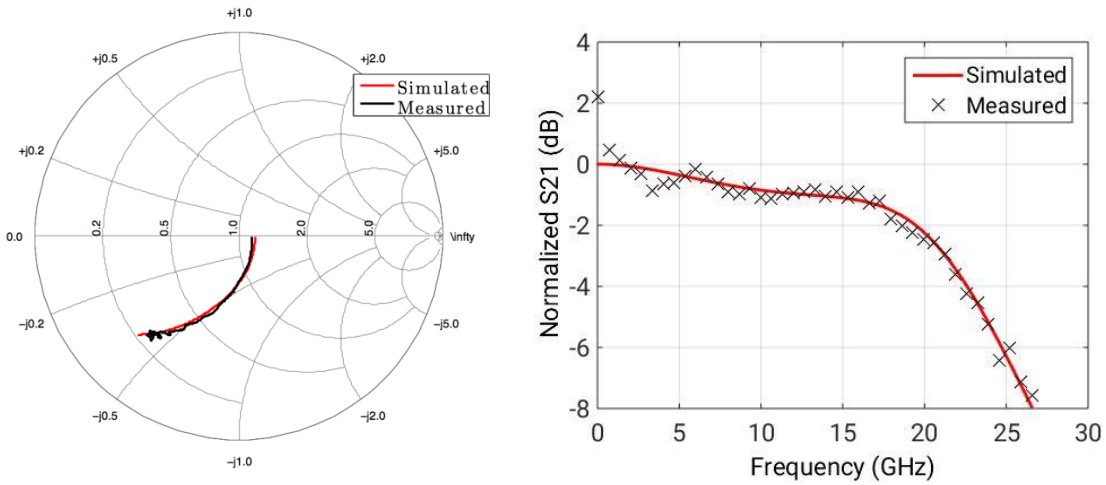


Figure 4 VCSEL model versus VCSEL measurements (a) S11 parameter (b) Normalized S21 parameter

10.3 Electronic drivers

10.3.1 VCSEL drivers

In the Phoxtrot project we focused on single-mode transmission at 1550nm, however, the VCSEL technology (Chapter 13) can be optimized for 1310nm operation as well. The main rationale for applying long-wavelength VCSELs is the compatibility with silicon photonic integrated circuits and to realize optical datacenter links beyond 500m which is not possible with 850nm multi-mode VCSELs. Without doubt, multi-mode devices are showing very interesting progress as well, although single-mode is considered to be most future proof. It is, however, somewhat more challenging to develop driver electronics for 1310nm or 1550nm VCSELs due to some key differences. First of all, long-wavelength VCSELs have a lower bandwidth. Today, the fastest long-wavelength VCSEL achieves 22GHz of bandwidth [Spiga2016], which makes it suitable for 28Gb/s and 40Gb/s NRZ applications. For 56Gb/s interconnects, a multi-level scheme such as duobinary or PAM-4 will likely be more efficient than NRZ, but by applying strong equalization as demonstrated by IBM and Vertilas it is still possible to realize 56Gb/s NRZ with a 18 GHz VCSEL [IBM]. However, equalization costs power and operational margins are needed for products to anticipate process variations, temperature variations, end-of-life degradation etc. A second key difference is that long-wavelength VCSEL arrays typically have a common anode, instead of the typical common cathode configuration for short-wavelength VCSELs. As a consequence, the long-wavelength VCSEL driver typically needs two supply voltages because the VCSEL anode needs to be connected to a higher supply voltage providing sufficient headroom for the driver output circuit, while a common-cathode array can connect its cathode to ground. The last, but also important, difference is that long-wavelength VCSELs typically require a higher drive current compared to short-wavelength VCSELs, but still considerably lower than DFB lasers of similar bandwidth.

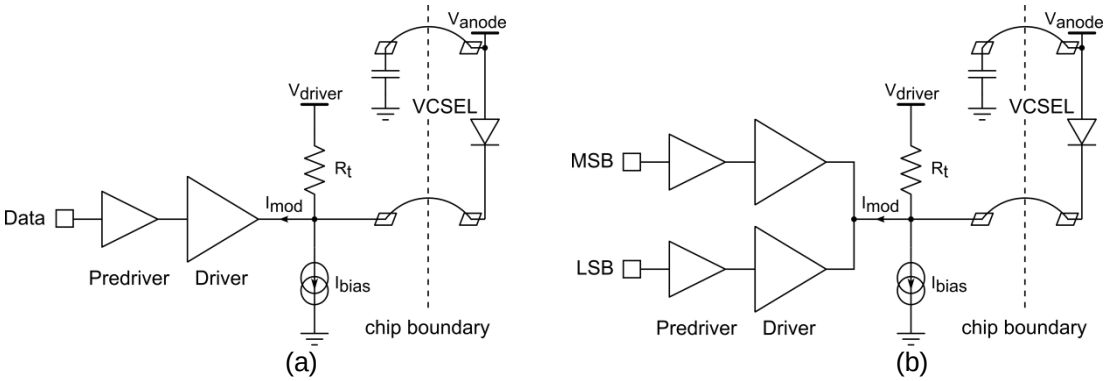


Figure 5 (a) Simplified VCSEL driver for NRZ or duobinary (b) Simplified VCSEL driver for PAM4

Figure 5 (a) and (b) illustrate the basic architectures of a VCSEL driver for NRZ, duobinary and PAM4. In both schemes, a bias current I_{bias} is used to operate the VCSEL above its threshold to obtain a high electro-optic conversion bandwidth. The high-speed modulation current is then added to the DC bias current to alternate the VCSEL optical output, as shown in Figure 6 for NRZ and PAM4 modulation. In the case of NRZ the drive current can take on two different values (I_{bias} and $I_{bias}+I_{mod}$) corresponding to a logical '0' or '1' bit. Duobinary can be obtained from the same structure, by tuning the bandwidth to introduce ISI according to $1 + z^{-1}$. For PAM4, two NRZ drivers, with binary weighted drive currents ($I_{msb}=2I_{lsb}$) are combined as shown in Figure 5 (b) so that the total drive current can take on four different values (I_{bias} , $I_{bias}+I_{lsb}$, $I_{bias}+I_{msb}$ and $I_{bias}+I_{lsb}+I_{msb}$), corresponding to logical symbols '00', '01', '10', '11'.

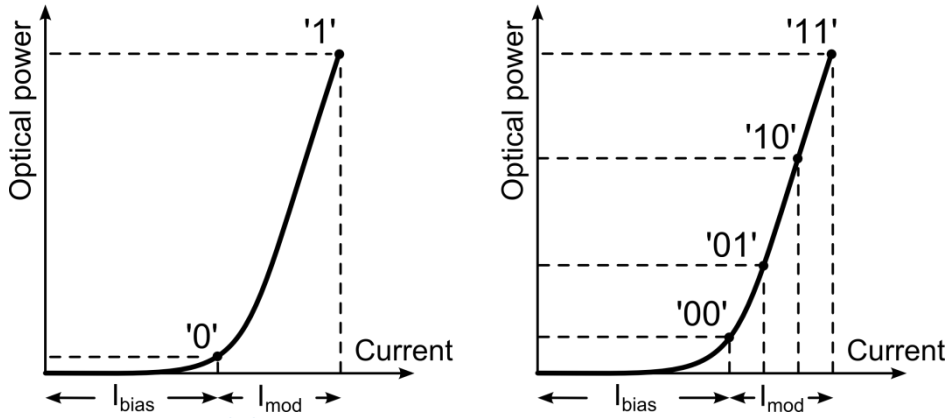


Figure 6 Power-current (PI) VCSEL characteristic and its application for NRZ and PAM4 modulation

A basic current switching VCSEL driver stage without equalization is shown in Figure 7. The DC current source I_{bias} is used to operate the VCSEL above its threshold, however, as a consequence, the optical "0" level will not be completely "dark" restricting the extinction ratio between optical "1" and "0" pulses. The high-speed modulation current is generated from the DC tail current source by switching with a fast differential pair. While the VCSEL is a single-ended device, the driver circuitry on-chip is typically differential because differential circuits such as amplifiers, buffers, flip-flops… can achieve higher speeds than their single-ended counterparts and the incoming data, delivered through transmission lines on a PCB, is also often differential to optimize signal integrity. Moreover, differential circuits are generally robust against common-mode disturbances and power supply noise. In addition, less "switching noise" is generated on the power and ground nets because the total supply current remains more or less constant during switching, improving crosstalk performance in multi-channel devices.

Depending on the input data signal polarity, the tail current is steered to the left or the right branch. When the tail current flows through the right transistor, it will be divided among the VCSEL and the back termination resistor R_t. So, a part of the tail current is dissipated in the back termination resistor, however, at high bit rate, R_t is needed to minimize the degradation of signal quality due to e.g. reflections or ringing. So the selection of the output resistance R_t is an important design choice and it depends on the VCSEL parasitics, the bit rate and the interconnection (wire bonding or flip-chip bonding). A high R_t leads to lower power consumption but also influences the bandwidth and high-speed characteristics of the interface. At the left side of the differential pair, a dummy resistor is typically added, to make the circuit more symmetrical as the (single-ended) VCSEL is added at the right side. The basic topology is the same for bipolar or CMOS implementations. In a practical realization, the performance of the driver circuit can be improved by various circuit techniques such as inductive peaking, cascode transistors etc.

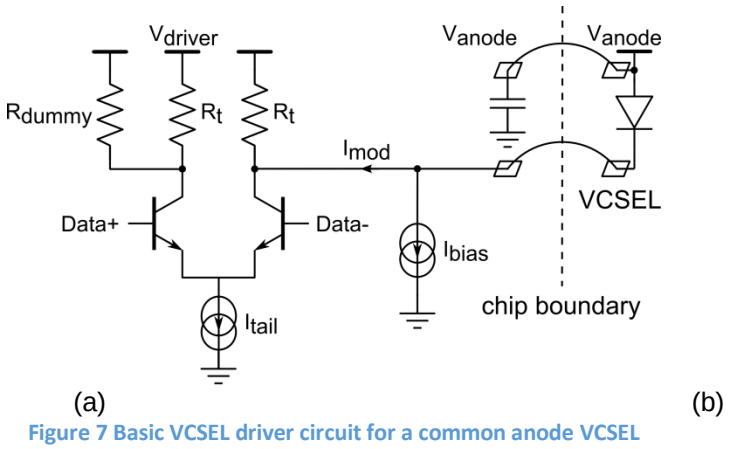


Figure 7 Basic VCSEL driver circuit for a common anode VCSEL

Today, however, increasing the data rate often relies on equalization techniques as the need for data outgrows the available bandwidth. In a driver circuit, equalization is often implemented using feed-forward equalization (FFE). In the case of NRZ and duobinary, FFE is applied to the incoming data, and the resulting pre-emphasized waveform is applied to the VCSEL, so that, after all O/E conversions and the fiber channel, the receiver captures a signal with sufficient quality. For PAM4, one could in principle apply the same architecture thereby requiring a PAM-4 input data signal and a linear FFE stage. As the data format in processors, memories, networking chips… is binary, one should at some point in the communications path translate the binary NRZ data into PAM4. For this purpose, the architecture in Figure 5 (b) is much more useful. In Figure 5 (b), two binary NRZ streams are combined into one PAM4 stream as in [Soenen2015]. As each incoming stream is binary, the FFE design is much easier compared to a fully linear FFE. To make sure that the three eyes in the resulting PAM4 signal are properly synchronized, a clock signal is used to synchronize the MSB and LSB bits in both paths.
To introduce FFE functionality in the driver, one can combine multiple basic driver stages, with different programmable tail current sources. By driving these stages with a delayed data signal, one actually obtains a finite impulse response filter (FIR), as illustrated in Figure 8.

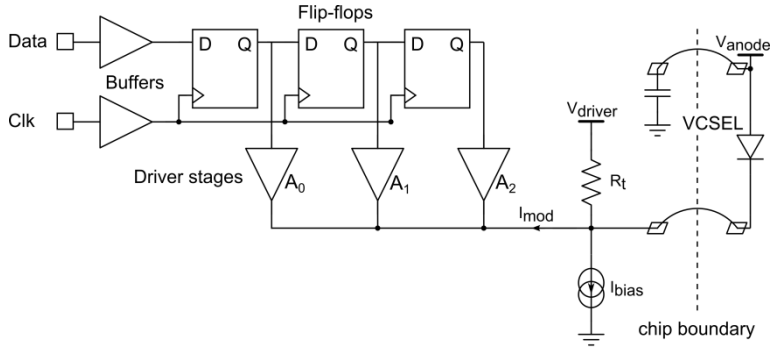


Figure 8 Simplified VCSEL driver with 3-tap symbol-spaced FFE

Recently, in the EU FP7 Phoxtrot project, a 2-channel and an improved 4-channel VCSEL driver array have been developed, optimized for Vertilas 1550nm BTJ VCSELs operating at 28 to 40Gb/s NRZ. The block diagram of the 2-channel VCSEL driver, designed in 130nm SiGe BiCMOS technology, is illustrated in Figure 9. The incoming differential data signal is terminated in a 100Ω differential impedance and buffered towards the predriver. The predriver in conjunction with the main driver delivers the modulation and bias current to the VCSEL. Since the response of the VCSEL strongly depends on the average operating current, the driving capability of the output stage covers a broad range without sacrificing signal integrity. For that reason, the gain of the predriver is dynamically adjusted according to the output current. A two tap fractionally spaced feed-forward equalizer (FFE) is implemented in the driver chip to compensate the bandwidth limitation of the VCSEL in order to achieve 40Gb/s NRZ operation.

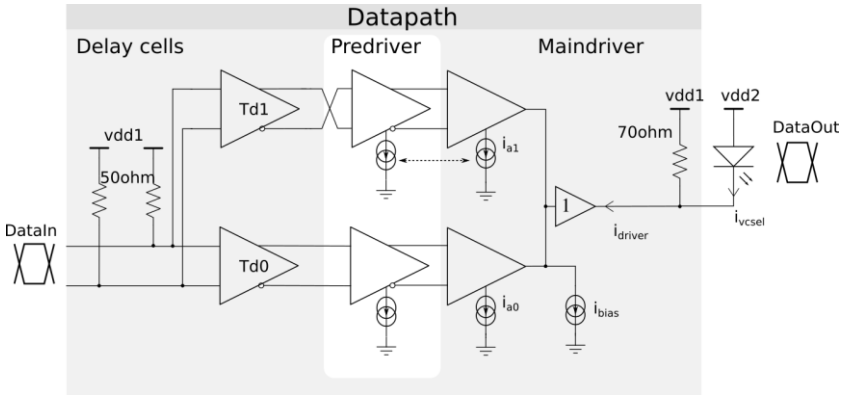


Figure 9 First Phoxtrot 2x40Gb/s NRZ VCSEL driver

This driver concept was then further improved to lower the power consumption by 50%, now estimated at 4.5pJ/bit at 40Gb/s, while extending the drive current range and supporting 4-channel VCSEL arrays with a common anode. This functionality is quite unique as most VCSEL drivers are designed for common cathode VCSELs. In the EU FP7 Mirage project, we developed PAM-4 VCSEL drivers for 1550nm VCSEL arrays, fabricated by TUM. The results of the first Mirage PAM-4 VCSEL driver chip are presented in [Soenen2015], whereas the optimized PAM-4 VCSEL driver is showing good optical performance at 56Gb/s (not yet published).

10.4. Transimpedance amplifiers

The receiver circuit design, as mentioned earlier, is quite different from the circuit design in optical transmitters. In particular, noise performance is rarely a limitation in transmitters but a very common and important aspect for the receiver front-end. Typically, the first stage in an optical receiver is a transimpedance amplifier (TIA) for converting a small input photo-current, provided by a photodiode (PD), into an output voltage signal V_{OUT}, for further processing.
The main design parameters of a TIA are the transimpedance gain, given by V_{OUT}/I_{PD}, the bandwidth, and the dynamic range determined by the sensitivity and the overload levels. The sensitivity of an optical receiver is the weakest optical power required to obtain a specified bit-error rate (BER) performance, while the strong signal handling capability is governed by the TIA's overload optical level.
Since a TIA can be considered in general as a current-to-voltage converter, the simplest form of a TIA is just a load resistor R_L, as shown in Figure 10 (a), which converts the photo-current I_{PD} to the output voltage V_{OUT} simply using Ohm's law. The simple resistive TIA topology shows some fundamental tradeoffs as both the transimpedance gain and input impedance equal the resistor R_L. In this case the lower limit of the transimpedance gain is determined by the current noise of the resistor R_L: $\overline{i_{n,RL}^2} = \frac{4kT}{R_L}$. In order to achieve a high sensitivity, the current noise must be low so for this simple circuit the load resistance R_L must be high. However, a high resistance decreases the receiver bandwidth, since the resistor is directly loaded by the photodiode capacitance and the capacitance of the output network. The high load resistance R_L causes another problem concerning the input overload current: as the output signal swing V_{OUT} is proportional $R_L.I_{PD}$, a high current will "overload" the receiver, resulting in a significant disturbance in photodetector's reverse bias condition. Ideally, creating a virtual ground at the TIA's input is preferable for reducing this overload effect.

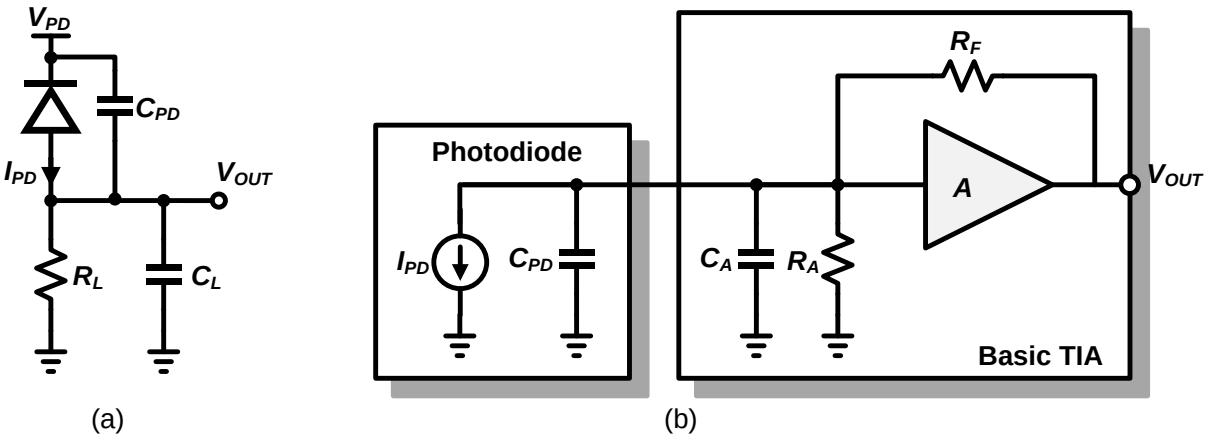


Figure 10 Basic TIA: (a) a simple resistive load (b) a shunt-feedback TIA

It is clear that the basic TIA circuit with a simple resistive load has several shortcomings. Much better performance can be achieved by introducing amplification and feedback in the TIA circuitry. So far the most common TIA configuration is the shunt-shunt feedback topology, where a negative feedback network shunts both the input and output of the main amplifier, sensing the output voltage and feeding back a proportional current to the input. This type of feedback provides a convenient low-impedance input node for the photodiode current I_{PD} and also ensures a small output resistance for better output voltage drive capability. Figure 10 (b) shows a basic shunt-feedback TIA configuration, where a feedback resistor R_F is connected across a voltage amplifier with gain A(s)=A0/(1+s*τA), input resistance R_A and input capacitor C_A. The transfer function of the basic shunt-feedback TIA can be expressed using,

$$H(s) = \frac{-R_T}{1 + s/(Q\omega_0) + (s/\omega_0)^2}$$

where

$$R_T = \frac{R_F}{1 + (R_A + R_F)/(A0 \cdot R_A)}$$

$$Q = \sqrt{\frac{(A0+1) \cdot \tau_{in} \cdot \tau_A}{\tau_{in} + \tau_A}}$$

$$\omega_0 = \sqrt{\frac{A0+1}{\tau_{in} \cdot \tau_A}}$$

in which $\tau_{in} = R_F(C_{PD} + C_A)$ is the input node time-constant, Q is the quality factor and ω_0 is the angular natural frequency. If $A0*R_A/(R_A+R_F) >> 1$, we find that the trans-resistance gain R_T reduces to a well-known form ≈ R_F. As R_F ideally determines the trans-resistance gain R_T and the TIA current noise, increasing R_F has a two-pronged effect on the noise at the output [Moeneclaey2015]: by reducing the bandwidth and quality factor of the transfer function, more noise is filtered out, and it decreases the input-referred noise spectral density. The quality factor Q provides another degree of freedom in TIA design, which is the gain near the angular natural frequency. For high values of Q, the maximum frequency response becomes larger than R_T, resulting in ringing and overshoot in the time-domain response. Therefore, the largest Q before onset of frequency peaking is particularly interesting: for $Q = 1/\sqrt{2} \approx 0.707$ we obtain the so-called Butterworth or maximally flat response, which has a good design balance between bandwidth and group-delay characteristics.

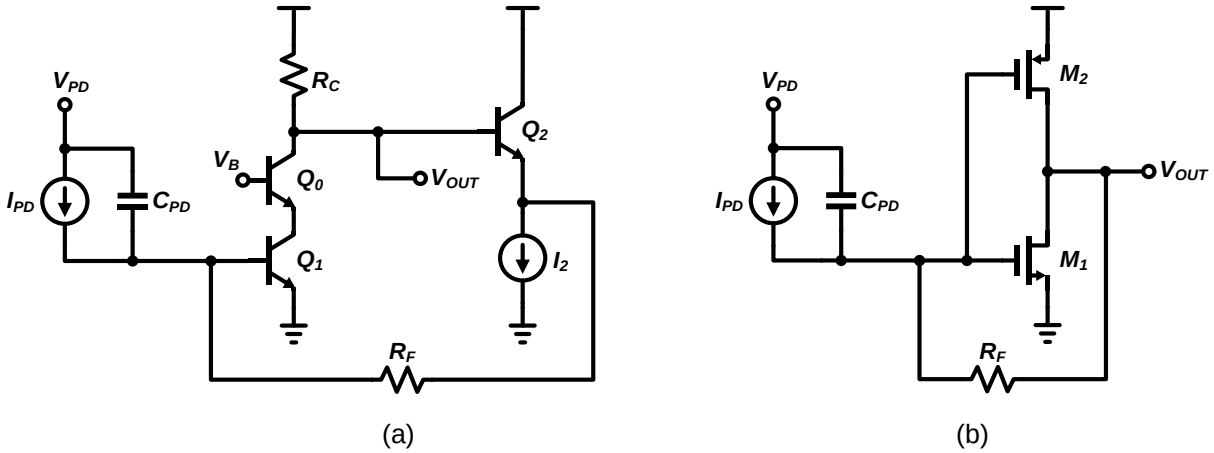


Figure 11 (a) Common-emitter/source shunt-feedback TIA (b) complementary shunt-feedback TIA

Figure 11 (a) shows a typical self-biased shunt-feedback TIA implementation with a common-emitter input stage [Verbrugghe2014]; a similar topology can be applied to a common-source input stage when using CMOS technologies. As shown in Figure 11 (a) Cascode Q_0 protects Q_1 from excessive collector-emitter voltage and reduces its Miller capacitance contribution to the input capacitance. In addition, it provides a convenient low-impedance input for current injection, which can be used to provide an extra bias current to Q_1. Q_1 has a large emitter area to reduce its base resistance and the associated thermal noise. This leads to an increased base-emitter junction capacitance. In turn, this requires a higher bias current in order to reduce the transition time through the base and to improve the high-frequency response. Note that the output has been taken from the collector of the cascade transistor Q_0, which grants better headroom for the subsequent stage compared to the conventional output at Q_2's emitter. Noise introduced by feedback resistor R_F and input transistor Q_1 are the two dominant sources of TIA noise. Taking into account tradeoffs between sensitivity, power consumption and bandwidth, detailed analysis and a design optimization scheme have been explained and proposed in [Moeneclaey2015].

One alternative is to replace the common-emitter/source amplifier with a parallel nMOS/pMOS gain stage, as shown in Figure 11 (b). Compared to the topology with an active pMOS load [Razavi2012], the complementary stage has a larger overall trans-conductance with the same bias current. The main problem of the complementary shunt-feedback TIA lies in the worse performance of pMOS transistors compared to nMOS transistors, resulting a larger pMOS transistor size (i.e. larger capacitance and lower speed) to achieve the same parallel trans-conductance. However, in more recent technologies below 45nm, pMOS transistors becomes comparable to nMOS transistors and thus using a complementary topology is gaining popularity as it can operate at a lower supply voltage [Liu2012]. For design purposes, the complementary stage can be treated as a single G_m cell and loaded directly by the feedback resistor R_F. One important drawback of this scheme is that the output impedance of this Gm cell is not buffered. Thus, direct feedthrough from the feedback network must be analyzed and designed properly, or a voltage buffer may be needed to isolate the complementary stage and the feedback network.

Finally, instead of using a shunt-shunt feedback, we may consider adding a current buffer in front of the load trans-resistance R_L in Figure 10 (a). A current buffer can be implemented by a common-base or a common-gate stage. More advanced implementations use a local feedback to improve the current buffer performance [Sackinger1990] especially for the common-gate topology (due to smaller g_m). This allows us to isolate the photodiode capacitance and the load resistance, keeping a stable TIA frequency response. The main drawback is the noise performance of the common-base/gate amplifier is in practice worse than the common-emitter/source stages, although it has been shown suitable to achieve very high bandwidth operation [Han2010].

Recently, in the EU FP7 Phoxtrot project, a 2 x 40 Gb/s TIA array has been design for use in high-speed short-range communication systems in data centers [Moeneclaey2015]. Figure 12 (a) Block-diagram of the TIA (b) chip micrograph (c) Measured BER for 25 Gb/s and 40 Gb/s NRZFigure 12(a) shows a simplified block diagram of the TIA chip and photodiode. The data path consists of a TIA input stage, a main amplifier and an output stage. The TIA input stage is a shunt-shunt feedback TIA optimized for high bandwidth and low noise performance. A control loop is formed using the balancing error integrator, which removes the dc-offset between both output signals by adjusting the dc-voltage at the inverting input of the main amplifier. This creates a low-frequency high-pass pole in the data path at 550 kHz. The TIA controller enables digital adjustment of the gain and bandwidth of the data path stages and is programmed via an external SPI interface.

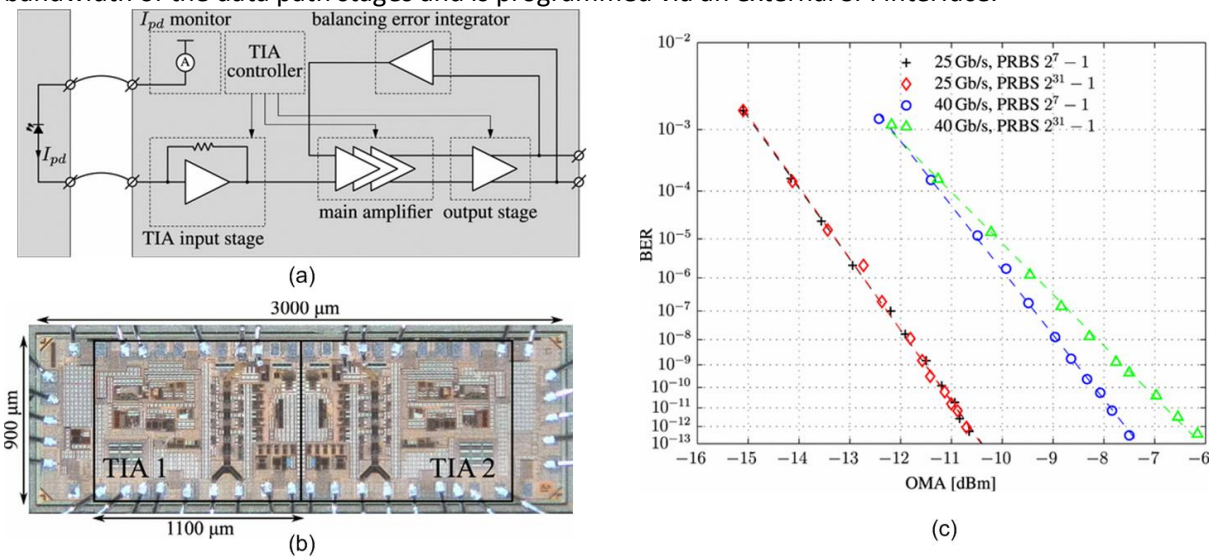


Figure 12 (a) Block-diagram of the TIA (b) chip micrograph (c) Measured BER for 25 Gb/s and 40 Gb/s NRZ

The TIA array was fabricated in a 0.13um SiGe BiCMOS technology and is shown in Figure 12(b). The single TIA channel runs off a 2.5V supply and draws 63mA. The total chip area is 3000um x 900um, with each TIA occupying 1100um x 900um. The BER was measured using an SHF 11100B error analyzer. The input was an NRZ signal using PRBS 2^7-1 and PRBS 2^{31}-1 patterns. Figure 12(c) shows the BER curves for 25 Gb/s and 40 Gb/s. When applying a PRBS 2^7-1 input pattern, the optical modulation amplitude (OMA) sensitivity at a BER of Formula is −10.6dBm for 25 Gb/s and −7.6dBm for 40Gb/s. For 25Gb/s, no significant penalty is observed when increasing the PRBS pattern length from 2^7-1 to 2^{31}-1. For 40 Gb/s, however, a 1.2 dB penalty is observed, deteriorating the sensitivity from −7.6dBm to −6.4dBm. Compared to state-of-the-art TIAs operating at 40 Gb/s, the presented TIA is characterized by a low power consumption while maintaining a competitive sensitivity.

As an alternative to NRZ, in the EU FP7 MIRAGE project, PAM4 is investigated for single-mode point-to-point links in data centers. PAM4 makes it possible to reach a higher bit rate, however, at the cost of an increased linearity requirement. In [Moeneclaey2015_OFC] we presented a linear optical receiver, operating with PAM4 signals at line rates ranging from 50 to 64 Gb/s. In the TIA input stage, the feedback resistor is implemented as an nMOS transistor biased in the linear region in order to control the transimpedance gain. The gain stages after the TIA input block utilize a degenerated differential pair topology for the required linearity.

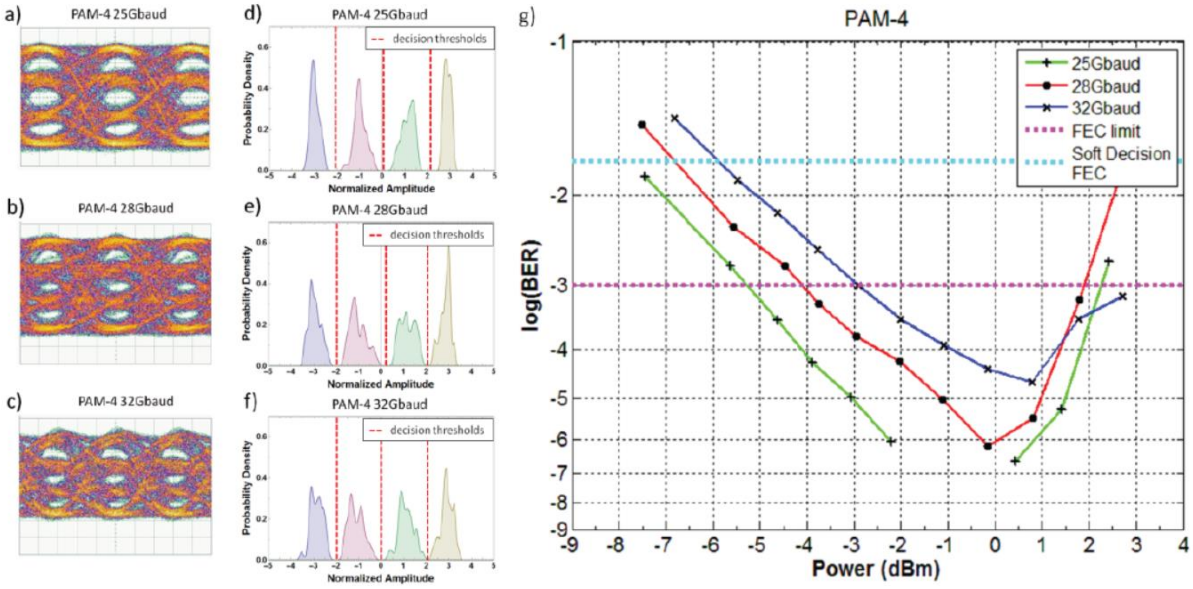
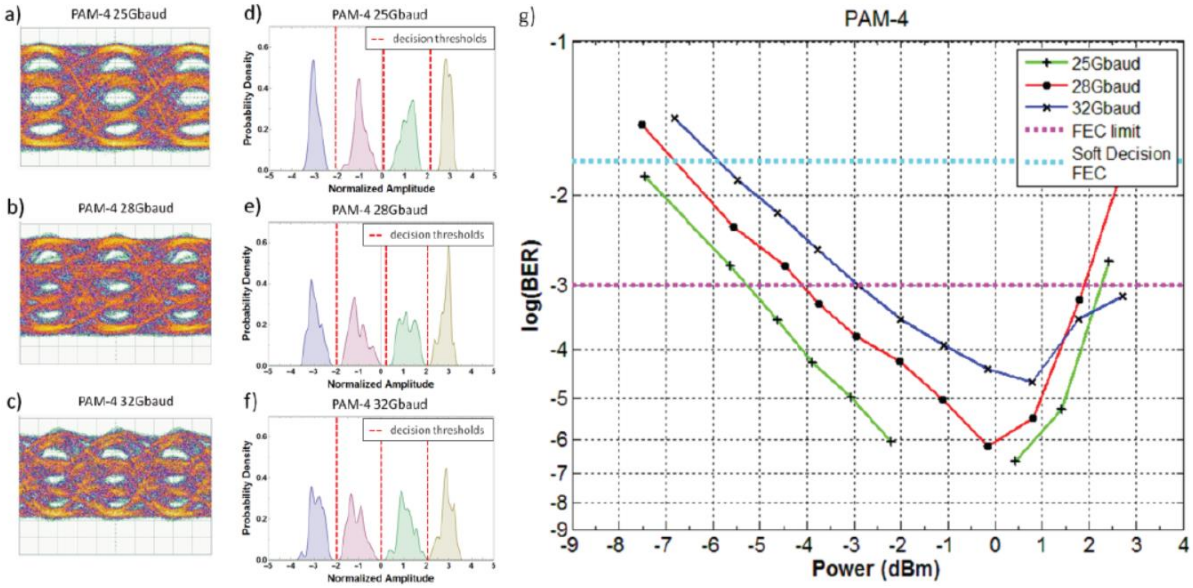


Figure 13. Receiver output eye-diagrams at (a) 25 (b) 28 and (c) 32 Gbaud; symbol histograms at (d) 25 (e) 28 and (f) 32 Gbaud; and BER measurement results (g).

The receiver was evaluated at 25, 28 and 32 Gbaud. The output electrical eye diagrams, acquired with the equivalent-time oscilloscope, are shown in Figure 13(a-c), while the distribution of PAM4 symbols is depicted in the respective histogram of



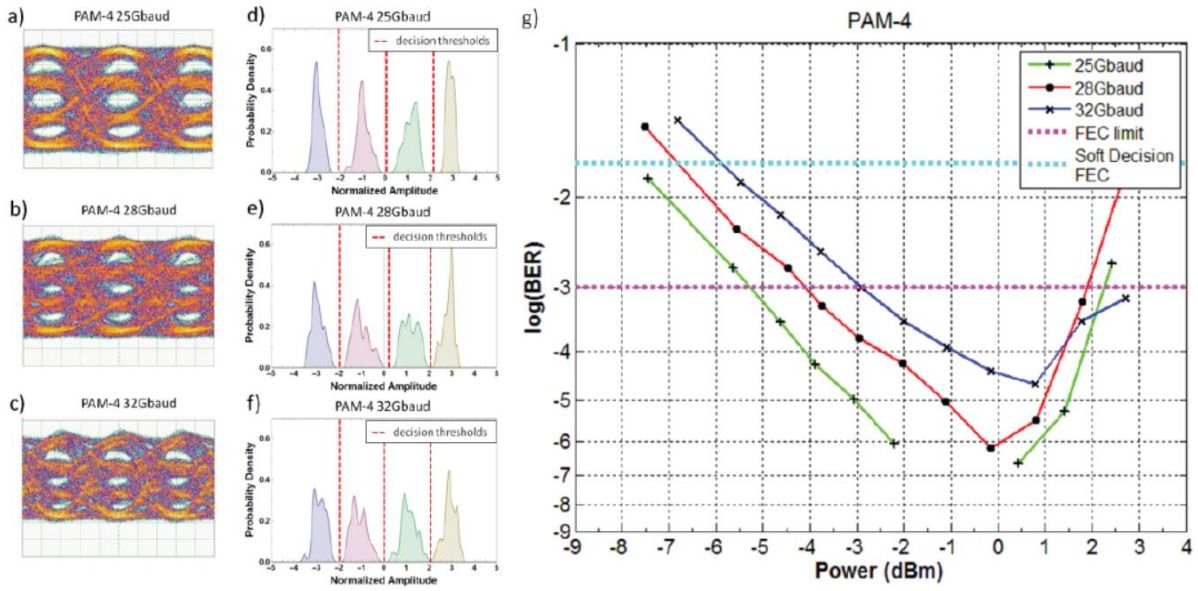


Figure 13(d-f), after signal acquisition in the real-time oscilloscope. It can be observed that the eye diagram is still quite open up to 32 Gbaud, whereas the clear separation of the symbol distributions in the corresponding histograms implies sufficient reception performance. The power consumption of the TIA channel after optimizing the receiver settings was 165 mW, yielding an energy consumption of 2.6 pJ/bit at 64 Gb/s. BER measurements were performed to the digitized signal at the real-time oscilloscope after offline clock recovery, re-sampling and automatic thresholding for symbol detection. As can be observed, at 25 Gbaud and average input power range between -2 dBm and 0.4 dBm, the received signal exhibits zero errors, which corresponds to an upper 95% confidence limit of 2.9×10^{-7}. Operation below the FEC limit was achieved in all cases, proving the suitability of the linear receiver for future interconnect standards with serial line rates above 50 Gb/s. In a very recent experiment (not yet published), by further optimizing the TIA chip and setup, we have been able to improve the sensitivity from -3 dBm to -7 dBm at 64 Gb/s for FEC limit of 1×10^{-3}. The new PIN-TIA experiment also achieved an excellent dynamic range of 8.8 dB by switching between a high and low gain mode. To our knowledge, this is the best sensitivity and dynamic range performance reported at 56-64 Gb/s PAM4 for PIN-TIA modules.

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