An Energy-Efficient, Dynamic Voltage Scaling Neural Stimulator for a Proprioceptive Prosthesis

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***Abstract*—This paper presents an energy-efficient neural stimulator capable of providing charge-balanced asymmetric pulses. Power consumption is reduced by implementing a fully-integrated DC-DC converter that uses a reconfigurable switched capacitor topology to provide 4 output voltages for Dynamic Voltage Scaling (DVS). DC conversion efficiencies of between 63% and 76% are achieved using integrated capacitances of under 1nF and the DVS approach offers power savings of up to 53.5% compared to the front end of a typical current controlled neural stimulator. A novel charge balancing method is used which has a low level of accuracy on a single pulse and a much higher accuracy over a series of pulses. The method used is robust to process and component variation and does not require any initial or ongoing calibration. Monte-Carlo simulations indicate that the charge imbalance can be less than 0.014% (at $\pm 3\sigma$) of charge delivered for a series of pulses. The circuit has been designed in a commercially-available 0.18μm HV CMOS technology and is estimated to require a die area of approximately 0.9mm^2 for a 16 channel implementation.**

I. Introduction

In recent years there have been exciting demonstrations of the potential benefits offered by electrical neural stimulators in a wide variety of applications such as vision and vestibular prostheses. Cochlear implants remain the main commercial success to date, but there are a wealth of sensory and motor rehabilitation applications that are showing rapid progress.

Despite the breadth of applications, the fundamental aim of all neural stimulators is the same – to deliver a packet of charge to an area of neural tissue, and to thereby initiate an action potential. In practice safe stimulation means that the packet of charge delivered to the tissue also needs to be removed - giving a charge balanced stimulation. Unbalanced stimulations give rise to DC currents flowing across the electrode / tissue interface and have been linked with tissue damage and deterioration of the electrode [1].

Delivery and recovery of this charge packet is typically achieved using a biphasic voltage or current controlled waveform. The former is much more power efficient but, does not allow the amount of charge delivered to be controlled. This has safety implications and also means that more frequent recalibration of stimulation intensity is required; as such current control is commonly preferred. However, the high degree of power wasted in current control (see Section III) is a serious concern for implanted systems for two reasons: (1) the power dissipated heats, and may damage the surrounding tissue, (2) the higher power usage drains the portable power source (reducing battery lifetime and increasing the number of charging cycles for a secondary battery).

This paper presents a low power current controlled neural stimulator targeted at a Peripheral Nervous System (PNS) implant for providing proprioceptive feedback from a prosthetic limb. The paper is organised as follows: Section II introduces the application, Section III introduces the system concept, Section IV details the circuit implementation, Section V presents simulated results and Section VI is the conclusion.

II. A Neural Prosthesis for Proprioception

A system providing proprioceptive feedback from a prosthetic arm (as indicated in Figure 1) could provide an amputee with a sense of motion and position from a prosthetic limb and greatly enhance their ability to control its movements. In order to make this feedback feel natural the system will aim to stimulate axons in the PNS carrying proprioceptive information from Golgi Tendon Organs and Muscle Spindles. In order to selectively stimulate a sufficient number of these axons we are planning to use an intrafascicular electrode with in the order of tens of active channels. An example of the type of suitable electrodes are the Transverse Intrafascicular Multichannel Electrode presented in [2] and we have therefore assumed a similar electrode impedance for the work presented here (6kΩ resistor in series with a 7nF capacitor).

III. System Concept

Power consumption in current-mode neural stimulation is typically dominated by the power used in the front-end to

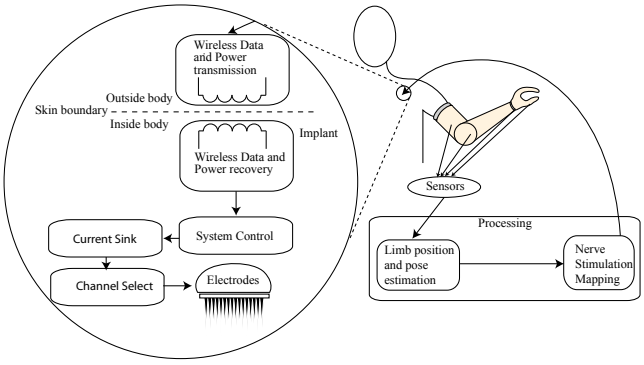
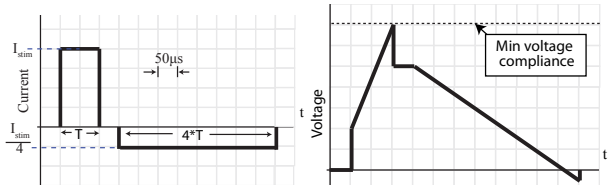
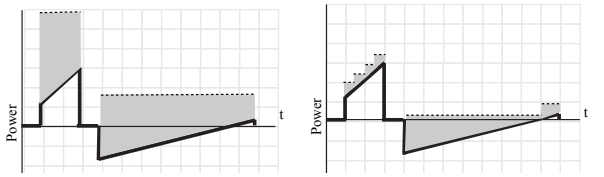


Fig. 1. Concept of neural prosthesis for proprioception



(a) Current waveform (b) Voltage across the electrode



(c) Power consumption in a typical stimulator (d) Power consumption in the proposed stimulator

Fig. 2. In (c) and (d) the dark line is the theoretical minimum power consumption, dotted line is the actual power consumption and the shaded area is the power wasted

drive the current flow (i.e. charge stimulus) into and out of electrodes. Kelly in [3] calculated that even using a *low power* current source, as much as 92% of the front end power is dissipated as heat by the current controlling transistors. The reason for this can be seen by looking at the voltages and currents associated with this proprioceptive stimulator.

Selective stimulation of efferent neurons (similar to the afferent Type Ia and Ib neurons we are targeting) in the human PNS has been demonstrated in [4], [5] to occur with charge packets of between 11±5nC to 29±17nC. Given these values our stimulator will be designed to deliver up to 50nC in a 100μs pulse (a common pulse duration). Using the chosen impedance mentioned in Section II the minimum voltage compliance of the system therefore needs to be 10.64V (calculated using: $I_{stim} \times R_{elec} + \frac{Q_{total}}{C}$, where I_{stim}, R_{elec}, Q_{total} and C are the stimulation current, electrode resistance, charge stimulus and capacitance respectively). This is just the peak voltage and for the vast majority of the time the system does not need to operate at this voltage (see Fig. 2(b)), however, a normal neural stimulator has fixed supplies and as such there is no option. This excess voltage leads to waste power (see Fig. 2(c)).

This paper discusses the application of Dynamic Voltage Scaling (DVS) to a neural stimulator to reduce power consumption by varying the power supply voltage as demonstrated in Fig. 2(d). An asymmetric waveform (Fig. 2(a)) with delay between the cathodic and anodic phases is used because it can reduce power consumption and has been shown to initiate action potentials at significantly lower charge thresholds [6].

IV. Circuit Implementation

The design was implemented in IBM 0.18μm HV CMOS technology. The outline stimulator design is shown in Figure 3. This consists of four main blocks: (1) the controller; (2) the DC-DC converter and comparator blocks; (3) the H-bridge (for current steering); and (4) the current generator.

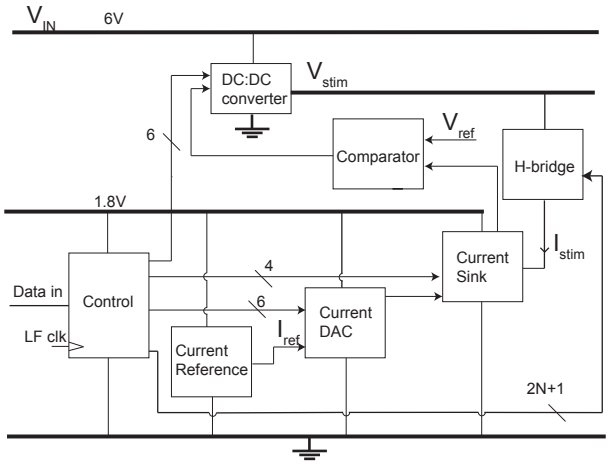


Fig. 3. Block-level system architecture

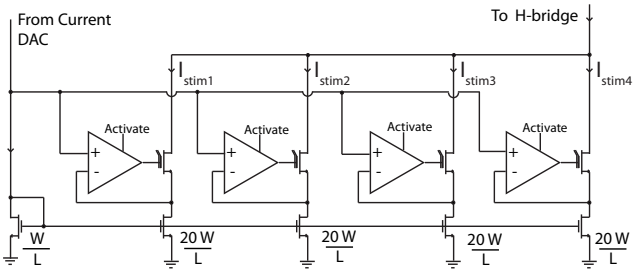


Fig. 4. The regulated-cascode current sink. Note that the cascoding transistor is a high voltage thin oxide device.

A. Controller

The stimulus output is defined by a 22-bit word, consisting of: channel selection (4-bit), stimulation current (6-bit) and two 6-bit clock frequencies (cathodic and anodic) for the DC converter. Once a control word is received, a stimulation cycle is initiated by enabling a synchronous counter. This counter provides the stimulation timing signals and enables/disables various sub-systems to reduce power consumption.

B. Current Generation

The current reference produces a stable 1.6μA current which flows into a 6-bit binary-weighted current-DAC which mirrors and amplifies the current according to the 6-bit stimulation level set within the control block. The gain of the DAC stage is between 0 and $3\frac{15}{16}$ and as such the output current is controllable in steps of 0.1μA up to 6.3μA.

The current generated by the DAC then flows into the front-end current sink that directly controls the stimulation current flow. The design of this block is shown in Fig. 4. It utilises four regulated-cascode current mirrors (with a W/L ratio of 1:20) to scale the DAC current by up to a factor of 80. Each folded cascode op-amp can be individually deactivated, thereby turning off the respective cascode device. During the cathodic stimulation phase all four op-amps are active providing the full factor of 80 gain, however, during the anodic stimulation phase only one of the op-amps is used and as such

the gain drops to a factor of 20. This provides the 4:1 ratio between the cathodic and anodic phases. The current sink is capable of sinking between 2μ and 504μA.

C. H-bridge

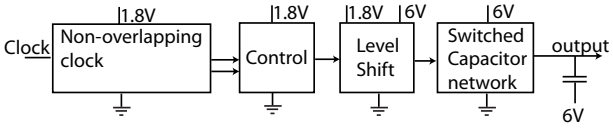
The current flowing into the sink is itself sourced through one of 16 parallel H-bridges which each have an electrode pair as their crossbar (similar to the approach described in [7]). This H-bridge topology enables a single-ended power supply to be used, and the same current sink to provide both the cathodic and anodic phases. Also because the H-bridge switches are individually controllable it enables a single current sink to selectively drive current through any of the 16 channels.

D. Charge Balancing

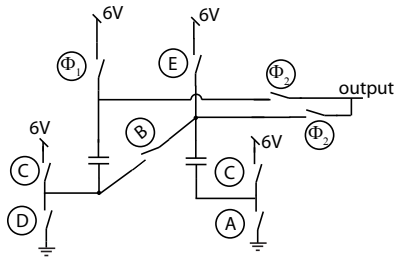
For a symmetrical biphasic waveform, accurate charge balancing is easily achievable in an H-bridge configuration because the same current sink is used for both phases and as such charge imbalance largely comes down to timing jitter, noise and any drift in the current sink output. This is a major advantage over non H-bridge designs which usually require calibration to achieve good matching of anodic and cathodic pulses. However, we are using an asymmetric waveform and as such both the H-bridge approach and normal current mirror calibration techniques are not directly applicable. Instead we propose that accurate charge balancing is achievable over a series of pulses rather than on a single pulse. Looking at Fig. 4, in the cathodic phase the total charge injected (Φ_c) into the electrodes will be: $\Phi_c = (I_{stim1}+I_{stim2}+I_{stim3}+I_{stim4})\times T$, where T is the cathodic phase duration. In the subsequent anodic phase, one of the regulated cascodes will be active for 4 times the duration and the charge removed from the electrodes will be (for example): $I_{stim2} \times 4T$. The 4 cascoded transistors are matched carefully so as to provide a certain level of charge balancing, but accurate charge balancing can be achieved if the op-amp activated in the anodic phase is changed sequentially for each stimulation. This is because over a series of 4 stimulations all the mirrors will have been active for the same amount of time *anodically* as they were *cathodically* and as such errors due to process variation and mismatch will cancel. The controller has a 2-bit counter for each channel that is incremented after each anodic stimulation to ensure that each op-amp is used in turn.

E. DC-DC converter

The core of this system is the DC-DC converter providing V_{stim}. This converter is a rapidly reconfigurable switched-capacitor network capable of outputting: 3V, 6V (input power supply), 9V and 12V. The DC converter operates in a free running mode whereby it starts outputting at 3V and automatically increases the output voltage during stimulation; if the cascode device (see Fig. 4) is forced away from its operating point. Monitoring of this operating point is achieved by comparing the output of the op-amps (i.e. the cascode device gates) with a reference voltage and when exceeded, the DC converter output voltage is raised.



(a) One phase of the DC converter



(b) Switched capacitor network

Fig. 5. Architecture and schematic of the DC-DC converter module

TABLE I
SWITCHING COMBINATIONS FOR THE DC-DC CONVERTER

Output voltage	Charging	Discharging
3V	ϕ_1, A, B	ϕ_2, A, D
6V	ϕ_1, ϕ_2	ϕ_1, ϕ_2
9V	ϕ_1, A, B	ϕ_2, C
12V	ϕ_1, A, E	ϕ_2, C

The implemented DC-DC converter is shown in Fig. 5(a). It uses two interleaved phases controlled by non-overlapping clocks and a reconfigurable switched-capacitor network (as shown in Fig. 5(b)). In total, it uses 900pF capacitance (implemented using dual-MIM capacitors) and operates at a maximum input clock frequency of 3.3MHz. Table I shows the various switching combinations utilised in the charging and discharging phases. Given that the load for this converter is a constant current, the optimum clock frequency (for efficiency and voltage ripple) for the converter is a fixed multiple of the stimulating current regardless of the output voltage. This clock frequency is set by the 6-bit input from the controller and is implemented using a 6-bit charge-based DAC and a voltage-controlled ring oscillator.

V. SIMULATION RESULTS

The circuit was simulated using foundry-supplied PSP models using Cadence Ultrasim and Spectre simulators. Fig. 6 shows an example transient response (output current, voltage across the electrode and output of the DC-DC converter) and indicates that current flow remains stable despite the changing output of the DC-DC converter.

The efficiency ranges of the DC-DC converter for various loads are as follows:

- At 3V: 63% - 68%
- At 6V: 92% and 100% (using input voltage supply)
- At 9V: 71%-76%
- At 12V: 69% - 73%

In order to benchmark the performance, the power consumption of a typical current-mode stimulator with fixed 11V supply is used. Fig. 7 illustrates how the energy used per

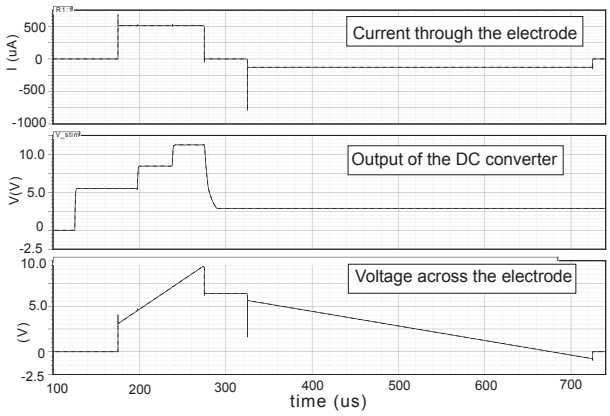


Fig. 6. Output waveforms for a maximum amplitude stimulation.

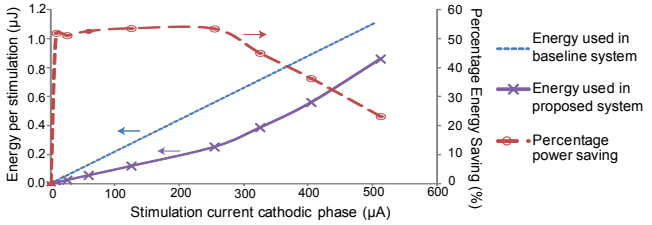


Fig. 7. Energy used per stimulation for the proposed and baseline system and percentage power savings

stimulation (for the full range of cathodic currents) varies for the baseline (typical current-mode) system and the system proposed here, as well as showing the percentage power savings that this proposed system achieves.

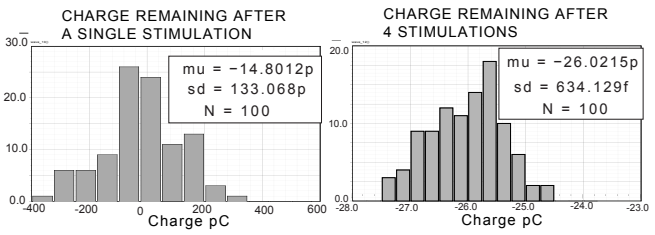


Fig. 8. Monte-Carlo simulations illustrating the net charge imbalance after delivery and removal of 50nC per stimulation

Monte-Carlo simulations were carried out with a fixed DC voltage source to ensure that the proposed charge balance approach was robust to process variation and mismatch. Fig. 8 shows charge imbalance after 1 and 4 stimulation cycles at maximum current.

VI. Conclusion

This work indicates that dynamic voltage scaling using switched capacitor DC-DC conversion can be employed on current-mode stimulation to achieve significant power savings across a wide range of stimulation currents and Table II shows how it compares to other low power approaches. Further, significant power savings should be possible by enabling V_{stim} to be set to $0V$ (ground) in the anodic phase and recovering

TABLE II
Comparison of results achieved by other low power neural stimulator designs.

	Arfin, S. K. and Sarpeshkar, R. [8]	Kelly, S.K. and Wyatt, J.L. [3]	This work
Dynamic range	0–450 μA	136μA	0–504μA
Stimulus control	Current control	Voltage control	Current control
Power savings*	58–62%	53%–66%	23% – 53.5%
External components	Yes	Yes	No
Charge balanced	No	No	Yes

**Power savings relative to a typical current controlled stimulator*

energy stored in the electrode capacitance, however, this remains an area for future work. The output currents (as seen in Fig. 6) are stable and show that the DC-DC converter has minimal impact on current stimulus output. The voltage ripple on the output of the converter does cause some current ripple through the electrodes but this is less than 0.5μA (peak-to-peak) at the maximum stimulation current. Furthermore, this is at the DC-DC converter clock frequency (i.e. between 50kHz - 3.3MHz) and is thus unlikely to have a physiological impact on stimulation. In IBM 0.18μm HV CMOS technology it is estimated to occupy an area of approximately 0.9mm^2. The Monte-Carlo simulations indicate that the charge imbalance is less than 0.83% of charge delivered for a single stimulation (at $\pm 3\sigma$) and less than 0.014% for a series of stimulations.

Acknowledgment

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