A Novel Charge-Metering Method for Voltage Mode Neural Stimulation

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***Abstract*—This paper presents a novel, fully-integrated circuit for achieving change-balanced voltage-mode neural stimulation based on a charge-metering technique. The proposed system uses two small on-chip capacitors, a counter, two comparators and a control-logic circuit to measure the charge delivered to the tissue. This has been designed to deliver a maximum charge stimulus of 10.24 nC within 100 μs. Simulated results show a charge delivery error of 0.4-4% and a maximum residual charge of −73 pC. Implemented in 0.18 μm CMOS, the total power consumption is 42 μW.**

I. Introduction

Electrical Neural Stimulation (ENS) provides a means of effectively interfacing to sensory and cognitive pathways within the human nervous system, in particular for neuro-rehabilitation applications. This technique has already demonstrated a significant impact in neuroprosthetics by improving the quality of life in individuals with neural damage or dysfunction. For example, to date over 219,000 people with profound hearing impairment have and are benefiting from cochlear implants [1], with a further 80,000 with cognitive disorders (such as Parkinson's and dystonia) benefitting from deep brain stimulation therapy [2].

Fundamentally, ENS is based on injecting charge extracellularly (to the neuron) to evoke action potentials (AP) as a means of modulating the spike rate. The charge is delivered through electrodes positioned in close proximity to the target site (neuron somas or neural tissue) using one of three typical methods: Current-Mode Stimulation (CMS) [3], Voltage-Mode Stimulation (VMS) and Charge-Mode Stimulation (ChgMS) [4]. In CMS, the charge is delivered by a constant current source with its quantity being controlled easily by setting the duration, but a voltage headroom must be maintained to ensure the output transistor is in saturation. In VMS, a constant voltage source is used, eliminating this constraint of voltage headroom but control is required to set the charge quantity. ChgMS provides a trade-off between these, by using a capacitor to set the charge, but typically requires large and therefore off-chip capacitors.

To achieve safe ENS, it is essential to recycle the charge precisely. Any residual charge can form a DC voltage across the electrode-electrolyte-tissue double layer capacitance, causing redox reactions [5] that lead to electrode degradation and tissue damage. Typically, this is achieved by using a biphasic waveform, with a cathodic phase to first deliver the stimulus, followed by an anodic phase for charge-balancing. Fig. 1 shows a typical waveform in CMS [3], [6]. In practice it is challenging to achieve a perfectly balanced biphasic delivery due to circuit non-idealities such as mismatch and non-linearities. To date, most work has concentrated on achieving good charge-balancing for CMS [7], [8] but limited progress for VMS. One approach for VMS, however, uses a sense resistor to monitor the stimulation current and track the charge so as to control the balance pulse [9].

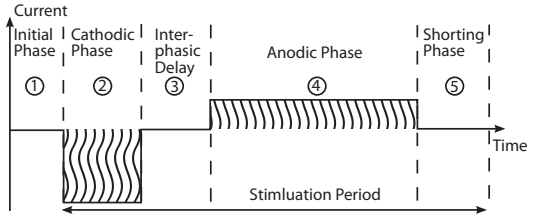

Fig. 1. Typical current mode stimulation waveform with a zero net charge, i.e. the cathodic and anodic shaded areas should be equal (and opposite).

This paper proposes a novel method for charge-metered VMS that achieves good charge balancing. Section II describes the concept and architecture of the proposed system. Section III and Section IV detail the circuit implementation and simulations. Section V concludes the paper.

II. System Overview

The system architecture is shown in Fig. 2. It can be divided into two sub-systems: an analogue front-end, responsible for charge sensing, and the digital back-end, responsible for charge measuring and system control. The target stimulus is set by the controller (user programmed) that sequences the switches to deliver the stimulation current via two paths

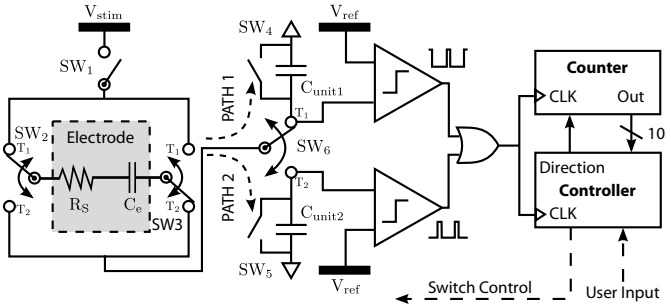

Fig. 2. System Architecture of the charge-metering system. (R_S represents the tissue spreading resistance and C_e the electrode-electrolyte-tissue double layer capacitance)

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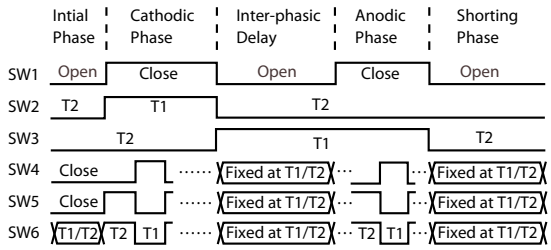

Fig. 3. Timing diagram of the 6 switches for the charge and discharge paths

formed by C_{unit1} and C_{unit2}.

Similar architecture is used in [10] to measure the current in the frequency domain.

A. Principle of Operation

The method proposed for charge-metering is based on integrating the stimulation current using the two capacitors. For instance, in *Path 1*, the maximum amount of charge stored on C_{unit1} is $C_{unit1} \times V_{ref}$. During the charging phase, once this amount is achieved, a pulse is issued by the comparator to the controller to discharge C_{unit1} completely. This charge and discharge sequence is repeated continuously under the control of the controller. The amount of charge delivered in each charge-discharge cycle is referred to as the *unit charge*.

It should be noted that *Path 1* will be broken during the discharge of C_{unit1} to prevent the stimulation current bypassing C_{unit1}. However, the break is undesirable as its physiological effect is unknown. Therefore, the circuit is replicated such that a second current path (*Path 2*) operates in a complementary fashion such as to maintain a continuous current flow.

If V_{ref} = 1V, the *unit charge* quantitatively equals to the value of C_{unit1} and C_{unit2}. From hereon, these two capacitors will be referred as the *unit capacitors* (C_{unit}). Each *unit charge* delivered to the electrode is counted and thus the total charge (Q_{total}) delivered can be determined by:

$$Q_{total} = \sum_{1}^{N} C_{unit} \times V_{ref} \quad (1)$$

Where N is the output of the counter.

The system comprises of 6 switches that control charge delivery/recycling: SW_1 enables both paths; SW_{2-3} determines the polarity of the stimulus and are used to short the electrodes; SW_{4-5} are used to discharge the *unit capacitors*; SW_6 steers the stimulation current between *Path 1* and *Path 2*.

B. Detailed Sequence

The system generates the biphasic stimulus (e.g. as Fig. 1) using five phases as described below. The timing diagram for the 6 switches during the 5 phases is shown in Fig. 3.

1) Initialisation Phase: The system is reset and the *unit capacitors* are discharged whilst V_{stim} is disconnected.

2) Cathodic Phase: The charge is delivered by continually alternating between *Path 1* and *Path 2*, whilst being metered by the counter. Once a pulse is signalled from the comparators, SW_{4-6} toggle, steering the path. During this phase, the counter counts upwards till the user-defined value is reached.

3) Inter-phasic Delay: A short delay is introduced between the cathodic and anodic phases to avoid blocking the propagation of the AP recruited [3]. SW_1 is set open to break both paths. The other switches are set as for the anodic phase.

4) Anodic Phase: The previously delivered charge is recycled. The operation is similar to that of cathodic phase, with SW_2 and SW_3 inverted and the counter down counting until reaching zero.

5) Shorting Phase: Any residual charge is removed here by shorting the electrode. The duration is determined by the repetition rate of the stimulus.

The stimulus parameters can be programmed as follows: the quantity of charge delivered is set by the limit of the counter; the stimulation rate by V_{stim}, and the length of inter-phasic delay is defined within the controller.

III. Circuit Implementation

The circuit has been implemented in *Austriamicrosystems* 0.18μm 1P4M CMOS technology. This section details specific design aspects of the circuit implementation.

A. Switch Design

All the switches are implemented using transmission gates with equal device sizes (W/L=10 μm/0.18 μm) for both PMOS and NMOS. Each Single Pole, Double Throw (SPDT) switch ($SW_{2,3,6}$) is implemented using two transmission gates. Switch charge injection is not expected as a challenge because: (1) transmission gates significantly reduce any switch-related charge injection; (2) the symmetry between switches in *Path 1* and *Path 2* ensures any injected charge is recycled; (3) all switches are present within the stimulation path, any charge injection is metered and therefore eliminated.

B. Unit Capacitor Selection

The unit capacitance value is a crucial design parameter. It not only defines the measurement resolution but also sets the scale and power requirement of the system. A smaller C_{unit} is preferable for a finer resolution and an reduced area, however this is at the expense of an extended counter resolution (for a fixed charge range). In turn, this requires the counter to operate at a higher frequency as C_{unit} is charged and discharged faster. Therefore, there is a power/area/resolution trade-off.

The unit capacitance selected here is C_{unit} = 10 pF, providing a charge resolution of 10 pC. With a 10-bit counter, a maximum charge of 10.24 nC can be delivered, meeting the requirement for intra-cortical stimulation for human vision prosthetics [11]. The time constant for charging C_{unit} is:

$$\tau \approx R_s \times (C_e^{-1} + C_{unit}^{-1})^{-1} \quad (2)$$

Where C_e is the electrode-electrolyte-tissue double layer capacitance (in the order of 10-100 nF) and R_s (the tissue impedance) is in the order of 10s of kΩ. Therefore the overall capacitance is determined by C_{unit}. This sets the time constant τ to be approximately 100 ns and the operating frequency of the digital controller to be approximately 10 MHz.

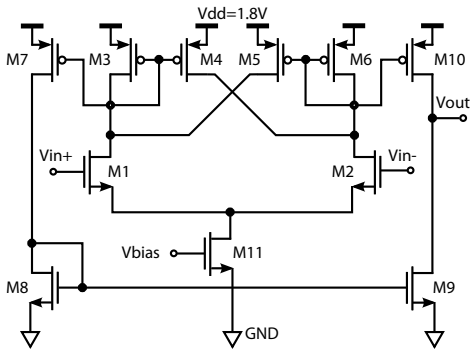

Fig. 4. Schematic of the comparator

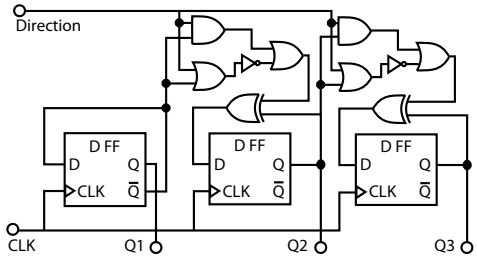

Fig. 5. Schematic of the bi-directional counter (first 3-bits shown)

C. Comparator

The comparator is shown in Fig. 4. A regenerative load is used to increase the gain. The strength of positive feedback formed by M5 and M6 is given by $\alpha = \frac{(W/L)_5}{(W/L)_6} = 1$. This means the comparator works as a latch. Since the load of the comparator is an OR gate whose input capacitance is ≈2 fF, the delay is limited mainly by the parasitic capacitance observed at the drains of M1 and M2. In order to minimise this parasitic capacitance and thus reduce power consumption, $(W/L)_{1-6}$=1 μm/1 μm, $(W/L)_{7,10}$=0.4 μm/1 μm. The bias current is set to 6μA (determined through simulation) such that the delay is around 10 ns. Although the output swing of the comparator is limited by the headroom of the output transistors, a full swing can be achieved at the output of the OR gate.

D. Counter

As previously mentioned, a 10-bit up/down binary counter is used to record the charge delivered. The circuit comprises of 10 flip-flops with supporting combinational logic. Fig. 5 shows the first 3-bits for illustration. The counter operates synchronously and counts upwards when *Direction* is HIGH and downwards when LOW. Although the counter operates at around 10 MHz, as not all the gates/flip-flops are working simultaneously, the average power consumption is relatively negligible (in comparison to the comparator).

E. Controller & V_{ref}

The controller is implemented using a Finite State Machine to achieve the operating sequence described in Section II-A.

V_{ref} sets the threshold of the voltage on the *unit capacitors*. Although it can be set by a predefined bias voltage (eg. 1 V), as the control loop has a delay of approximately 10 ns, it will cause the unit capacitors to be charged slightly above the target. This means the amount of charge delivered will be slightly higher than targeted, degrading the accuracy of the system. Therefore V_{ref} should be made tunable as this delay varies with process variation and mismatch. In a future implementation, a predictive comparator [12] could be used to automatically generate this threshold for the comparators.

IV. Simulation Results

The circuit has been simulated using Cadence Spectre 5.1.41ISR2 with foundry-supplied PSP-models.

A. Test Setup

V_{stim} is set to 1.8 V, the typical supply voltage for a 0.18μm CMOS technology. C_e and R_s are set to 100 nF and 10 kΩ respectively, based on values modelled for a platinum electrode with a diameter of 430μm [13]. V_{ref} is set to 920 mV to compensate the delay of the control loop (determined through simulations). For proof-of-concept and future *in-vitro* tests, the voltages on the *unit capacitors* are monitored so as to calibrate the system. The simulations include all the charge injection effect of the switches.

B. Charge-Metering & Recycling

Simulations are carried out to characterise the performance of charge-metering and recycling. The first test is to characterise the error in charge delivery and residual charge against the target. The results are shown in Table. I. The delivered charge and residual charge are calculated by integrating the stimulation current. As an example, Fig. 6 shows the transient results of the stimulation current and voltage across the model for 10 nC run. The delivered charge and residual charge is calculated to be 10.04 nC and -70.33 pC respectively.

The *unit charge* comprises of a fixed part set by V_{ref} and a variable part set by the control loop delay and stimulation current. Therefore there is an error (δ) between the quantities of unit charge and the target charge.

$$\delta = Q_{\text{Unit Charge}} - Q_{\text{Target Charge}} \tag{3}$$

Since the delay is fixed and the current is determined by $(V_{stim} - V_{C_e})/R_S$ (V_{C_e} is the voltage on C_e), $Q_{\text{Unit Charge}}$ and thus δ decreases as V_{C_e} increases. As a result, the *charge delivery differences* (the accumulation of δ) increases with the *target charge* but drops after reaching 10 nC since δ becomes negative. This also happens during charge recycling with a different value of δ as the initial condition (V_{C_e}) is different. Therefore, the residual charge increases with the target charge.

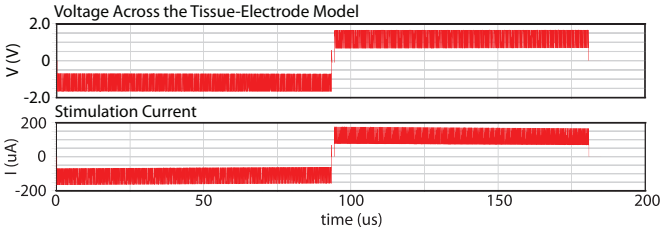

Fig. 6. Stimulation voltage and current across the tissue-electrode model for a 10 nC stimulus

Target Charge (nC)	10	9	8	7	6	5	4	3	2	1	0.01
Delivered Charge (nC)	10.04	9.072	8.067	7.061	6.054	5.047	4.039	3.031	2.021	1.011	0.0104
Residual Charge (pC)	-70.33	-56.91	-45.32	-34.25	-25.05	-17.25	-10.887	-5.94	-2.4	-0.3057	0.3011
Charge Delivery Difference (nC)	0.04	0.072	0.067	0.061	0.054	0.047	0.039	0.031	0.021	0.11	0.0004
Charge Delivery Error (%)	0.40	0.80	0.84	0.87	0.90	0.94	0.97	1.03	1.05	1.10	4

TABLE I
ACTUAL DELIVERED CHARGE AND RESIDUAL CHARGE FOR DIFFERENT CHARGE REQUIREMENTS

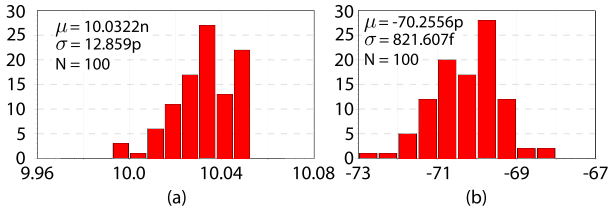

Fig. 7. Monte-Carlo analysis for: (a) charge delivered, and (b) residual charge

The *charge delivery error* is the *charge delivery difference* divided by the *target charge* and thus decreases with increasing target charge. The best and worst cases are 0.4% and 4% respectively, and although the worst case is 4%, this happens only at the minimum scale, i.e. for delivering a *unit charge* with the *charge delivery difference* of just 400 fC.

The second test is to investigate the effect of process variation and device mismatch. For this, a 10 nC stimulus was selected because this has the largest *residual charge* and longest counting process for δ to accumulate. Fig. 7 shows the results of a Monte-Carlo analysis. After considering the 6σ range, the charge delivery error and charge imbalance for that run is approximately 0.7% and 0.73% respectively. Therefore, the system is relatively insensitive to mismatch (as expected) due to the fact that the core circuit is digital.

C. Physiological Effect

It is expected that the observed ripple on the stimulation current (see Fig. 6) will not cause any undesirable physiological effects ([14] observed a similar ripple). To evaluate the physiological effect of this stimulus, the current waveform is applied to neuron model (Hodgkin-Huxley model implemented in Matlab). Comparing the response to a current stimulus with and without the ripple, shows no difference in the neural behaviour. The reason is that the ripple has a much more smaller time constant (90ns) than that required for sodium channel activation (100-200 μs) [15].

D. Power Consumption

The complete system consumes a power of 42 μW (excluding stimulus), of which the comparators consume 30 μW and the counter consumes 4.98 μW. The comparator consumption is limited by the requirement to reduce the delay. This could be reduced using a predictive comparator [12] but is outside the scope of the current design.

V. CONCLUSION

This paper has presented a novel method for charge-balanced VMS using charge-metering. The system architecture and circuit implementation have been presented with the key design considerations. The circuit achieves a maximum charge delivery of 10.24 nC with a resolution of approx. 10 pC. Simulations including charge injection effect show a charge delivery error of 0.4-4% with a maximum residual charge of -73 pC. The total power consumption is 42 μW. The circuit performance is compared to the state-of-the-art in Table. II.

TABLE II
PERFORMANCE COMPARISON WITH EXISTING WORK

	This work	[7]	[8]	[9]
Residual Charge(pC)	-70	120	<5000	8
Full-scale Current	-	10 mA	1 mA	-
Full-scale Charge(nC)	10.24	-	-	-
Resolution (pF)	10.4	-	-	250
Charge Delivery Error	0.4-4%	-	-	0.5%
Voltage Rails (V)	1.8	+6, -9	3.3, 22.5	1.8/3.3
Power Consumption	42 μW	47 μW	198 μW	50 μW
CMOS Technology	0.18μm	0.7μm HV	0.35μm HV	0.18μm

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