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Journal of The Electrochemical Society, 148 (7) G370-G374 (2001)
0013-4651/2001/148(7)/G370/5/$7.00 © The Electrochemical Society, Inc.

150°C Amorphous Silicon Thin-Film Transistor Technology for Polyimide Substrates

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We have developed a 150°C technology for amorphous silicon thin-film transistors (a-Si:H TFTs) on polyimide substrates deposited by plasma enhanced chemical vapor deposition. The silicon nitride gate dielectric and the a-Si:H channel material were tailored to provide the least leakage current and midgap defect density, respectively. In addition, we conducted experiments on the TFT structure and fabrication with the aim of obtaining high electron mobility. TFTs with back-channel etch and channel-passivated structures were fabricated on glass or 51 μm thick polyimide foil. The a-Si:H TFTs have an on/off current ratio of $\sim 10^7$ and an electron mobility of $\sim 0.7\ cm^2/V\ s$.
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Manuscript submitted July 20, 2000; revised manuscript received March 1, 2001. Available electronically May 30, 2001.

Plastic substrate films for active electronic circuits are attracting increasing attention. Circuit fabrication processes must not exceed the glass transition temperature of the substrate. At present, the principal materials technology for thin-film transistors (TFTs) is based on silicon. We have been developing an amorphous silicon (a-Si:H) based TFT process with 150°C maximum temperature for compatibility with flexible polyimide foil substrates. A key component of the process is the deposition of the silicon nitride (SiN_x), which serves as the passivation layer for the substrate and as the gate dielectric. In conventional a-Si:H TFT fabrication, the SiN_x is deposited at 300-350°C, which is the highest temperature step in the entire process and is needed to ensure low gate leakage current. Reduction of the SiN_x deposition temperature from 350 to 150°C, while retaining low gate leakage, is a serious challenge.

Plasma enhanced chemical vapor deposition (PECVD) is the standard technique for the fabrication of a-Si:H TFTs. A number of authors have reported silicon nitride films deposited by PECVD at a temperature lower than 250°C,[1-10] but only a few studies were aimed at process optimization.[8-10] Encouraged by the rapid growth of the liquid crystal display industry, several groups have worked on adapting the currently practiced a-Si:H TFT technology to various plastic substrates[11-16] by reducing the deposition temperature. In this paper we summarize the results of the optimization of PECVD silicon nitride deposition at 150°C using primarily the leakage current as the quality criterion, and show that high quality a-Si:H TFTs can be fabricated at this temperature.

Silicon Nitride Deposition and Experimental Results

The SiN_x films were deposited from mixtures of SiH_4, NH_3, and H_2 using 13.56 MHz PECVD at a pressure of 500 mTorr (∼67 Pa). All layers were deposited at 150°C and the silane and ammonia flows were kept constant at 5 and 50 standard cubic centimeters per minute (sccm), respectively. We varied the H_2 flow rate from 55 to 220 sccm and the plasma power from 5 to 50 W. The electrode area was $\sim 250\ cm^2$. Each layer was simultaneously deposited on a clean Corning 7059 substrate (for optical measurements), on Corning 7059 coated with Cr (for electrical measurements,) and on a p-type Si wafer of [111] orientation (for infrared measurements). Most of the films were around 0.5 μm thick. We measured the growth rate, the index of refraction n (from optical transmission measurements using the Swanepoel method[17]), the leakage current through the nitride [from current-voltage (I-V) curves taken from −100 to +100 V], the dielectric breakdown field, the dielectric constant ϵ at 1 MHz (from C-V measurement of $Cr/SiN_x/Cr$ structures), the etch rate in 10:1 buffered oxide etch,[18] (10:1, with surfactant, complementary metal oxide semiconductor) the Fourier-transform infrared absorption (FTIR) spectrum, the Rutherford backscattering (RBS) spectrum, and the secondary ion mass spectrum (SIMS).[d] Selected SiN_x recipes were then tested by fabricating inverted staggered a-Si:H TFTs with either the back-channel etch or the SiN_x channel-passivated structure.

Figure 1 shows the SiN_x growth rate and the index of refraction as functions of hydrogen dilution and power. Figure 1a depicts the variation in these parameters for the radio frequency (rf) power of 5 W and a hydrogen flow from 55 to 220 sccm. Adding more hydrogen reduces the growth rate from ∼1.6 to ∼1.1 Å/s and increases the index of refraction from 1.75 to 1.79. Figure 1b shows the deposition rate and index of refraction as functions of rf power for the hydrogen flow rate of 165 sccm. An increase in the rf power from 5 to 20 W causes an increase in the growth rate from 1.2 to 2.1 Å/s and a slight increase in the index of refraction from 1.79 to 1.80. The bottom graph, Fig. 1c, shows the same parameters for the highest hydrogen flow of 220 sccm and a large variation in rf power from 5 to 50 W. Over this power range, the deposition rate increases from 1.1 to 2.9 Å/s and the index of refraction increases slightly from 1.79 to 1.81, both with increasing power.

Figure 2 correlates the dielectric constant ϵ, calculated from capacitance-voltage (C-V) curves measured at 1 MHz, and the etch rate in 10:1 buffered oxide etch[18] with hydrogen flow and deposition power. As the hydrogen flow increases, the etch rate drops dramatically from 412 to 96 Å/s, indicating that the most dense films are deposited with the highest hydrogen flow. The dielectric constant of ∼6.85 does not change much with hydrogen flow rates between 55 and 110 sccm, but for larger hydrogen flows it increases to a value of 7.38. With an increase in the rf power from 5 to 20 W, there is a large increase in ϵ from 7.14 to 8.49 and a decrease in the etch rate from 172 to 73 Å/s, again indicating that denser films are deposited at higher power. For the highest hydrogen flow, the etch rate and the dielectric constant do not vary much in the rf power range from 5 to 50 W. Up to 40 W, the dielectric constant varies between 7.29 and 7.44 and reaches a value of 8.18 for the power of 50 W. The etch rate drops slightly between 5 and 20 W; above that, it remains constant at a value of about 65 Å/s.

All films were tested in a sandwich configuration for leakage current and the dielectric breakdown field. The maximum voltage applied to the samples was 100 V. No major differences were observed in the leakage current, which varied from 20 to 30 pA at 100 V. All films easily withstood the applied electric field and in all

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[d] Analysis performed by Evans East, Plainsboro, New Jersey.

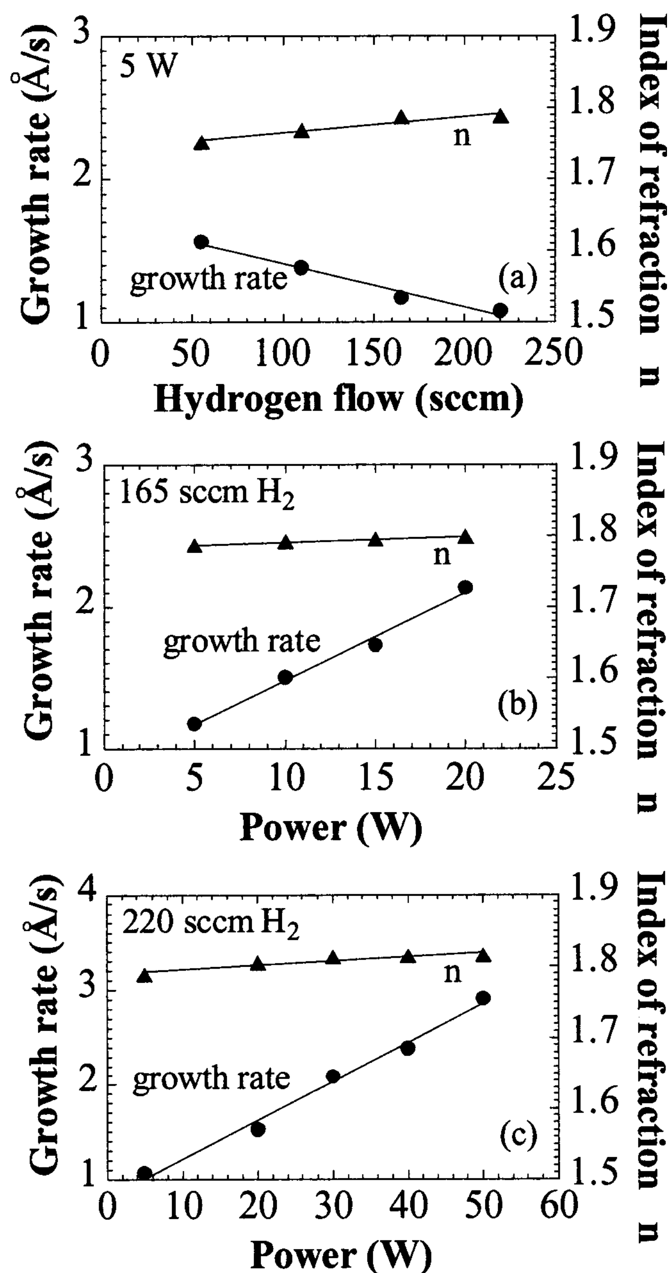

Figure 1. Growth rate and index of refraction of SiN_x films as functions of rf power and hydrogen flow during the 150°C PECVD deposition.

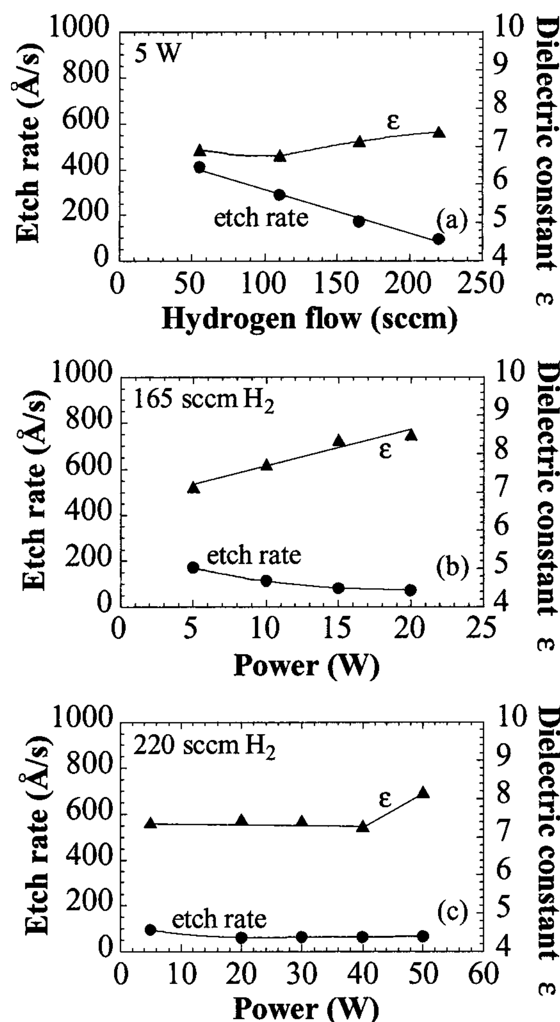

Figure 2. Etch rate and dielectric constant of SiN_x films as functions of rf power and hydrogen flow during the 150°C PECVD deposition.

cases the breakdown field was larger than 2 MV/cm.

Figure 3 summarizes the FTIR absorption spectra for experimental conditions identical to those of Fig. 1. The IR scans of the background and of the substrate were subtracted from all spectra. The main vibrational bands are as follows: N-H stretching band around 3340 cm^{-1}, Si-H stretching band around 2170 cm^{-1}, N-H_2 scissors around 1550 cm^{-1}, a band around 1190 cm^{-1}, and the Si-N stretching band around 890 cm^{-1}. While the size of most IR bands does not vary much with changing hydrogen flow or rf power, the Si-H stretching band at 2170 cm^{-1} decreases with both increasing hydrogen flow and increasing rf power.

Figure 4 summarizes the results on the Si/N ratio measured by RBS, and on the hydrogen concentration from SIMS, for selected samples. The value of Si/N for a stoichiometric film is 0.75. All measured films are nitrogen rich and the Si/N ratio varies between 0.56 and 0.67. As the hydrogen flow increases, the films become more ''silicon rich'' with higher values of Si/N. The dependence of the Si/N ratio on power is more complicated and appears to reach maximum of 0.67 at the rf power of about 20 W. The SIMS measurements reveal that the hydrogen content remains nearly constant at a value of 2×10^{22} cm^{-3} in the tested interval of hydrogen flow and rf power.

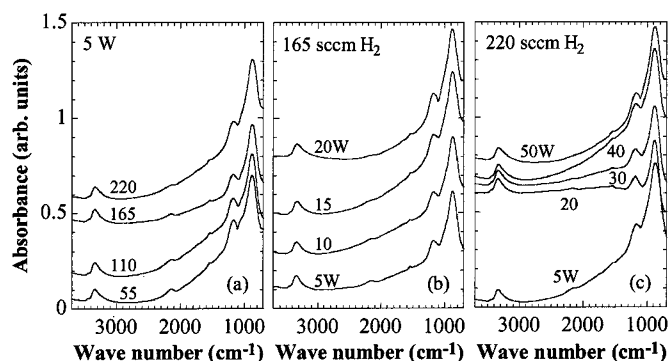

Figure 3. Infrared spectra of SiN_x films deposited over a range of rf power and hydrogen flow. (a) Hydrogen flow varied from 55 to 220 sccm, (b) rf power varied from 5 to 20 W, and (c) rf power varied from 5 to 50 W.

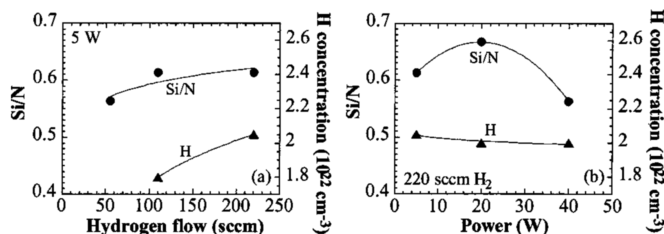

Figure 4. Si/N ratio (RBS) and H concentration (SIMS) for selected PECVD SiN_x films deposited at 150°C.

Optimized Low Temperature Silicon Nitride

Device quality SiN_x gate dielectric deposited at the standard temperatures of 300-350°C usually is slightly nitrogen rich. Nitrogen rich SiN_x results in better TFT characteristics and is more stable than silicon rich SiN_x.[19] Nitrogen rich SiN_x contains a large amount of hydrogen, 20-35 atom %, with the larger fraction bound in N-H groups.[20] The threshold voltage of the TFTs is lowest when the refractive index of the SiN_x layer lies in the range of 1.85 to 1.90.[21] The index of refraction is related to the stoichiometry of the film, being larger for silicon rich films.[22] The etch rate in 10:1 buffered HF[18] usually has a value of 20 Å/s.[23] It decreases rapidly with increasing index of refraction, n, up to the value of about 1.83 and remains constant for higher values of n.[2] The etch rate has been reported to rise with increasing concentration of bonded hydrogen in the film.[22]

Based on the knowledge collected from the SiN_x films deposited at 300-350°C, the low temperature film should be slightly nitrogen rich with low hydrogen content, low etch rate, high dielectric breakdown field, index of refraction of about 1.85, and preferably high growth rate. Figure 5 shows a strong correlation between the etch rate in 10:1 buffered HF[18] and the index of refraction n for our 150°C SiN_x layers. This dependence is qualitatively (but not quantitatively) similar to the one observed in high temperature SiN_x, which is represented by the dashed line in Fig. 5.[2] At low n, the etch rate decreases linearly with increasing index of refraction and it remains almost constant for $n \geqslant 1.80$. Following upon the above mentioned requirements, the SiN_x layer deposited from the gas mixture of 5 sccm of SiH_4, 50 sccm of NH_3, and 220 sccm of H_2, at the power of 20 W fulfills these requirements best. This film has a growth rate of 1.5 Å/s, etch rate of 61 Å/s, $n = 1.80$, dielectric constant $\epsilon = 7.46$, dielectric breakdown field >3.4 MV/cm, Si/N ratio of 0.67, and H content of $\sim 2 \times 10^{22}$ cm^{-3}.

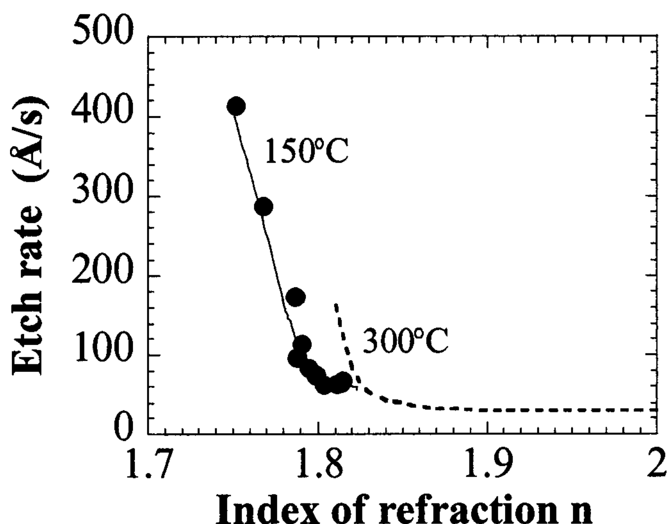

Figure 5. Etch rate as function of index of refraction for all SiN_x layers deposited at 150°C. The dashed line, corresponding to SiN_x deposited at 300°C,[2] is plotted for reference.

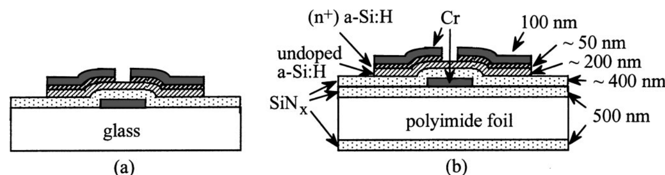

Figure 6. Schematic cross-sectional view of TFT on (a) Corning 7059 glass, and (b) Kapton. Note the SiN_x passivation of the polyimide substrate.

Back-Channel Etch a-Si:H TFTs

We fabricated a series of back-channel etch a-Si:H TFTs by depositing at 150°C on Corning 7059 glass or 51 μm thick Kapton E substrate using a three-chamber PECVD system.

Their cross-sectional views are shown in Fig. 6. First, the polyimide substrate was coated on both sides with a 0.5 μm thick layer of SiN_x, which serves as a diffusion barrier (against outgassing from the polyimide) and as an adhesion layer for the TFT structure. All TFTs had the following structure: ~100 nm thick Cr layer as gate electrode, ~400 nm of gate SiN_x, ~200 nm of undoped a-Si:H, ~50 nm of (n^+) a-Si:H, and ~100 nm thick Cr layer for the source/drain. The fabrication details are given elsewhere.[24] The channel length was $L = 15$ μm and width $W = 210$ μm. Using an identical recipe for all transistors, the undoped a-Si:H was deposited from a mixture of SiH_4 and H_2, and the (n^+) a-Si:H from a mixture of SiH_4, PH_3, and H_2. The optimized 150°C SiN_x recipe was used for TFTs deposited on both polyimide and glass, for comparison. Two other sets of TFTs with different SiN_x layers were deposited on glass. For both sets, the gas flow rates during the SiN_x deposition were identical to the optimized recipe, but the rf power was reduced to 15 or 10 W.

The TFT transfer characteristics of a transistor deposited on a polyimide substrate are shown in Fig. 7a. The source/drain current, I_{ds}, as a function of the source/drain voltage V_{ds} for nine different gate voltages V_{gs} is shown in Fig. 7b. The off current is $\sim 1 \times 10^{-12}$ A ($<1 \times 10^{-14}$ A/μm) and the on/off current ratio is $>10^7$. At $V_{ds} = 0.1$ V, we obtain a threshold voltage $V_T \sim 3.5$ V and a value of ~ 0.5 cm^2 V^{-1} s^{-1} for the linear mobility. Except for the slightly lower mobility, all other values are comparable to those of a-Si:H TFTs fabricated on glass substrates at temperatures between 250 and 350°C.[13]

Figure 8 summarizes results of all fabricated TFT sets. The off current I_{off}, the on current, I_{on}, and the gate leakage current, I_{leak}, are plotted as functions of the rf power applied during the gate SiN_x growth. The definition of these currents is as follows: the off current is the smallest source/drain current at $V_{ds} = 10$ V, the on current is the source/drain current for $V_{ds} = 10$ V and $V_{gs} = 20$ V, and the leakage current is the source/gate current for $V_{ds} = 10$ V and $V_{gs} = 20$ V. I_{leak} and I_{off} do not vary much among different SiN_x recipes, even though the TFTs on the polyimide have slightly lower leakage and off currents. The on current has a maximum around 15 W and at 20 W it is slightly higher for TFTs on polyimide than on glass. These differences might be related to a slight variation in the dielectric constant and/or the thickness of the SiN_x layers.

a-Si:H TFTs with Channel Passivation

Next, we chose a different structure for the a-Si:H TFTs, one where the channel area is passivated with a SiN_x layer. The cross-sectional view of this structure is shown in Fig. 9. This structure allows one to reduce the thickness of the a-Si:H channel layer while protecting the channel from the environment. All TFTs were deposited on Corning 7059 glass at 150°C using the same recipes as

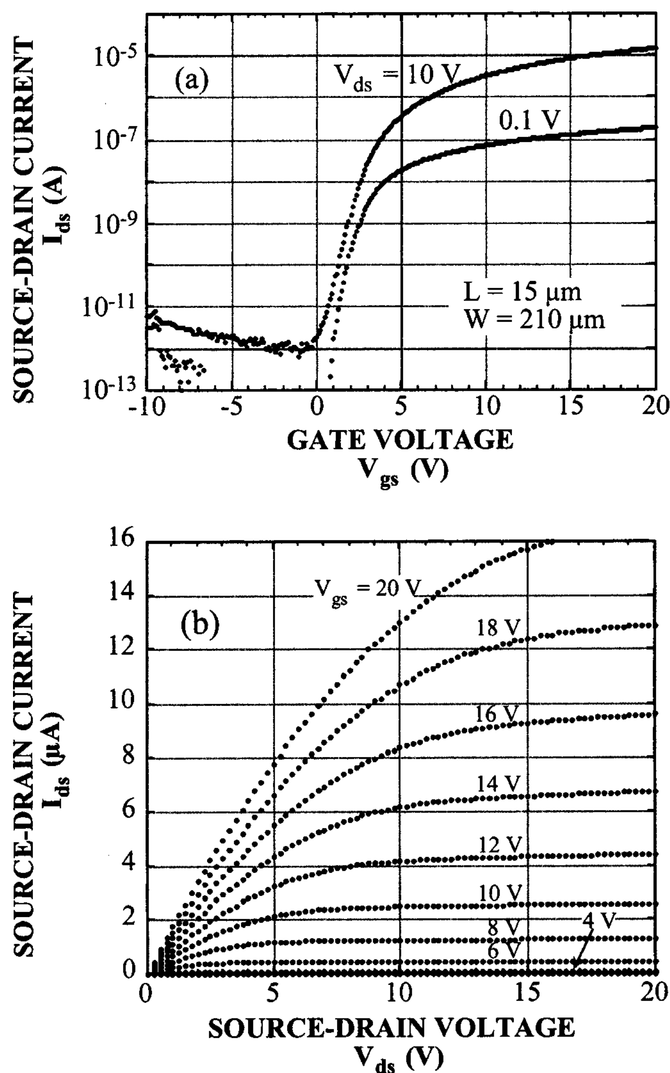

Figure 7. (a) Source/drain current as a function of gate voltage for V_{ds} = 0.1 and 10 V. The source electrode is grounded. The substrate is 51 μm thick polyimide. (b) Source/drain current as a function of source/drain voltage for V_{gs} from 4 to 20 V.

before. The SiN_x layer was deposited using the optimized recipe. In some TFTs, we varied the amount of the hydrogen flow for either the SiN_x or the a-Si:H layer next to the SiN_x/a-Si:H interface, thus modifying the interface layer to a depth of about 20 nm. The TFT channel length was 40 μm and channel width was 400 μm. The gate dielectric was ~360 nm thick and the channel layer was either 100 or 200 nm thick. After fabrication, the transistors were annealed at ~150°C for 30 min in forming gas to anneal out the radiation damage caused by reactive ion etching.

Figure 10 shows the transfer characteristics for all TFTs. TFT of Fig. 10a is similar to the back-channel etch TFT in which the SiN_x layer was deposited at 20 W, but the channel now is passivated. For the TFT of Fig. 10b, the thickness of the a-Si:H channel layer is reduced to 100 nm, which is half of that of TFT of Fig. 10a. The transfer characteristics of Fig. 10c correspond to TFTs in which the thickness of a-Si:H layer is 100 nm, but the first 20 nm (next to the SiN_x layer) were modified during growth by doubling the hydrogen flow. In Fig. 10d, the thickness of a-Si:H layer is again 100 nm, but the last 20 nm of SiN_x layer (next to the a-Si:H layer) were modified during growth by increasing the hydrogen flow to 330 sccm.

As expected, the off current is reduced by a factor of two when the channel layer thickness is reduced to one-half. The calculated

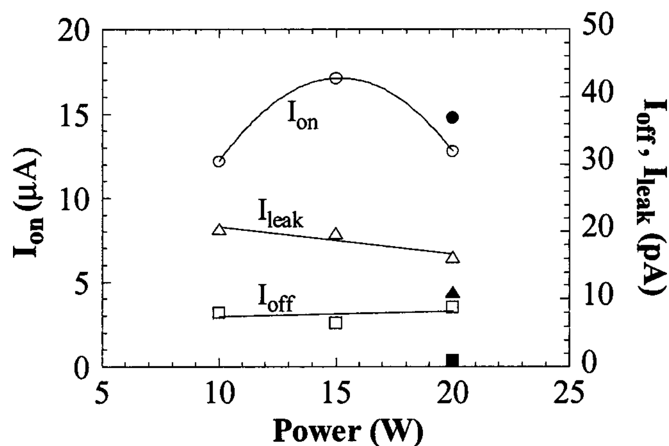

Figure 8. The off-current I_{off}, the on-current I_{on}, and the gate-leakage current I_{leak} as a function of the rf power applied during the gate SiN_x growth. The TFT structure and all other TFT layers are identical. Open symbols are for TFTs on glass, full symbols for TFTs on polyimide. The data are average values from several TFTs.

linear mobilities reveal that the thickness reduction in the a-Si:H channel layer from 200 to 100 nm had the most pronounced effect on the mobility. A further slight improvement was achieved by raising the hydrogen flow during the growth of the a-Si:H layer, while a deterioration occurred when the hydrogen flow was raised to 330 sccm during the growth of the SiN_x gate dielectric layer. The threshold voltages are low and vary between 1.4 and 1.9 V. The values for the linear mobility and the threshold voltage are averaged over several devices.

In the last step, we fabricated TFTs on 51 μm thick polyimide foil with procedures very similar to those for TFTs on glass. But before the TFT growth, the polyimide was coated on both sides with a 0.5 μm thick layer of SiN_x. The Cr layers, used previously for metallization, were replaced with more ductile metals. The gate electrode was made of Ti/Cr and the source/drain contacts of Al. Figure 11 shows the transfer characteristic and the calculated mobilities as function of applied gate voltage for these devices. The TFTs on Kapton have slightly higher off current, lower on current, and lower mobilities than the same structure on glass. The linear mobility, calculated from the transfer characteristic of Fig. 9 at V_{ds} = 0.1 V, is ~0.4 cm^2/Vs, while the saturated mobility, calculated from the transfer characteristic at V_{ds} = 10 V, varies with V_{gs}, as shown in Fig. 9. The peak mobility for V_{ds} = 10 V is ~0.7 cm^2/V s, suggesting that high quality a-Si:H TFTs can be made with further process improvement.

Conclusions

We have presented a step-by-step optimization process for the fabrication of amorphous silicon thin-film transistors by plasma enhanced chemical vapor deposition at 150°C. The most critical step is the deposition of a high quality low temperature silicon nitride gate

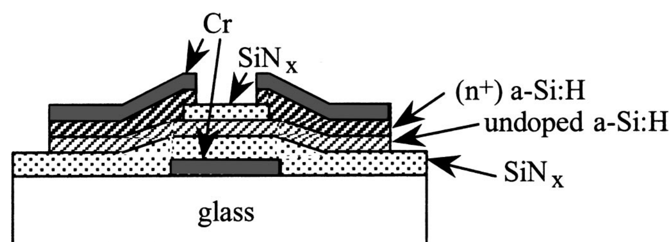

Figure 9. Cross-sectional view of the channel-passivated TFT on glass.

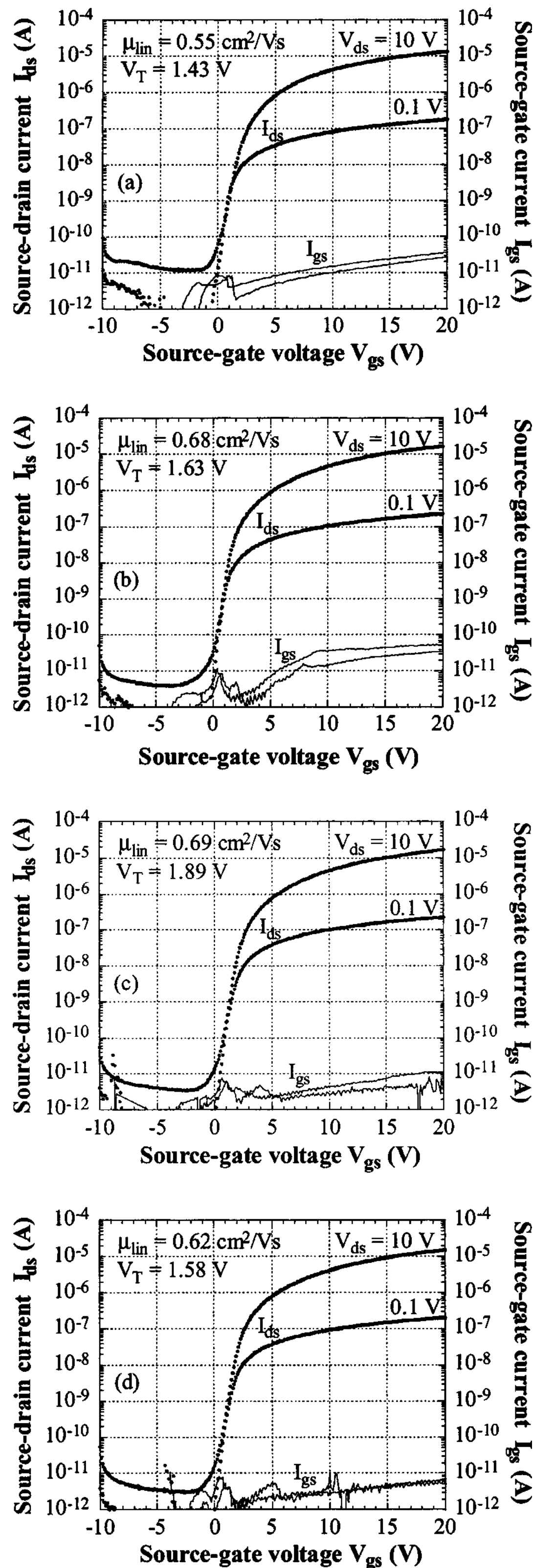

Figure 10. Transfer characteristics of four groups of a-Si:H TFTs with back-channel passivation, fabricated at 150°C with the aim to reach a high mobility. See text for explanation of channel and a-Si:H/SiN_x interface structures (a, top)-(d, bottom).

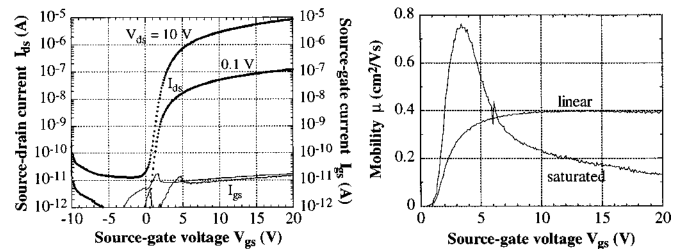

Figure 11. Transfer characteristics (on the left) and mobilities (on the right) for a-Si:H TFTs with back-channel passivation, fabricated on 51 μm polyimide foil by PECVD at a maximum process temperature of 150°C.

dielectric. Our experimental data prove that hydrogen dilution is a suitable technique to ensure low gate leakage current, because the optimized SiN_x layers have parameters comparable to those of standard SiN_x prepared at 300-350°C. These SiN_x layers were tested in a-Si:H TFTs with either back-channel etch or channel-passivated structure, prepared on glass or 51 μm thick polyimide substrates. In these low temperature TFTs, the mobility is the only parameter that ''suffers'' from the low temperature process. Nevertheless, we have achieved mobilities as high as ~0.7 cm^2/V s and thus have documented that low temperature a-Si:H based electronics on plastic substrates is feasible.

Acknowledgment

The work at Princeton is supported by DARPA's High Definition Systems Program. The research at Comenius University acknowledges support from the Slovak VEGA Grant Agency, grant no. 1/7672/20.

Princeton University assisted in meeting the publication costs of this article.

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