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Tradeoffs between AC power quality and DC bus ripple for 3-phase 3-wire inverter-connected devices within microgrids (Extended version)

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***Abstract*— Visions of future power systems contain high penetrations of inverters which are used to convert power from DC (direct current) to AC (alternating current) or vice versa. The behavior of these devices is dependent upon the choice and implementation of the control algorithms. In particular, there is a tradeoff between DC bus ripple and AC power quality. This study examines the tradeoffs. Four control modes are examined. Mathematical derivations are used to predict the key implications of each control mode. Then, an inverter is studied both in simulation and in hardware at the 10kVA scale, in different microgrid environments of grid impedance and power quality. It is found that voltage drive mode provides the best AC power quality, but at the expense of high DC bus ripple. Sinusoidal current generation and dual sequence controllers provide relatively low DC bus ripple and relatively small effects on power quality. High bandwidth DC bus ripple minimization mode works well in environments of low grid impedance, but is highly unsuitable within higher impedance microgrid environments and/or at low switching frequencies. The findings also suggest that the certification procedures given by G5/4, P29 and IEEE 1547 are potentially not adequate to cover all applications and scenarios.**

***Index Terms*— Inverters, Power quality, Power system harmonics, Power system simulation**

I. Nomenclature - all values pu (per-unit) unless stated

C_{DC}	DC bus capacitance (in Farads)
E_{abc}	Drive voltages synthesized by the inverter bridge
E_{dq}^{p}	Positive-sequence drive voltages in the synchronous reference frame (SRF)
E_{dq}^{n}	Negative-sequence drive voltages in the SRF
E_{rPkPk}	Peak-to-peak energy ripple to/from the DC bus (per unit, relative to S_{rated} for 1 second)
f	Frequency (as measured by the PLL) in Hz
I_{abc}	Inverter output currents
I_{dq}^{p}	Positive sequence component of I_{abc} in SRF, equal to $I_d^p + jI_q^p$
I_{dq}^{p1}	Filtered I_{dq}^{p} by averaging over exactly 1 cycle, to reveal the mean value of I_{dq}^{p} which represents the fundamental
I_{dq}^{p*}	Reference (target) value of I_{dq}^{p}
I_{dq}^{n}	Negative sequence component of I_{abc} in SRF, equal to $I_d^n + jI_q^n$
I_{dq}^{n1}	Filtered I_{dq}^{n} by averaging over exactly 1 cycle, to reveal the mean value of I_{dq}^{n} which represents the fundamental
I_{dq}^{n*}	Reference (target) value of I_{dq}^{n}
P	Active power flow (export to AC grid)
P^*	Active power target (export to AC grid)
P_{rRMS}	RMS ripple of the instantaneous power-flow
Q	Reactive power flow (export to AC grid)
Q^*	Reactive power target (export to AC grid)
R_G	Per-unit grid impedance (resistive)
R_L	Per-unit inductor resistance
S_{rated}	The rating of the inverter (in VA)
T	The time (in seconds) for each controller frame. i.e. the reciprocal of the switching frequency
V_{abc}	Voltages at the point of common coupling (PCC)
V_{dq}^{p}	Positive sequence component of V_{abc} in SRF, equal to $V_d^p + jV_q^p$
V_{dq}^{p1}	Filtered V_{dq}^{p} by averaging over exactly 1 cycle, to reveal the mean value of V_{dq}^{p} which represents the fundamental
V_{dq}^{n}	Negative sequence component of V_{abc} in SRF, equal to $V_d^n + jV_q^n$
V_{dq}^{n1}	Filtered V_{dq}^{n} by averaging over exactly 1 cycle, to reveal the mean value of V_{dq}^{n} which represents the fundamental
V_{DC}	The nominal DC bus voltage (in Volts)
X_G	Per-unit grid impedance (inductive)
X_L	Per-unit inductor reactance
V_{DCPkPk}	Peak-to-Peak DC bus ripple voltage (in Volts)
ω	2π times f (frequency) in radians per second
θ	Angle of V_{dq} measured at the PLL (radians)
Ψ	Calibration angle (radians) to add, to account for controller lag

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II. Introduction

VISIONS of future power systems contain high penetrations of power electronic inverters which are used to convert power from DC (direct current) to AC (alternating current) or vice-versa. Simple examples are generator interfaces where the power flow is unidirectional, such as required to connect a DC fuel cell to an AC power distribution network. More complex bi-directional examples are required to connect DC electrical storage devices to the AC distribution network, as in the case of a battery, reversible fuel cell, or vehicle-to-grid storage systems. More complex bidirectional inverter systems are required to connect devices such as rotating flywheel storage devices, where the DC link is an intermediate stage between a variable-speed drive/generator and the AC power system. Some specialized inverter applications are designed to provide optimum power quality to

local sensitive loads, within microgrid environments [1].

As such inverters become more commonplace, their combined effect on the AC power network becomes more significant. Thus, their aggregated impact on AC voltage power quality becomes a more significant concern than it has been in the past [2]. At the same time, there is a desire to keep the DC power flow ripple to a minimum. This desire comes from the manufacturers of both the inverters and the devices supplying or receiving the DC power. This is to minimize the size (and expense) of DC bus capacitance and switch ratings, to minimize torque ripples in rotating machines, and/or to minimize ripple voltages/currents to/from batteries or fuel cells.

For traditional synchronous generators, the response of the machine to voltage unbalance or harmonics is well understood [3], behaving like a "voltage behind a transient reactance", As such, these machines present a passive mitigation of voltage unbalance and harmonics at a PCC (Point of Common Coupling), by sinking or sourcing currents which tend to return the PCC voltages to a balanced sinusoidal condition. The degree of AC voltage power quality improvement is determined by the generator rating and its per-unit value of the transient reactance, and the grid impedance (fault level) at the PCC. The improvement of AC voltage power quality is generally at the expense of torque ripples presented to the generator, aside from tripleN harmonics which can be absorbed in the machine windings.

For inverter-connected equipment, the response of the device to AC voltage power quality deviations at the PCC is dependent on the control software and design of hardware [4] [5]. These can vary on a case-by-case basis and there is no generic inverter-connected model which can be used for system studies [6]. The response is determined by the designer who may deliberately or accidentally equip the inverter with desirable or undesirable behaviors.

Many previous works have presented control strategies which aim for either high power quality of AC current waveforms or minimization of DC bus power-flow ripple, in isolation. In contrast this paper, for the first time, considers both DC bus power-flow ripple and AC power quality together, and the tradeoffs between them, provided by different high-level control strategies. The interactions between the inverter and the power network, via the PCC, is key to this study. The nature of this interaction is governed by the control algorithm, grid impedance, switching frequency, harmonic filter, and choice of active and reactive power targets. In this study, the focus is on unbalance and the lower-order harmonics. The topology of the inverter and the switching harmonics [7] are assumed to be suitable to meet the requirements for limiting the levels of injected switching harmonics.

A fundamental point is that within the inverter, the switching bridge(s) contain no significant energy storage mechanism. Thus, instantaneous three-phase AC power flow is, for practical purposes, equal to the DC bus power flow. Therefore, DC bus power-flow ripple and AC power quality are inherently linked which leads to compromises between the potentially conflicting desires of low DC bus power-flow ripple with the maintenance of good AC power quality.

In this paper, improved AC power quality is defined by a reduction in the levels of voltage unbalance and harmonics at the PCC, and vice versa. This view is taken since customers connected to the PCC will be directly exposed to these voltages. This means that it is possible to achieve an improved AC power quality at the PCC, by sinking or sourcing non-sinusoidal and/or unbalanced inverter currents from a distributed-resource (DR) inverter, if these act to reduce the AC voltage unbalance and/or harmonic levels.

While the above rationale makes common sense, there are regional variations between the applicable standards for DR, and inconsistencies in their approaches. For example, in the USA, IEEE 1547 [8] [9] provides a relatively inflexible specification for limits of harmonic current injection, which does not allow large DR harmonic currents even if they actually improve AC power quality. IEEE 1547 also makes no mention of unbalanced voltages or currents. In the UK, Engineering Recommendation G5/4-1 [10] provides a similar "1st stage" analysis for harmonics, but also allows a 2nd and 3rd stage analysis which allow potentially higher levels of harmonic current, so long as the final AC voltage power quality is acceptable, accounting for the actual DR installation scenario, including existing customers and grid impedances. Also in the UK, Engineering Recommendation P29 [11] places limits on the final resulting unbalance, similarly to the 2nd and 3rd stage G5/4-1 process.

Both sets of standards allow certification to be achieved within test-facility power systems where voltage unbalance and harmonic voltage contamination is low or zero. Indeed, the IEEE 1547 test procedure [12] specifically requires DR testing with voltage THD less than 2.5% and with voltage unbalance less than 3%. It is generally favorable for a DR manufacturer to have the DR tested at conditions as close to zero unbalance and zero THD as possible. The measured values of unbalanced and harmonic currents can then be used to gain IEEE 1547 or G5/4 acceptance relatively easily. However, such a test procedure does not guarantee to expose the DR to conditions which it may experience in its final application.

In such real-world conditions with degraded power quality, the DR may respond in quite different ways, dependent upon the control algorithms used within the DR inverter. This means that the DR may lead to different effect on power quality at the PCC than the initial IEEE 1547 or G5/4 assessment predicts. The aim of this paper is to highlight mechanisms by which these effects can occur. This is achieved by presenting and comparing four quite different inverter control strategies in sections IV thru VII, from the perspectives of both AC power quality and DC bus power-flow ripple.

III. Summary of harmonic and unbalance standards governing connection

This section presents an extremely condensed and simplified overview of the current standards in the USA and UK, which govern the connection of three-phase distributed-resource (DR) inverters, from the standpoint of unbalance and harmonics.

A. USA

In the USA, IEEE 1547 [8] and its test procedure [12] defines the standard for interconnection of DR within electric power systems. This document says nothing about the allowed levels of unbalanced current from the DR. There are, however, strict and tight requirements on the harmonic currents with the DR is allowed to inject, which are the same as those laid down in IEEE 519 [13] [9]. However, these limits (see Table 1) can be specified as a percentage of an overall maximum customer demand, so the actual DR harmonics can be proportionately larger, relative to its own rating, if the DR is regarded as part of a larger installation with existing significant demand. The test procedures also dictate that a stiff grid source with a maximum impedance of $0.05j$ pu is used.

B. UK

In the UK, engineering recommendations [14] for the connection of distributed generation refer to G75/1 [15] for equipment above 20kV or 5MW capacity, G83/1 [16] for equipment below 16A per phase, and G59-1 [17] for equipment in between. All these documents in turn effectively refer to UK Engineering Recommendations G5/4-1 [10] for harmonic performance and P29 [11] for unbalance. In these documents, the emphasis is on ensuring that the voltage power quality at the PCC remains within acceptable bounds, by accounting for an assumed or actual fault level (grid impedance) at the PCC. This allows some scope for DR to output significant unbalanced and harmonic currents, particularly if these do not degrade, or even improve, the PCC voltage power quality.

G5/4-1 defers regulation of the connection of 3-phase inverters up to 16A per phase (aggregate) at any single customer site to EN 61000-3-2 [18]. This is a loose specification in Amps for each harmonic, which allows significant THD up to and over 100%. For example the 2nd harmonic is allowed to be up to 2.3A when the nominal load current may be of this order or even less for a small inverter. Even for a 10kW inverter (14.4A/phase), 2.3A represents a 16% distortion in just a single harmonic. For significant or aggregated equipment, G5/4-1 "stage 1" refers to a section of EN 61000-3-12 [19] which allows three-phase equipment up to 75A per phase to be connected so long as emissions are below those shown in Table 1. G5/4-1 also allows for more complicated "stage 2" and "stage 3" analyses which allow different potentially higher levels of harmonic current, so long as the final voltage power quality is acceptable. As an example, Table 2 shows the allowable harmonic voltages for the lower order harmonics and the overall THD limit which is 8%. These figures are almost identical to those laid down in BS EN 50160 [20].

P29 describes that three-phase equipment should be designed to tolerate at least 2% voltage unbalance, and does recognize that inverters generate "additional harmonic currents in both AC and DC circuits when subjected to unbalanced voltage". For acceptance on the public network, any new aggregate installation must

- not cause PCC voltage unbalance to exceed 2% for any whole minute, over an annual operating period
- never cause PCC voltage unbalance to exceed 1.3%, starting from an assumed balanced condition before the equipment is connected, for more than 5 minutes in every 30 minutes. (1% for equipment connected at 33kV or above)

Harmonic	Harmonic current as a percentage of fundamental at full-rated operation of the DR or optionally (for IEEE 1547) as a percentage of the overall maximum customer demand current	
	EN 61000-3-12	IEEE 1547
2	8 %	1 %
3		4 %
4	4 %	1 %
5	10.7 %	4 %
6	2.7 %	1 %
7	7.2 %	4 %
8	2 %	1 %
9		4 %
10	1.6 %	1 %
11	3.1 %	2 %
12	1.3 %	0.5 %
13	2 %	2 %
Overall current THD (%)	13 %	5 %

Table 1 : Acceptable proportions of selected harmonic currents under IEEE 1547 and under the most conservative interpretation of table 3 of EN 61000-3-12

Harmonic	Harmonic voltage level (%)	
	400V systems	Up to 36.5kV
2	2 %	2 %
3	4 %	5 %
4	1 %	1 %
5	6 %	6 %
6	0.5 %	0.5 %
7	5 %	5 %
8	0.5 %	0.5 %
9	1.2 %	1.5 %
10	0.5 %	0.5 %
11	3.5 %	3.5 %
12	0.2 %	0.2 %
13	3 %	3 %
Overall current THD (%)	8 %	8 %

Table 2 : Harmonic voltage compatibility levels for selected harmonics under G5/4 for 400V systems and systems up to 36.5kV

C. Potential problems with the existing standards

In terms of harmonics, therefore IEEE 1547 therefore

provides a very strict and relatively inflexible specification for harmonic current injection, while G5/4 offers a potentially more flexible assessment based upon meeting voltage power quality. In terms of unbalanced current injection, IEEE 1547 says nothing, whilst G5/4 aims to meet a sensible final voltage unbalance level of 1.3%.

Both sets of standards, however, contain loopholes which this paper will highlight. Specifically, during certification the measurement of DR performance can be made within power systems where voltage unbalance and harmonic voltage contamination is low or zero. Indeed, [12] specifically requires the DR test condition to be with voltage THD less than 2.5% and with unbalance less than 3%. Thus, any sensible DR manufacturer will arrange to test the DR at conditions as close to zero unbalance and zero THD as possible. The measured values of unbalanced and harmonic currents can then be used to gain IEEE 1547 or G5/4 acceptance. Such a test procedure does not guarantee to expose the DR to conditions which it may experience in its final application.

In such real-world conditions, the DR may respond in quite different ways, dependent upon the control algorithms and software used within the DR inverter. This means that the DR may lead to a far higher degradation of power quality at the PCC than the IEEE 1547 or G5/4 assessment predicts. Conversely, there is very little allowance within either set of standards for DR inverters to output very high levels of unbalanced or harmonic current, if these were such that they would improve the local power quality. This paper will highlight mechanisms by which these effects can occur.

IV. The Impacts of Voltage Power Quality on V_{dq}^{p} Trajectory

A. Park transformation convention

All of the control modes presented in this study require conversion of the measured three-phase voltages and currents into the synchronous reference frame *dq* components via the Park transformation. In this paper, the transformation used is the same as that used by MATLAB® SimPowerSystems [21]:

$$V_{dq}^{p} = \left(V_d^{p} + V_q^{p} j\right) = \frac{2}{3} j e^{-jwt}\left[V_a + e^{j\frac{2\pi}{3}} V_b + e^{-j\frac{2\pi}{3}} V_c\right] \quad (1)$$

All voltage and current measurements are expressed in per-unit, with values of 1 as nominal. Use of one of the alternative conventions of Park transformation will lead to different phases or directions-of-rotation of the V_{dq} trajectories quoted in Table 3, but will not affect the overall performance of any inverter system, so long as consistency is maintained in the inverse-Park transformation used to create the drive currents and voltages. The negative-sequence dual of (1) is:

$$V_{dq}^{n} = \left(V_d^{n} + V_q^{n} j\right) = \frac{2}{3} j e^{-jwt}\left[V_a + e^{-j\frac{2\pi}{3}} V_b + e^{j\frac{2\pi}{3}} V_c\right] \quad (2)$$

While the controllers implemented during this study use the synchronous reference frame, similar performance can be obtained by the use of a stationary reference frame approach. In this case, resonant controllers [22] [23] are then required.

B. Trajectories of V_{dq}^{p} due to unbalanced and harmonics

At the heart of any inverter is a phased-locked-loop (PLL). For a three-phase inverter this can be a single positive-sequence PLL which locks such that V_q^{p1}, the filtered value of V_q^{p}, is held at zero value. This can be achieved using exact-time averaging over 1 cycle, as described in [24],[25], or by a different filtering technique such as [26]. The filtering allows the PLL to output estimates of system frequency *f* and phase θ which are immune to ripple due to unbalance and harmonics. However, in real time the instantaneous measurement of V_{dq}^{p} will vary from the nominal value of (1+0*j*) due to the voltage unbalance and harmonics [27]. This effect was quantified in [26], although this work did not examine the effect of unbalanced harmonics (i.e. when the voltage waveform shapes are not the same on all three phases). Following the analysis methodology of [26], the effect on V_{dq}^{p} of both balanced and unbalanced effects, at any harmonic and at any phase, can be deduced, leading to the results of Table 3.

In Table 3, it can be seen that the disturbances lead to circular V_{dq}^{p} deviations which can be generalized to the form $\alpha e^{j(Nwt+\phi)}$, defined by α (amplitude), *N* (harmonic frequency of rotation) and ϕ (phase offset). These variables will be used in section V to form general expressions for current and power flows.

Scenario		V_{dq}^{p} trajectories, as deviations from the nominal (1+0j) point. $\alpha e^{j(Nwt+\phi)}$
Balanced 1pu positive-sequence, no harmonics		0
Unbalance of magnitude M_U at phase ϕ_U relative to the fundamental		$M_U e^{j(-2wt-\phi_U+\pi)}$
Balanced harmonics order M_H with phases ϕ_H relative to the fundamentals	"TripleN" harmonics eg. 3rd, 6th, 9th etc.	0
	"Positive-sequence" harmonics (4th, 7th, 10th etc.)	$M_H e^{j((N_H-1)wt+\phi_H)}$
	"Negative-sequence" harmonics (2nd, 5th, 8th etc.)	$M_H e^{j(-(N_H+1)wt-\phi_H+\pi)}$
Unbalanced harmonic order N_H on a single phase with magnitude M_H and phase ϕ_H relative to the fundamental.		$\frac{M_H}{3} e^{j((N_H-1)wt+\phi_H)}$ and $\frac{M_H}{3} e^{j(-(N_H+1)wt-\phi_H+\pi)}$ (for a harmonic on phase A; for harmonics on phases B and C, the phase of the V_{dq}^{p} trajectories are different to that given, and also depend upon N_H)
Unbalanced DC bias of V_{DC} on 1 measurement of V_a, V_b or V_c		$\frac{2V_{DC}}{3} e^{j(wt+\pi)}$
Balanced DC bias of V_{DC} on all measurements of V_a, V_b and V_c		0

Table 3 : V_{dq}^{p} perturbations due to voltage unbalance and harmonics.

V. Schemes for Inverter Control, Optionally with Power-Flow Ripple Minimisation

A. High-bandwidth power-flow ripple minimization using a single controller

This control mode allows power-flow ripple minimization under conditions of unbalance, harmonic content and non-zero Q^*. It requires high-bandwidth controllers, i.e. controllers whose bandwidth is at least 3 times the fundamental frequency [28]. The desired currents are derived in the positive sequence only by (3) [22] (see Fig. 1), using unfiltered synchronous reference frame measurements of V_{dq}^{p}, leading to I_{dq}^{p*} trajectories with significant harmonic content:

$$\begin{bmatrix} I_d^{p*} \\ I_q^{p*} \end{bmatrix} = \frac{1}{\left(\left(V_d^{p}\right)^2+\left(V_q^{p}\right)^2\right)} \begin{bmatrix} V_d^{p} & V_q^{p} \\ V_q^{p} & -V_d^{p} \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix} \quad (3)$$

The choice of P^* and Q^* in (3) and Fig. 1 is made via conventional droop controllers, or modified droop controllers to account for renewable power sources or DC bus voltage requirements [29] [30]. Equation (3) minimizes power-flow ripple in all cases using only a positive-sequence analysis. This is possible because the analysis is unfiltered, and so information describing all sequences and all harmonics is present in V_{dq}^{p} and I_{dq}^{p*}. For example, in the presence of unbalanced voltages, V_{dq}^{p} moves in a circular trajectory at twice the fundamental frequency, leading to an I_{dq}^{p*} trajectory which also has a second harmonic component. Thus, although only a positive-sequence controller is used, its bandwidth is high enough to also capture and control negative sequence and harmonic effects.

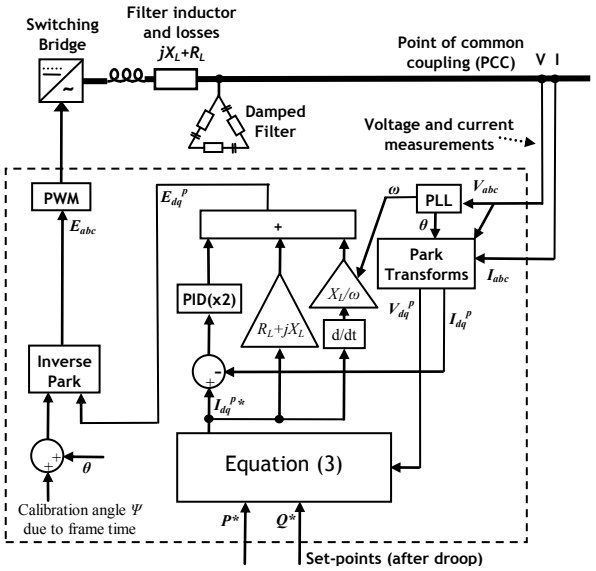

Fig. 1. Control diagram for high-bandwidth power-flow ripple minimization

The reaction of such a control scheme to unbalance and harmonics can be derived by looking at the response to the generalized V_{dq}^{p} trajectories $\alpha e^{j(Nwt+\phi)}$ shown in Table 3. Equation (3) expands to:

$$\begin{bmatrix} I_d^{p*} \\ I_q^{p*} \end{bmatrix} = \begin{bmatrix} \frac{P^*\left(1+\alpha\cos\left(N\omega t+\phi\right)\right)+Q^*\left(\alpha\sin\left(N\omega t+\phi\right)\right)}{\left(1+\alpha^2+2\alpha\cos\left(N\omega t+\phi\right)\right)} \\ \frac{P^*\left(\alpha\sin\left(N\omega t+\phi\right)\right)-Q^*\left(\left(1+\alpha\cos\left(N\omega t+\phi\right)\right)\right)}{\left(1+\alpha^2+2\alpha\cos\left(N\omega t+\phi\right)\right)} \end{bmatrix} \quad (4)$$

I_{abc} can then be found from (4), using the inverse Park transform and further mathematical analysis:

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = P_t \begin{bmatrix} \left(\sin\left(\omega t\right)-\sum_{k=1}^{\infty}\left(-\alpha\right)^k\sin\left(\left(kN-1\right)\omega t+k\phi\right)\right) \\ \left(\sin\left(\omega t-\frac{2\pi}{3}\right)-\sum_{k=1}^{\infty}\left(-\alpha\right)^k\sin\left(\left(kN-1\right)\omega t+\frac{2\pi}{3}+k\phi\right)\right) \\ \left(\sin\left(\omega t+\frac{2\pi}{3}\right)-\sum_{k=1}^{\infty}\left(-\alpha\right)^k\sin\left(\left(kN-1\right)\omega t-\frac{2\pi}{3}+k\phi\right)\right) \end{bmatrix} - Q_t \begin{bmatrix} \left(\cos\left(\omega t\right)+\sum_{k=1}^{\infty}\left(-\alpha\right)^k\cos\left(\left(kN-1\right)\omega t+k\phi\right)\right) \\ \left(\cos\left(\omega t-\frac{2\pi}{3}\right)+\sum_{k=1}^{\infty}\left(-\alpha\right)^k\cos\left(\left(kN-1\right)\omega t+\frac{2\pi}{3}+k\phi\right)\right) \\ \left(\cos\left(\omega t+\frac{2\pi}{3}\right)+\sum_{k=1}^{\infty}\left(-\alpha\right)^k\cos\left(\left(kN-1\right)\omega t-\frac{2\pi}{3}+k\phi\right)\right) \end{bmatrix} \quad (5)$$

This shows that the fundamental component of the current is always balanced. It also shows that the current harmonics contain the 1st, and an infinite sequence of harmonics at

($kN-1$), at amplitudes decreasing with increasing k. Further analysis of (5) in conjunction with Table 3 shows that when the voltages contain balanced fundamentals and harmonics (either "positive sequence" or "negative sequence" harmonics), then mod(N,3)=0. In this case, the currents of (5) will always be balanced and have the same shape, although their harmonic content may be significant. For unbalanced voltage fundamentals or harmonics,. mod(N,3)≠0 and (5) shows that the harmonic content of the current waveforms will be unbalanced. The clearest example is that unbalanced fundamental voltages will lead to $N=-2$ and unbalanced 3rd harmonic currents, giving different wave-shapes on the 3 phases. To demonstrate this effect, Fig. 2 shows the theoretical output currents from this controller and the low-bandwidth dual-sequence controller (section V.C), under the exaggerated scenario of 20% voltage unbalance so that the distortion is easily visible in the time domain.

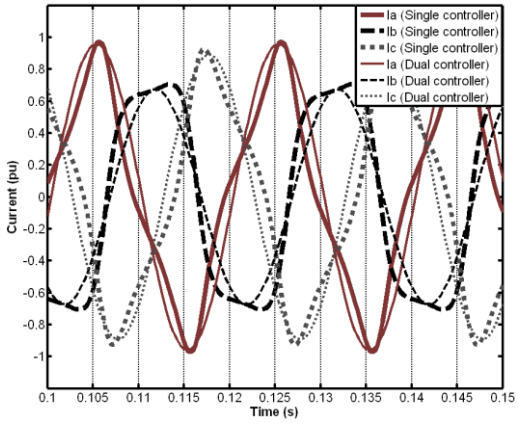

Fig. 2. Theoretical output currents from low-bandwidth dual-sequence and high-bandwidth single controllers for power-flow ripple minimization, with 20% voltage unbalance. P^*=0.8, Q^*=0.

For practical implementation, the simplest form of the high-bandwidth controller is to measure the actual currents I_{dq}^{p}, compare them to the target currents I_{dq}^{p*} from (3), and then implement a high-bandwidth PID (Proportional Integral Derivative) controller to control the inverter bridge drive voltages E_{dq}^{p}. However, the burden on the PID controller can be significantly reduced by adding feed-forward terms, as shown in Fig. 1. The following relationship describes E_{dq}^{p} required to generate the currents I_{dq}^{p*} across the primary inductor with assumed per-unit impedance (R_L+jX_L) [31]:

$$E_{dq}^{p} = V_{dq}^{p} + R_L \cdot I_{dq}^{p*} + jX_L \cdot I_{dq}^{p*} + \frac{X_L}{\omega}\frac{d}{dt}\left(I_{dq}^{p*}\right) \qquad (6)$$

These terms can all be added within the control software as feed-forward terms, with a dynamic value for ω provided by the PLL. In this way, the PID controllers only need to make adjustments due to hardware component variations from assumed values, perturbations of the system, and because the control system has a finite switching frequency. In this control mode, both simulation and hardware experiments show that the actual currents I_{dq}^{p} can be made to track the reference currents I_{dq}^{p*} much more accurately by the use of the unfiltered positive-sequence voltage feedforward term V_{dq}^{p} in (6), rather than any filtered values.

By Table 3 and (5), the primary response to any voltage harmonic of order N_H will primarily be current harmonics of order (N_H-2) and/or (N_H+2), while the primary response to unbalance is unbalanced 3rd harmonics. However, these primary responses will tend to induce further voltage harmonics at the PCC at these new frequencies, and these in turn can cause secondary current harmonics. In a weak grid scenario, this can make the control mode highly undesirable, as will be shown in section VII.

B. High-bandwidth sinusoidal balanced currents

This scheme does not attempt to minimize power-flow ripple, although the ripple which results is found to be relatively small, particularly in practice. The scheme aims for perfectly balanced, sinusoidal currents on all three phases. This is achieved by modifying (3) to:

$$\begin{bmatrix} I_d^{p*} \\ I_q^{p*} \end{bmatrix} = \frac{1}{\left|V_d^{p1} + jV_q^{p1}\right|}\begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}\begin{bmatrix} P^* \\ Q^* \end{bmatrix} \qquad (7)$$

In terms of practical implementation (Fig. 3) , this scheme uses a similar high-bandwidth controller as described previously. However, both simulation and hardware experiments show that the best performance is achieved by feeding forward only the filtered fundamental positive and negative sequence terms V_d^{p1} and V_{dq}^{n1}, in place of the unfiltered V_{dq}^{p} term in (6). The differential feedforward term in (6) is also not required, since I_{dq}^{p*} is invariant against unbalance and harmonics on the PCC voltages, via the use of only the positive-sequence fundamental component V_{dq}^{p1} in (7).

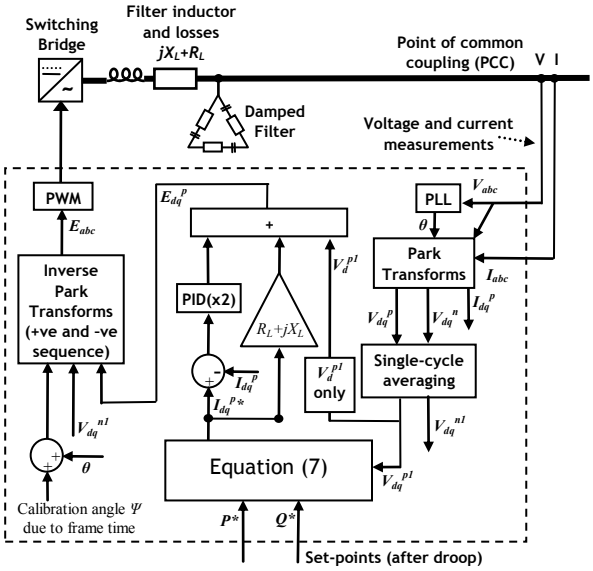

Fig. 3. Control diagram for high-bandwidth sinusoidal balanced currents

The actual power flows, in the presence of a V_{dq}^{p} voltage

disturbance $\alpha e^{j(N\omega t+\phi)}$, can be derived as:

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \frac{P*}{\left|V_d^{p1} + jV_q^{p1}\right|}\begin{bmatrix} 1+\alpha\sin\left(N\omega t+\phi+\frac{\pi}{2}\right) \\ \alpha\sin\left(N\omega t+\phi\right) \end{bmatrix} + \frac{Q*}{\left|V_d^{p1} + jV_q^{p1}\right|}\begin{bmatrix} \alpha\sin\left(-N\omega t-\phi\right) \\ 1+\alpha\sin\left(N\omega t+\phi+\frac{\pi}{2}\right) \end{bmatrix} \quad (8)$$

Thus, the active power ripples will be at frequencies equal to the $V_{dq}^{\ p}$ disturbances from Table 3, with amplitudes equal to the magnitudes of the $V_{dq}^{\ p}$ disturbances times the P^* and/or Q^* target outputs. So, for example, a 2% fundamental voltage unbalance will lead to a ±2% peak (0.014 pu RMS) power ripple at the 2nd harmonic, for $P^*=1$, $Q^*=0$.

C. Dual low-bandwidth positive and negative sequence controllers

It is possible to use low-bandwidth (i.e. significantly less than the fundamental frequency) controllers to minimize power-flow ripple in the presence of unbalanced (but zero THD) voltages, if the desired Q^* is zero [32], [33],[34]. Solving the equations of [32] leads to:

$$\begin{bmatrix} I_d^{p1*} \\ I_q^{p1*} \\ I_d^{n1*} \\ I_q^{n1*} \end{bmatrix} = \begin{bmatrix} V_d^{p1} & V_q^{p1} \\ V_q^{p1} & -V_d^{p1} \\ -V_d^{n1} & V_q^{n1} \\ -V_q^{n1} & -V_d^{n1} \end{bmatrix} \begin{bmatrix} \frac{P*}{\left(\left(V_d^{p1}\right)^2+\left(V_q^{p1}\right)^2\right)-\left(\left(V_d^{n1}\right)^2+\left(V_q^{n1}\right)^2\right)} \\ \frac{Q*}{\left(\left(V_d^{p1}\right)^2+\left(V_q^{p1}\right)^2\right)+\left(\left(V_d^{n1}\right)^2+\left(V_q^{n1}\right)^2\right)} \end{bmatrix} \quad (9)$$

In the presence of unbalanced fundamental alone, all the terms of (9) will be steady-state values, and the controllers can have very slow bandwidths, leading to a dual pair of relatively constant $E_{dq}^{\ p}$ and $E_{dq}^{\ n}$ drive voltages (Fig. 4). This is analogous to a synchronous generator which has two controllable contra-rotating rotors, one in the positive-sequence direction and one in the negative-sequence direction. In this scenario, the desired output currents will be unbalanced (with unbalance magnitude equal to the voltage unbalance), but sinusoidal, containing no harmonics. Due to the low-bandwidth controllers, limitations of (9), and the use of only filtered fundamental sequence information this algorithm is not capable of minimizing power-flow ripple when the voltages have harmonic content. When such harmonics are present, the output currents will contain harmonics, and power-flow ripple will increase, in a similar manner to that of the pure balanced voltage drive mode, described in section V.D. This analysis extends to the 0th harmonic (i.e. DC), and therefore the control algorithm also requires some additional low-bandwidth low-gain controllers to ensure that DC currents remain at zero (Fig. 4). Proposed enhancements to this algorithm [23] [27] [34] describe slightly alternative derivations of the $I_{dq}^{\ p*}$ and $I_{dq}^{\ n*}$ references, together with higher-bandwidth current controllers. These alternative implementations will produce slightly different results than described in this paper, particularly with respect to their response to harmonics. Of particular interest is [35] which demonstrates the power-quality versus power-ripple properties of 5 variants of such controllers when exposed to unbalanced fundamental voltages.

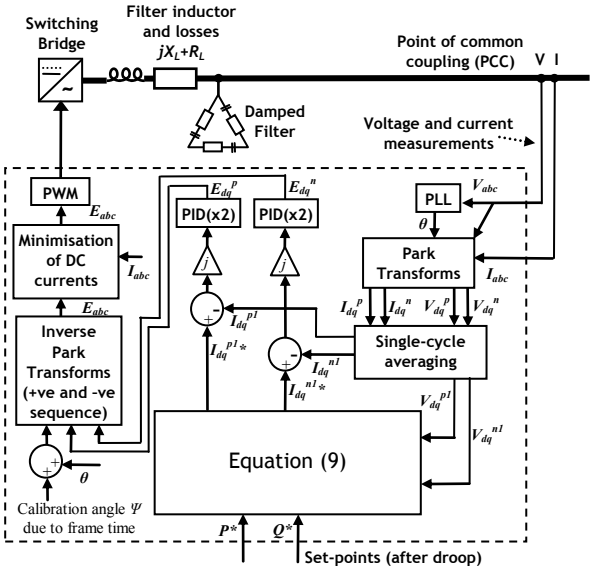

Fig. 4. Control diagram for low-bandwidth dual-sequence controllers

Assuming that unbalanced fundamental voltage is the only disturbance initially present, the effect of this control strategy on power quality at the PCC can be determined mathematically. This can be done by examining the additional positive and negative sequence voltage components which arise at the PCC due to the inverter currents flowing through the finite grid impedance. The analysis accounts for the fact that any resulting change in local voltage unbalance, caused by this effect, will cause a further change in current reference calculation, in the manner of a converging geometric series, assuming that the unbalance and grid impedance are small on a per-unit basis.

The expression:

$$\left(\Delta V_d^{n1} + j\Delta V_q^{n1}\right) = \left(\Delta I_d^{n1} + j\Delta I_q^{n1}\right)\left(R_G + jX_G\right) \quad (10)$$

gives the incremental negative-sequence voltage component which will arise due to the incremental inverter currents, and the per-unit grid impedance (R_G+jX_G). The increase in overall magnitude of negative-sequence voltage can be evaluated exactly by:

$$\Delta\left|V_{dq}^{n1}\right| = \left|\left(V_d^{n1} + jV_q^{n1}\right) + \left(\Delta V_d^{n1} + j\Delta V_q^{n1}\right)\right| - \left|\left(V_d^{n1} + jV_q^{n1}\right)\right| \quad (11)$$

When the incremental unbalance is smaller than the existing unbalance, or when they are not orthogonal, a good approximation to (11) is:

$$\Delta V^{n1} = \Delta\left|V_{dq}^{n1}\right| = \frac{\left(\left(\Delta I_d^{n1} + j\Delta I_q^{n1}\right)\left(R_G + jX_G\right)\right)\bullet\left(V_d^{n1} + jV_q^{n1}\right)}{\left|\left(V_d^{n1} + jV_q^{n1}\right)\right|} \quad (12)$$

Now, if the pre-existing negative sequence is given by:

$$\begin{aligned} V_d^{n1} &= V^{n1}\cos\phi^{n1} \\ V_q^{n1} &= V^{n1}\sin\phi^{n1} \end{aligned} \quad (13)$$

where the negative sequence voltage is at a magnitude and phase of $V^{n1}\angle\phi^{n1}$ relative to the positive sequence, and assuming a nominal 1pu positive sequence voltage, then (9) becomes:

$$\begin{bmatrix} I_d^{p1} \\ I_q^{p1} \\ I_d^{n1} \\ I_q^{n1} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & -1 \\ -V^{n1}\cos\phi^{n1} & V^{n1}\sin\phi^{n1} \\ -V^{n1}\sin\phi^{n1} & -V^{n1}\cos\phi^{n1} \end{bmatrix} \begin{bmatrix} \dfrac{P*}{\left(1-\left(V^{n1}\right)^2\right)} \\ \dfrac{Q*}{\left(1+\left(V^{n1}\right)^2\right)} \end{bmatrix} \quad (14)$$

Evaluating (12) given (13) & (14), yields:

$$\Delta V^{n1} = \left(\frac{V^{n1}}{\left(1-\left(V^{n1}\right)^2\right)}\right)\left(-R_G P* + X_G Q*\right) \quad (15)$$

This demonstrates an interesting independence of the phase of the original negative sequence, and also that the incremental change ΔV^{n1} will be small (justifying the approximation of (12)) since $V^{n1}<<1$, $R_L<<1$ and $X_L<1$ in normal circumstances. Indeed, one would hope that this would be the case, since in reality the incremental change ΔV^{n1} causes the actual perceived value V^{n1} at the inverter to change slightly, forming a closed feedback loop. Allowing for this feedback loop with a geometric series, (assuming that $V^{n1}<<1$), leads to:

$$\Delta V_{ClosedLoop}^{n1} \approx \left(\frac{V^{n1}\left(-R_G P* + X_G Q*\right)}{1 - V^{n1}\left(-R_G P* + X_G Q*\right)}\right) \quad (16)$$

When (15) or (16) evaluates as a positive number, then the fundamental negative sequence voltage magnitude at the inverter terminals will decrease, and vice-versa. Thus, in a network which is predominantly inductive, negative sequence voltage will tend to be increased when reactive power is exported. Conversely, it will tend to be decreased when reactive power is imported. However, to estimate the actual resultant unbalance, equation (15) or (16) must be used in tandem with the expected change in positive-sequence voltage magnitude at the inverter terminals, due to the positive-sequence relation (17).

$$\Delta V^{p1} = \frac{P*}{\left(1-\left(V^{n1}\right)^2\right)} R_G + \frac{Q*}{\left(1+\left(V^{n1}\right)^2\right)} X_G \quad (17)$$

The overall expected change in unbalance can be calculated accurately using (16) and (17) together. However, assuming $V^{n1}<<1$ and $V^{p1}\approx 1$, i.e. unbalance <5% and approximately nominal positive-sequence voltage, several terms cancel out.

The change in unbalance is approximately:

$$\Delta U \approx \frac{V^{n1}\left(-2R_G P*\right)}{\left(1 + P* R_G + Q* X_G\right)} \quad (18)$$

Equation (18) is interesting, in that it shows that the change in unbalance (power quality) is largely independent of $Q*$ and X_G. This is useful since many networks are predominantly inductive. This feature arises because the currents due to reactive power tend to cause increases or decreases in both negative and positive sequence together, leading to a null change in unbalance. Unbalance should only be increased by importing active power in a network with a resistive component of impedance.

D. *Voltage drive mode*

The inverter can be operated such that the bridge synthesizes a balanced sinusoidal voltage set, using low-bandwidth PI controllers to set a relatively constant value of E_{dq}^{p}, i.e. "rotor advance angle" and "field voltage" which are exactly analogous to the "voltage behind a transient reactance" behavior of a synchronous generator [3]. This is shown in Fig. 5. It is also possible to create a similar effect by removing all the negative sequence signals from the dual-sequence controller of Fig. 4. Also, similarly to the low-bandwidth dual-sequence controller, the use of the filtered fundamental-only values means that additional low-bandwidth low-gain controllers are required to control DC (the 0th harmonic) currents.

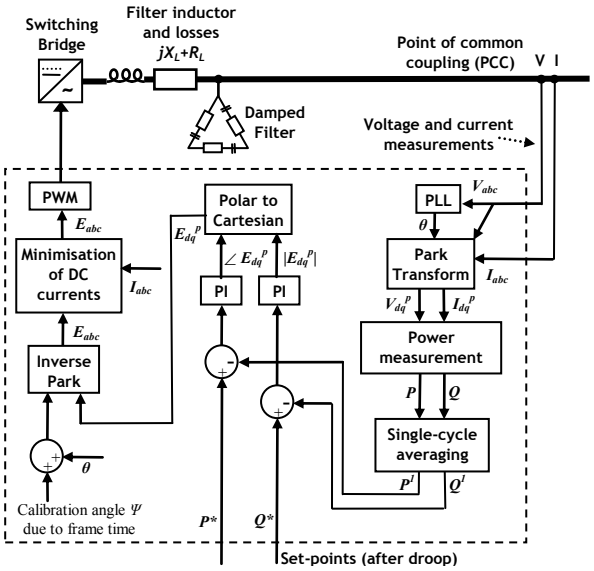

Fig. 5. Control diagram for voltage-drive mode

In this mode, the inverter will tend to passively mitigate both unbalance and harmonics on the voltages at the PCC, at the expense of (potentially large) power-flow ripple. The output currents, in the presence of a V_{dq}^{p} voltage disturbance $\alpha e^{j(N\omega t+\phi)}$, can be derived as (assuming $X_L>>R_L$):

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \frac{\alpha}{X_L(N+1)} \begin{bmatrix} \cos\left((N+1)\omega t+\phi\right) \\ \cos\left((N+1)\omega t-\frac{2\pi}{3}+\phi\right) \\ \cos\left((N+1)\omega t+\frac{2\pi}{3}+\phi\right) \end{bmatrix} + P* \begin{bmatrix} \sin(\omega t) \\ \sin\left(\omega t-\frac{2\pi}{3}\right) \\ \sin\left(\omega t+\frac{2\pi}{3}\right) \end{bmatrix} - Q* \begin{bmatrix} \cos(\omega t) \\ \cos\left(\omega t-\frac{2\pi}{3}\right) \\ \cos\left(\omega t+\frac{2\pi}{3}\right) \end{bmatrix} \quad (19)$$

This shows that there will be balanced currents determined by $P*$ and $Q*$, plus further harmonic currents determined by the voltage unbalance and harmonics at the PCC. These are potentially large since X_L is usually in the region of 0.05 to 0.2. Similarly to the analysis following (5), the currents produced in the presence of balanced harmonics will also be balanced, but the currents due to unbalanced harmonics (including unbalanced fundamental) with mod(N,3)≠0 will lead to unbalanced current harmonics, giving. different wave-shapes on the three phases. The corresponding power ripple can also

be derived:

$$P = P^* + \alpha\left[P^* \sin\left(N\omega t + \phi + \frac{\pi}{2}\right) + Q^* \sin\left(N\omega t + \phi + \pi\right) + \frac{\sin\left(N\omega t + \phi + \pi\right)}{X_L(N+1)}\right] \quad (20)$$

This shows that the power ripple (like the harmonic currents) can be very large, even with $P^*=Q^*=0$. For example, in the presence of unbalance at 2%, with X_L=0.1, N=−2 and α=0.02 by Table 3, and thus the power ripple amplitude will be of the order of ±0.2pu (0.14 pu RMS) at 100Hz (for a 50Hz fundamental).

While this mode passively mitigates unbalance and harmonics, in [36] an extended control mode is described, which actively mitigates voltage harmonics at the PCC to provide even greater improvements in power quality. Such modes might incur even higher power-flow ripple, and risk of overloading the inverter components.

VI. Practical Limitations within Real Inverters and Real Scenarios

Aside from the theoretical results of Fig. 2, all the results generated during this study are generated by considering a 3-wire grid-connected inverter using a standard 6-switch IGBT bridge. This inverter exists both as a simulation, and also as a real inverter with a nominal rating of 10kVA, embedded within a laboratory power system environment. The bridge is controlled using SV-PWM (Space Vector Pulse Width Modulation), at a 4kHz switching frequency. This frequency is a compromise between lower switching losses on the one hand, and high-bandwidth controllability and low switching harmonics on the other. Both the simulations and the hardware use the same control code, which is largely created in MATBAB® Simulink. The simulations use this code directly within the MATLAB® SimPowerSystems environment. The hardware inverter requires the Simulink code to be converted to embedded 'C' code using the MATLAB® Real-Time Workshop and Embedded Coder toolboxes, before it can be inserted into the microcontroller which controls the hardware. The control application is capable of seamlessly switching between the 4 different grid-connected control modes described in section V, and an extra islanded (voltage drive) mode, in real time and under full load. Such seamless mode-switching requires careful software design [37], for example pre-loading of integrators within PID control loops. The application (in simulation and hardware) also provides measurement, diagnosis and data logging functions, which are used to gather the data which is presented in thus study.

A. Inverter design and simulation fidelity

A simplified diagram of the inverter is shown in Fig. 6. The link inductor has been characterized by using the inverter to output full power at both 50Hz and also at 100Hz. The measured values are 2.9mH and 0.51Ω at 50Hz (X_L=0.17pu, R_L=0.096pu), with resistance rising to 0.59Ω at 100Hz. The resistance of the link inductor also includes the resistance of the switching devices. The 50Hz values are used to calculate the feed-forward terms in (6). Accurately modeling the inductor using ladder networks [38] [39] presents several simulation difficulties, and also requires characterizing the inductor over the full frequency range from DC to 4kHz at full power, which is problematic. In the simulations presented here, the effect of the increasing inductor loss versus frequency has been more simply approximated by inclusion of an extra 0.25Ω in series with actual 10Ω damping resistors. In practice this provides a good agreement between simulation and practical experience.

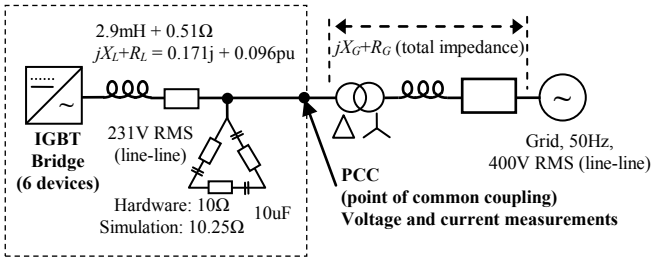

Fig. 6. High-level 10kVA Inverter design (one-line diagram)

The capacitative element of the LC filter is necessary to enable islanded operation and to reduce switching harmonics [40]. The 10Ω damping resistors are included to reduce oscillations at the LC filter corner frequency of 530Hz, and to damp resonant modes in the control-network system [41]. The resulting damping for the LC filter is ζ=0.2. Increasing this damping would be desirable to reduce the risk of oscillatory modes. However, the damping resistors currently dissipate 0.16% of the rated power of the inverter, and increasing the damping would increase this figure.

B. Limitations due to switching frequency

Finite switching frequency poses challenges for all inverter control algorithms and their stability. The switching frequency defines the sample rate (conventionally the same as the switching frequency). The control frame time T is the reciprocal of the sample rate. The frame time needs to be accounted for in the inverter control algorithms and simulation environment [6] [42] [43]. In particular, the total time lag between actual measurements and the effective control of bridge voltage is more than one frame. It is made up of:

- Analogue filter delay (20kHz low-pass filter). 50µs.
- The effective time between the reading of the ADC channels, accounting for de-skewing [24] [44] and the beginning of the computational frame. 37µs.
- The computational frame at 4kHz lasts 250µs.
- The computed SV-PWM drive timings are output to the switches. They appear as (on average) voltages which are effectively lagged by ½ a frame, or 125µs.

The combined round-trip control lag is thus approximately 460µs, or 1.8 frames. For the voltage drive mode, and dual positive-negative sequence control mode, the lag time can be accounted for almost completely by the addition of a phase rotation of $\Psi=2\pi f^*1.8^*T$ to the drive voltages during the inverse Park transformation from $E_{dq}{}^p$ and $E_{dq}{}^n$ to E_{abc}, where f

is the measured frequency in Hz from the PLL.

The 1.8 frame round-trip delay causes very real constraints for the high-bandwidth power-flow ripple minimization and sinusoidal-current modes. For the high-bandwidth power-flow ripple minimization, the feed-forward term V_{dq}^{p} in (6) suffers directly from the delay, reducing the performance of the control. For both high-bandwidth control modes, the remaining feed-forward terms and PID controllers also have to contend with the round-trip delay, reducing the performance. Additional techniques such as Kalman filtering [42] might be used to partially compensate the effect of these delays.

Within the simulation environment, all these loop delays are carefully simulated to match the hardware environment.

VII. Results from Simulations and Hardware at 4kHz Switching Frequency

In this section, a suite of simulations and hardware experiments are summarized and discussed. The scenarios used are shown in Fig. 7, with different grid types and grid impedances (jX_G+R_G pu). In all cases, inverter diagnostics are used to characterize the power quality of the voltage and current waveforms at the PCC, and also to characterize the power-flow ripple, which is determined from the AC currents and voltages at the PCC. The discerning reader will note that the AC power flow is not exactly equal to the DC bus power flow, due to the dissipation of energy (resistive/core losses) and storage of energy (inductive) within the primary link inductor (jX_L+X_R pu) and filter capacitors. However, the difference between the AC power flow and DC power flow is very small in practice, and a minimization of AC power flow ripple at the PCC does, to all intents and purposes, also provide minimization of DC bus power ripple.

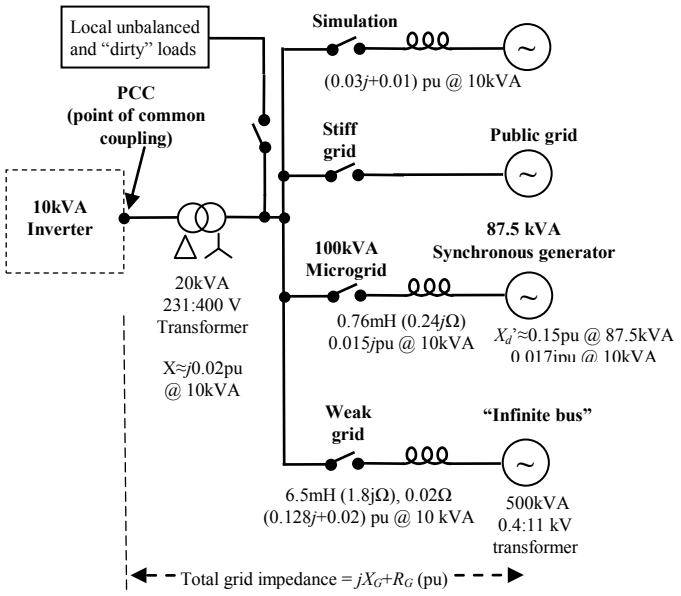

Fig. 7. Simulation and hardware experiment scenarios

The power-flow ripple results are provided in two formats. The first format is a per-unit RMS power ripple, P_{rRMS}. In the tables, this is recorded as mpu (milli-per-unit) RMS.

$$P_{rRMS}=\sqrt{\left(\frac{1}{T}\int_{0}^{t=T}\left(P(t)-\overline{P}\right)^2\cdot dt\right)} \quad \text{where} \quad \overline{P}=\frac{1}{T}\int_{0}^{t=T}P(t)\cdot dt \tag{21}$$

P_{rRMS} shows the magnitude of the power-flow ripples, but provides no indication of the frequency of the ripple, nor the potential magnitude of any resulting DC bus ripple voltage. Therefore, the second format given is the peak-to-peak energy ripple E_{rPkPk}, reported in μpu. This is the peak-to-peak energy, as a per-unit fraction of the inverter power rating times 1 second, which flows in and out of the DC bus every cycle, incremental to the average energy flow per cycle. This measure is used in this paper instead of the voltage ripple, since its value is independent of DC bus voltage and DC bus capacitance, and thus provides a fairer basis for comparison between control strategies.

$$E_{rPkPk}=\max\left(\int_{o}^{t_1}\left(P(t)-\overline{P}\right)\cdot dt\right)-\min\left(\int_{o}^{t_2}\left(P(t)-\overline{P}\right)\cdot dt\right) \tag{22}$$

where t_1 and t_2 can be set anywhere within the ranges $0\le t_1\le T$ and $0\le t_2\le T$ to find the maximum (i.e. true) value of E_{rPkPk}. In practice, within simulation or numerical controller algorithms, E_{rPkPk} is easily found using "peak hold" and "minimum hold" functions, which can be reset each cycle. E_{rPkPk} can be directly related to the peak-to-peak DC bus voltage ripple V_{DCPkPk}, for a given inverter rating, nominal DC bus voltage, and DC bus capacitance, by evaluating the energy exchange with the DC bus capacitance:

$$E_{rPkPk}\times S_{rated}=\frac{C_{DC}\left(V_1+V_{DC}\right)^2}{2}-\frac{C_{DC}\left(V_2+V_{DC}\right)^2}{2}$$

where V_1 and V_2 describe maximum and minimum DC bus voltage offsets from the nominal value V_{DC}, defining the peak-to-peak voltage ripple as (V_1-V_2).

$$\Rightarrow E_{rPkPk}\times S_{rated}=\frac{C_{DC}\left(V_1^2+V_{DC}^2+2V_1V_{DC}-V_2^2-V_{DC}^2-2V_2V_{DC}\right)}{2}$$

$$\Rightarrow E_{rPkPk}\times S_{rated}=\frac{C_{DC}\left(V_1^2+2V_1V_{DC}-V_2^2-2V_2V_{DC}\right)}{2}$$

$$\Rightarrow V_1V_{DC}-V_2V_{DC}=\frac{E_{rPkPk}\times S_{rated}}{C_{DC}} \text{ since } V_{DC}>>V_1 \ \&\ V_{DC}>>V_2$$

$$\Rightarrow V_{DCPkPk}=\frac{E_{rPkPk}\times S_{rated}}{C_{DC}\times V_{DC}} \tag{23}$$

Notably, for a given value of RMS power ripple P_{rRMS}, a lower value of energy ripple E_{rPkPk} will result if the power ripple is primarily due to higher-order harmonics rather than the 2nd harmonic power ripple which arises due to voltage unbalance, because of the smaller time period of the harmonic power-flow ripples.

A. Simulation : 0.05pu inductive grid impedance

Table 4 to Table 7 show the results of simulations using all four control modes, using a grid impedance of (0.05*j*+0.01) pu

(Fig. 7). Table 4 shows the results using a clean infinite bus, while Table 5 & Table 6 show the results using 2% unbalance at the infinite bus, and Table 7 shows the results using 2% unbalance and 5% balanced 5th harmonic. Table 5 to Table 7 also include data in square brackets []. These are predictions for:

- THD of currents using high-bandwidth DC bus ripple minimization mode, by (5), ignoring effects due to secondary harmonics and finite controller bandwidth.
- RMS power ripple using high-bandwidth sinusoidal balanced current mode, by (8), ignoring effects due to finite controller bandwidth.
- Voltage unbalance at the PCC, using low-bandwidth dual-sequence controllers, by (18).
- THD of currents using low-bandwidth dual-sequence controllers and voltage-drive mode, and also for current unbalance in voltage-drive mode, by (19).
- THD of voltages at the PCC using voltage-drive mode and low-bandwidth dual-sequence controllers, by considering attenuation through a divider formed by the inductor and grid impedances, and accounting for increased inductive reactance at higher harmonics. Voltage unbalance at the PCC can also be predicted for voltage-drive mode in this way.
- RMS power ripple using voltage-drive mode, by (20).
- Additional predictions for zero or unchanged responses based upon ideal controller responses.

In the simulations, although all loop delays are carefully simulated as previously described, there are other effects which are not simulated. These include component tolerances, variable core losses, measurement noise, and EMC (electromagnetic coupling) issues. Because the simulations do not include these effects, the feed-forward terms are very effective, and only very low control gains are required. However, these control gains are not suitable for real scenarios and the actual control gains used are determined using both simulation and hardware experimentation. For the 3 control modes other than the high-bandwidth power-flow ripple minimization, a single set of control gains (for each mode) is found which works well in all scenarios, for both "stiff" and "weak" grids, in simulation and hardware (Table 18). However, for the high-bandwidth power-flow ripple minimization mode, two different sets of control gains are presented. The results labeled "HH" use high gains (the same as used for sinusoidal current generation), and provide the best performance in "stiff" grid scenarios. The results labeled "HL" use proportional gains which are halved from the "HH" sets. These are found to be necessary for stability in weaker grid scenarios.

Table 4 shows that all control modes function as expected during good power quality.

Table 5 shows that during voltage unbalance, the dual-sequence controller, "HH", and "HL" successfully minimize power-flow ripple, as they should. Voltage drive provides mitigation of voltage unbalance from 2% to 1.6%, by sourcing currents which are 10% unbalanced, close to the predictions. Table 6 (with additional reactive power export), shows that the dual-sequence controller no longer totally minimizes power-flow ripple, as described in section V.C, but that the "HL" controller does. The "HL" controller in this case provides better performance than its higher-gain "HH" equivalent. It is found by experimentation that a grid impedance of approximately 0.05pu is about the breakpoint at which the "HH" and "HL" controllers offer roughly equal performance. For lower grid impedances, the "HH" controller is better. For higher grid impedances, the "HL" controller is better. This is further discussed below.

Table 5 and Table 6 also verify (within the attainable accuracy of the simulation results, which is finite and varies with the choice of Simulink solver configuration) the unbalance predictions of (18) for the dual-sequence controller.

Table 7 shows the results when both unbalance and THD is applied to the infinite bus voltages. In this case, the dual-sequence controller is not able to reduce the power-flow ripple as effectively due to the presence of harmonics which are not captured by the control loops which only operate on the fundamentals, with low bandwidth. The high-bandwidth power-flow ripple minimization mode functions much better at limiting RMS power ripple: to 18 mpu. This is achieved by sourcing balanced currents with significant THD. The predicted level of current THD from (5) is only 5.4% (2% 3rd harmonic and 5% 7th harmonic), but the simulation shows current THD at double this value. This is due in part to the finite controller bandwidth, which means that the control loops struggle to respond to a 5th harmonic voltage by sourcing 7th harmonic currents at approximately 350Hz, which is comparable to both the control bandwidth and the LC filter resonant frequency. In addition, the sourced 3rd and 7th harmonics excite further voltage harmonics at the PCC, as previously described. These in turn produce secondary current harmonics at other frequencies. Some of these frequencies can excite the LC filter, even though it is damped. All these factors together lead to a higher actual level of current and voltage THD than predicted by a simple analysis of (5).

It is interested that the high-bandwidth sinusoidal current mode is able to provide the same (or better) power-flow ripple minimization, using significantly lower current distortion, and also providing better power quality at the PCC. The voltage drive mode provides the best power quality in all of Table 4 to Table 7, at the expense of significant power-flow ripple. The behavior for this mode is generally as predicted, although the measured RMS power-flow ripple is lower than predicted. This is mainly due to the assumption in (20) that $X_L >> R_L$. In the scenario presented, this assumption is only marginally true (Fig. 6), leading to the observed discrepancy. In a real inverter, more care would be paid to reducing R_L to minimize losses,

making (20) more accurate.

Measure / Control method	RMS power ripple (mpu)	Pk-Pk energy ripple (μpu)	I THD (%)	I Unbal (%)	V THD (%)	V Unbal (%)
OFF					0.0	0.0
"HL"	0	0	0.5	0.2	0.4	0.0
"HH"	1	0	0.9	0.1	0.4	0.0
Sinusoidal	0	0	0.2	0.1	0.1	0.0
Dual sequence	1	0	0.3	0.1	0.2	0.0
Voltage drive	2	20	0.4	0.3	0.2	0.0

Table 4. Simulation, X_G=0.05, R_G=0.01, clean infinite bus, P*=0.8pu, Q*=0

Measure / Control method	RMS power ripple (mpu)	Pk-Pk energy ripple (μpu)	I THD (%)	I Unbal (%)	V THD (%)	V Unbal (%)
OFF					0.0 [0.0]	2.0 [2.0]
"HL"	5 [0]	20	2.5 [2.0]	0.7 [0.0]	0.5	2.0 [2.0]
"HH"	3 [0]	10	2.5 [2.0]	0.3 [0.0]	0.5	2.0 [2.0]
Sinusoidal	11 [11]	50	0.2 [0.0]	1.5 [0.0]	0.2 [0.0]	2.0 [2.0]
Dual sequence	2 [0]	10	0.4 [0.0]	2.0 [2.0]	0.3 [0.0]	1.979 [1.968]
Voltage drive	53 [66]	250	0.3 [0.0]	10.0 [11.7]	0.2 [0.0]	1.6 [1.6]

Table 5. Simulation, X_G=0.05, R_G=0.01, 2% unbalance at infinite bus, P*=0.8pu, Q*=0. Predictions in brackets [ ]

Measure / Control method	RMS power ripple (mpu)	Pk-Pk energy ripple (μpu)	I THD (%)	I Unbal (%)	V THD (%)	V Unbal (%)
OFF					0.0 [0.0]	2.0 [2.0]
"HL"	5 [0]	20	2.7 [2.0]	0.4 [0.0]	0.5	1.9 [2.0]
"HH"	33 [0]	110	7.9 [2.0]	0.4 [0.0]	3.3	1.9 [2.0]
Sinusoidal	12 [14]	40	1.1 [0.0]	0.4 [0.0]	0.3 [0.0]	1.9 [2.0]
Dual sequence	14	60	1.1 [0.0]	1.7 [2.0]	0.3 [0.0]	1.963 [1.969]
Voltage drive	48 [67]	220	0.3 [0.0]	8.1 [9.4]	0.2 [0.0]	1.6 [1.6]

Table 6. Simulation, X_G=0.05, R_G=0.01, 2% unbalance at infinite bus, P*=0.8pu, Q*=0.6. Predictions in brackets [ ]

Measure / Control method	RMS power ripple (mpu)	Pk-Pk energy ripple (μpu)	I THD (%)	I Unbal (%)	V THD (%)	V Unbal (%)
OFF					5.4 [5.0]	2.0 [2.0]
"HL"	18 [0]	50	9.7 [5.4]	0.8 [0.0]	6.2	2.0 [2.0]
"HH"	16 [0]	40	11.2 [5.4]	0.3 [0.0]	6.2	2.0 [2.0]
Sinusoidal	15 [30]	60	4.9 [0.0]	0.1 [0.0]	4.6 [5.0]	2.0 [2.0]
Dual sequence	32	60	4.8 [5.7]	2.0 [2.0]	4.1 [3.9]	1.978 [1.969]
Voltage drive	62 [77]	280	5.3 [5.7]	10.0 [11.7]	4.1 [3.9]	1.6 [1.6]

Table 7. Simulation, X_G=0.05, R_G=0.01, 2% unbalance & 5% balanced 5th harmonic at infinite bus, P*=0.8pu, Q*=0. Predictions in brackets [ ]

Measure / Control method	RMS power ripple (mpu)	Pk-Pk energy ripple (μpu)	I THD (%)	I Unbal (%)	V THD (%)	V Unbal (%)
OFF					5.4	2.0
"HL"	10	30	8.9	0.2	6.2	1.9
"HH"	17	40	10.0	0.1	6.1	1.9
Sinusoidal	15	40	5.3	0.7	4.4	1.9
Dual sequence	26	80	4.6	1.8	4.0	2.0
Voltage drive	53	240	4.3	8.2	4.0	1.6

Table 8. Simulation, X_G=0.05, R_G=0.01, 2% unbalance & 5% balanced 5th harmonic at infinite bus, P*=0.8pu, Q*=0.6

B. Hardware experiments : stiff grid

For the stiff grid experiments, the hardware inverter was coupled to a 3-phase wall supply, via its delta-star transformer (Fig. 7). The resulting grid impedance is approximately 0.03j pu. In this case, it is difficult to deliberately modify the PCC power quality using a 10kVA inverter or convenient loads. Therefore, only results with low unbalance and voltage THD are presented. In these scenarios, the high-gain "HH" mode is better performing than the lower-gain "HL" mode, because the grid impedance is low and therefore the effect of secondary harmonics is also small. This also means that there is a relatively low risk of the LC filter resonating. Even so, the dual-sequence controller performs as-well or better on all measures. It gives a low power ripple since the existing voltage THD is low, and it has little tendency to increase PCC voltage harmonics since only fundamental voltage sources are synthesized. The PCC voltage unbalance is almost unchanged, as predicted by (18) when R_G is small. The sinusoidal balanced current mode performs almost as well at power-flow ripple minimization, actually performing better in terms of energy ripple (and therefore resulting DC bus voltage ripple by (23)) than any other mode.

In these experiments, the voltage drive mode actually causes the measurement of voltage unbalance at the PCC to increase relative to the other control modes, when one would expect it to give the lowest unbalance. This can be explained by the combination of:

- Component value imbalances between the three phases (IGBTs, inductors, capacitors, damping resistors, etc.), and
- Calibration accuracy and linearity of the instrumentation.

In this case, both the uncertainty of the unbalance measurement, and the natural unbalance voltage output by the inverter in voltage drive mode, are of the order of 0.5-1% and 0.5-1°. Commercial inverters could easily have similar performance, unless accurate (periodic) calibration and self-calibration procedures are implemented. These might be expensive, and might be difficult to maintain across changes in environmental conditions such as temperature.

Measure Control method	RMS power ripple (mpu)	Pk-Pk energy ripple (μpu)	I THD (%)	I Unbal (%)	V THD (%)	V Unbal (%)
OFF					1.5	0.3
"HL"	29	220	5.4	3.4	2.3	0.3
"HH"	16	110	5.5	1.8	2.3	0.3
Sinusoidal	16	100	2.0	2.1	2.1	0.2
Dual sequence	15	120	2.2	0.5	2.0	0.3
Voltage drive	51	300	2.2	8.0	2.0	0.4

Table 9. Hardware, X_G≈0.03, P*=0.8pu, Q*=0

Measure Control method	RMS power ripple (mpu)	Pk-Pk energy ripple (μpu)	I THD (%)	I Unbal (%)	V THD (%)	V Unbal (%)
OFF					1.9	0.4
"HL"	33	220	4.8	3.0	1.8	0.6
"HH"	22	130	4.7	1.5	1.8	0.6
Sinusoidal	23	110	3.2	1.9	1.7	0.6
Dual sequence	17	130	2.9	0.6	1.6	0.5
Voltage drive	49	280	2.8	6.0	1.7	0.7

Table 10. Hardware, X_G≈0.03 , P*=0.8pu, Q*=0.6

C. *Hardware experiments : 100kVA microgrid*

Table 11 and Table 12 show a subset of the results taken using a higher impedance network. In this case, an 87.5kVA synchronous generator was used to simulate a 100kVA microgrid scenario, in which the 10kVA inverter is embedded. The grid impedance is approximately 0.05*j* pu, as in the simulated studies. Table 11 shows results where ~0.6% voltage unbalance has been induced, by using 2 domestic kettles loaded onto phase A only (Fig. 7). Table 12 shows results where both voltage unbalance and harmonics have been induced by using 3 domestic microwave ovens, loaded onto phase A only. The harmonics are spread at a variety of frequencies (approx 0.2% 2nd, 1.4% 3rd, 1.2% 5th, 0.5% 7th, 0.2% 9th, 0.3% 11th, 0.3% 13th).

In both cases, the dual-sequence controller provides the lowest RMS power ripple, but the sinusoidal current mode provides the lowest energy ripple, which is perhaps more valuable since it relates to DC bus voltage ripple by (23). The high-bandwidth power-flow ripple minimization control mode appears to be of little value, providing both poor minimization of power-flow ripple and poor power quality. This is because the increased grid impedance leads to higher proportions of secondary harmonics at a scattering of frequencies at the PCC, as described previously. The higher harmonics cannot be as accurately controlled due to the finite controller bandwidth, and can also excite the LC filter resonance. The voltage drive mode should provide mitigation of voltage unbalance, but in this case it does not, since the pre-existing unbalance is quite low (0.6%) and of the same order as the natural output of the inverter in voltage drive mode, due to the tolerance and calibration issues discussed previously. Both the voltage drive mode and dual-sequence controller mode should provide passive mitigation of voltage harmonics, since they synthesize only fundamental voltage sources, but in these scenarios it is difficult to observe due to the relatively low levels of pre-existing voltage THD.

Measure Control method	RMS power ripple (mpu)	Pk-Pk energy ripple (μpu)	I THD (%)	I Unbal (%)	V THD (%)	V Unbal (%)
OFF					2.2	0.6
"HL"	47	350	7.9	2.9	3.9	0.8
"HH"	49	200	11.7	1.6	4.9	0.9
Sinusoidal	24	130	2.0	1.9	2.3	0.8
Dual sequence	21	150	2.0	1.0	2.3	1.0
Voltage drive	50	300	1.9	5.7	2.3	1.0

Table 11. Hardware, X_G≈0.05, unbalanced voltages (2 kettles on phase A) ,P*=0.8pu, Q*=0.6

Measure Control method	RMS power ripple (mpu)	Pk-Pk energy ripple (μpu)	I THD (%)	I Unbal (%)	V THD (%)	V Unbal (%)
OFF					2.5	0.5
"HL"	39	250	7.6	2.4	4.1	0.8
"HH"	51	250	11.9	1.3	5.1	0.8
Sinusoidal	28	150	2.5	1.9	2.7	0.8
Dual sequence	25	250	3.7	1.3	3.0	0.9
Voltage drive	55	310	2.7	5.6	2.8	0.9

Table 12. Hardware, X_G≈0.05, unbalanced harmonic voltages (3 microwave ovens on phase A) , P*=0.8pu, Q*=0.6

D. *Hardware experiments : weak grid*

Finally, Table 13 thru Table 17 show a suite of experiments using a very weak grid. Such a scenario might arise where an inverter is installed via a transformer of marginally 1pu rating, and/or at the end of a long overhead MV transmission line. Equally, the situation might arise where many small inverters with similar control algorithms are connected together so their output is aggregated. These tables show no-load, unbalanced, and unbalanced-plus-harmonic scenarios. As before, kettles and microwave ovens are used to induce the unbalance and harmonics.

Firstly, Table 13 demonstrates that the high-gain "HH" algorithm is entirely unsuitable in these weak grids. This is due to very large proportions of secondary harmonics at many frequencies at the PCC (Fig. 8), which cannot be accurately controlled by the finite controller bandwidth, and also excite the LC filter resonance which further complicates the situation. In this particular case the currents contain substantial ~20% 4th and ~16% 6th harmonic components. The "HH" mode is therefore not presented further in Table 14 to Table 17.

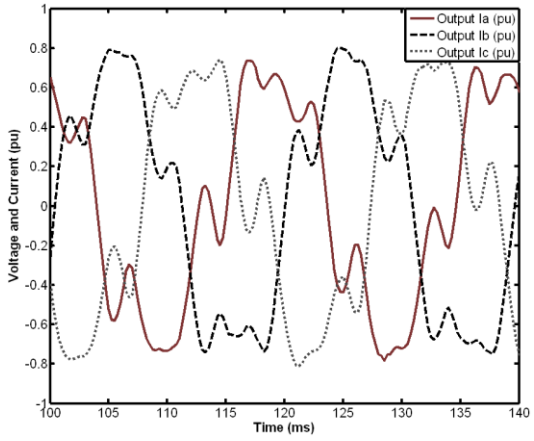

Fig. 8. Output currents from the high-bandwidth power-flow minimization mode controller in a weak grid scenario with inappropriately high control gains.

Table 14 to Table 17 show that in terms of power-flow ripple minimization, even the lower-gain "HL" mode is not as effective at minimizing power-flow ripple in weak grids, as the dual-sequence controller or sinusoidal balanced current mode (Fig. 9). This is true even with significant reactive power export targets and in the presence of voltage harmonics, when both these latter modes are, in theory, less effective. There is little to choose between the dual-sequence controller or sinusoidal balanced current modes, except that the dual-sequence controller mode tends to passively mitigate voltage harmonics, whereas the sinusoidal balanced current mode should in theory have no effect on power quality since it exports only balanced sinusoidal currents, but in practice can have a small (in this case beneficial) effect due to the finite switching frequency and control bandwidth.

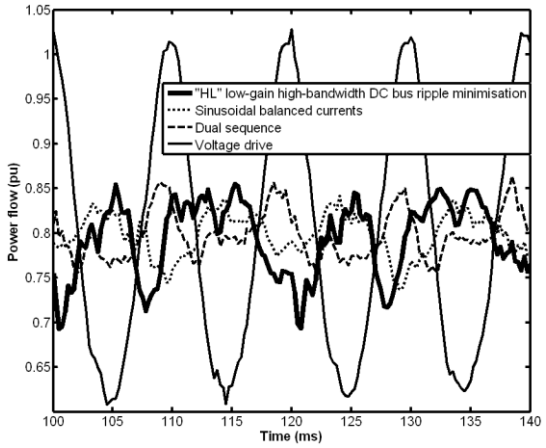

Fig. 9. Power-flow ripple in 4 control modes, weak grid (X_G≈0.15), unbalanced harmonic voltages (3 microwave ovens on phase A), P*=0.8pu, Q*=0

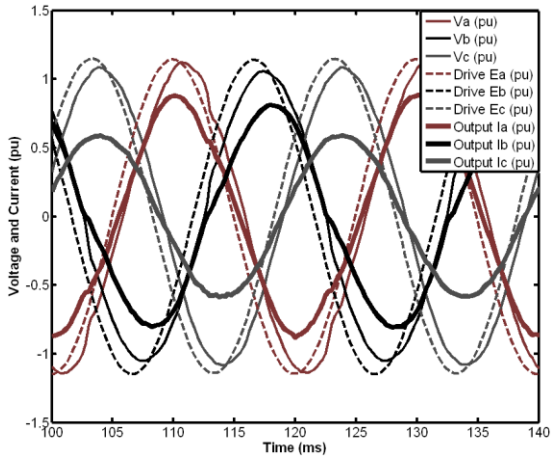

Fig. 10. PCC voltages, drive voltage, and currents in voltage drive mode, weak grid (X_G≈0.15), unbalanced harmonic voltages (3 microwave ovens on phase A), P*=0.8pu, Q*=0

To explain the effects of the control strategies on AC power quality, it is possible to consider the impedances which the infinite bus and inverter present to the power network in Fig. 7 for the weak grid scenario. The infinite bus presents a zero impedance to unbalance and harmonics, but it is separated from the dirty loads (which sink or source unbalanced and/or harmonic currents) by the grid impedance. Without the presence of the inverter, the resulting unbalanced and harmonic voltages at the PCC could be estimated by a $V = ZI$ approach, accounting for the grid impedance at each harmonic frequency. The inverter in voltage-drive mode which synthesizes a balanced sinusoidal voltage source, also presents a zero impedance to ground for both unbalanced and harmonic currents (aside from the errors due to calibration and linearity previously discussed). Therefore, in voltage-drive mode, the effective impedance to ground for the unbalanced and harmonic currents, from the PCC, is the grid impedance in parallel with the inverter inductor impedance. Thus, in Table 14 to Table 17, it is clear that the voltage drive mode is successful in significantly reducing voltage both unbalance and THD at the PCC from ~4% to ~2.3% and from 6% to 3.8% respectively. A reduction in either inductor impedance or grid impedance will further improve the power quality in this scenario.

An inverter using the dual-sequence controller also presents a zero impedance to harmonics, and therefore the resulting voltage THD is the same as for the voltage-drive mode. However, it does not present a zero impedance to unbalance, and instead has a much smaller effect on unbalance than the voltage-drive mode by (18), since even in the weak-grid scenario the grid resistance R_G is only 0.02pu and the net predicted change in unbalance is ≈-4%*-2*0.02*0.8≈-0.13%, which is small enough to be difficult to observe accurately.

The AC power-quality improvements achieved by the voltage-drive mode in these scenarios are obtained at the expense of significant current unbalance (Fig. 10) and THD, and also with significant power-flow ripple. A comparison between power-flow ripple for the 4 control modes in this weak-grid scenario is shown in Fig. 9. This clearly shows the voltage-drive mode having the largest power-flow ripple, while the sinusoidal current mode and the dual-sequence controllers have the lowest power-flow ripples.

Measure / Control method	RMS power ripple (mpu)	Pk-Pk energy ripple (μpu)	I THD (%)	I Unbal (%)	V THD (%)	V Unbal (%)
OFF					2.0	0.2
"HL"	30	200	8.9	3.9	4.0	0.5
"HH"	44	160	32.0	3.7	14.4	0.6
Sinusoidal	19	120	2.4	2.1	1.9	0.4
Dual sequence	12	110	2.0	0.6	2.0	0.5
Voltage drive	32	200	1.9	4.2	2.0	0.8

Table 13. Hardware, X_G≈0.15, no local loads, P*=0.8pu, Q*=0

Measure / Control method	RMS power ripple (mpu)	Pk-Pk energy ripple (μpu)	I THD (%)	I Unbal (%)	V THD (%)	V Unbal (%)
OFF					2.3	4.3
"HL"	35	230	13.2	2.5	5.4	4.0
"HH"						
Sinusoidal	23	140	2.3	2.2	2.1	4.0
Dual sequence	14	120	2.1	4.1	2.2	4.1
Voltage drive	130	650	2.2	21.4	2.2	2.3

Table 14. Hardware, X_G≈0.15, unbalanced voltages (2 kettles on phase A), P*=0.8pu, Q*=0

Measure / Control method	RMS power ripple (mpu)	Pk-Pk energy ripple (μpu)	I THD (%)	I Unbal (%)	V THD (%)	V Unbal (%)
OFF					2.3	4.3
"HL"	52	320	13.9	1.7	6.1	4.3
"HH"						
Sinusoidal	30	170	2.3	2.2	2.3	4.0
Dual sequence	30	150	1.8	2.3	2.1	4.4
Voltage drive	123	600	2.1	17.7	2.1	2.6

Table 15. Hardware, X_G≈0.15, unbalanced voltages (2 kettles on phase A), P*=0.8pu, Q*=0.6

Measure / Control method	RMS power ripple (mpu)	Pk-Pk energy ripple (μpu)	I THD (%)	I Unbal (%)	V THD (%)	V Unbal (%)
OFF					6.0	3.9
"HL"	41	270	18.7	4.4	8.4	3.5
"HH"						
Sinusoidal	23	150	6.9	2.3	4.2	3.6
Dual sequence	28	150	6.6	3.8	3.9	3.9
Voltage drive	141	670	5.7	20.2	3.6	2.1

Table 16. Hardware, X_G≈0.15, unbalanced harmonic voltages (3 microwave ovens on phase A), P*=0.8pu, Q*=0.0

Measure / Control method	RMS power ripple (mpu)	Pk-Pk energy ripple (μpu)	I THD (%)	I Unbal (%)	V THD (%)	V Unbal (%)
OFF					6.0	3.9
"HL"	80	400	20.3	1.4	10.5	3.5
"HH"						
Sinusoidal	27	180	4.1	2.1	4.0	3.3
Dual sequence	25	110	5.0	2.9	3.8	4.0
Voltage drive	135	670	3.8	16.1	3.8	2.2

Table 17. Hardware, X_G≈0.15, unbalanced harmonic voltages (3 microwave ovens on phase A), P*=0.8pu, Q*=0.6

Parameter / Control method	K_p	K_i	K_d
"HL"	2.5 x X_L	100 x X_L	0.0003 x X_L
"HH"	5 x X_L	100 x X_L	0.0003 x X_L
Sinusoidal	5 x X_L	100 x X_L	0.0003 x X_L
Dual sequence	0.25 x X_L	12 x X_L	0.0005 x X_L
Voltage drive (angle)	0.225 x X_L	10.8 x X_L	-
Voltage drive (magnitude)	0.1537	7.379	-

Table 18. Control gains for PID and PI controllers

VIII. CONCLUSIONS

In this paper, four different inverter control modes were summarized. These have been analyzed to examine their effects both on AC power quality and power-flow ripple at the DC bus, for various scenarios of voltage power quality.

When connected to stiff AC grids with impedance less than or equal to about 0.03pu, the high-bandwidth power-flow ripple minimization mode can provide effective minimization of power and energy ripple, if the switching frequency is high enough. However, within weaker grid scenarios, or with limited switching frequency, this control mode becomes unusable. In all scenarios, this control mode will tend to degrade power quality due to its injection of current harmonics at harmonic orders which are shown to occur at 2 above and/or 2 below the harmonic orders of any voltage disturbance.

The use of a low-bandwidth dual-sequence controller provides, in practice, for all scenarios other than the stiffest grids and highest switching frequencies, a better performance in all respects than the high-bandwidth power-flow ripple minimization mode. It is shown by theory and practice that this mode has little beneficial or detrimental effect on voltage unbalance at the PCC unless the grid impedance contains a significant resistive component. When this is the case, exporting real power to the grid results in slightly improved voltage unbalance, and vice versa. It is also shown that this mode tends to reduce voltage harmonics at the PCC. In this mode, the levels of unbalance and THD in the injected currents will increase from zero, as the voltage unbalance and THD at the PCC increase. The controller performance is not reliant on high switching frequencies. It might be possible to extend the mathematics of this controller to minimize power-flow ripple due to the presence of individual targeted voltage harmonics. For example the 5th harmonic may also be considered, by measuring the positive and negative-sequence 5th voltage harmonic and additionally sourcing 5th harmonic currents. This might, however, be reliant on the inversion of 8x8 (or larger) matrices in real time and would require 2 additional control loops. Further extension of the algorithm to deal with finite values of Q* would require the injection of additional current harmonics.

A high-bandwidth controller which aims to produce balanced sinusoidal currents is shown to provide similar power and energy ripple performance to the low-bandwidth dual-sequence controller, and in some practical cases the energy ripple is actually lower than that provided by the dual-sequence controller. The fidelity of the balanced sinusoidal currents is limited by the switching frequency.

A low-bandwidth balanced sinusoidal voltage drive mode, which emulates a synchronous generator, should provide the best voltage power quality at the PCC. This is shown to be true both in simulation and practice, especially within weaker grid scenarios with existing voltage THD and unbalance. This is achieved by allowing significant levels of current unbalance and THD, and also by allowing significant power and energy ripple on the DC bus. One notable exception to this behavior is that the inverter will have a natural level of voltage unbalance which it produces due to component tolerances and calibration accuracy. Achieving and maintaining high accuracy over the lifetime of the inverter, including temperature and environmental effects, is a challenge. Therefore, there is the risk that the voltage drive mode may increase the level of

voltage unbalance at the PCC, if it is lower than the calibrated accuracy of the inverter itself.

At present, an inverter using any of the four control modes studied could be able to pass the tests of IEEE 1547, which specifies that the grid impedance during testing is at most $0.05j$ pu, and that the tests are done in an environment that can be as close to 0% voltage unbalance and 0% voltage THD as possible. However, the same inverter using the high-bandwidth power-flow ripple minimization mode could fail if the test conditions were instead set to 3% unbalance and 2.5% THD which IEEE 1547 also allows. Thus, the test conditions of IEEE 1547, as they stand, provide an somewhat random provision of "pass" or "fail", based upon the quality of the test facility power system, which is only loosely specified. It does little to predict what the actual impact on power quality at the PCC will be.

An inverter using any of the four control modes could also be granted certification under G5/4 stage 1, if they were tested in environments of low voltage THD and unbalance, and low grid impedance. However, under stage 2 and stage 3 analyses, if the devices were tested in environments of imperfect power quality or in-situ, other results could be obtained. The high-bandwidth power-flow ripple minimization mode might be failed. The dual-sequence and voltage drive modes might be recognized for their harmonic mitigation tendencies. The voltage drive mode might similarly also be recognized for its mitigation of unbalance. The dual-sequence mode might fail on unbalance in weak grids with resistive impedance components, if the pre-existing voltage unbalance was close to 2%, and the inverter was required to import active power during its operational cycle.

Any future standards governing the testing or certification of inverter hardware and controls for microgrids must take into account the potential effects of grid impedance and voltage power quality on the inverter response, and the interactions with the PCC (as G5/4 attempts to do). The testing should include scenarios of imperfect power quality, and appropriate grid impedance. The inverter must be tested in all its potential modes of control, especially if it is capable of switching between different modes in real-time based upon automatic or manual decisions. Knowledge of the control mode(s) might influence the tests, and test conditions, applied.

Finally, although the detailed studies in this paper focus on a single inverter connected to a grid (or microgrid), with a range of grid impedances, it must be remembered that many much smaller inverters with similar control algorithms may respond together in an aggregated fashion. Thus, although a grid may appear stiff to a single inverter, the grid may actually be considered weak when the aggregated set of inverters is considered. This is especially relevant in microgrid applications where many inverters or drives may be connected.

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