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Impact of Marine Power System Architectures on IFEP Vessel Availability and Survivability

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Abstract—**In recent years Integrated Full Electric Propulsion (IFEP) has become a popular power system concept within the marine community, both for the naval and the commercial community. In this paper the authors discuss the need for a detailed investigation into the impact of different IFEP power system architectures on the availability of power and hence on the survivability of the vessel. The power system architectures considered here could relate to either a commercial or a naval vessel and include radial, ring and hybrid AC/DC arrangements.**

Comparative fault studies of the architectures were carried out in an attempt to make valuable observations on the survivability of a vessel. Simulation results demonstrate that the ring and hybrid AC/DC architectural contribute to a higher survivability than the radial architecture. However, there are still challenges that need to be addressed and therefore potential solutions such as fault current limiters will be considered.

Index Terms—**Marine technology, power distribution, power system availability, power system protection.**

I. INTRODUCTION

THE introduction of Integrated Full Electric Propulsion (IFEP), and its associated characteristics such as higher generation and load levels, variable modes of operation, and the implementation of power electronics and novel loads, has resulted in a need for marine electrical system engineers to reconsider protection and reconfiguration philosophies. The presently adopted protection philosophy is mainly based on commonly used radial network architectures with coordinated overcurrent protection.

An example of a typical IFEP challenge can be illustrated through the fact that sometimes as little as 10% of the installed generation capacity may be used for a significant time duration, due to operational requirements; this may cause problems in terms of satisfying protection criteria such as speed and sensitivity, as the prospective fault levels will change in proportion with the connected generation. Also, reconfiguration of IFEP systems has become an area of interest over recent years. This is particularly true for the naval shipping industry where Fight Through Power (FTP) capabilities for naval vessels are essential for battle situations

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[1]. In [1] naval vessel survivability is defined as a combination of avoiding a threat (susceptibility), withstanding a casualty (vulnerability) and recovering from a casualty (recoverability). This paper will focus on the vulnerability and recoverability. The vulnerability and recoverability can be represented in a 3D model as illustrated in Fig. 1 [2].

Point (1,1,1) represents the maximum survival state of the vessel, in which a naval vessel can fight unrestricted with all its available systems [2]. This model consists of three components including "structural integrity" (bottom surface), "battle systems" (front surface) and "mobility systems" (left surface). As IFEP systems provide power for propulsion and radar systems that are related to "mobility systems" and "battle systems", any degradation of the delivering of power to these components has a significant impact on the vessel's survivability. Network architecture is therefore a critical element in assessing survivability.

In commercial applications, survivability may also be influenced by a non-combat related incident, e.g. a short-circuit fault on the network, the tripping of a gas turbine/generator, etc. Such non-combat incidents can also affect naval vessels. A similar 3D model as in Fig. 1 can be used for commercial applications as well where "battle systems" can be replaced by just navigational equipment such as radar.
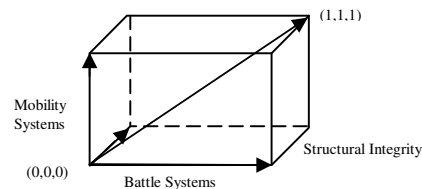

Fig. 1. Survivability state components after hit [2]

A number of alternative IFEP power system architectures have been discussed such as radial and ring [3] [4]. In [4] and [5], hybrid power system architectures are considered, where there is a combination of AC and DC distribution. In addition, different configurations of commonly used radial and ring architectures have also been presented [6]. Although numerous IFEP power system architectures exist and have been proposed, little discussion has been conducted with respect to the impact of different architectures on system protection and reconfiguration. This has the potential to affect the availability

of electrical power and therefore the survivability of the vessel (Fig. 1).

As indicated in [2], quantification of survivability is difficult if not infeasible. It has therefore been suggested that a relative comparison would be more appropriate [2]. Therefore three IFEP power system architectures; a commonly used radial architecture, a ring and a hybrid AC/DC will be compared against each other in order to ascertain their respective survivability contributions to vessels. Although 3 architectures are considered here, other existing and concept architectures can be included in a similar study. In the following sections of the paper, an introduction to the 3 architectures will be discussed. Simulation results from behavioral models for each of the architectures will be used.

II. POWER SYSTEM ARCHITECTURES FOR IFEP

Table 1 presents examples of each of the three architectures, with references to actual applications of these architectures.

TABLE 1 IFEP ARCHITECTURE EXAMPLES

	Radial	Hybrid	Ring
Application	Military/Commercial	Military	Military/Commercial
Example	Type 45 [4][7]	DDG1000 [8]	RFA *Sir Bedevere* [3]

A. Radial Architecture

A typical modern electric ship architecture follows the radial design [6] with MV connected generation units in large capacity systems; generation may be connected at LV in smaller capacity applications. Fig. 2 represents one "half" of a typical marine radial architecture.
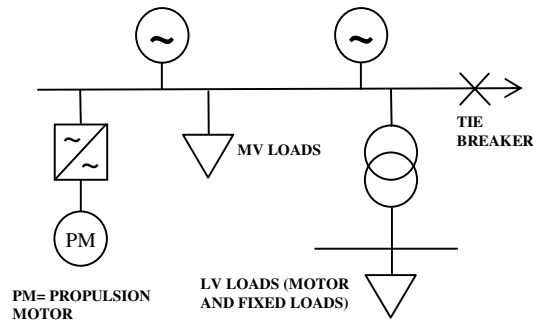

Fig. 2. Radial IFEP Architecture

Overcurrent protection is commonly used for such architectures. This approach relies on inverse time-current relays that protect each feeder in the system. All relays in the system should be set to operate in a coordinated fashion. Therefore, faults on a lower feeder level will be cleared by the relays on this level before the feeder protection at a higher level will attempt to clear this fault on backup.

B. Ring Architecture

Fig. 3 represents one "half" of a typical ring main architecture where multiple generation sources are connected in parallel. This architecture can be found on vessels such as offshore supply vessels with Dynamic Positioning (DP) equipment [10]. Rules and regulations allow DP class 3 [11] operation with closed tie breakers, provided that a fault can be detected and isolated before healthy parts of the system are tripped.
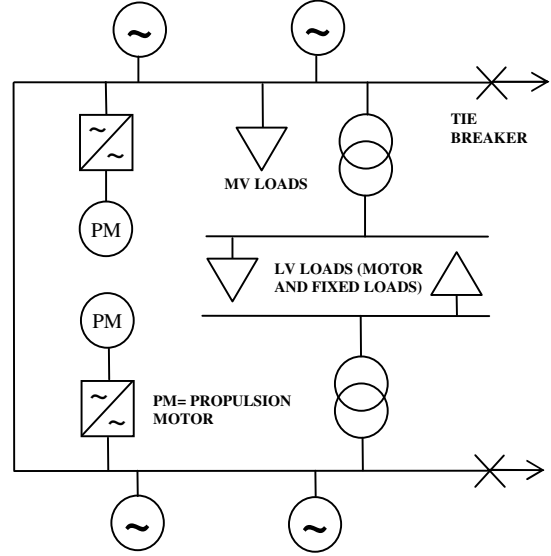

Fig. 3. Ring IFEP Architecture

In the case of a fault on this architecture, alternative paths can be used to maintain supply to other parts of the systems. Such architectures possess multiple sources and fault current flows can be bi-directional, depending on fault location; therefore protecting such systems can be relatively complex and may require the use of directional relays. However, after reconfiguration, where the supply paths may have changed, the protection configuration and settings may require re-evaluation. This may present challenges and more effective solutions must be considered.

C. Hybrid Architecture

Within the marine community there has been a debate for some time regarding DC versus AC power distribution systems [3], [4], [5], [8], [9]. The use of DC distribution offers certain advantages over AC distribution such as higher power transfers for similar voltages, unity power factor, no frequency synchronization for connecting ac systems coupled via a DC bus, no AC noise coupling, etc.

Associated disadvantages of DC power distribution systems such as no zero crossing to aid fault interruption, weight and cost, means that in many cases AC remains the first choice for marine power systems. However, if cost is not the dominating factor, the advantages outweigh the disadvantages of DC distribution systems; this can be seen in modern applications such as space- and fighter crafts and naval vessels where DC is used [8].

However, most naval mission systems, such as Electro Magnetic Aircraft Launch System (EMALS), weapons systems, communications and radar systems, require a DC

supply. This is also the case for future high power weapon systems such as rail guns and lasers [8]. Furthermore, the breaking of DC fault currents has always been very difficult, although research into electro-mechanical hybrid and solid-state current interruption has shown promising results [12].

Papers [4] and [5] suggest the use of a hybrid IFEP power system (Fig. 4.), consisting of both AC and DC distribution systems. In this case, the AC distribution subsystem is used to distribute energy from the generator sets to the propulsion motors. Each DC zone can be supplied through either of the 2 supply paths in order to improve redundancy.

Paper [8] mentions the use of an Integrated Fight Through Power (IFTP) system for the US DDG-1000 destroyer program where a 60Hz, 4160VAC system provides power for the propulsion system; IFTP rectifiers supply a 1000 VDC distribution system for other vessel loads.

This hybrid architecture presents research challenges in terms of system protection and reconfiguration. For example, faults in the DC network may cause very high fault current peaks due to stored energy within capacitors used for voltage smoothing purposes.
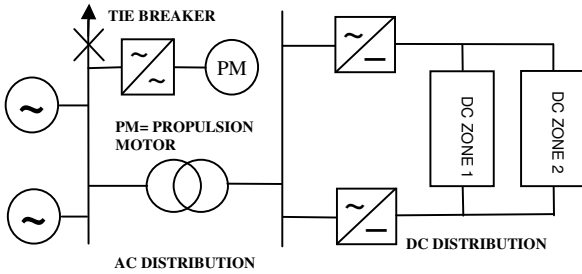

Fig. 4. Hybrid AC/DC IFEP Architecture

III. POWER SYSTEM PROTECTION

Anecdotal evidence has shown that on modern ships, spurious tripping and mal-operations do occur. To limit the impact of excessive fault currents, devices such as Super-conducting Fault Current Limiters (SFCL) and series-in line reactors have been researched and demonstrated. Such devices, and the increasing use of power electronic devices, will act to reduce fault current levels and this has the potential to cause problems for power system protection discrimination and operation.

A. Power Converters

Coordination of protection across the AC/DC interface and ensuring converter device protection acts in harmony with the power system protection is also a challenge that must be addressed. Power converter devices consist of semiconductors of which the thermal mass is low. This means that an over current will cause the temperature to rise rapidly beyond its safe limit. Since mechanical breakers often rely on clearing the fault at a subsequent current zero, this method is too slow to protect the semiconductors. To protect the semiconductor from overcurrents, fuses are used which are faster then the mechanical breakers [13]. However, if the converter is in the

path between a faulted section and the rest of the system, the fuses may act before the power system protection can act, which should be the case to preserve system integrity and protection system discrimination.

B. Fault Current Limiters

To limit fault currents, devices such as SFCL and series in-line-reactors can be used [6]. Conventional power system protection methods are based on overcurrent protection. However, fault level limiters such as SFCLs will make it difficult to establish a distinction between faults and other "natural" phenomena such as motor starts and inrush currents associated with transformer energisation. Unit protection based methods such as differential protection may be used but overcurrent backup protection will still have the same problems as aforementioned. Furthermore, excessively limited fault current may result in slow or non-operation of conventional current-based protection systems.

IV. SIMULATION AND RESULTS

In order to assess the impact of the different IFEP architectures on the survivability of the vessel, a comparative study has been carried out. The aim of this study has been to compare the fault current peaks for different IFEP architectures when a fault is applied. To make a fair comparative study, the total installed generation capacity is the same for each of the three architectures, which in this case constitutes 4 generator units. All three architectures used the same data and ratings in terms of generator, transformer, load, etc. Table 2 presents an overview of the data used in the models. Generator preset models were used to obtain realistic data such as generator reactances and rotor inertia. The system models were developed and simulated in SimPowerSystems, a toolbox within Matlab/Simulink® [14]

TABLE 2 COMMON IFEP MODEL PARAMETERS

Generators	10MVA, 6.6kV
Fixed MV load	5MW, pf0.85
Fixed LV load	2.125MW, pf0.85
Transformer (Dyn)	3MVA, 6.6kV/0.44kV
Leakage inductance transformer	0.045p.u.
6.6kV cable (per phase); 10,20m	0.22988 Ω/km
0.44kV cable (per phase); 10m	0.148 Ω/km

For comparative analysis of the performance of each system under fault conditions, a three-phase fault was applied to the LV side of the radial and ring system. A positive to negative fault was applied to the LV DC side of the hybrid system. Only the fault on the hybrid system was cleared in order to see the regulating action of the rectifier controller.

The three-phase fault condition is the worst-case scenario in terms of fault levels; therefore these fault conditions were used in the case studies in this paper. Although these fault conditions are rare, these conditions are credible and are encountered in practice. The letters in Fig. 5, Fig. 10, and Fig. 15 are used to illustrate the locations where measurements have been taken and to represent the applied fault locations.

Both the radial and the hybrid AC/DC architecture model have 2 generators since in this case study only one "half" of the network with in total 4 generators is modeled; for these architectures it has been assumed to operate the network with an open tie breaker. In order to model a ring architecture involving the entire network, the model contains all 4 generators.

A. Performance of the radial architecture

1) Simulation procedure and results

The radial architecture (one half of the split running system) was modeled as shown in Fig. 5. A three phase fault was applied at location D at time t=1s. The simulation results relating to this are presented in Fig. 6 to Fig. 9.
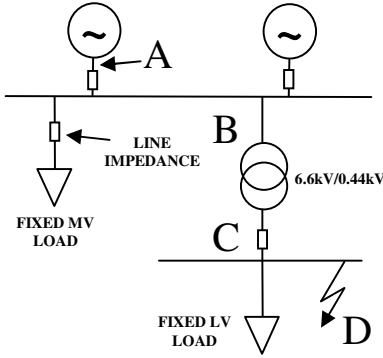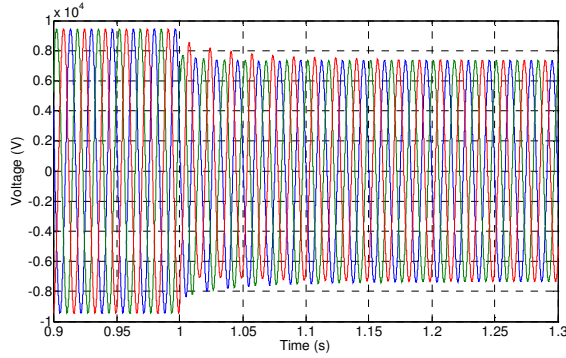
Fig. 5. Radial IFEP Architecture with Fault
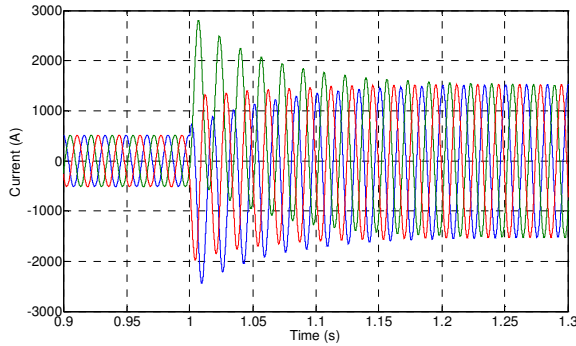
Fig. 6. L-L voltages at location A

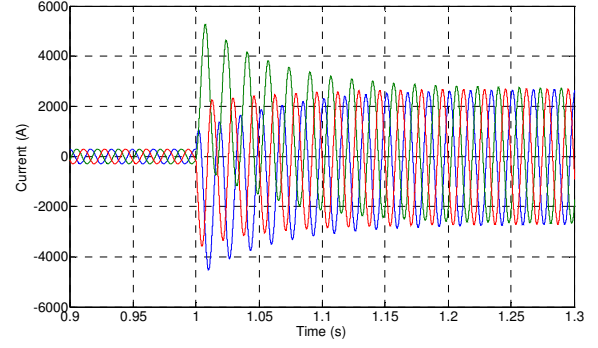Fig. 7. Currents at location A

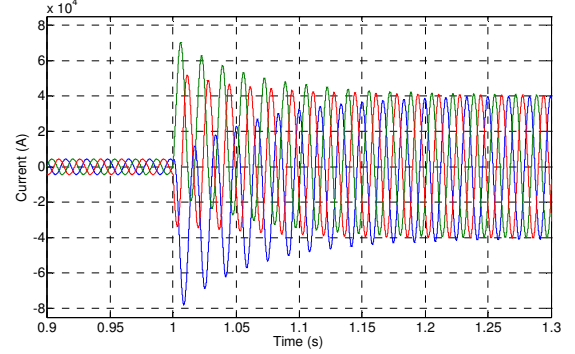Figure 8 Currents at location B

Fig. 9. Currents at location C

2) Comments and observations

The voltage drop as shown in Fig. 6 is approximately 22%. The currents are presented in Table 3 where "I_{peak}" is the peak current due to the fault and "factor" represents I_{peak} as a multiple of the nominal current.

TABLE 3 RADIAL CURRENTS

Location	A	B	C
I_{peak} (kA)	2.8	5.26	78
factor	5.4	18	17.8

The currents are considerable and the level depends on the impedance between the fault and on the nature of the energy source. Other studies conducted by the authors have revealed fault currents in excess of 200kA peak for high-capacity marine power systems. As expected, the corresponding voltage close to the fault location collapses to almost 0, not shown in the paper. There is also a depressing impact on the MV voltage, but this is buffered through the impedance of the transformer in the fault current path. This is shown in Fig. 6 and Fig. 7. Not shown in this paper is the current of the LV load which collapses, the degree of collapse depending on the fault path impedance.

The approximate voltages and currents drop of the MV load are 22% and 18% respectively (plots not shown).

B. Performance of the ring architecture

1) Simulation procedure and results

The IFEP ring architecture has been modeled with 4 generators as shown in Fig. 10. The reason to have 4 generators has been explained at the beginning of this section.

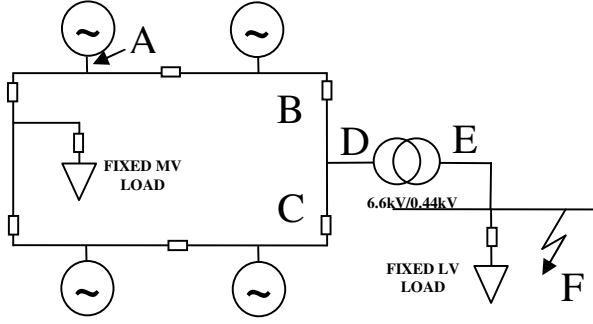At time t=1s, a three phase fault was applied on the LV side at location F.

Fig. 10. Ring IFEP Architecture with Fault

Since the ring architecture is symmetrical in length and therefore in cable impedance, the voltages and currents observed at B and C should be essentially equal. The simulation results relating to this architecture are presented in Fig. 11 to Fig. 14.
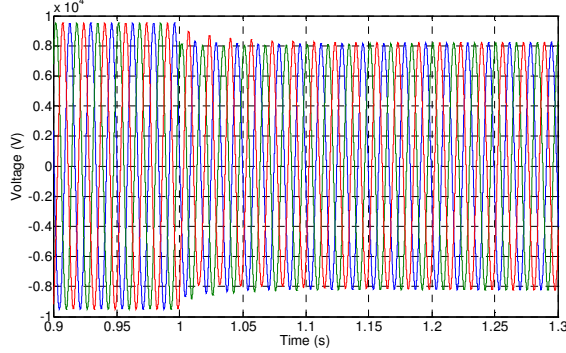

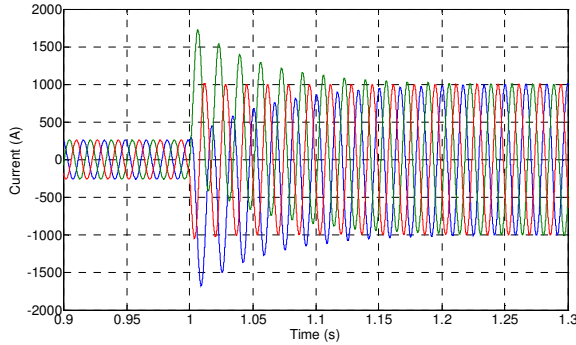Fig. 11. L-L voltages at location A

Fig. 12. Currents at location A

2) Comments and observations

The voltage drop in Fig. 11 due to the LV fault is approximately 14%. Similar voltage drops can be observed at location B, C, D and other generators although not shown in this paper. Some of the currents in the system are represented in Table 4 where E represents the fault current.

TABLE 4 RING CURRENTS

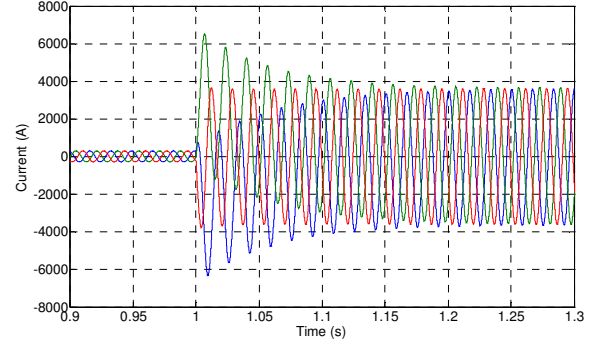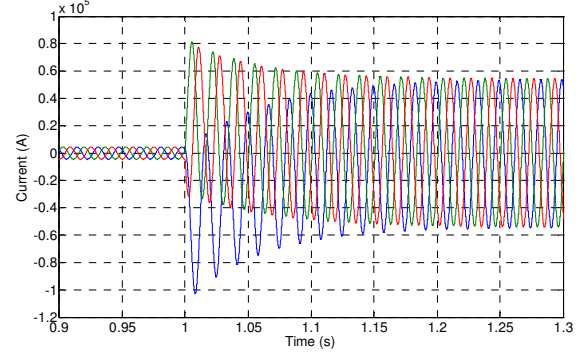| Location	A	B	D	E
I_{peak} (kA)	1.726	3.265	6.53	103
factor	6.6	22	21.8	23.4

Fig. 13. Currents at location D

Fig. 14. Currents at location E

Although not shown in this paper, the MV load voltage and current drops are both approximately 14%.

Furthermore, the potential for bi-directional current flow in such architectures may result in a more complex protection solution being required. This would be the case if a fault would occur on the MV bus in Fig. 10. Problems with fault level variability due to different proportions of generation being in-service and different ring configuration being used may also be experienced.

C. Performance of the hybrid AC/DC architecture

1) Simulation procedure and results

Fig. 15 represents (one half of the split running system) a hybrid AC/DC IFEP architecture. A 6-pulse controlled thyristor rectifier was used to control the DC voltage. A capacitor with a value of 0.05F was used to smooth the voltage output. At time t=1s, a positive to negative DC rail bus fault was applied (location F); after 100ms the fault was cleared.
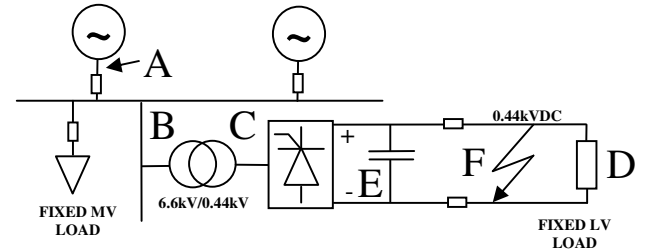

Fig. 15. Hybrid AC/DC IFEP Architecture with Fault

Fig. 16 shows a block diagram for the control system of the thyristor subsystem. The DC voltage V_{dc} is measured and

compared with the required DC voltage; V_{dc*}. The output of the pulses block regulates the firing angle, α, which in turn determines the average voltage V_{dc}. For rectifier operation where a negative V_{dc} is to be avoided, α can not be more than 90°. Therefore the output of the PI controller is limited between 0° and 90°.
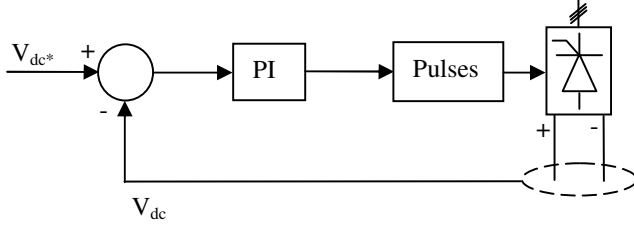

Fig. 16. Control scheme for thyristor

This simulation results are shown in Fig. 17 to Fig. 23.
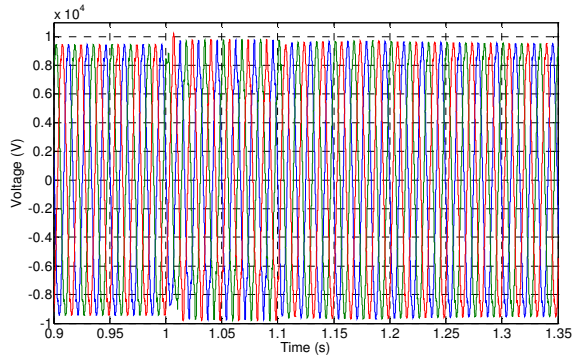
Fig. 17. L-L voltages at location A
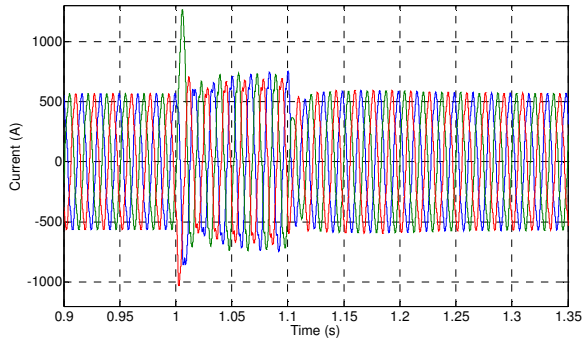
Fig. 18. Currents at location A
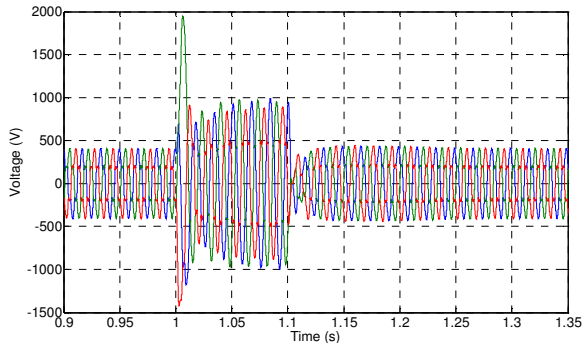
Fig. 19 Currents at location B

Fig. 20. Currents at location C

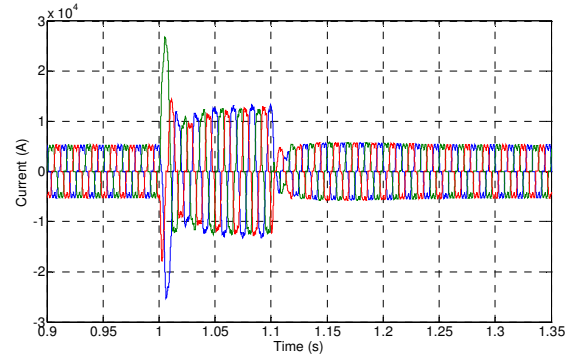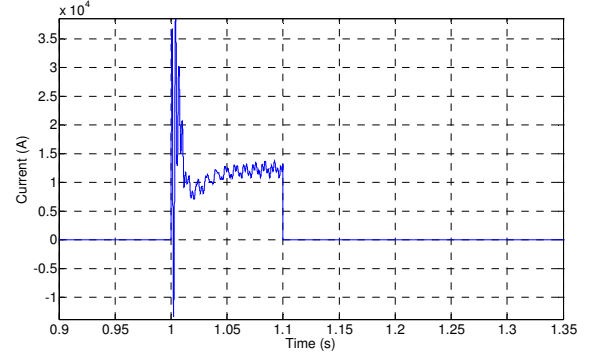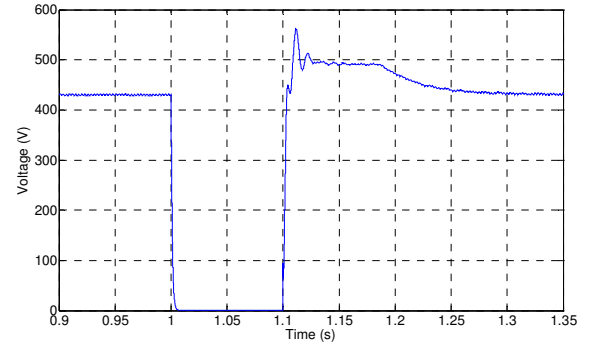Fig. 21. Fault Current at location F

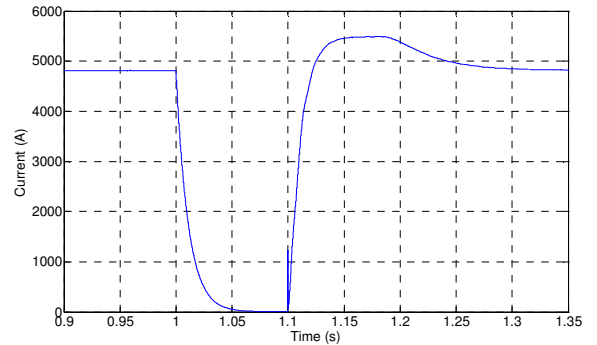Fig. 22. DC voltage at location D

Fig. 23. DC current at location D

2) Comments and observations

It can be noticed from Fig. 17 and Fig. 18 that the impact of a fault at the LV side on the MV side is not as severe as is the case for the radial and ring architectures.

Not shown in this paper are the voltage and current drops of

19

the MV load; there is a short (10ms) voltage and current drop of approximately 11% and 8% respectively. About 10ms after the fault occurs, the MV load voltage increases to a value which is approximately 3% more then the nominal voltage. The voltage levels are restored after the fault is cleared. This voltage profile is similar to the voltage profile at location A, Fig. 17

Table 5 represents the peak currents at several locations in the system as illustrated in Fig. 15. "E" and "F" are the capacitor and peak fault current respectively.

TABLE 5 HYBRID CURRENTS

Location	A	B	C
I_{peak} (kA)	1.26	1.95	26.9
factor	2.2	4.8	5.1
	E	F	Thyristor
I_{peak} (kA)	41.5	38.4	41.6

Fig. 21 shows the peak fault current at location F, which is of the order of 38kA due to the instantaneous discharge of the stored energy within the capacitor into the short circuit. This represent a significant challenge and fault containment, energy dissipation and voltage surge arresting technologies may be required to mitigate against such high-energy discharges. The oscillations in Fig. 21 are due to the interaction between the capacitance and inductance in the system. Fig. 22 and Fig. 23 show the DC bus bar voltage and current respectively.

Not shown are the thyristor peak fault currents of 41.6 kA, which may cause fuses inside the converter to trip. As explained before, a fuse trip in the converter may cause spurious tripping and mal-operation of the power system protection.

After the fault is cleared at t= 1.1s, the system takes approximately 0.2s to regulate the voltage back to the desired value. This is due to the saturation of the PI controller. V_{dc} experiences oscillation with an overshoot of 27% before it settles as shown in Fig. 22. As the circuit is inductive, a freewheel diode was connected parallel to the load.

D. Comparison of architectures

Table 6 compares the three IFEP architectures for faults on the LV side of the system. The radial architecture was used as a benchmark since this is the most commonly used architecture at present. All results have been normalized with respect to the results of the radial architecture. The letter behind the value refers to the measurement point of that particular architect; either in Fig. 5, Fig. 10 and Fig. 15.

TABLE 6 COMPARISON OF IFEP ARCHITECTURES

Architecture	Radial	Hybrid	Ring
Current levels LV	1 (C)	0.49 (F)	1.32 (E)
Current levels MV	1 (B)	0.37 (B)	1.24 (D)
Voltage drop MV load	18-22%	8-11%	14%
Criteria comparison			
Protection system	0	-	-
Vulnerability (P_V)	0	0	0
Recoverability (P_R)	0	+	+

Comparing the radial with the ring architecture, the peak fault currents on the LV and MV side are higher for the ring architecture; a factor 1.32 and 1.24 times respectively as illustrated in Table 6. This is because of an increased number of generators and reduced fault path impedance due to parallelism within the network. As more power is available in the ring network than in the radial network, the MV side and therefore the MV load seems to be affected less than it is the case with the radial network. This can be concluded from the comparison of the MV load voltage and current drops which is 18-22% and 14% for the radial and ring architecture respectively. As MV load will include propulsion power, it can be seen from Fig. 1 that "mobility systems" play an important part in the survivability of a vessel.

The hybrid AC/DC architecture has a lower LV and MV peak fault current than the radial architecture, a factor 0.49 and 0.37 less respectively. The MV load voltage and current drops of 11% and 8% respectively are less than that of the radial and ring architecture.

Criteria such as vulnerability and recoverability have also been subjectively compared against the radial architecture which was given the baseline value of 0. This comparison as illustrated in Table 6 will be discussed below.

In terms of protection challenges, the radial architecture requires the least complex protection system, as overcurrent protection may well be sufficient. This in contrast to the hybrid AC/DC architecture which suffers from issues relating to DC fault current breaking and converter protection. Also the protection for the ring is more complicated than the protection for the radial architecture as bi-directional protection will be required for faults on the MV bus. The hybrid AC/DC and ring are given the same protection complexity level as a comparison between these two architectures would be too arbitrary.

Assessment of the vulnerability of each of the architectures is difficult at this stage. Equipment such as power converters are mounted on shock absorbing devices so they should withstand a certain level of shock for example due to a missile hit. However, damage to auxiliary equipment such cooling systems may damage systems such as power converters and transformers. All of these systems can be found on either of the architectures.

In terms of recoverability both the ring and hybrid AC/DC architecture offer advantages over the radial architecture. If for example the cabling on one side of the vessel is damaged, the power can be rerouted to the healthy other part of the network.

Assuming the susceptibility (P_X) and vulnerability (P_V) are equal for all three architectures, the survivability (P_S) [2] can be expressed as (1) where P_R is the recoverability.

$$P_S = 1 - (P_X . P_V)(1 - P_R) \qquad (1)$$

From Table 6 and (1), it can be seen that without knowing the vulnerability and susceptibility, the P_S is already higher for the ring and hybrid AC/DC architecture than the P_S for the

radial architecture.

V. POTENTIAL SOLUTIONS AND FUTURE WORK

Devices such as SFCLs, in-line-reactors, fuses, etc. can be used as fault-containment and limiting devices. However, these devices may disrupt the proper operation of the power system protection. Investigation into what degree the fault currents should be reduced (if at all) are necessary to establish a balance between possible damage due to high fault levels and the use of current limiters which may result in improper operation of the power system protection.

Further investigation into the propagation of damage to the loads due to a fault is required; in particular for DC systems as sensitive equipment will be connected to the DC bus.

Apart from using devices that limit/contain fault levels, investigations must also focus on removing the cause of excessive fault levels. For example, removing or reducing the value of the smoothing capacitor in the hybrid architecture may reduce the fault current peak, but this may require alternative converter technologies to be used.

Investigation into adaptive or predictive protection settings in combination with reconfiguration methods is also necessary to improve the survivability of vessels. In particular this is true for ring architectures where there are multiple fault current paths possible and in situations where fault currents may be subject to very wide variation depending on the prevailing generation and system configuration.

Lastly, the electro-mechanical interactions of large prime movers and loads must also be considered during fault conditions to ensure that they do not have a detrimental effect on the operation of protection systems.

VI. CONCLUSION

The study has shown that both the ring and the hybrid AC/DC architecture have a higher survivability than the radial architecture. If taking into account the DC advantages as aforementioned and the results of the fault study, the hybrid AC/DC architecture seems to be the favorable architecture over the ring architecture.

However, challenges such as protection coordination and high peak fault currents need to be addressed. Solutions may be found in combining architectures and using devices such as SFCLs and surge arresters. This offers scope for further research as the relative comparison approach outlined in this paper can be used to evaluate the impact of the suggested solutions on the vessel's survivability.

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