(12) UK Patent Application (19) GB (11) 2462770 (13) A

(43) Date of Printing by UK Office 24.02.2010

(21) Application No: 0921638.3

(22) Date of Filing: 30.05.2008

(30) Priority Data:
(31) 0710377 (32) 31.05.2007 (33) GB

(86) International Application Data:
PCT/GB2008/001821 En 30.05.2008

(87) International Publication Data:
WO2008/145995 En 04.12.2008

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(51) INT CL:
G06F 15/82 (2006.01)

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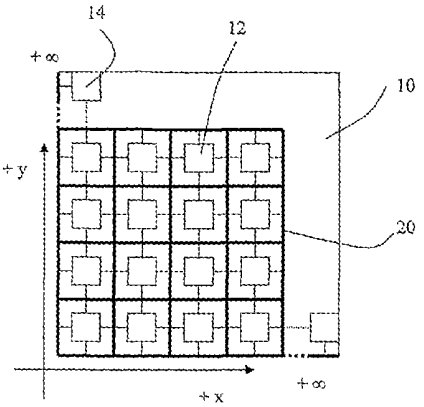
(58) Field of Search by ISA:
INT CL G06F
Other: EPO-Internal

(54) Abstract Title: **Processors**

(57) A processing apparatus comprises a plurality of processors (12), each arranged to perform an instruction, and a bus (20) arranged to carry data and control tokens between the processors. Each processor (12) is arranged, if it receives a control token via the bus, to carry out the instruction, and on carrying out the instruction, to perform an operation on the data, to identify any of the processors (12) which are to be data target processors, and to transmit output data to any identified data target processors, to identify any of the processors which are to be control target processors, and to transmit a control token to any identified control target processors.

Fig. 1



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