COMMUTATION PROCESSES IN MULTIRESONANT ZVS BRIDGE CONVERTER

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Summary The analysis of the multiresonant ZVS DC/DC bridge converter is presented. The control system of the converter is based on the method of frequency control at the constant time of transistor turn-off with a phase shift. The operation of the circuit is given and the operating range of the converter is defined where ZVS switching operation is assured. Control characteristics are given and the converter's efficiency is defined. The circuit's operation is analysed on the basis of results of the converter simulation tests using Simplorer programme.

1. INTRODUCTION

The interest in multiresonant power converters DC/DC (MRCs), switched at high operating frequency is prompted by attempts to obtain great efficiency, minimize dimensions, and in effect to reduce cost of such circuits. Topologies of MRCs remain a widely studied issue, as demonstrated by numerous, though not exhaustive papers, published in periodicals and conference materials [2,4,5,6].

The reference [1] presents analytical study of an indirect DC/DC converter using a bridge series resonant inverter operating above the resonant frequency. ZVS mode is obtained in the inverter, when a phase shift is introduced between the controls of the two legs. For purposes of the analysis, ideal (i.e. without power losses and time delays) semiconductor elements were assumed.

This article discusses a multiresonant ZVS bridge converter (ZVS bridge MRC) comprising real semiconductor elements. The article presents an analysis of the circuit's operation on the basis of results of the converter simulation tests using Simplorer programme.

2. TOPOLOGY OF MULTIRESONANT ZVS BRIDGE CONVERTER

The structure of ZVS bridge MRC is shown in Figure 1 [3]. The circuit is supplied with DC voltage E. MOSFETs $T_1 \div T_4$, at conductance resistances $R_{T1} \div R_{T4} = R_T$ and output capacitances $C_{OS1} \div C_{OS4} = C_{OS}$, are switched at frequency f. Diodes $D_{S1} \div D_{S4}$ are integral parts of the transistors and enable bi-directional conductance of currents $i_{S1} \div i_{S4}$. Snubber capacitors at $C_{S1} \div C_{S4} = C_S$, in parallel with transistor output capacitances, assist switching processes in the resonant circuit.

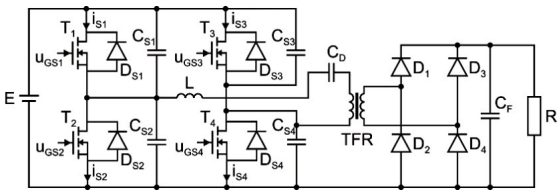


Fig.1. ZVS bridge MRC

Capacitor at C_D, reactor at inductance L, and transformer TFR are elements of the series resonant circuit. The reactor's L quality factor is assumed to be very high, therefore, the impact of its resistance is negligible. TFR separates the load resistance R from the resonant circuit. The transformer's leakage and main inductances are parts of the resonant inductance. The output circuit, consisting of TFR, rectifier and capacitor at C_F, is in series with the capacitor C_D. The rectifier contains fast recovery diodes $D_1 \div D_4$ of junction capacitances $C_{OD1} \div C_{OD4} = C_{OD}$. Capacitor at C_F is a low-pass filter limiting ripples of the converter's output voltage.

3. CONTROL ALGORITHM OF THE MULTIRESONANT ZVS BRIDGE CONVERTER

The converter in Figure 1 is controlled using the control system based on the method of frequency control at the constant time of transistor turn-off t_{off} with a phase shift. Within the full range of pulse width variation, the area of ZVS mode in the converter is limited. In this area, transistors begin to conduct when diodes, as integral parts of transistors, stop conducting. Transistors are turned off at approximately zero value of drain-source transistor voltage.

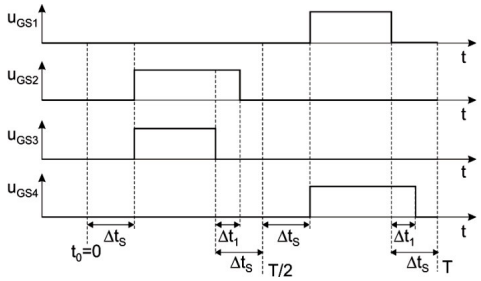


Fig.2. Control signals algorithm of the ZVS bridge MRC shown in Figure 1

Figure 2 shows control signals $u_{GS1} \div u_{GS4}$, supplied to $T_1 \div T_4$ of the converter (Fig. 1). The control signals are divided in two groups:

- the first group, including u_{GS1}, u_{GS3}, controls the upper bridge transistors: T_1, T_3,

- the second group, including u_{GS2}, u_{GS4}, controls the lower bridge transistors: T_2, T_4.

u_{GS1}, u_{GS3} are distributed centrally in the middle of the converter's operation period $\Delta t=T/2$. T_3 is turned on with a delay time Δt_S in relation to the initial moment $t=t_0$ of T. T_3 is turned off Δt_S prior to $t=T/2$. Turn-on and turn-off of T_1 are in the analogous manner in the second half of the converter's operation period. The delay time Δt_S is expressed:

$$\Delta t_s = \frac{\beta \cdot T}{2} \text{ for } \beta \in (0 \div 0{,}5) \tag{1}$$

where: T – period of the converter's operation; $T=1/f$, Δt_S – delay time of the one group of transistors, β – modulation factor of delay time Δt_S.

The control signals u_{GS2} and u_{GS4} are turned on at the same instants as the corresponding u_{GS3} and u_{GS1} of the first group, with a time delay Δt_S. T_2, T_4 are turned off with a delay Δt_1 in relation to the time of turn off of T_3, T_1. The delay Δt_1 is expressed:

$$\Delta t_1 = (1-\gamma) \cdot \Delta t_s \text{ for } \gamma \in \langle 0; 1 \rangle \tag{2}$$

where: Δt_1 – delay of second group transistor turn-off in relation to the time of first group transistor turn-off, γ – delay factor of control signals of second group transistors.

At $\gamma=1$, transistors in the same leg (e.g.: T_1, T_4) are turned off at the same moment. At $\gamma=0$, transistors T_2, T_4 are turned off at: $t=T/2$ and $t=T$, respectively.

Transistors are characterised by delay times of: turn-off t_{off} and turn-on t_{on}, where $t_{off} > t_{on}$. To avoid short-circuits in bridge legs (T_1,T_2), (T_3,T_4) the criterion of minimum delay of control signals must be fulfilled, as expressed in:

$$\beta > \frac{2 \cdot (t_{off} - t_{on})}{(1+\gamma) \cdot T} \tag{3}$$

4. OPERATION OF THE CIRCUIT

In respect of topology and control algorithm, a bridge converter is divided in two symmetrical circuits including the transistors T_1, T_4 and T_3, T_2. Due to the symmetry, operation of only one leg will be discussed, containing T_3, T_2, for which the control signals are shown in Fig. 2, at $\gamma=0.5$. Values of β and γ are assumed, for which the ZVS criterion is met. Converter current and voltage waveforms, obtained in simulation testing, are presented in Figure 3. The resonant circuits for individual time intervals are shown in Figure 4.

Resonant circuit consists of C_D, L and TFR. Application of a transformer in series with a resonant circuit, causes junction capacitances of diodes $D_1 \div D_4$, inductances of the secondary circuit and load resistance R to become elements of the resonant circuit as well. The complex configuration of the connections among these elements poses significant difficulty for theoretical calculation of the resonant circuit frequency. The notation for the resonant frequencies during a full cycle of the converter operation are following:

- f_{01} – resonant frequency of the circuit whose topology is shown in Fig. 4a,
- f_{02} – resonant frequency of the circuit whose topology is shown in Fig. 4c,
- f_{03} – resonant frequency of the circuit whose topology is shown in Fig. 4d.

Resonant frequency f_0 of the circuit including L, C_D is expressed:

$$f_0 = \frac{1}{2\pi \cdot \sqrt{L \cdot C_D}} \tag{4}$$

At the instant $t=t_1$ (Fig. 3a), the control signals u_{GS3}, u_{GS2} are fed with a delay time Δt_S with respect to $t=t_0$ of the cycle origin. In the time interval ($t_1 \le t \le t_2$), however, T_3, T_2 do not begin to conduct since the direction of the resonant current i_L enforces current conductance by D_{S3}, D_{S2}. In the time interval ($t_0 \le t \le t_2$), i_L of the frequency f_{01} occurs in the circuit: L, C_D, TFR, D_{S3}, E, D_{S2} (Fig. 4a). At the instant $t=t_2$, the value of i_L is zero, changing the direction of conductance.

In the time interval ($t_2 \le t \le t_4$) (Fig. 3a,b), T_3, T_2 conduct i_L of f_{01} in the circuit: R_{T2}, L, C_D, TFR, R_{T3}, E (Fig. 4b). At the instant $t=t_3$, u_{GS3} of T_3 is turned off. Due to the delay in turn-off of T_3, related to t_{off}, the process of commutation of i_{S3} with the currents: i_{CS3}, i_{CS4} begins at the moment $t=t_4$ (Fig. 3b).

In the time interval ($t_4 \le t \le t_6$) (Fig. 3b), C_{S3} overloads in the circuit: C_{S3}, E, R_{T2}, L, C_D, TFR (Fig. 4c) The current of C_{S3} commutes with i_{S3} of T_3, at the growing R_{T3}. At the same time, the energy stored in L causes C_{S4} to discharge in the circuit: L, C_D, TFR, C_{S4}, R_{T2}. The output capacitance C_{OS4}, in parallel with C_{S4}, also discharges, as proven by the negative value of i_{S4} in the time interval ($t_4 \le t \le t_6$). The resonant frequency f_{02} of C_{S3}, C_{S4} discharge is greater than f_0 due to the series connection of C_{S3}, C_{S4} with C_D. At the instant $t=t_5$, the control signal u_{GS2} is turned off. Owing to the delay of t_{off}, the transistor T_2 conducts current until $t=t_6$. At the instant $t=t_6$, i_{S2} of T_2 begins to commute with i_{CS2} and i_{CS1}. At the same time, the process of discharging C_{S1} and C_{S2} begins.

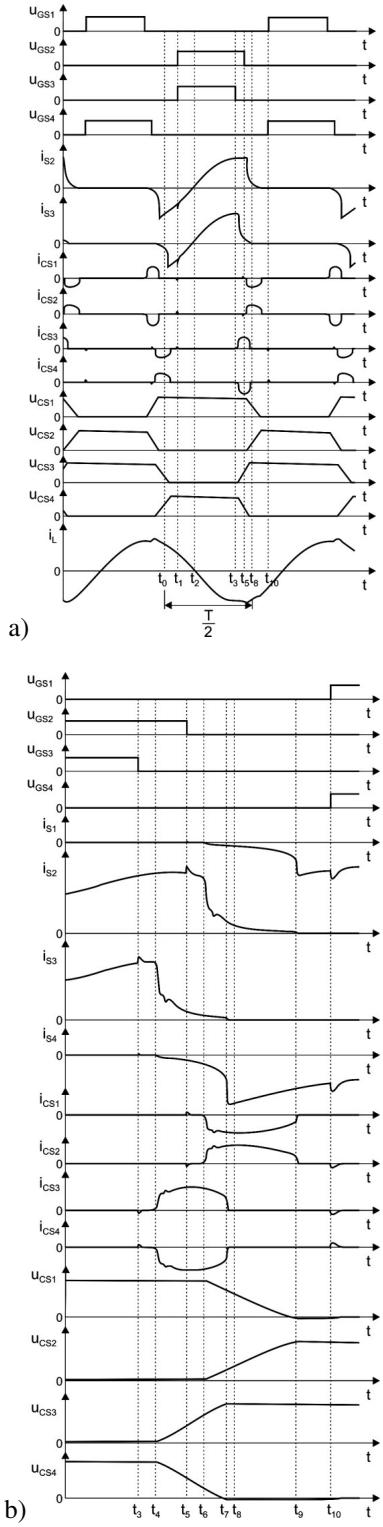


Fig.3. Current and voltage waveforms in the ZVS bridge MRC shown in Fig. 1, a) during a half of the operation cycle Δt=T/2 b) at switching between legs of T_3, T_2 and T_4, T_1

In the time interval ($t_6 \le t \le t_7$) (Fig. 3b), the energy stored in L enables discharge of all capacitors in parallel with transistors at f_{03} (Fig.4d). C_{S2} discharges in the circuits: L, C_D, TFR, $C_{S4}||C_{OS4}$, C_{S2}, and L, C_D, TFR, $C_{S3}||C_{OS3}$, E, C_{S2}. In the course of this discharge, i_{CS2} commutes with i_{S2} of T_2, at the growing R_{T2}. In this time interval, loading of C_{S3} with i_{CS3}, and of the output capacitance C_{OS3} with i_{S3}, come to the end. C_{S1} discharges in the circuits: L, C_D, TFR, $C_{S3}||C_{OS3}$, $C_{S1}||C_{OS1}$, and L, C_D, TFR, $C_{S4}||C_{OS4}$, E, $C_{S1}||C_{OS1}$. The output capacitance C_{OS1}, which also discharges with i_{S1}, is in parallel with C_{S1}. At the instant $t=t_7$, voltages: $u_{CS4}=-u_{DS}$ and $u_{CS3}=E+u_{DS}$. The process of commutation of i_{CS4}, i_{S4}, i_{CS3} by D_{S4} begins, and charging of: $C_{S4}||C_{OS4}$, $C_{S3}||C_{OS3}$ ends.

In the time interval ($t_7 \le t \le t_9$) (Fig. 3b), $C_{S2}||C_{OS2}$, $C_{S1}||C_{OS1}$ continue to discharge at the frequency f_{02} owing to the energy stored in L in the circuits: L, $C_{S2}||C_{OS2}$, D_{S4}, TFR, C_D, and L, $C_{S1}||C_{OS1}$, E, D_{S4}, TFR, C_D (Fig. 4e). At the instant $t=t_9$, voltages: $u_{CS1}=-u_{DS}$ and $u_{CS2}=E+u_{DS}$, and values of i_{CS2} and i_{S2} are zero. At the instant $t=t_9$, commutation of i_{CS1}, i_{CS2}, i_{S2}, by i_{S1} of D_{S1} begins.

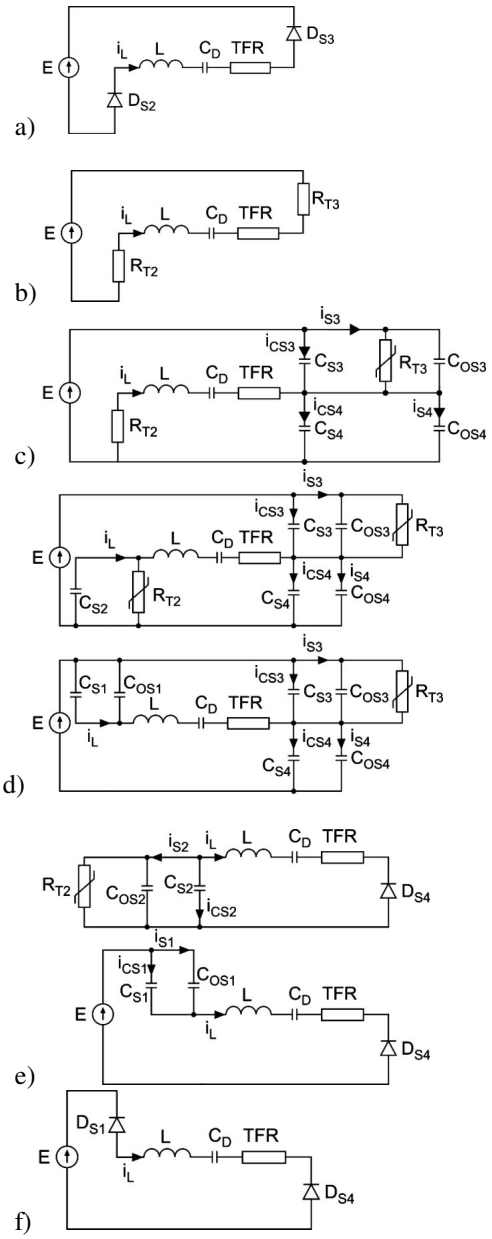


Fig.4. Resonant circuits of the ZVS bridge MRC a) for ($t_1 \le t \le t_2$), b) for ($t_2 \le t \le t_4$), c) for ($t_4 \le t \le t_6$), d) for ($t_6 \le t \le t_7$), e) for ($t_7 \le t \le t_9$), f) ($t_9 \le t \le t_{10}$)

In the time interval ($t_9 \le t \le t_{10}$), the energy stored in L maintains conductance of the resonant current i_L at f_{01} in the circuit: L, C_D, TFR, D_{S4}, E, D_{S1}. At the instant $t=t_{10}$, the control signals u_{GS1}, u_{GS4} initiate the second half of the converter's operation. Electromagnetic phenomena in this second half are analogous with those in the first half of the operation.

The analysis for $0<\gamma<1$ indicates, that three values of resonant frequency: f_{01}, f_{02}, f_{03} can occur as configuration of the resonant circuit changes. At $\gamma=1$, transistors of the same leg, e.g. T_2, T_3, turn off at the same moment. The resonant circuit operates at only two frequencies: f_{01} and f_{03}, then. If values of γ are small (at $\gamma\approx0$), the current of C_{S2} may reach zero before C_{S3} starts conducting. In the event, the resonant circuit operates at two frequencies: f_{01} and f_{02}.

ZVS MRC is characterized by conversion ratio M (output voltage in relative units), which is expressed:

$$M = \frac{U_o}{E} \tag{5}$$

5. RESULTS OF SIMULATION TESTING OF THE ZVS BRIDGE MRC

Multiresonant ZVS bridge was subject to simulation testing with Simplorer programme. The model of simulation circuit shown in Figure 5 consists of MOSFET IRFP460 transistor (output capacitance C_{OS}=870pF), HFA25TB60 fast recovery diode (junction capacitance C_{OD}=100pF) made by International Rectifier, and SPIRO TFR1P2W2 transformer (leakage inductance L_S=0,58μH, main inductance L_M=3,34μH). Beside the transformer, the resonant circuit comprises: L=3μH, $C_{S1}=C_{S2}=C_{S3}=C_{S4}$=7nF, C_D=23nF, C_F=1μF, R=30Ω or 60Ω. Resonant frequency f_0=400kHz. Supply voltage E=20V DC.

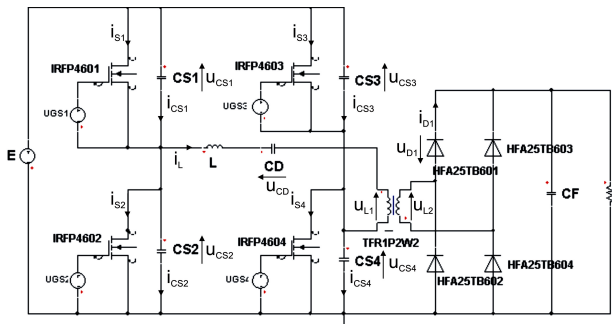


Fig.5. Simulation model of ZVS bridge MRC

On the basis of simulation testing, it was concluded that at f lower than the resonant frequency f_0, ZVS operation does not occur. In the vicinity of $f= f_0$, the system's operation meets ZVS criteria at high transistor currents of around 25A. Due to the range of output power regulation, simulation testing was performed at $f \ge$ 440kHz.

Based on results of simulation testing, the area of converter's operation were defined as β=f(f), where R=30Ω, γ=1, γ=0.5, γ=0 (Fig.6a) and R=60Ω, γ=1, γ=0.5 γ=0 (Fig.6b). The area determines the ranges of: f and β for which ZVS criteria are obtained at γ=const. β reaches its minimum β_{min} and maximum β_{max} at constant f. At R=const, γ=const, f=const, in the range $\beta_{min} \le \beta \le \beta_{max}$ selected values of: conversion ratio M, maximum voltage in semiconductor elements U_{SCmax}, U_{Dmax}, and maximum transistor currents I_{Smax} vary only slightly. The efficiency η reduces by 1÷3% as β climbs, at f=const. For γ=var, the frequency ranges of ZVS operation, $f_{min} \le f \le f_{max}$, are variable. The boundary frequency f_{max} tends to decrease as γ reduces.

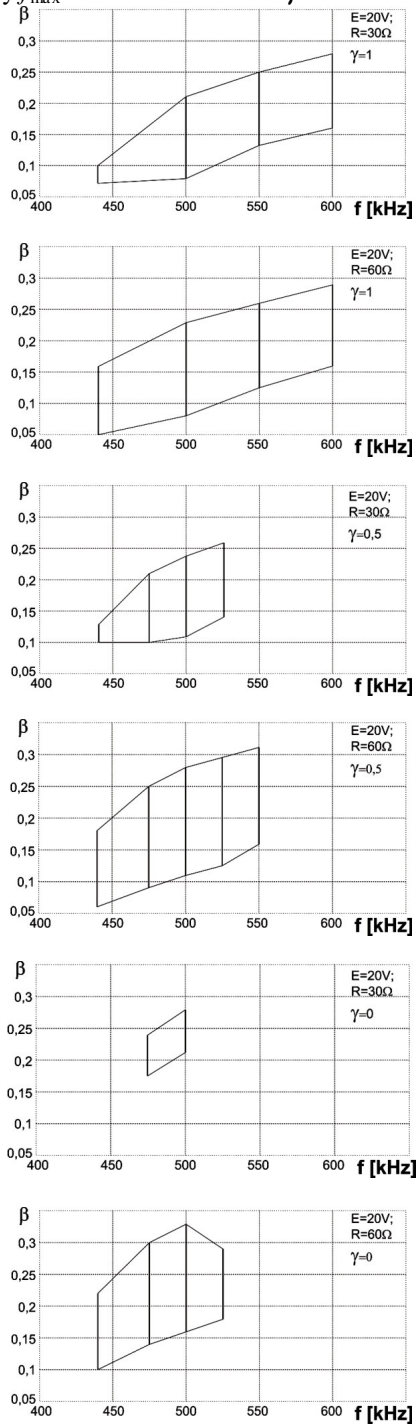
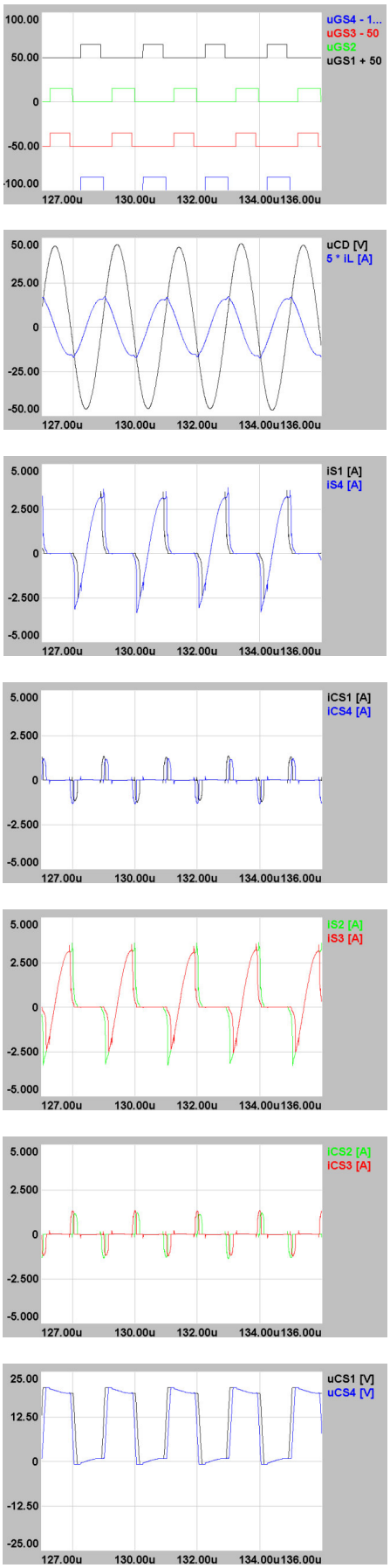


Fig.6. ZVS operation area of the bridge converter for a) R=30Ω, b) R=60Ω



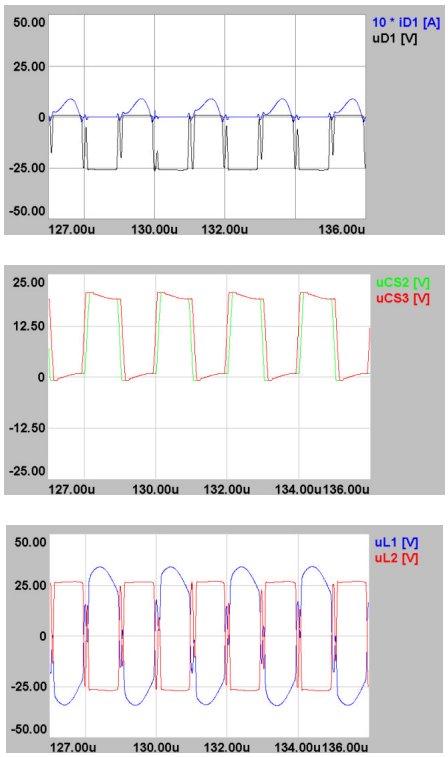
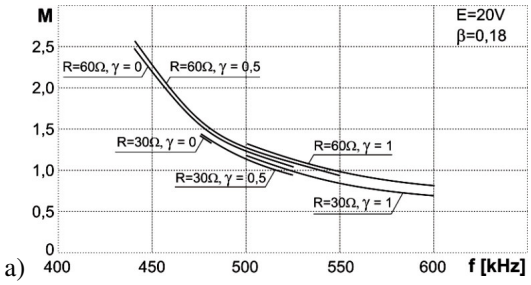


Fig.7. Current and voltage waveforms in ZVS bridge MRC, R=60Ω, f=500kHz, β=0.18, γ=0.5

Figure 7 illustrates selected current and voltage waveforms in the state of operation at f=500kHz, β=0.18, and γ=0.5. Transistors are turned on when diodes D_S are conducting, at $u_{CS}=u_{DS}$. At turn-on and turn-off of the transistors, slight oscillations of transistor currents i_S occur, due to capacitances C_{OS}.

Figure 8 presents selected control characteristics obtained in simulation testing: $M=f_1(f)$, $I_{Smax}=f_2(f)$, $U_{CSmax}/E=f_3(f)$, $U_{CDmax}/E=f_4(f)$ for the f and factors β, γ, at which ZVS operation of the converter is obtained. Growth of γ increases the frequency f range of the circuit's operation at R=const, β=const. Increase of R and γ causes growth of M, U_{Dmax}, I_{Smax}. Maximum voltage across the transistors U_{CSmax} is constant, $U_{CSmax}=E+u_{DS}$, which is an advantage of the converter under analysis.



a)

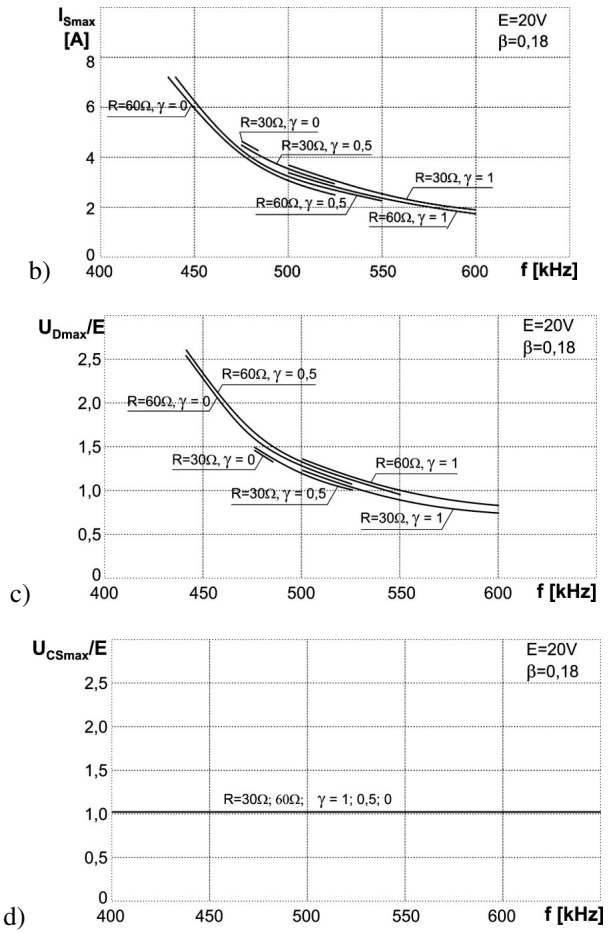
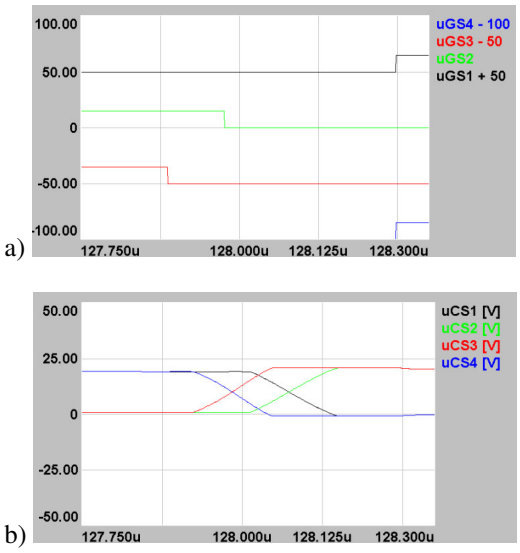


Fig.8. Control characteristics of the ZVS bridge MRC, at R=30Ω, R=60Ω, γ=1, γ=0,5, γ=0 a) conversion ratio M, b) maximum transistor current I_{Smax}, c) maximum diode voltage U_{Dmax}/E, d) maximum transistor voltage U_{CSmax}/E



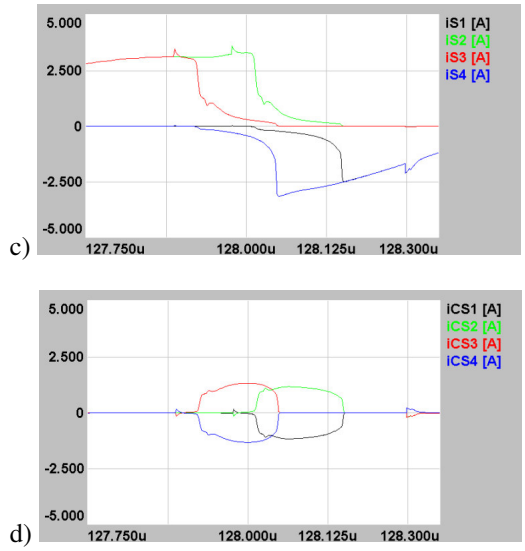
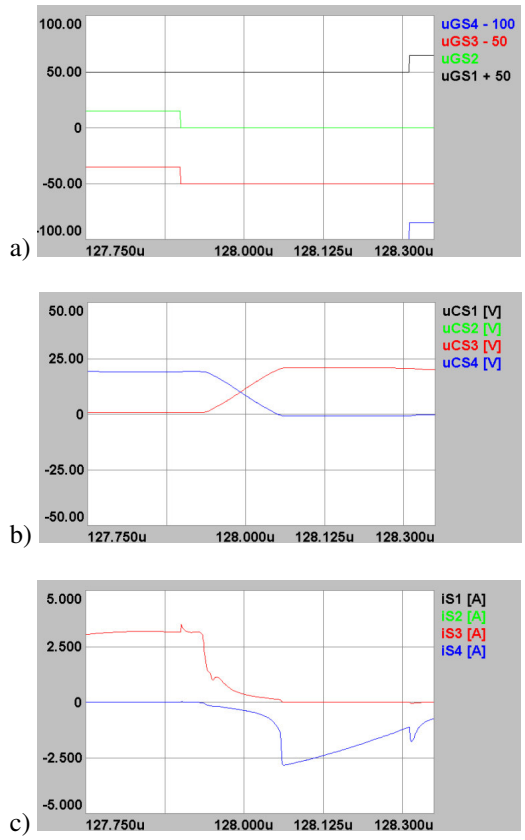


Fig.9. Current and voltage waveforms during transistor switching, at; γ=0.5, β=0.18, f=500kHz, R=60Ω a) control signals, b) transistor voltages, c) transistor currents, d) snubber capacitors currents

Figure 9 shows current and voltage waveforms in the converter at γ=0.5 when T_3, T_2 are turned off and T_1, T_4 are turned on. In the case under discussion, three resonant frequencies: f_{01}, f_{02}, f_{03} occur in the converter.



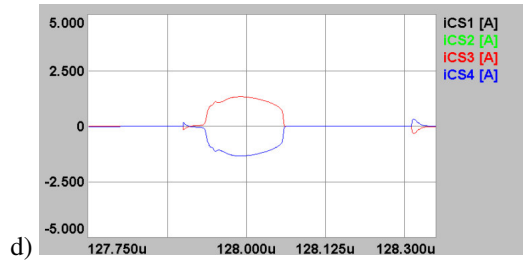


Fig.10. Current and voltage waveforms during transistor switching; γ=1, β=0.18, f=500kHz, R=60Ω a) control signals, b) transistor voltages, c) transistor currents, d) snubber capacitors currents

Figure 10 shows current and voltage waveforms in the converter at γ=1 when T_3, T_2 are turned off and T_1, T_4 are turned on. In transition processes, two resonant frequencies: f_{01}, f_{02}, occur in the converter.

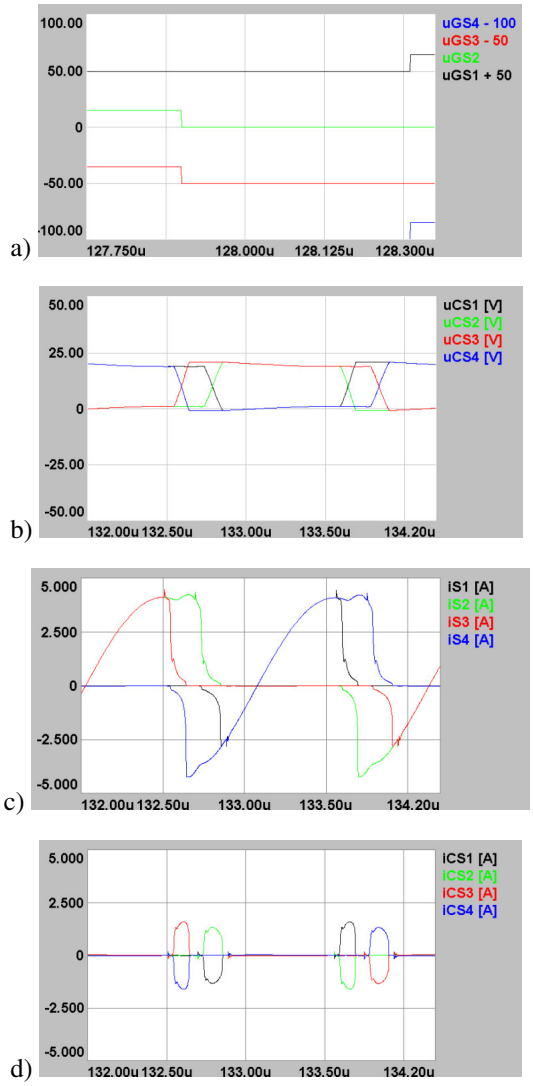


Fig.11. Current and voltage waveforms during transistor switching; γ=0, β=0.18, f=475kHz, R=60Ω a) control signals, b) transistor voltages, c) transistor currents, d) snubber capacitors currents

Figure 11 shows current and voltage waveforms in the converter at γ=0 when T_3, T_2 are turned off and T_1, T_4 are turned on. In transition processes, two resonant frequencies: f_{01}, f_{02}, occur in the converter.

Figure 12 illustrates total power losses P_T+P_D in semiconductor elements of the converter. Simulation testing results indicate that P_T+P_D equal conduction losses in semiconductor components. Switching losses in the transistors and the diodes are negligible. As f grows, transistors and diodes conduction losses reduce owing to lower current values in the circuit.

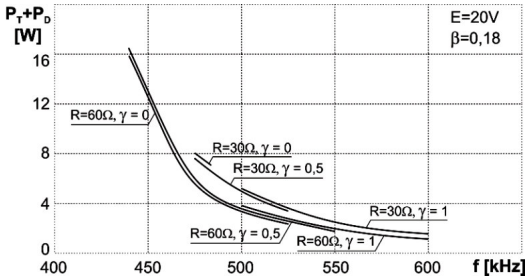


Fig.12. Total power losses in semiconductor elements of the ZVS bridge MRC

The converter's efficiency η is about 80% and slightly increases as γ and f climb. Growth of R causes η to decline (Fig.13).

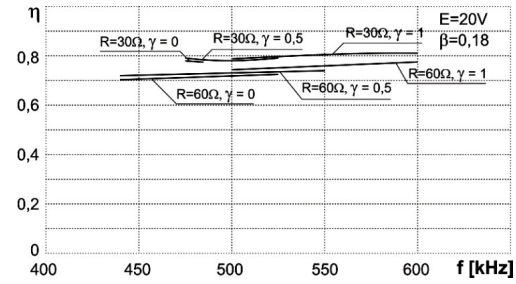


Fig.13. Efficiency η of the ZVS bridge MRC

Figure 14 presents the converter's output power P_{out} as a function of frequency f. Growth of: f and R, and reduction of γcause a decrease in P_{out}.

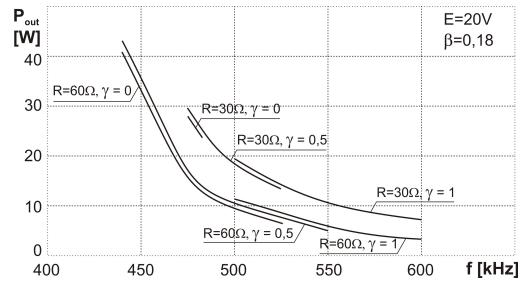


Fig.14. Output power P_{out} of the ZVS bridge MRC

6. CONCLUSION

The simulation testing of the bridge converter leads to the conclusions:

1. The ZVS operation of the converter is realized in the control area defined by: β (modulation factor of delay time Δt_S), Δt_S (delay time), γ (delay factor of control signals), and operating frequency f. At $\gamma \neq 1$, the control of f is the most extensive. Decrease of γ restricts the range of f control.
2. Presence of the separation transformer in the converter's topology poses great difficulty for calculation of mathematical dependences determining elements of the resonant circuit, which also includes charge elements of the transformer. The author proposes a method of selecting elements on the basis of simulation using computer software, e.g. Simplorer, through the following stages:
   - Determination of elements of the resonant circuit L, C_D,
   - Determination of transformer leakage and main inductances,
   - Choice of R of the transformer's load without a bridge rectifier in order to obtain the desired output power,
   - Choice of the output filter C_F,
   - The element values should be verified with simulation waveforms to confirm ZVS operation of the converter.
3. The control algorithm should ensure:
   - Safe operation of the converter where control signals are separated from one another (including t_{on}, t_{off}) so that transistors do not short-circuit,
   - ZVS converter's operation,
   - Obtaining of maximum converter efficiencies.
4. The output power of the system is defined by mean current of the transistor. Transistor voltage, approximately equal to the supply voltage, is not a criterion of its selection. Thus, the output power is enlarged as the value of supply voltage increases.
5. Maximum converter efficiencies obtained on the basis of simulation are about 80%. Compared to converters including only one transistor, efficiency of the circuit under analysis is lower by about 10%, which constitutes its disadvantage. The greater losses across the converter result from presence of greater numbers of semiconductor elements. The results provide evidence against using bridge converters in low-power applications.
6. A serious drawback of the converter including galvanic separation is involvement of elements on the transformer's secondary side in the series resonant circuit. This causes:
   - Variation of resonant frequency at different values of these elements,
   - Reduced quality factor of the resonant circuit.

   In consequence, there is a reduction of the output power and ZVS operation area of the circuit.

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