EXPERIMENTAL ANALYSIS OF COMMUTATION PROCESS OF POWER SEMICONDUCTOR TRANSISTOR'S STRUCTURES

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Summary The paper deals with testing device designed for experimental examination of processes in power electronics devices during various switching modes is described. Through the use of auxiliary circuits additional switching modes (ZVS, ZCS) are realized except hard switching, and turning-off with reduced current respectively. The device´s advantage is possibility of fine dead time setting, allowing us analyzing the effects of phenomenon noted above, on measurements of commutation losses.

1. INTRODUCTION

Current tendencies on field of power semiconductor devices is characterized by increasing of efficiency (reducing of losses) and power density (decreasing of volume). This means contradictory tendencies because increasing the power density is realized by increasing the switching frequency, what results in increase of commutation losses.

The possible solution is using of soft switching commutation, realized by auxiliary circuit, or more perfectly, by utilization of parasitic elements of main´s circuit. In the case of semiconductor devices, these parasitic elements are internal capacitors, while in transformers it is its leakage inductance, often modified with specific construction of magnetic circuit [3].

Efficiency of soft switching application and therefore selection of correspondent commutation mode is dependent on properties of concrete power semiconductor device. Even if exist some specific known general standards (rules) which we can specify for example by computer simulation, the final acknowledgement of advantage of specific commutation technique have to be realized by experimental way. Standard progress expects measuring on prototype or in better case on physical converter model. Potential change of main´s circuit parameters is technically difficult and introduces additional cost of equipment´s development.

2. SPECIFICATION OF DEVICE´S PROPERTIES

The standard methods of experimental examination of specified commutation technique have some disadvantage, which lead us to construct universal testing device designed for measuring of the losses generated by semiconductor devices during various commutation modes. The main criterion was its ability of use as well as in research and pedagogical process. This mentioned specifications define simplicity of service, accuracy and reproducibility of measurement and possibility to choose commutation technique with variable dead-time.

Primary requirement was to gain exact emulation of different soft – switching techniques and consecutive interpretation of generated switching loss. Proposed topology of main circuit look like half – bridge inverter modificated by additional circuits, which serves to realize required commutation technique (Hard switching, ZVS, ZCS). Generator of gate impulses has to have possibility of optional and gently – adjustable dead – time. Measuring of losses generated by semiconductor device, the method of calculation the instantaneous power is being used. Construction of whole testing device has been issued from requirement of its application like teaching instrument (understanding of processes of semiconductor devices during various commutation techniques) and also as research instrument for choosing the optimal switching technique characterized by minimal losses of semiconductor device.

3. DESCRIPTION AND PRINCIPLE OF OPERATION DEVICE

Principle schematics is shown on *Fig. 1.* Circuit consist of main sub - circuit, auxiliary sub - circuit, filtration capacitor´s battery and actuators of power elements. Resonant circuits for emulation soft switching method are designed on several boards. It is possible to use three values of resonant level, for measuring at three different frequencies. Simultaneously are being used as passive part of resonant converter, which together with testing elements in main sub - circuit and load can form real resonant converter in various modifications [1]. The main sub – circuit consists of tested elements (Q1, Q2). Auxiliary sub – circuit (Qaux1, Qaux2) serves to create various operative conditions for main sub - circuit elements, especially for testing recuperative energy stored in parasitic capacitance of measured element. It is possible to emulate some new switching techniques – turning off at reduced current, turn off using auxiliary element etc. For

described purposes it is important to generate exact waveforms with rapid increase and decrease of current. Therefore is auxiliary branch shouldered by MOSFET transistors (MTW10N100E).

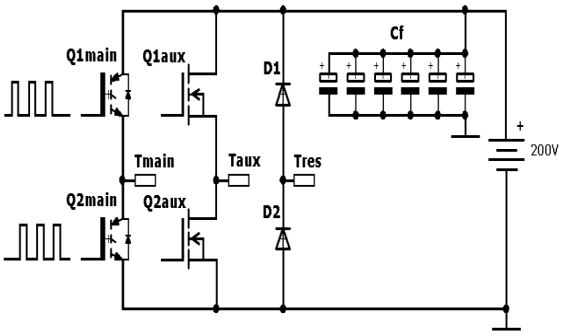

Figure 1: Principle schematics of main circuit

Actuator´s schematic is shown on *Fig. 2.* Core of this sub – circuit is integrated circuit MC33153 designed by ON SEMICONDUCTOR in basic application [4]. Problem which is well - known as galvanic connection between control and power circuits is eliminated by fast opto - couplers 6N137.

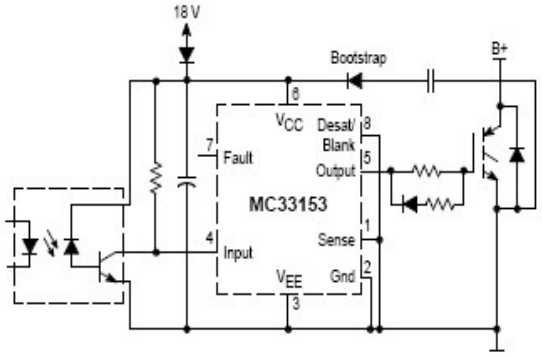

Figure 2: Actuator´s schematics for basic application

Control circuit is designed with reference to actual requirements, which are outcome from executed experiments. One of the most up to date 16 bit digital signal processor (MOTOROLA 56F8013) is used. This processor, that is primary developed for control of converters, is characterized by high calculating rating, fast peripherals and full controlled PWM modulators with switching frequency up to 96 MHz [2]. Control circuit must ensure correct pulse sequence in next modes of operation: hard switching (initial measurement, used as reference for other techniques), measuring of recuperative capacitance energy W_{KAP}, standard ZCS technique (applied in Clamped Voltage Series Resonant Converter) and ZVS technique (emulated with RL load circuit). Each of these techniques needs different control algorithms, which must ensure high flexibility of control. Control circuit provides optional switching frequency for various types of components and allows us to fine set up of dead time, with minimal step size 10 ns. Control circuit also prevents simultaneous conducting of both transistors in one leg, consequently the safety start of testing device is ensured.

4. EXPERIMENTAL RESULTS

This experiment has been realized at 25 kHz (10% of dead time) of switching frequency with input voltage of 100V. *Fig. 3* shows waveforms of current, voltage and instant power of measured transistor (IRG4PH40KD) at hard switching mode. We can see that the amplitude of instant power reaches 400W. This value can be eliminated using different switching mode. After realization of another switching techniques (Zero voltage, Zero current switching – *Fig. 4, Fig. 5*), the measured waveforms shows minimalization of power loss during turn-off process at Zero current switching at *Fig. 5.* This experimental result shows, that the best switching mode for measured device should be Zero current switching.

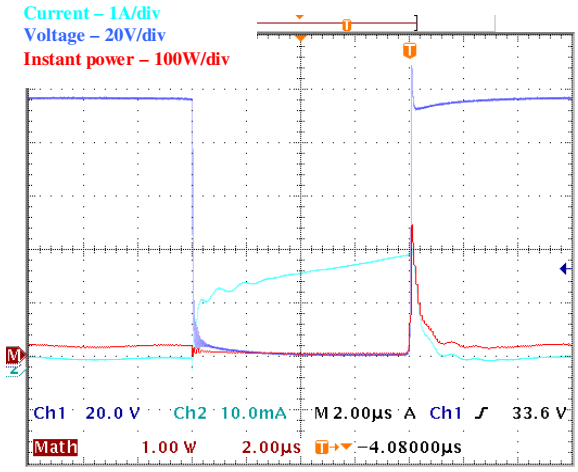

Figure 3: Hard-switching technique

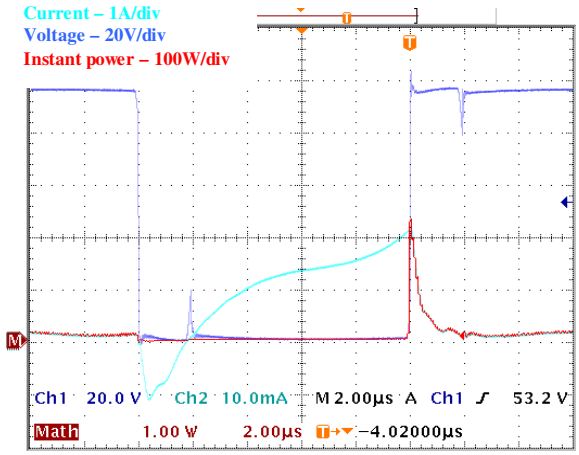

Figure 4: Zero – Voltage switching

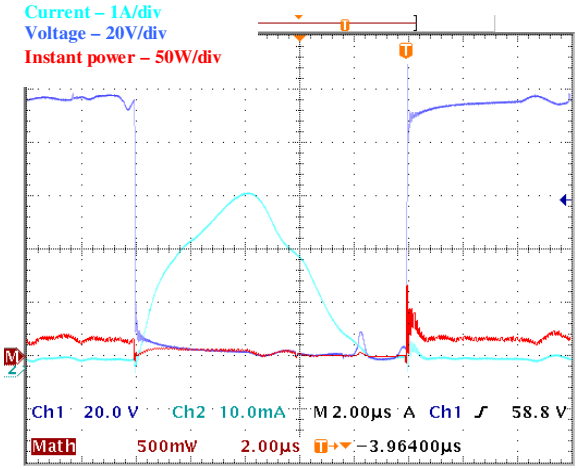

Figure 5: Zero – Current switching

There is also possibility of calculating each data using equation (1), that enables evaluate energy losses which are generated in transistor structure during switching cycle.

$$P_{TOT} = \frac{1}{T} W_{CON} + \frac{1}{T} W_{ON} + \frac{1}{T} W_{TOFF} + \frac{1}{T} W_{OFF} =, \quad \frac{1}{T}\left[W_{CON} + W_{ON} + W_{TOFF} + W_{OFF}\right] \quad (1)$$

where

P_{TOT} – total power loss during switching cycle
W_{CON} – conduction energy losses
W_{ON} – energy losses generated during turn – on process
W_{TOFF} – energy losses generated during turn – off process
W_{OFF} – energy losses generated during stabilized off state
T – time period of computed action

For calculating the apportionable parts of expression (1) next equations have to be used.

$$W_{CON} = W_{OFF} = \int_{t_1}^{t_2} u_P(t)\, i_P(t)\, d$$

$$= \int_{t_1}^{t_2} (U_T + R_D\, i_P) i_P\, dt = \int_{t_1}^{t_2} U_T\, i_P\, dt + \int_{t_1}^{t_2} R_D\, {i_P}^2\, dt \Rightarrow$$

$$W_{CON} = W_{OFF} = U_T \int_{t_1}^{t_2} i_P\, dt + R_D \int_{t_1}^{t_2} {i_P}^2\, dt\,, \quad (2)$$

where

U_T - transistor's threshold voltage
Ip - time function of current flowing through the transistor
R_D - internal resistance of transistor
$t1$ – initial time of stabilized conductivity/non-conductivity of device
$t2$ – final time of stabilized conductivity/non-conductivity of device

$$W_{ON} = W_{TOFF} = \int_{t_1}^{t_2} i_P(t)\, u_P(t)\, dt\,, \quad (3)$$

where

ip – time function of device's current
up – time function of device's voltage
$t1$ – initial time of turn – on/off process
$t2$ – final time of turn – on/off process

Because measured data (current, voltage) from oscilloscope mostly aren't in form of (2) or (3), it is necessary to use a discrete form of equations (2) and (3) as shown in expression (4).

$$W = \sum_{i=T_{Z1}}^{T_{Z2}} I_P[i]\, U_P[i]\, \Delta T\,, \quad (4)$$

where

T_1 – is sequence of sample at the begin of process (turn – on/off, stabilized conductivity/non-conductivity of device)
T_2 – is sequence of sample at the end of process (turn – on/off, stabilized conductivity/non-conductivity of device)
$I_P[i]$ – i-sample of current through device
$U_P[i]$ - i-sample of device's voltage
ΔT – sampling time

5. CONCLUSION

Practical experiences with testing device confirmed its utilization in experimental part of pedagogic process and research activities of our department. Its major advantage is demonstrative representation of effects of various switching techniques on power losses in power semiconductor device. Another advantage is possibility of changing the dead time with minimal step, which allows high accuracy analyzing impact of previously described phenomenon on power losses and character of electromagnetic events in circuit. Practical utilization of this knowledge is especially in the field of drivers and commutation techniques optimalization.

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