MATEC Web of Conferences **97**, 01059 (2017) DOI: 10.1051/matecconf/20179701059
ETIC 2016

Influence of Material Properties on the Fluid-Structure Interaction aspects during Molded Underfill Process

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Abstract. This paper presents the investigation of the effects of epoxy moulding compound' (EMC) viscosity on the FSI aspects during moulded underfill process (MUF). Finite volume (FV) code and finite element (FE) code were connected online through the Mesh-based Parallel Code Coupling Interface (MpCCI) method for fluid and structural analysis. The EMC flow behaviour was modelled by Castro-Macosko model, which was written in C language and incorporated into the FV analysis. Real-time predictions on the flow front, chip deformation and stress concentration were solved by FV- and FE-solver. Increase in EMC viscosity raises the deformation and stress imposed on IC and solder bump, which may induce unintended features on the IC structure. The current simulation is expected to provide the better understandings and clear visualization of FSI in the moulded underfill process.

1 Introduction

Transfer moulding is a well-known technique used for the integrated circuit (IC) encapsulation. The feeding of the epoxy-moulding compound (EMC) is transferred from the transfer pot to the mould cavity, which consists of the IC chip. The interaction between EMC and IC structures (i.e., silicon chip, solder bump, wire bonding, paddle and lead-frame) may induce unintended defects; hence, reduces packaging reliability. Although the IC encapsulation technology is quite mature, it is still not widely applied in moulded underfill (MUF) package. The encapsulation of the miniaturized IC package with a thinned silicon chip and the micro-bump has created the challenges to engineer to sustain the

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package reliability. Therefore, the better understandings and clear visualization of the FSI phenomenon are important for the engineer and package designer, to eliminate the package defects and maintain the package reliability.

The FSI phenomenon in IC packaging was widely reported on the IC package that using wire bonding, lead frame and paddle. However, the investigations of the moulded underfill process for an IC package considering FSI aspect with MpCCI coupling method [1-3] are still lacking. Therefore, the FSI simulation using MpCCI coupling method was considered in the study on an IC package with dimensions of 9 mm × 9 mm × 0.7 mm, which consisting of a silicon chip (5 mm × 5 mm × 0.25 mm) and perimeter arrangement of solder bumps. FV-based and FE-based [4, 5] software were used to solve the fluid flow and structural analyses. EMC flow behaviour was modelled by Castro-Macosko model, which was incorporated into FV-solver by user-defined functions (UDFs) using C language. In the simulation, the flow-induced forces were transferred to FE-solver for simultaneous structural analysis and vice versa. In the current study, the EMC flow front profile, chip and solder bump stress were investigated through the FSI simulation. Three types of EMC [6-8] (e.g., Sumikon EME 6300HN, SUMITOMO 6300 HG) with different material properties, namely Case 1, 2 and 3 were considered in the analysis.

2 Viscosity models

The proper selection of viscosity model is crucial for the simulation of encapsulation process. In the simulation, the encapsulant material was assumed as generalized Newtonian fluid (GNF). The Castro-Macosko model [6, 9] was applied to predict the relationship between the viscosity and degree of polymerization and describe the viscosity of the encapsulant material as follows:

$$\eta(T,\dot{\gamma}) = \frac{\eta_0(T)}{1+\left(\frac{\eta_0\dot{\gamma}}{\tau^*}\right)^{1-n}}\left(\frac{\alpha_g}{\alpha_g-\alpha}\right)^{C_1+C_2\alpha} \quad (1)$$

where

$$\eta_0(T) = B\exp\left(\frac{T_b}{T}\right) \quad (2)$$

B is an exponential-fitted constant, T_b is a temperature fitted-constant, n is the power law index, η_o is the zero shear viscosity, α is the degree of conversion, α_{gel} is the degree of conversion at gel point, and τ^* is the parameter that describes the transition region between the zero shear rate and power law region of the viscosity curve.

Kamal's equation [6, 9] described the curing effect and integrated with the Castro-Macosko model in the current study. The rate of the chemical conversion of the compound in this model can be predicted as follows:

$$\frac{d\alpha}{dt} = \left(k_1 + k_2\alpha^{m_1}\right)(1-\alpha)^{m_2} \quad (3)$$

$$k_1 = A_1\exp\left(-\frac{E_1}{T}\right) \quad (4)$$

and

$$k_2 = A_2\exp\left(-\frac{E_2}{T}\right) \quad (5)$$

where A_1 and A_2 are Arrhenius pre-exponential factors, E_1 and E_2 are activation energies, m and n are reaction orders, and T is the absolute temperature.

3 Results and discussion

3.1 Deformation of silicon chip

Figure 1 shows the simulation results of the FV and FE analyses. The selected flow front advancement at two filling times are presented together with the chip deformation during IC encapsulation process. At filling time 1.4 s, the EMC flow front covered nearly 30% in the top space (upper stream) of the chip. Faster flow front at upper stream has induced the unstable forces acting on the silicon chip. Thus, the silicon chip deformed downwardly as depicted in Figure 1 (Column of FE-solver). Conversely, upward deformation was found at the chip edge that closer to inlet gate. This situation was attributed from the continuous inlet flow. At 3.2s, the filling of the mould cavity is nearly completed. The faster flow front totally covered the chip and resulted in the air trap beneath the chip [10]. The variations of the flow-induced forces on the chip caused the deformation around the middle region, which has no solder bump supported. Consequently, the chip edges deformed upwardly corresponded to the structural reactions.

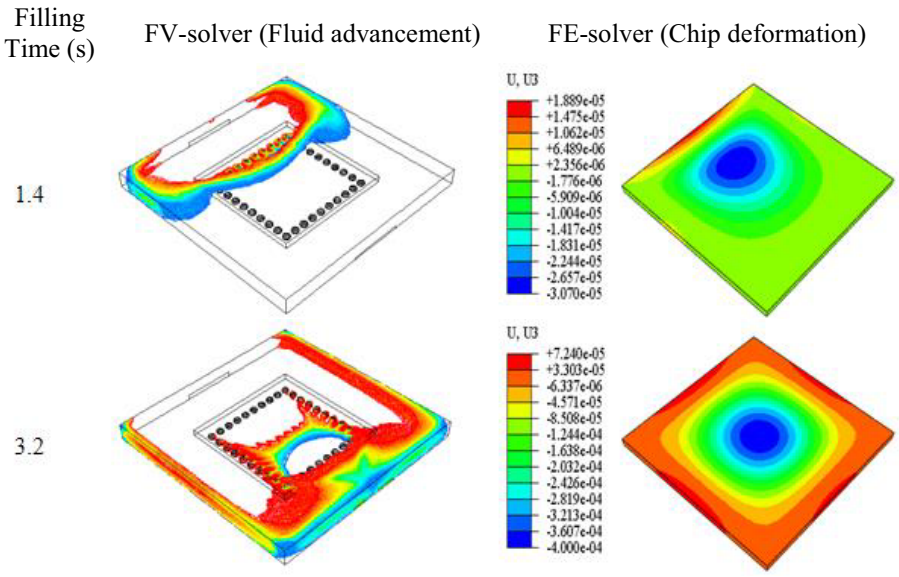

Fig. 1. FSI simulation results of FV-solver (Flow front advancement) and FE-solver (deformation, U in unit: mm)

3.2 Von Mises stress analysis

Aforementioned, the FSI has caused the deformation of the silicon chip. The unintended deformation may reduce the package reliability in the subsequent packaging process. During the encapsulation process, the silicon chip subjected to the stress due to the flow-induced forces. Figure 2 shows the stress distribution profile of the silicon chip at filling times, 1.4 s and 3.2 s. The stress distribution was corresponded to the EMC flow front and

varied with the filling time. Figure 3 depicts the stress concentration on a solder bump. The predicted solder bump experienced higher stress concentration compared with the silicon chip during the process. High stress concentration may cause structure cracking or fracture, if exceeding the yield stress of the solder bump material. Therefore, the proper control, package design and material selection are important to maintain the package reliability. The moulded underfill process was investigated by using different EMC material properties. As illustrated in Figure 4, the IC structure (silicon chip and solder bump) of Case 3 experienced the highest stress. This situation was mainly contributed from the viscosity of the EMC used during the moulded underfill process. Success MUF process at low viscosity regime allows the EMC material flows easily and resulting low stress subjected to IC structure. The variations of the viscosity were found highest for Case 3 followed by Case 2 and Case 1. Case 3 has the highest viscosity at the shear rate regime >300 1/s compared to cases 1 and 2. Thus, the IC structure of Case 3 experienced highest stresses.

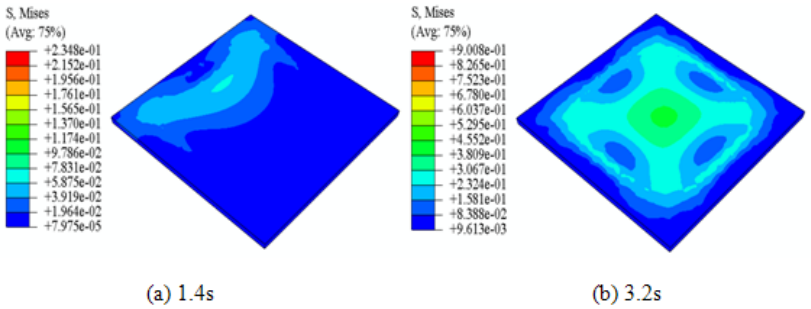

Fig. 2. Stress concentration (Unit: MPa) at silicon chip.

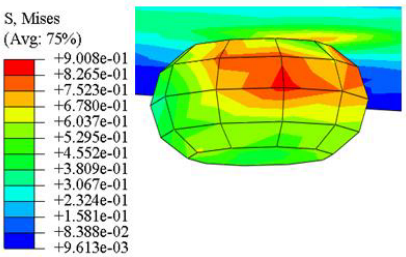

Fig. 3. Stress concentration at the solder bump.

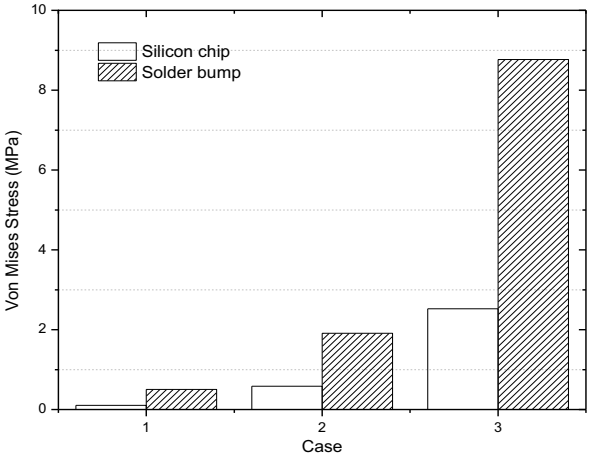

Fig. 4. Stress of silicon chip and solder bump for EMC 1, 2 and 3.

4 Conclusion

The investigation of the effects of material properties by considering the FSI aspects in MUF process has been carried out using finite volume and finite element codes, which coupled by MpCCI software. The FSI phenomenon and stress concentration during the MUF process were predicted through the simulation. The FSI methodology has been well validated. The increase in EMC viscosity raises the stress imposed on the IC structure and void in the package. The highest flow viscosity of Case 3 yield highest stress and void in the package. Extremely high stress and void will cause the deduction of package reliability in the subsequent manufacturing process. The maximum stress of solder bump and silicon chip for Case 3 were 8.8 MPa and 2.5 MPa. The proposed MUF simulation yields the clear visualization of FSI phenomenon and provides better understandings of the process to the engineers and package designers. The extension of this work will focus on the parametric investigations and development of analytical models for predicting the deformation and stress of the IC structure.

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