A Low-Voltage CMOS Buffer for RF Applications Based on a Fully-Differential Voltage-Combiner

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Abstract. This paper presents a new CMOS buffer circuit topology for radio-frequency (RF) applications based on a fully-differential voltage-combiner circuit, capable of operating at low-voltage. The proposed circuit uses a combination of common-source (CS) and common-drain (CD) devices. The simulation results show good levels of linearity and bandwidth. To improve total harmonic distortion (THD) a source degeneration technique is used. The proposed circuit has been designed in a 130nm logic CMOS technology and it achieves a simulated gain of 1.54 dB, a bandwidth of 1.14 GHz for a total power dissipation of 13.34 mW, when driving an RF active probe (with 0.8 pF in parallel with 200 kΩ).

Keywords: buffer, common-source, common-drain, RF, CMOS, low-voltage.

1 Introduction

In recent years, there has been an increasing trend in incorporating complete systems in longer lasting battery-powered equipment which requires low power dissipation circuits 0. Particularly, buffer circuits used as an important functional block of high performance communication systems, e.g. RF applications like drivers of passive switched-capacitor down-converter circuits. Circuit For this purpose is essential to provide good linearity in terms of both output level and intercept-point performance. Provided that the transient response of the buffer is fast enough, which implies a bandwidth greater than 1 GHz, errors will be minimal. Low levels of total harmonic distortion (THD) are also essential for compatibility with communication standards. Moreover, traditionally, buffers present a gain near equal to unit but always with some signal attenuation. Some examples are the elastic source-follower or the enhanced voltage-follower as proposed in 0.

The objective of this paper is to propose a novel voltage buffer based on a voltage-combiner topology, i.e. a common-source/common-drain structure. It achieves a gain that can be designed in the range from0 dB to 6 dB; the input impedance is equally high; and the parasitic capacitance of its inputs is low. For improving THD the source degeneration method has been used. The supply voltage variability was studied for 1.2 V ± 5% for three levels, i.e.,1.14 V, 1.2 V and 1.26 V. Since the voltage gain of

the proposed circuit is higher than the unit, it is expected to compensate for the gain loss due to linearization of the circuit.

2 Internet-Of-Things

The buffer circuit presented in this paper is an essential part of RF transceiver integrated circuits (a paramount building block in modems) and it can be used either for driving a passive down-converter or for on-chip built-in self-testing purposes. This circuit can be used as an interface to environmental data signals collectors such as temperature smart sensors. The circuit reading environmental data, passes the information to an Internet Web server to display temperature information. This way it can contribute to Internet of Things.

3 Proposed Circuit Basic Concept

The basic idea of voltage-combiner (VCOM) technique is depicted in Fig. 1. It basically employs a combination of NMOS transistors in configuration of common-source, M_Y, and common-drain, M_X. High input impedance is equally accomplished.

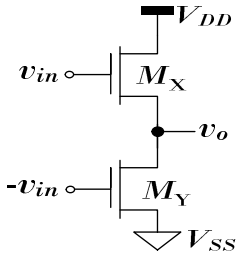

Fig. 1. VCOM circuit conceptual idea.

After simplifying the small signal equivalent (differential-mode, DM) of the VCOM and substituting the components by their Y-parameter equivalents, the behavioral signal path model [3] is extracted and illustrated in Fig. 2 (for simplicity only half the circuit is shown).

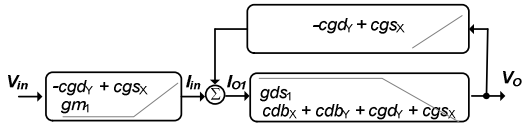

Fig. 2. Behavioral signal path model of the voltage combiner stage (for simplicity only half the circuit is shown).

This model permits large insight in the small-signal behavior of the amplifier and is a fundamental tool in the extraction of the differential gain transfer function. It is

possible to verify: the Miller effect through parasitic capacitance cgd_1, the pole(s) and zero(s), and the order of the transfer function (in this case, 1st order).

Using the behavioral signal path model described in Fig. 2 and writing the equations for I_{O1} and V_O, it is possible to extract the transfer function of the VCOM. For the sake of simplicity, minor simplifications were used in the derived equations:

$$gds_1 = gds_Y + gds_X \tag{1}$$

$$cdb_1 = cdb_Y + cdb_X \tag{2}$$

Body effect of transistors M_Y and M_X has been neglected, for the sake of simplicity, But it can be easily included into the equations.

$$\mathrm{TF}_{VCOM} = \\ = \frac{gm_Y + gm_X + (cgs_X - cgd_Y)\cdot s}{gm_X + gds_1 + (cdb_1 + cgs_X + cgd_Y)\cdot s} \tag{3}$$

From the transfer function it is possible to obtain the low-frequency open-loop gain (DC gain) of the VCOM stage, A_{VCOM},

$$A_{VCOM} = \frac{gm_Y + gm_X}{gm_X + gds_1} \tag{4}$$

considering that $gm_X >> gds_1$, a good approximation can be given by,

$$A_{VCOM} \approx \left(1 + \frac{gm_Y}{gm_X}\right), \qquad |A_{VCOM}| > 1 \tag{5}$$

Sizing the circuit to attain $gm_{13} \approx gm_{12}$, 6 dB are added in the overall DC gain of the amplifier.

Also, the dominate pole, ω_{p1VCOM}, is computed using:

$$\omega_{P1_{VCOM}} = \frac{gm_X + gds_1}{cdb_1 + cgs_X + cgd_Y} \tag{6}$$

The gain-bandwidth product performance parameter of this buffer (GBW) can be expressed by

$$\mathrm{GBW}_{VCOM} = \frac{gm_Y + gm_X}{cdb_1 + cgs_X + cgd_Y}. \tag{7}$$

4 Complete Circuit Description, Linearization and Simulation Results

4.1 Circuit Description

The proposed fully-differential voltage combiner buffer circuit (VCOM) is shown in Fig. 3.

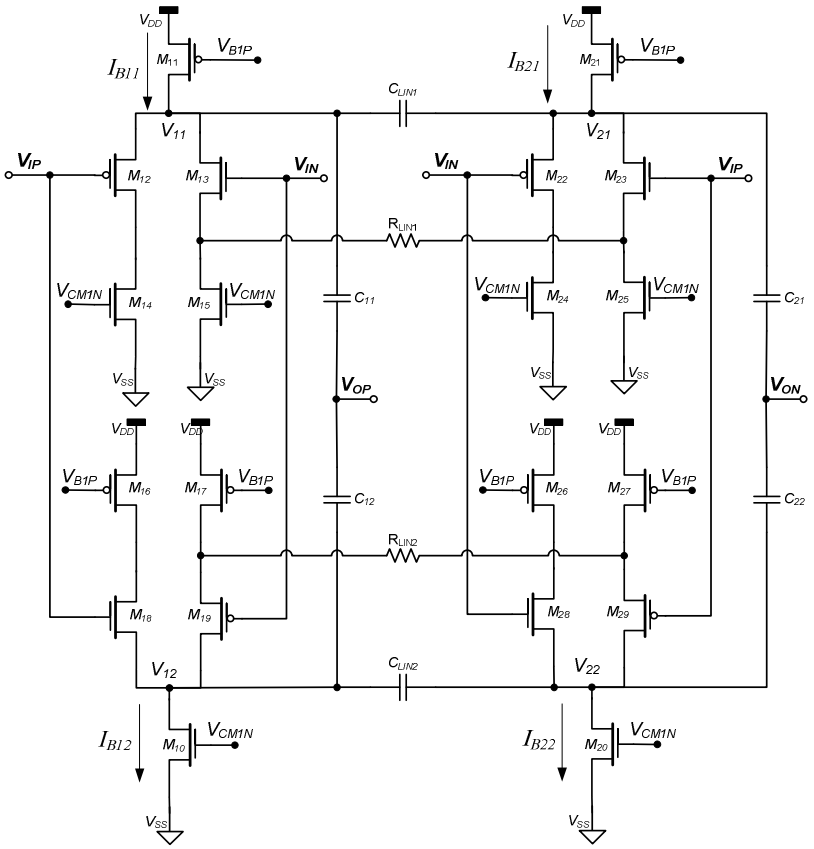

Fig. 3. Proposed input fully differential voltage combiner circuit (VCOM) (Biasing circuitry not shown for simplicity).

It consists of a cross-coupled (i.e. NMOS and PMOS) fully-differential buffer. The differential voltage-combiner is represented by M12, M13, M19 and M18 in CD and CS configurations, respectively. The remaining transistors are simple PMOS current-sources (M11, M16, M17) and NMOS current-sources (M14, M15 and M10). The circuit structure is duplicated to complete the cross-coupled fully-differential circuit. As stated before, in order to linearize the circuit, following the source degeneration resistors presented earlier, two resistors, RLIN1 and RLIN2, were added

to improve the THD of both the odd and even harmonics. Furthermore, two capacitances, CLIN1 and CLIN2, were also added to filter the even harmonics. For the output signal AC coupling were used four capacitances: C11, C12, C21, and C22. To minimize the power consumption and area, transistors widths and current in the biasing circuit are scaled down by a factor of ten with respect to the main amplifier circuit.

4.2 Linearization Technique

Nonlinearity of the MOS transistors limits the circuit linearity (dynamic related with THD) between -40 dB and -60 dB [4]. In order to reach better linearity performance, resistor-based degeneration can be used [5]. The resistive source degeneration (RLIN1 and RLIN2) method is used to enhance the linear range of the transconductor (CS devices, M13, M23, M19 and M29, operating in a degenerated differential-pair fashion) circuit through transconductance reduction. The degeneration resistor increases the source terminal of the transistors, reducing the drain current [6]. Furthermore, in order to reduce odd harmonics, capacitive coupling has also been employed (through capacitors CLIN1 and CLIN2).

4.3 Simulation Results

The circuit proposed here (the circuit shown in Fig. 1) was designed in a 130 nm high-speed CMOS technology (Lmin = 120 nm). The mobility and threshold parameters (Level 2), KN, KP, VTN and VTP parameters of the devices are, respectively, 525 mAV-2, 145 mAV-2, 0.38 V and -0.33 V. For VCMI, the value of 550 mV was used. The linearization elements, source degeneration resistors are 75 Ω and the capacitances are 0.2 pF. Three voltage values were used as supply voltage of the circuit: 1.14 V, 1.2 V, and 1.26 V.

Table 1 shows the summary of the simulation results of the relevant performance parameters.

Table 1. Key simulated performance parameters

Technology	130 nm
Supply Voltage	1.2 V
DC Gain	1.54 dB
f_{-3dB}(@ *CL* = 0.8 pF and *RL* = 200 kΩ)	1.14 GHz
Total input capacitance, C_{pi}	89.64 fF
Total current	11.40 mA
Total power dissipation	13.34 mW

The simulation results were obtained using HSPICE simulator. In nominal conditions, using a supply voltage of 1.2 V, the simulated amplifier achieves a DC gain of about 1.54 dB, a bandwidth with a frequency cutoff, f_{-3dB}, of 1.14 GHz and a power dissipation of 13.34mW.

Figure 4 shows the bode plot indicating the DC gain and bandwidth for a voltage supply of 1.2 V, 1.54 dB and 1.14 GHz, respectively. In order to compare the key performance parameters (KPP) of the buffer over a wide positive-power supply variation [1.14 V to 1.26 V]: distortion (THD) (Fig. 5), DC Gain (Fig. 6), cutoff bandwidth (Fig. 7) and dissipated power (Fig. 8). The KPP results are evaluated for the linearized circuit, which employs resistive and capacitive source degeneration (Fig. 3).

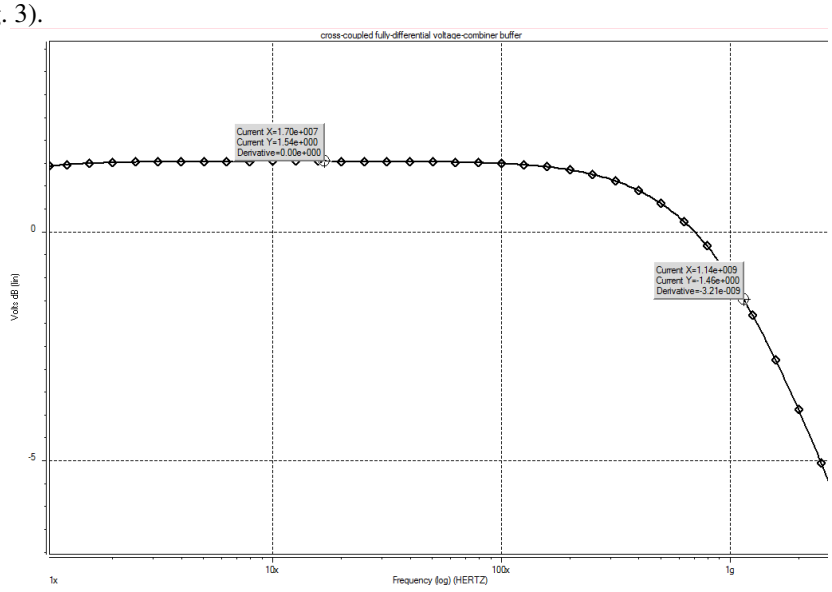

Fig. 4. Bode Plot @ Vdd = 1.2 V.

Figure 5 shows the results of the THD of the linearized circuit for a fully differential input signal range from 20 mV to 400 mV with an input frequency of 250MHz.The |THD| value is above 42 dB for input amplitude voltage until 120 mV and a supply voltage of 1.26 V. For a supply voltage of 1.14 V the input amplitude voltage can go up to 200 mV for the |THD|. The circuit presents a better THD value for lower supply voltage.

The DC gain increases approximately logarithmically (i.e. linearly in dB) with the supply voltage, from 0.66 dB to 2 dB, as shown in the Fig. 6.

Figure 7 displays the cutoff bandwidth results. The better results are for the lower power supply voltage. Also, the input signal amplitude does not influence the bandwidth result. The power dissipation is only dependent on power supply voltage, as expected. Figure 8 shows that higher supply voltages originate higher power supply losses. Again, the variation of input signal amplitude does not influence the power dissipation.

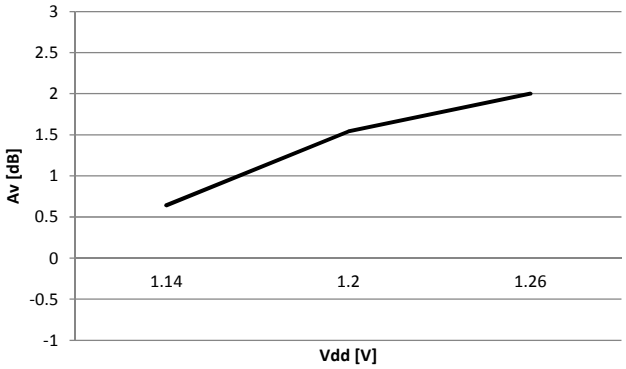

Fig. 6. Low-frequency (DC) gain vs. supply voltage.

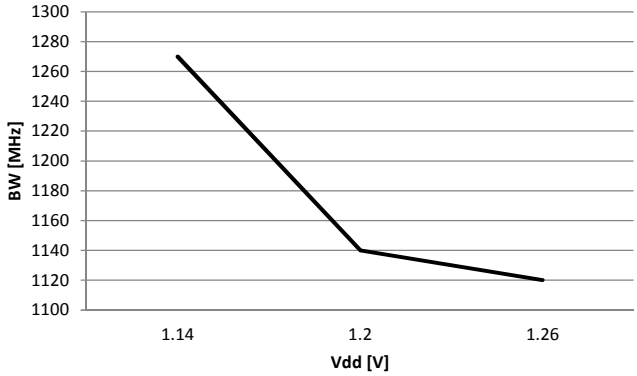

Fig. 7. Cutoff bandwidth vs. supply voltage.

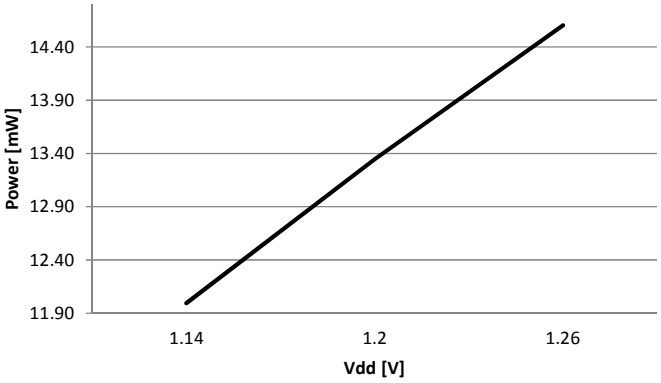

Fig. 8. Power dissipation vs. supply voltage.

5 Conclusions

This paper presented a new CMOS buffer circuit topology for RF applications based on a fully-differential voltage-combiner circuit, operating at low-voltage. The proposed circuit uses a combination of CS and CD transistors. The simulation results show good levels of linearity and bandwidth. For improved THD the source degeneration method was employed. Using the proposed CS and CD fully-differential structure, the circuit achieves, in nominal conditions, a simulated gain of 1.54 dB, a bandwidth of 1.14 GHz for a total power dissipation of 13.34 mW.

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